ADCS747x 1MSPS、12ビット、10ビット、および8ビットのA/Dコンバータ

1 特長

- 可変電力管理
- 6ピンSOT-23パッケージ
- 電源をリファレンスとして使用
- 単一の2.7V～5.25V電源で動作
- 対応規格: SPI™、 QSPI™、 MICROWIRE™、DSP
- 主な仕様
  - 欠損コードなしでの分解能(12ビット、10ビット、8ビット)
  - 変換速度: 1MSPS
  - DNL: 0.5、-0.3LSB (標準値)
  - INL: ±0.4LSB (標準値)
  - 消費電力:
    - 3V電源: 2mW (標準値)
    - 5V電源: 10 mW (標準値)

2 アプリケーション

- 車載用ナビゲーション
- FAまたはATM機器
- ポータブル・システム
- 医療機器
- モバイル通信
- 計測および制御システム

3 概要

ADCS7476、ADCS7477、ADCS7478デバイスは低消費電力のモノリシックCMOSの12、10、および8ビットA/Dコンバータで、1MSPSで動作します。ADCS747xデバイスは、アナログ・デバイセズ製のAD747xに置き換えて使用可能です。各デバイスは、逐次比較型のアーキテクチャをベースとし、内部的なトラック・アンド・ホールドを行います。シリアル・インターフェイスは、SPI、QSPI、MICROWIREなどいくつかの標準、および多くの一般的なDSPシリアル・インターフェイスと互換性があります。

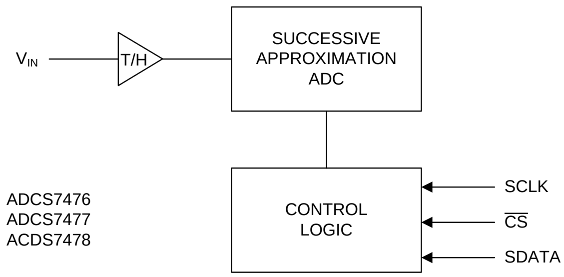
ADCS747xは電源電圧をリファレンスとして使用するため、0からV_{DD}までのフルスケール入力電圧範囲で動作できます。変換速度は、シリアル・クロック(SCLK)の速度により決定されます。これらのコンバータにはシャットダウン・モードが存在し、消費電力とスループットの適切なバランスを実現するために使用できます。ADCS747xは2.7V～5.25Vの範囲の単一電源で動作します。連続的な変換時の通常の消費電力は、3Vまたは5Vの電源を使用するとき、それぞれ2mWまたは10mWです。パワーダウン機能はチップセレクト($\overline{CS}$)ピンで有効になり、5V電源を使用している場合に消費電力が5µW未満に低下します。これら3つのコンバータはすべて6ピンのSOT-23パッケージで供給され、占有面積が極めて小さいため、容積の制限が非常に厳しいアプリケーションに使用できます。これらの製品は、車載および拡張工業用温度範囲の−40°C～125°Cで動作するよう設計されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ADCS7476 ADCS7477 ADCS7478	SOT-23 (6)	1.60mm×2.90mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

ブロック図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (March 2013) から Revision G に変更 **Page**

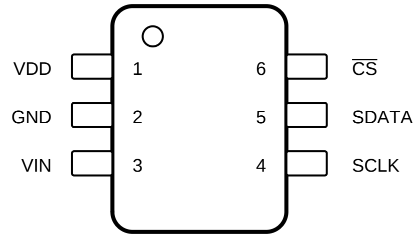
- 「*ESD定格*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- Moved V_{DD} from the *Electrical Characteristics* tables to the *Recommended Operating Conditions* table ... 5

Revision E (March 2013) から Revision F に変更 **Page**

- ナショナル セミコンダクターのデータシートのレイアウトをTIフォーマットへ 変更 ... 1

5 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Not to scale

Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	V_{DD}	P	Positive supply pin. These pins must be connected to a quiet 2.7-V to 5.25-V source and bypassed to GND with 0.1-µF and 1-µF monolithic capacitors placed within 1 cm of the power pin. ADCS747x uses this power supply as a reference, so it must be thoroughly bypassed.
2	GND	G	The ground return for the supply.
3	V_{IN}	I	Analog input. This signal can range from 0 V to V_{DD}.
4	SCLK	I	Digital clock input. The range of frequencies for this input is 10 kHz to 20 MHz, with ensured performance at 20 MHz. This clock directly controls the conversion and readout processes.
5	SDATA	O	Digital data output. The output words are clocked out of this pin by the SCLK pin.
6	$\overline{CS}$	I	Chip select. A conversion process begins on the falling edge of $\overline{CS}$.

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

	MIN	MAX	UNIT
Supply voltage, V_{DD}	–0.3	6.5	V
Voltage on any analog pin to GND	–0.3	V_{DD} + 0.3	V
Voltage on any digital pin to GND	–0.3	6.5	V
Input current at any pin (except power supply pins)		±10	mA
Soldering temperature, infrared (10 sec)		215	°C
Operating temperature, T_A		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2.7	5.25	V
	Digital input pins voltage (independent of supply voltage)	2.7	5.25	V
T_A	Operating temperature	–40	125	°C

6.4 Thermal Information

THERMAL METRIC(1)		ADCS7476, ADCS7477, ADCS7478	UNIT
		DBV (SOT-23)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	184.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	151.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics – ADCS7476

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC CONVERTER CHARACTERISTICS							
	Resolution with no missing codes	V_{DD} = 2.7 V to 3.6 V, –40°C ≤ T_A ≤ 125°C				12	Bits
INL	Integral non-linearity	V_{DD} = 2.7 V to 3.6 V	T_A = 25°C		±0.4		LSB
			–40°C ≤ T_A ≤ 85°C			±1	
		V_{DD} = 2.7 V to 3.6 V, T_A = 125°C		–1.1		1	LSB
DNL	Differential non-linearity	V_{DD} = 2.7 V to 3.6 V	T_A = 25°C	–0.3	0.5		LSB
			–40°C ≤ T_A ≤ 85°C	–0.9		1	
		V_{DD} = 2.7 V to 3.6 V, T_A = 125°C				±1	LSB
V_{OFF}	Offset error	V_{DD} = 2.7 V to 3.6 V	T_A = 25°C		±0.1		LSB
			−40°C ≤ T_A ≤ 125°C			±1.2	
GE	Gain error	V_{DD} = 2.7 V to 3.6 V	T_A = 25°C		±0.2		LSB
			–40°C ≤ T_A ≤ 125°C			±1.2	
DYNAMIC CONVERTER CHARACTERISTICS							
SINAD	Signal-to-noise plus distortion ratio	f_{IN} = 100 kHz	T_A = 25°C		72		dB
			–40°C ≤ T_A ≤ 125°C	70			
SNR	Signal-to-noise ratio	f_{IN} = 100 kHz	T_A = 25°C		72.5		dB
			–40°C ≤ T_A ≤ 85°C	70.8			
		f_{IN} = 100 kHz, T_A = 125°C		70.6			dB
THD	Total harmonic distortion	f_{IN} = 100 kHz			–80		dB
SFDR	Spurious-free dynamic range	f_{IN} = 100 kHz			82		dB
IMD	Intermodulation distortion, second order terms	f_a = 103.5 kHz, f_b = 113.5 kHz			–78		dB
	Intermodulation distortion, third order terms	f_a = 103.5 kHz, f_b = 113.5 kHz			–78		dB
FPBW	–3-dB full power bandwidth	5-V supply			11		MHz
		3-V supply			8		MHz
POWER SUPPLY CHARACTERISTICS							
I_{DD}	Normal mode (static)	V_{DD} = 4.75 V to 5.25 V, SCLK On or Off			2		mA
		V_{DD} = 2.7 V to 3.6 V, SCLK On or Off			1		mA
	Normal mode (operational)	V_{DD} = 4.75 V to 5.25 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		2		mA
			–40°C ≤ T_A ≤ 85°C			3.5	
		V_{DD} = 2.7 V to 3.6 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		0.6		mA
			–40°C ≤ T_A ≤ 85°C			1.6	
	Shutdown mode	V_{DD} = 5 V, SCLK Off			0.5		µA
		V_{DD} = 5 V, SCLK On			60		µA
P_D	Power consumption, normal mode (operational)	V_{DD} = 5 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		10		mW
			–40°C ≤ T_A ≤ 85°C			17.5	
		V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		2		mW
			–40°C ≤ T_A ≤ 85°C			4.8	
	Power consumption, shutdown mode	V_{DD} = 5 V, SCLK Off			2.5		µW
		V_{DD} = 3 V, SCLK Off			1.5		µW
ANALOG INPUT CHARACTERISTICS							
V_{IN}	Input range				0 to V_{DD}		V
I_{DCL}	DC leakage current	–40°C ≤ T_A ≤ 85°C				±1	µA
C_{INA}	Analog input capacitance				30		pF
DIGITAL INPUT CHARACTERISTICS							

(1) Data sheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.

Electrical Characteristics – ADCS7476 (continued)

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	Input high voltage	–40°C ≤ T_A ≤ 85°C		2.4			V
V_{IL}	Input low voltage	V_{DD} = 5 V, –40°C ≤ T_A ≤ 85°C				0.8	V
		V_{DD} = 3 V, –40°C ≤ T_A ≤ 85°C				0.4	V
I_{IN}	Input current	V_{IN} = 0 V or V_{DD}	T_A = 25°C		±10		nA
			–40°C ≤ T_A ≤ 85°C			±1	µA
C_{IND}	Digital input capacitance	T_A = 25°C			2		pF
		–40°C ≤ T_A ≤ 85°C				4	
DIGITAL OUTPUT CHARACTERISTICS							
V_{OH}	Output high voltage	I_{SOURCE} = 200 µA, V_{DD} = 2.7 V to 5.25 V, –40°C ≤ T_A ≤ 85°C		V_{DD} – 0.2			V
V_{OL}	Output low voltage	I_{SINK} = 200 µA, –40°C ≤ T_A ≤ 85°C				0.4	V
I_{OL}	TRI-STATE leakage current	–40°C ≤ T_A ≤ 85°C				±10	µA
C_{OUT}	TRI-STATE output capacitance	T_A = 25°C			2		pF
		–40°C ≤ T_A ≤ 85°C				4	
	Output coding			Straight (natural) binary			
AC ELECTRICAL CHARACTERISTICS							
f_{SCLK}	Clock frequency	–40°C ≤ T_A ≤ 125°C				20	MHz
DC	SCLK duty cycle	–40°C ≤ T_A ≤ 85°C		40%		60%	
t_{TH}	Track or hold acquisition time	–40°C ≤ T_A ≤ 85°C				400	ns
f_{RATE}	Throughput rate	–40°C ≤ T_A ≤ 85°C				1	MSPS
t_{AD}	Aperture delay				3		ns
t_{AJ}	Aperture jitter				30		ps

6.6 Electrical Characteristics – ADCS7477

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC CONVERTER CHARACTERISTICS							
	Resolution with no missing codes	–40°C ≤ T_A ≤ 85°C				10	Bits
INL	Integral non-linearity	T_A = 25°C			±0.2		LSB
		–40°C ≤ T_A ≤ 85°C				±0.7	
DNL	Differential non-linearity	T_A = 25°C		–0.2		0.3	LSB
		T–40°C ≤ T_A ≤ 85°C		±0.7		±0.7	
V_{OFF}	Offset error	T_A = 25°C			±0.1		LSB
		–40°C ≤ T_A ≤ 85°C				±0.7	
GE	Gain error	T_A = 25°C			±0.2		LSB
		–40°C ≤ T_A ≤ 85°C				±1	
DYNAMIC CONVERTER CHARACTERISTICS							
SINAD	Signal-to-noise plus distortion ratio	f_{IN} = 100 kHz	T_A = 25°C		61.7		dBFS
			–40°C ≤ T_A ≤ 85°C	61			
SNR	Signal-to-noise ratio	f_{IN} = 100 kHz			62		dB
THD	Total harmonic distortion	f_{IN} = 100 kHz	T_A = 25°C		–77		dB
			–40°C ≤ T_A ≤ 85°C			–73	
SFDR	Spurious-free dynamic range	f_{IN} = 100 kHz	T_A = 25°C		78		dB
			–40°C ≤ T_A ≤ 85°C	74			

(1) Data sheet minimum and maximum specification limits are ensured by design, test, or statistical analysis.

Electrical Characteristics – ADCS7477 (continued)

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IMD	Intermodulation distortion, second order terms	f_a = 103.5 kHz, f_b = 113.5 kHz			–78		dB
	Intermodulation distortion, third order terms	f_a = 103.5 kHz, f_b = 113.5 kHz			–78		dB
FPBW	–3-dB full power bandwidth	5-V supply			11		MHz
		3-V supply			8		MHz
POWER SUPPLY CHARACTERISTICS							
I_{DD}	Normal mode (static)	V_{DD} = 4.75 V to 5.25 V, SCLK On or Off			2		mA
		V_{DD} = 2.7 V to 3.6 V, SCLK On or Off			1		mA
	Normal mode (operational)	V_{DD} = 4.75 V to 5.25 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		2		mA
			–40°C ≤ T_A ≤ 85°C			3.5	
		V_{DD} = 2.7 V to 3.6 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		0.6		mA
			–40°C ≤ T_A ≤ 85°C			1.6	
	Shutdown mode	V_{DD} = 5 V, SCLK Off			0.5		µA
		V_{DD} = 5 V, SCLK On			60		
P_D	Power consumption, normal mode (operational)	V_{DD} = 5 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		10		mW
			–40°C ≤ T_A ≤ 85°C			17.5	
		V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		2		mW
			–40°C ≤ T_A ≤ 85°C			4.8	
	Power consumption, shutdown mode	V_{DD} = 5 V, SCLK Off			2.5		µW
		V_{DD} = 3 V, SCLK Off			1.5		
ANALOG INPUT CHARACTERISTICS							
V_{IN}	Input range				0 to V_{DD}		V
I_{DCL}	DC leakage current	T_A = −40°C to 85°C				±1	µA
C_{INA}	Analog input capacitance				30		pF
DIGITAL INPUT CHARACTERISTICS							
V_{IH}	Input high voltage	T_A = −40°C to 85°C		2.4			V
V_{IL}	Input low voltage	V_{DD} = 5 V, –40°C ≤ T_A ≤ 85°C				0.8	V
		V_{DD} = 3 V, –40°C ≤ T_A ≤ 85°C				0.4	V
I_{IN}	Input current	V_{IN} = 0 V or V_{DD}	T_A = 25°C		±10		nA
			–40°C ≤ T_A ≤ 85°C			±1	µA
C_{IND}	Digital input capacitance	T_A = 25°C			2		pF
		–40°C ≤ T_A ≤ 85°C				4	
DIGITAL OUTPUT CHARACTERISTICS							
V_{OH}	Output high voltage	I_{SOURCE} = 200 µA, V_{DD} = 2.7 V to 5.25 V, –40°C ≤ T_A ≤ 85°C		V_{DD} – 0.2			V
V_{OL}	Output low voltage	I_{SINK} = 200 µA, –40°C ≤ T_A ≤ 85°C				0.4	V
I_{OL}	TRI-STATE leakage current	–40°C ≤ T_A ≤ 85°C				±10	µA
C_{OUT}	TRI-STATE output capacitance	T_A = 25°C			2		pF
		–40°C ≤ T_A ≤ 85°C				4	
	Output coding			Straight (natural) binary			
AC ELECTRICAL CHARACTERISTICS							
f_{SCLK}	Clock frequency	–40°C ≤ T_A ≤ 85°C				20	MHz
DC	SCLK duty cycle	–40°C ≤ T_A ≤ 85°C		40%		60%	
t_{TH}	Track or hold acquisition time	–40°C ≤ T_A ≤ 85°C				400	ns
f_{RATE}	Throughput rate	–40°C ≤ T_A ≤ 85°C				1	MSPS
t_{AD}	Aperture delay				3		ns

Electrical Characteristics – ADCS7477 (continued)

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{AJ}	Aperture jitter			30		ps

6.7 Electrical Characteristics – ADCS7478

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
STATIC CONVERTER CHARACTERISTICS							
	Resolution with no missing codes	–40°C ≤ T_A ≤ 85°C				8	Bits
INL	Integral non-linearity	T_A = 25°C			±0.05		LSB
		–40°C ≤ T_A ≤ 85°C				±0.3	
DNL	Differential non-linearity	T_A = 25°C			±0.07		LSB
		–40°C ≤ T_A ≤ 85°C				±0.3	
V_{OFF}	Offset error	T_A = 25°C			±0.03		LSB
		–40°C ≤ T_A ≤ 85°C				±0.3	
GE	Gain error	T_A = 25°C			±0.08		LSB
		–40°C ≤ T_A ≤ 85°C				±0.4	
	Total unadjusted error	T_A = 25°C			±0.07		LSB
		–40°C ≤ T_A ≤ 85°C				±0.3	
DYNAMIC CONVERTER CHARACTERISTICS							
SINAD	Signal-to-noise plus distortion ratio	f_{IN} = 100 kHz	T_A = 25°C		49.7		dB
			–40°C ≤ T_A ≤ 85°C	49			
SNR	Signal-to-noise ratio	f_{IN} = 100 kHz			49.7		dB
THD	Total harmonic distortion	f_{IN} = 100 kHz	T_A = 25°C		–77		dB
			–40°C ≤ T_A ≤ 85°C			–65	
SFDR	Spurious-free dynamic range	f_{IN} = 100 kHz	T_A = 25°C		69		dB
			–40°C ≤ T_A ≤ 85°C	65			
IMD	Intermodulation distortion, second order terms	f_a = 103.5 kHz, f_b = 113.5 kHz			–68		dB
	Intermodulation distortion, third order terms	f_a = 103.5 kHz, f_b = 113.5 kHz			–68		dB
FPBW	–3-dB full power bandwidth	5-V supply			11		MHz
		3-V supply			8		MHz
POWER SUPPLY CHARACTERISTICS							
I_{DD}	Normal mode (static)	V_{DD} = 4.75 V to 5.25 V, SCLK On or Off			2		mA
		V_{DD} = 2.7 V to 3.6 V, SCLK On or Off			1		mA
	Normal mode (operational)	V_{DD} = 4.75 V to 5.25 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		2		mA
			–40°C ≤ T_A ≤ 85°C			3.5	
		V_{DD} = 2.7 V to 3.6 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		0.6		mA
			–40°C ≤ T_A ≤ 85°C			1.6	
	Shutdown mode	V_{DD} = 5 V, SCLK Off			0.5		µA
		V_{DD} = 5 V, SCLK On			60		

(1) Data sheet min/max specification limits are ensured by design, test, or statistical analysis.

Electrical Characteristics – ADCS7478 (continued)

T_A = 25°C, V_{DD} = 2.7 V to 5.25 V, f_{SCLK} = 20 MHz, and f_{SAMPLE} = 1 MSPS (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_D	Power consumption, normal mode (operational)	V_{DD} = 5 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		10		mW
			–40°C ≤ T_A ≤ 85°C			17.5	
		V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS	T_A = 25°C		2		mW
			–40°C ≤ T_A ≤ 85°C			4.8	
	Power consumption, shutdown mode	V_{DD} = 5 V, SCLK Off			2.5		µW
		V_{DD} = 3 V, SCLK Off			1.5		
ANALOG INPUT CHARACTERISTICS							
V_{IN}	Input range				0 to V_{DD}		V
I_{DCL}	DC leakage current	–40°C ≤ T_A ≤ 85°C				±1	µA
C_{INA}	Analog input capacitance				30		pF
DIGITAL INPUT CHARACTERISTICS							
V_{IH}	Input high voltage	–40°C ≤ T_A ≤ 85°C		2.4			V
V_{IL}	Input low voltage	V_{DD} = 5 V, –40°C ≤ T_A ≤ 85°C				0.8	V
		V_{DD} = 3 V, –40°C ≤ T_A ≤ 85°C				0.4	V
I_{IN}	Digital input current	V_{IN} = 0 V or V_{DD}	T_A = 25°C		±10		nA
			–40°C ≤ T_A ≤ 85°C			±1	µA
C_{IND}	Input capacitance	T_A = 25°C			2		p
		–40°C ≤ T_A ≤ 85°C				4	
DIGITAL OUTPUT CHARACTERISTICS							
V_{OH}	Output high voltage	I_{SOURCE} = 200 µA, V_{DD} = 2.7 V to 5.25 V, –40°C ≤ T_A ≤ 85°C		V_{DD} − 0.2			V
V_{OL}	Output low voltage	I_{SINK} = 200 µA, –40°C ≤ T_A ≤ 85°C				0.4	V
I_{OL}	TRI-STATE leakage current	–40°C ≤ T_A ≤ 85°C				±10	µA
C_{OUT}	TRI-STATE output capacitance				2	4	pF
	Output coding				Straight (natural) binary		
AC ELECTRICAL CHARACTERISTICS							
f_{SCLK}	Clock frequency	–40°C ≤ T_A ≤ 85°C				20	MHz
DC	SCLK duty cycle	–40°C ≤ T_A ≤ 85°C		40%		60%	
t_{TH}	Track or hold acquisition time	–40°C ≤ T_A ≤ 85°C				400	ns
f_{RATE}	Throughput rate	–40°C ≤ T_A ≤ 85°C (see *Application Information*)		1			MSPS
t_{AD}	Aperture delay				3		ns
t_{AJ}	Aperture jitter				30		ps

6.8 Timing Requirements

–40°C ≤ T_A ≤ 85°C, V_{DD} = 2.7 V to 5.25 V, and f_{SCLK} = 20 MHz (unless otherwise noted)(1)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
$t_{CONVERT}$		T_A = 25°C		16 × t_{SCLK}		
t_{QUIET}	Quiet time(2)		50			ns
t_1	Minimum $\overline{CS}$ pulse width		10			ns
t_2	$\overline{CS}$ to SCLK setup time		10			ns
t_3	Delay from $\overline{CS}$ until SDATA TRI-STATE disabled (3)				20	ns

(1) All input signals are specified as t_r = t_f = 5 ns (10% to 90% V_{DD}) and timed from 1.6 V.
(2) Minimum quiet time required between bus relinquish and start of next conversion.
(3) Measured with the load circuit (Figure 1), and defined as the time taken by the output to cross 1 V.

Timing Requirements (continued)

–40°C ≤ T_A ≤ 85°C, V_{DD} = 2.7 V to 5.25 V, and f_{SCLK} = 20 MHz (unless otherwise noted)[1]

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
t_4	Data access time after SCLK falling edge[4]	V_{DD} = 2.7 V to 3.6 V			40	ns
		V_{DD} = 4.75 V to 5.25 V			20	ns
t_5	SCLK low pulse width		0.4 × t_{SCLK}			ns
t_6	SCLK high pulse width		0.4 × t_{SCLK}			ns
t_7	SCLK to data valid hold time	V_{DD} = 2.7 V to 3.6 V	7			ns
		V_{DD} = 4.75 V to 5.25 V	5			ns
t_8	SCLK falling edge to SDATA high impedance [5]	V_{DD} = 2.7 V to 3.6 V	6		25	ns
		V_{DD} = 4.75 V to 5.25 V	5		25	ns
$t_{POWER-UP}$	Power-up time from full power down	T_A = 25°C		1		µs

(4) Measured with the load circuit (Figure 1), and defined as the time taken by the output to cross 1 V or 2 V.
(5) t_8 is derived from the time taken by the outputs to change by 0.5 V with the loading circuit (Figure 1). The measured number is then adjusted to remove the effects of charging or discharging the 25-pF capacitor. This means t_8 is the true bus relinquish time, independent of the bus loading.

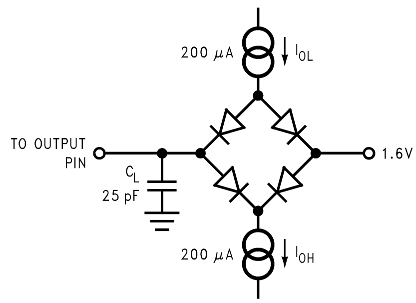


Figure 1. Timing Test Circuit

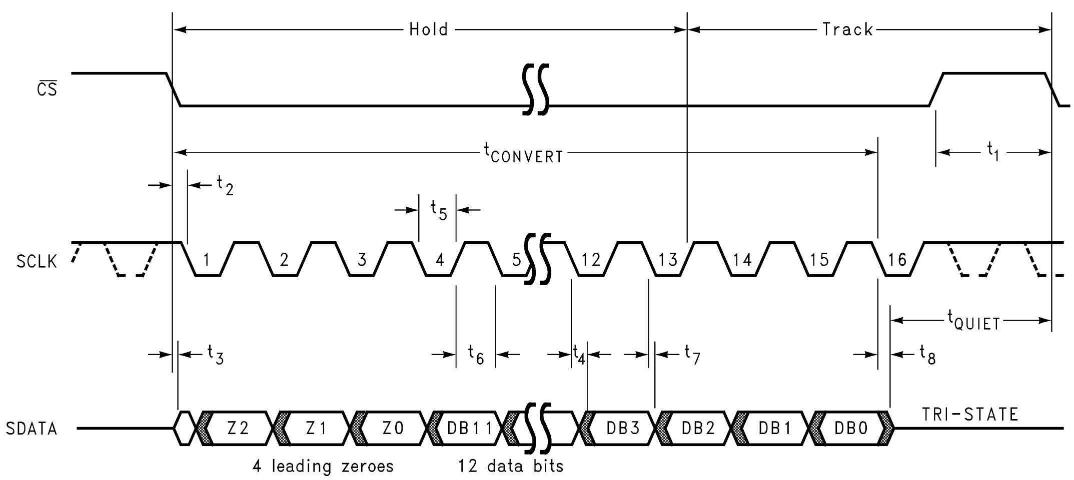


Figure 2. ADCS7476 Serial Interface Timing Diagram

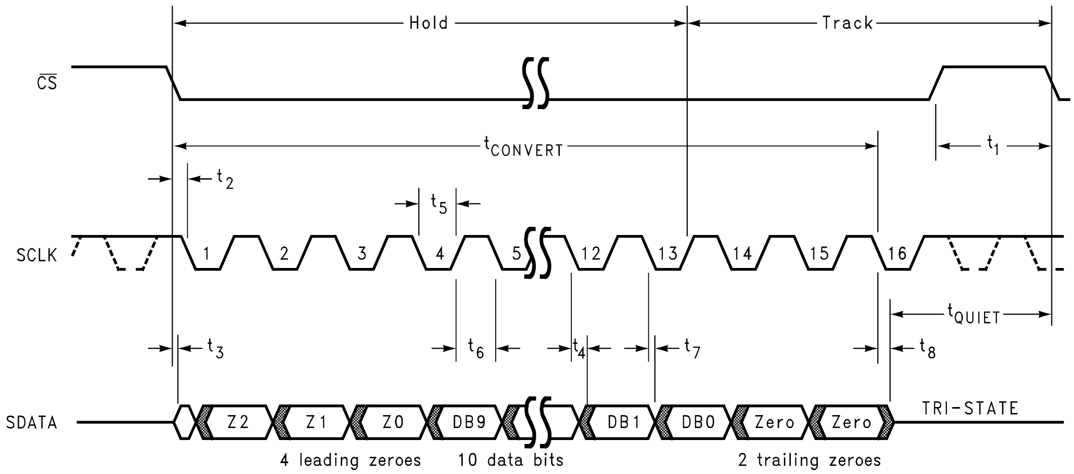


Figure 3. ADCS7477 Serial Interface Timing Diagram

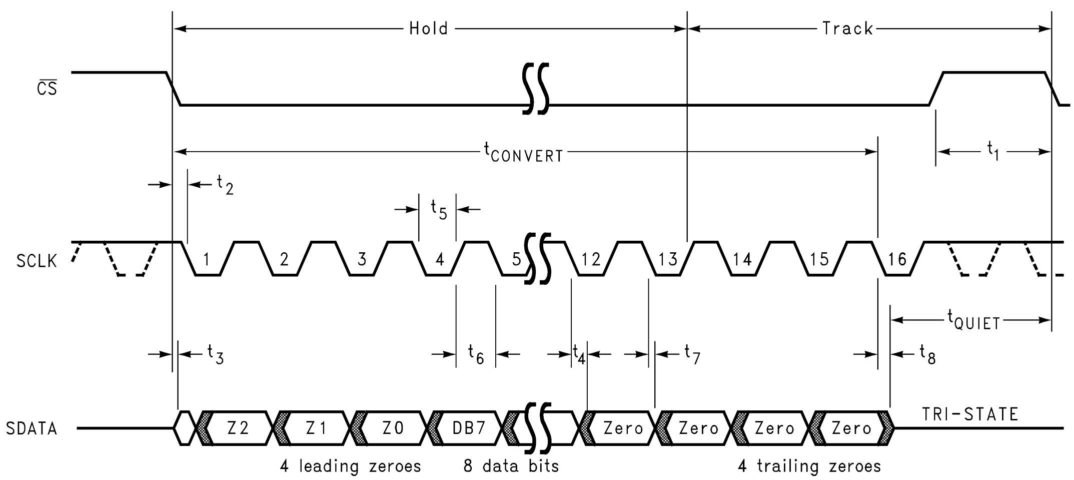


Figure 4. ADCS7478 Serial Interface Timing Diagram

6.9 Typical Characteristics

T_A = 25°C, V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, and f_{IN} = 100 kHz (unless otherwise noted)

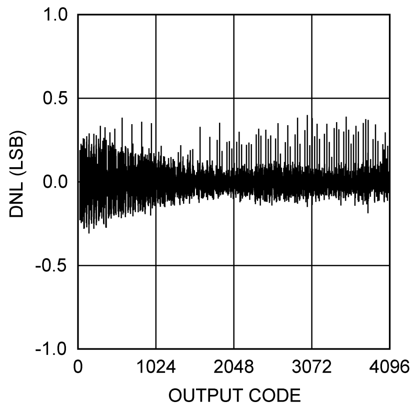


Figure 5. ADCS7476 DNL

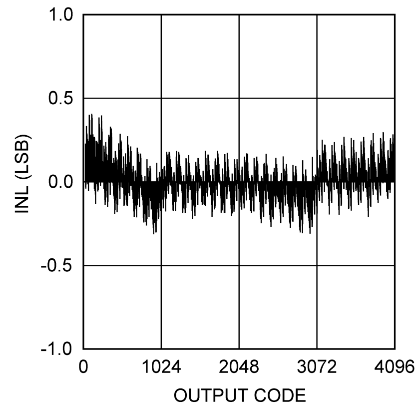


Figure 6. ADCS7476 INL

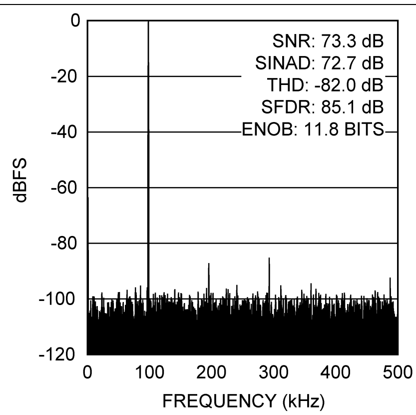


Figure 7. ADCS7476 Spectral Response at 100-kHz Input

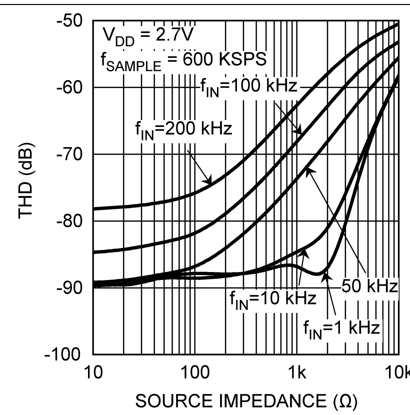


Figure 8. ADCS7476 THD vs Source Impedance

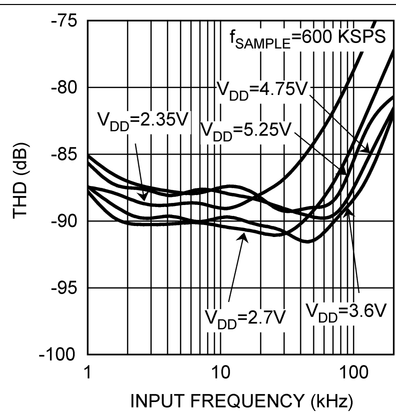


Figure 9. ADCS7476 THD vs Input Frequency, 600 KSPS

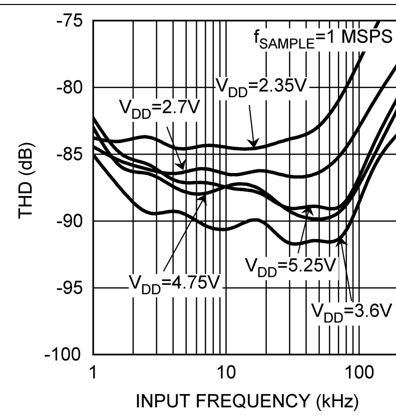


Figure 10. ADCS7476 THD vs Input Frequency, 1 MSPS

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, and f_{IN} = 100 kHz (unless otherwise noted)

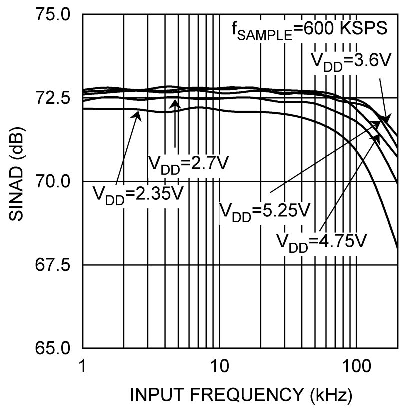


Figure 11. ADCS7476 SINAD vs Input Frequency, 600 KSPS

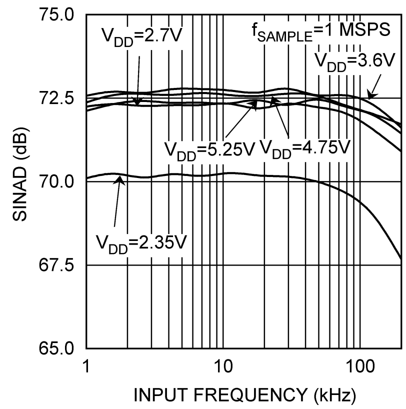


Figure 12. ADCS7476 SINAD vs Input Frequency, 1 MSPS

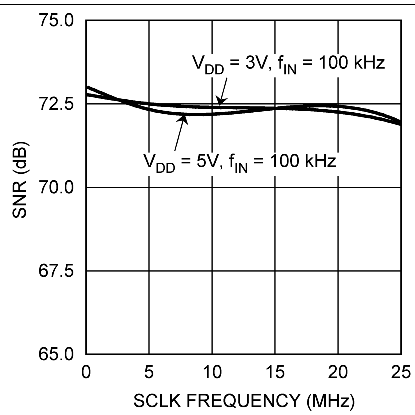


Figure 13. ADCS7476 SNR vs f_{SCLK}

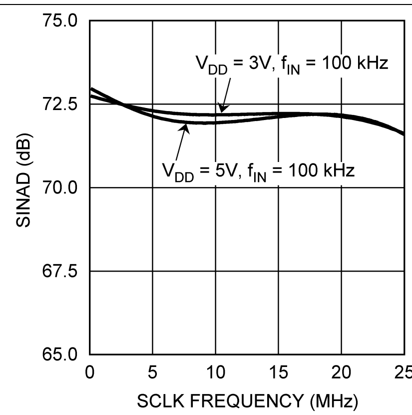


Figure 14. ADCS7476 SINAD vs f_{SCLK}

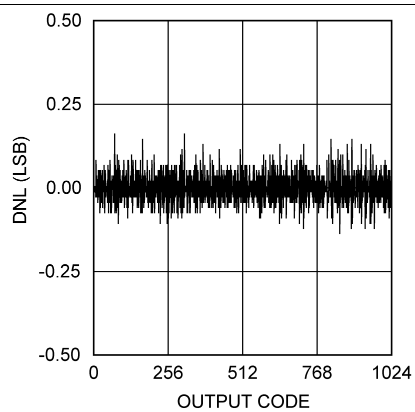


Figure 15. ADCS7477 DNL

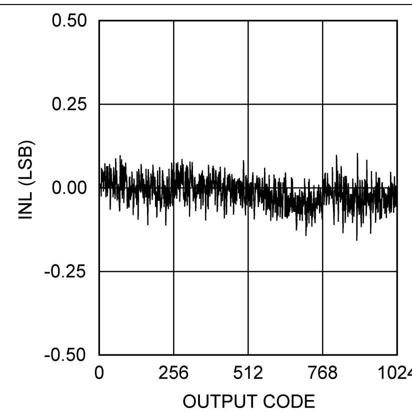


Figure 16. ADCS7477 INL

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, and f_{IN} = 100 kHz (unless otherwise noted)

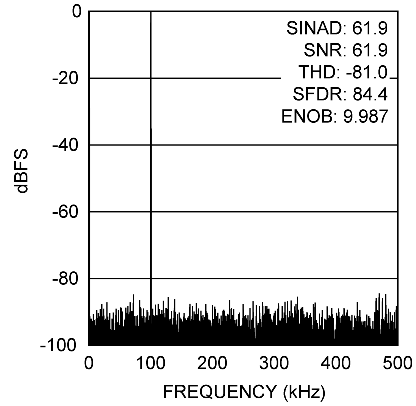


Figure 17. ADCS7477 Spectral Response at 100-kHz Input

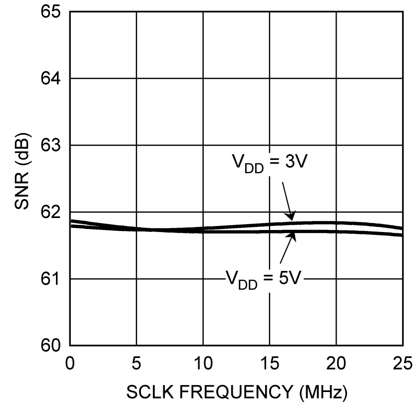


Figure 18. ADCS7477 SNR vs f_{SCLK}

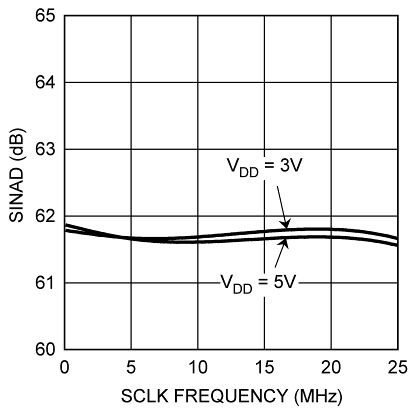


Figure 19. ADCS7477 SINAD vs f_{SCLK}

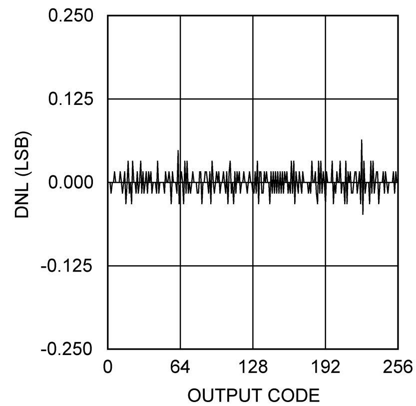


Figure 20. ADCS7478 DNL

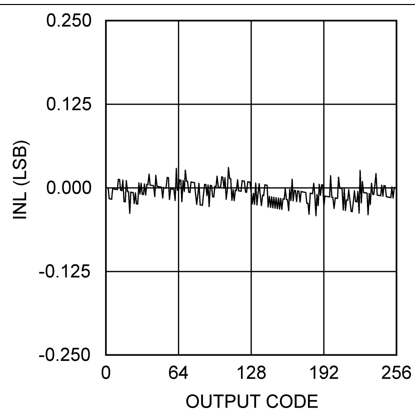


Figure 21. ADCS7478 INL

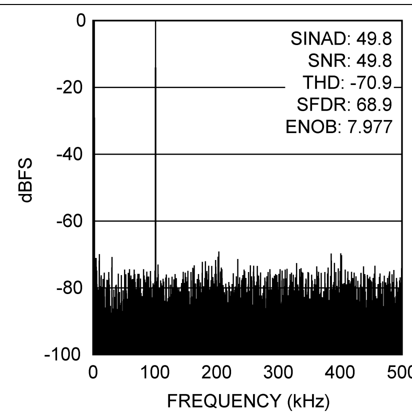


Figure 22. ADCS7478 Spectral Response at 100-kHz Input

Typical Characteristics (continued)

T_A = 25°C, V_{DD} = 3 V, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 20 MHz, and f_{IN} = 100 kHz (unless otherwise noted)

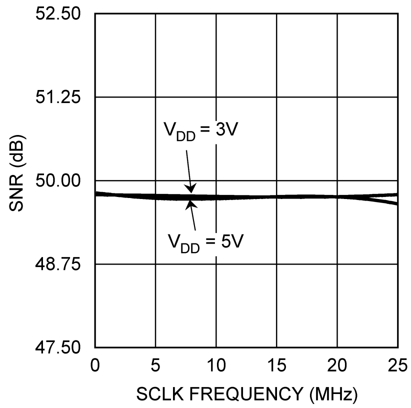


Figure 23. ADCS7478 SNR vs f_{SCLK}

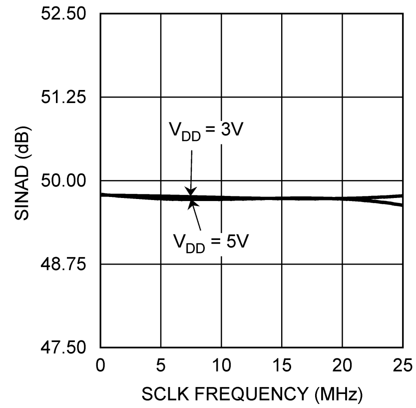


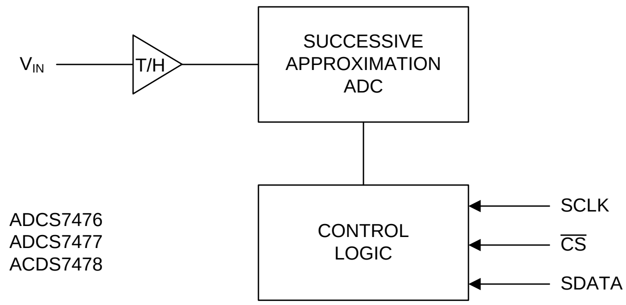
Figure 24. ADCS7478 SINAD vs f_{SCLK}

7 Detailed Description

7.1 Overview

The ADCS747x devices are successive-approximation analog-to-digital converters designed around a charge-redistribution digital-to-analog converter. Simplified schematics of the ADCS747x in both track and hold operation are shown in Figure 25 and Figure 26. In Figure 26, the device is in track mode where the switch SW1 connects the sampling capacitor to the input, and SW2 balances the comparator inputs. The device is in this state until $\overline{CS}$ is brought low, at which point the device moves to hold mode.

7.2 Functional Block Diagram



7.3 Feature Description

Serial interface timing diagrams for the ADCS747x are shown in Figure 2, Figure 3, and Figure 4. $\overline{CS}$ is chip select, which initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. SDATA is the serial data out pin, where a conversion result is found.

Basic operation of the ADCS747x begins with $\overline{CS}$ going low, which initiates a conversion process and data transfer. Subsequent rising and falling edges of SCLK will be labeled with reference to the falling edge of $\overline{CS}$; for example, *the third falling edge of SCLK* shall refer to the third falling edge of SCLK after $\overline{CS}$ goes low.

At the fall of $\overline{CS}$, the SDATA pin comes out of TRI-STATE, and the converter moves from track mode to hold mode. The input signal is sampled and held for conversion at the falling edge of $\overline{CS}$. The converter moves from hold mode to track mode on the 13th rising edge of SCLK (see Figure 2, Figure 3, or Figure 4). The SDATA pin is placed back into TRI-STATE after the 16th falling edge of SCLK, or at the rising edge of $\overline{CS}$, whichever occurs first. After a conversion is completed, the quiet time t_{QUIET} must be satisfied before bringing $\overline{CS}$ low again to begin another conversion.

Sixteen SCLK cycles are required to read a complete sample from the ADCS747x. The sample bits (including any leading or trailing zeroes) are clocked out on falling edges of SCLK, and are intended to be clocked in by a receiver on subsequent falling edges of SCLK. ADCS747x produces four leading zeroes on SDATA, followed by twelve, ten, or eight data bits (the most significant first). After the data bits, the ADCS7477 clocks out two trailing zeros, and the ADCS7478 clocks out four trailing zeros. The ADCS7476 does not clock out any trailing zeros; the least significant data bit is valid on the 16th falling edge of SCLK.

Depending upon the application, the first edge on SCLK after $\overline{CS}$ goes low may be either a falling edge or a rising edge. If the first SCLK edge after $\overline{CS}$ goes low is a rising edge, all four leading zeroes are valid on the first four falling edges of SCLK. If instead the first SCLK edge after $\overline{CS}$ goes low is a falling edge, the first leading zero may not be set up in time for a microprocessor or DSP to read it correctly. The remaining data bits are still clocked out on the falling edges of SCLK.

7.4 Device Functional Modes

Figure 25 shows the device in hold mode where the switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The device moves from hold mode to track mode (Figure 26) on the 13th rising edge of SCLK.

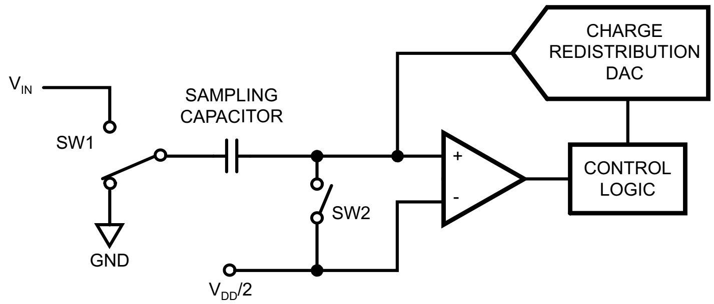


Figure 25. ADCS747x in Hold Mode

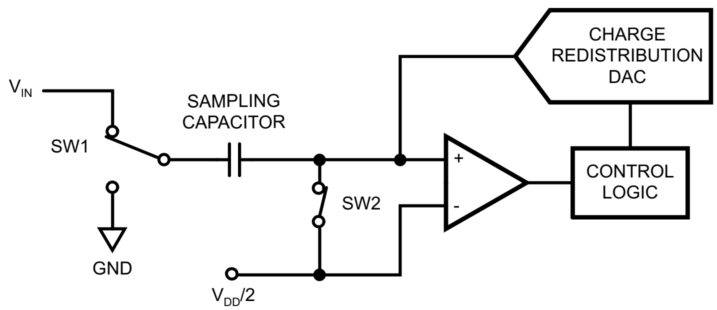


Figure 26. ADCS747x in Track Mode

7.4.1 Transfer Function

The output format of ADCS747x is straight binary. Code transitions occur midway between successive integer LSB values. The LSB widths for the ADCS7476 is V_{DD} / 4096; for the ADCS7477 the LSB width is V_{DD} / 1024; for the ADCS7478, the LSB width is V_{DD} / 256. The ideal transfer characteristic for the ADCS7476 and ADCS7477 is shown in Figure 27, while the ideal transfer characteristic for the ADCS7478 is shown in Figure 28.

Device Functional Modes (continued)

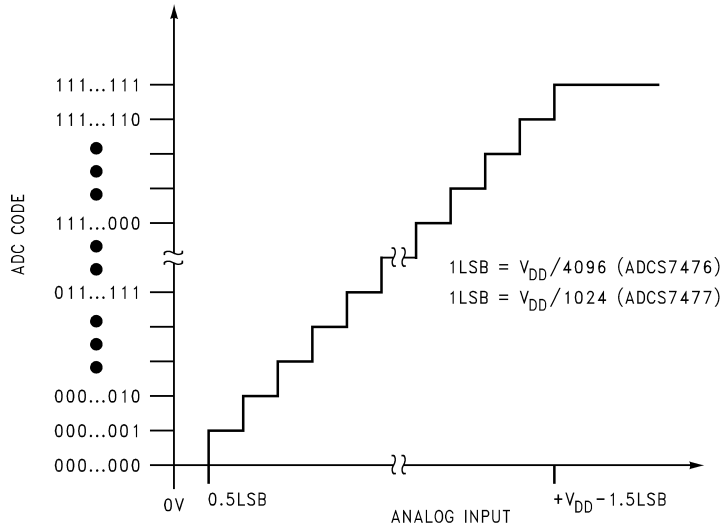


Figure 27. ADCS7476/77 Ideal Transfer Characteristic

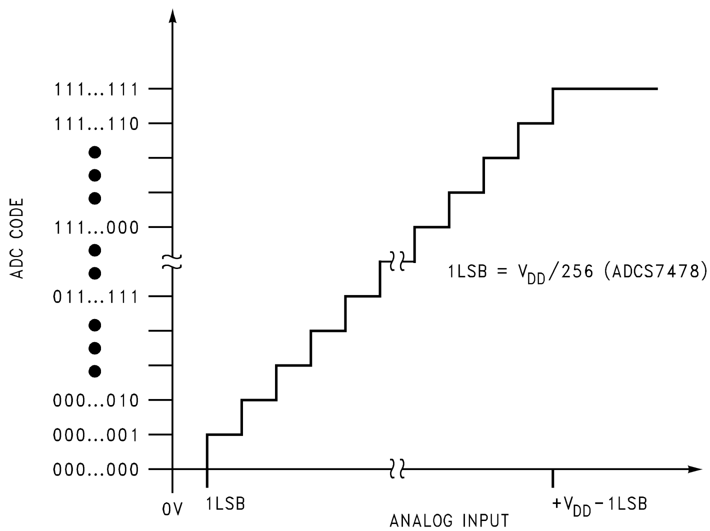


Figure 28. ADCS7478 Ideal Transfer Characteristic

7.4.2 Power-Up Timing

The ADCS747x typically requires 1 µs to power up, either after first applying V_{DD}, or after returning to normal mode from shutdown mode. This corresponds to one *dummy* conversion for any SCLK frequency within the specifications in this document. After this first dummy conversion, the ADCS747x performs conversions properly.

NOTE

The t_{QUIET} time must still be included between the first dummy conversion and the second valid conversion.

Device Functional Modes (continued)

7.4.3 Modes of Operation

The ADCS747x has two possible modes of operation: *Normal Mode* and *Shutdown Mode*. ADCS747x enters normal mode (and a conversion process is begun) when $\overline{CS}$ is pulled low. The device enters shutdown mode if $\overline{CS}$ is pulled high before the tenth falling edge of SCLK after $\overline{CS}$ is pulled low, or stays in normal mode if $\overline{CS}$ remains low. Once in shutdown mode, the device stays there until $\overline{CS}$ is brought low again. By varying the ratio of time spent in the normal and shutdown modes, a system may trade off throughput for power consumption.

7.4.3.1 Normal Mode

The best possible throughput is obtained by leaving the ADCS747x in normal mode at all times, so there are no power-up delays. To keep the device in normal mode continuously, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK after the start of a conversion (remember that a conversion is initiated by bringing $\overline{CS}$ low).

If $\overline{CS}$ is brought high after the 10th falling edge, but before the 16th falling edge, the device remains in normal mode, but the current conversion is aborted, and SDATA returns to TRI-STATE (truncating the output word).

Sixteen SCLK cycles are required to read all of a conversion word from the device. After sixteen SCLK cycles have elapsed, $\overline{CS}$ may be idled either high or low until the next conversion. If $\overline{CS}$ is idled low, it must be brought high again before the start of the next conversion, which begins when $\overline{CS}$ is again brought low.

After sixteen SCLK cycles, SDATA returns to TRI-STATE. Another conversion may be started, after t_{QUIET} has elapsed, by bringing $\overline{CS}$ low again.

7.4.3.2 Start-Up Mode

When the V_{DD} supply is first applied, the ADCS747x may power up in either of the two modes: normal or shutdown. As such, one dummy conversion should be performed after start-up, exactly as described in *Power-Up Timing*. The part may then be placed into either normal mode or the shutdown mode, as described in *Normal Mode* and *Shutdown Mode*.

7.4.3.3 Shutdown Mode

Shutdown mode is appropriate for applications that either do not sample continuously, or are willing to trade throughput for power consumption. When the ADCS747x is in shutdown mode, all of the analog circuitry is turned off.

To enter shutdown mode, a conversion must be interrupted by bringing $\overline{CS}$ back high anytime between the second and tenth falling edges of SCLK, as shown in Figure 29. Once $\overline{CS}$ has been brought high in this manner, the device enters shutdown mode; the current conversion is aborted and SDATA enters TRI-STATE. If $\overline{CS}$ is brought high before the second falling edge of SCLK, the device does not change mode; this is to avoid accidentally changing mode as a result of noise on the $\overline{CS}$ line.

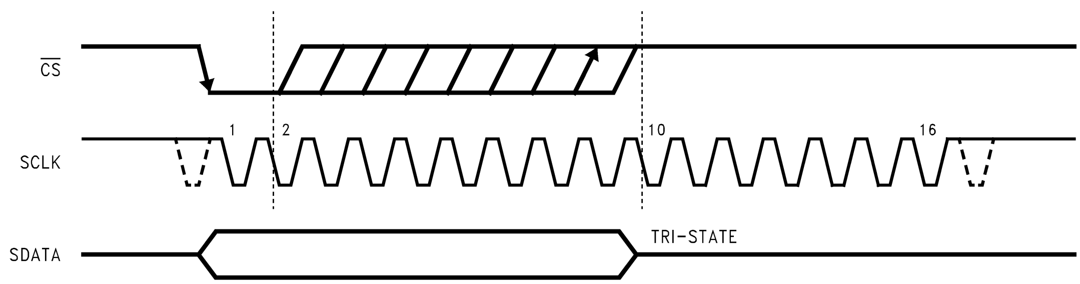


Figure 29. Entering Shutdown Mode

Device Functional Modes (continued)

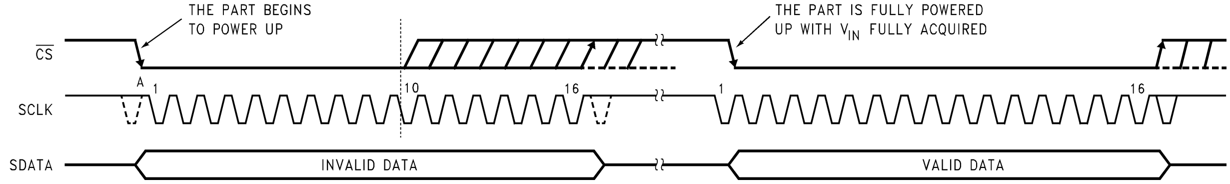


Figure 30. Entering Normal Mode

To exit shutdown mode, bring $\overline{CS}$ back low. Upon bringing $\overline{CS}$ low, the ADCS747x begins powering up. Power up typically takes 1 µs. This microsecond of power-up delay results in the first conversion result being unusable. The second conversion performed after power-up, however, is valid, as shown in Figure 30.

If $\overline{CS}$ is brought back high before the 10th falling edge of SCLK, the device returns to shutdown mode. This is done to avoid accidentally entering normal mode as a result of noise on the $\overline{CS}$ line. To exit shutdown mode and remain in normal mode, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK. The ADCS747x is fully powered up after 16 SCLK cycles.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

A typical application of ADCS747x is shown in Figure 32. The combined analog and digital supplies are provided in this example by the TI LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The supply is bypassed with a capacitor network located close to the device. The three-wire interface is also shown connected to a microprocessor or DSP.

8.1.1 Analog Inputs

An equivalent circuit for the ADCS747x input channel is shown in Figure 31. The diodes D1 and D2 provide ESD protection for the analog inputs. At no time should an analog input exceed V_{DD} + 300 mV or GND – 300 mV, as these ESD diodes begin conducting current into the substrate or supply line and affect ADC operation.

The capacitor C1 in Figure 31 typically has a value of 4 pF, and is mainly due to pin capacitance. The resistor R1 represents the ON resistance of the multiplexer and track or hold switch, and is typically 100 Ω. The capacitor C2 is the ADCS747x sampling capacitor, and is typically 26 pF.

The sampling nature of the analog input causes input current pulses that result in voltage spikes at the input. ADCS747x delivers best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. In some applications where dynamic performance is critical, the input must be driven with a low output-impedance amplifier. In addition, when using ADCS747x to sample AC signals, a band-pass or low-pass filter reduces harmonics and noise and thus improve THD and SNR.

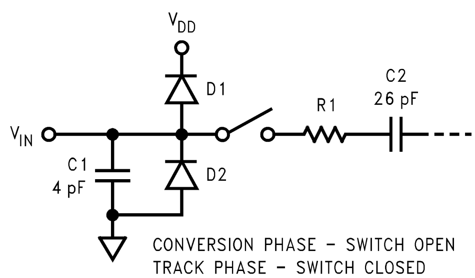


Figure 31. Equivalent Input Circuit

8.1.2 Digital Inputs and Outputs

The ADCS747x digital inputs (SCLK and $\overline{CS}$) are not limited by the same absolute maximum ratings as the analog inputs. The digital input pins are instead limited to 6.5 V with respect to GND, regardless of V_{DD}, the supply voltage. This allows ADCS747x to be interfaced with a wide range of logic levels, independent of the supply voltage.

NOTE

Even though the digital inputs are tolerant of up to 6.5 V above GND, the digital outputs are only capable of driving V_{DD} out.

In addition, the digital input pins are not prone to latch-up; SCLK and $\overline{CS}$ may be asserted before V_{DD} without any risk.

8.2 Typical Application

The ADCS747x are monolithic CMOS 12-, 10-, and 8-bit ADCs that use the supply voltage as a reference, enabling the devices to operate with a full-scale input range of 0 to V_{DD}. An example low-power application with the LMT87, which is a wide range ±0.3°C accurate temperature sensor, is shown in Figure 32.

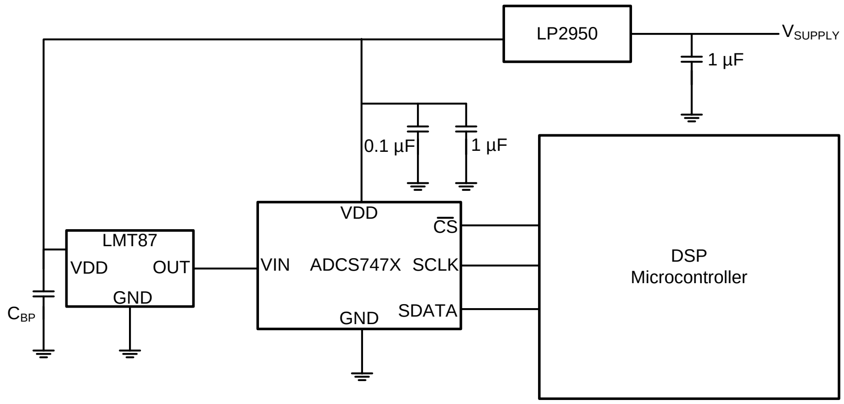


Figure 32. Typical Application Circuit

8.2.1 Design Requirements

A successful ADCS747x and LMT87 design is constrained by the following factors:

- V_{IN} range must be 0 V to V_{DD} where V_{DD} can range from 2.7 V to 5.25 V.

8.2.2 Detailed Design Procedure

Designing for an accurate measurement requires careful attention to the timing requirements for the ADCS747x parts.

Because the ADC747x parts use the supply voltage as a reference, ensuring that the supply voltage is settled to its final level before exiting the shutdown mode and beginning a conversion is important. After the supply voltage has settled, the $\overline{CS}$ is brought to a low level (ideally 0 V) to start a conversion.

Ensuring that any noise on the power supply is less than ½ LSB in amplitude is also important. The supply voltage must be regarded as a precise voltage reference.

After the $\overline{CS}$ has been brought low, the user must wait for one complete conversion cycle (approximately 1 µs) for meaningful data. The dummy conversion cycle is the start-up time of the ADCS747x. The ADCS747x digital output can then be correlated to the LMT87 output level to get an accurate temperature reading. At V_{DD} = 3.3 V, 1 LSB of ADCS7476 is 0.805 mV.

Typical Application (continued)

8.2.3 Application Curves

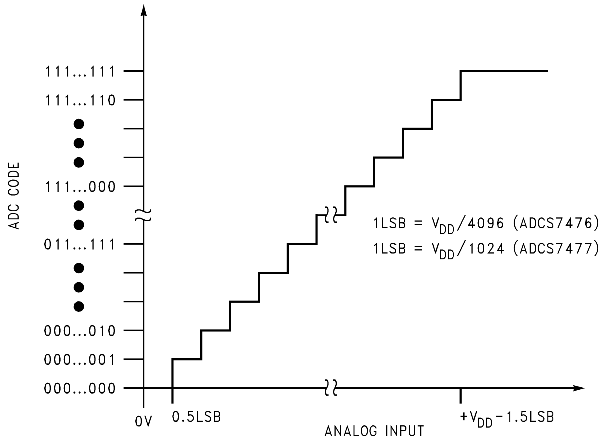


Figure 33. ADCS7476/77 Ideal Transfer Characteristic

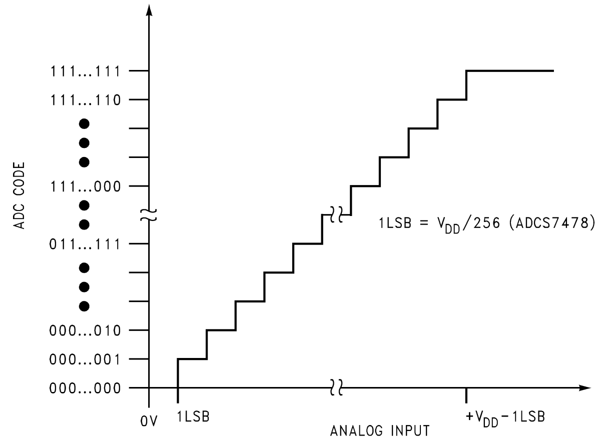


Figure 34. ADCS7478 Ideal Transfer Characteristic

9 Power Supply Recommendations

There are three concerns relating to the power supply of these products: the effects of *Power Supply Noise* upon the conversion process, the *Digital Output Effect Upon Noise* upon the conversion process, and *Power Management* of the product.

9.1 Power Supply Noise

Because the supply voltage of the ADCS747x is the reference voltage, any noise greater than 1/2 LSB in amplitude has some effect upon the converter noise performance. This effect is proportional to the input voltage level. The power supply must receive all the considerations of a reference voltage as far as stability and noise is concerned. Using the same supply voltage for these devices as is used for digital components leads to degraded noise performance.

9.2 Digital Output Effect Upon Noise

The charging of any output load capacitance requires current from the digital supply, V_{DD}. The current pulses required from the supply to charge the output capacitance causes voltage variations at the ADC supply line. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Similarly, discharging the output capacitance when the digital output goes from a logic high to a logic low dumps current into the die substrate, causing *ground bounce* noise in the substrate that degrades noise performance if that current is large enough. The larger the output capacitance, the more current flows through the device power supply line and die substrate and the greater is the noise coupled into the analog path.

The first solution to keeping digital noise out of the power supply is to decouple the supply from any other components or use a separate supply for the ADC. To keep noise out of the supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100-Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This limits the charge and discharge current of the output capacitance and improve noise performance. Because the series resistor and the load capacitance form a low frequency pole, verify signal integrity when the series resistor is added.

9.3 Power Management

When ADCS747x is operated continuously in normal mode, throughput up to 1 MSPS can be achieved. The user may trade throughput for power consumption by simply performing fewer conversions per unit time and putting the ADCS747x into shutdown mode between conversions. This method is not advantageous beyond 350-kSPS throughput.

Power Management (continued)

A plot of maximum power consumption versus throughput is shown in Figure 35. To calculate the power consumption for a given throughput, remember that each time the part exits shutdown mode and enters normal mode, one dummy conversion is required. Generally, the user puts the part into normal mode, execute one dummy conversion followed by one valid conversion, and then put the part back into shutdown mode. When this is done, the fraction of time spent in normal mode may be calculated by multiplying the throughput (in samples per second) by 2 µs, the time taken to perform one dummy and one valid conversion. The power consumption can then be found by multiplying the fraction of time spent in normal mode by the normal mode power consumption figure. The power dissipated while the part is in shutdown mode is negligible.

For example, to calculate the power consumption at 300 kSPS with V_{DD} = 5 V, begin by calculating the fraction of time spent in normal mode: 300,000 samples/second x 2 µs = 0.6, or 60%. The power consumption at 300 kSPS is then 60% of 17.5 mW (the maximum power consumption at V_{DD} = 5 V) or 10.5 mW.

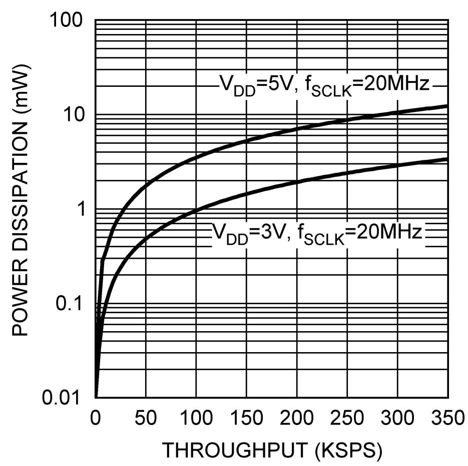


Figure 35. Maximum Power Consumption vs Throughput

10 Layout

10.1 Layout Guidelines

Capacitive coupling between noisy digital circuitry and sensitive analog circuitry can lead to poor performance. The solution is to keep the analog and digital circuitry separated from each other and the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. This digital noise could have significant impact upon system noise performance. To avoid performance degradation of the ADCS747x due to supply noise, do not use the same supply for the ADCS747x that is used for digital logic.

Generally, analog and digital lines must cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line must also be treated as a transmission line and be properly terminated.

The analog input must be isolated from noisy signal lines to avoid coupling of spurious signals into the input. Any external component (that is, a filter capacitor) connected between the input pins and ground of the converter or to the reference input pin and ground must be connected to a very clean point in the ground plane.

TI recommends the use of a single, uniform ground plane and the use of split power planes. The power planes must be placed within the same board layer. All analog circuitry (input amplifiers, filters, reference components, and so on) must be placed over the analog power plane. All digital circuitry and I/O lines must be placed over the digital power plane. Furthermore, all components in the reference circuitry and the input signal chain that are connected to ground must be connected together with short traces and enter the analog ground plane at a single, quiet point.

10.2 Layout Example

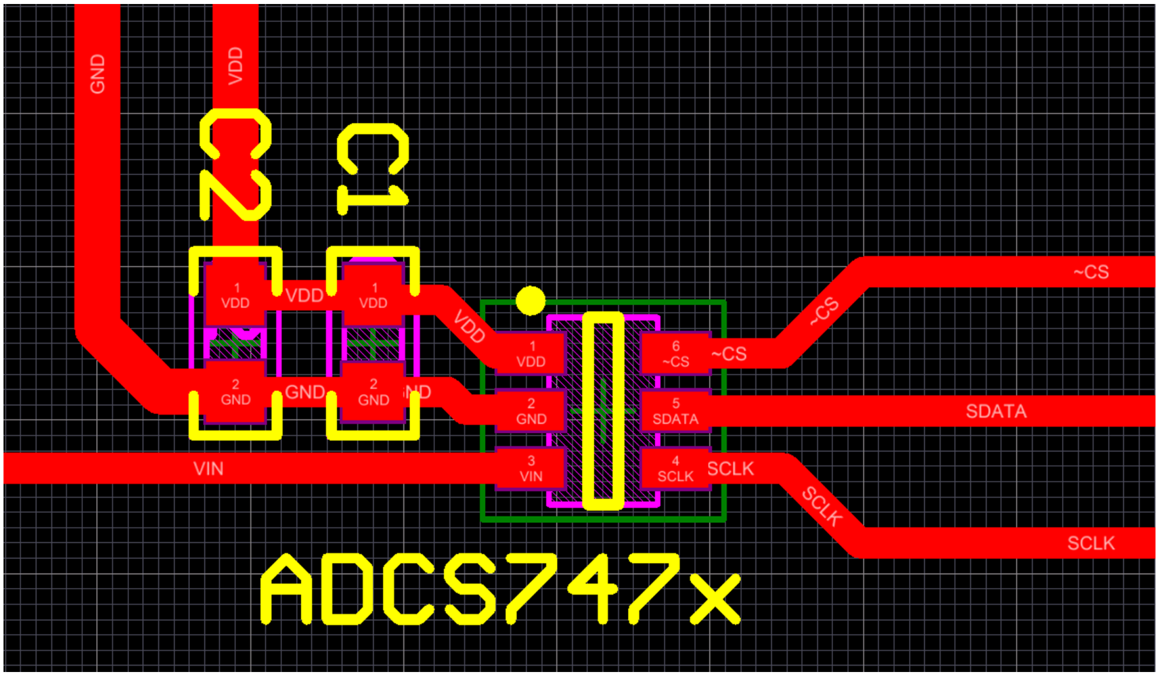


Figure 36. Layout Example

11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

11.1.1 デバイスの関連用語

アパーチャ遅延　は、入力信号が取得されるか、変換用にホールドされるときの、CSの立ち下がりエッジ以後の時間です。

アパーチャ・ジッタ(アパーチャの不安定性)　は、サンプル間でのアパーチャ遅延の偏差です。アパーチャ・ジッタは、出力にノイズとして現れます。

差動非直線性(DNL)　は、理想的なステップ・サイズである1 LSBからの最大偏差の測定値です。

デューティ・サイクル　は、繰り返しのデジタル波形が1周期の合計時間のうちHIGHになる時間の割合です。ここでは、SCLKを基準とします。

実効ビット数(ENOBまたはEFFECTIVE BITS)　は、信号対ノイズ+歪み比率(SINAD)を規定する別の方法です。ENOBは(SINAD - 1.76) / 6.02で定義され、コンバータがこの(ENOB)ビット数を持つ完全なADCと等価であることを示します。

フルパワー帯域幅　は、再構築された出力基本波が、フルスケール入力について、低周波数の値より3dB低下する周波数の測定値です。

ゲイン誤差　は、最後のコード遷移[(111...110)から(111...111)]が、オフセット誤差の調整後に、理想的な値(ADCS7476およびADCS7477ではV_{REF} - 1.5 LSB、ADCS7478ではV_{REF} - 1 LSB)とどれだけの差異があるかを示します。

積分非直線性(INL)　は、それぞれのコードが、負のフルスケール(最初のコード遷移より½ LSBだけ下)と正のフルスケール(最後のコード遷移より½ LSBだけ上)との間に引かれた直線との間にどれだけ差異があるかの測定値です。任意のコードについて、この直線からの差異は、そのコード値の中間から測定されます。

相互変調歪み(IMD)　は、2つの正弦周波数が同時にADC入力へ印加されたとき、その結果として新たなスペクトル成分が発生することです。2つの2次、または4つすべての3次相互変調積の電力と、元の周波数における両方の電力の合計との比率と定義されます。IMDは通常、dBFS単位で表記されます。

欠損コード　は、ADC出力に一切出現しない出力コードです。ADCS747xは、欠損コードが存在しないことが保証されています。

オフセット誤差　は、最初のコード遷移[(000...000)から(000...001)]と、理想値(すなわち、ADCS7476およびADCS7477ではGND + 0.5 LSB、ADCS7478ではGND + 1 LSB)との差異です。

信号対ノイズ比(SNR)　は、入力信号のrms値と、サンプリング周波数の半分より低い他のすべてのスペクトル成分(高調波やDCは含まれません)の合計のrms値との比率で、dB単位で表記されます。

信号対ノイズ+歪み比率(S/N+DまたはSINAD)　は、入力信号のrms値と、クロック周波数の半分より低い他のすべてのスペクトル成分(高調波を含みますが、DCは含まれません)のrms値との比率で、dB単位で表記されます。

スプリアス・フリー・ダイナミック・レンジ(SFDR)　は、入力信号のrms値と、ピーク・スプリアス信号との差で、dB単位で表記されます。このスプリアス信号には、出力スペクトラムに存在し、入力には存在しないすべての信号が含まれます。

全高調波歪み(THD)　は、出力における最初の5つの高調波レベルの合計rmsと、出力の基本波レベルとの比率で、dBc単位で表記されます。THDは次の式で計算されます。

$$THD = 20 \times \log \sqrt{\frac{f_2^2 + . . . + f_6^2}{f_1^2}} \quad (1)$$

ここで

- f_1は、基本波(出力)周波数のRMS電力です。
- f_2からf_6までは、最初の5つの高調波周波数のRMS電力です。

全未調整誤差　は、理想的な伝達関数からの、検出された最大の偏差です。このため、この値はフルスケール誤差、直線性誤差、オフセット誤差を含む包括的な仕様です。

11.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商標

SPI, QSPI, MICROWIRE, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静電気放電に関する注意事項

これらのデバイスは、限定的なESD(静電破壊)保護機能を内蔵しています。保存時または取り扱い時は、MOSゲートに対する静電破壊を防止するために、リード線同士をショートさせておくか、デバイスを導電フォームに入れる必要があります。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADCS7476AIMF/NOPB	Active	Production	SOT-23 (DBV) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X01A
ADCS7476AIMF/NOPB.A	Active	Production	SOT-23 (DBV) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X01A
ADCS7476AIMFE/NOPB	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X01A
ADCS7476AIMFE/NOPB.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X01A
ADCS7476AIMFX/NOPB	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X01A
ADCS7476AIMFX/NOPB.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 125	X01A
ADCS7477AIMF/NOPB	Active	Production	SOT-23 (DBV) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X02A
ADCS7477AIMF/NOPB.A	Active	Production	SOT-23 (DBV) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X02A
ADCS7477AIMFE/NOPB	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X02A
ADCS7477AIMFE/NOPB.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X02A
ADCS7477AIMFX/NOPB	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X02A
ADCS7477AIMFX/NOPB.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X02A
ADCS7478AIMF/NOPB	Active	Production	SOT-23 (DBV) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X03A
ADCS7478AIMF/NOPB.A	Active	Production	SOT-23 (DBV) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X03A
ADCS7478AIMFE/NOPB	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X03A
ADCS7478AIMFE/NOPB.A	Active	Production	SOT-23 (DBV) | 6	250 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X03A
ADCS7478AIMFX/NOPB	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X03A
ADCS7478AIMFX/NOPB.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X03A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

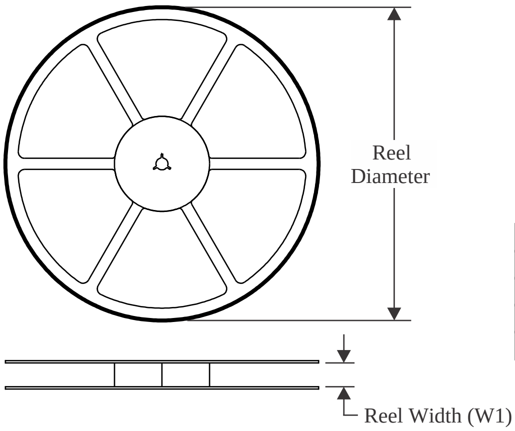
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

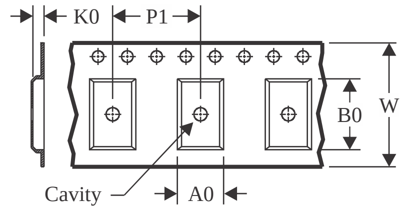
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

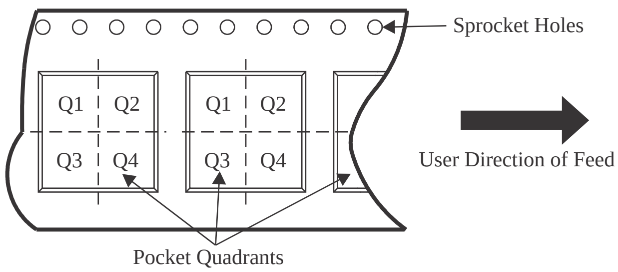


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

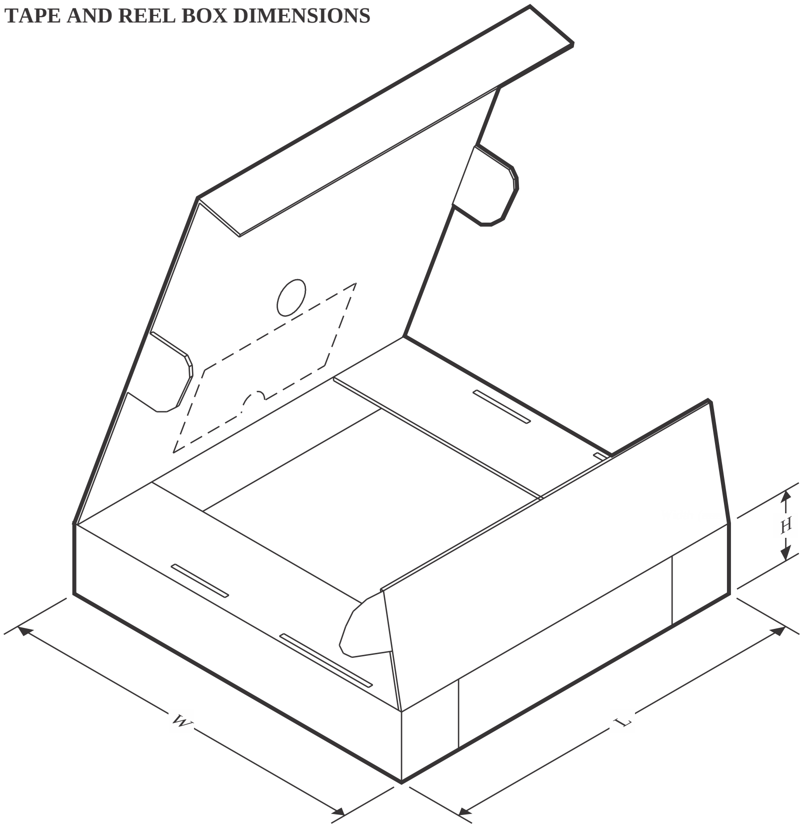
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

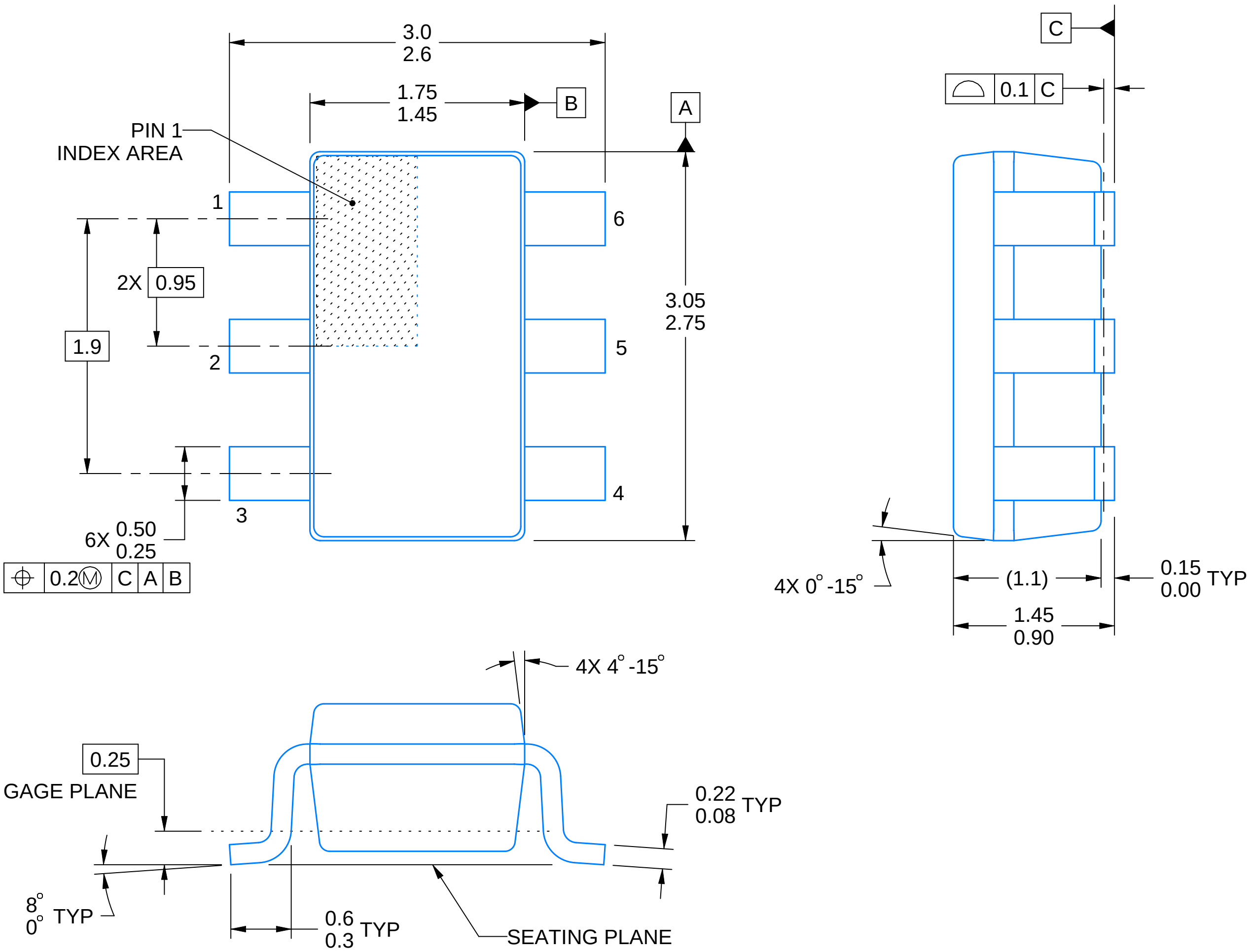
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADCS7476AIMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7476AIMFE/NOPB	SOT-23	DBV	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7476AIMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7477AIMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7477AIMFE/NOPB	SOT-23	DBV	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7477AIMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7478AIMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7478AIMFE/NOPB	SOT-23	DBV	6	250	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADCS7478AIMFX/NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

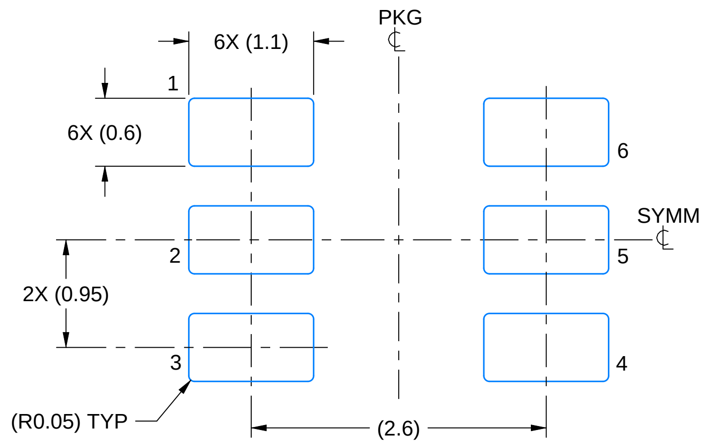
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADCS7476AIMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
ADCS7476AIMFE/NOPB	SOT-23	DBV	6	250	210.0	185.0	35.0
ADCS7476AIMFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
ADCS7477AIMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
ADCS7477AIMFE/NOPB	SOT-23	DBV	6	250	210.0	185.0	35.0
ADCS7477AIMFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
ADCS7478AIMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
ADCS7478AIMFE/NOPB	SOT-23	DBV	6	250	210.0	185.0	35.0
ADCS7478AIMFX/NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0



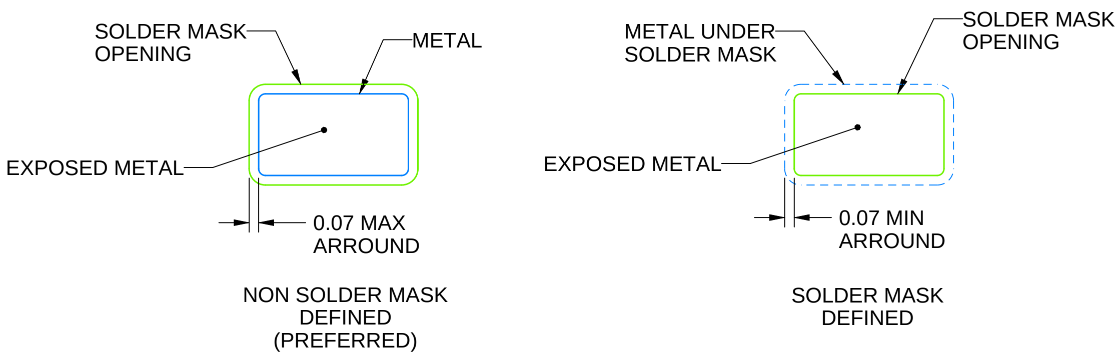
4214840/G 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

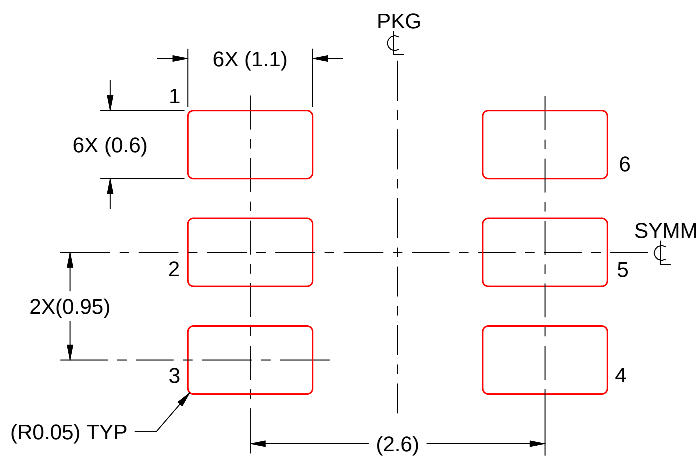


SOLDER MASK DETAILS

4214840/G 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/G 08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

テキサス･インスツルメンツは、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、 テキサス･インスツルメンツ製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した テキサス･インスツルメンツ製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている テキサス･インスツルメンツ製品を使用するアプリケーションの開発の目的でのみ、 テキサス･インスツルメンツはその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。 テキサス･インスツルメンツや第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、 テキサス･インスツルメンツおよびその代理人を完全に補償するものとし、 テキサス･インスツルメンツは一切の責任を拒否します。

テキサス･インスツルメンツの製品は、 テキサス･インスツルメンツの販売条件、または ti.com やかかる テキサス･インスツルメンツ製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。 テキサス･インスツルメンツがこれらのリソースを提供することは、適用される テキサス･インスツルメンツの保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、 テキサス･インスツルメンツはそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265