

ADC3683-SP 放射線耐性保証、18 ビット、デュアル チャネル、1~65MSPS、 低レイテンシ、低ノイズ、超低消費電力の A/D コンバータ (ADC)

1 特長

- スクリーニングと耐放射線特性:
 - QMLV スクリーニングと信頼性
 - 吸収線量 (TID): 300krad (Si)
 - シングル イベント ラッチアップ (SEL):75MeVcm²/mg
- 周囲温度範囲:-55℃~105℃
- デュアル チャネル ADC
- 18 ビット 65MSPS
- ノイズ フロア:-160dBFS/Hz
- 小さい消費電力と最適化された電力スケーリング:
 - 64mW/ch (10MSPS)
 - 84mW/ch (65MSPS)
- レイテンシ:
 - 1線式モードでの1クロックサイクル
 - 2線式モードでの2クロックサイクル
- 18 ビット、ミッシング コードなし
- INL:±7LSB、DNL:±0.7LSB
- 内部または外部のリファレンス
- 入力帯域幅:200MHz (-3dB)
- オプションのデジタル降圧コンバータ (DDC):
 - 実数または複素数のデシメーション
 - デシメーション比:2、4、8、16、32
 - 32 ビット NCO
- シリアル LVDS (SLVDS) インターフェイス (2 線式、1 線式、
- 1/2 線式)
- スペクトル性能 (F_{IN} = 5MHz):
 - 信号対雑音比:83.6dBFS
 - SFDR:87.1dBc
 - HD23 以外:102dBC

2 アプリケーション

- 光学画像処理ペイロード
- レーダー画像処理ペイロード
- 衛星通信ペイロード

3 概要

ADC3683-SP は、低レイテンシ、低ノイズ、超低消費電 力、18 ビット、65MSPS の高速デュアル チャネル A/D コ ンバータ (ADC) です。 最善のノイズ性能を実現するように 設計されており、この ADC は、ノイズ スペクトル密度 -160dBFS/Hz で、優れた直線性とダイナミック レンジを備 えています。 ADC3683-SP は IF サンプリングをサポート すると共に DC 精度を達成しているため、幅広いアプリケ ーションの設計が可能になります。低レイテンシアーキテ クチャ (最小 1 クロック サイクル レイテンシ) と高いサンプ ルレートにより、高速な制御ループも実現できます。この ADC の消費電力は 1 チャネルあたりわずか 84mW (1/2 スイングがイネーブル) (65Msps 時) であり、サンプリング レートにより、消費電力を良好に増減できます。

このデバイスは、シリアル LVDS (SLVDS) インターフェイ スを使用してデータを出力し、デジタル相互接続の数を最 小限に抑えます。このデバイスは、デジタル降圧コンバー タ (DDC) も内蔵しており、データレートの低減とシステム の消費電力の低減に役立ちます。この ADC3683-SP は、14 ビット、125MSPS、ADC3664-SP とピン互換で す。本デバイスは 64 ピンの CFP パッケージ (10.9mm x 10.9mm) で供給され、-55℃~+125℃の温度範囲をサ ポートしています。

ป品情報

部品番号	グレード	パッケージ ⁽¹⁾					
5962F2320401VXC	放射線耐性保証 QML-V	10.0mm v 10.0mm 61 k ²)					
ADC3683HBP/EM ⁽²⁾	エンジニアリング モデル、ノ ンフライト プロトタイプ作業 用	セラミック フラット パック (HBP)					

- (1) 詳細については、セクション 11 を参照してください。
- これらのユニットは、技術的な評価のみを目的としています。規格 (2) に準拠したフローを実施していません (そのため、バーンインはな く、25℃テストのみなど)。さらにこれらのユニットは、認定、量産、 放射線テスト、航空での使用には適していません。部品は、温度ま たは動作寿命全体にわたる性能を保証されていません。



シングル トーン スペクトル、 $F_s = 65MSPS$ 、 $F_{in} =$ 5MHz





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4 Pin Configuration and Functions



図 4-1. HBP Package, 64-Pin CFP (Top View)

表 4-1. Pin Functions	表 4-1.	Pin	Functions
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PIN		TYPE	DESCRIPTION		
NAME	NO.				
INPUT					
AINP	21	I	Positive analog input for ADC A.		
AINM	22	I	Negative analog input for ADC A.		
BINP	60	I Positive analog input for ADC B.			
BINM	59	I	Negative analog input for ADC B.		
CLKP	8	I	Positive sampling clock input for ADCs A & B.		
CLKM	9	I	Negative sampling clock input for ADCs A & B.		
VREF	4	I	External, 1.6V, voltage reference input.		
REFGND	GND 5 I Voltage reference ground. This pin allows close placement of the decoupling capacitor near the VREF input when using either the internal reference or an external reference				
CTRL	6	I	This pin is used to configure the default sampling clock type and voltage reference source upon power up (see セクション 7.5.1). There is an internal 100kΩ pull-up resistor to AVDD.		
PDN/SYNC 3		I	Dual purpose, active high, pin. The pin can be configured to control the power down state of the device or as a synchronization input. The pin functionality can be configured via SPI (default function is PDN). This pin has an internal $21k\Omega$ pull-down resistor.		
RESET	12	I	Active high hardware reset pin. This pin has an internal $21k\Omega$ pull-down resistor.		
DCLKINP	39	I	Positive input for the interface clock. This pin connects to DCLKINM through an internal 100Ω termination resistor.		
DCLKINM 38		I	Negative input for the interface clock. This pin connects to DCLKINP through an internal 100Ω termination resistor.		
OUTPUT	Υ.				
DA0P	29	0	Positive output for interface lane A0.		



PIN		TYPE	DESCRIPTION			
NAME	NO.	TIPE				
DA0M	28	0	Negative output for interface lane A0.			
DA1P	27	0	Positive output for interface lane A1.			
DA1M	26	0	Negative output for interface lane A1.			
DB0P	52	0	Positive output for interface lane B0.			
DB0M	53	0	Negative output for interface lane B0.			
DB1P	54	0	Positive output for interface lane B1.			
DB1M	55	0	Negative output for interface lane B1.			
DCLKP	37	0	Positive output of the interface clock.			
DCLKM	36	0	Negative output of the interface clock.			
FCLKP	42	0	Positive output of the interface frame clock.			
FCLKM	43	0	Negative output of the interface frame clock.			
VCM	11	O Common-mode output voltage of the analog inputs (typically 0.95V).				
SPI						
SEN	25	I	Active low SPI enable. This pin has an internal $21k\Omega$ pull-up resistor to AVDD.			
SCLK	56	I	SPI clock input. This pin has an internal $21k\Omega$ pull-down resistor.			
SDIO	13	I/O	SPI data input or output. This pin has an internal 21k Ω pull-down resistor.			
POWER						
AVDD	7, 24, 57	I	Analog supply input, 1.8V.			
GND	20, 23, 58, 61	I	Ground supply input, 0V.			
IOVDD	35, 44	I	Interface supply input, 1.8V.			
IOGND	40	I	Interface ground supply input, 0V.			
OTHER						
DAP	DAP	-	Die attached pad (thermal pad), connect to GND.			
NC	1, 2, 10, 14, 15, 16, 17, 18, 19, 30, 31, 32, 33, 34, 41, 45, 46, 47, 48, 49, 50, 51, 62, 63, 64	-	No connect pins. Connect to ground or leave floating. ⁽¹⁾			

表 4-1. Pin Functions (続き)

(1) Thermal pad and top metal lid are connected to pin 17. Can be grounded or no connect.



5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Supply voltage range, AVDD, IOVDD		-0.3	2.1	V
Supply voltage range, GND, IOGND, REFGND		-0.3	0.3	V
	AINP/M, BINP/M, CLKP/M, VREF, CTRL	-0.3	MIN(2.1, AVDD+0.3)	
input pins	PDN/SYNC, RESET, SCLK, SEN, SDIO	-0.3	MIN(2.1, AVDD+0.3)	V
	DCLKINP/M	-0.3	MIN(2.1, IOVDD+0.3)	
Junction temperature, T _J			125	°C
Storage temperature	, T _{stg}	-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
V	Electrostatic	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins ⁽¹⁾	1000	V
V(ESD)	discharge	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	250	v

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply	AVDD ⁽¹⁾	1.75	1.8	1.85	V
voltage range	IOVDD ⁽¹⁾	1.75	1.8	1.85	V
T _A	Operating free-air temperature	-55		105	°C
TJ	Operating junction temperature			105 <mark>(2)</mark>	°C

(1) Measured with respect to GND.

(2) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

5.4 Thermal Information

		ADC3683-SP		
	THERMAL METRIC ⁽¹⁾	HBP (CFP)	UNIT	
		64 Pins		
R _{OJA}	Junction-to-ambient thermal resistance	28.4	°C/W	
R _{OJC(top)}	Junction-to-case (top) thermal resistance	12.0	°C/W	
R _{OJB}	Junction-to-board thermal resistance	14.1	°C/W	
Ψ_{JT}	Junction-to-top characterization parameter	7.8	°C/W	
Ψ_{JB}	Junction-to-board characterization parameter	13.8	°C/W	
R _{OJC(bot)}	Junction-to-case (bottom) thermal resistance	7.0	°C/W	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.



5.5 Electrical Characteristics - Power Consumption

Typical values are at $T_A = 25^{\circ}$ C, full temperature range is $T_{MIN} = -55^{\circ}$ C to $T_{MAX} = 105^{\circ}$ C, ADC sampling rate = 65MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8V, external 1.6V reference, and -1dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT			
ADC3683-	ADC3683-SP: 65MSPS								
1	Analog outputy ourrent	Internal reference		69					
AVDD	Analog supply current	External reference		63	83.5	mA			
IIOVDD	/DD I/O supply current	2-wire		41	48.5				
P _{DIS}	Power dissipation	External reference, 2-wire		187	232	mW			
		2-wire, 1/2-swing		34					
		4x real decimation, 1-wire		46		mA			
		4x real decimation, 1/2-wire		47					
	1/O oupply ourropt	16x real decimation, 1-wire		43					
IOVDD	OVDD I/O supply current	16x real decimation, 1/2-wire		43					
		4x complex decimation, 1-wire		48					
		16x complex decimation, 1-wire		43					
		16x complex decimation, 1/2-wire		44					
D	Power consumption in global power DIS down mode	Default mask settings, internal reference		8		m\//			
DIS		Default mask settings, external reference		10		TTVV			



5.6 Electrical Characteristics - DC Specifications

Typical values are at $T_A = 25^{\circ}$ C, full temperature range is $T_{MIN} = -55^{\circ}$ C to $T_{MAX} = 105^{\circ}$ C, ADC sampling rate = 65MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8V, 1.6V external reference, and -1dBFS differential input, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURA	CY					
No missing co	des		18			bits
PSRR	Power supply rejection ratio	F _{IN} = 1MHz		50		dB
DNL	Differential nonlinearity	F _{IN} = 5MHz	-0.9	±0.7	1.8	LSB
INL	Integral nonlinearity	F _{IN} = 5MHz		±7	±23.5	LSB
V _{OS}	Input offset			±130	±510	LSB
V _{OS_DRIFT}	Offset drift			±0.2		LSB/ºC
	Gain error and internal reference	Both channels are powered up	-5.5	±2.1	5.5	%FSR
Error	combined error	F _s = 10MSPS, both channels are powered up	-3	±0.5	3	%FSR
		Both channels are powered up	-5.2	±1.3	5.2	%FSR
	Gain error	F _s = 10MSPS, both channels are powered up	-2.5	±0.2	2.5	%FSR
		External 1.6V reference		68		ppm/ºC
	Gain drift	Internal reference		242		ppm/ºC
Transition nois	se			5		LSB
ADC ANALO	G INPUT (AINP/M, BINP/M)				I	
FS	Input full scale	Differential		3.2		V _{pp}
V _{CM}	Input common-mode voltage			0.95		V
R _{IN}	Differential input resistance	F _{IN} = 100kHz		8		kΩ
C _{IN}	Differential input capacitance	F _{IN} = 100kHz		7		pF
V _{OCM}	Output common-mode voltage			0.95		V
BW	Analog input bandwidth (-3dB)			200		MHz
INTERAL VO	LTAGE REFERENCE					
V _{REF}	Internal reference voltage			1.6		V
V _{REF} output in	npedance			8		Ω
EXTERNAL V						
V _{REF}	External voltage reference			1.6		V
Input current				0.35		mA
Input impedan	ce			5.3		kΩ
CLOCK INPU	T (CLKP/M)		1			
Input clock fre	quency		1		65	MHz
V _{ID}	Differential input voltage		0.5	1		V _{pp}
V _{CM}	Input common-mode voltage			0.9		V
R _{IN}	Single-ended input resistance to common mode			5		kΩ
C _{IN}	Single-ended input capacitance			1.5		pF
Clock duty cyc	cle		40	50	60	%

5.6 Electrical Characteristics - DC Specifications (続き)

Typical values are at $T_A = 25^{\circ}$ C, full temperature range is $T_{MIN} = -55^{\circ}$ C to $T_{MAX} = 105^{\circ}$ C, ADC sampling rate = 65MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8V, 1.6V external reference, and -1dBFS differential input, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPU	JTS (RESET, PDN, SCLK, <u>SEN</u> , SDIO)					
V _{IH}	High level input voltage		1.5			V
V _{IL}	Low level input voltage				0.3	V
I _{IH}	High level input current			90	150	uA
IIL	Low level input current		-150	-90		uA
CI	Input capacitance			1.5		pF
DIGITAL OUTPUT (SDOUT)						
V _{OH}	High level output voltage	I _{LOAD} = -400uA	IOVDD - 0.1	IOVDD		V
V _{OL}	Low level output voltage	I _{LOAD} = 400uA			0.1	V
SLVDS INTER	RFACE					
LVDS lane rat	e				1	Gbps
V _{ID}	DCLKIN differential input voltage		200	350		mV _{pp}
V _{CM}	DCLKIN input common-mode voltage		1.1	1.2	1.3	V
V _{OD}	Differential output voltage		0.585	700	0.785	mV _{pp}
V _{CM}	Output common-mode voltage		0.85	1.0	1.15	V



5.7 Electrical Characteristics - AC Specifications

Typical values are at $T_A = 25^{\circ}$ C, full temperature range is $T_{MIN} = -55^{\circ}$ C to $T_{MAX} = 105^{\circ}$ C, ADC sampling rate = 65MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8V, 1.6V external reference, and -1dBFS differential input, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
ADC3683-SF	P: 65MSPS							
NSD	Noise spectral density	F _{IN} = 1.1MHz, A _{IN} = –20dBFS		-160		dBFS/Hz		
		F _{IN} = 1.1MHz, A _{IN} = –20dBFS		84.8				
		F _{IN} = 1.1 MHz		84.2				
		F _{IN} = 5MHz	78	83.6				
SNR	Signal to noise ratio	F _{IN} = 10MHz		83.6		dBFS		
		F _{IN} = 20MHz		82.6				
		F _{IN} = 40MHz		81.0				
		F _{IN} = 70MHz		77.3				
		F _{IN} = 1.1MHz		80.0				
		F _{IN} = 5MHz		82.7				
	Signal to noise and	F _{IN} = 10MHz		82.7				
SINAD	distortion ratio	F _{IN} = 20MHz		80.2		abes		
		F _{IN} = 40MHz		78.7				
		F _{IN} = 70MHz		75.8				
		F _{IN} = 1.1MHz		13.7				
	Effective number of bits	F _{IN} = 5MHz		13.6		bits		
ENOD		F _{IN} = 10MHz		13.6				
ENOB		F _{IN} = 20MHz		13.4				
		F _{IN} = 40MHz		13.2				
		F _{IN} = 70MHz		12.5				
	Total harmonic distortion	F _{IN} = 1.1MHz		81				
		F _{IN} = 5MHz	76.5	88		dBc		
TUD		F _{IN} = 10MHz		89				
THD	(first five harmonics)	F _{IN} = 20MHz		83				
		F _{IN} = 40MHz		82				
		F _{IN} = 70MHz		80				
		F _{IN} = 1.1MHz		82				
		F _{IN} = 5MHz	78.5	89				
SEDD	Spurious free dynamic range	F _{IN} = 10MHz		92		dPo		
SEDI	harmonic distortion	F _{IN} = 20MHz		85		UDC		
		F _{IN} = 40MHz		84				
		F _{IN} = 70MHz		82				
		F _{IN} = 1.1MHz		101				
		F _{IN} = 5MHz	85	101				
	Spurious free dynamic range	F _{IN} = 10MHz		100		ARES		
	(excluding HD2 and HD3)	F _{IN} = 20MHz		97		UDFS		
		F _{IN} = 40MHz		91				
		F _{IN} = 70MHz		88				
	Two tone inter-modulation	$F_1 = 10MHz$, $F_2 = 12MHz$, $A_{IN} = -7dBFS/tone$		83		dPo		
	distortion	F_1 = 40MHz, F_2 = 45MHz, A_{IN} = -7dBFS/tone		78		UDC		

5.8 Timing Requirements

Typical values are at $T_A = 25^{\circ}$ C, MIN and MAX timing values are characterized over the full temperature range $T_{MIN} = -55^{\circ}$ C to $T_{MAX} = 105^{\circ}$ C and are NOT production tested, ADC sampling rate = 65MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8V, 1.6V external reference, and -1dBFS differential input, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN NOM	MAX	UNIT		
ADC TIMI	NG SPECIFICATIONS						
t _{AD}	Aperture delay		0.85		ns		
t _A	Aperture jitter	Square wave clock with fast edges	180		fs		
		F _S = 10Msps	-T _S /2		Sampling		
t _{ACQ}	Signal acquisition period, referenced to sampling clock falling edge	F _S = 25Msps	-T _S /2		clock		
		F _S = 65Msps	-T _S /4		period		
t _{conv}		F _S = 10Msps	+T _S × 1/5		Sampling clock period		
	Signal conversion period, referenced to sampling clock falling edge	F _S = 25Msps	+T _S × 3/8				
		F _S = 65Msps	+T _S × 5/8	+T _S × 5/8			
Wake up time	Time to valid data after coming out of power down	External 1.6V reference, differential sampling clock		100	μs		
t _{S,SYNC}	Setup time for SYNC input signal	Peteropood to compling clock riging edge		500			
t _{H,SYNC}	Hold time for SYNC input signal			600	ps		
		SLVDS 2-wire	2		ADC		
		SLVDS 1-wire	1		clock		
ADC	Signal input to data output	SLVDS 1/2-wire	1		cycles		
latency		Real decimation by 2	21		Output clock		
		Complex decimation by 2	22				
		Real or complex decimation by 4, 8, 16, 32	23		cycles		



5.8 Timing Requirements (続き)

Typical values are at $T_A = 25^{\circ}$ C, MIN and MAX timing values are characterized over the full temperature range $T_{MIN} = -55^{\circ}$ C to $T_{MAX} = 105^{\circ}$ C and are NOT production tested, ADC sampling rate = 65MSPS, 50% clock duty cycle, AVDD = IOVDD = 1.8V, 1.6V external reference, and -1dBFS differential input, unless otherwise noted.

	PARAMETER	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INTERFAC	E TIMING: SERIAL LVDS INTERFACE					
teo	Propagation delay: sampling clock falling edge to DCLK rising edge	Delay between sampling clock falling edge to DCLKIN falling edge < 2.5ns. t_{DCLK} = DCLK period t_{CDCLK} = Sampling clock falling edge to DCLKIN falling edge	2 + t _{DCLK} + t _{CDCLK}	3 + t _{DCLK} + t _{CDCLK}	4 + t _{DCLK} + t _{CDCLK}	ns
		Delay between sampling clock falling edge to DCLKIN falling edge >= 2.5ns. t_{DCLK} = DCLK period t_{CDCLK} = Sampling clock falling edge to DCLKIN falling edge	2 + t _{CDCLK}	3 + t _{CDCLK}	4 + t _{CDCLK}	ns
		F _{out} = 10MSPS, data rate = 90MBPS, 2-wire	0	0.1	0.3	
		F _{out} = 65MSPS, data rate = 585MBPS, 2-wire	0	0.1	0.3	
t	DCLK rising edge to output data delay	F _{out} = 10MSPS, data rate = 180MBPS, 1-wire	0.1	0.2	0.3	ns
^L CD		F _{out} = 55MSPS, data rate = 990MBPS, 1-wire	-0.4	0.1	0.3	
		F _{out} = 5MSPS, data rate = 180MBPS, 1/2-wire	0	0.1	0.3	
		F _{out} = 25MSPS, data rate = 720MBPS, 1/2-wire	0	0.1	0.3	
	Data valid	F _{out} = 10MSPS, DA/B0,1 = 90MBPS, 2-wire	10.5	10.7	10.8	
		F _{out} = 65MSPS, DA/B0,1 = 585MBPS, 2-wire	1.3	1.4	1.5	ns
tov		F _{out} = 10MSPS, DA/B0 = 180MBPS, 1-wire	4.7	4.8	4.9	
^v Dv		F _{out} = 55MSPS, DA/B0 = 990MBPS, 1-wire	0.5	0.6	0.75	
		F _{out} = 5MSPS, DA0 = 180MBPS, 1/2-wire	4.7	4.8	4.9	
		F _{out} = 25MSPS, DA0 = 900MBPS, 1/2-wire	0.6	0.7	0.85	
SERIAL PF	ROGRAMMING INTERFACE (SCLK, S	EN, SDIO) - INPUT				
f _{CLK(SCLK)}	Serial clock frequency				20	MHz
t _{SU(SEN)}	SEN to rising edge of SCLK				11	ns
t _{H(SEN)}	SEN from rising edge of SCLK				18	ns
t _{SU(SDIO)}	SDIO to rising edge of SCLK				18	ns
t _{H(SDIO)}	SDIO from rising edge of SCLK				11	ns
SERIAL PF	ROGRAMMING INTERFACE (SDIO) - (OUTPUT				
t _(OZD)	SDIO HiZ to LoZ				20	ns
t _(ODZ)	SDIO LoZ to HiZ				18	ns
t _(OD)	Falling edge of SCLK to SDIO data valid				20	ns



5.9 Typical Characteristics





5.9 Typical Characteristics (continued)





5.9 Typical Characteristics (continued)





5.9 Typical Characteristics (continued)





6 Parameter Measurement Information



図 6-1. Timing diagram: 2-wire



図 6-2. Timing diagram: 1-wire

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Input Signal



図 6-3. Timing diagram: 1/2-wire



7 Detailed Description

7.1 Overview

The ADC3683-SP is a low latency, low noise, and ultra low power 18-bit high speed dual channel ADC with a max sampling rate of 65MSPS. It is intended for use in space applications with mission profiles of total ionizing dose (TID) less than 300krad (Si) and single event latch-up (SEL) of less than 75MeV-cm²/mg. The ADC has an internal reference option and supports the use of an external, high precision, 1.6V reference (see $\pm 29 \ge 27$.3.3). Optionally, integrated programmable digital down converters (DDCs) enable output data rate reduction and channelization (see $\pm 29 \ge 27$.3.5). The DDCs, if operated in a complex decimation mode, offer a 32-bit programmable NCO for complex mixing. The DDCs also support a real decimation mode with no mixing.

The ADC3683-SP uses a serial LVDS (SLVDS) interface to output the data which minimizes the number of digital interconnects (see 2222 7.3.4.2). The SLVDS interface can be configured to one of the following modes: two LVDS lanes per channel (2-wire), one LVDS lane per channel (1-wire), or a single lane mode (1/2-wire) where both channels are multiplexed on the same LVDS lane. The device supports configurable output resolutions from 14-bit to 20-bit. Due to the inherent low latency ADC architecture, the digital output result is available after only one or two clock cycles depending on the output interface mode.

The ADC3683-SP is intended to be controlled through the Serial Peripheral Interface (SPI) by configuring registers (セクション 7.5); however, the CTRL pin can also be used to configure the voltage reference source and sampling clock input type upon power up.

7.2 Functional Block Diagram



図 7-1. Simplified Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The analog inputs of the ADC3683-SP are intended to be driven differentially. Both AC coupling and DC coupling of the analog inputs is supported. The analog inputs are designed for an input common-mode voltage of 0.95V which must be provided externally on each input pin. \boxtimes 7-2 shows the analog input model of the ADCs. First, 8 switches are closed during acquisition for a period of t_{ACQ}. Then, all switches are open for a period of t_{CONV}. Finally, before the next acquisition period, the reset switch is closed for a period of t_{RST}.



🛛 7-2. Analog Input Model



7.3.1.1 Analog Input Bandwidth

 \boxtimes 7-3 shows the analog full power input bandwidth of the ADC3683-SP with a 50 Ω differential termination. The -3dB bandwidth is approximately 200MHz. The ADC architecture limits the full power bandwidth to 65MHz; therefore, to avoid significantly degrading the ADC performance. The recommendation is that the input power is decreased linearly with increasing input frequency above 65MHz.



図 7-3. ADC Analog Input Bandwidth Response



7.3.1.2 Analog Front End Design

The ADC3683-SP should be used with a passive filter to absorb the glitches on the input due to sampling. Additionally, a passive DC bias circuit is needed in AC-coupled applications which can be combined with a termination network.

7.3.1.2.1 Sampling Glitch Filter

The sampling glitch filter is designed to optimize the SNR and HD3 performance of the ADC. The filter performance is dependent on input frequency: therefore, the following filter designs are recommended for different input frequency ranges as shown in \boxtimes 7-4 and \boxtimes 7-5 (assuming a 50 Ω source impedance).



図 7-4. Sampling Glitch Filter for Input Frequencies from 0Hz to 30MHz



図 7-5. Sampling Glitch Filter for Input Frequencies from 30MHz to 70MHz



7.3.1.2.2 AC Coupling

The ADC3683-SP analog inputs require an external DC bias to the common-mode voltage (VCM) of the ADC when the input is AC coupled. An example AC coupled input network is shown in \boxtimes 7-6.



図 7-6. AC Coupled Input Network

7.3.1.2.3 DC Coupling

In DC coupled applications, the DC bias needs to be provided from the driver (typically a fully differential amplifier or FDA) using the VCM output of the ADC as shown in \boxtimes 7-7.



図 7-7. DC Coupled Input Network



7.3.2 Clock Input

To maximize the ADC3683-SP SNR performance, the external sampling clock should be a low jitter differential signal. The device provides the option to operate with a single-ended clock input to reduce the device power consumption and simplify system design at the expense of performance.

7.3.2.1 Differential Vs Single-ended Clock Input

The ADC3683-SP can be operated using a differential or a single-ended clock input where the single-ended clock input consumes less power at the expense of performance.

- Differential clock input mode: the clock input must be AC coupled externally. The ADC3683-SP has an internal DC bias.
- Single-ended clock input mode: this mode is configured either using SPI (D3 and D0 of 0x0E), or with the CTRL pin. In this mode, there is no internal clock biasing. The clock input needs to be DC coupled with a common-mode voltage of 0.9V. The unused clock input should be AC coupled to ground.

7.3.2.2 Signal Acquisition Time Adjust

The ADC3683-SP includes a register (D2 of 0x11) to power down an internal DLL which increases the signal acquisition time for sample rates below 30MSPS from 25% to 50% of the clock period. When powering down the DLL, the acquisition time tracks the clock duty cycle.

SAMPLING CLOCK F _S (MSPS)	DLL_PDN (D2 of 0x11)	ACQUISITION TIME (t _{ACQ})						
> 30	0	T _S / 4						
≤ 30	1	T _S / 2						

表 7-1. Acquisition Time Vs DLL_PDN Setting

7.3.3 Voltage Reference

The ADC3683-SP provides two different options for supplying the voltage reference to the ADCs. The first option is an internal 1.6V reference. The second option is an external 1.6V reference that can be directly connected to the VREF input for best performance. The reference noise can be filtered by connecting a 10μ F and a 0.1μ F ceramic bypass capacitor to the VREF pin irrespective of the reference source (internal or external).

注

The voltage reference mode can be selected via SPI or by using the CTRL pin ($222 \times 7.5.1$). If the CTRL pin is not used for configuration, the CTRL pin should be connected to AVDD and the voltage reference may be selected via SPI.



7.3.3.1 Internal Voltage Reference

The ADC3683-SP has a 1.6V reference that may be used in the absence of an external reference. A 10μ F decoupling capacitor and a 0.1μ F decoupling capacitor should be connected between VREF and REFGND. The capacitors should be placed as close to the device pins as possible.



☑ 7-8. Internal Reference Mode

7.3.3.2 External Voltage Reference

For the highest accuracy and best drift performance, the ADC3683-SP reference voltage can be sourced externally. When using an external reference, the VREF pin can be directly connected to an external 1.6V reference. A 10 μ F decoupling capacitor and a 0.1 μ F decoupling capacitor should be connected between VREF and REFGND. The capacitors should be placed as close to the device pins as possible.



☑ 7-9. External Reference Mode



7.3.4 Digital Data Path & Interface

The ADC3683-SP uses a serial LVDS (SLVDS) interface to output the ADCs' data which minimizes the number of digital interconnects. The SLVDS interface can be configured to one of the following modes: two LVDS lanes per channel (2-wire), one LVDS lane per channel (1-wire), or a half-lane mode (1/2-wire) option where both channels are multiplexed on a single LVDS lane. The device supports configurable output resolutions from 14-bit to 20-bit.

The ADC3683-SP requires an external interface clock (DCLKIN). A delayed version of DCLKIN is used as the interface output clock (DCLK).

7.3.4.1 Data Path Overview

The ADC3683-SP offers a flexible set of digital signal processing (DSP) features (\boxtimes 7-10) where all or a subset of the features can be used. The ADC cores provide an 18-bit output which can be passed to the digital down converters (DDCs) or directly provided to the digital interface. Since the ADC core offers very low latency, the DSP features have to be disabled (D2 of 0x24) for the lowest latency.

Before data is sent on the data lanes, the data first passes through a resolution selection block and then an output bit mapper. The resolution selector offers selection of output resolutions: 14-bit, 16-bit, 18-bit, or 20-bit. For 14-bit and 16-bit output resolutions, the LSBs are truncated during the reformatting. Note, in 20-bit output mode, if the DDCs are not used, then two zeros are simply appended as LSBs. The output bit mapper maps each data bit to a position within the data stream for each active lane.



☑ 7-10. Digital Data Path Overview



7.3.4.2 Digital Interface

7-2 provides an overview for the resulting serialization factor depending on output resolution and interface mode. The output serialization factor is internally adjusted based on the interface mode setting and resolution; however, the maximum SLVDS interface output data rate of 1Gbps can not be exceeded regardless of the interface settings. Note, the DCLKIN frequency needs to be adjusted accordingly as well. For example, changing the output resolution from 18-bit to 16-bit in 2-wire mode results in DCLKIN equaling F_S * 4 instead of F_S * 4.5.

The programming sequence for changing the output interface and/or resolution is shown in セクション 7.5.3.

注 When possible, interface modes that allow for an integer ratio between the DCLKIN frequency and the sample clock (CLK) frequency are recommended. This eases meeting the DCLKIN to CLK timing requirements described in セクション 7.3.4.3.

注

Since the ADC3683-SP SNR is very high, the LVDS outputs can potentially couple and degrade the SNR. Therefore, a half swing LVDS mode is provided to reduce the LVDS output swing and minimize coupling. When possible, enable half swing (D6 of 0x1A) to minimize degrading the ADC SNR.

Output Resolution	Interface	Serialization Factor	FCLK	DCLKIN	DCLK	Data Rate			
	2-Wire	7x	F _S /2	F _S * 3.5	F _S * 3.5	F _S * 7			
14-bit	1-Wire	14x	F _S	F _S * 7	F _S * 7	F _S * 14			
	1/2-Wire	28x	Fs	F _S * 14	F _S * 14	F _S * 28			
16-bit	2-Wire	8x	F _S /2	F _S * 4	F _S * 4	F _S * 8			
	1-Wire	16x	Fs	F _S * 8	F _S * 8	F _S * 16			
	1/2-Wire	32x	Fs	F _S * 16	F _S * 16	F _S * 32			
	2-Wire	9x	F _S /2	F _S * 4.5	F _S * 4.5	F _S * 9			
18-bit	1-Wire	18x	Fs	F _s * 9	F _S * 9	F _S * 18			
	1/2-Wire	36x	Fs	F _S * 18	F _S * 18	F _S * 36			
20-bit	2-Wire	10x	F _S /2	F _S * 5	F _S * 5	F _S * 10			
	1-Wire	20x	Fs	F _S * 10	F _S * 10	F _S * 20			
	1/2-Wire	40x	Fs	F _S * 20	F _S * 20	F _S * 40			

表 7-2. Digital Interface Modes

7.3.4.3 DCLKIN

DCLKIN is an external clock to the ADC3683-SP where a delayed version of this clock is used as the output interface clock (DCLK). DCLKIN can be configured for external or internal biasing to a 1.2V common-mode voltage via SPI (D5 of 0x244). DCLKIN also has an internal 100Ω termination resistor.

注 DCLKIN can be a maximum of 500MHz which limits the LVDS lanes to a maximum of 1Gbps per lane as data is sent on both rising edge and falling edge of DCLK.

Given the low latency architecture of the ADC3683-SP, the relationship between the sample clock (CLK) and DCLKIN needs to be controlled. DCLKIN and CLK must be phase locked to the same reference frequency. The falling edges of CLK and DCLKIN need to be 2.5ns apart otherwise a timing violation occurs. If a timing violation is observed, an internal timing violation detection circuit adds a 1ns delay between CLK and DCLKIN. The effect of this detection circuit is observed as a change in the t_{PD} specification by one DCLK cycle.

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7.3.4.4 Output Scrambler

The ADC3683-SP includes an optional output scrambler feature in 2-wire mode only. The scrambler can enabled by enabling the DSP features (D2 of 0x24) and enabling scrambling (D6 of 0x22). When enabled, each sample is split into two halves. Each half of the samples stream is scrambled independently. For example, if the samples stream is at an 18-bit resolution, the stream is divided into two halves consisting of bits D17-D9 & D8-D0. The two halves are fed into independent scrambling blocks where each input bit (x[k]) of each scrambler is XOR-ed with 2 previous bits (y[k-14] and y[k-15]) as shown in \mathbb{X} 7-11. Since this is a self-synchronizing scrambler, the start up state of the scrambler can be ignored.



☑ 7-11. Scrambler and Descrambler Operation

注

The sample streams fed into each scrambler are fed to the scrambler LSB first. Therefore, in the previous example, the sample stream half consisting of D8-D0 is provided to the scrambler with D0 first as x[k] followed by D1 as x[k+1] and so on.

For proper descrambling, the sample stream halves must be descrambled independently then the descrambled data can be used to reconstruct the samples. On the receiver side, the incoming serial data stream can be descrambled by XOR-ing each incoming bit (y[k]) with 2 previous bits (y[k-14] and y[k-15]).



注

Since the scramblers are looking at the two halves of the sample stream, the output bit mapper needs to be configured such that each lane contains only one of the sample halves.

For example, in 2-wire and 18-bit mode, by default (\boxtimes 6-1), one lane carries the odd bits (D17, D15, D13, etc.) and one lane carries the even bits (D16, D14, D12, etc.). When scrambling is enabled, the bit mapper needs to be configured so that one lane carries bits D9-D17 and the other lane carries D0-D8 (LSB first for each lane). An example data flow diagram of scrambling an 18-bit sample stream is shown in \boxtimes 7-12, where D17:D0 is the sample provided by the ADC after the resolution select block, the sample is split into D0-D8 and D9-D17 and fed into each scrambler (LSB first) and S0-S17 are the resultant scrambled bits.



図 7-12. 18-bit Scrambling Example



7.3.4.5 Output Bit Mapper

The output bit mapper sits right before the physical output interface and dictates the transmitted bit order on each active lane. Each sample bit is uniquely identifiable by a value as shown in $\frac{1}{27}$ 7-3. Similarly, each bit position in each lane is also uniquely identifiable with each bit position having an independent register address. To map a specific bit to a specific bit position (and a specific lane), the value for the bit from the $\frac{1}{27}$ 7-3 needs to be written to the address corresponding to the desired bit position in the desired lane.

The ADC3683-SP supports a maximum output resolution of 20-bit; therefore, there are 20-bits that are uniquely identifiable per channel. In 2-wire mode, two samples are considered part of the same frame; therefore, there are two sets of 20-bits each, one for the previous sample and another for the current sample. $\forall p \forall \exists \forall 7.3.4.5.1$, $\forall p \forall \exists \forall 7.3.4.5.2$, and $\forall p \forall \exists \forall 7.3.4.5.3$ provide the register addresses that correspond to each bit position in each lane for 2-wire, 1-wire, and 1/2-wire, respectively.

BIT_ID	Chan	nel A	Channel B		
	Previous sample (2w only)	Current sample	Previous sample (2w only)	Current sample	
D19 (MSB)	0x2D	0x6D	0x29	0x69	
D18	0x2C	0x6C	0x28	0x68	
D17	0x27	0x67	0x23	0x63	
D16	0x26	0x66	0x22	0x62	
D15	0x25	0x65	0x21	0x61	
D14	0x24	0x64	0x20	0x60	
D13	0x1F	0x5F	0x1B	0x5B	
D12	0x1E	0x5E	0x1A	0x5A	
D11	0x1D	0x5D	0x19	0x59	
D10	0x1C	0x5C	0x18	0x58	
D9	0x17	0x57	0x13	0x53	
D8	0x16	0x56	0x12	0x52	
D7	0x15	0x55	0x11	0x51	
D6	0x14	0x54	0x10	0x50	
D5	0x0F	0x4F	0x0B	0x4B	
D4	0x0E	0x4E	0x0A	0x4A	
D3	0x0D	0x4D	0x09	0x49	
D2	0x0C	0x4C	0x08	0x48	
D1	0x07	0x47	0x03	0x43	
D0 (LSB)	0x06	0x46	0x02	0x42	

表 7-3. Unique Bit Identifiers



7.3.4.5.1 2-Wire Mode

In 2-wire mode, both the current sample and the previous sample columns of $\frac{1}{2}$ 7-3 are used. Furthermore, each BIT_ID for the current and previous sample in $\frac{1}{2}$ 7-3 needs to be mapped to a specific address which indicates the position of the bit in the respective lane. The address space order is different for 14-bit/18-bit resolutions and 16-bit/20-bit resolutions. The bit mapper address space is also different for each lane.

注 Depending on the resolution, there can be unused addresses between samples which can be skipped. For example, going from 18-bit resolution to 14-bit, the addresses corresponding to the last two LSBs per lane can be ignored.

 \boxtimes 7-13 and \boxtimes 7-14 show register addresses that correspond to the bit positions for each resolution setting and lane. The default values shown for each address are after configuring the ADC3683-SP into the 2-wire interface mode.



図 7-13. Default Bit Mapping for 2-wire, 14-bit/18-bit



図 7-14. Default Bit Mapping for 2-wire, 16-bit/20-bit

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⊠ 7-15 shows how the bit mapper can be configured to support 16-bit scrambled output. The bit mapper is configured so that the top and bottom halves of the samples are sent on separate lanes and the bits are sent out LSB first as described in $\forall 2 \forall 2 \Rightarrow 7.3.4.4$.



図 7-15. Example of Configuring the Bit Mapper for 16-bit Scrambled Output

7.3.4.5.2 1-Wire Mode

☑ 7-16 shows the register addresses that correspond to the bit positions for each resolution setting and lane used for 1-wire mode. The default values shown for each address are after configuring the ADC3683-SP into the 1-wire interface mode.



図 7-16. Default Bit Mapping for 1-wire

7.3.4.5.3 1/2-Wire Mode

In 1/2-wire mode, both channels multiplexed on the same lane and is provided only on lane DA0. \boxtimes 7-17) shows the register addresses that correspond to the bit positions on the lane for each resolution setting in 1-wire mode. The default values shown for each address are after configuring the ADC3683-SP into the 1/2-wire interface mode.





図 7-17. Default Bit Mapping for 1/2-wire

7.3.4.6 Output Data Format

The ADC3683-SP samples can be configured for either two's complement format (default) or offset binary via SPI (D2 of 0x8F and 0x92). \gtrsim 7-4 provides an overview for minimum and maximum output codes for the two formatting options based on resolution.

	Two's Complement (default)				Offset Binary			
RESOLUTION (BIT)	14	16	18	20	14	16	18	20
V _{IN,MAX}	0x1FFF	0x7FFF	0x1FFFF	0x7FFFF	0x3FFF	0xFFFF	0x3FFFF	0xFFFFF
0	0x0	0x0000		0x00000		0x8000	0x20000	0x80000
V _{IN,MIN}	0x2000	0x8000	0x20000	0x80000	0x0000		0x00	0000

表 7-4. Minimum and Maximum ADC Codes

7.3.4.7 Test Pattern

 \boxtimes 7-10 shows the location of the test pattern blocks within the device. When the digital signal processing (DSP) features are disabled (D2 of 0x24), a test pattern block can be enabled to replace the ADC data. Similarly, when using the DDC, a test pattern is available to replace the DDC data.

注 No test pattern block is available when the DSP features are enabled and the DDC is not used.

Each test pattern block has the capability to generate one of the following outputs:

- Ramp pattern with programmable step size set by PAT_DATA.
- Constant pattern with a programmable custom pattern set by PAT_DATA.

As shown in \boxtimes 7-10, there are two test pattern blocks, test pattern 0 and test pattern 1. The test pattern mode for each block can be configured via D7:D5 and D4:D2 of 0x16. A shared set of data bits (PAT_DATA) is given to the test pattern blocks and this data is used as ramp pattern step size and/or the constant pattern. The PAT_DATA is an 18-bit value located across three different registers: D17:D16 in 0x16, D15:D8 in 0x15, and D7:D0 in 0x14. The PAT_DATA is MSB aligned. For example, if the device is configured for 14-bit resolution and constant pattern, only the top 14-bits of the PAT_DATA are used for the constant pattern. Additionally, in ramp mode, the test pattern counter operates at a 18-bit resolution; therefore, the ramp pattern step size must be configured based on the desired resolution and the step size at that resolution.

- The test pattern data must be configured to the following for a step size of one at each resolution:
 - 0x00001: 18-bit output resolution
 - 0x00004: 16-bit output resolution
 - 0x00010: 14-bit output resolution



7.3.5 Digital Down Converter

The ADC3683-SP includes an optional digital down converters (DDCs). The DDCs Supports real and complex decimation by 2, 4, 8, 16 and 32. Additionally, each DDC has a 32-bit numerically controlled oscillator (NCO) available in complex decimation.

Internally, the DDC data path operates at a 20-bit resolution to avoid any SNR degradation due to quantization. Depending on the configured resolution, the DDC output is truncated to the selected resolution prior to outputting the data on the digital interface.

⊠ 7-18 shows a detailed view of the DDCs. The DDC MUX maps one of three different inputs to each DDC. By default, ADC A and ADC B are mapped to DDC0 and DDC1, respectively. However, the DDC MUX allows for one ADC to be mapped to both DDCs or the average of both ADCs to be mapped to each DDC.



図 7-18. Digital Down Converter Overview



7.3.5.1 Decimation Operation

The complex decimation operation is illustrated with an example in \boxtimes 7-19. First, the input signal (and the negative image) are frequency shifted by the NCO frequency as shown on the left side of the figure. Next, a digital filter is applied (centered around 0Hz) and the output data rate is decimated by 8 complex, In this example, the output data rate is complex of $F_{OUT} = F_S/8$ complex with a spectrum from $-F_S/16$ to $F_S/16$. During the complex mixing operation, the spectrum (signal and noise) is split into real and complex parts, and the amplitude is reduced by 6dB. To compensate for the amplitude reduction, there is a 6dB digital gain option in the decimation filter block that can be enabled via SPI.





The real decimation operation is shown in \boxtimes 7-20. There is no mixing in this mode, only the real portion of the complex digital filter is exercised, and the output data rate is reduced. A real decimation by 8 results in an output data rate of $F_{OUT} = F_S/8$ with a spectrum from 0 to $F_S/16$.



図 7-20. Real Decimation Examples



(1)

7.3.5.2 Numerically Controlled Oscillator (NCO)

The DDC blocks are equipped with a 32-bit NCOs for mixing in the complex decimation mode prior to the digital filtering. The NCOs provide a complex output of:

where the frequency ω is specified as a 32-bit signed number also known as the frequency control word (FCW).

The complex output is multiplied with the real input from the ADC to mix the desired carrier to a frequency equal to $F_{IN} \pm F_{NCO}$. The NCO frequency can be tuned from $-F_S/2$ to $F_S/2$ and is processed as a signed, 2s complement number. After programming a new NCO frequency, either the NCO_RES (D5 & D1 of 0x26) or the SYNC pin have to be toggled for the new frequency to take effect.

The NCO FCW is calculated as follows:

FCW =
$$F_{NCO} \times 2^{32} / F_S$$
 for an f_{NCO} in range of 0 to + $F_S/2$ (2)

FCW =
$$(F_{NCO} + F_S) \times 2^{32} / F_S$$
 for an F_{NCO} in range of $-F_S/2$ to 0 (3)

7.3.5.3 Decimation Filters

7-5 provides an overview of the passband bandwidths and output data rates of the different decimation settings with respect to the ADC sampling rate F_S.

REAL/COMPLEX DECIMATION	DECIMATION SETTING N	OUTPUT RATE	OUTPUT BANDWIDTH	OUTPUT RATE (F _S = 65 MSPS)	OUTPUT BANDWIDTH (F _S = 65 MSPS)			
	2	F _S / 2 complex	0.8 × F _S / 2	32.5 MSPS complex	26 MHz			
	4	F _S / 4 complex	0.8 × F _S / 4	16.25 MSPS complex	13 MHz			
Complex	8	F _S / 8 complex	0.8 × F _S / 8	8.125 MSPS complex	6.5 MHz			
	16	F _S / 16 complex	0.8 × F _S / 16	4.0625 MSPS complex	3.25 MHz			
	32	F _S / 32 complex	0.8 × F _S / 32	2.03125 MSPS complex	1.625 MHz			
	2	F _S / 2	0.4 × F _S / 2	32.5 MSPS	13 MHz			
	4	F _S / 4	0.4 × F _S / 4	16.25 MSPS	6.5 MHz			
Real	8	F _S / 8	0.4 × F _S / 8	8.125 MSPS	3.25 MHz			
	16	F _S / 16	0.4 × F _S / 16	4.0625 MSPS	1.625 MHz			
	32	F _S / 32	0.4 × F _S / 32	2.03125 MSPS	0.8125 MHz			

表 7-5. Decimation Filter Summary and Maximum Available Output Bandwidth

The decimation filter responses are normalized to the ADC sampling clock frequency F_S and illustrated in \boxtimes 7-21 to \boxtimes 7-30. Each figure contains the filter passband, transition band(s) and stopband(s).









7.3.5.4 SYNC

The PDN/SYNC pin can be used to synchronize multiple devices using an external SYNC signal. The PDN/ SYNC pin can be configured via SPI to function as the synchronization input. Once configured for SYNC, the SYNC signal is latched by the rising edge of the sampling clock as shown in \boxtimes 7-31.



☑ 7-31. External SYNC Timing Diagram

The synchronization signal is only required when using the DDCs. When using the SPI based SYNC or the PDN/ SYNC pin, the internal clock divider is reset. If no SYNC signal is given, the internal clock dividers may not be synchronized across devices. The SYNC signal also resets the NCO phase, and loads the new NCO frequency. The SYNC signal should be provided as a single pulse with a pulse width of at least 256 clock cycles.



7.3.5.5 Output Data Format with Decimation

When using decimation, the digital output data is formatted as shown in \boxtimes 7-32 (complex decimation) and \boxtimes 7-33 (real decimation). The figures are representative of 18-bit output resolution.



図 7-32. Output Data Format in Complex Decimation (18-bit Output Resolution)





図 7-33. Output Data Format in Real Decimation (18-bit Output Resolution)



7.4 Device Functional Modes

7.4.1 Low Latency Mode

The ADC3683-SP low latency mode can be configured by disabling the digital signal processing (DSP) features. The DSP features can be disabled via SPI (D2 of 0x24) to make sure the ADC latency is 2 clock cycles in 2-wire mode or 1 clock cycle in 1-wire mode.

7.4.2 Averaging Mode

The ADC3683-SP includes a digital channel averaging feature which enables improvement of the ADC SNR (see \boxtimes 7-34). The same input signal is given to both ADC inputs externally and the outputs of the two ADCs are averaged internally. Through averaging, uncorrelated noise (such as ADC thermal noise) adds incoherently which improves SNR by about 3dB.



🛛 7-34. Averaging Diagram



7.5 Programming

The device is primarily configured and controlled using the Serial Peripheral Interface (SPI); however, the device can operate in a default configuration without requiring the SPI. The power down state, internal or external reference selection, and sampling clock input type are configurable via the PDN/SYNC and CTRL pins.

注 The power down functionality requires the ADC sampling clock to be present.

7.5.1 Pin Control

The ADC voltage reference and sampling clock input type can be selected using the CTRL pin. Even though there is an internal $100k\Omega$ pull-up resistor to AVDD, the CTRL pin should be set to a voltage externally and not left floating. When using a voltage divider to set the CTRL pin voltage, resistor values less than $5k\Omega$ should be used.

CTRL PIN VOLTAGE	VOLTAGE REFERENCE OPTION	CLOCKING TYPE					
> 1.7V (Default)	External reference	Differential clock input					
0.5 - 0.7V	Internal reference	Differential clock input					
< 0.1V	Internal reference	Single-ended clock input					

表 7-6. CTRL Pin Settings

7.5.2 Serial Peripheral Interface (SPI)

The device has a set of internal registers that can be accessed via SPI formed by the \overline{SEN} (serial interface enable), SCLK (serial interface clock) and SDIO (serial interface data input/output) pins. Bits are serially shifted into the device when \overline{SEN} is low. Input data is latched at every SCLK rising edge when \overline{SEN} is active (low). The serial data is loaded into the register at the 24th SCLK rising edge when \overline{SEN} is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active \overline{SEN} pulse. The interface can function with SCLK frequencies from 20MHz down to as slow as a few hertz.



7.5.2.1 Register Write

The internal registers can be programmed by following these steps:

- 1. Drive the \overline{SEN} pin low.
- 2. Set the R/W bit to 0 (bit A15 of the 16-bit address) and bits A[14:12] in the address field to 0.
- 3. Initiate a serial interface cycle by specifying the address of the register (A[11:0]) whose content is to be written.
- 4. Write the 8-bit data that to be latched on the SCLK rising edges.
- ☑ 7-35 shows the relevant timing requirements for the register write operation.





7.5.2.2 Register Read

The device includes a mode where the contents of the internal registers can be read back using the SDIO pin. This read back mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

- 1. Drive the $\overline{\text{SEN}}$ pin low.
- 2. Set the R/W bit (A15) to 1. Set A[14:12] in the address field to 0.
- 3. Initiate a serial interface cycle specifying the address of the register (A[11:0]) whose content will be read.
- 4. The device launches the contents (D[7:0]) of the selected register on the SDIO pin on SCLK falling edge.
- 5. The external controller can capture the contents on the SCLK rising edge.



図 7-36. Serial Register Read Timing Diagram

7.5.3 Device Configuration Steps

The following sequence summarizes all the relevant registers for changing the ADC3683-SP modes including the digital signal processing (DSP) features and the output interface. Steps 1 and 2 must come first since the E-Fuse load resets some of the device registers, the remaining steps can come in any order.

STEP	FEATURE	ADDRESS	DESCRIPTION							
			Select the output in	Select the output interface mode based on output resolution.						
		Output R	esolution	2-wire	1-wire	1/2-wire				
			14	-bit	0x2B					
1		0x07	16	-bit	0x4B					
			18	-bit	0x2B	0x6C	0x8D			
			20	-bit	0x4B					
2	•	0x13	Load the output inte ~ 1ms so that the bi	erface bit mapping us it mapping is loaded	ing the E-fuse loade properly, and write 0	r (D0 of 0x13). Write x00 to 0x13.	0x01 to 0x13, wait			
			Configure the FCLK	Configure the FCLK settings based on the desired device modes and interface modes.						
			Mode	Interface Mode	FCLK_SRC	FCLK_DIV	TOG_FCLK			
			DSP Features	2-wire	0	1	0			
2		0v10	Disabled/Real	1-wire	0	0	0			
3		019	Decimation	1/2-wire	0	0	0			
	Output Interface			2-wire	1	0	0			
			Complex Decimation	1-wire	1	0	0			
				1/2-wire	0	0	1			
4		0x1B	Select the output in	elect the output interface resolution.						
		0x20 0x21 0x22	Configure the FCLK pattern based on device modes.							
			Mode	Output Resolution	2-wire	1-wire	1/2-wire			
				14-bit	0xFFC00	0xFE000				
			DSP Features Disabled/Real Decimation	16-bit		0xFF000	0xFFC00			
5				18-bit		0xFF800	0.01000			
				20-bit		0xFFC00				
				14-bit		0xFFFFF				
			Complex	16-bit			0xFFFFF			
			Decimation	18-bit						
				20-bit						
6		0x390x60 0x610x88	Change output bit n	napping from the defa	ault as needed (for e	xample, if enabling t	he scrambler).			
7		0x24 0x22	Optionally, the scrat	mbler can be enabled	d if the device is conf	igured in the 2-wire i	nterface mode.			
8		0x24	Optionally, enable th	he DDCs.						
9		0x25	If using the DDCs, o	configure the DDCs s	ettings.					
10	1	0x2A/B/C/D 0x31/2/3/4	If using complex de	cimation, program the	e desired NCO frequ	ency.				
	Digital Down		Set both bits to 0 i	f not using complex	decimation.					
	converters	0.07	Interface Mode			IQ_ORDER	Q_DEL			
11		0x27 0x2E	2-wire			1	0			
			1-wire			0	1			
			1/2-wire			1	1			
12		0x26	Set the DDC gain a	et the DDC gain and toggle the NCO reset bit to update the NCO frequency.						



7.5.4 Register Map

REGISTER ADDRESS				REGISTI	ER DATA			
A[11:0]	D7	D6	D5	D4	D3	D2	D1	D0
0x00	0	0	0	0	0	0	0	RESET
0x07	IF		E	0	IF_SEL_EN	IF_MODE_SEL		
0x08	0	0	0	0	0	PDN_A	PDN_B	PDN_ GLOBAL
0x09	0	0	0	0	PDN_DA1	PDN_DA0	PDN_DB1	PDN_DB0
0x0E	SYNC_ PIN_EN	SPI_SYNC_ VAL	SYNC_SRC_ SEL	0	CTRL_MODE	REF_	_SEL	SE_CLK_EN
0x11	0	0	0	0	0	DLL_PDN	0	0
0x13	0	0	0	0	0	0	0	FUSE_LD
0x14				PAT_D	ATA[7:0]			
0x15				PAT_DA	TA[15:8]			
0x16		TP1_MODE			TP0_MODE		PAT_DAT	A_[17:16]
0x19	FCLK_SRC	0	0	FCLK_DIV	0	0	0	TOG_FCLK
0x1A	0	HALF_ SWING_EN	0	0	0	0	0	0
0x1B	RES_ SEL_EN	20B_EN		RES_SEL 0				0
0x1E	0 0 0 0 LVDS_DATA_DEL LVDS_DCLK_DEL							
0x20	FCLK_PAT[7:0]							
0x21	FCLK_PAT[15:8]							
0x22	0	SCR_EN	0	0		FCLK_P	AT[19:16]	
0x24	0	0	AVG_EN	DDC_I	IP_SEL	DSP_EN	DDC_EN	0
0x25	DDC_ MUX_EN		DEC_FACTOR		DDC_MODE	0	0	0
0x26	DDC0	_GAIN	NCO0_RES	0	DDC1	_GAIN	NCO1_RES	0
0x27	0	0	0	IQ0_ORDER	Q0_DEL	0	0	0
0x2A				FCW	0[7:0]			
0x2B				FCW0)[15:8]			
0x2C				FCW0	[23:16]			
0x2D				FCW0	[31:24]			
0x2E	0	0	0	IQ1_ORDER	Q1_DEL	0	0	0
0x31				FCW	1[7:0]			
0x32				FCW1	[15:8]			
0x33				FCW1	[23:16]			
0x34				FCW1	[31:24]			
0x390x60				BIT_MA	PPER_A			
0x610x88				BIT_MA	PPER_B			
0x8F	0	0	0	0	0	0	FORMAT_A	0
0x92	0	0	0	0	0	0	FORMAT_B	0
0x244	0	0	DCLKIN_ VCM	0	0	0	0	0



7.5.4.1 Detailed Register Description

図 7-37. Register 0x00

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	RESET
R/W-0							

表 7-9. Register 0x00 Field Descriptions

Bit	Field	Туре	Reset	Description
7-1	0	R/W	0	Must write 0.
0	RESET	R/W	0	This bit resets all internal registers to the default values and self clears to 0.

🖾 7-38. Register 0x07

7	6	5	4	3	2	1	0
	IF_MAPPER_SEL	-	0	IF_SEL_EN		IF_MODE_SEL	
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

	X /-	iv. Regis		
Bit	Field	Туре	Reset	Description
7-5	IF_MAPPER_SEL	R/W	000	Select the proper bit mapping based on the desired interface mode. The bit mapping for each mode is described under セクシ ョン 7.3.4.5. The default bit mapping for each interface mode is loaded from internal fuses and also requires a fuse load sequence (see 表 7-15). It is imperative that this field is set before the fuse load sequence. 001: bit mapping for 2-wire, 18-bit and 14-bit. 010: bit mapping for 2-wire, 16-bit. 011: bit mapping for 1-wire. 100: bit mapping for 1/2-wire.
4	0	R/W	0	Must write 0.
3	IF_SEL_EN	R/W	0	Enables selection of the output interface mode. 0: interface mode selection is disabled. 1: interface mode selection is enabled.
2-0	IF_MODE_SEL	R/W	000	Select the desired output interface mode (2-wire, 1-wire, or 1/2- wire). IF_SEL_EN must be set to 1 for this setting to take effect. 011: interface mode set to 2-wire. 100: interface mode set to 1-wire. 101: interface mode set to 1/2-wire.

表 7-10. Register 0x07 Field Descriptions



	図 7-39. Register 0x08									
7	6	5	4	3	2	1	0			
0	0	0	0	0	PDN_A	PDN_B	PDN_ GLOBAL			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			

表 7-11. Register 0x08 Field Descriptions

Bit	Field	Туре	Reset	Description	
7-3	0	R/W	0	Must write 0.	
2	PDN_A	R/W	0	Power down ADC A.	
				0: ADC A is enabled. 1: ADC A is powered down.	
1	PDN_B	R/W	0	Power down ADC B.	
				0: ADC B is enabled.	
				1: ADC B is powered down.	
0	PDN_GLOBAL	R/W	0	Device global power down.	
				0: device is enabled.	
				1: device is powered down.	

図 7-40. Register 0x09

7	6	5	4	3	2	1	0
0	0	0	0	PDN_DA1	PDN_DA0	PDN_DB1	PDN_DB0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-12. Register 0x09 Field Descriptions

Bit	Field	Туре	Reset	Description	
7-4	0	R/W	0	Must write 0.	
3	PDN_DA1	R/W	0	Lane A1 power down control. This lane is not powered down automatically in the 1-wire and 1/2-wire interface modes.	
				0: lane A1 is enabled. 1: lane A1 is powered down.	
2	PDN_DA0	R/W	0	Lane A0 power down control.	
				0: lane A0 is enabled. 1: lane A0 is powered down.	
1	PDN_DB1	R/W	0	Lane B1 power down control. This lane is not powered down automatically in the 1-wire and 1/2-wire interface modes.	
				0: lane B1 is enabled. 1: lane B1 is powered down.	
0	PDN_DB0	R/W	0	Lane B0 power down control. This lane is not powered down automatically in the 1/2-wire interface mode.	
				0: lane B0 is enabled. 1: lane B0 is powered down.	



	図 7-41. Register 0x0E										
7	6	5	4	3	2	1	0				
SYNC_ PIN_EN	SPI_SYNC_ VAL	SYNC_SRC_ SEL	0	CTRL_MODE	REF_SEL		SE_CLK_EN				
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0				

表 7-13. Register 0x0E Field Descriptions

Bit	Field	Туре	Reset	Description
7	SYNC_PIN_EN	R/W	0	The PDN/SYNC pin is a dual purpose pin.
				0: the PDN/SYNC pin is configured as the global power down control pin.1: the PDN/SYNC pin is configured as a SYNC pin.
6	SPI_SYNC_VAL	R/W	0	Set the internal SYNC state when SYNC_SRC_SEL is set. SPI_SYNC_VAL should be toggled to issue a SYNC sequence. Doesn't automatically reset to 0.
				0: internal SYNC state is set to 0 (normal operation).1: internal SYNC state set to 1 (initiate SYNC sequence).
5	SYNC_SRC_SEL	R/W	0	Select the SYNC source for the device.
				0: SYNC internal state from the PDN/SYNC pin. 1: SYNC internal state from the SPI_SYNC_VAL field.
4	0	R/W	0	Must write 0.
3	CTRL_MODE	R/W	0	Select if the ADC reference mode and sample clock type is set through the CTRL pin or based on the REF_SEL and SE_CLK_EN fields.
				0: the CTRL pin controls the ADC reference mode and sample clock input type.1: the REF_SEL and SE_CLK_EN fields control the ADC reference mode and sampling clock type, respectively.
2-1	REF_SEL	R/W	00	Select the ADC reference mode via SPI. CTRL_MODE must be set to 1 for this setting to take effect.
				00: internal 1.6V reference used as the ADC reference. 10: the ADC reference is provided externally.
0	SE_CLK_EN	R/W	0	Select the ADC sampling clock input type. CTRL_MODE must be set to 1 for this setting to take effect.
				0: the ADC sampling clock input configured as a differential input. 1: the ADC sampling clock input configured as a single-ended input.



図 7-42. Register 0x11

7	6	5	4	3	2	1	0
0	0	0	0	0	DLL_PDN	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-14. Register 0x11 Field Descriptions

Bit	Field	Туре	Reset	Description
7-3	0	R/W	0	Must write 0.
2	DLL_PDN	R/W	0	Select power down state for an internal DLL. See セクション 7.3.2.2.
1-0	0	R/W	0	Must write 0.

1 7-43. Register 0x13

7	6	5	4	3	2	1	0
0	0	0	0	0	0		FUSE_LD
R/W-0							

表 7-15. Register 0x13 Field Descriptions

Bit	Field	Туре	Reset	Description
7-1	0	R/W	0	Must write 0.
0	FUSE_LD	R/W	0	Internal fuse load control. Set to 1, wait for ~1ms, and set to 0 to load the device configuration based on the interface mode settings.

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	図 7-44. Register 0x14/15/16										
7	6	5	4 3 2 1 0								
	PAT_DATA[7:0]										
			PAT_DA	TA[15:8]							
TP1_MODE TP0_MODE PAT_DATA[17:16]											
R/W-0	R/W-0	R/W-0	R/W-0 R/W-0 R/W-0 R/W-0								

表 7-16. Register 0x14/15/16 Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	TP1_MODE	R/W	000	Located in 0x16. Select the mode for test pattern 1 (default data path for ADC B).
				000: test pattern is disabled (normal output mode). 010: ramp pattern mode where PAT_DATA sets the ramp pattern increment size. 011: constant pattern mode where PAT_DATA[17:0] is the MSB aligned constant pattern.
4-2	TP0_MODE	R/W	000	Located in 0x16. Select the mode for test pattern 0 (default data path for ADC A).
				000: test pattern is disabled (normal output mode). 010: ramp pattern mode where PAT_DATA sets the ramp pattern increment size. 011: constant pattern mode where PAT_DATA[17:0] is the MSB aligned constant pattern.
1-0, 7-0, 7-0	PAT_DATA[17:0]	R/W	0	PAT_DATA[17:0] is split across three registers: [17:16] in 0x16, [15:8] in 0x15, and [7:0] in 0x14. The PAT_DATA:
				 Used as the constant pattern when the test pattern mode is set to constant pattern. Used as the ramp pattern step size when test pattern mode is set to ramp pattern



図 7-45. Register 0x19

7	6	5	4	3	2	1	0
FCLK_SRC	0	0	FCLK_DIV	0	0	0	TOG_FCLK
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-17. Register 0x19 Field Descriptions

Bit	Field	Туре	Reset	Description
7	FCLK_SRC	R/W	0	Select the FCLK signal source. See 表 7-18.
6-5	0	R/W	0	Must write 0.
4	FCLK_DIV	R/W	0	Select the FCLK divider setting. See 表 7-18.
3-1	0	R/W	0	Must write 0.
0	TOG_FCLK	R/W	0	Select the FCLK toggle setting. See 表 7-18.

表 7-18. FCLK Settings Based on Device Mode

Mode	Interface Mode	FCLK_SRC	FCLK_DIV	TOG_FCLK
	2-wire	0	1	0
DSP Features Disabled/Real Decimation	1-wire	0	0	0
	1/2-wire	0	0	0
	2-wire	1	0	0
Complex Decimation	1-wire	1	0	0
	1/2-wire	0	0	1



図 7-46. Register 0x1A

7	6	5	4	3	2	1	0
0	HALF_ SWING_EN	0	0	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-19. Register 0x1A Field Descriptions

Bit	Field	Туре	Reset	Description
7	0	R/W	0	Must write 0.
6	HALF_SWING_EN	R/W	0	This bit reduces the LVDS output swing.
5-0	0	R/W	0	Must write 0.

図 7-47. Register 0x1B

7	6	5	4	3	2	1	0
RES_SEL_EN	20B_EN		RES_SEL		0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-20. Register 0x1B Field Descriptions

Bit	Field	Туре	Reset	Description
7	RES_SEL_EN	R/W	0	Select if the resolution select block is enabled. The resolution select block is not needed for setting the output resolution to 20-bit.
				0: the resolution select block is disabled.1: the resolution select block is enabled.
6	20B_EN	R/W	0	Control 20-bit output resolution mode.
				0: 20-bit output resolution mode is disabled. 1: 20-bit output resolution mode is enabled.
5-3	RES_SEL	R/W	000	Select the output resolution. If the DSP features are disabled, RES_SEL_EN needs to be set to 1 for this setting to take effect.
				000: the output resolution is set to 18-bit. 001: the output resolution is set to 16-bit. 010: the output resolution is set to 14-bit.
2-0	0	R/W	0	Must write 0.

表 7-21. Setting Output Resolution Based on Mode

Mode	RES_SEL_EN	RES_SEL
DSP Features Disabled	1	000: the output resolution is set to 18-bit.
Real Decimation	0	001: the output resolution is set to 16-bit.
Complex Decimation	0	010: the output resolution is set to 14-bit.



図 7-48. Register 0x1E 2 0 7 6 5 4 3 1 0 0 0 0 LVDS DATA DEL LVDS DCLK DEL R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0

表 7-22. Register 0x1E Field Descriptions

Bit	Field	Туре	Reset	Description
7-4	0	R/W	0	Must write 0
3-2	LVDS_DATA_DEL	R/W	00	Control delay on the data lanes. 00: no delay (normal mode). 01: the data lanes are advanced by 50ps. 10: the data lanes are delayed by 50ps. 11: the data lanes are delayed by a 100ps.
1-0	LVDS_DCLK_DEL	R/W	00	Control delay on the interface data clock. 00: no delay (normal mode). 01: DCLK is advanced by 50ps. 10: DCLK is delayed by 50ps. 11: DCLK is delayed by a 100ps.

図 7-49. Register 0x20/21/22

7	6	5	4	3	2	1	0		
FCLK_PAT[7:0]									
FCLK_PAT_[15:8]									
0	0 SCR_EN 0 0 FCLK_PAT_[19:16]								
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0 R/W-0 R/W-0 R/W-					

表 7-23. Register 0x20/21/22 Field Descriptions

Bit	Field	Туре	Reset	Description
6	SCR_EN	R/W	0	Located in 0x22. Configure the scrambler enable state. Scrambler should only be used in the 2-wire interface mode. DSP_EN needs to be set to 1 for this setting to take effect. 0: the output scrambler is disabled. 1: the output scrambler is enabled.
3-0, 7-0, 7-0	FCLK_PAT[19:0]	R/W	0xFFC00	FCLK_PAT is split across three registers. [19:16] in 0x22, [15:8] in 0x21, and [7:0] in 0x20. See 表 7-24.

表 7-24. FCLK Pattern in Different Modes

Mode	Output Resolution	2-wire	1-wire	1/2-wire	
DSP Features	14-bit		0xFE000		
	16-bit		0xFF000		
Decimation	18-bit		0xFF800		
	20-bit		0xFFC00		
Complex Decimation	14-bit	UXFFC00			
	16-bit		0xFFFFF	0xFFFFF	
	18-bit				
	20-bit				

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図 7-50. Register 0x24										
7	6	5	4	3	2	1	0			
0	0	AVG_EN	DDC_INP_SEL		DSP_EN	DDC_EN	0			
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0			

表 7-25. Register 0x24 Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	0	R/W	0	Must write 0.
5	AVG_EN	R/W	0	Control the averaging block which averages the outputs of ADCs A & B. 0: the averaging block is disabled.
				1: the averaging block is enabled.
4-3	DDC_INP_SEL	R/W	0	Select the source of the DDC input. DDC_MUX_EN must be set to 1 for this setting to take effect.
				 00: output of ADC A as DDC0 input. Output of ADC B as DDC1 input. 01: output of ADC A as DDC0 and DDC1 input. 10: output of ADC B as DDC0 and DDC1 input. 11: output of ADC averaging block as DDC0 and DDC1 input.
2	DSP_EN	R/W	0	Enable the DSP features data path. 0: DSP features data path is disabled. 1: DSP features data path is enabled.
1	DDC_EN	R/W	0	Enable the DDCs. 0: DDCs are disabled. 1: DDCs are enabled.
0	0	R/W	0	Must write 0.



図 7-51. Register 0x25 5 2 7 6 4 3 1 0 DDC_MUX_EN DEC FACTOR DDC MODE 0 0 0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0

表 7-26. Register 0x25 Field Descriptions

Bit	Field	Туре	Reset	Description
7	DDC_MUX_EN	R/W	0	Control the DDC_MUX enable. The DDC_MUX must be enabled for DDC_INP_SEL to take effect.
				0: the DDC_MUX is disabled. 1: the DDC_MUX enabled,
6-4	DEC_FACTOR	R/W	000	Decimation factor setting.
				000: no decimation. 001: decimation by 2. 010: decimation by 4. 011: decimation by 8. 100: decimation by 16. 101: decimation by 32.
3	DDC_MODE	R/W	0	DDC mode and applies to both DDCs. 0: the DDC mode is set to complex decimation. 1: the DDC mode is set to real decimation.
2-1	0	R/W	0	Must write 0.

図 7-52. Register 0x26

7	6	5	4	3	2	1	0
DDC0	_GAIN	NCO0_RES	0	DDC1	_GAIN	NCO1_RES	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-2	7. Register	0x26 Field	Descriptions
-------	-------------	------------	--------------

Bit	Field	Туре	Reset	Description
7-6	DDC0_GAIN	R/W	00	Select the digital gain setting for DDC0 to compensate for the complex decimation amplitude reduction for DDC0.
				00: no digital gain added. 10: 6-dB digital gain is added (should be enabled in the complex decimation mode only).
5	NCO0_RES	R/W	0	Toggling this bit resets the NCO phase of NCO0 in DDC0 and loads the current FCW0 as the NCO frequency. This setting is not self clearing.
4	0	R/W	0	Must write 0.
3-2	DDC0_GAIN	R/W	00	Select the digital gain setting for DDC1 to compensate for the complex decimation amplitude reduction for DDC1.
				00: no digital gain added. 10: 6-dB digital gain is added (should be enabled in the complex decimation mode only).
1	NCO1_RES	R/W	0	Toggling this bit resets the NCO phase of NCO1 in DDC1 and loads the current FCW1 as the NCO frequency. This setting is not self clearing.
0	0	R/W	0	Must write 0.



図 7-53. Register 0x27

7	6	5	4	3	2	1	0
0	0	0	IQ0_ORDER	Q0_DEL	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-28. Register 0x27 Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	0	R/W	0	Must write 0.
4	IQ0_ORDER	R/W	0	Swaps the I and Q output order for DDC0. Set to 0 if not using complex decimation; otherwise, see $ arrow$ 7-29.
3	Q0_DEL	R/W	0	This delays the quadrature output of DDC0 by one sample. Set to 0 if not using complex decimation; otherwise, see $\frac{1}{5}$ 7-29.
2-0	0	R/W	0	Must write 0

表 7-29. IQ_ORDER and Q_DEL Register Settings for Complex Decimation

Interface Mode	IQ_ORDER	Q_DEL
2-wire	1	0
1-wire	0	1
1/2-wire	1	1

図 7-54. Register 0x2A/B/C/D

7	6	5	4	3	2	1	0				
FCW0[7:0]											
FCW0[15:8]											
	FCW0[23:16]										
FCW0[31:24]											
R/W-0	R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0										

表 7-30. Register 0x2A/2B/2C/2D Field Descriptions

Bit	Field	Туре	Reset	Description		
	FCW0[31:0]	R/W	0	FCW for NCO0 and is split across four registers. [31:24] in 0x2D, [23:16] in 0x2C, [15:8] in 0x2B, and [7:0] in 0x2A.		



図 7-55. Register 0x2E 7 6 5 4 3 2 1 0 0 0 0 IQ1 ORDER Q1 DEL 0 0 0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0

表 7-31. Register 0x2E Field Descriptions

Bit	Field	Туре	Reset	Description
7-5	0	R/W	0	Must write 0
4	IQ1_ORDER	R/W	0	Swaps the I and Q output order for DDC1. Set to 0 if not using complex decimation; otherwise, see $\frac{1}{7}$ 7-29.
3	Q1_DEL	R/W	0	This delays the quadrature output of DDC1 by one sample. Set to 0 if not using complex decimation; otherwise, see $\frac{1}{2}$ 7-29.
2-0	0	R/W	0	Must write 0.

図 7-56. Register 0x31/32/33/34

7	6	5	4	3	2	1	0				
FCW1[7:0]											
FCW1[15:8]											
	FCW1[23:16]										
FCW1[31:24]											
R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0											

表 7-32. Register 0x31/32/33/34 Field Descriptions

Bit	Field	Туре	Reset	Description
	FCW1[31:0]	R/W	0	FCW for NCO1 and is split across four registers. [31:24] in 0x34,
				[23:16] in 0x33, [15:8] in 0x32, and [7:0] in 0x31.

図 7-57. Register 0x39..0x60

7	6	5	4	3	2	1	0					
	BIT_MAPPER_A											
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0					

表 7-33. Register 0x39..0x60 Field Descriptions

Bit	Field	Туре	Reset	Description
	BIT_MAPPER_A	R/W	0	See the セクション 7.3.4.5.

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	図 7-58. Register 0x610x88												
7 6 5 4 3 2 1 0													
	BIT_MAPPER_B												
R/W-0	R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0 R/W-0												

表 7-34. Register 0x61..0x88 Field Descriptions

Bit	Field	Туре	Reset	Description
7-0	BIT_MAPPER_B	R/W	0	See the セクション 7.3.4.5.

🛛 7-59. Register 0x8F

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FORMAT_A	0
R/W-0	R/W-0						

表 7-35. Register 0x8F Field Descriptions

Bit	Field	Туре	Reset	Description
7-2	0	R/W	0	Must write 0
1	FORMAT_A	R/W	0	Sets the output data format for the channel A data path. The DSP_EN must be set to 1 for this setting to take effect. 0: output data format is 2s complement. 1: output data format is offset binary.
0	0	R/W	0	Must write 0

図 7-60. Register 0x92

7	6	5	4	3	2	1	0
0	0	0	0	0	0	FORMAT_B	0
R/W-0	R/W-0						

表 7-36. Register 0x92 Field Descriptions

Bit	Field	Туре	Reset	Description
7-2	0	R/W	0	Must write 0
1	FORMAT_B	R/W	0	Sets the output data format for the channel B data path. The DSP_EN must be set to 1 for this setting to take effect. 0: output data format is 2s complement. 1: output data format is offset binary.
0	0	R/W	0	Must write 0

表 7-37. Register 0x244

7	6	5	4	3	2	1	0
0	0	DCLKIN_VCM	0	0	0	0	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0

表 7-38. Register 0x244 Field Descriptions

Bit	Field	Туре	Reset	Description
7-6	0	R/W	0	Must write 0.
5	DCLKIN_VCM	R/W	0	This bit sets the common-mode source for DCLKIN.
				0: DCLKIN common-mode is provided externally. 1: DCLKIN is internally biased to a 1.2V common-mode.
4-0	0	R/W	0	Must write 0.



8 Application Information Disclaimer

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The ADC3683-SP can be used in a variety of space applications as a high speed and low latency digitizer. Some of the common applications for the ADC3683-SP are found in optical imaging payloads.

8.2 Typical Application





8.2.1 Design Requirements

表 8-1. Design Requirement	s	
---------------------------	---	--

Requirement	Description
Signal Bandwidth	DC to 20MHz
Input Driver	Single ended to differential signal conversion and DC coupling
Clock Source	Low jitter differential clock

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8.2.2 Detailed Design Procedure

The application requirements are provided in $\forall 2 \neq 2 \neq 8.2.1$. Since the supported signal bandwidth is as low as DC, an amplifier is used to DC couple the signal to the input of the ADC. Additionally, the ADC VCM output provides the amplifier common-mode as shown in \boxtimes 8-1.

When designing the amplifier or filter driving circuit, the ADC input full-scale voltage needs to be taken into consideration. For example, the ADC3683-SP input full-scale is $3.2V_{PP}$. Texas Instruments (TI) offers a variety of amplifiers to be used in space applications such as LMH5485-SP and THS4511-SP. For best DC accuracy an external reference can be used.

8.3 Initialization Set Up

The following steps should be followed for device initialization.

- 1. Apply AVDD and IOVDD (no specific sequence required). After AVDD is applied, the internal reference powers up and settles in approximately 2ms.
- 2. Configure the CTRL pin and apply the sampling clock.
- 3. Apply a hardware reset. After the hardware reset is released, the default registers are loaded from internal fuses and the internal power up calibration is initiated. The calibration takes approximately 200000 clock cycles.
- 4. Begin programming via the SPI.

表 8-2. Power Up Timing

		Minimum Time	Unit
t ₁	Delay from power up to logic level of CTRL pin	2	ms
t ₂	RESET pulse width	1	μs
t ₃	Delay from RESET disable to SEN active	~ 200000	Clock Cycles



8.4 Power Supply Recommendations

The ADC3683-SP requires two different power supplies. The A_{VDD} supply provides power for the internal analog circuits and to the ADC while the I_{OVDD} supply powers the digital interface and the internal digital circuits. Power sequencing is not required.

A low noise power supply should supply the AVDD rail to achieve data sheet performance.

There are two recommended power-supply architectures:

- 1. A high efficiency switching regulator followed by a low noise LDO to suppress the switching noise and improve voltage accuracy.
- 2. Directly step down to the final ADC supply voltage using a high efficiency switching regulator. This approach provides the best efficiency; however, care must be taken to make sure the switching regulator noise doesn't degrade the ADC performance.

The TPS7H4002-SP is recommended as the first stage radiation hardened switching regulator. The switching regulator can be followed by either the TPS7A4501-SP or the TPS7H1111-SP which are both space hardened LDOs.

注A_{VDD} and I_{OVDD} supply voltages should not be shared to prevent digital switching noise from coupling into the analog signal chain.



図 8-3. Example Switcher Only Approach

資料に関するフィードバック(ご意見やお問い合わせ)を送信 61



8.5 Layout

8.5.1 Layout Guidelines

There are several critical signals which require specific care during board design:

- 1. Analog inputs and clock signals:
 - Traces should be as short as possible and vias should be avoided where possible to minimize impedance discontinuities.
 - Traces should be routed using loosely coupled 100Ω differential traces.
 - Differential trace lengths should be matched as close as possible to minimize phase imbalance and HD2 degradation.
- 2. Digital output interface:
 - Traces should be routed using tightly coupled 100Ω differential traces.
 - Ensure the LVDS lanes are routed as far as possible from the analog inputs to minimize coupling.
- 3. Voltage reference:
 - The decoupling capacitors should be placed as close to the device pins as possible and connected between VREF and REFGND – avoid using vias by having the capacitors on the same layer as the device.
- 4. Power and ground connections:
 - Provide low resistance connection paths to all power and ground pins.
 - Avoid narrow and isolated paths which increase the connection resistance.
 - Add GND layers between power and signal layers in the PCB stack up.



8.5.2 Layout Example

The following is an example showing the top layer layout of the ADC3683-SP on the ADC3683-SP EVM.

- Signal and clock inputs are routed as differential signals on the top layer.
- LVDS lanes go through vias to the bottom layer to minimize coupling on the analog inputs.



図 8-4. Layout Example for the ADC3683-SP EVM



9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jpのデバイス製品フォルダを開いてください。[通知]をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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9.5 用語集

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10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

C	hanges from Revision * (March 2024) to Revision A (December 2024)	Page
•	製品情報の表の 5962F2320401VXC から製品プレビューの注を削除	1
•	Changed the Detailed Design Procedure	60
•	Deleted the Application Curves	<mark>60</mark>

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



11.1 Mechanical Data





NOTES:

All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
 This drawing is subject to change without notice.
 This package is hermetically sealed with a metal lid.
 Ground pad to be electronic connected to heat sink and seal ring.

- 5. The leads are gold plated and can be solder dipped.





PACKAGING INFORMATION

Orderable part number	Status	Material type	Package Pins	Package qty Carrier	RoHS	Lead finish/	MSL rating/	Op temp (°C)	Part marking
	(1)	(2)			(3)	Ball material	Peak reflow		(6)
						(4)	(5)		
5962F2320401VXC	Active	Production	CFP (HBP) 64	24 TUBE	Yes	NIAU	N/A for Pkg Type	-55 to 105	F2320401VXC ADC3683-SP
5962F2320401VXC.A	Active	Production	CFP (HBP) 64	24 TUBE	Yes	NIAU	N/A for Pkg Type	-55 to 105	F2320401VXC ADC3683-SP
ADC3683HBP/EM	Active	Production	CFP (HBP) 64	24 TUBE	Yes	Call TI	Call TI	25 to 25	ADC3683HBP/EM EVAL ONLY
ADC3683HBP/EM.A	Active	Production	CFP (HBP) 64	24 TUBE	Yes	Call TI	Call TI	25 to 25	ADC3683HBP/EM EVAL ONLY

⁽¹⁾ **Status:** For more details on status, see our product life cycle.

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

⁽⁴⁾ Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ADC3683-SP :

Catalog : ADC3683

NOTE: Qualified Version Definitions:

Catalog - TI's standard catalog product

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