

ADC324x Dual-Channel, 14-Bit, 25-MSPS to 125-MSPS, Analog-to-Digital Converters

1 Features

- Dual Channel
- 14-Bit Resolution
- Single Supply: 1.8 V
- Serial LVDS Interface (SLVDS)
- Flexible Input Clock Buffer with Divide-by-1, -2, -4
- SNR = 72.4 dBFS, SFDR = 87 dBc at $f_{IN} = 70$ MHz
- Ultra-Low Power Consumption:
 - 116 mW/Ch at 125 MSPS
- Channel Isolation: 105 dB
- Internal Dither and Chopper
- Support for Multi-Chip Synchronization
- Pin-to-Pin Compatible with 12-Bit Version
- Package: VQFN-48 (7 mm × 7 mm)

2 Applications

- Multi-Carrier, Multi-Mode Cellular Base Stations
- Radar and Smart Antenna Arrays
- Munitions Guidance
- Motor Control Feedback
- Network and Vector Analyzers
- Communications Test Equipment
- Nondestructive Testing
- Microwave Receivers
- Software-Defined Radios (SDRs)
- Quadrature and Diversity Radio Receivers
- Handheld Radio and Instrumentation

3 Description

The ADC324x are a high-linearity, ultra-low power, dual-channel, 14-bit, 25-MSPS to 125-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider allows more flexibility for system clock architecture design and the SYSREF input enables complete system synchronization. The ADC324x family supports serial low-voltage differential signaling (LVDS) in order to reduce the number of interface lines, thus allowing for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 14-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-----------|-------------------|
| ADC324x | VQFN (48) | 7.00 mm × 7.00 mm |

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Performance at $f_S = 125$ MSPS, $f_{IN} = 10$ MHz

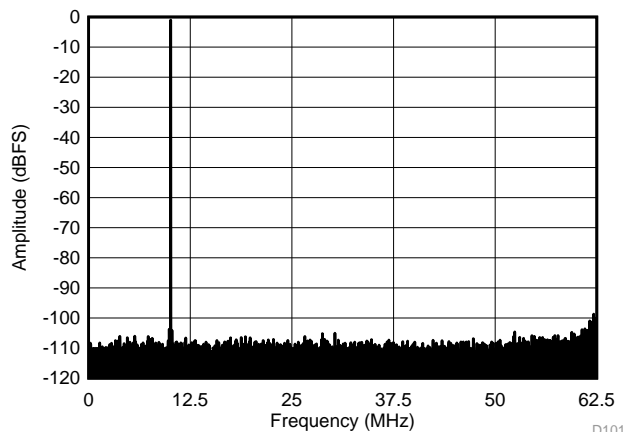


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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision B (March 2015) to Revision C | Page |
|---|-----------|
| • Added <i>Digital Inputs</i> section to <i>Digital Characteristics</i> table | 17 |
| • Changed <i>Wake-up time</i> parameter maximum specifications in <i>Timing Requirements: General</i> table | 17 |
| • Updated Figure 19 , Figure 20 , Figure 23 , Figure 24 , Figure 25 , and Figure 26 | 22 |
| • Updated Figure 50 , Figure 51 , Figure 54 , Figure 55 , Figure 56 , and Figure 57 | 28 |
| • Updated Figure 81 , Figure 82 , Figure 85 , Figure 86 , Figure 87 , and Figure 88 | 34 |
| • Updated Figure 112 , Figure 113 , Figure 116 , Figure 117 , Figure 118 , and Figure 119 | 40 |
| • Changed Figure 133 | 45 |
| • Changed <i>SNR and Clock Jitter</i> section: changed typical thermal noise value and changed Figure 141 to reflect updated thermal noise value | 49 |
| • Changed Table 3 | 50 |
| • Changed Figure 142 | 51 |
| • Added <i>Improving Wake-Up Time From Global Power-Down</i> section | 53 |
| • Changed Table 8 : changed <i>FLIP BITS</i> to <i>FLIP WIRE</i> in register 4h, changed bit D7 in row 70A, and added register 13 row | 57 |
| • Changed <i>Summary of Special Mode Registers</i> section: changed title, moved section to correct location | 58 |
| • Changed register 04h description | 59 |
| • Changed register 0Ah and 0Bh descriptions | 61 |
| • Added register 13h | 63 |
| • Changed register 70Ah to include DIS CLK FILT bit | 68 |

Revision History (continued)

Changes from Revision A (December 2014) to Revision B **Page**

- Changed document status from Mixed Status to Production Data: releasing ADC3241 and ADC3242 to Production; changes made to product preview devices 1
-

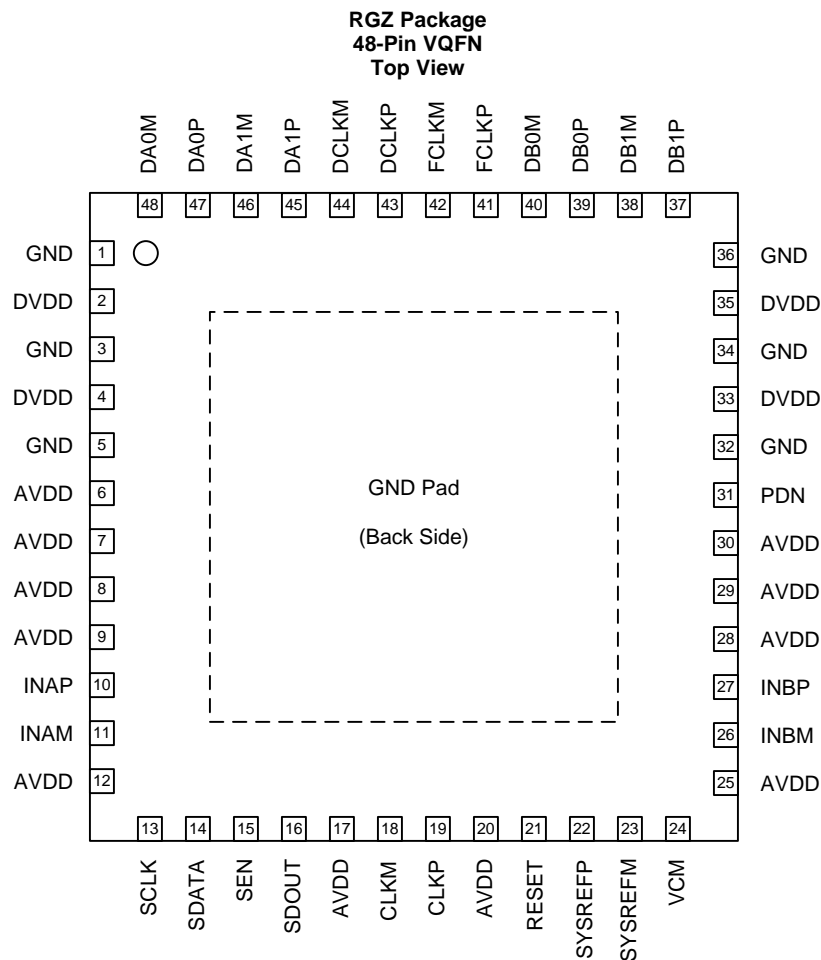
Changes from Original (July 2014) to Revision A **Page**

- Changed document status to Mixed Status 1
 - Made changes to product preview data sheet 1
-

5 Device Comparison Table

| INTERFACE | RESOLUTION (Bits) | 25 MSPS | 50 MSPS | 80 MSPS | 125 MSPS | 160 MSPS |
|-------------|-------------------|-------------------------|--------------------------|--------------------------|--------------------------|--------------------------|
| Serial LVDS | 12 | ADC3221 | ADC3222 | ADC3223 | ADC3224 | — |
| | 14 | ADC3241 | ADC3242 | ADC3243 | ADC3244 | — |
| JESD204B | 12 | — | ADC32J22 | ADC32J23 | ADC32J24 | ADC32J25 |
| | 14 | — | ADC32J42 | ADC32J43 | ADC32J44 | ADC32J45 |

6 Pin Configuration and Functions



Pin Functions

| PIN | | I/O | DESCRIPTION |
|---------|--------------------------------|-----|---|
| NAME | NO. | | |
| AVDD | 6-9, 12, 17, 20, 25, 28-30 | I | Analog 1.8-V power supply |
| CLKM | 18 | I | Negative differential clock input for the ADC |
| CLKP | 19 | I | Positive differential clock input for the ADC |
| DA0M | 48 | O | Negative serial LVDS output for channel A0 |
| DA0P | 47 | O | Positive serial LVDS output for channel A0 |
| DA1M | 46 | O | Negative serial LVDS output for channel A1 |
| DA1P | 45 | O | Positive serial LVDS output for channel A1 |
| DB0M | 40 | O | Negative serial LVDS output for channel B0 |
| DB0P | 39 | O | Positive serial LVDS output for channel B0 |
| DB1M | 38 | O | Negative serial LVDS output for channel B1 |
| DB1P | 37 | O | Positive serial LVDS output for channel B1 |
| DCLKM | 44 | O | Negative bit clock output |
| DCLKP | 43 | O | Positive bit clock output |
| DVDD | 2, 4, 33, 35 | I | Digital 1.8-V power supply |
| FCLKM | 42 | O | Negative frame clock output |
| FCLKP | 41 | O | Positive frame clock output |
| GND | 1, 3, 5, 32, 34, 36, PowerPAD™ | I | Ground, 0 V |
| INAM | 11 | I | Negative differential analog input for channel A |
| INAP | 10 | I | Positive differential analog input for channel A |
| INBM | 26 | I | Negative differential analog input for channel B |
| INBP | 27 | I | Positive differential analog input for channel B |
| PDN | 31 | I | Power-down control. This pin can be configured via the SPI. This pin has an internal 150-kΩ pull-down resistor. |
| RESET | 21 | I | Hardware reset; active high. This pin has an internal 150-kΩ pull-down resistor. |
| SCLK | 13 | I | Serial interface clock input. This pin has an internal 150-kΩ pull-down resistor. |
| SDATA | 14 | I | Serial interface data input. This pin has an internal 150-kΩ pull-down resistor. |
| SDOUT | 16 | O | Serial interface data output |
| SEN | 15 | I | Serial interface enable; active low. This pin has an internal 150-kΩ pull-up resistor to AVDD. |
| SYSREFM | 23 | I | Negative external SYSREF input |
| SYSREFP | 22 | I | Positive external SYSREF input |
| VCM | 24 | O | Common-mode voltage for analog inputs |

7 Specifications

7.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|------------------------------------|------------------------------------|------|-----------------------|------|
| Analog supply voltage range, AVDD | | -0.3 | 2.1 | V |
| Digital supply voltage range, DVDD | | -0.3 | 2.1 | V |
| Voltage applied to input pins | INAP, INBP, INAM, INBM | -0.3 | min (1.9, AVDD + 0.3) | V |
| | CLKP, CLKM | -0.3 | AVDD + 0.3 | |
| | SYSREFP, SYSREFM | -0.3 | AVDD + 0.3 | |
| | SCLK, SEN, SDATA, RESET, PDN | -0.3 | 3.9 | |
| Temperature | Operating free-air, T _A | -40 | 85 | °C |
| | Operating junction, T _J | | 125 | |
| | Storage, T _{stg} | -65 | 150 | |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--------------------|-------------------------|---|------------|
| V _(ESD) | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 V |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|------------------------|---|---------------------------------|-----|--------------------|-----------------|
| SUPPLIES | | | | | |
| AVDD | Analog supply voltage range | 1.7 | 1.8 | 1.9 | V |
| DVDD | Digital supply voltage range | 1.7 | 1.8 | 1.9 | V |
| ANALOG INPUT | | | | | |
| V _{ID} | Differential input voltage | For input frequencies < 450 MHz | | 2 | V _{PP} |
| | | For input frequencies < 600 MHz | | 1 | |
| V _{IC} | Input common-mode voltage | VCM ± 0.025 | | | V |
| CLOCK INPUT | | | | | |
| | Input clock frequency | Sampling clock frequency | 10 | 125 ⁽²⁾ | MSPS |
| | Input clock amplitude (differential) | Sine wave, ac-coupled | 0.2 | 1.5 | V _{PP} |
| | | LVPECL, ac-coupled | | 1.6 | |
| | | LVDS, ac-coupled | | 0.7 | |
| | Input clock duty cycle | | 35% | 50% | 65% |
| | Input clock common-mode voltage | | | 0.95 | V |
| DIGITAL OUTPUTS | | | | | |
| C _{LOAD} | Maximum external load capacitance from each output pin to GND | | | 3.3 | pF |
| R _{LOAD} | Differential load resistance placed externally | | | 100 | Ω |

- (1) After power-up, to reset the device for the first time, only use the RESET pin; see the [Register Initialization](#) section.
 (2) With the clock divider enabled by default for divide-by-1. Maximum sampling clock frequency for the divide-by-4 option is 500 MSPS.

7.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | ADC324x | |
|-------------------------------|--|------------|------|
| | | RGZ (VQFN) | |
| | | 48 PINS | |
| Symbol | Description | Value | UNIT |
| R _{θJA} | Junction-to-ambient thermal resistance | 25.7 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 18.9 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 3.0 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 0.2 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 3 | °C/W |
| R _{θJC(bot)} | Junction-to-case (bottom) thermal resistance | 0.5 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics: ADC3241, ADC3242

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

| PARAMETER | ADC3241 | | | ADC3242 | | | UNIT |
|--------------------------------|---------|-----|-----|---------|-----|-----|------|
| | MIN | TYP | MAX | MIN | TYP | MAX | |
| ADC clock frequency | | | 125 | | | 125 | MSPS |
| 1.8-V analog supply current | | 31 | 71 | | 39 | 81 | mA |
| 1.8-V digital supply current | | 35 | 65 | | 43 | 75 | mA |
| Total power dissipation | | 118 | 205 | | 147 | 245 | mW |
| Global power-down dissipation | | 5 | 17 | | 5 | 17 | mW |
| Standby power-down dissipation | | 78 | 103 | | 78 | 103 | mW |

7.6 Electrical Characteristics: ADC3243, ADC3244

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 85°C, maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

| PARAMETER | ADC3243 | | | ADC3244 | | | UNIT |
|--------------------------------|---------|-----|-----|---------|-----|-----|------|
| | MIN | TYP | MAX | MIN | TYP | MAX | |
| ADC clock frequency | | | 80 | | | 125 | MSPS |
| 1.8-V analog supply current | | 50 | 91 | | 65 | 106 | mA |
| 1.8-V digital supply current | | 52 | 85 | | 64 | 95 | mA |
| Total power dissipation | | 183 | 285 | | 233 | 325 | mW |
| Global power-down dissipation | | 5 | 17 | | 5 | 17 | mW |
| Standby power-down dissipation | | 72 | 103 | | 78 | 103 | mW |

7.7 Electrical Characteristics: General

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, maximum sampling rate, 50% clock duty cycle, $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|-----|-------------|-----|-----------------------------|
| RESOLUTION | | | | | |
| Resolution | | 14 | | | Bits |
| ANALOG INPUT | | | | | |
| Differential input full-scale | | | 2.0 | | V_{PP} |
| R_{IN} Input resistance | Differential at dc | | 6.6 | | $\text{k}\Omega$ |
| C_{IN} Input capacitance | Differential at dc | | 3.7 | | pF |
| $V_{\text{OC(VCM)}}$ VCM common-mode voltage output | | | 0.95 | | V |
| VCM output current capability | | | 10 | | mA |
| Input common-mode current | Per analog input pin | | 1.5 | | $\mu\text{A/MSPS}$ |
| Analog input bandwidth (3 dB) | 50- Ω differential source driving 50- Ω termination across INP and INM | | 540 | | MHz |
| DC ACCURACY | | | | | |
| E_{O} Offset error | | -25 | | 25 | mV |
| α_{EO} Temperature coefficient of offset error | | | ± 0.024 | | $^\circ\text{C}$ |
| $E_{\text{G(REF)}}$ Gain error as a result of internal reference inaccuracy alone | | -2 | | 2 | %FS |
| $E_{\text{G(CHAN)}}$ Gain error of channel alone | | | -2 | | %FS |
| $\alpha_{\text{(EGCHAN)}}$ Temperature coefficient of $E_{\text{G(CHAN)}}$ | | | ± 0.008 | | $\Delta\%FS/^\circ\text{C}$ |
| CHANNEL-TO-CHANNEL ISOLATION | | | | | |
| Crosstalk ⁽¹⁾ | $f_{\text{IN}} = 10\text{ MHz}$ | | 105 | | dB |
| | $f_{\text{IN}} = 100\text{ MHz}$ | | 105 | | |
| | $f_{\text{IN}} = 200\text{ MHz}$ | | 105 | | |
| | $f_{\text{IN}} = 230\text{ MHz}$ | | 105 | | |
| | $f_{\text{IN}} = 300\text{ MHz}$ | | 105 | | |

(1) Crosstalk is measured with a -1-dBFS input signal on one channel and no input on the other channel.

7.8 AC Performance: ADC3241

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | ADC3241 ($f_s = 25 \text{ MSPS}$) | | | | | | UNIT |
|-----------------------------------|--|-----------------------------------|-------------------------------------|--------|-----|------------|-----|-----|---------|
| | | | DITHER ON | | | DITHER OFF | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| DYNAMIC AC CHARACTERISTICS | | | | | | | | | |
| SNR | Signal-to-noise ratio (from 1-MHz offset) | $f_{\text{IN}} = 10 \text{ MHz}$ | 73.3 | | | 73.7 | | | dBFS |
| | | $f_{\text{IN}} = 20 \text{ MHz}$ | 69.7 | 73.4 | | 73.7 | | | |
| | | $f_{\text{IN}} = 70 \text{ MHz}$ | 72.8 | | | 73.2 | | | |
| | | $f_{\text{IN}} = 100 \text{ MHz}$ | 72.4 | | | 72.8 | | | |
| | | $f_{\text{IN}} = 170 \text{ MHz}$ | 71.3 | | | 71.6 | | | |
| | | $f_{\text{IN}} = 230 \text{ MHz}$ | 70.1 | | | 70.4 | | | |
| | Signal-to-noise ratio (full Nyquist band) | $f_{\text{IN}} = 10 \text{ MHz}$ | 72.2 | | | 72.6 | | | dBFS |
| | | $f_{\text{IN}} = 20 \text{ MHz}$ | 72.3 | | | 72.6 | | | |
| | | $f_{\text{IN}} = 70 \text{ MHz}$ | 71.8 | | | 72.2 | | | |
| | | $f_{\text{IN}} = 100 \text{ MHz}$ | 71.5 | | | 71.9 | | | |
| | | $f_{\text{IN}} = 170 \text{ MHz}$ | 70.5 | | | 70.8 | | | |
| | | $f_{\text{IN}} = 230 \text{ MHz}$ | 69.3 | | | 69.6 | | | |
| NSD ⁽¹⁾ | Noise spectral density (averaged across Nyquist zone) | $f_{\text{IN}} = 10 \text{ MHz}$ | –143.9 | | | –144.3 | | | dBFS/Hz |
| | | $f_{\text{IN}} = 20 \text{ MHz}$ | –144.0 | –140.7 | | –144.3 | | | |
| | | $f_{\text{IN}} = 70 \text{ MHz}$ | –143.4 | | | –143.8 | | | |
| | | $f_{\text{IN}} = 100 \text{ MHz}$ | –143.0 | | | –143.4 | | | |
| | | $f_{\text{IN}} = 170 \text{ MHz}$ | –141.9 | | | –142.2 | | | |
| | | $f_{\text{IN}} = 230 \text{ MHz}$ | –140.7 | | | –141.0 | | | |
| SINAD ⁽¹⁾ | Signal-to-noise and distortion ratio | $f_{\text{IN}} = 10 \text{ MHz}$ | 73.3 | | | 73.5 | | | dBFS |
| | | $f_{\text{IN}} = 20 \text{ MHz}$ | 69.1 | 73.1 | | 73.5 | | | |
| | | $f_{\text{IN}} = 70 \text{ MHz}$ | 72.8 | | | 72.9 | | | |
| | | $f_{\text{IN}} = 100 \text{ MHz}$ | 72.2 | | | 72.4 | | | |
| | | $f_{\text{IN}} = 170 \text{ MHz}$ | 71.2 | | | 71.2 | | | |
| | | $f_{\text{IN}} = 230 \text{ MHz}$ | 69.7 | | | 69.7 | | | |
| ENOB ⁽¹⁾ | Effective number of bits | $f_{\text{IN}} = 10 \text{ MHz}$ | 11.9 | | | 11.9 | | | Bits |
| | | $f_{\text{IN}} = 20 \text{ MHz}$ | 11.2 | 11.8 | | 11.9 | | | |
| | | $f_{\text{IN}} = 70 \text{ MHz}$ | 11.8 | | | 11.8 | | | |
| | | $f_{\text{IN}} = 100 \text{ MHz}$ | 11.7 | | | 11.7 | | | |
| | | $f_{\text{IN}} = 170 \text{ MHz}$ | 11.5 | | | 11.5 | | | |
| | | $f_{\text{IN}} = 230 \text{ MHz}$ | 11.3 | | | 11.3 | | | |
| SFDR | Spurious-free dynamic range | $f_{\text{IN}} = 10 \text{ MHz}$ | 95 | | | 87 | | | dBc |
| | | $f_{\text{IN}} = 20 \text{ MHz}$ | 84 | 94 | | 89 | | | |
| | | $f_{\text{IN}} = 70 \text{ MHz}$ | 92 | | | 86 | | | |
| | | $f_{\text{IN}} = 100 \text{ MHz}$ | 85 | | | 81 | | | |
| | | $f_{\text{IN}} = 170 \text{ MHz}$ | 86 | | | 83 | | | |
| | | $f_{\text{IN}} = 230 \text{ MHz}$ | 81 | | | 79 | | | |

(1) Reported from a 1-MHz offset.

AC Performance: ADC3241 (continued)

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 25 MSPS, 50% clock duty cycle, $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | ADC3241 ($f_S = 25\text{ MSPS}$) | | | | | | UNIT |
|--------------|--|--|------|-----|------------|-----|-----|------|
| | | DITHER ON | | | DITHER OFF | | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| HD2 | Second-order harmonic distortion | $f_{\text{IN}} = 10\text{ MHz}$ | | 104 | | | 96 | dBc |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 84 | 100 | | | 95 | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 100 | | | 95 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 95 | | | 93 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 87 | | | 87 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 81 | | | 81 | |
| HD3 | Third-order harmonic distortion | $f_{\text{IN}} = 10\text{ MHz}$ | | 95 | | | 88 | dBc |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 84 | 94 | | | 92 | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 92 | | | 86 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 85 | | | 82 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 87 | | | 83 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 82 | | | 80 | |
| Non HD2, HD3 | Spurious-free dynamic range (excluding HD2, HD3) | $f_{\text{IN}} = 10\text{ MHz}$ | | 100 | | | 92 | dBc |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 87 | 101 | | | 92 | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 100 | | | 92 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 98 | | | 92 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 100 | | | 92 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 96 | | | 92 | |
| THD | Total harmonic distortion | $f_{\text{IN}} = 10\text{ MHz}$ | | 94 | | | 85 | dBc |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 80.5 | 92 | | | 85 | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 91 | | | 84 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 86 | | | 82 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 84 | | | 81 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 78 | | | 76 | |
| IMD3 | Two-tone, third-order intermodulation distortion | $f_{\text{IN1}} = 45\text{ MHz}$, $f_{\text{IN2}} = 50\text{ MHz}$ | | -94 | | | -93 | dBFS |
| | | $f_{\text{IN1}} = 185\text{ MHz}$, $f_{\text{IN2}} = 190\text{ MHz}$ | | -92 | | | -90 | |

7.9 AC Performance: ADC3242

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | ADC3242 ($f_s = 50\text{ MSPS}$) | | | | | | UNIT |
|-----------------------------------|--|----------------------------------|------------------------------------|--------|-----|------------|-----|-----|---------|
| | | | DITHER ON | | | DITHER OFF | | | |
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| DYNAMIC AC CHARACTERISTICS | | | | | | | | | |
| SNR | Signal-to-noise ratio (from 1-MHz offset) | $f_{\text{IN}} = 10\text{ MHz}$ | 73.3 | | | 73.7 | | | dBFS |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 70.5 | 73.3 | | 73.8 | | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 73 | | | 73.3 | | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | 72.6 | | | 73.1 | | | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | 71.7 | | | 72.1 | | | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | 70.9 | | | 71.2 | | | |
| | Signal-to-noise ratio (full Nyquist band) | $f_{\text{IN}} = 10\text{ MHz}$ | 72.5 | | | 72.9 | | | |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 72.6 | | | 73.1 | | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 72.3 | | | 72.6 | | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | 71.9 | | | 72.4 | | | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | 71.1 | | | 71.5 | | | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | 70.3 | | | 70.6 | | | |
| NSD ⁽¹⁾ | Noise spectral density (averaged across Nyquist zone) | $f_{\text{IN}} = 10\text{ MHz}$ | -147.1 | | | -147.5 | | | dBFS/Hz |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | -147.1 | -144.5 | | -147.6 | | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | -146.8 | | | -147.1 | | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | -146.4 | | | -146.9 | | | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | -145.5 | | | -145.9 | | | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | -144.7 | | | -145 | | | |
| SINAD ⁽¹⁾ | Signal-to-noise and distortion ratio | $f_{\text{IN}} = 10\text{ MHz}$ | 73.2 | | | 73.6 | | | dBFS |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 69.6 | 73.4 | | 73.6 | | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 72.9 | | | 73.2 | | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | 72.5 | | | 72.9 | | | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | 71.5 | | | 71.7 | | | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | 70.5 | | | 70.6 | | | |
| ENOB ⁽¹⁾ | Effective number of bits | $f_{\text{IN}} = 10\text{ MHz}$ | 11.9 | | | 11.9 | | | Bits |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 11.3 | 11.9 | | 11.9 | | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 11.8 | | | 11.9 | | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | 11.7 | | | 11.8 | | | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | 11.6 | | | 11.6 | | | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | 11.4 | | | 11.4 | | | |
| SFDR | Spurious-free dynamic range | $f_{\text{IN}} = 10\text{ MHz}$ | 89 | | | 95 | | | dBc |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 83 | 93 | | 91 | | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 94 | | | 93 | | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | 88 | | | 86 | | | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | 85 | | | 82 | | | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | 82 | | | 80 | | | |

(1) Reported from a 1-MHz offset.

AC Performance: ADC3242 (continued)

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | ADC3242 ($f_s = 50\text{ MSPS}$) | | | | | | UNIT |
|--------------|--|--|-----|-----|------------|-----|-----|------|
| | | DITHER ON | | | DITHER OFF | | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| HD2 | Second-order harmonic distortion | $f_{\text{IN}} = 10\text{ MHz}$ | | 103 | | | 97 | dBc |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 83 | 99 | | | 95 | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 96 | | | 94 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 94 | | | 92 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 88 | | | 89 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 82 | | | 83 | |
| HD3 | Third-order harmonic distortion | $f_{\text{IN}} = 10\text{ MHz}$ | | 89 | | | 97 | dBc |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 83 | 93 | | | 95 | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 94 | | | 93 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 88 | | | 86 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 85 | | | 82 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 82 | | | 80 | |
| Non HD2, HD3 | Spurious-free dynamic range (excluding HD2, HD3) | $f_{\text{IN}} = 10\text{ MHz}$ | | 99 | | | 96 | dBc |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 87 | 101 | | | 93 | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 100 | | | 94 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 99 | | | 94 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 99 | | | 93 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 97 | | | 93 | |
| THD | Total harmonic distortion | $f_{\text{IN}} = 10\text{ MHz}$ | | 88 | | | 90 | dBc |
| | | $f_{\text{IN}} = 20\text{ MHz}$ | 79 | 92 | | | 87 | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | | 92 | | | 88 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 89 | | | 86 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 83 | | | 81 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 79 | | | 78 | |
| IMD3 | Two-tone, third-order intermodulation distortion | $f_{\text{IN1}} = 45\text{ MHz}$, $f_{\text{IN2}} = 50\text{ MHz}$ | | -95 | | | -95 | dBFS |
| | | $f_{\text{IN1}} = 185\text{ MHz}$, $f_{\text{IN2}} = 190\text{ MHz}$ | | -92 | | | -89 | |

7.10 AC Performance: ADC3243

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | ADC3243 ($f_s = 80\text{ MSPS}$) | | | | | | UNIT | |
|-----------------------------------|--|------------------------------------|--------|--------|------------|--------|-----|------|---------|
| | | DITHER ON | | | DITHER OFF | | | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| DYNAMIC AC CHARACTERISTICS | | | | | | | | | |
| SNR | Signal-to-noise ratio (from 1-MHz offset) | $f_{\text{IN}} = 10\text{ MHz}$ | 73.1 | | | 73.5 | | | dBFS |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 70.7 | 72.9 | | 73.3 | | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | 72.7 | | | 73 | | | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | 72 | | | 72.4 | | | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | 71.4 | | | 71.7 | | | |
| | Signal-to-noise ratio (full Nyquist band) | $f_{\text{IN}} = 10\text{ MHz}$ | 72.4 | | | 72.8 | | | |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 72.3 | | | 72.6 | | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | 72.1 | | | 72.3 | | | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | 71.4 | | | 71.7 | | | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | 70.9 | | | 71.2 | | | |
| NSD ⁽¹⁾ | Noise spectral density (averaged across Nyquist zone) | $f_{\text{IN}} = 10\text{ MHz}$ | -149.0 | | | -149.4 | | | dBFS/Hz |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | -148.8 | -146.7 | | -149.2 | | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | -148.6 | | | -148.9 | | | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | -147.9 | | | -148.3 | | | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | -147.3 | | | -147.6 | | | |
| SINAD ⁽¹⁾ | Signal-to-noise and distortion ratio | $f_{\text{IN}} = 10\text{ MHz}$ | 73.1 | | | 73.4 | | | dBFS |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 69.6 | 72.9 | | 73.2 | | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | 72.7 | | | 72.9 | | | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | 71.9 | | | 72.2 | | | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | 71.2 | | | 71.3 | | | |
| ENOB ⁽¹⁾ | Effective number of bits | $f_{\text{IN}} = 10\text{ MHz}$ | 11.8 | | | 11.9 | | | Bits |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 11.3 | 11.8 | | 11.9 | | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | 11.8 | | | 11.8 | | | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | 11.6 | | | 11.7 | | | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | 11.5 | | | 11.6 | | | |
| SFDR | Spurious-free dynamic range | $f_{\text{IN}} = 10\text{ MHz}$ | 89 | | | 94 | | | dBc |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 82 | 93 | | 93 | | | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | 93 | | | 91 | | | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | 87 | | | 87 | | | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | 85 | | | 83 | | | |

(1) Reported from a 1-MHz offset.

AC Performance: ADC3243 (continued)

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | ADC3243 ($f_S = 80\text{ MSPS}$) | | | | | | UNIT |
|--------------|--|--|-----|-----|------------|-----|-----|------|
| | | DITHER ON | | | DITHER OFF | | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| HD2 | Second-order harmonic distortion | $f_{\text{IN}} = 10\text{ MHz}$ | | 102 | | | 98 | dBc |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 82 | 95 | | | 93 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 95 | | | 93 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 87 | | | 87 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 85 | | | 85 | |
| HD3 | Third-order harmonic distortion | $f_{\text{IN}} = 10\text{ MHz}$ | | 89 | | | 95 | dBc |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 83 | 94 | | | 94 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 95 | | | 96 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 92 | | | 90 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 89 | | | 84 | |
| Non HD2, HD3 | Spurious-free dynamic range (excluding HD2, HD3) | $f_{\text{IN}} = 10\text{ MHz}$ | | 93 | | | 95 | dBc |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 86 | 100 | | | 95 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 100 | | | 95 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 99 | | | 95 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 98 | | | 94 | |
| THD | Total harmonic distortion | $f_{\text{IN}} = 10\text{ MHz}$ | | 88 | | | 91 | dBc |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 76 | 91 | | | 89 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 91 | | | 88 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 85 | | | 84 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 83 | | | 81 | |
| IMD3 | Two-tone, third-order intermodulation distortion | $f_{\text{IN1}} = 45\text{ MHz}$, $f_{\text{IN2}} = 50\text{ MHz}$ | | -93 | | | -92 | dBFS |
| | | $f_{\text{IN1}} = 185\text{ MHz}$, $f_{\text{IN2}} = 190\text{ MHz}$ | | -91 | | | -89 | |

7.11 AC Performance: ADC3244

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and -1-dBFS differential input, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | ADC3244 ($f_s = 125 \text{ MSPS}$) | | | | | | UNIT | |
|-----------------------------------|--|--------------------------------------|--------|--------|------------|--------|-----|------|---------|
| | | DITHER ON | | | DITHER OFF | | | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| DYNAMIC AC CHARACTERISTICS | | | | | | | | | |
| SNR | Signal-to-noise ratio (from 1-MHz offset) | $f_{\text{IN}} = 10 \text{ MHz}$ | 72.9 | | | 73.3 | | | dBFS |
| | | $f_{\text{IN}} = 70 \text{ MHz}$ | 71 | 72.6 | | 73 | | | |
| | | $f_{\text{IN}} = 100 \text{ MHz}$ | 72.4 | | | 72.8 | | | |
| | | $f_{\text{IN}} = 170 \text{ MHz}$ | 71.7 | | | 72.2 | | | |
| | | $f_{\text{IN}} = 230 \text{ MHz}$ | 71 | | | 71.6 | | | |
| | Signal-to-noise ratio (full Nyquist band) | $f_{\text{IN}} = 10 \text{ MHz}$ | 72.5 | | | 72.9 | | | |
| | | $f_{\text{IN}} = 70 \text{ MHz}$ | 72.2 | | | 72.6 | | | |
| | | $f_{\text{IN}} = 100 \text{ MHz}$ | 72.1 | | | 72.5 | | | |
| | | $f_{\text{IN}} = 170 \text{ MHz}$ | 71.4 | | | 71.9 | | | |
| | | $f_{\text{IN}} = 230 \text{ MHz}$ | 70.7 | | | 71.3 | | | |
| NSD ⁽¹⁾ | Noise spectral density (averaged across Nyquist zone) | $f_{\text{IN}} = 10 \text{ MHz}$ | -150.8 | | | -151.1 | | | dBFS/Hz |
| | | $f_{\text{IN}} = 70 \text{ MHz}$ | -150.5 | -148.9 | | -150.9 | | | |
| | | $f_{\text{IN}} = 100 \text{ MHz}$ | -150.3 | | | -150.7 | | | |
| | | $f_{\text{IN}} = 170 \text{ MHz}$ | -149.6 | | | -150.1 | | | |
| | | $f_{\text{IN}} = 230 \text{ MHz}$ | -148.9 | | | -149.5 | | | |
| SINAD ⁽¹⁾ | Signal-to-noise and distortion ratio | $f_{\text{IN}} = 10 \text{ MHz}$ | 72.8 | | | 73 | | | dBFS |
| | | $f_{\text{IN}} = 70 \text{ MHz}$ | 69.6 | 72.6 | | 72.9 | | | |
| | | $f_{\text{IN}} = 100 \text{ MHz}$ | 72.3 | | | 72.5 | | | |
| | | $f_{\text{IN}} = 170 \text{ MHz}$ | 71.5 | | | 71.9 | | | |
| | | $f_{\text{IN}} = 230 \text{ MHz}$ | 70.7 | | | 71.1 | | | |
| ENOB ⁽¹⁾ | Effective number of bits | $f_{\text{IN}} = 10 \text{ MHz}$ | 11.8 | | | 11.8 | | | Bits |
| | | $f_{\text{IN}} = 70 \text{ MHz}$ | 11.3 | 11.8 | | 11.8 | | | |
| | | $f_{\text{IN}} = 100 \text{ MHz}$ | 11.7 | | | 11.8 | | | |
| | | $f_{\text{IN}} = 170 \text{ MHz}$ | 11.6 | | | 11.6 | | | |
| | | $f_{\text{IN}} = 230 \text{ MHz}$ | 11.5 | | | 11.5 | | | |
| SFDR | Spurious-free dynamic range | $f_{\text{IN}} = 10 \text{ MHz}$ | 93 | | | 86 | | | dBc |
| | | $f_{\text{IN}} = 70 \text{ MHz}$ | 82 | 94 | | 89 | | | |
| | | $f_{\text{IN}} = 100 \text{ MHz}$ | 89 | | | 85 | | | |
| | | $f_{\text{IN}} = 170 \text{ MHz}$ | 85 | | | 85 | | | |
| | | $f_{\text{IN}} = 230 \text{ MHz}$ | 83 | | | 82 | | | |

(1) Reported from a 1-MHz offset.

AC Performance: ADC3244 (continued)

Typical values are over the operating free-air temperature range, at $T_A = 25^\circ\text{C}$, full temperature range is $T_{\text{MIN}} = -40^\circ\text{C}$ to $T_{\text{MAX}} = 85^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $\text{AVDD} = \text{DVDD} = 1.8\text{ V}$, and -1-dBFS differential input, unless otherwise noted.

| PARAMETER | TEST CONDITIONS | ADC3244 ($f_s = 125\text{ MSPS}$) | | | | | | UNIT |
|--------------|--|--|-----|-----|------------|-----|-----|------|
| | | DITHER ON | | | DITHER OFF | | | |
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| HD2 | Second-order harmonic distortion | $f_{\text{IN}} = 10\text{ MHz}$ | | 95 | | | 96 | dBc |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 82 | 96 | | | 95 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 91 | | | 90 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 85 | | | 85 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 83 | | | 83 | |
| HD3 | Third-order harmonic distortion | $f_{\text{IN}} = 10\text{ MHz}$ | | 94 | | | 86 | dBc |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 83 | 94 | | | 89 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 91 | | | 85 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 97 | | | 89 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 87 | | | 85 | |
| Non HD2, HD3 | Spurious-free dynamic range (excluding HD2, HD3) | $f_{\text{IN}} = 10\text{ MHz}$ | | 100 | | | 95 | dBc |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 86 | 99 | | | 95 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 99 | | | 95 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 100 | | | 91 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 96 | | | 92 | |
| THD | Total harmonic distortion | $f_{\text{IN}} = 10\text{ MHz}$ | | 91 | | | 85 | dBc |
| | | $f_{\text{IN}} = 70\text{ MHz}$ | 76 | 91 | | | 86 | |
| | | $f_{\text{IN}} = 100\text{ MHz}$ | | 87 | | | 83 | |
| | | $f_{\text{IN}} = 170\text{ MHz}$ | | 84 | | | 82 | |
| | | $f_{\text{IN}} = 230\text{ MHz}$ | | 81 | | | 80 | |
| IMD3 | Two-tone, third-order intermodulation distortion | $f_{\text{IN1}} = 45\text{ MHz}$, $f_{\text{IN2}} = 50\text{ MHz}$ | | -97 | | | -95 | dBFS |
| | | $f_{\text{IN1}} = 185\text{ MHz}$, $f_{\text{IN2}} = 190\text{ MHz}$ | | -91 | | | -90 | |

7.12 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|--|---------------------------|------|------|------|
| DIGITAL INPUTS (RESET, SCLK, SDATA, SEN, PDN) | | | | | | |
| V _{IH} | High-level input voltage | All digital inputs support 1.8-V and 3.3-V CMOS logic levels | 1.3 | | | V |
| V _{IL} | Low-level input voltage | All digital inputs support 1.8-V and 3.3-V CMOS logic levels | | | 0.4 | V |
| I _{IH} | High-level input current | RESET, SDATA, SCLK, PDN | V _{HIGH} = 1.8 V | 10 | | μA |
| | | SEN ⁽¹⁾ | V _{HIGH} = 1.8 V | 0 | | |
| I _{IL} | Low-level input current | RESET, SDATA, SCLK, PDN | V _{LOW} = 0 V | 0 | | μA |
| | | SEN | V _{LOW} = 0 V | 10 | | |
| DIGITAL INPUTS (SYSREFF, SYSREFM) | | | | | | |
| V _{IH} | High-level input voltage | | | 1.3 | | V |
| V _{IL} | Low-level input voltage | | | 0.5 | | V |
| | Common-mode voltage for SYSREF | | | 0.9 | | V |
| DIGITAL OUTPUTS, CMOS INTERFACE (SDOUT) | | | | | | |
| V _{OH} | High-level output voltage | | DVDD – 0.1 | DVDD | | V |
| V _{OL} | Low-level output voltage | | | 0 | 0.1 | V |
| DIGITAL OUTPUTS, LVDS INTERFACE | | | | | | |
| V _{ODH} | High-level output differential voltage | With an external 100-Ω termination | 280 | 410 | 460 | mV |
| V _{ODL} | Low-level output differential voltage | With an external 100-Ω termination | –460 | –410 | –280 | mV |
| V _{OCM} | Output common-mode voltage | | | 1.05 | | V |

- (1) SEN has an internal 150-kΩ pull-up resistor to AVDD. Because the pull-up resistor is weak, SEN can also be driven by 1.8-V or 3.3-V CMOS buffers.

7.13 Timing Requirements: General

Typical values are at T_A = 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C.

| | | | MIN | TYP | MAX | UNIT |
|----------------------------|-----------------------|--|------|------|------|--------------------|
| t _A | Aperture delay | | 1.24 | 1.44 | 1.64 | ns |
| | | Aperture delay matching between two channels of the same device | | ±70 | | ps |
| | | Variation of aperture delay between two devices at the same temperature and supply voltage | | ±150 | | ps |
| t _J | Aperture jitter | | | 130 | | f _S rms |
| Wake-up time | | Time to valid data after exiting standby power-down mode | | 35 | 65 | μs |
| | | Time to valid data after exiting global power-down mode (in this mode, both channels power down) | | 85 | 140 | |
| ADC latency ⁽¹⁾ | | 2-wire mode (default) | | 9 | | Clock cycles |
| | | 1-wire mode | | 8 | | |
| t _{SU_SYSREF} | SYSREF reference time | Setup time for SYSREF referenced to input clock rising edge | 1000 | | | ps |
| t _{H_SYSREF} | | Hold time for SYSREF referenced to input clock rising edge | 100 | | | |

- (1) Overall latency = ADC latency + t_{PD}.

7.14 Timing Requirements: LVDS Output

Typical values are at 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, 7x serialization, C_{LOAD} = 3.3 pF⁽¹⁾, and R_{LOAD} = 100 Ω⁽²⁾, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 85°C.⁽³⁾⁽⁴⁾

| | | MIN | TYP | MAX | UNIT | |
|--|--|-------------|--|-----|------|----|
| t _{SU} | Data setup time: data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM) ⁽⁵⁾ | 0.36 | 0.42 | | ns | |
| t _{HO} | Data hold time: zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid ⁽⁵⁾ | 0.36 | 0.47 | | ns | |
| | LVDS bit clock duty cycle: duty cycle of differential clock (CLKOUTP – CLKOUTM) | 49% | | | | |
| t _{PDI} | Clock propagation delay: input clock falling edge cross-over to frame clock rising edge cross-over 10 MSPS < sampling frequency < 125 MSPS | 1-wire mode | 2.7 | 4.5 | 6.5 | ns |
| | | 2-wire mode | 0.44 × t _S + t _{DELAY} | | | |
| t _{DELAY} | Delay time | 3 | 4.5 | 5.9 | ns | |
| t _{FALL} , t _{RISE} | Data fall time, data rise time: rise time measured from –100 mV to 100 mV, 10 MSPS ≤ Sampling frequency ≤ 125 MSPS | 0.11 | | | ns | |
| t _{CLKRISE} , t _{CLKFALL} | Output clock rise time, output clock fall time: rise time measured from –100 mV to 100 mV, 10 MSPS ≤ Sampling frequency ≤ 125 MSPS | 0.11 | | | ns | |

- (1) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground
- (2) R_{LOAD} is the differential load resistance between the LVDS output pair.
- (3) Measurements are done with a transmission line of a 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
- (4) Timing parameters are ensured by design and characterization and are not tested in production.
- (5) Data valid refers to a logic high of +100 mV and a logic low of –100 mV.

Table 1. LVDS Timings at Lower Sampling Frequencies: 7x Serialization (2-Wire Mode)

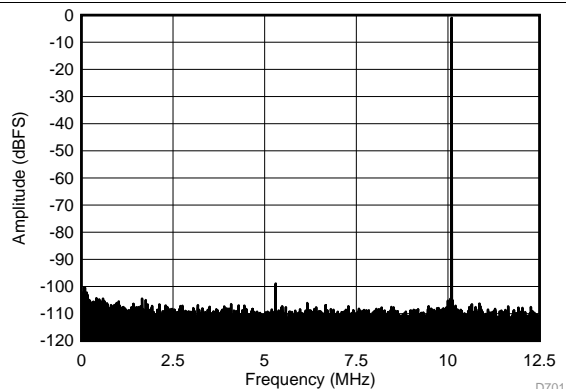
| SAMPLING FREQUENCY (MSPS) | SETUP TIME (t _{SU} , ns) | | | HOLD TIME (t _{HO} , ns) | | |
|---------------------------|-----------------------------------|------|-----|----------------------------------|------|-----|
| | MIN | TYP | MAX | MIN | TYP | MAX |
| 25 | 2.27 | 2.6 | | 2.41 | 2.6 | |
| 40 | 1.44 | 1.6 | | 1.51 | 1.7 | |
| 50 | 1.2 | 1.32 | | 1.24 | 1.4 | |
| 60 | 0.95 | 1.04 | | 0.97 | 1.09 | |
| 80 | 0.68 | 0.75 | | 0.72 | 0.81 | |
| 100 | 0.5 | 0.57 | | 0.53 | 0.62 | |

Table 2. LVDS Timings at Lower Sampling Frequencies: 14x Serialization (1-Wire Mode)

| SAMPLING FREQUENCY (MSPS) | SETUP TIME (t _{SU} , ns) | | | HOLD TIME (t _{HO} , ns) | | |
|---------------------------|-----------------------------------|------|-----|----------------------------------|------|-----|
| | MIN | TYP | MAX | MIN | TYP | MAX |
| 25 | 1.1 | 1.24 | | 1.19 | 1.34 | |
| 40 | 0.66 | 0.72 | | 0.74 | 0.82 | |
| 50 | 0.48 | 0.55 | | 0.54 | 0.64 | |
| 60 | 0.35 | 0.41 | | 0.42 | 0.51 | |
| 80 | 0.17 | 0.24 | | 0.3 | 0.38 | |

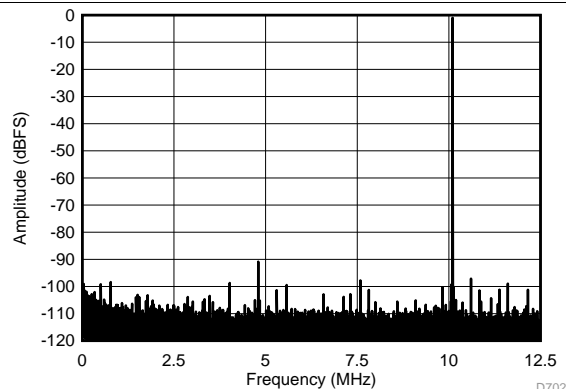
7.15 Typical Characteristics: ADC3241

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 25 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.



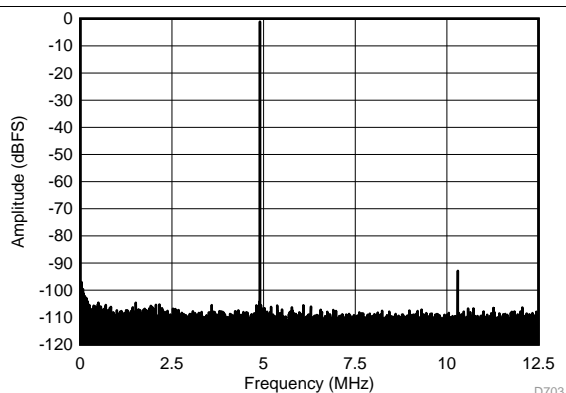
SFDR = 97.9 dBc, SNR = 73.8 dBFS, SINAD = 73.8 dBFS,
THD = 96.8 dBc, HD2 = -110.0 dBc, HD3 = -97.9 dBc

Figure 1. FFT for 10-MHz Input Signal (Dither On)



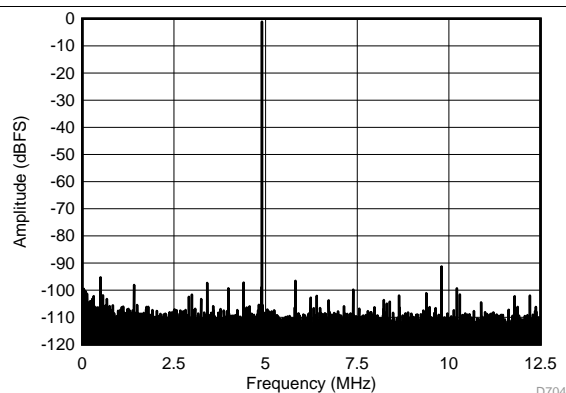
SFDR = 89.8 dBc, SNR = 74.5 dBFS, SINAD = 74.3 dBFS,
THD = 88.3 dBc, HD2 = -89.8 dBc, HD3 = -100.3 dBc

Figure 2. FFT for 10-MHz Input Signal (Dither Off)



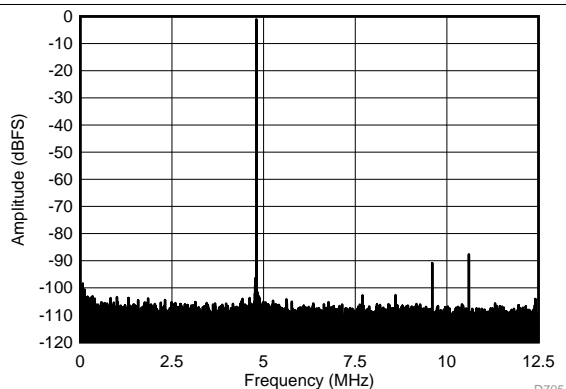
SFDR = 91.8 dBc, SNR = 73.4 dBFS, SINAD = 73.4 dBFS,
THD = 91.4 dBc, HD2 = -108.2 dBc, HD3 = -91.8 dBc

Figure 3. FFT for 70-MHz Input Signal (Dither On)



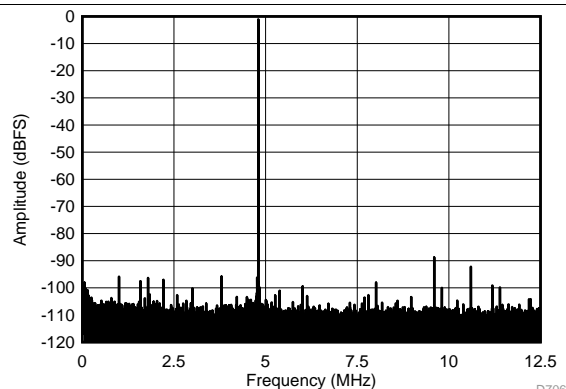
SFDR = 90.2 dBc, SNR = 74.1 dBFS, SINAD = 73.9 dBFS,
THD = 88.7 dBc, HD2 = -90.2 dBc, HD3 = -100.5 dBc

Figure 4. FFT for 70-MHz Input Signal (Dither Off)



SFDR = 86.6 dBc, SNR = 72.1 dBFS, SINAD = 71.9 dBFS,
THD = 84.7 dBc, HD2 = -89.8 dBc, HD3 = -86.6 dBc

Figure 5. FFT for 170-MHz Input Signal (Dither On)

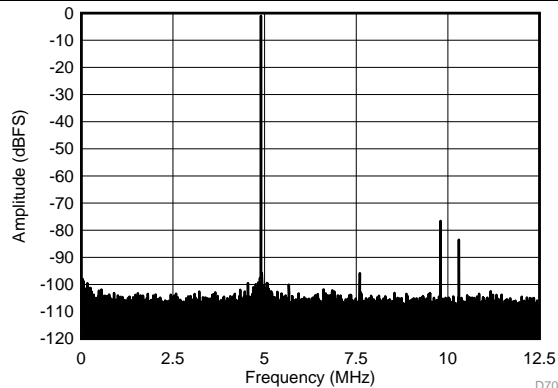


SFDR = 87.7 dBc, SNR = 72.5 dBFS, SINAD = 72.3 dBFS,
THD = 85 dBc, HD2 = -87.7 dBc, HD3 = -91.2 dBc

Figure 6. FFT for 170-MHz Input Signal (Dither Off)

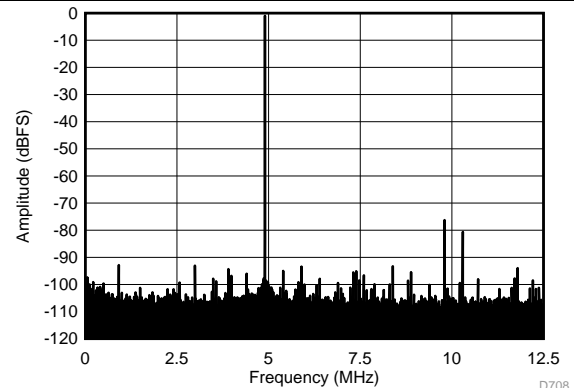
Typical Characteristics: ADC3241 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 25 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1 dBFS differential input, $2\text{-}V_{pp}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.



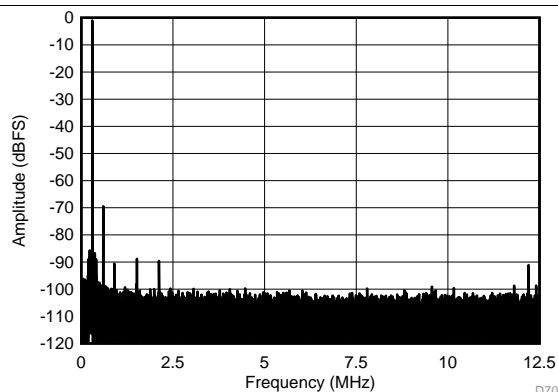
SFDR = 75.6 dBc, SNR = 69.8 dBFS, SINAD = 68.8 dBFS, THD = 74.8 dBc, HD2 = -75.6 dBc , HD3 = -82.5 dBc

Figure 7. FFT for 270-MHz Input Signal (Dither On)



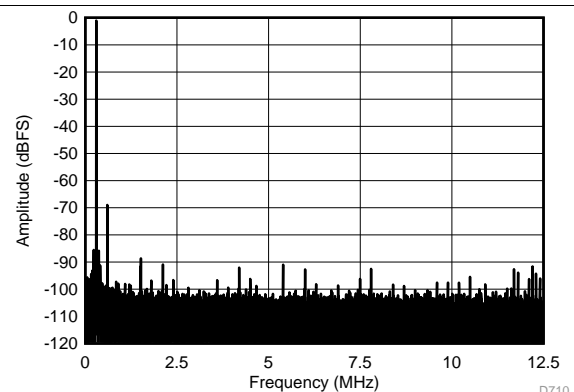
SFDR = 75.3 dBc, SNR = 70.0 dBFS, SINAD = 68.8 dBFS, THD = 73.8 dBc, HD2 = -75.3 dBc , HD3 = -79.6 dBc

Figure 8. FFT for 270-MHz Input Signal (Dither Off)



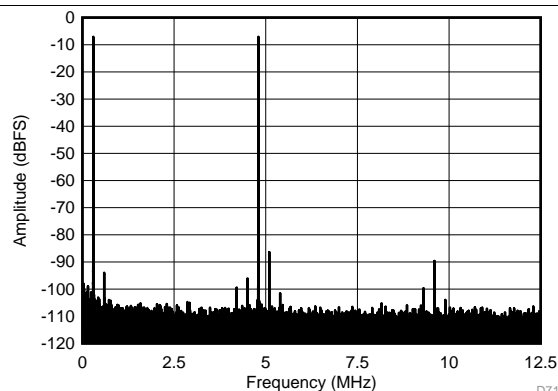
SFDR = 68.4 dBc, SNR = 67.2 dBFS, SINAD = 67.2 dBFS, THD = 92.6 dBc, HD2 = -68.4 dBc , HD3 = -89.5 dBc

Figure 9. FFT for 450-MHz Input Signal (Dither On)



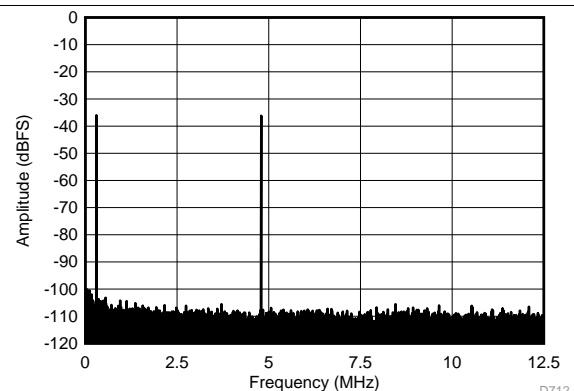
SFDR = 67.9 dBc, SNR = 67.2 dBFS, SINAD = 67.2 dBFS, THD = 87.6 dBc, HD2 = -67.9 dBc , HD3 = -96.9 dBc

Figure 10. FFT for 450-MHz Input Signal (Dither Off)



$f_{IN1} = 46\text{ MHz}$, $f_{IN2} = 50\text{ MHz}$, IMD3 = 82.4 dBFS, each tone at -7 dBFS

Figure 11. FFT for Two-Tone Input Signal (-7 dBFS at 46 MHz and 50 MHz)

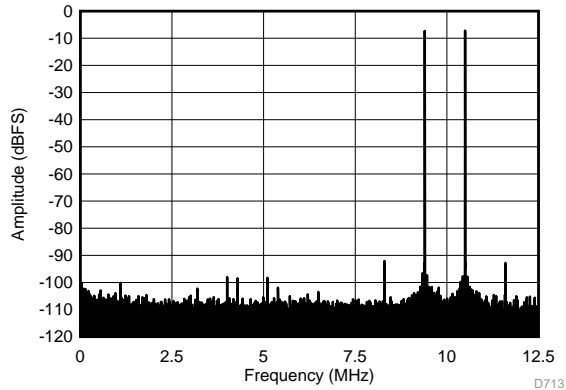


$f_{IN1} = 46\text{ MHz}$, $f_{IN2} = 50\text{ MHz}$, IMD3 = 90 dBFS, each tone at -36 dBFS

Figure 12. FFT for Two-Tone Input Signal (-36 dBFS at 46 MHz and 50 MHz)

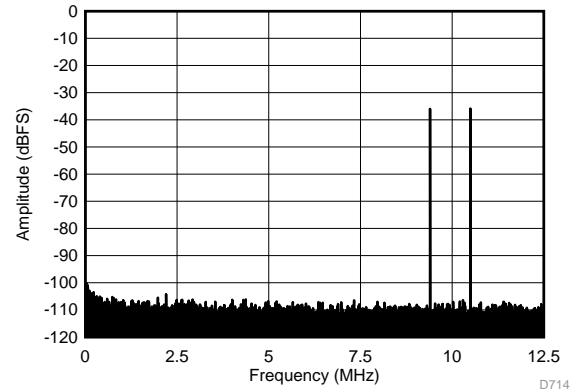
Typical Characteristics: ADC3241 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 25 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1 dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.



$f_{IN1} = 185\text{ MHz}$, $f_{IN2} = 190\text{ MHz}$, $\text{IMD3} = 78\text{ dBFS}$, each tone at -7 dBFS

Figure 13. FFT for Two-Tone Input Signal (-7 dBFS at 185 MHz and 190 MHz)



$f_{IN1} = 185\text{ MHz}$, $f_{IN2} = 190\text{ MHz}$, $\text{IMD3} = 89\text{ dBFS}$, each tone at -36 dBFS

Figure 14. FFT for Two-Tone Input Signal (-36 dBFS at 185 MHz and 190 MHz)

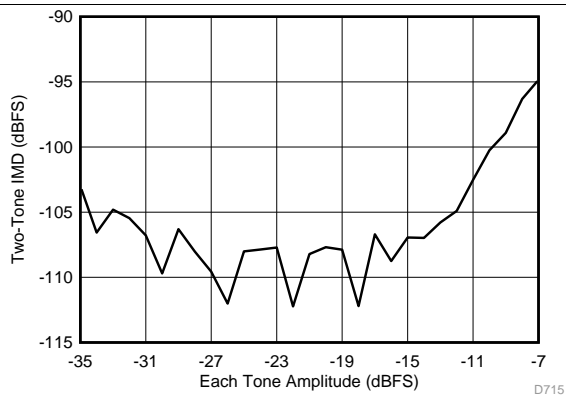


Figure 15. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

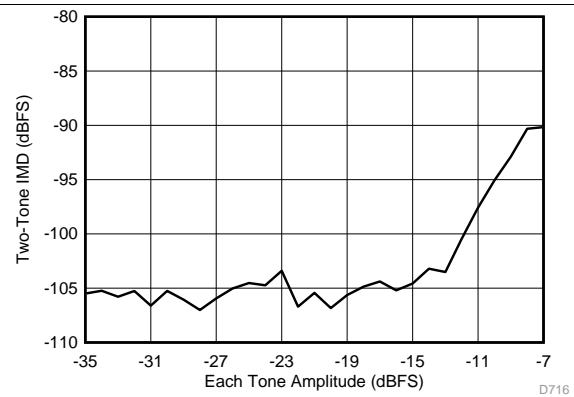


Figure 16. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

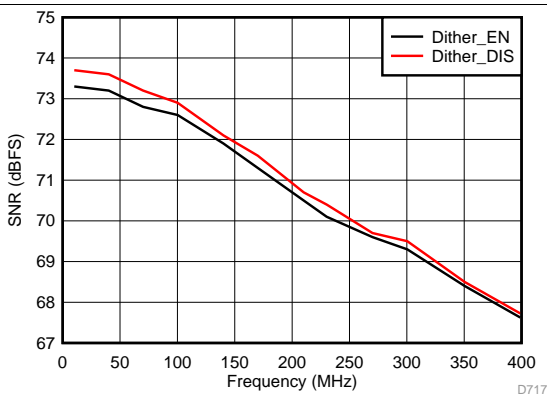


Figure 17. Signal-to-Noise Ratio vs Input Frequency

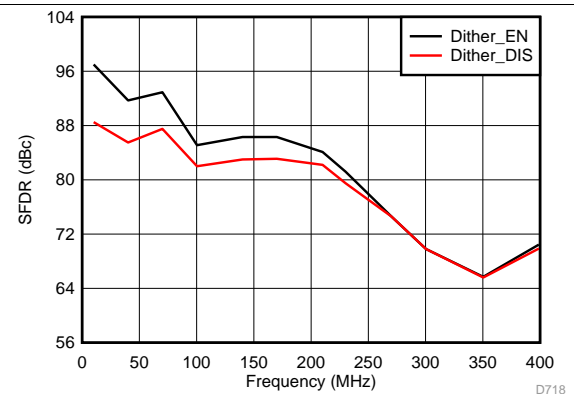


Figure 18. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics: ADC3241 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, $2\cdot V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.

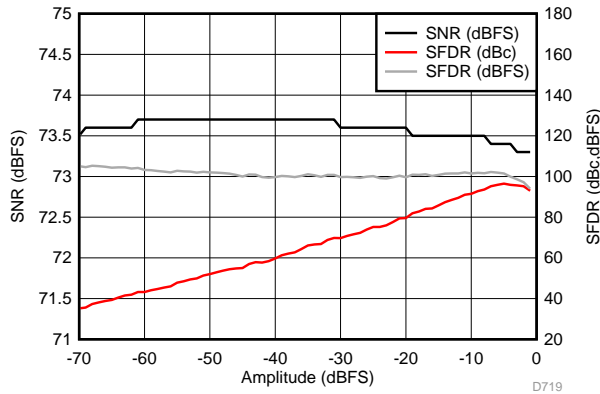


Figure 19. Performance vs Input Amplitude (30 MHz)

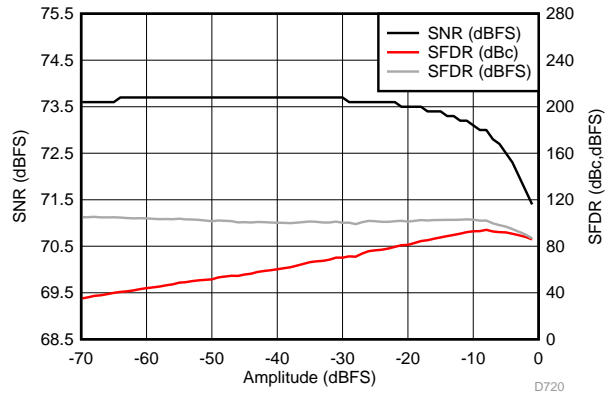


Figure 20. Performance vs Input Amplitude (170 MHz)

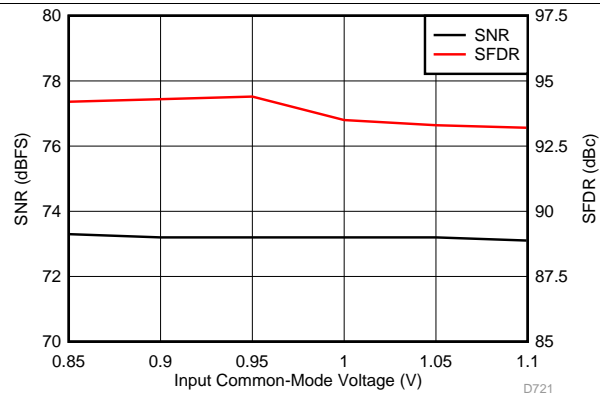


Figure 21. Performance vs Input Common-Mode Voltage (30 MHz)

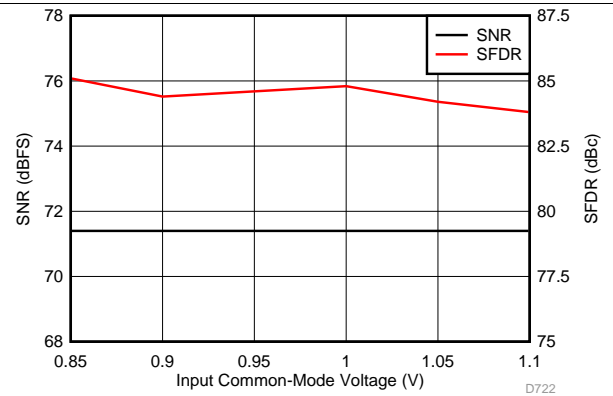


Figure 22. Performance vs Input Common-Mode Voltage (170 MHz)

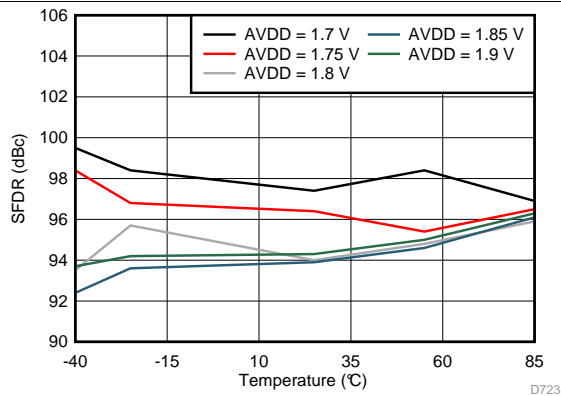


Figure 23. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (30 MHz)

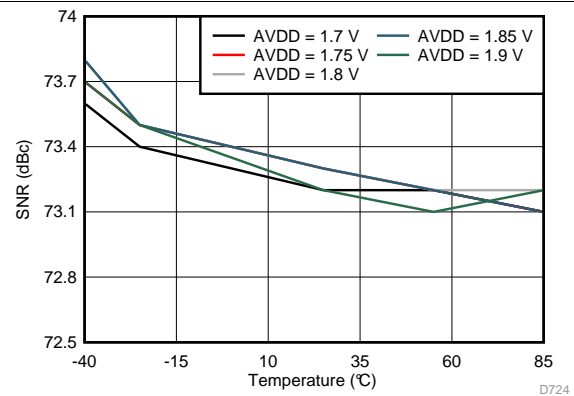


Figure 24. Signal-to-Noise Ratio vs AVDD Supply and Temperature (30 MHz)

Typical Characteristics: ADC3241 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, 2- V_{pp} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.

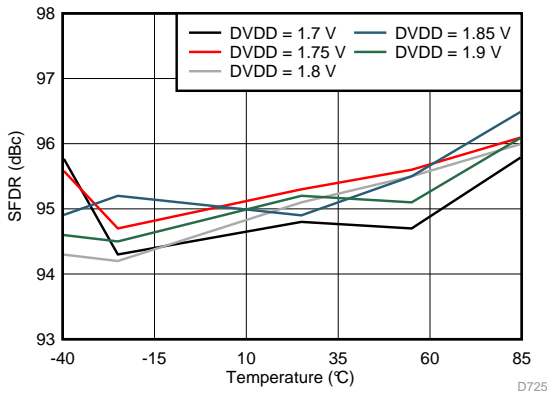


Figure 25. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (30 MHz)

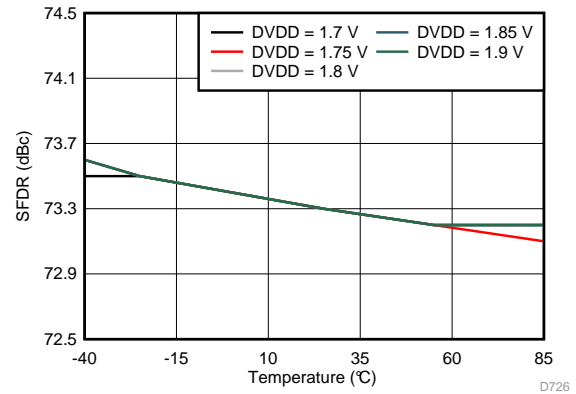


Figure 26. Signal-to-Noise Ratio vs DVDD Supply and Temperature (30 MHz)

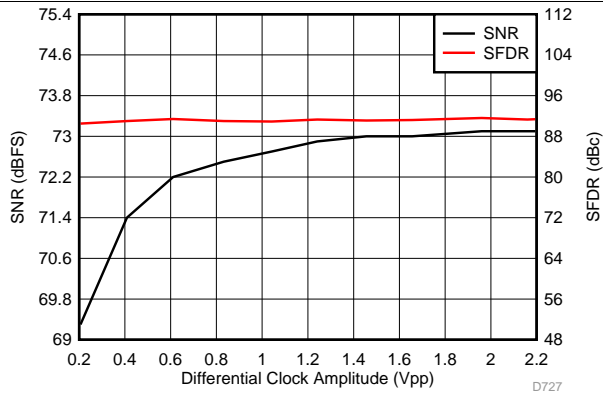


Figure 27. Performance vs Clock Amplitude (40 MHz)

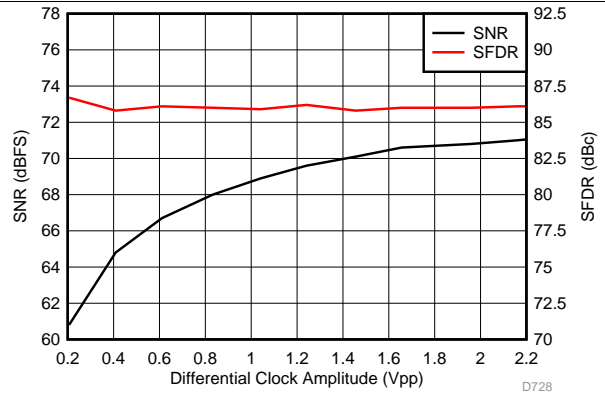


Figure 28. Performance vs Clock Amplitude (150 MHz)

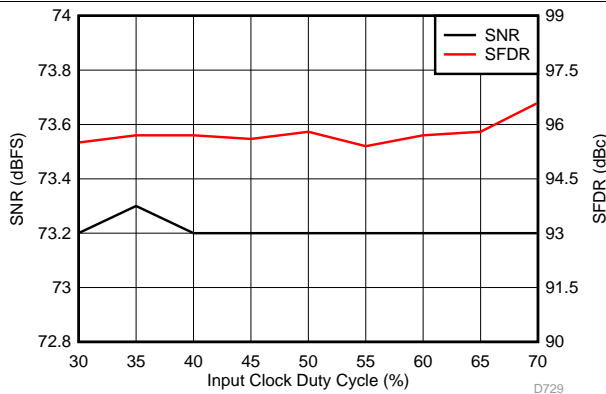


Figure 29. Performance vs Clock Duty Cycle (30 MHz)

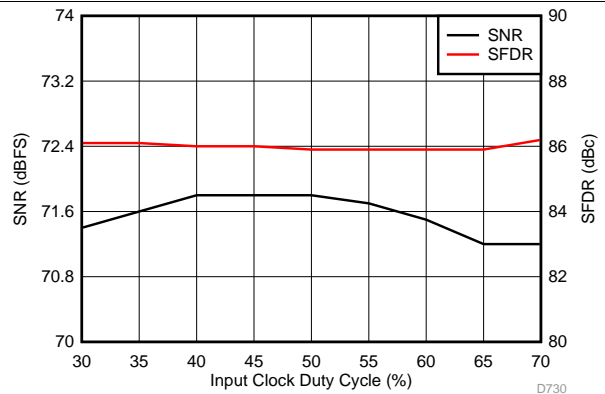
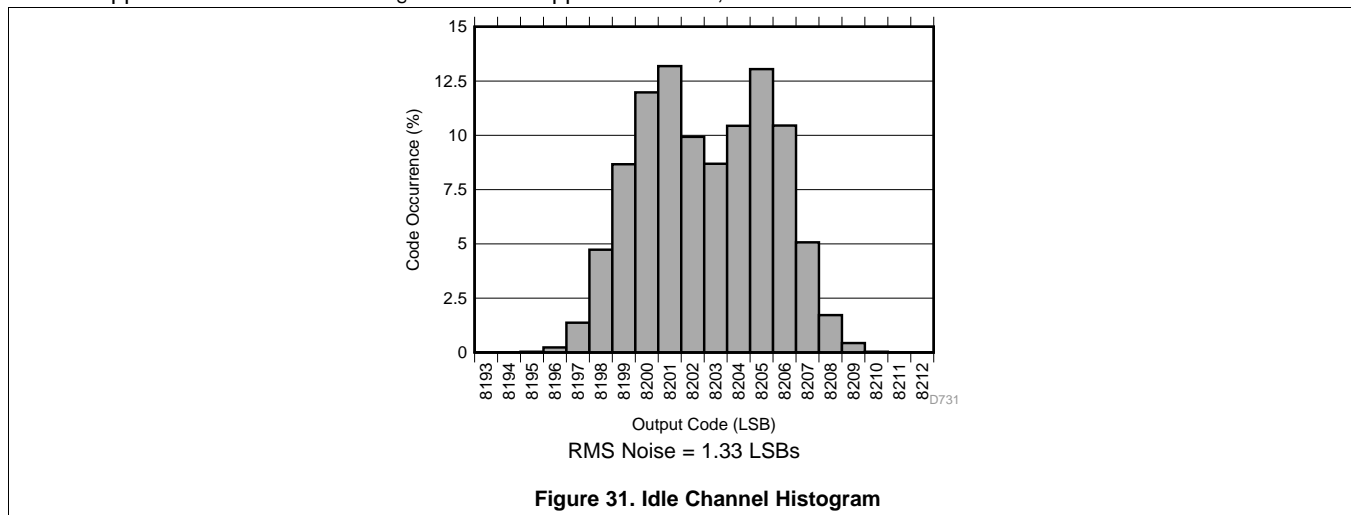


Figure 30. Performance vs Clock Duty Cycle (150 MHz)

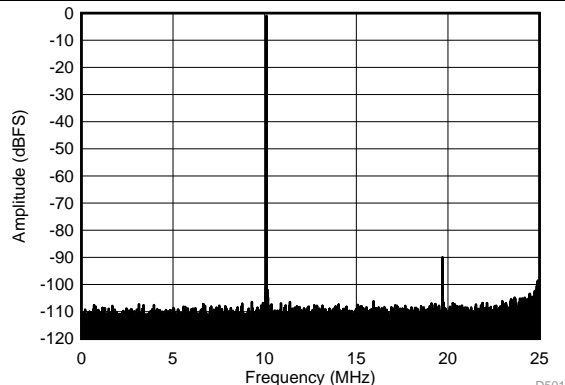
Typical Characteristics: ADC3241 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 25 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1 dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_S / 2$ when chopper is enabled, unless otherwise noted.



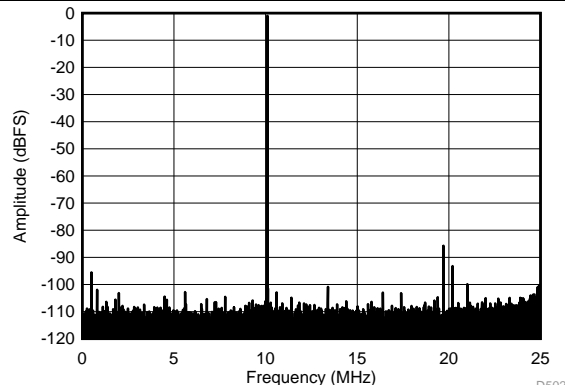
7.16 Typical Characteristics: ADC3242

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.



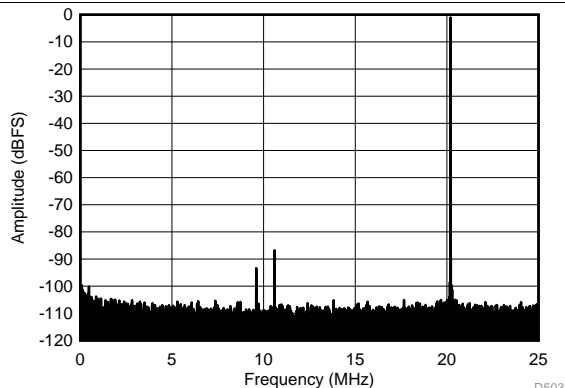
SFDR = 88.9 dBc, SFDR = 99.8 dBc (non 23), SNR = 73.6 dBFS, SINAD = 73.5 dBFS, THD = 88.8 dBc, HD2 = -111.4 dBc, HD3 = -88.9 dBc

Figure 32. FFT for 10-MHz Input Signal (Dither On)



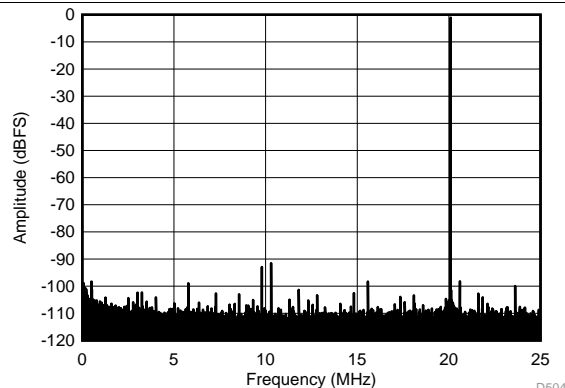
SFDR = 84.7 dBc, SFDR = 96.1 dBc (non 23), SNR = 74.1 dBFS, SINAD = 73.8 dBFS, THD = 83.5 dBc, HD2 = -92.2 dBc, HD3 = -84.7 dBc

Figure 33. FFT for 10-MHz Input Signal (Dither Off)



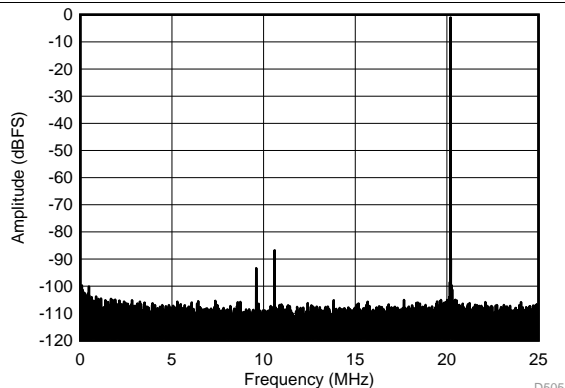
SFDR = 85.8 dBc, SFDR = 100.3 dBc (non 23), SNR = 72.4 dBFS, SINAD = 72.2 dBFS, THD = 84.8 dBc, HD2 = -92.3 dBc, HD3 = -85.8 dBc

Figure 34. FFT for 70-MHz Input Signal (Dither On)



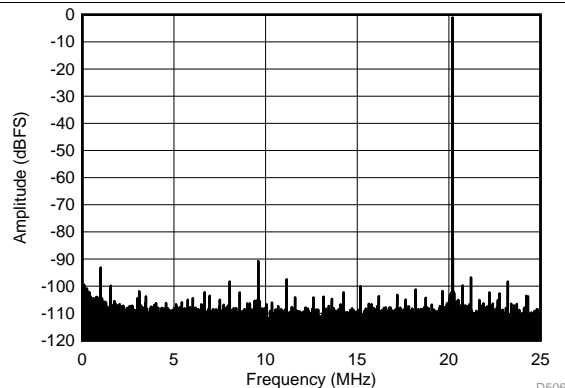
SFDR = 90.4 dBc, SFDR = 94.7 dBc (non 23), SNR = 73.9 dBFS, SINAD = 73.7 dBFS, THD = 87.5 dBc, HD2 = -91.9 dBc, HD3 = -90.4 dBc

Figure 35. FFT for 70-MHz Input Signal (Dither Off)



SFDR = 85.8 dBc, SFDR = 99.1 dBc (non 23), SNR = 72.4 dBFS, SINAD = 72.2 dBFS, THD = 84.8 dBc, HD2 = -92.3 dBc, HD3 = -85.8 dBc

Figure 36. FFT for 170-MHz Input Signal (Dither On)

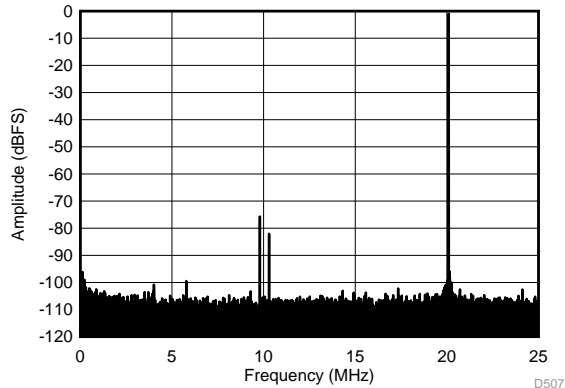


SFDR = 89.7 dBc, SFDR = 93 dBc (non 23), SNR = 72.9 dBFS, SINAD = 72.8 dBFS, THD = 86.6 dBc, HD2 = -89.7 dBc, HD3 = -107.7 dBc

Figure 37. FFT for 170-MHz Input Signal (Dither Off)

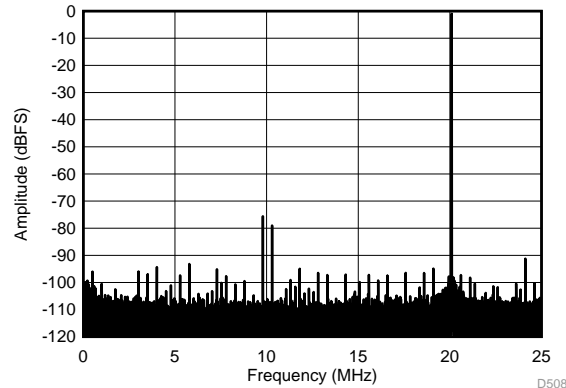
Typical Characteristics: ADC3242 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1 dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.



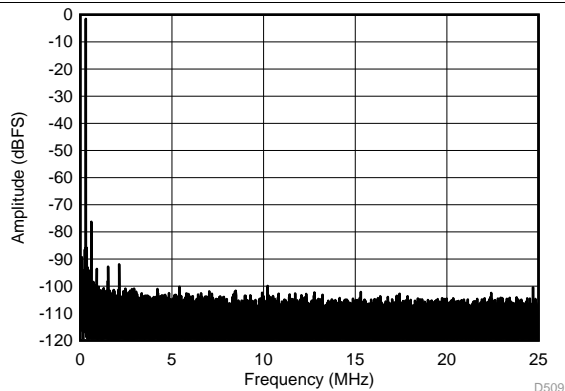
SFDR = 74.7 dBc, SFDR = 95.2 dBc (non 23), SNR = 70.7 dBFS, SINAD = 69.3 dBFS, THD = 73.8 dBc, HD2 = -74.7 dBc, HD3 = -81.1 dBc

Figure 38. FFT for 270-MHz Input Signal (Dither On)



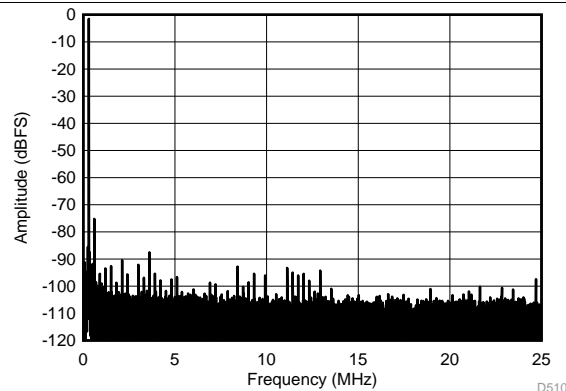
SFDR = 74.6 dBc, SFDR = 91.1 dBc (non 23), SNR = 70.9 dBFS, SINAD = 69.2 dBFS, THD = 72.9 dBc, HD2 = -74.6 dBc, HD3 = -78.0 dBc

Figure 39. FFT for 270-MHz Input Signal (Dither Off)



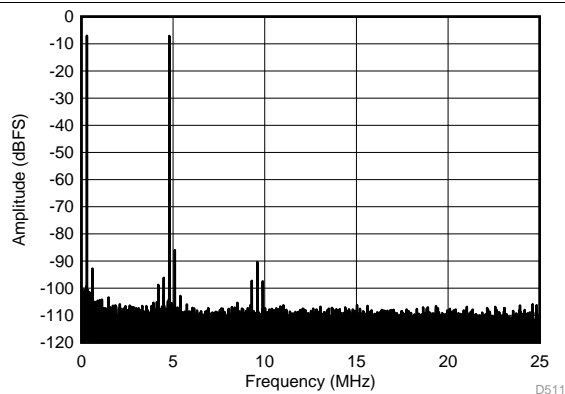
SFDR = 68.2 dBc, SNR = 69.0 dBFS, SINAD = 69.0 dBFS, THD = -85.7 dBc, HD2 = -68.2 dBc, HD3 = -86.5 dBc

Figure 40. FFT for 450-MHz Input Signal (Dither On)



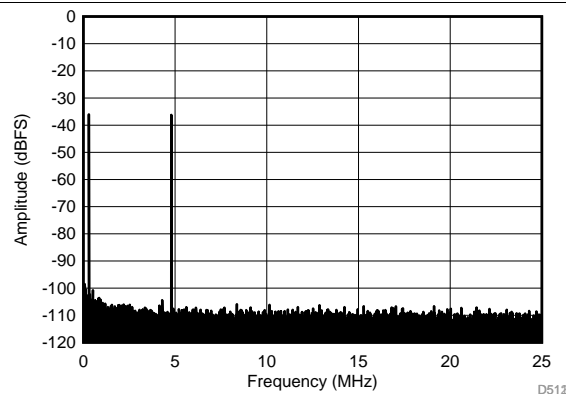
SFDR = 68.2 dBc, SNR = 69.2 dBFS, SINAD = 69.2 dBFS, THD = -86.4 dBc, HD2 = 68.2 dBc, HD3 = -90.3 dBc

Figure 41. FFT for 450-MHz Input Signal (Dither Off)



$f_{IN1} = 46\text{ MHz}$, $f_{IN2} = 50\text{ MHz}$, IMD3 = 87 dBFS, each tone at -7 dBFS

Figure 42. FFT for Two-Tone Input Signal (-7 dBFS at 46 MHz and 50 MHz)



$f_{IN1} = 46\text{ MHz}$, $f_{IN2} = 50\text{ MHz}$, IMD3 = 88 dBFS, each tone at -36 dBFS

Figure 43. FFT for Two-Tone Input Signal (-36 dBFS at 46 MHz and 50 MHz)

Typical Characteristics: ADC3242 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, $2 \cdot V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.

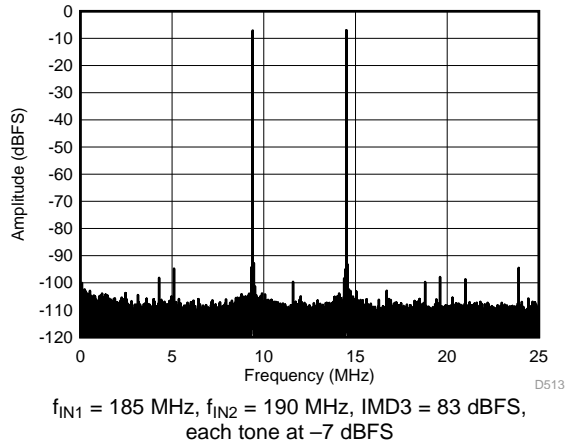


Figure 44. FFT for Two-Tone Input Signal (-7 dBFS at 185 MHz and 190 MHz)

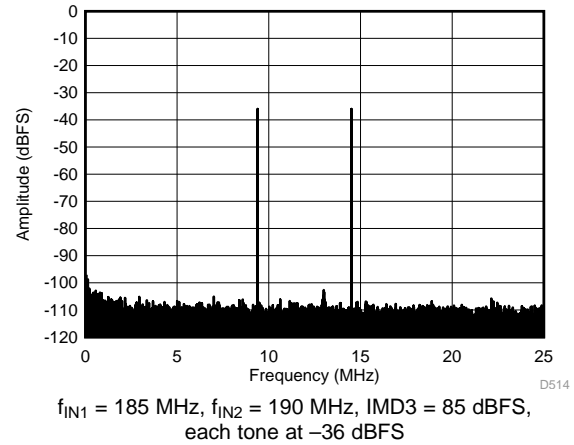


Figure 45. FFT for Two-Tone Input Signal (-36 dBFS at 185 MHz and 190 MHz)

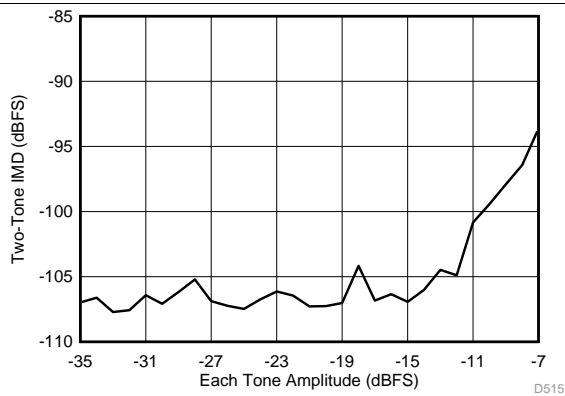


Figure 46. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

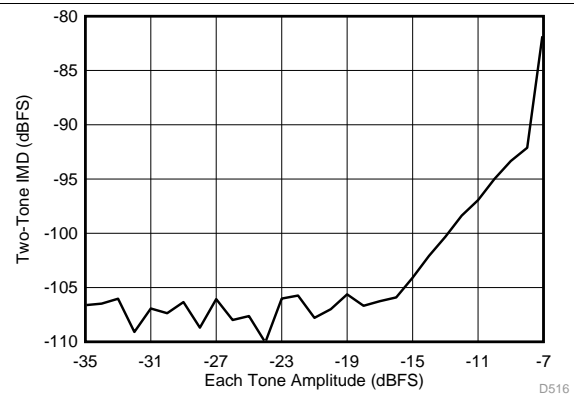


Figure 47. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

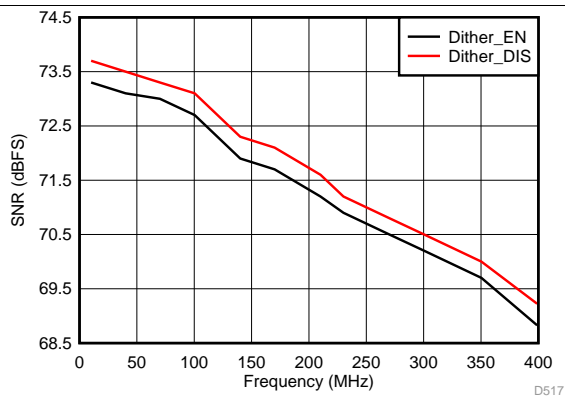


Figure 48. Signal-to-Noise Ratio vs Input Frequency

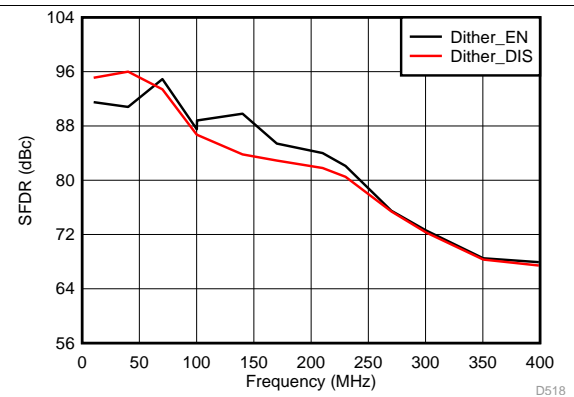
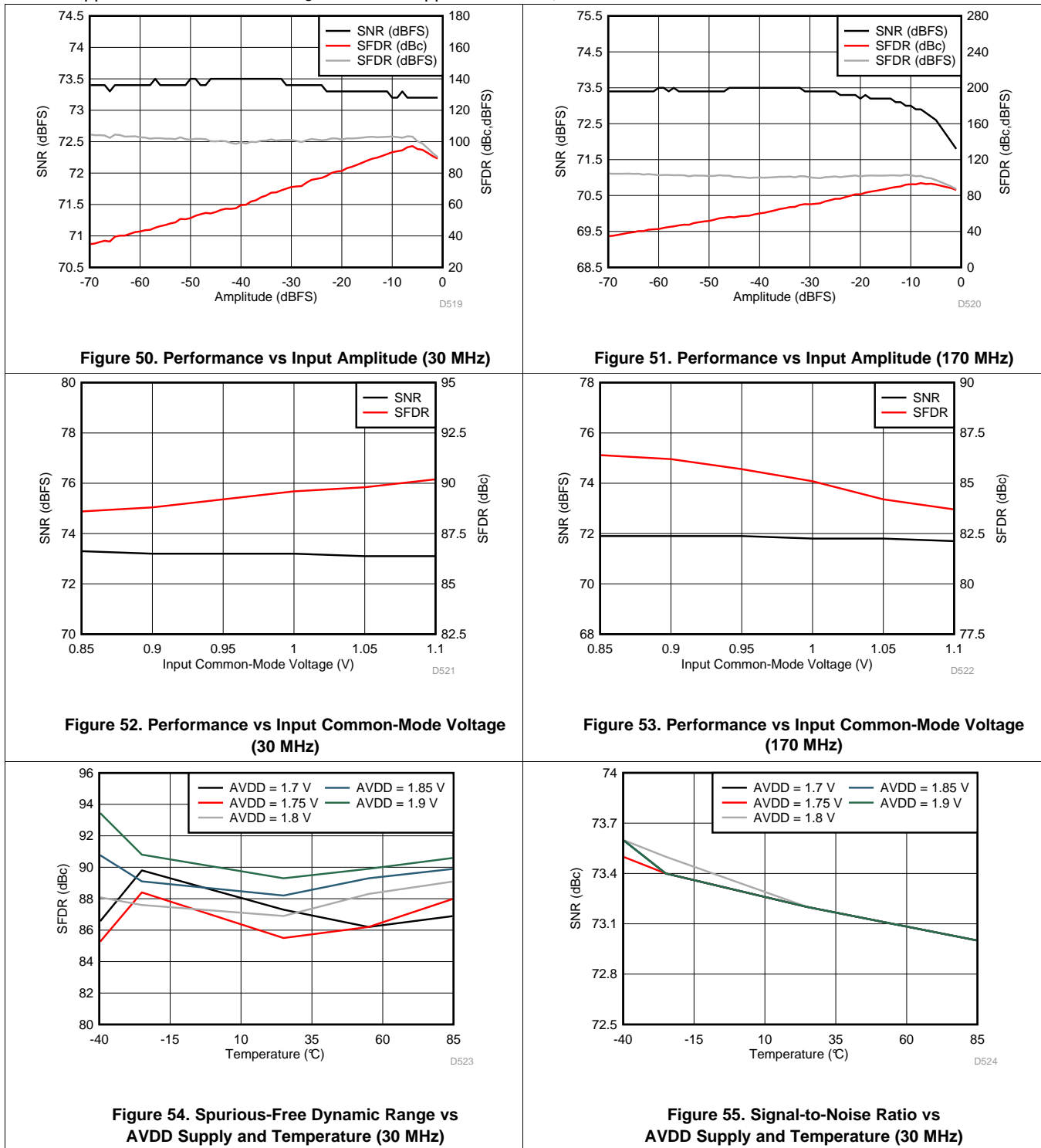


Figure 49. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics: ADC3242 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.



Typical Characteristics: ADC3242 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, $2\cdot V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_S / 2$ when chopper is enabled, unless otherwise noted.

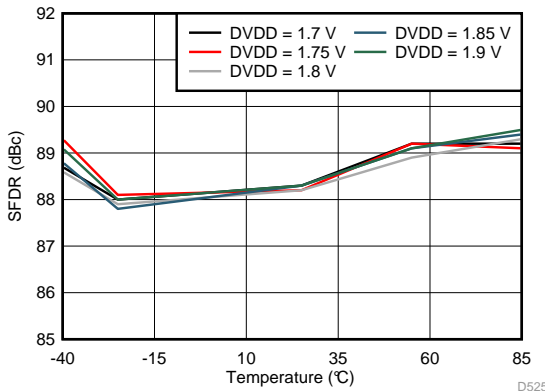


Figure 56. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (30 MHz)

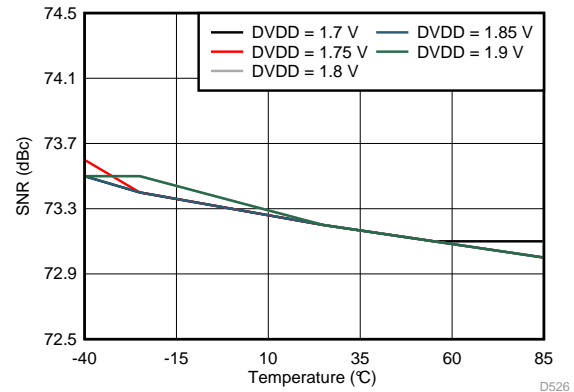


Figure 57. Signal-to-Noise Ratio vs DVDD Supply and Temperature (30 MHz)

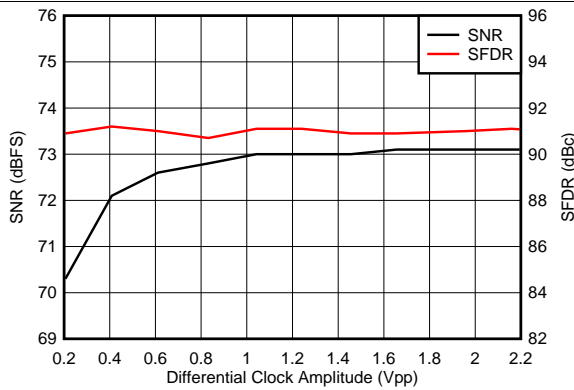


Figure 58. Performance vs Clock Amplitude (40 MHz)

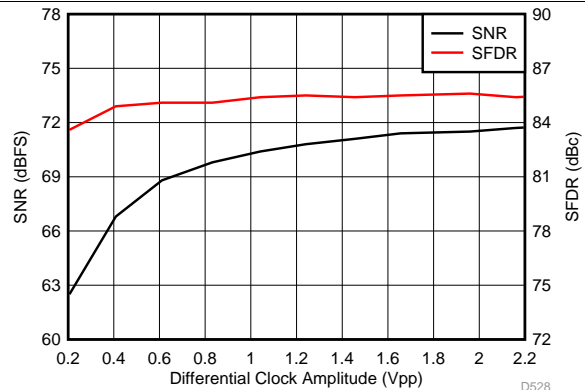


Figure 59. Performance vs Clock Amplitude (150 MHz)

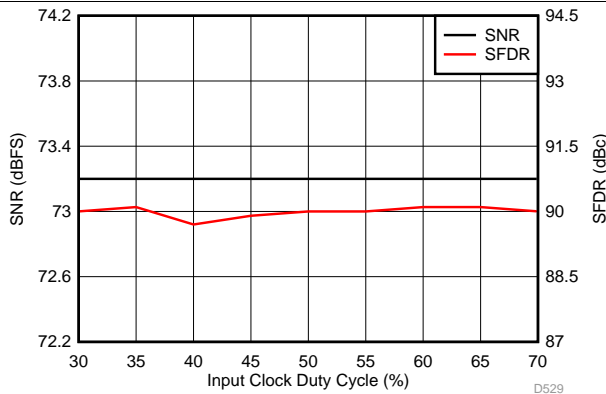


Figure 60. Performance vs Clock Duty Cycle (30 MHz)

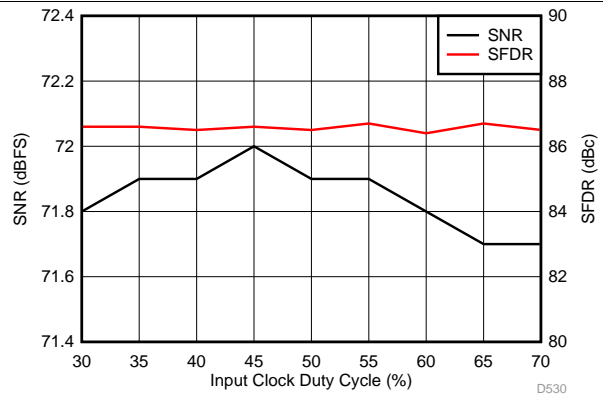
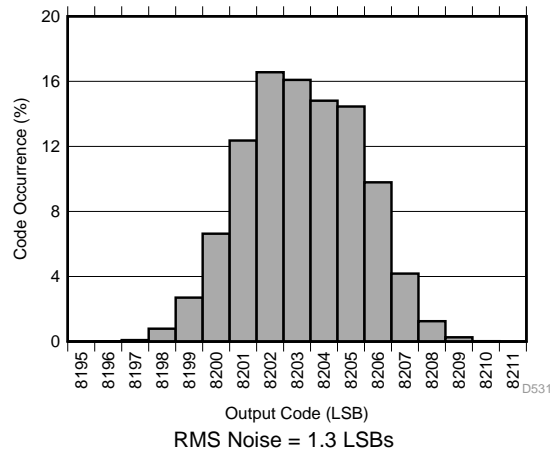


Figure 61. Performance vs Clock Duty Cycle (150 MHz)

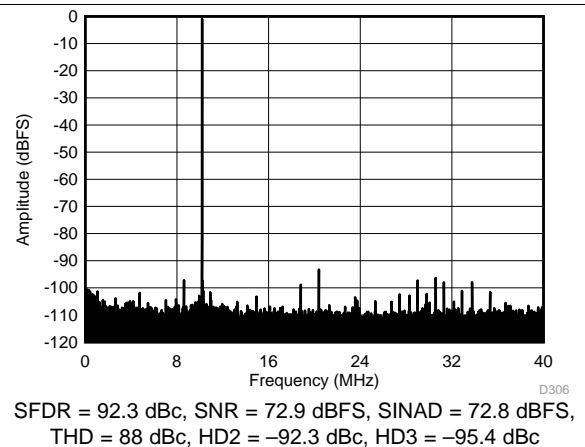
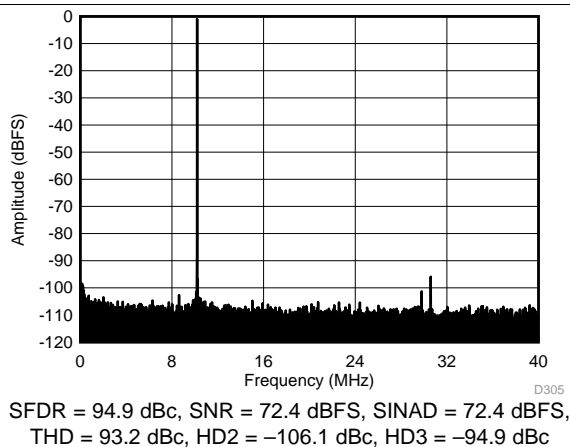
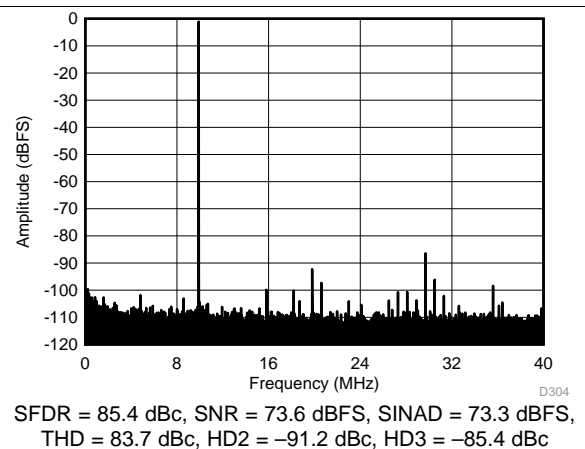
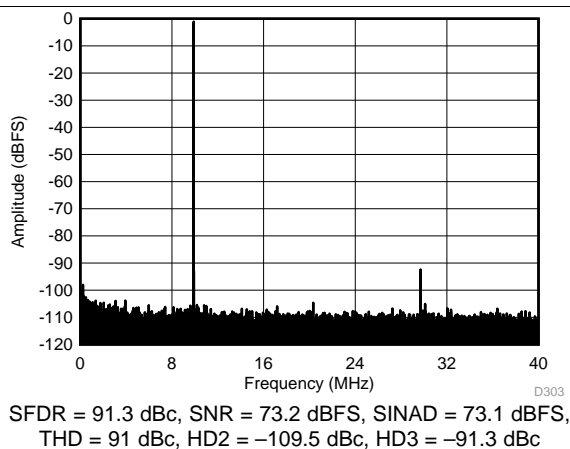
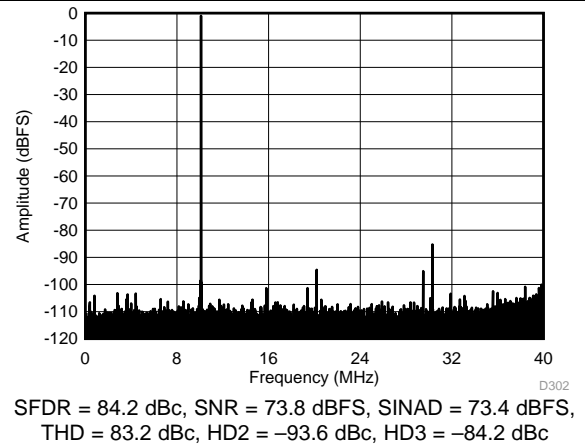
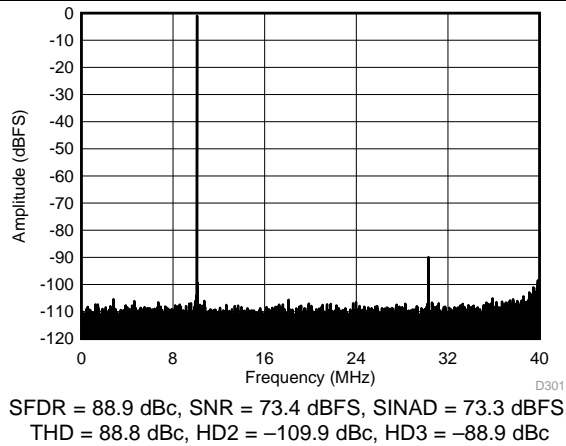
Typical Characteristics: ADC3242 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 50 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, $2-V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_S / 2$ when chopper is enabled, unless otherwise noted.


Figure 62. Idle Channel Histogram

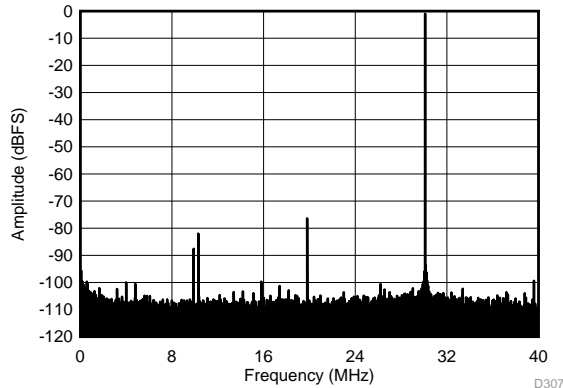
7.17 Typical Characteristics: ADC3243

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_S / 2$ when chopper is enabled, unless otherwise noted.



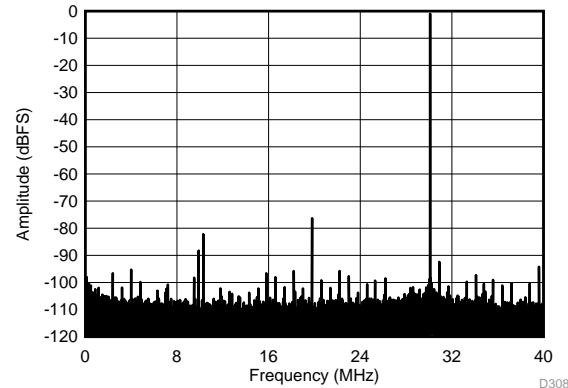
Typical Characteristics: ADC3243 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, $2 \cdot V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.



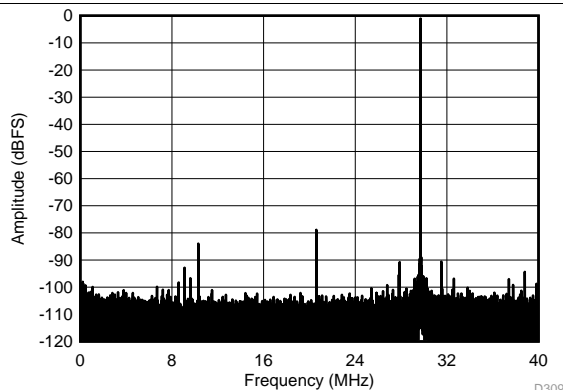
SFDR = 75.4 dBc, SNR = 70.9 dBFS, SINAD = 69.6 dBFS, THD = 74.3 dBc, HD2 = -75.4 dBc, HD3 = -81.0 dBc

Figure 69. FFT for 270-MHz Input Signal (Dither On)



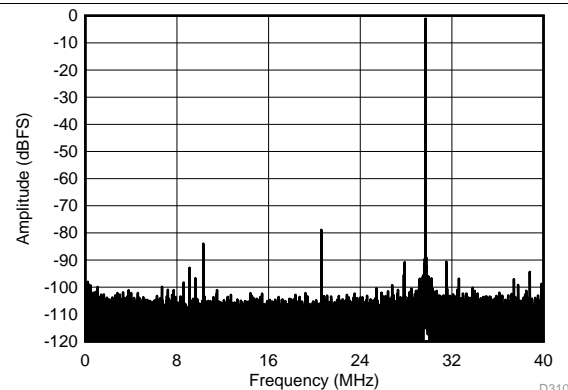
SFDR = 75.4 dBc, SNR = 71.2 dBFS, SINAD = 69.8 dBFS, THD = 74.2 dBc, HD2 = -75.4 dBc, HD3 = -81.2 dBc

Figure 70. FFT for 270-MHz Input Signal (Dither Off)



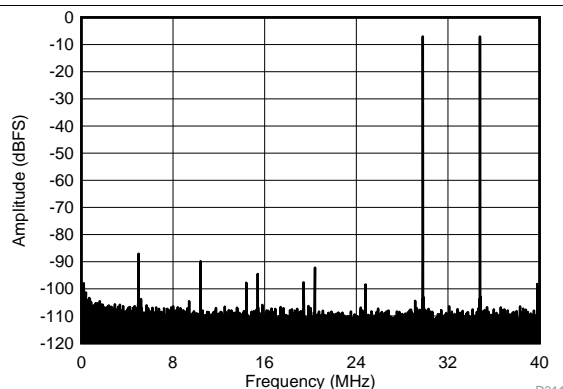
SFDR = 77.8 dBc, SNR = 68.8 dBFS, SINAD = 68.3 dBFS, THD = 77.5 dBc, HD2 = -77.8 dBc, HD3 = -91.8 dBc

Figure 71. FFT for 450-MHz Input Signal (Dither On)



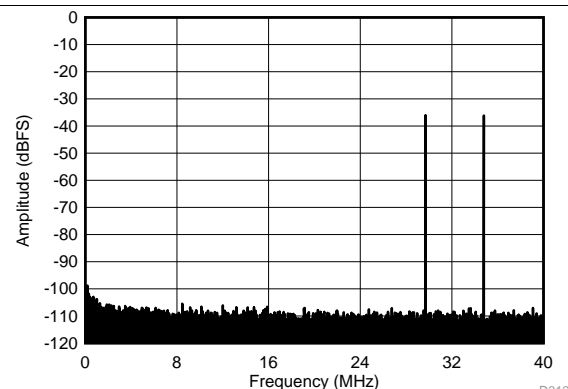
SFDR = 77.8 dBc, SNR = 68.8 dBFS, SINAD = 68.3 dBFS, THD = 77.5 dBc, HD2 = -77.8 dBc, HD3 = -91.8 dBc

Figure 72. FFT for 450-MHz Input Signal (Dither Off)



$f_{IN1} = 46 \text{ MHz}$, $f_{IN2} = 50 \text{ MHz}$, IMD3 = 87 dBFS, each tone at -7 dBFS

Figure 73. FFT for Two-Tone Input Signal (-7 dBFS at 46 MHz and 50 MHz)

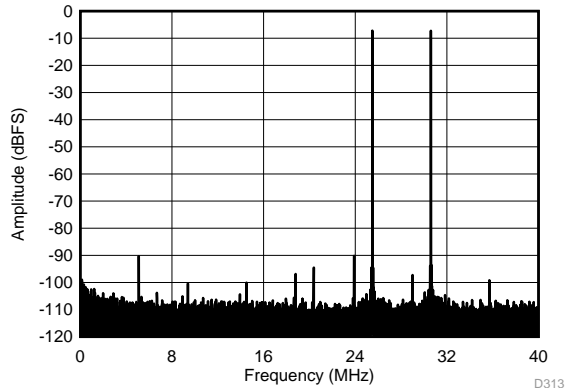


$f_{IN1} = 46 \text{ MHz}$, $f_{IN2} = 50 \text{ MHz}$, IMD3 = 92.8 dBFS, each tone at -36 dBFS

Figure 74. FFT for Two-Tone Input Signal (-36 dBFS at 46 MHz and 50 MHz)

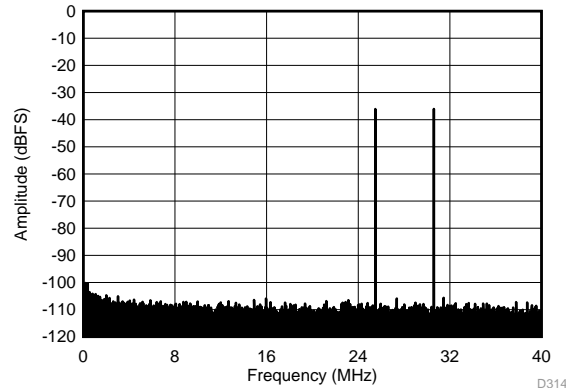
Typical Characteristics: ADC3243 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.



$f_{IN1} = 185 \text{ MHz}$, $f_{IN2} = 190 \text{ MHz}$, $\text{IMD3} = 78.8 \text{ dBFS}$, each tone at -7 dBFS

Figure 75. FFT FOR Two-Tone Input Signal (-7 dBFS at 185 MHz and 190 MHz)



$f_{IN1} = 185 \text{ MHz}$, $f_{IN2} = 190 \text{ MHz}$, $\text{IMD3} = 91 \text{ dBFS}$, each tone at -36 dBFS

Figure 76. FFT FOR Two-Tone Input Signal (-36 dBFS at 185 MHz and 190 MHz)

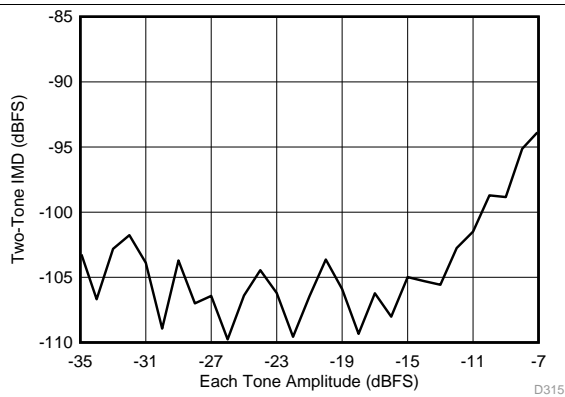


Figure 77. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

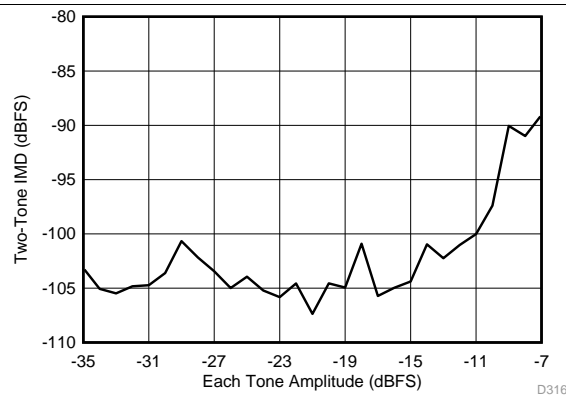


Figure 78. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

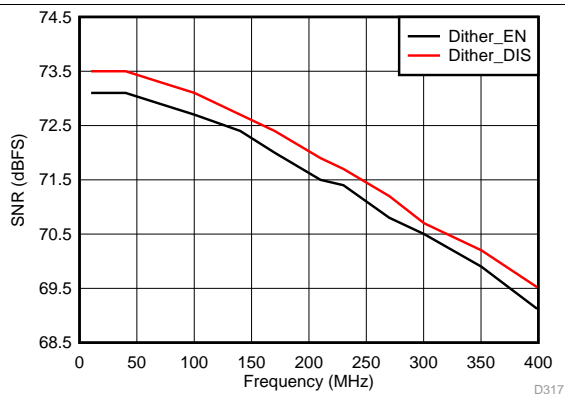


Figure 79. Signal-to-Noise Ratio vs Input Frequency

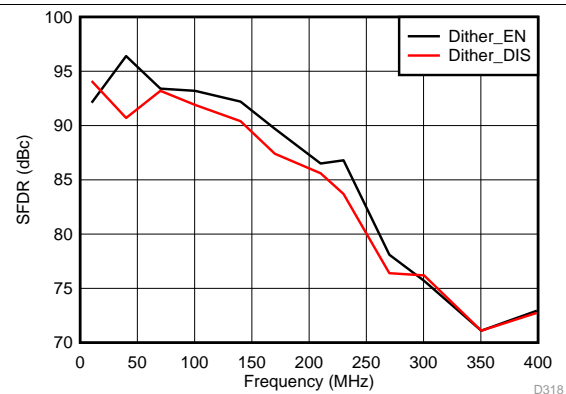


Figure 80. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics: ADC3243 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, $2 \cdot V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.

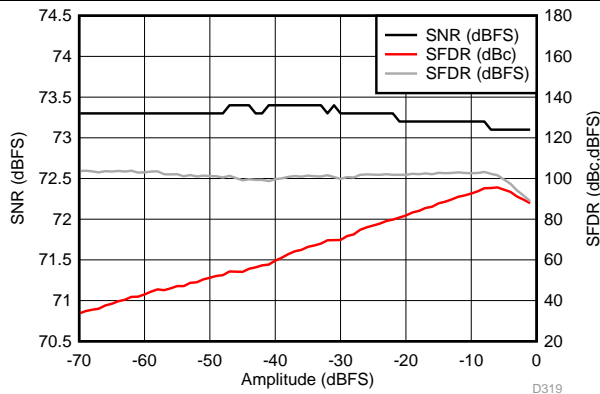


Figure 81. Performance vs Input Amplitude (30 MHz)

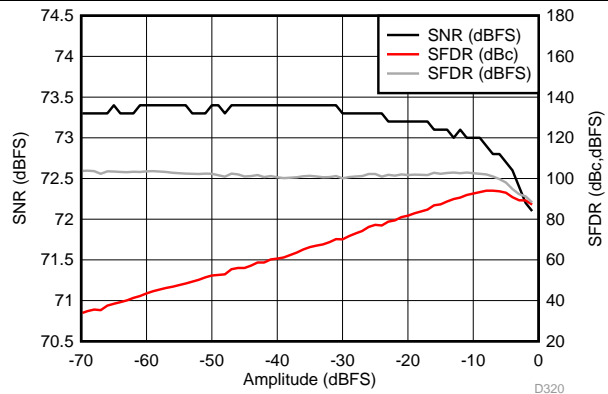


Figure 82. Performance vs Input Amplitude (170 MHz)

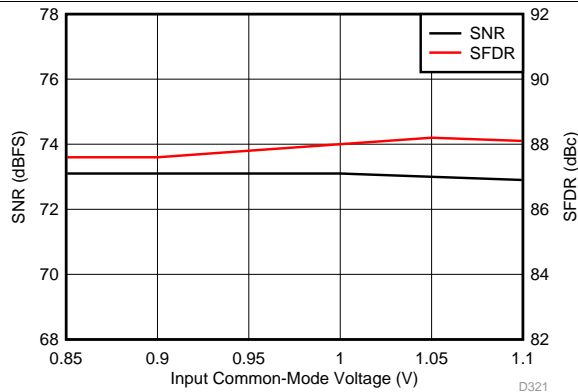


Figure 83. Performance vs Input Common-Mode Voltage (30 MHz)

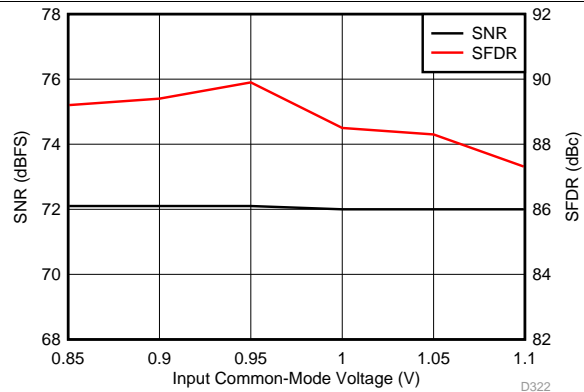


Figure 84. Performance vs Input Common-Mode Voltage (170 MHz)

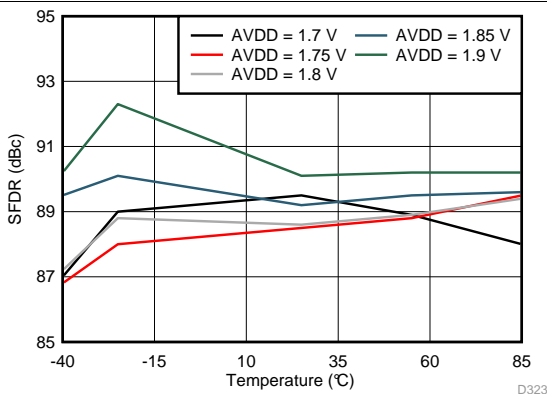


Figure 85. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (170 MHz)

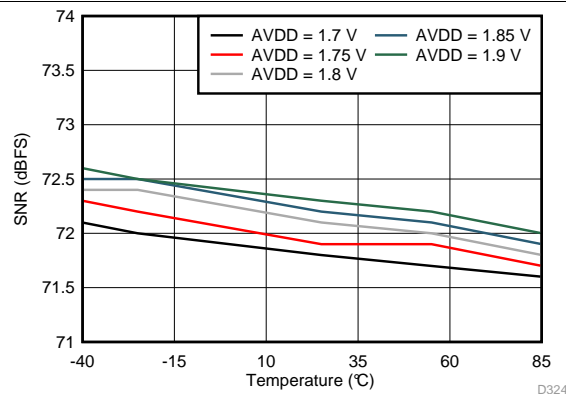


Figure 86. Signal-to-Noise Ratio vs AVDD Supply and Temperature (170 MHz)

Typical Characteristics: ADC3243 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, 2- V_{pp} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.

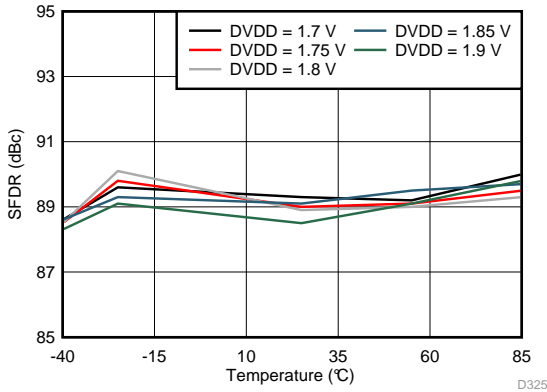


Figure 87. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (170 MHz)

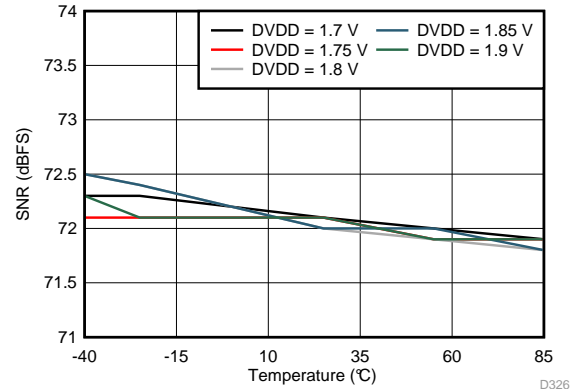


Figure 88. Signal-to-Noise Ratio vs DVDD Supply and Temperature (170 MHz)

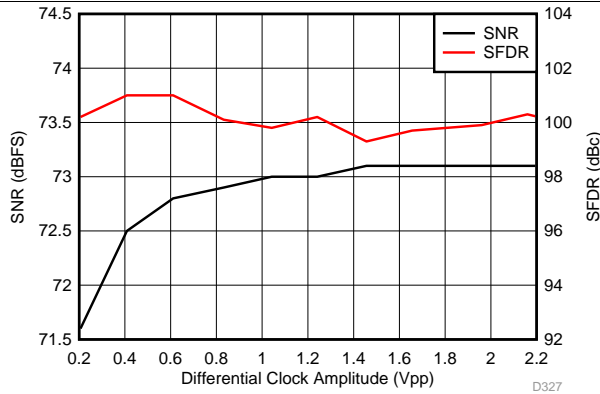


Figure 89. Performance vs Clock Amplitude (40 MHz)

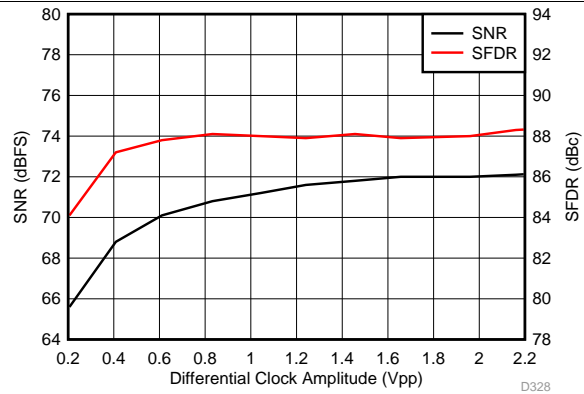


Figure 90. Performance vs Clock Amplitude (150 MHz)

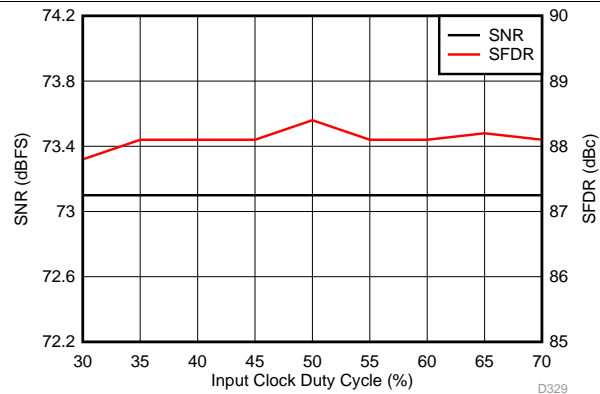


Figure 91. Performance vs Clock Duty Cycle (30 MHz)

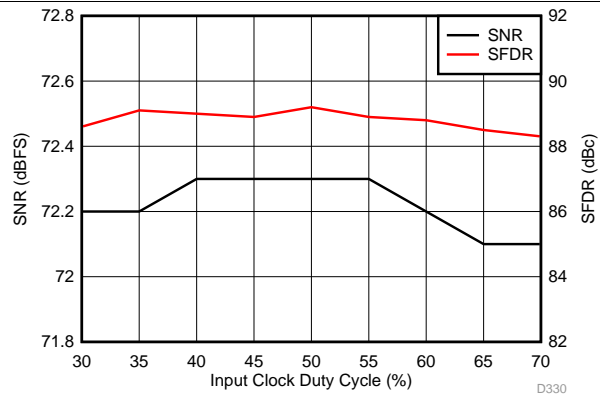
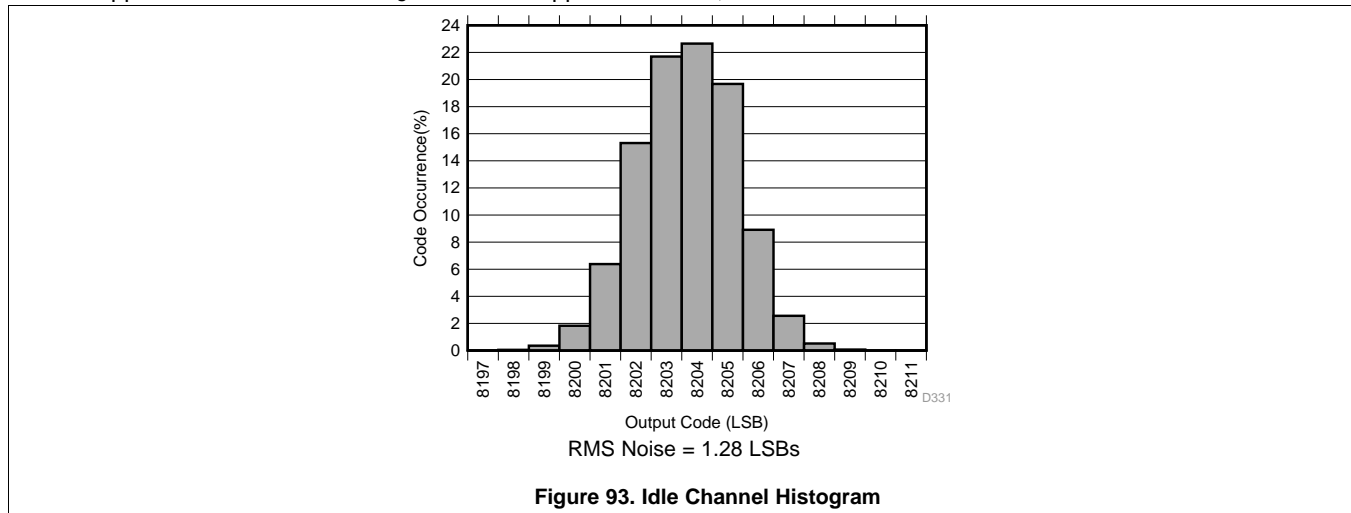


Figure 92. Performance vs Clock Duty Cycle (150 MHz)

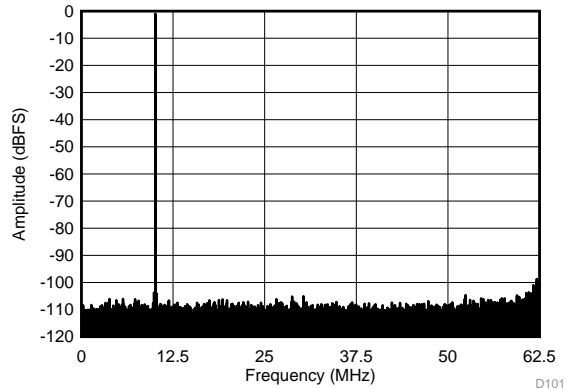
Typical Characteristics: ADC3243 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 80 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_S / 2$ when chopper is enabled, unless otherwise noted.



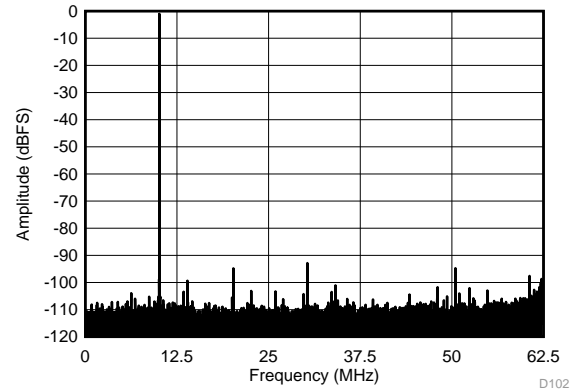
7.18 Typical Characteristics: ADC3244

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.



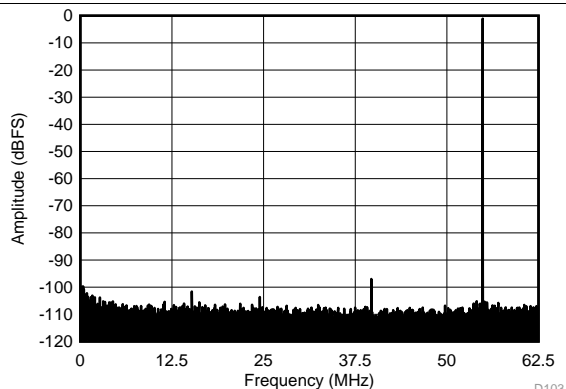
SFDR = 102.6 dBc, SNR = 72.9 dBFS, SINAD = 72.8 dBFS, THD = 99.8 dBc, HD2 = -108.6 dBc , HD3 = -104.0 dBc

Figure 94. FFT for 10-MHz Input Signal (Chopper On, Dither On)



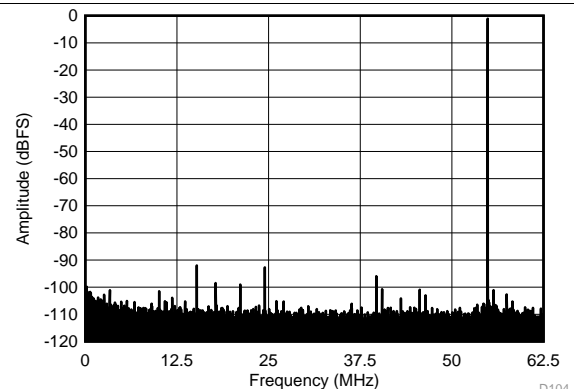
SFDR = 91.8 dBc, SNR = 73.5 dBFS, SINAD = 73.4 dBFS, THD = 87.3 dBc, HD2 = -93.8 dBc , HD3 = -91.8 dBc

Figure 95. FFT for 10-MHz Input Signal (Chopper On, Dither Off)



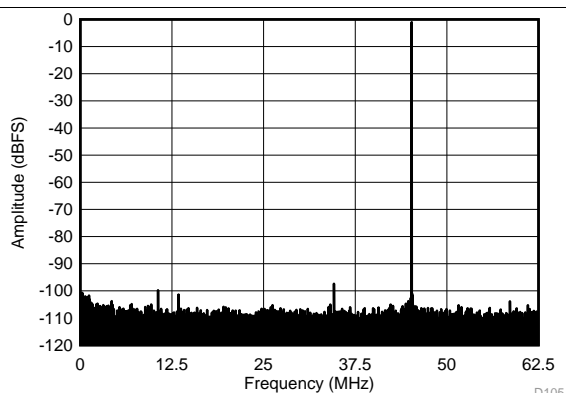
SFDR = 95.9 dBc, SNR = 72.7 dBFS, SINAD = 72.7 dBFS, THD = 93.6 dBc, HD2 = -100.6 dBc , HD3 = -95.9 dBc

Figure 96. FFT for 70-MHz Input Signal (Dither On)



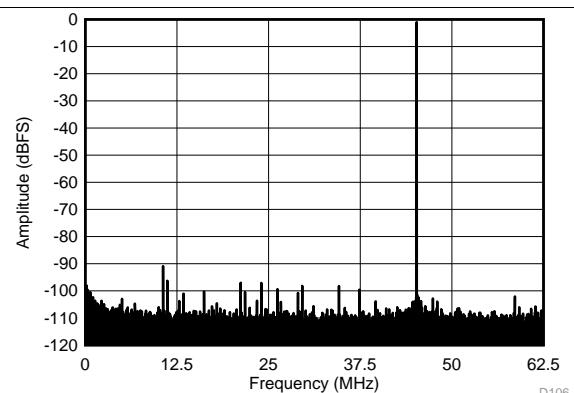
SFDR = 90.9 dBc, SNR = 73.3 dBFS, SINAD = 73.1 dBFS, THD = 87 dBc, HD2 = -90.9 dBc , HD3 = -94.9 dBc

Figure 97. FFT for 70-MHz Input Signal (Dither Off)



SFDR = 96.4 dBc, SNR = 72.1 dBFS, SINAD = 72.0 dBFS, THD = 92.6 dBc, HD2 = -96.4 dBc , HD3 = -98.8 dBc

Figure 98. FFT for 170-MHz Input Signal (Dither On)

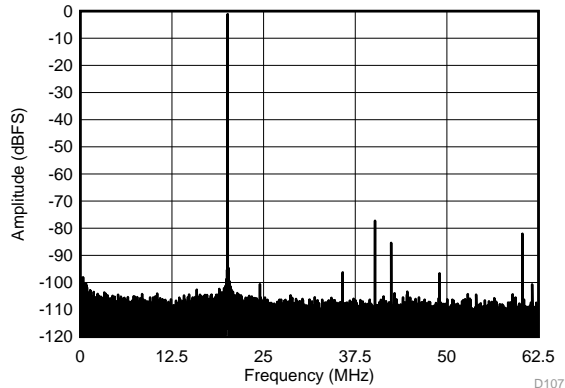


SFDR = 89.9 dBc, SNR = 72.8 dBFS, SINAD = 72.6 dBFS, THD = 87.1 dBc, HD2 = -97.2 dBc , HD3 = -89.9 dBc

Figure 99. FFT for 170-MHz Input Signal (Dither Off)

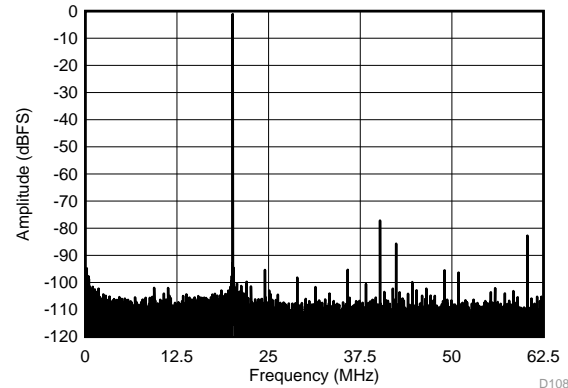
Typical Characteristics: ADC3244 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1 dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.



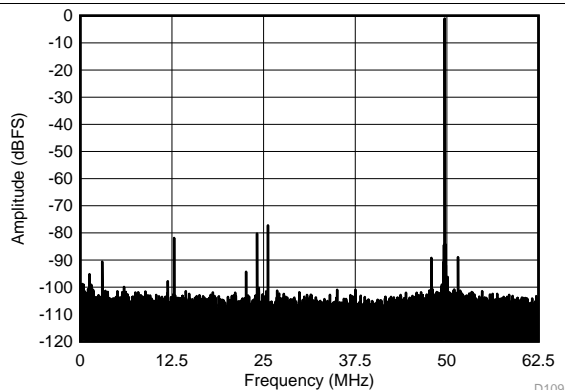
SFDR = 76.1 dBc, SNR = 70.8 dBFS, SINAD = 69.8 dBFS, THD = 74.8 dBc, HD2 = -76.1 dBc , HD3 = -80.9 dBc

Figure 100. FFT for 270-MHz Input Signal (Dither On)



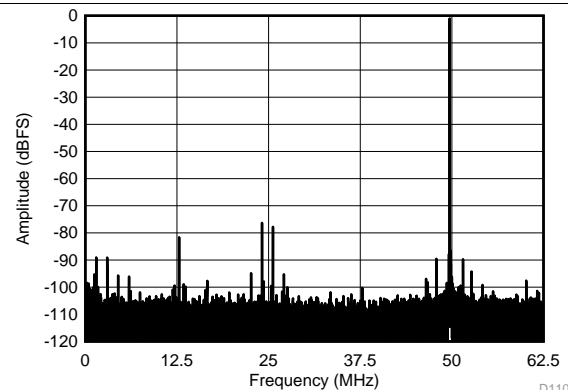
SFDR = 76.1 dBc, SNR = 71.2 dBFS, SINAD = 70.2 dBFS, THD = 74.9 dBc, HD2 = -76.1 dBc , HD3 = -81.6 dBc

Figure 101. FFT for 270-MHz Input Signal (Dither Off)



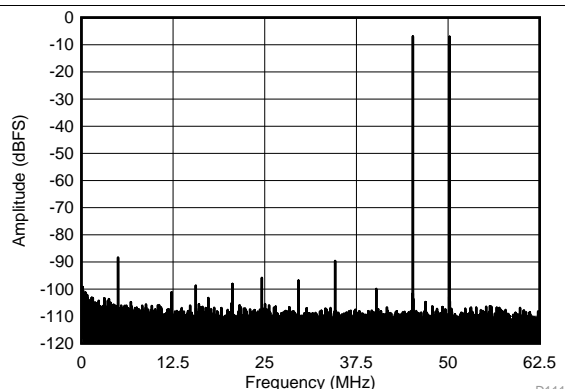
SFDR = 76.2 dBc, SNR = 68.3 dBFS, SINAD = 67.5 dBFS, THD = 74.3 dBc, HD2 = -76.2 dBc , HD3 = -79.2 dBc

Figure 102. FFT for 450-MHz Input Signal (Dither On)



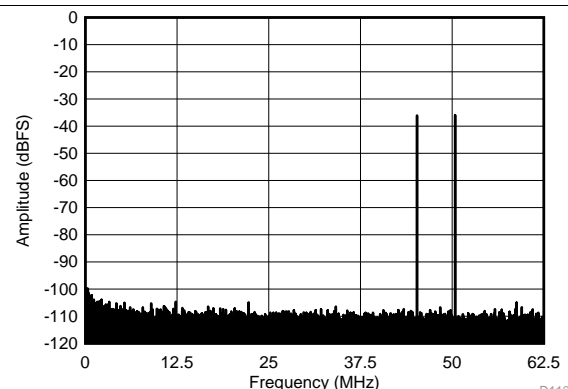
SFDR = 75.3 dBc, SNR = 69.1 dBFS, SINAD = 67.8 dBFS, THD = 72.7 dBc, HD2 = -76.7 dBc , HD3 = -75.3 dBc

Figure 103. FFT for 450-MHz Input Signal (Dither Off)



$f_{IN1} = 46\text{ MHz}$, $f_{IN2} = 50\text{ MHz}$, IMD3 = 88.3 dBFS, each tone at -7 dBFS

Figure 104. FFT for Two-Tone Input Signal (-7 dBFS at 46 MHz and 50 MHz)

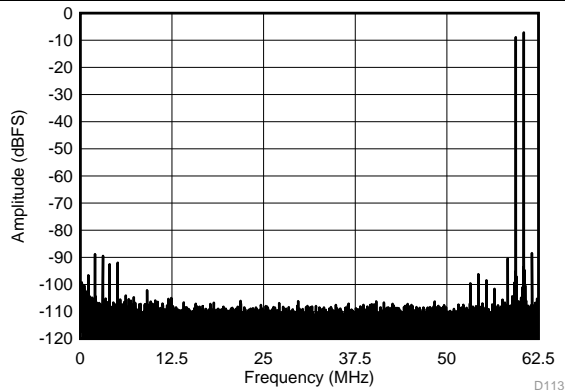


$f_{IN1} = 46\text{ MHz}$, $f_{IN2} = 50\text{ MHz}$, IMD3 = 90.8 dBFS, each tone at -36 dBFS

Figure 105. FFT for Two-Tone Input Signal (-36 dBFS at 46 MHz and 50 MHz)

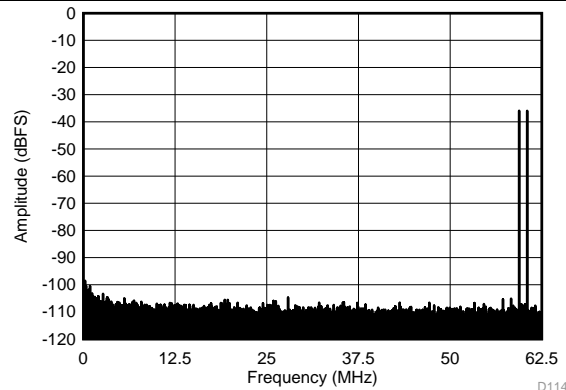
Typical Characteristics: ADC3244 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1 dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.



$f_{IN1} = 185\text{ MHz}$, $f_{IN2} = 190\text{ MHz}$, $\text{IMD3} = 86.4\text{ dBFS}$, each tone at -7 dBFS

Figure 106. FFT for Two-Tone Input Signal (-7 dBFS at 185 MHz and 190 MHz)



$f_{IN1} = 185\text{ MHz}$, $f_{IN2} = 190\text{ MHz}$, $\text{IMD3} = 87.28\text{ dBFS}$, each tone at -36 dBFS

Figure 107. FFT for Two-Tone Input Signal (-36 dBFS at 185 MHz and 190 MHz)

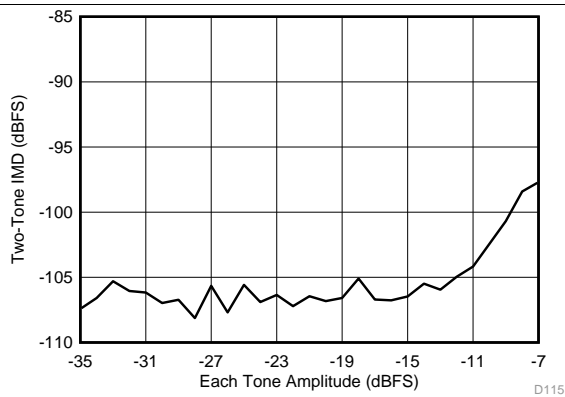


Figure 108. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

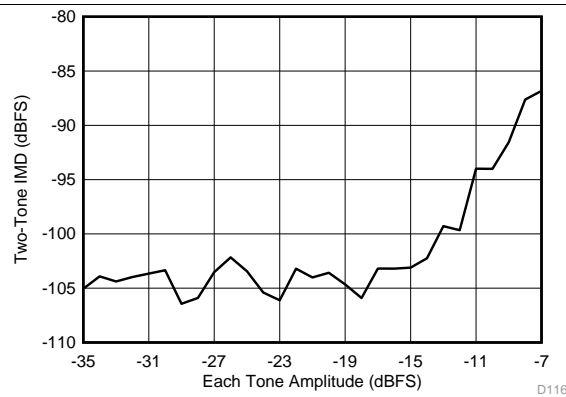


Figure 109. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

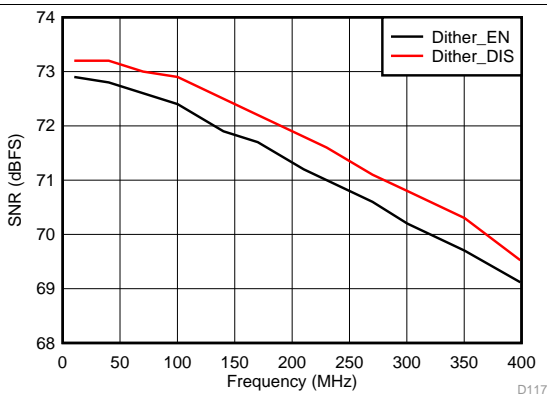


Figure 110. Signal-to-Noise Ratio vs Input Frequency

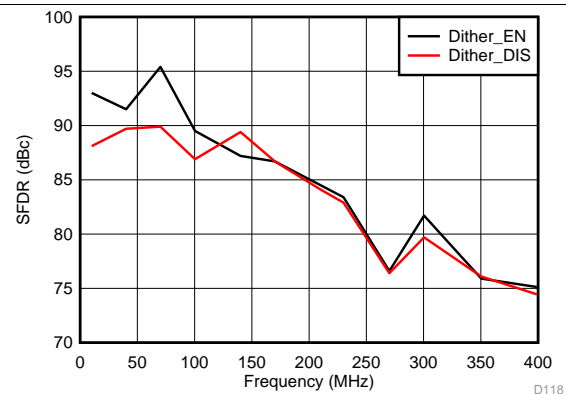


Figure 111. Spurious-Free Dynamic Range vs Input Frequency

Typical Characteristics: ADC3244 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1 dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.

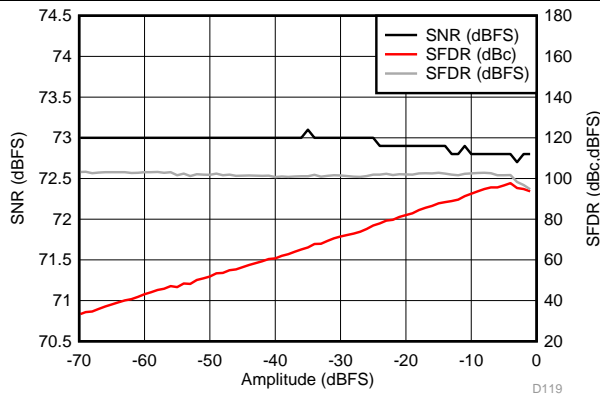


Figure 112. Performance vs Input Amplitude (30 MHz)

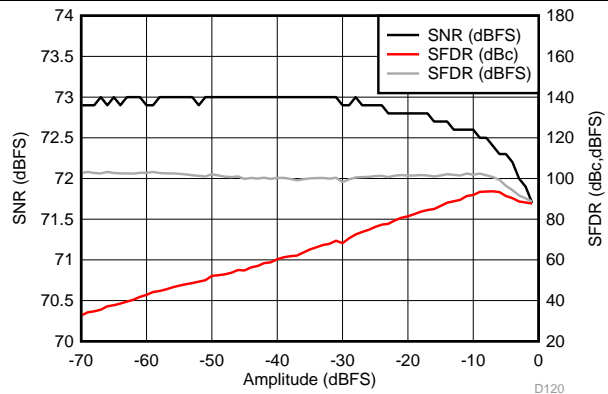


Figure 113. Performance vs Input Amplitude (170 MHz)

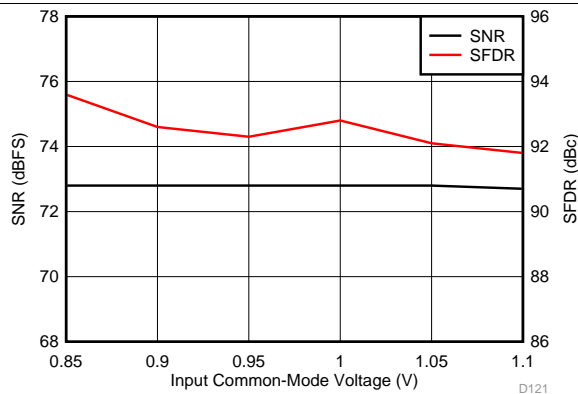


Figure 114. Performance vs Input Common-Mode Voltage (30 MHz)

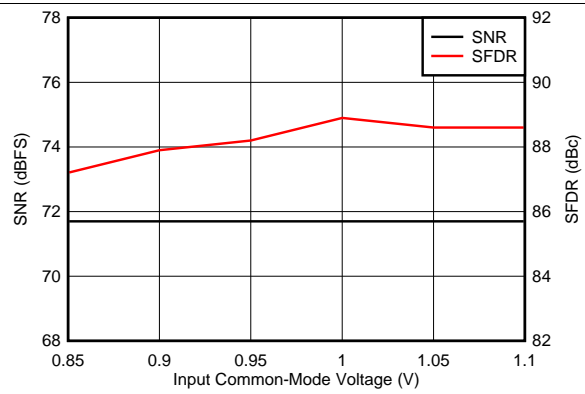


Figure 115. Performance vs Input Common-Mode Voltage (170 MHz)

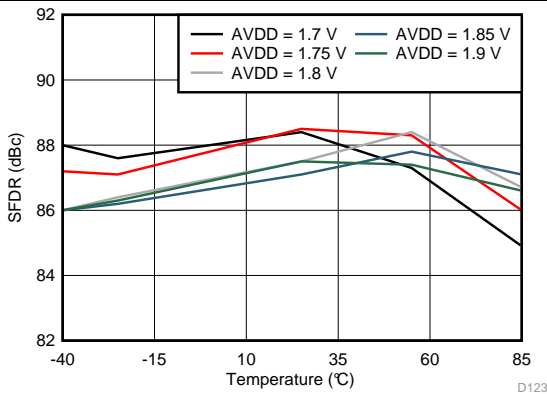


Figure 116. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (170 MHz)

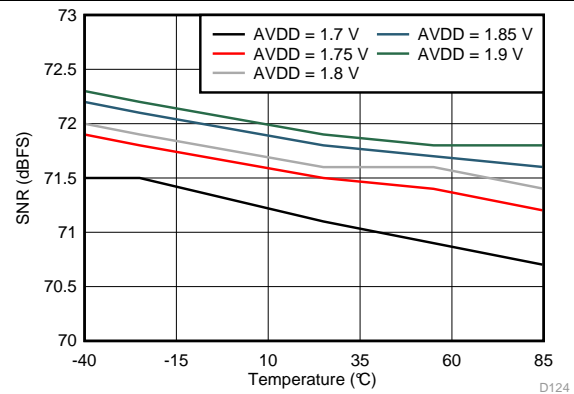


Figure 117. Signal-to-Noise Ratio vs AVDD Supply and Temperature (170 MHz)

Typical Characteristics: ADC3244 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, -1-dBFS differential input, $2\cdot V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_S / 2$ when chopper is enabled, unless otherwise noted.

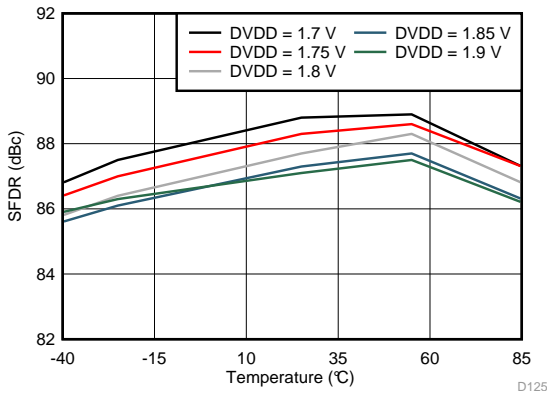


Figure 118. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (170 MHz)

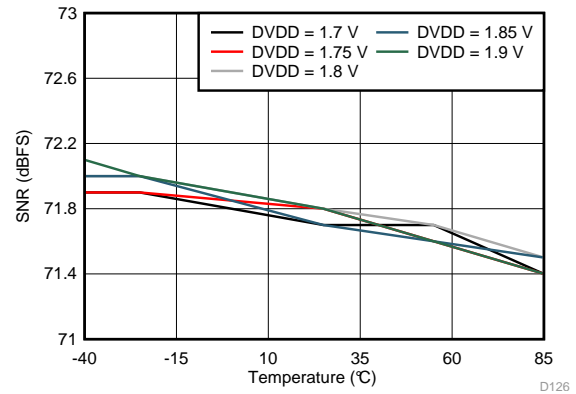


Figure 119. Signal-to-Noise Ratio vs DVDD Supply and Temperature (170 MHz)

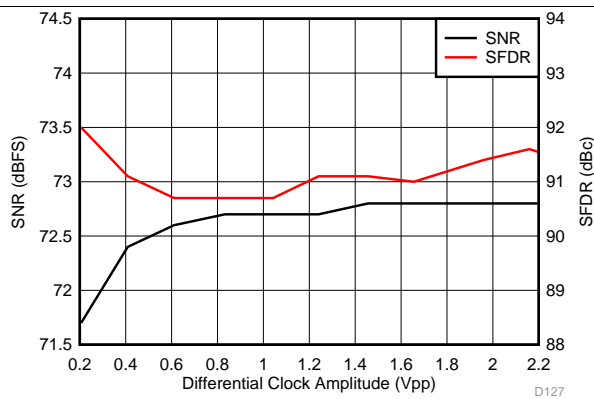


Figure 120. Performance vs Clock Amplitude (40 MHz)

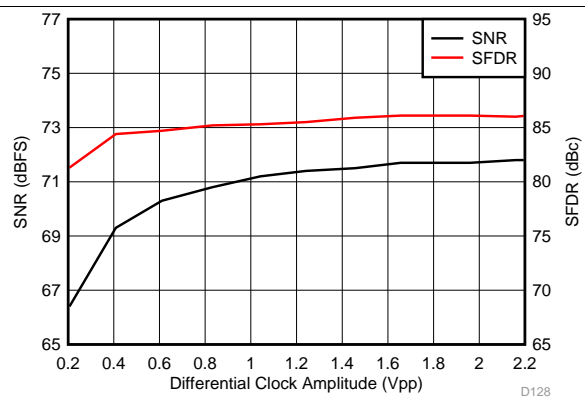


Figure 121. Performance vs Clock Amplitude (150 MHz)

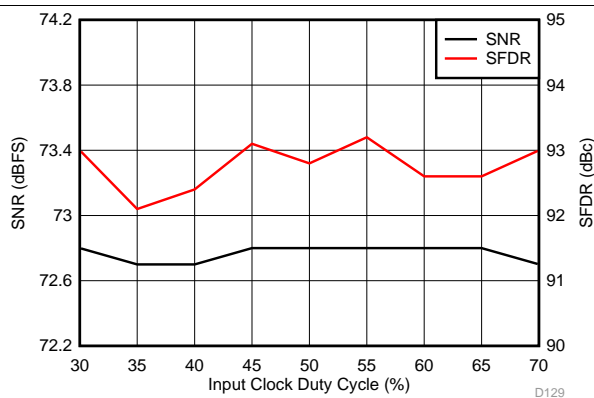


Figure 122. Performance vs Clock Duty Cycle (30 MHz)

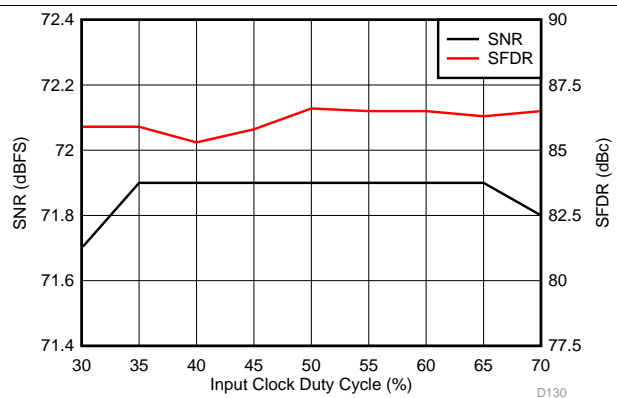
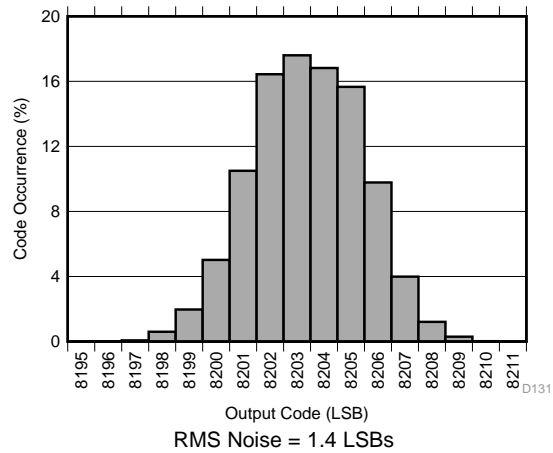


Figure 123. Performance vs Clock Duty Cycle (150 MHz)

Typical Characteristics: ADC3244 (continued)

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AVDD = 1.8\text{ V}$, $DVDD = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_S / 2$ when chopper is enabled, unless otherwise noted.


Figure 124. Idle Channel Histogram

7.19 Typical Characteristics: Common

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AV_{DD} = 1.8\text{ V}$, $DV_{DD} = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when chopper is enabled, unless otherwise noted.

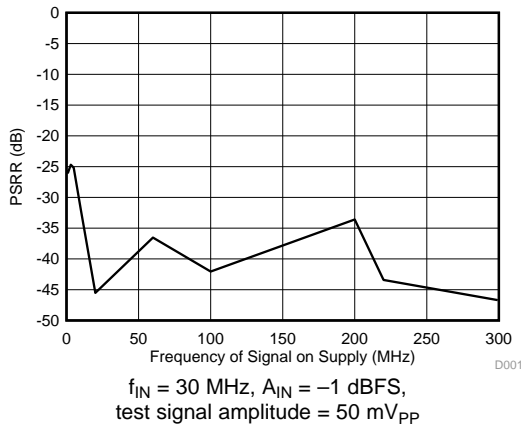


Figure 125. Power-Supply Rejection Ratio vs Test Signal Frequency

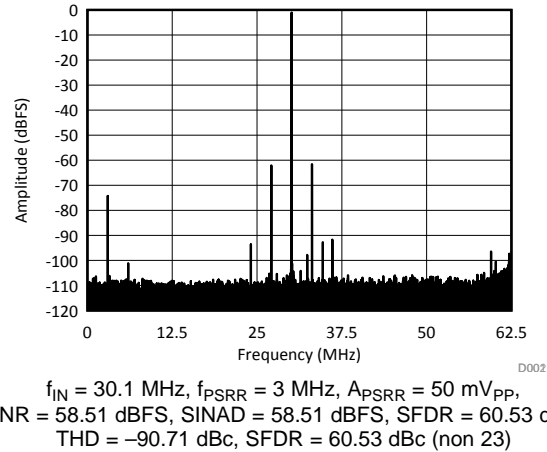


Figure 126. Power-Supply Rejection Ratio Spectrum

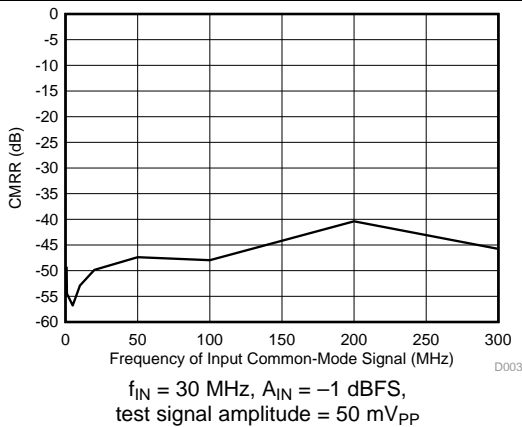


Figure 127. Common-Mode Rejection Ratio vs Test Signal Frequency

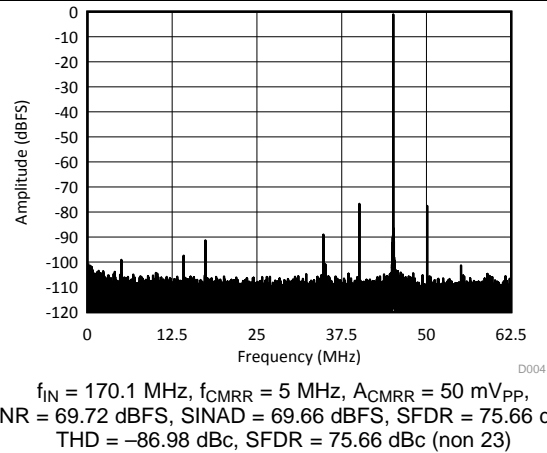


Figure 128. Common-Mode Rejection Ratio Spectrum

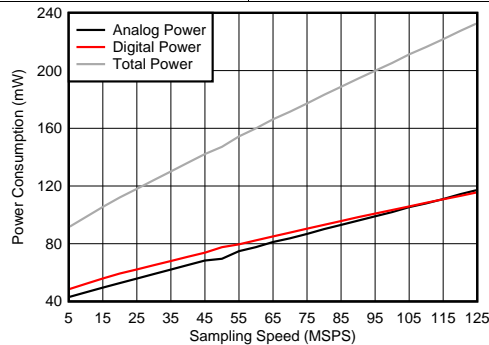


Figure 129. Power vs Sampling Frequency (One-Wire Mode)

7.20 Typical Characteristics: Contour

Typical values are at $T_A = 25^\circ\text{C}$, ADC sampling rate = 125 MSPS, 50% clock duty cycle, $AVDD = 1.8\text{ V}$, $DVDD = 1.8\text{ V}$, -1-dBFS differential input, $2\text{-}V_{PP}$ full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from $f_s / 2$ when is chopper enabled, unless otherwise noted.

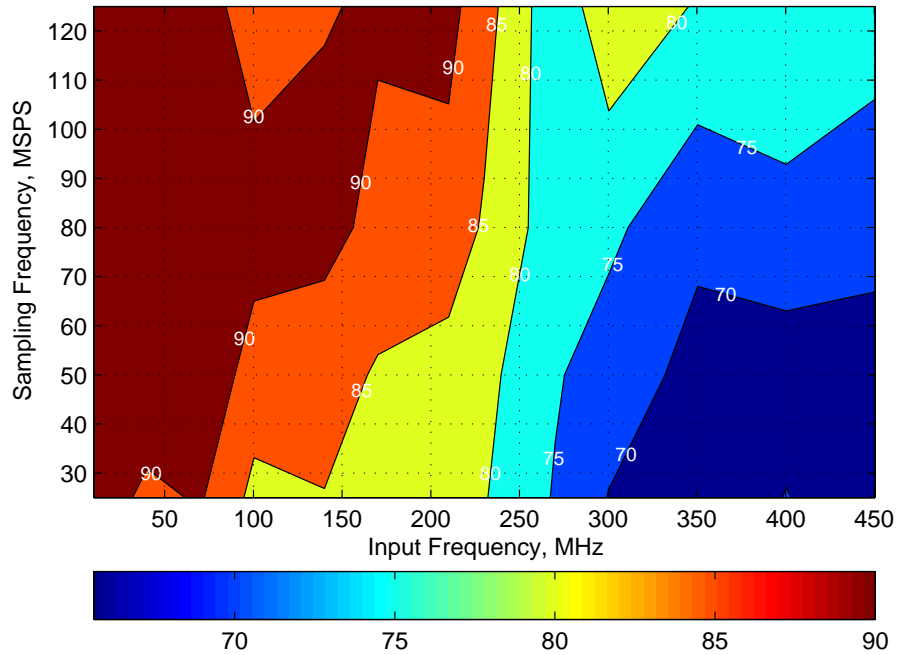


Figure 130. Spurious-Free Dynamic Range (SFDR)

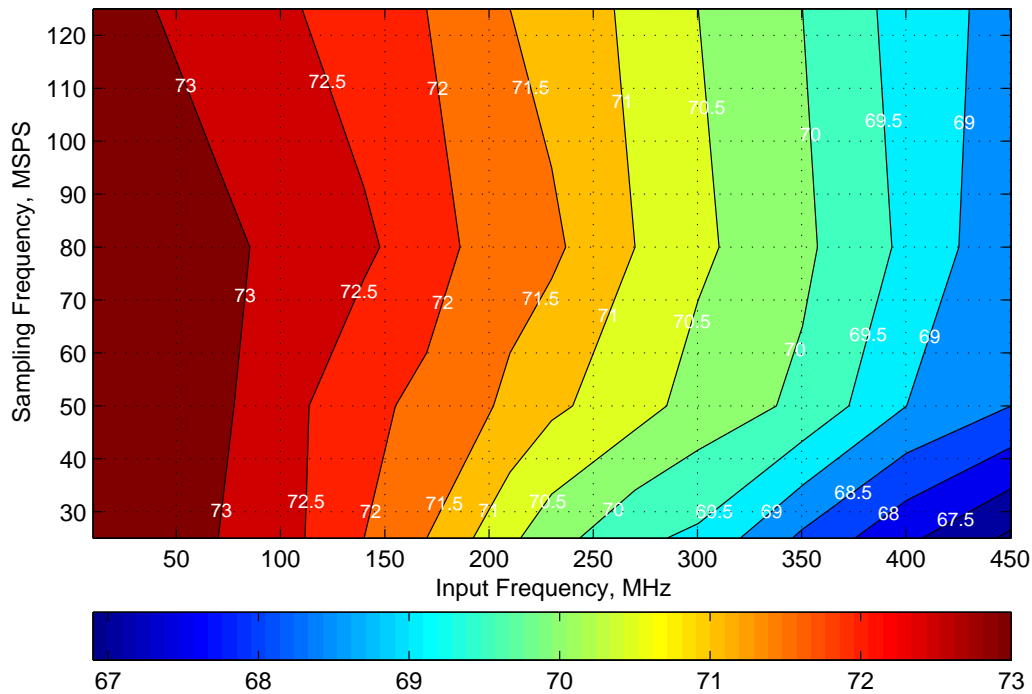
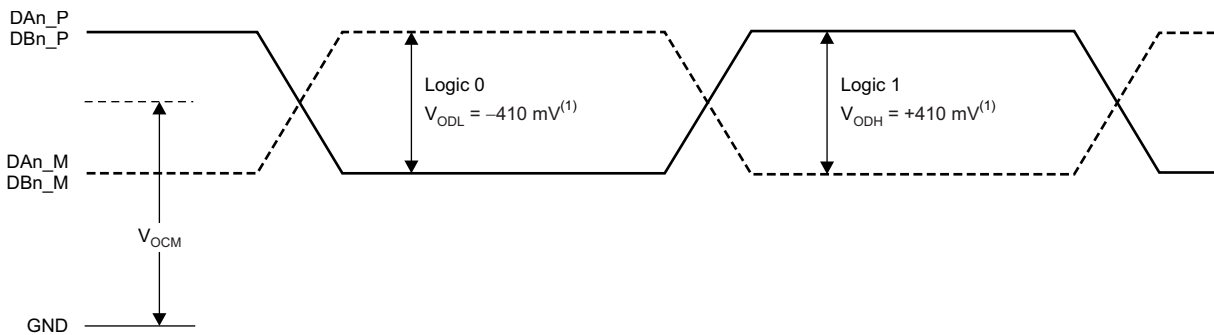


Figure 131. Signal-to-Noise Ratio (SNR)

8 Parameter Measurement Information

8.1 Timing Diagrams



(1) With an external 100-Ω termination.

Figure 132. Serial LVDS Output Voltage Levels

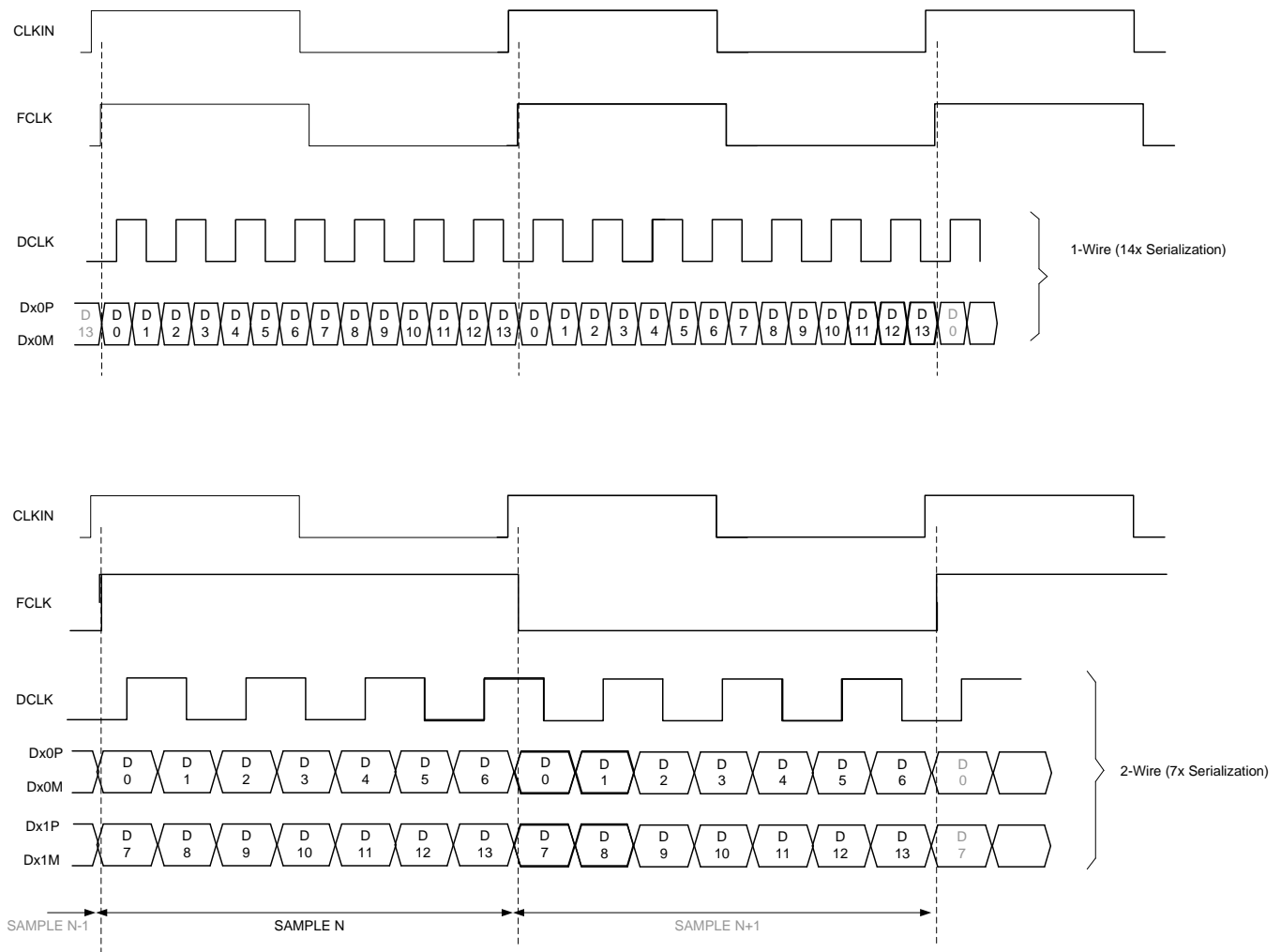


Figure 133. Output Timing Diagram

Timing Diagrams (continued)

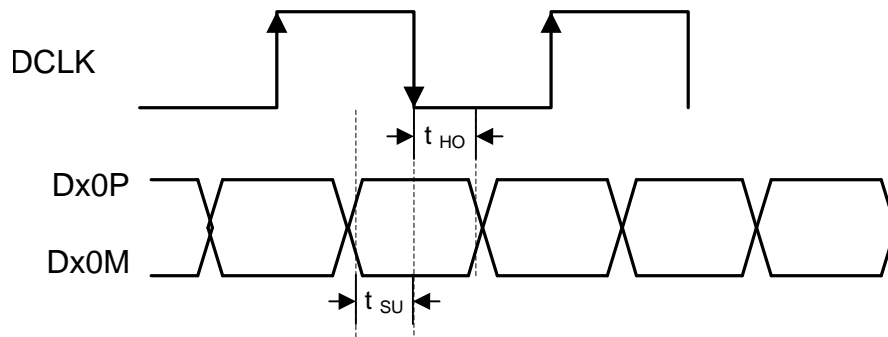
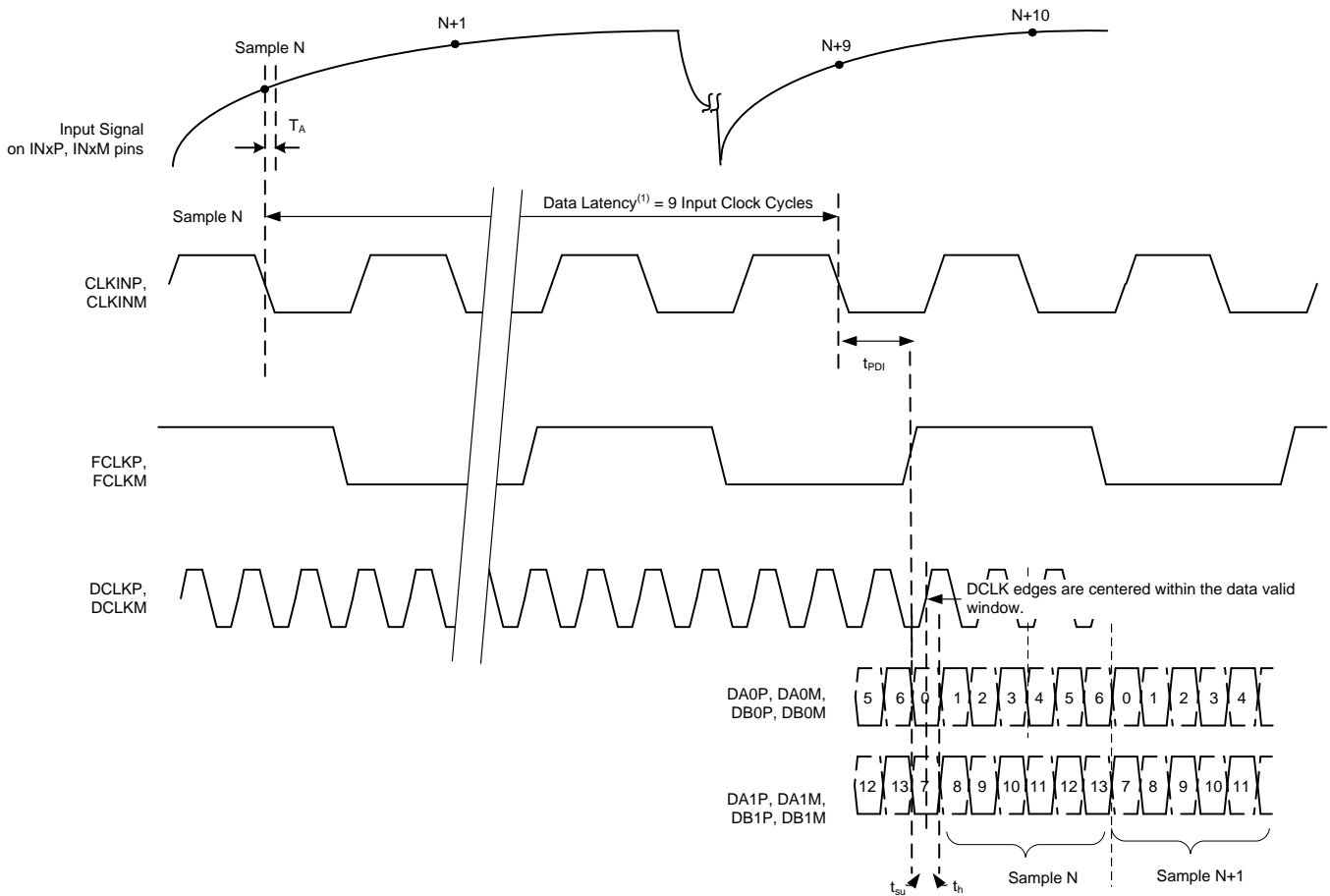


Figure 134. Setup and Hold Time



(1) Overall latency = data latency + t_{PD} .

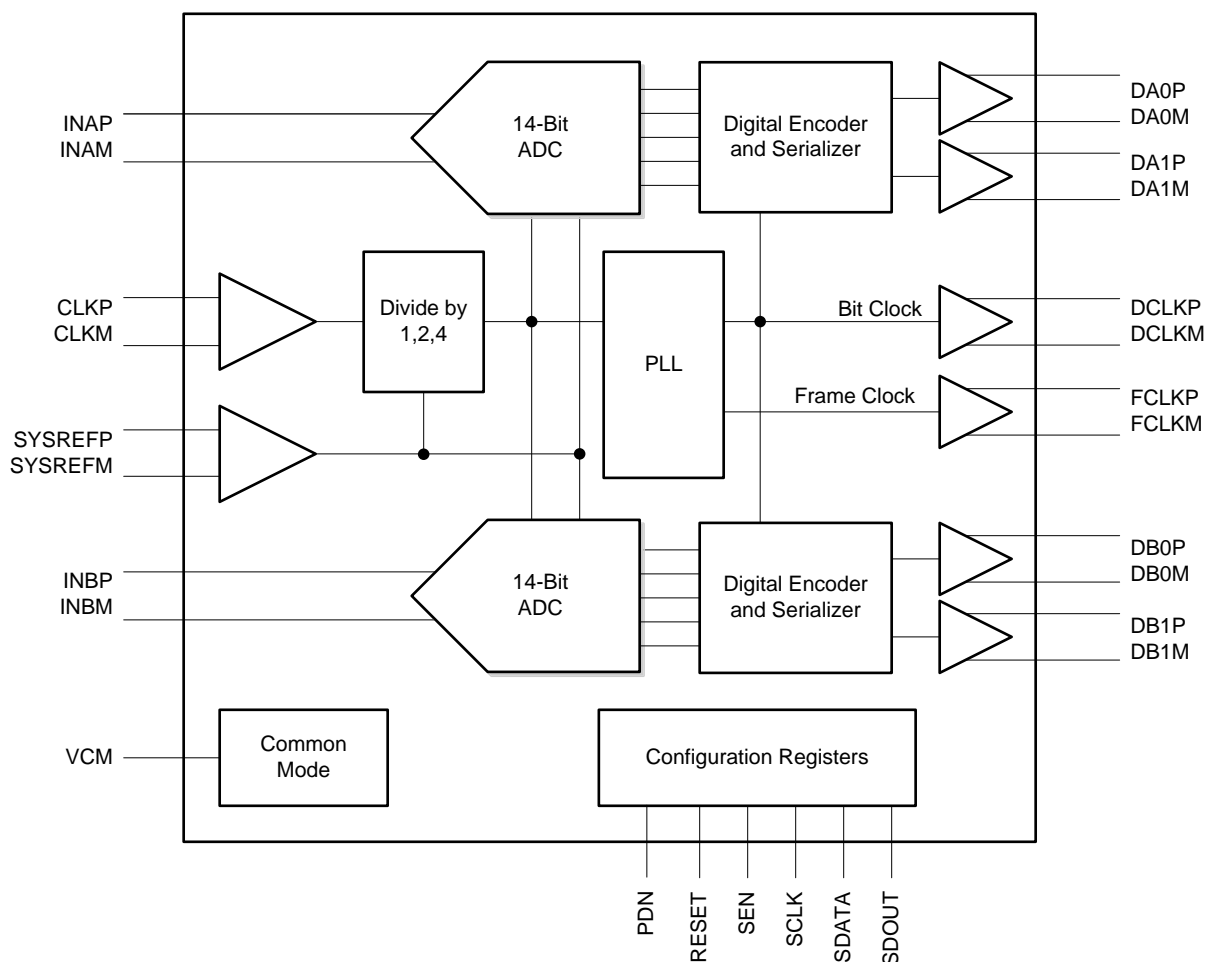
Figure 135. Latency Diagram

9 Detailed Description

9.1 Overview

The ADC324x are a high-linearity, ultra-low power, quad-channel, 14-bit, 25-MSPS to 125-MSPS, analog-to-digital converter (ADC) family. The devices are designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider allows more flexibility for system clock architecture design while the SYSREF input enables complete system synchronization. The ADC324x family supports serial LVDS interface in order to reduce the number of interface lines, thus allowing for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 14-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

9.2 Functional Block Diagram



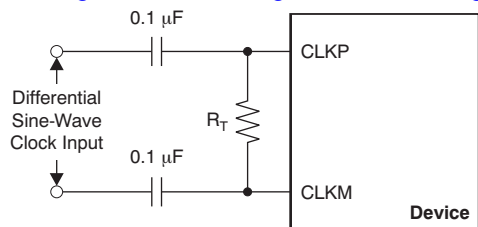
9.3 Feature Description

9.3.1 Analog Inputs

The ADC324x analog signal inputs are designed to be driven differentially. Each input pin (INP, INM) must swing symmetrically between $(V_{CM} + 0.5\text{ V})$ and $(V_{CM} - 0.5\text{ V})$, resulting in a $2\text{-}V_{PP}$ (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 540 MHz (50- Ω source driving 50- Ω termination between INP and INM).

9.3.2 Clock Input

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 0.95 V using internal 5-k Ω resistors. The self-bias clock inputs of the ADC324x can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 136, Figure 137, and Figure 138. See Figure 139 for details regarding the internal clock buffer.



NOTE: R_T = termination resistor, if necessary.

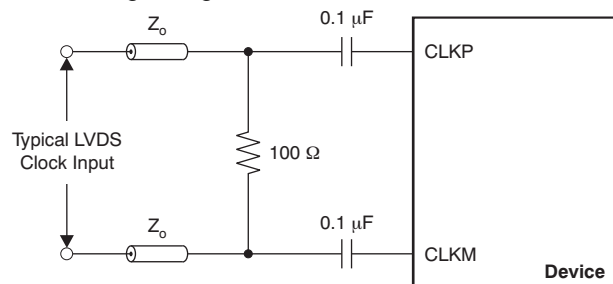


Figure 136. Differential Sine-Wave Clock Driving Circuit

Figure 137. LVDS Clock Driving Circuit

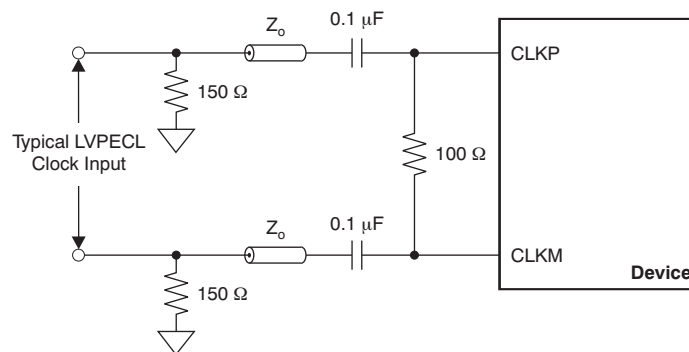
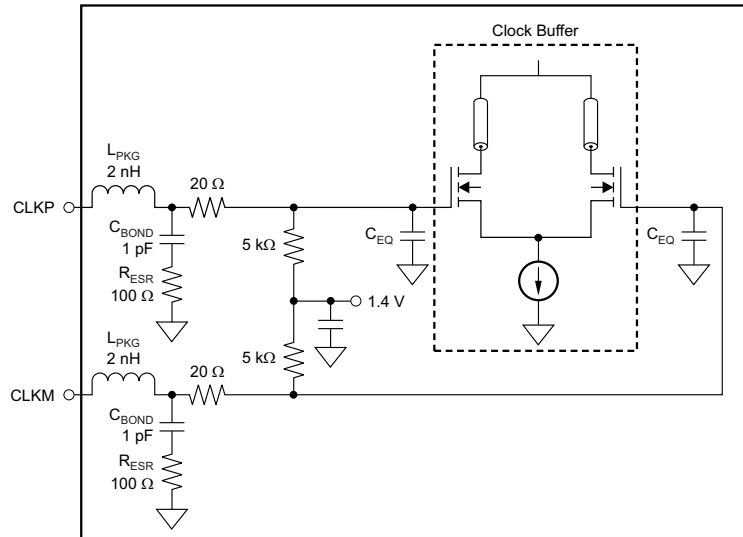


Figure 138. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 139. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-μF capacitor, as shown in Figure 140. However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

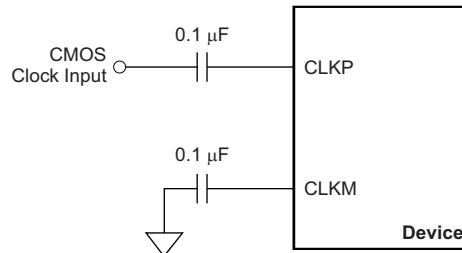


Figure 140. Single-Ended Clock Driving Circuit

9.3.2.1 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors, as shown in Equation 1. Quantization noise (typically 86 dB for a 14-bit ADC) and thermal noise limit SNR at low input frequencies while the clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \cdot \log \sqrt{\left(10^{\frac{SNR_{Quantization\ Noise}}{20}}\right)^2 + \left(10^{\frac{SNR_{Thermal\ Noise}}{20}}\right)^2 + \left(10^{\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

The SNR limitation resulting from sample clock jitter can be calculated with Equation 2.

$$SNR_{Jitter}[dBc] = -20 \cdot \log(2\pi \cdot f_{in} \cdot T_{Jitter}) \quad (2)$$

The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (130 fs for the device) which is set by the noise of the clock input buffer and the external clock. T_{Jitter} can be calculated with Equation 3.

$$T_{Jitter} = \sqrt{(T_{Jitter,Ext.Clock_Input})^2 + (T_{Aperture_ADC})^2} \quad (3)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band pass filters at the clock input while a faster clock slew rate improves the ADC aperture jitter. The ADC324x has a typical thermal noise of 73.5 dBFS and internal aperture jitter of 130 fs. [Figure 141](#) shows SNR (from 1 MHz offset leaving the 1/f flicker noise) for different jitter of clock driver.

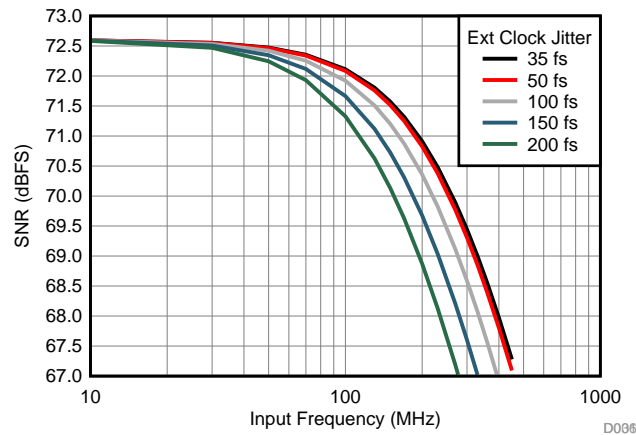


Figure 141. SNR vs Frequency for Different Clock Jitter

9.3.3 Digital Output Interface

The devices offer two different output format options, thus making interfacing to a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC) easy. Each option can be easily programmed using the serial interface, as shown in [Table 3](#). The output interface options are:

- One-wire, 1x frame clock, 14x serialization with the DDR bit clock and
- Two-wire, 0.5x frame clock, 7x serialization with the DDR bit clock.

Table 3. Interface Rates

| INTERFACE OPTIONS | SERIALIZATION | RECOMMENDED SAMPLING FREQUENCY (MSPS) | | BIT CLOCK FREQUENCY (MHz) | FRAME CLOCK FREQUENCY (MHz) | SERIAL DATA RATE (Mbps) |
|------------------------------|---------------|---------------------------------------|---------|---------------------------|-----------------------------|-------------------------|
| | | MINIMUM | MAXIMUM | | | |
| 1-wire | 14x | 15 ⁽¹⁾ | — | 105 | 15 | 210 |
| | | — | 80 | 560 | 80 | 1120 |
| 2-wire (default after reset) | 7x | 20 ⁽¹⁾ | — | 70 | 10 | 140 |
| | | — | 125 | 437.5 | 62.5 | 875 |

(1) Use the LOW SPEED ENABLE register bits for low speed operation; see [Table 22](#).

9.3.3.1 One-Wire Interface: 14x Serialization

In this interface option, the device outputs the data of each ADC serially on a single LVDS pair (one-wire). The data are available at the rising and falling edges of the bit clock (DDR bit clock). The ADC outputs a new word at the rising edge of every frame clock, starting with the MSB. The data rate is 14x sample frequency (14x serialization).

9.3.3.2 Two-Wire Interface: 7x Serialization

The two-wire interface is recommended for sampling frequencies above 65 MSPS. The output data rate is 7x sample frequency because seven data bits are output every clock cycle on each differential pair. Each ADC sample is sent over the two wires with the seven MSBs on Dx1P, Dx1M and the seven LSBs on Dx0P, Dx0M, as shown in Figure 142. Note that in two-wire mode, the frame clock (FCLK) frequency is half of sampling clock (CLKIN) frequency.

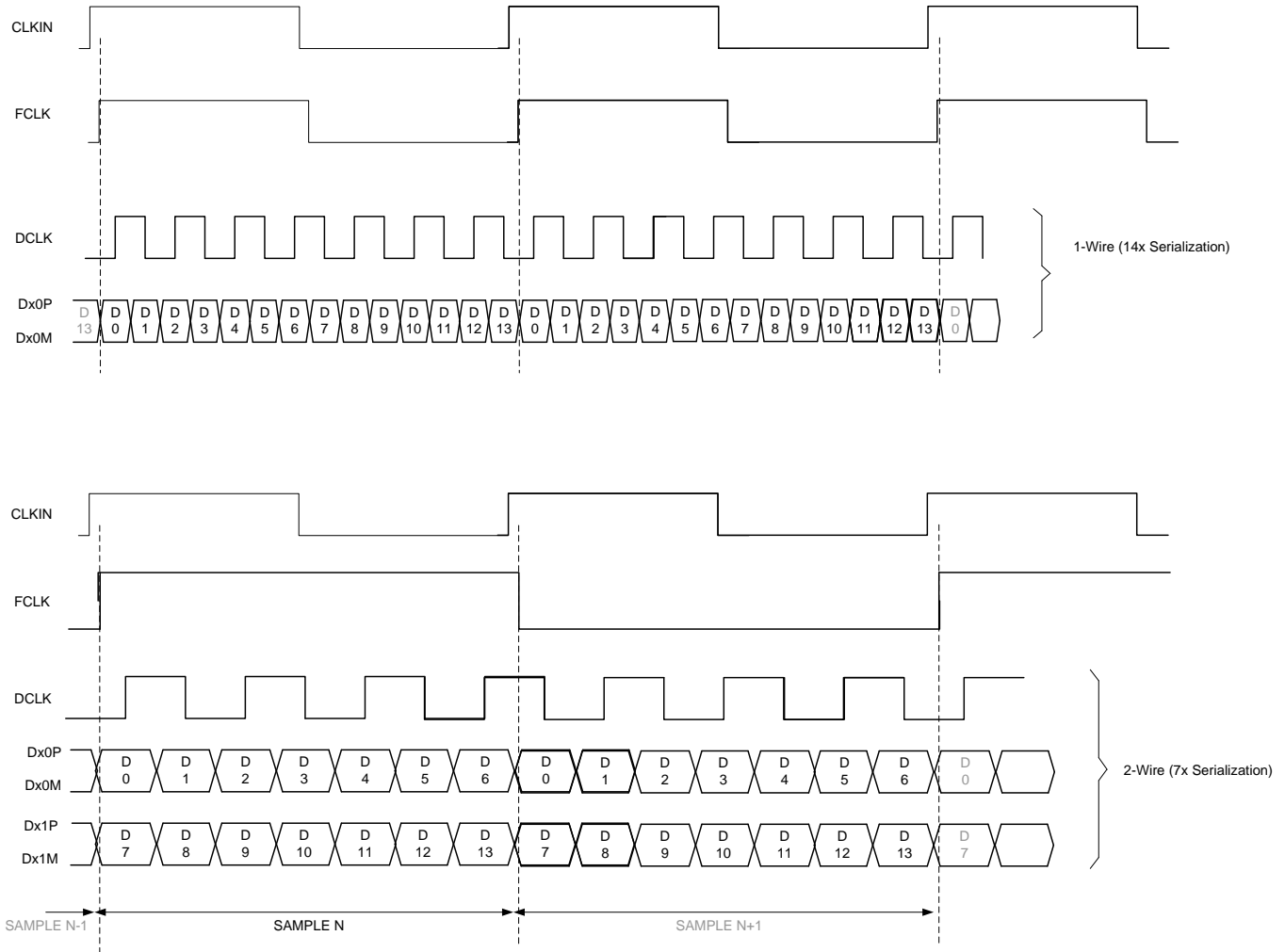


Figure 142. Output Timing Diagram

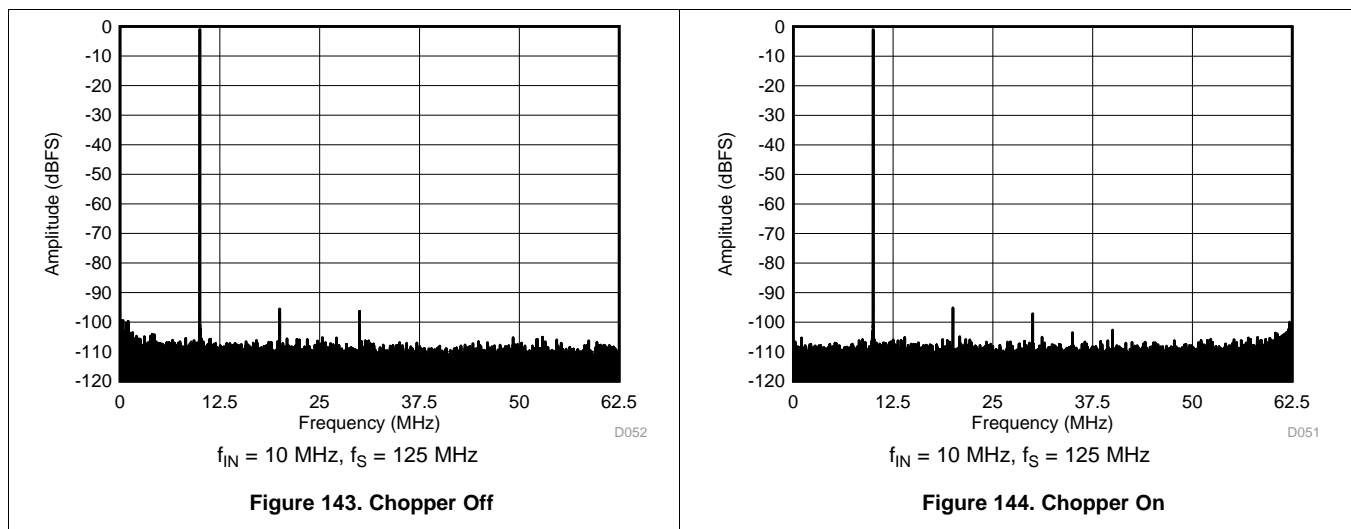
9.4 Device Functional Modes

9.4.1 Input Clock Divider

The devices are equipped with an internal divider on the clock input. The clock divider allows operation with a faster input clock, thus simplifying the system clock distribution design. The clock divider can be bypassed for operation with a 125-MHz clock while the divide-by-2 option supports a maximum input clock of 250 MHz and the divide-by-4 option provides a maximum input clock frequency of 500 MHz.

9.4.2 Chopper Functionality

The devices are equipped with an internal chopper front-end. Enabling the chopper function swaps the ADC noise spectrum by shifting the $1/f$ noise from dc to $f_S / 2$. [Figure 143](#) shows the noise spectrum with the chopper off and [Figure 144](#) shows the noise spectrum with the chopper on. This function is especially useful in applications requiring good ac performance at low input frequencies or in dc-coupled applications. The chopper can be enabled via SPI register writes and is recommended for input frequencies below 30 MHz. The chopper function creates a spur at $f_S / 2$ that must be filtered out digitally.



9.4.3 Power-Down Control

The power-down functions of the ADC324x can be controlled either through the parallel control pin (PDN) or through an SPI register setting (see [register 15h](#)). The PDN pin can also be configured via SPI to a global power-down or standby functionality, as shown in [Table 4](#).

Table 4. Power-Down Modes

| FUNCTION | POWER CONSUMPTION (mW) | WAKE-UP TIME (μ s) |
|-------------------|------------------------|-------------------------|
| Global power-down | 5 | 85 |
| Standby | 81 | 35 |

9.4.3.1 Improving Wake-Up Time From Global Power-Down

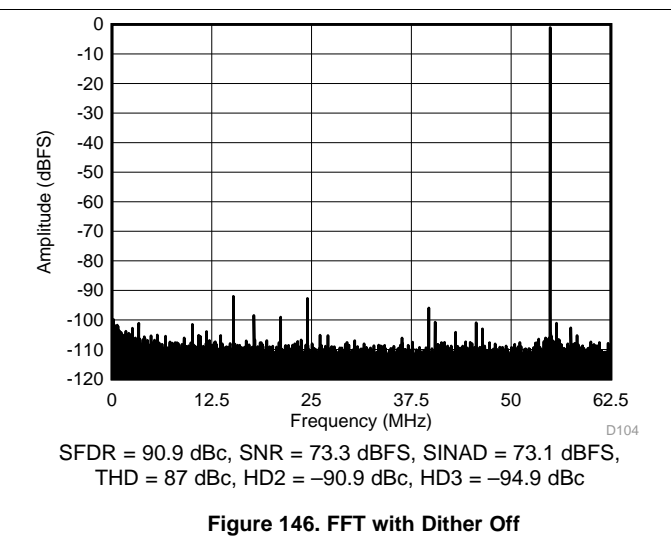
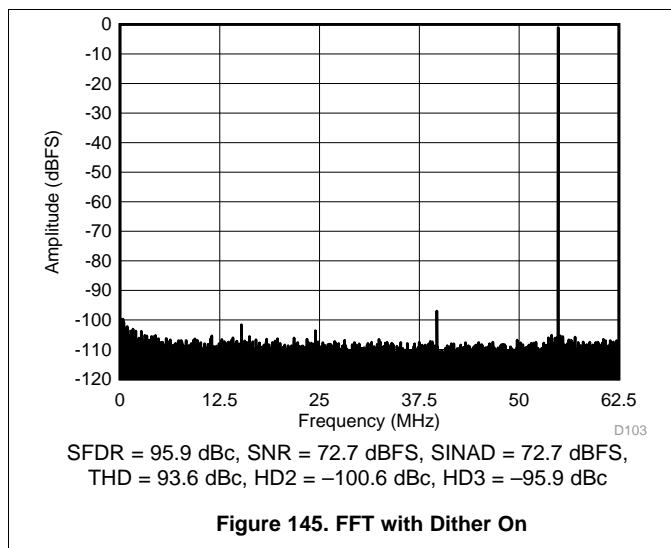
The device has an internal low-pass filter in the sampling clock path. This low-pass filter helps improve the aperture jitter of the device. However, in applications where input frequencies are < 200 MHz, noise from the aperture jitter does not dominate the overall SNR of the device. In such applications, the wake-up time from a global power-down can be reduced by bypassing the low-pass filter using the DIS CLK FILT register bit (write 80h to register address 70Ah). As shown in Table 5, setting the DIS CLK FILT bit improves the wake-up time from a global power-down from 85 μ s to 55 μ s.

Table 5. Wake-Up Time From Global Power-Down

| DIS CLK FILT REGISTER BIT | GLOBAL PDN REGISTER BIT | WAKE-UP TIME | | |
|---------------------------|-------------------------|--------------|-----|---------|
| | | TYP | MAX | UNIT |
| 0 | 0→1→0 | 85 | 140 | μ s |
| 1 | 0→1→0 | 55 | 81 | μ s |

9.4.4 Internal Dither Algorithm

The ADC324x use an internal dither algorithm to achieve high SFDR and a clean spectrum. However, the dither algorithm marginally degrades SNR, creating a trade-off between SNR and SFDR. If desired, the dither algorithm can be turned off by using the DIS DITH CHx registers bits. Figure 145 and Figure 146 show the effect of using dither algorithms.



9.5 Programming

The ADC324x can be configured using a serial programming interface, as described in this section.

9.5.1 Serial Interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

Programming (continued)

9.5.1.1 Register Initialization

After power-up, the internal registers **must be** initialized to their default values through a hardware reset by applying a high pulse on the RESET pin (of durations greater than 10 ns), as shown in Figure 147. If required, the serial interface registers can be cleared during operation either:

1. Through a hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

9.5.1.1.1 Serial Register Write

The device internal register can be programmed with these steps:

1. Drive the SEN pin low,
2. Set the R/W bit to 0 (bit A15 of the 16-bit address),
3. Set bit A14 in the address field to 1,
4. Initiate a serial interface cycle by specifying the address of the register (A13 to A0) whose content must be written, and
5. Write the 8-bit data that are latched in on the SCLK rising edge.

Figure 147 and Table 6 show the timing requirements for the serial register write operation.

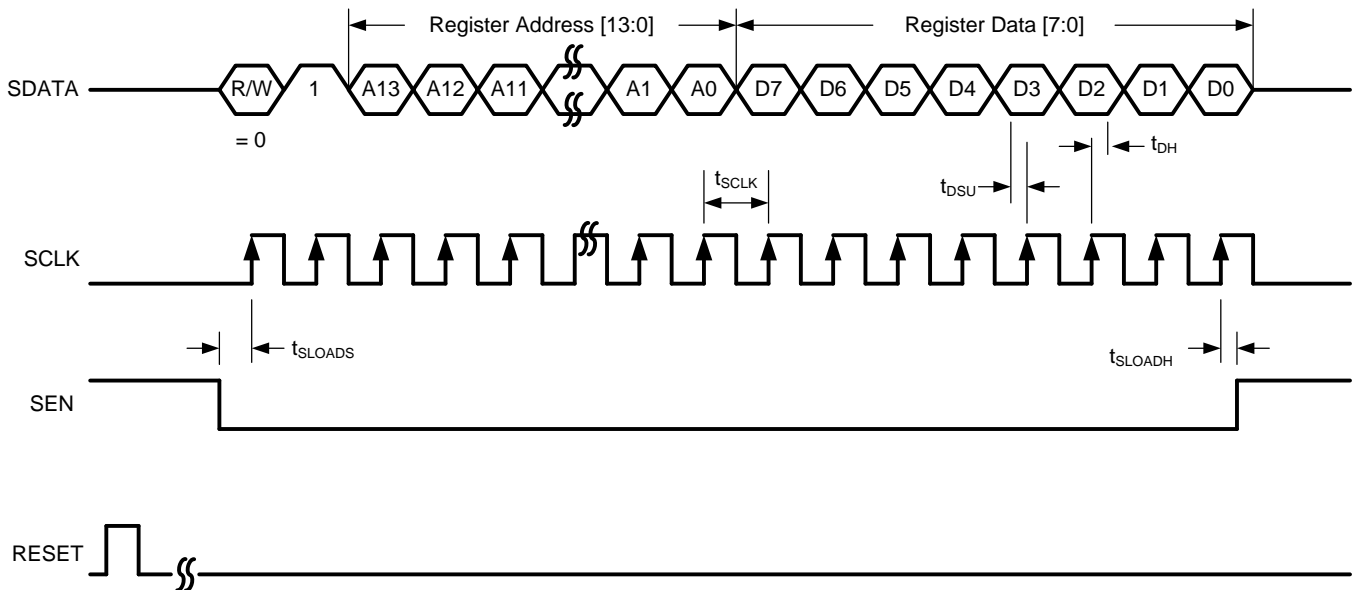


Figure 147. Serial Register Write Timing Diagram

Table 6. Serial Interface Timing⁽¹⁾

| | | MIN | TYP | MAX | UNIT |
|--------------|---|------|-----|-----|------|
| f_{SCLK} | SCLK frequency (equal to $1 / t_{SCLK}$) | > dc | | 20 | MHz |
| t_{SLOADS} | SEN to SCLK setup time | 25 | | | ns |
| t_{SLOADH} | SCLK to SEN hold time | 25 | | | ns |
| t_{DSU} | SDIO setup time | 25 | | | ns |
| t_{DH} | SDIO hold time | 25 | | | ns |

(1) Typical values are at 25°C, full temperature range is from $T_{MIN} = -40^{\circ}\text{C}$ to $T_{MAX} = 85^{\circ}\text{C}$, and $AVDD = DVDD = 1.8\text{ V}$, unless otherwise noted.

9.5.1.1.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDOUT pin. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. Given below is the procedure to read contents of serial registers:

1. Drive the SEN pin low.
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers.
3. Set bit A14 in the address field to 1.
4. Initiate a serial interface cycle specifying the address of the register (A13 to A0) whose content must be read.
5. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin.
6. The external controller can latch the contents at the SCLK rising edge.
7. To enable register writes, reset the R/W register bit to 0.

When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float. Figure 148 shows a timing diagram of the serial register read operation. Data appear on the SDOUT pin at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 20 ns, as shown in Figure 149.

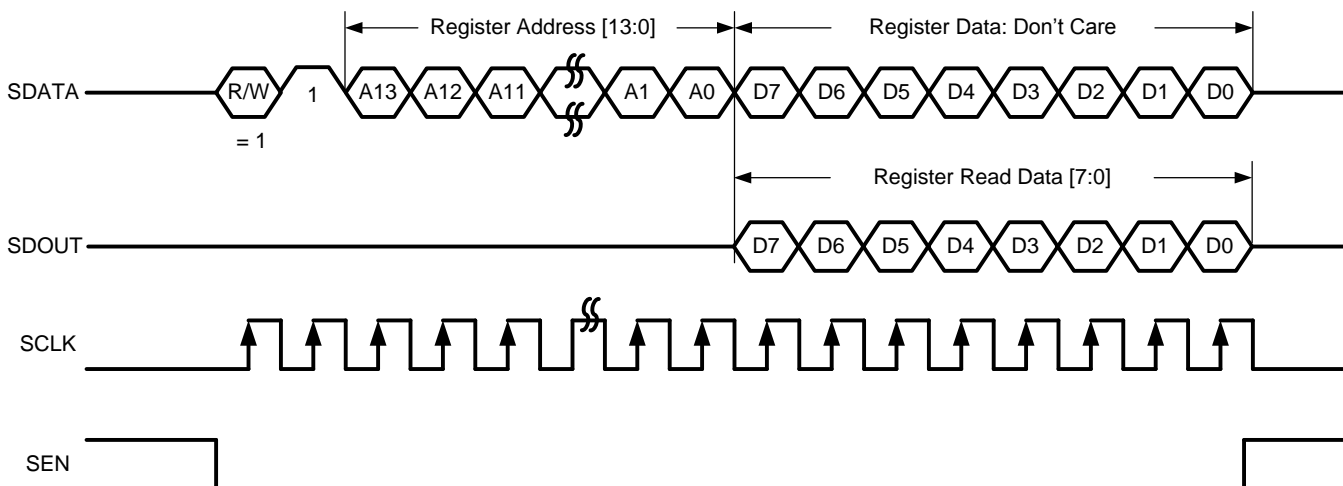


Figure 148. Serial Register Read Timing Diagram

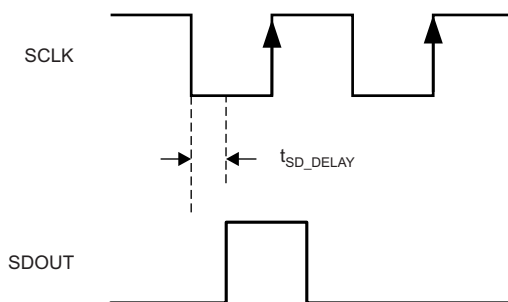


Figure 149. SDOUT Timing Diagram

9.5.2 Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin, as shown in [Figure 150](#) and [Table 7](#).

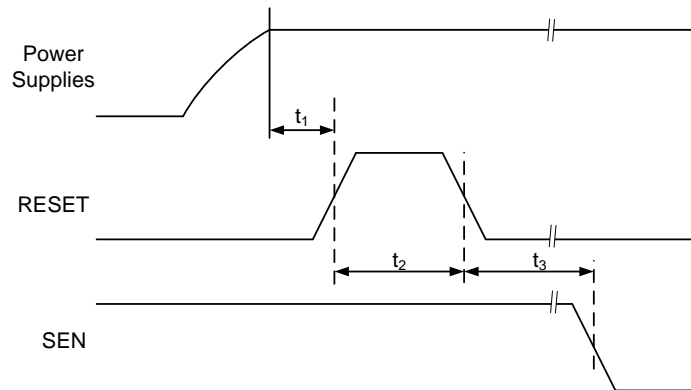


Figure 150. Initialization of Serial Registers after Power-Up

Table 7. Power-Up Timing

| | | MIN | TYP | MAX | UNIT |
|-------|--|-----|-----|------|------|
| t_1 | Power-on delay: delay from power up to active high RESET pulse | 1 | | | ms |
| t_2 | Reset pulse duration: active high RESET pulse duration | 10 | | 1000 | ns |
| t_3 | Register write delay: delay from RESET disable to SEN active | 100 | | | ns |

If required, the serial interface registers can be cleared during operation either:

1. Through hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

9.6 Register Maps

Table 8. Register Map Summary

| REGISTER ADDRESS | REGISTER DATA | | | | | | | |
|------------------|----------------------|---------|--------------|----|------------------|------------|--------------------|----------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 01 | 0 | 0 | DIS DITH CHA | | DIS DITH CHB | | 0 | 0 |
| 03 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | ODD EVEN |
| 04 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | FLIP WIRE |
| 05 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1W-2W |
| 06 | 0 | 0 | 0 | 0 | 0 | 0 | TEST PATTERN EN | RESET |
| 07 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | OVR ON LSB |
| 09 | 0 | 0 | 0 | 0 | 0 | 0 | ALIGN TEST PATTERN | DATA FORMAT |
| 0A | 0 | 0 | 0 | 0 | CHA TEST PATTERN | | | |
| 0B | CHB TEST PATTERN | | | 0 | 0 | 0 | 0 | 0 |
| 0E | CUSTOM PATTERN[13:6] | | | | | | | |
| 0F | CUSTOM PATTERN[5:0] | | | | | | 0 | 0 |
| 13 | 0 | 0 | 0 | 0 | 0 | 0 | LOW SPEED ENABLE | |
| 15 | 0 | CHA PDN | CHB PDN | 0 | STANDBY | GLOBAL PDN | 0 | CONFIG PDN PIN |
| 25 | LVDS SWING | | | | | | | |
| 27 | CLK DIV | | 0 | 0 | 0 | 0 | 0 | 0 |
| 41D | 0 | 0 | 0 | 0 | 0 | 0 | HIGH IF MODE0 | 0 |
| 422 | 0 | 0 | 0 | 0 | 0 | 0 | DIS CHOP CHA | 0 |
| 434 | 0 | 0 | DIS DITH CHA | 0 | DIS DITH CHA | 0 | 0 | 0 |
| 439 | 0 | 0 | 0 | 0 | SP1 CHA | 0 | 0 | 0 |
| 51D | 0 | 0 | 0 | 0 | 0 | 0 | HIGH IF MODE1 | 0 |
| 522 | 0 | 0 | 0 | 0 | 0 | 0 | DIS CHOP CHB | 0 |
| 534 | 0 | 0 | DIS DITH CHB | 0 | DIS DITH CHB | 0 | 0 | 0 |
| 539 | 0 | 0 | 0 | 0 | SP1 CHB | 0 | 0 | 0 |
| 608 | HIGH IF MODE[3:2] | | 0 | 0 | 0 | 0 | 0 | 0 |
| 70A | DIS CLK FILT | 0 | 0 | 0 | 0 | 0 | 0 | PDN SYSREF |

9.6.1 Summary of Special Mode Registers

Table 9 lists the location, value, and functions of special mode registers in the device.

Table 9. Special Modes Summary

| MODE | REGISTER SETTINGS | DESCRIPTION |
|-----------------|---|---|
| Special modes | Registers 439h (bit 3) and 539h (bit 3) | Always set these bits high for best performance |
| Disable dither | Registers 1h (bits 5-2), 434h (bits 5 and 3), and 534h (bits 5 and 3) | Disable dither to improve SNR |
| Disable chopper | Registers 422h (bit 1) and 522h (bit 1) | Disable chopper to shift 1/f noise floor at dc |
| High IF modes | Registers 41Dh (bit 1), 51Dh (bit 1), and 608h (bits 7-6) | Improves HD3 for IF > 100 MHz |

9.6.2 Serial Register Description

9.6.2.1 Register 01h

Figure 151. Register 01h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|--------------|---|--------------|---|------|------|
| 0 | 0 | DIS DITH CHA | | DIS DITH CHB | | 0 | 0 |
| W-0h | W-0h | R/W-0h | | R/W-0h | | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 10. Register 01h Description

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-6 | 0 | W | 0h | Must write 0 |
| 5-4 | DIS DITH CHA | R/W | 0h | These bits enable or disable the on-chip dither. Control this bit with bits 5 and 3 of register 434h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz. |
| 3-2 | DIS DITH CHB | R/W | 0h | These bits enable or disable the on-chip dither. Control this bit with bits 5 and 3 of register 434h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz. |
| 1-0 | 0 | W | 0h | Must write 0 |

9.6.2.2 Register 03h

Figure 152. Register 03h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | ODD EVEN |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 11. Register 03h Description

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | ODD EVEN | R/W | 0h | This bit selects the bit sequence on the output lanes (in 2-wire mode only). 0 = Bits 0, 1, and 2 appear on lane 0; bits 7, 8, and 9 appear on lane 1 1 = Bits 0, 2, and 4 appear on lane 0; bits 1, 3, and 5 appear on lane 1 |

9.6.2.3 Register 04h

Figure 153. Register 04h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|-----------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | FLIP WIRE |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 12. Register 04h Description

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | FLIP WIRE | R/W | 0h | This bit flips the data on the output wires. Valid only in two wire configuration. 0 = Default 1 = Data on output wires is flipped. Pin D0x becomes D1x, and vice versa. |

9.6.2.4 Register 05h

Figure 154. Register 05h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|--------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1W-2W |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 13. Register 05h Description

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | 1W-2W | R/W | 0h | This bit transmits output data on either one or two wires. 0 = Output data are transmitted on two wires (Dx0P, Dx0M and Dx1P, Dx1M) 1 = Output data are transmitted on one wire (Dx0P, Dx0M). In this mode, the recommended f_s is less than 62.5 MSPS. |

9.6.2.5 Register 06h

Figure 155. Register 06h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|-----------------|-------|
| 0 | 0 | 0 | 0 | 0 | 0 | TEST PATTERN EN | RESET |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 14. Register 06h Description

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7-2 | 0 | W | 0h | Must write 0 |
| 1 | TEST PATTERN EN | R/W | 0h | This bit enables test pattern selection for the digital outputs. 0 = Normal output 1 = Test pattern output enabled |
| 0 | RESET | W | 0h | This bit applies a software reset. This bit resets all internal registers to the default values and self-clears to 0. |

9.6.2.6 Register 07h
Figure 156. Register 07h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------|------------|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | OVR ON LSB |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 15. Register 07h Description

| Bit | Field | Type | Reset | Description |
|-----|------------|------|-------|---|
| 7-1 | 0 | W | 0h | Must write 0 |
| 0 | OVR ON LSB | R/W | 0h | This bit provides the overrange (OVR) information on the LSB bits. 0 = Output data bit 0 functions as the LSB of the 14-bit data 1 = Output data bit 0 carries the OVR information. |

9.6.2.7 Register 09h
Figure 157. Register 09h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|--------------------|-------------|
| 0 | 0 | 0 | 0 | 0 | 0 | ALIGN TEST PATTERN | DATA FORMAT |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 16. Register 09h Description

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7-2 | 0 | W | 0h | Must write 0 |
| 1 | ALIGN TEST PATTERN | R/W | 0h | This bit aligns the test patterns across the outputs of both channels. 0 = Test patterns of both channels are free running 1 = Test patterns of both channels are aligned |
| 0 | DATA FORMAT | R/W | 0h | This bit programs the digital output data format. 0 = Twos complement 1 = Offset binary |

9.6.2.8 Register 0Ah
Figure 158. Register 0Ah

| | | | | | | | |
|------|------|------|------|------------------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| 0 | 0 | 0 | 0 | CHA TEST PATTERN | | | |
| W-0h | W-0h | W-0h | W-0h | R/W-0h | | | |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 17. Register 0Ah Description

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 7-4 | 0 | W | 0h | Must write 0 |
| 3-0 | CHA TEST PATTERN | R/W | 0h | <p>These bits control the test pattern for channel A after the TEST PATTERN EN bit is set.</p> <p>0000 = Normal operation</p> <p>0001 = All 0's</p> <p>0010 = All 1's</p> <p>0011 = Toggle pattern: data alternate between 101010101010 and 010101010101</p> <p>0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383</p> <p>0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits</p> <p>0110 = Deskew pattern: data are 2AAAh</p> <p>1000 = PRBS pattern: data are a sequence of pseudo random numbers</p> <p>1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399.</p> <p>Others = Do not use</p> |

9.6.2.9 Register 0Bh
Figure 159. Register 0Bh

| | | | | | | | |
|------------------|---|---|---|------|------|------|------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHB TEST PATTERN | | | | 0 | 0 | 0 | 0 |
| R/W-0h | | | | W-0h | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 18. Register 0Bh Description

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|---|
| 7-4 | CHB TEST PATTERN | R/W | 0h | <p>These bits control the test pattern for channel B after the TEST PATTERN EN bit is set.</p> <p>0000 = Normal operation</p> <p>0001 = All 0's</p> <p>0010 = All 1's</p> <p>0011 = Toggle pattern: data alternate between 101010101010 and 010101010101</p> <p>0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 16383</p> <p>0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits</p> <p>0110 = Deskew pattern: data are 2AAAh</p> <p>1000 = PRBS pattern: data are a sequence of pseudo random numbers</p> <p>1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 2399, 8192, 13984, 16383, 13984, 8192, 2399.</p> <p>Others = Do not use</p> |
| 3-0 | 0 | W | 0h | Must write 0 |

9.6.2.10 Register 0Eh
Figure 160. Register 0Eh

| | | | | | | | |
|----------------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CUSTOM PATTERN[13:6] | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 19. Register 0Eh Description

| Bit | Field | Type | Reset | Description |
|-----|----------------------|------|-------|--|
| 7-0 | CUSTOM PATTERN[13:6] | R/W | 0h | These bits set the 14-bit custom pattern (bits 13-6) for all channels. |

9.6.2.11 Register 0Fh
Figure 161. Register 0Fh

| | | | | | | | |
|---------------------|---|---|---|---|---|------|------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CUSTOM PATTERN[5:0] | | | | | | 0 | 0 |
| R/W-0h | | | | | | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 20. Register 0Fh Description

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 7-2 | CUSTOM PATTERN[5:0] | R/W | 0h | These bits set the 14-bit custom pattern (bits 5-0) for all channels. |
| 1-0 | 0 | W | 0h | Must write 0 |

9.6.2.12 Register 13h (address = 13h)
Figure 162. Register 13h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|------------------|---|
| 0 | 0 | 0 | 0 | 0 | 0 | LOW SPEED ENABLE | |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | |

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 21. Register 13h Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|--|
| 7-2 | 0 | W | 0h | Must write 0. |
| 1-0 | LOW SPEED ENABLE | R/W | 0h | Enables low speed operation in 1-wire and 2-wire mode. Depending upon sampling frequency, write this bit as per Table 22 . |

Table 22. LOW SPEED ENABLE Register Bit Settings Across f_s

| f_s (MSPS) | | REGISTER BIT LOW SPEED ENABLE | |
|--------------|-----|-------------------------------|---------------|
| MIN | MAX | 1-WIRE MODE | 2-WIRE MODE |
| 25 | 125 | 00 | 00 |
| 20 | 25 | 00 | 10 |
| 15 | 20 | 10 | Not supported |

9.6.2.13 Register 15h
Figure 163. Register 15h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|---------|---------|------|---------|------------|------|----------------|
| 0 | CHA PDN | CHB PDN | 0 | STANDBY | GLOBAL PDN | 0 | CONFIG PDN PIN |
| W-0h | R/W-0h | R/W-0h | W-0h | R/W-0h | R/W-0h | W-0h | R/W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 23. Register 15h Description

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | 0 | W | 0h | Must write 0 |
| 6 | CHA PDN | R/W | 0h | 0 = Normal operation 1 = Power-down channel A |
| 5 | CHB PDN | R/W | 0h | 0 = Normal operation 1 = Power-down channel B |
| 4 | 0 | W | 0h | Must write 0 |
| 3 | STANDBY | R/W | 0h | The ADCs of both channels enter standby. 0 = Normal operation 1 = Standby |
| 2 | GLOBAL PDN | R/W | 0h | 0 = Normal operation 1 = Global power-down |
| 1 | 0 | W | 0h | Must write 0 |
| 0 | CONFIG PDN PIN | R/W | 0h | This bit configures the PDN pin as either a global power-down or standby pin. 0 = Logic high voltage on the PDN pin sends the device into global power-down 1 = Logic high voltage on the PDN pin sends the device into standby |

9.6.2.14 Register 25h
Figure 164. Register 25h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------------|---|---|---|---|---|---|---|
| LVDS SWING | | | | | | | |
| R/W-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 24. Register 25h Description

| Bit | Field | Type | Reset | Description |
|-----|------------|------|-------|--|
| 7-0 | LVDS SWING | R/W | 0h | These bits control the swing of the LVDS outputs (including the data output, bit clock, and frame clock). For details see Table 25 . |

Table 25. LVDS Output Swing

| BITS 7-4 | BITS 3-0 | LVDS OUTPUT SWING |
|----------|----------|---------------------------|
| 0h | 0h | Default (± 425 mV) |
| Dh | 9h | Swing reduces by 50 mV |
| Eh | Ah | Swing reduces by 100 mV |
| Fh | Dh | Swing reduces by 300 mV |
| Ch | Eh | Swing increases by 100 mV |
| Others | Others | Do not use |

9.6.2.15 Register 27h
Figure 165. Register 27h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------|---|------|------|------|------|------|------|
| CLK DIV | | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W-0h | | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 26. Register 27h Description

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 7-6 | CLK DIV | R/W | 0h | These bits set the internal clock divider for the input sampling clock. 00 = Divide-by-1 01 = Divide-by-1 10 = Divide-by-2 11 = Divide-by-4 |
| 5-0 | 0 | W | 0h | Must write 0 |

9.6.2.16 Register 41Dh
Figure 166. Register 41Dh

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|---------------|------|
| 0 | 0 | 0 | 0 | 0 | 0 | HIGH IF MODE0 | 0 |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 27. Register 41Dh Description

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7-2 | 0 | W | 0h | Must write 0 |
| 1 | HIGH IF MODE0 | R/W | 0h | This bit improves HD3 for IF > 100 MHz. 0 = Normal operation For best HD3 at IF > 100 MHz, set HIGH IF MODE[3:0] to 1111. |
| 0 | 0 | W | 0h | Must write 0 |

9.6.2.17 Register 422h
Figure 167. Register 422h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|--------------|------|
| 0 | 0 | 0 | 0 | 0 | 0 | DIS CHOP CHA | 0 |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 28. Register 422h Description

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7-2 | 0 | W | 0h | Must write 0 |
| 1 | DIS CHOP CHA | R/W | 0h | Disable chopper. Set this bit to shift a 1/f noise floor at dc. 0 = 1/f noise floor is centered at $f_S / 2$ (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc |
| 0 | 0 | W | 0h | Must write 0 |

9.6.2.18 Register 434h
Figure 168. Register 434h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|--------------|------|--------------|------|------|------|
| 0 | 0 | DIS DITH CHA | 0 | DIS DITH CHA | 0 | 0 | 0 |
| W-0h | W-0h | R/W-0h | W-0h | R/W-0h | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 29. Register 434h Description

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-6 | 0 | W | 0h | Must write 0 |
| 5 | DIS DITH CHA | R/W | 0h | Set this bit with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz. |
| 4 | 0 | W | 0h | Must write 0 |
| 3 | DIS DITH CHA | R/W | 0h | Set this bit with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.5 dB at 70 MHz. |
| 2-0 | 0 | W | 0h | Must write 0 |

9.6.2.19 Register 439h
Figure 169. Register 439h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|---------|------|------|------|
| 0 | 0 | 0 | 0 | SP1 CHA | 0 | 0 | 0 |
| W-0h | W-0h | W-0h | W-0h | R/W-0h | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 30. Register 439h Description

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|---|
| 7-4 | 0 | W | 0h | Must write 0 |
| 3 | SP1 CHA | R/W | 0h | Special mode for best performance on channel A. Always write 1 after reset. |
| 2-0 | 0 | W | 0h | Must write 0 |

9.6.2.20 Register 51Dh
Figure 170. Register 51Dh

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|---------------|------|
| 0 | 0 | 0 | 0 | 0 | 0 | HIGH IF MODE1 | 0 |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 31. Register 51Dh Description

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7-2 | 0 | W | 0h | Must write 0 |
| 1 | HIGH IF MODE1 | R/W | 0h | This bit improves HD3 for IF > 100 MHz. 0 = Normal operation For best HD3 at IF > 100 MHz, set HIGH IF MODE[3:0] to 1111. |
| 0 | 0 | W | 0h | Must write 0 |

9.6.2.21 Register 522h
Figure 171. Register 522h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|------|------|--------------|------|
| 0 | 0 | 0 | 0 | 0 | 0 | DIS CHOP CHB | 0 |
| W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 32. Register 522h Description

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7-2 | 0 | W | 0h | Must write 0 |
| 1 | DIS CHOP CHB | R/W | 0h | Disable chopper. Set this bit to shift a 1/f noise floor at dc. 0 = 1/f noise floor is centered at $f_s / 2$ (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc |
| 0 | 0 | W | 0h | Must write 0 |

9.6.2.22 Register 534h
Figure 172. Register 534h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|--------------|------|--------------|------|------|------|
| 0 | 0 | DIS DITH CHA | 0 | DIS DITH CHA | 0 | 0 | 0 |
| W-0h | W-0h | R/W-0h | W-0h | R/W-0h | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 33. Register 534h Description

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-6 | 0 | W | 0h | Must write 0 |
| 5 | DIS DITH CHA | R/W | 0h | Set this bit with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz. |
| 4 | 0 | W | 0h | Must write 0 |
| 3 | DIS DITH CHA | R/W | 0h | Set this bit with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.5 dB at 70 MHz. |
| 2-0 | 0 | W | 0h | Must write 0 |

9.6.2.23 Register 539h
Figure 173. Register 539h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|------|------|------|------|---------|------|------|------|
| 0 | 0 | 0 | 0 | SP1 CHB | 0 | 0 | 0 |
| W-0h | W-0h | W-0h | W-0h | R/W-0h | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 34. Register 539h Description

| Bit | Field | Type | Reset | Description |
|-----|---------|------|-------|--|
| 7-4 | 0 | W | 0h | Must write 0 |
| 3 | SP1 CHB | R/W | 0h | Special mode for best performance on channel B. Always write 1 after reset. |
| 0 | 0 | W | 0h | Must write 0 |

9.6.2.24 Register 608h
Figure 174. Register 608h

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------------|---|------|------|------|------|------|------|
| HIGH IF MODE[3:2] | | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W-0h | | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 35. Register 608h Description

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 7-6 | HIGH IF MODE[3:2] | R/W | 0h | This bit improves HD3 for IF > 100 MHz. 0 = Normal operation For best HD3 at IF > 100 MHz, set HIGH IF MODE[3:0] to 1111. |
| 5-0 | 0 | W | 0h | Must write 0 |

9.6.2.25 Register 70Ah
Figure 175. Register 70Ah

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|------|------|------|------|------|------|------------|
| DIS CLK FILT | 0 | 0 | 0 | 0 | 0 | 0 | PDN SYSREF |
| R/W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | W-0h | R/W-0h |

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

Table 36. Register 70Ah Description

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7 | DIS CLK FILT | R/W | 0h | Set this bit to improve wake-up time from global power-down mode; see the Improving Wake-Up Time From Global Power-Down section for details. |
| 6-1 | 0 | W | 0h | Must write 0 |
| 0 | PDN SYSREF | R/W | 0h | If the SYSREF pins are not used in the system, the SYSREF buffer must be powered down by setting this bit. 0 = Normal operation 1 = Powers down the SYSREF buffer |

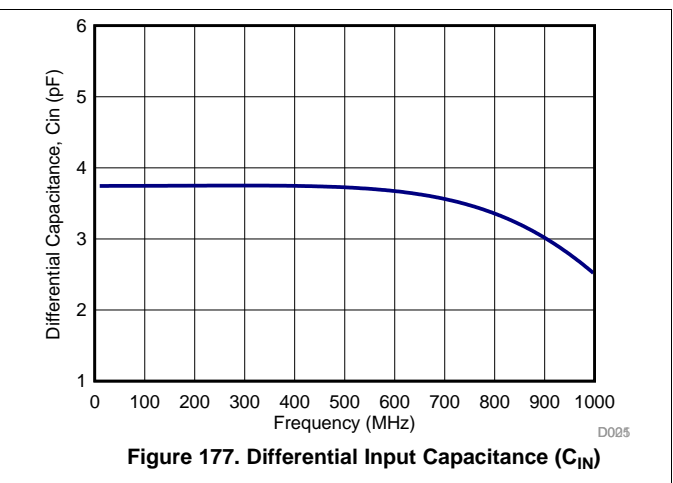
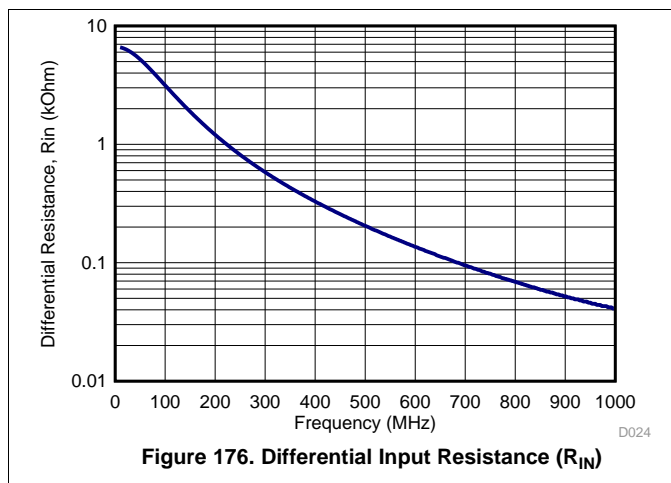
10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

Typical applications involving transformer coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) can be used up to 250 MHz to achieve good phase and amplitude balances at ADC inputs. While designing the dc driving circuits, the ADC input impedance must be considered. [Figure 176](#) and [Figure 177](#) show the impedance ($Z_{in} = R_{in} || C_{in}$) across the ADC input pins.



10.2 Typical Applications

10.2.1 Driving Circuit Design: Low Input Frequencies

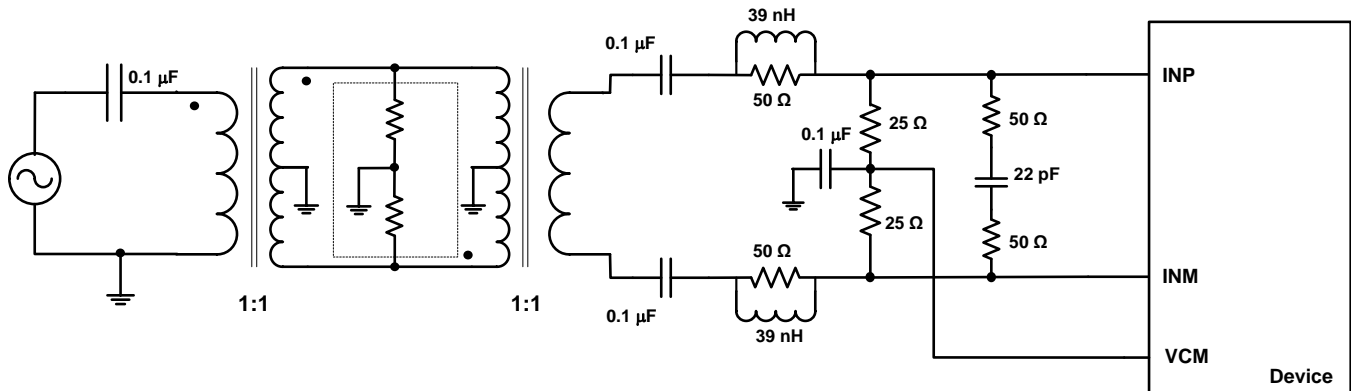


Figure 178. Driving Circuit for Low Input Frequencies

10.2.1.1 Design Requirements

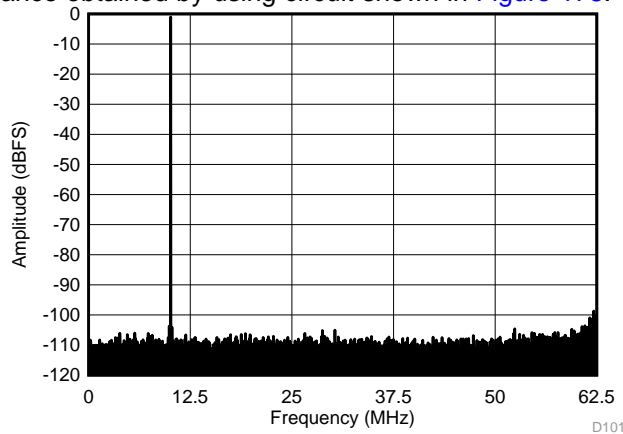
For optimum performance, the analog inputs must be driven differentially. An optional 5-Ω to 15-Ω resistor in series with each input pin can be kept to damp out ringing caused by package parasitic. The drive circuit may have to be designed to minimize the impact of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as ensuring low insertion loss over the desired frequency range and matched impedance to the source.

10.2.1.2 Detailed Design Procedure

A typical application involving using two back-to-back coupled transformers is shown in [Figure 178](#). The circuit is optimized for low input frequencies. An external R-C-R filter using 50-Ω resistors and a 22-pF capacitor is used with the series inductor (39 nH), this combination helps absorb the sampling glitches.

10.2.1.3 Application Curve

[Figure 179](#) shows the performance obtained by using circuit shown in [Figure 178](#).



SFDR = 102.6 dBc, SNR = 72.9 dBFS, SINAD = 72.8 dBFS,
THD = 99.8 dBc, HD2 = -108.6 dBc, HD3 = -104.0 dBc

Figure 179. Performance FFT at 10 MHz (Low Input Frequency)

Typical Applications (continued)

10.2.2 Driving Circuit Design: Input Frequencies Between 100 MHz to 230 MHz

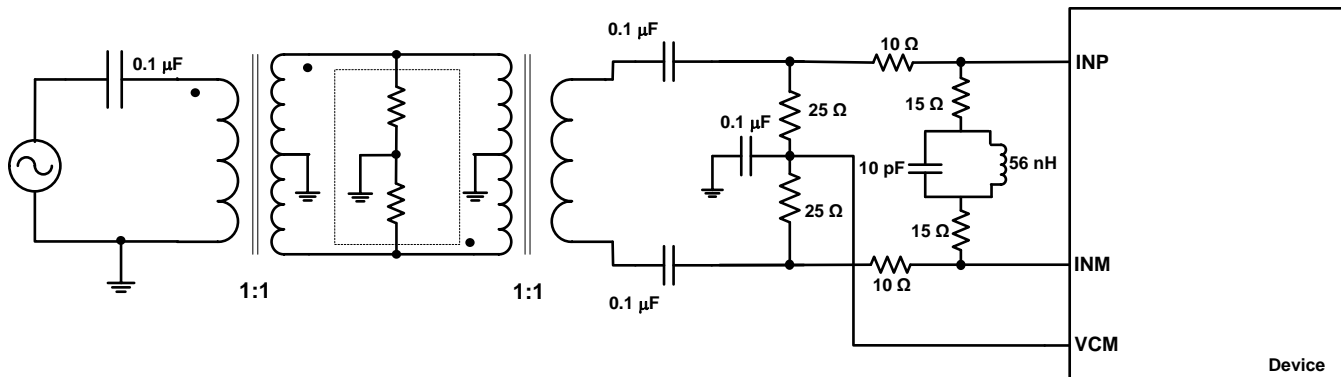


Figure 180. Driving Circuit for Mid-Range Input Frequencies ($100 \text{ MHz} < f_{IN} < 230 \text{ MHz}$)

10.2.2.1 Design Requirements

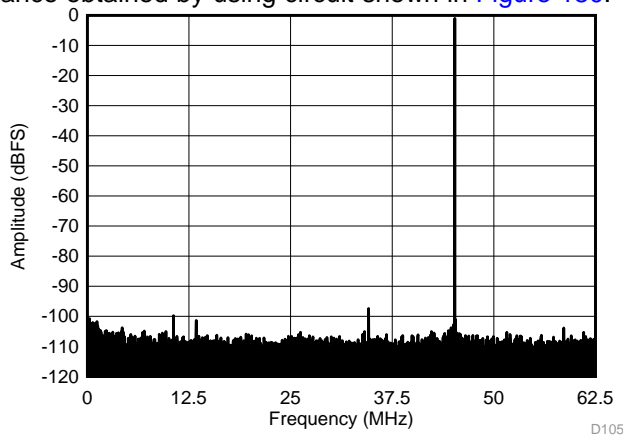
See the [Design Requirements](#) section for further details.

10.2.2.2 Detailed Design Procedure

When input frequencies are between 100 MHz to 230 MHz, an R-LC-R circuit can be used to optimize performance, as shown in [Figure 180](#).

10.2.2.3 Application Curve

[Figure 181](#) shows the performance obtained by using circuit shown in [Figure 180](#).



SFDR = 96.4 dBc, SNR = 72.1 dBFS, SINAD = 72.0 dBFS,
THD = 92.6 dBc, HD2 = -96.4 dBc, HD3 = -98.8 dBc

Figure 181. Performance FFT at 170 MHz (Mid Input Frequency)

Typical Applications (continued)

10.2.3 Driving Circuit Design: Input Frequencies Greater than 230 MHz

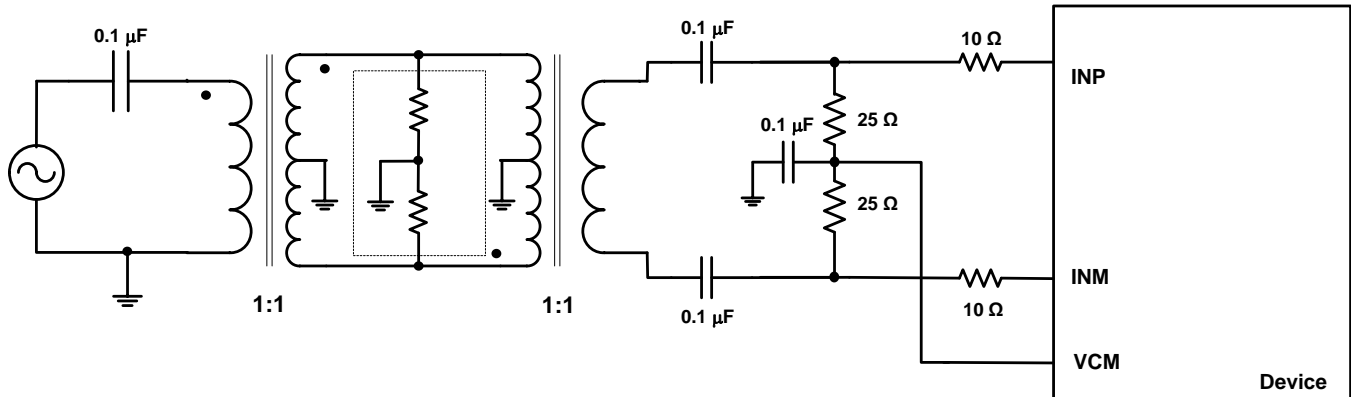


Figure 182. Driving Circuit for High input Frequencies ($f_{IN} > 230$ MHz)

10.2.3.1 Design Requirements

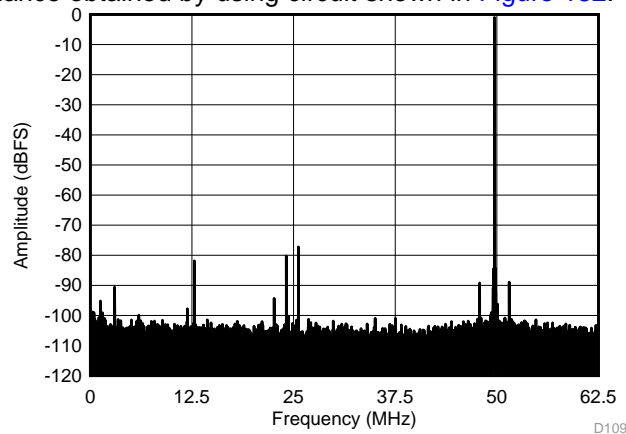
See the [Design Requirements](#) section for further details.

10.2.3.2 Detailed Design Procedure

For high input frequencies (> 230 MHz), using the R-C-R or R-LC-R circuit does not show significant improvement in performance. However, a series resistance of $10\ \Omega$ can be used as shown in [Figure 182](#).

10.2.3.3 Application Curve

[Figure 183](#) shows the performance obtained by using circuit shown in [Figure 182](#).



SFDR = 76.2 dBc, SNR = 68.3 dBFS, SINAD = 67.5 dBFS,

THD = 74.3 dBc, HD2 = -76.2 dBc, HD3 = -79.2 dBc

Figure 183. Performance FFT at 450 MHz (High Input Frequency)

11 Power-Supply Recommendations

The device requires a 1.8-V nominal supply for AVDD and DVDD. There are no specific sequence power-supply requirements during device power-up. AVDD and DVDD can power up in any order.

12 Layout

12.1 Layout Guidelines

The ADC324x EVM layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in [Figure 184](#). Some important points to remember during laying out the board are:

1. Analog inputs are located on opposite sides of the device pin out to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pin out in opposite directions, as shown in the reference layout of [Figure 184](#) as much as possible.
2. In the device pin out, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of [Figure 184](#) as much as possible.
3. Keep digital outputs away from the analog inputs. When these digital outputs exit the pin out, do not keep the digital output traces parallel to the analog input traces because this configuration can result in coupling from digital outputs to analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.
4. At each power-supply pin (AVDD and DVDD), keep a 0.1- μ F decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10- μ F, 1- μ F, and 0.1- μ F capacitors can be kept close to the supply source.

12.2 Layout Example

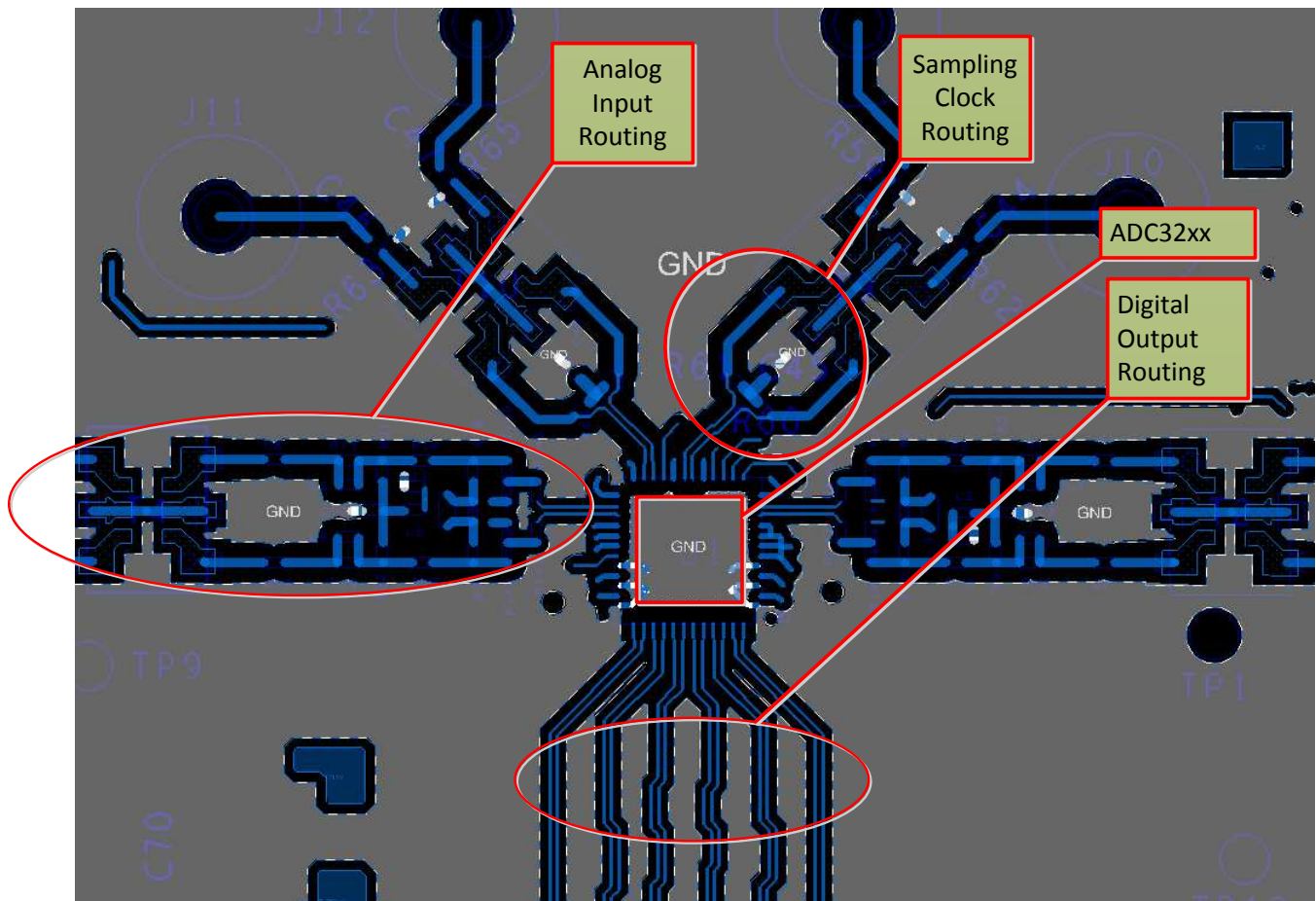


Figure 184. Typical Layout of the ADC324x Board

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 37. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|---------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| ADC3241 | Click here | Click here | Click here | Click here | Click here |
| ADC3242 | Click here | Click here | Click here | Click here | Click here |
| ADC3243 | Click here | Click here | Click here | Click here | Click here |
| ADC3244 | Click here | Click here | Click here | Click here | Click here |

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.

PowerPAD is a trademark of Texas Instruments, Inc.

All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|------------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| ADC3241IRGZR | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3241 |
| ADC3241IRGZR.A | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3241 |
| ADC3241IRGZT | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3241 |
| ADC3241IRGZT.A | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3241 |
| ADC3242IRGZR | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3242 |
| ADC3242IRGZR.A | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3242 |
| ADC3242IRGZT | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3242 |
| ADC3242IRGZT.A | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3242 |
| ADC3243IRGZR | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3243 |
| ADC3243IRGZR.A | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3243 |
| ADC3243IRGZT | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3243 |
| ADC3243IRGZT.A | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3243 |
| ADC3244IRGZR | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3244 |
| ADC3244IRGZR.A | Active | Production | VQFN (RGZ) 48 | 2500 LARGE T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3244 |
| ADC3244IRGZT | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3244 |
| ADC3244IRGZT.A | Active | Production | VQFN (RGZ) 48 | 250 SMALL T&R | Yes | NIPDAUAG | Level-3-260C-168 HR | -40 to 85 | AZ3244 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| ADC3241IRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q2 |
| ADC3242IRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q2 |
| ADC3243IRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q2 |
| ADC3244IRGZR | VQFN | RGZ | 48 | 2500 | 330.0 | 16.4 | 7.3 | 7.3 | 1.5 | 12.0 | 16.0 | Q2 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|--------------|--------------|-----------------|------|------|-------------|------------|-------------|
| ADC3241IRGZR | VQFN | RGZ | 48 | 2500 | 350.0 | 350.0 | 43.0 |
| ADC3242IRGZR | VQFN | RGZ | 48 | 2500 | 350.0 | 350.0 | 43.0 |
| ADC3243IRGZR | VQFN | RGZ | 48 | 2500 | 350.0 | 350.0 | 43.0 |
| ADC3244IRGZR | VQFN | RGZ | 48 | 2500 | 350.0 | 350.0 | 43.0 |

GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

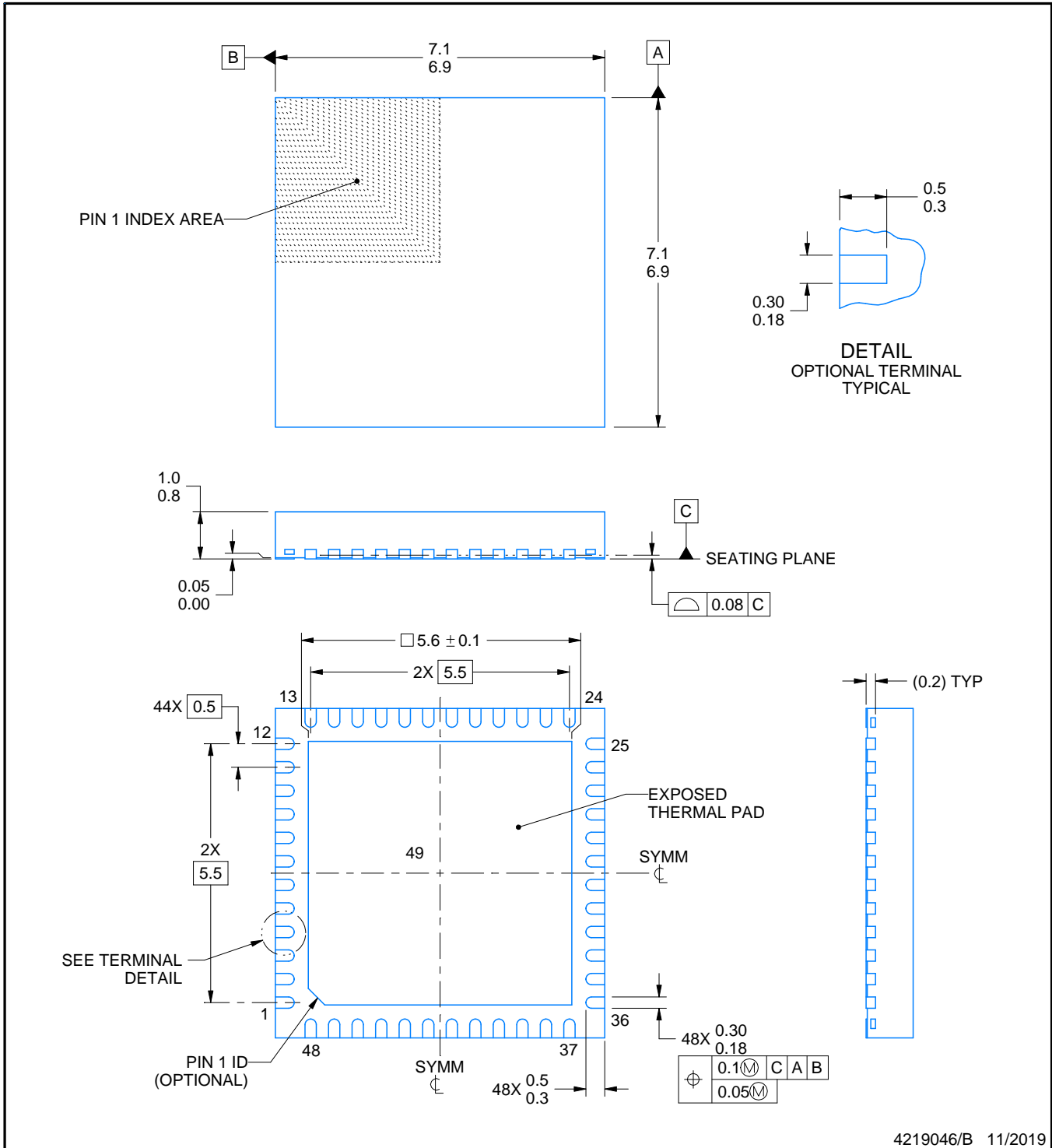
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4224671/A



4219046/B 11/2019

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

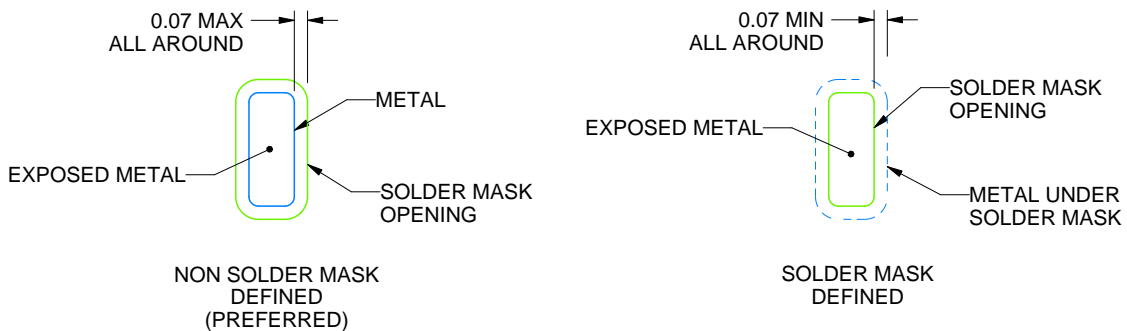
RGZ0048D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

4219046/B 11/2019

NOTES: (continued)

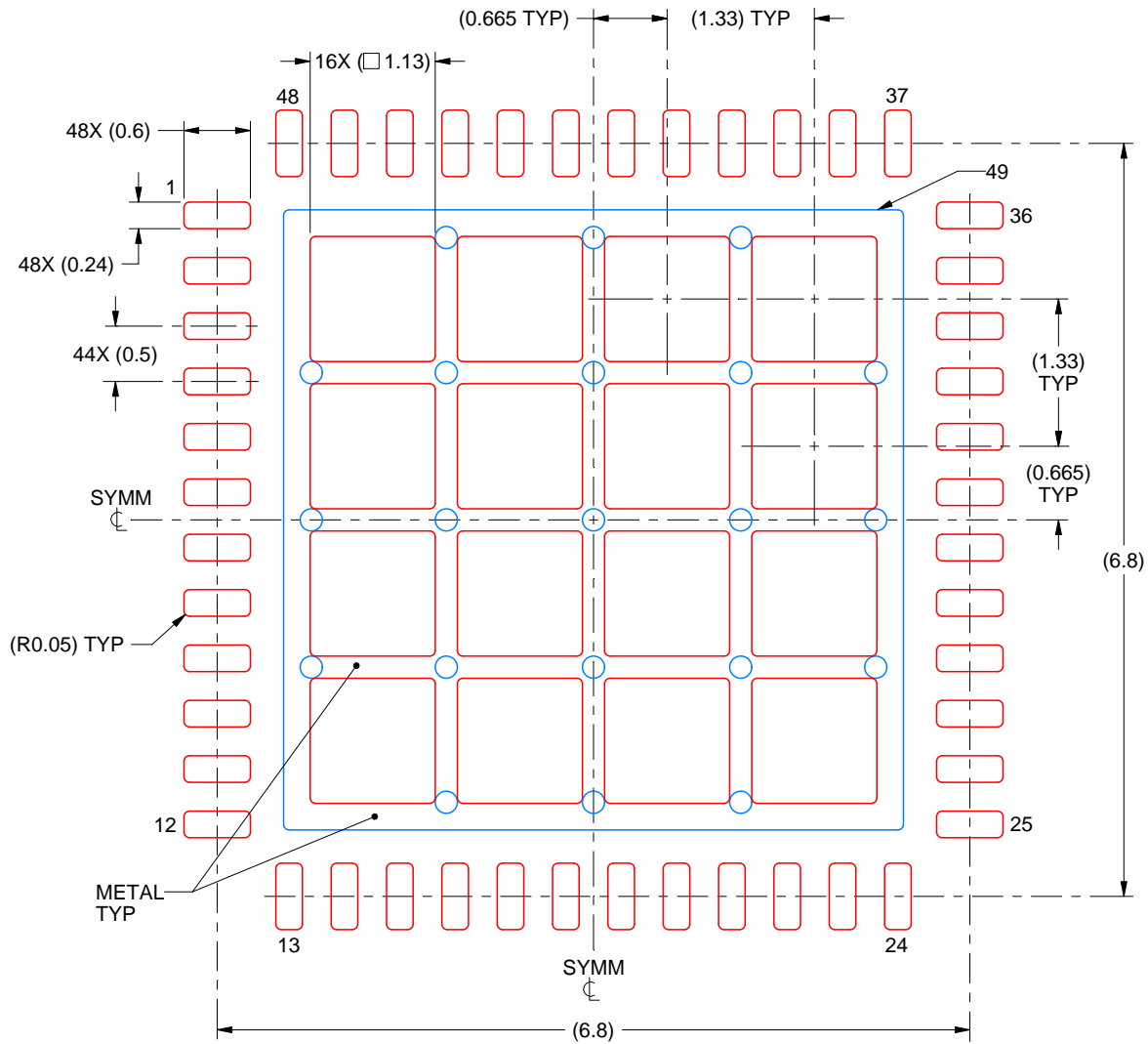
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGZ0048D

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
 66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 SCALE:15X

4219046/B 11/2019

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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