ADC12xJ1600-Q1 クワッド / デュアル / シングル チャネル、1.6GSPS、12 ビット、JESD204C インターフェイス搭載、A/D コンバータ (ADC)

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～+125℃、T_A
- ADC コア:
  - 分解能:12 ビット
  - 最大サンプリング レート:1.6GSPS
  - インターリーブなしのアーキテクチャ
  - 内部ディザリングにより高次高調波を低減
- パフォーマンス仕様 (–1dBFS):
  - SNR (100MHz):57.4dBFS
  - ENOB (100MHz):9.1 ビット
  - SFDR (100MHz):64dBc
  - ノイズ フロア (–20dBFS):–147dBFS
- フルスケール入力電圧:800$mV_{PP-DIFF}$
- フルパワー入力帯域幅:6GHz
- JESD204C シリアル データ インターフェイス
  - 合計 2～8 (クワッド / デュアル チャネル) または 1～4 (シングル チャネル) の SerDes レーン数に対応
  - 最大ボー レート:17.16Gbps
  - 64B/66B と 8B/10B のエンコード モード
  - Subclass-1 サポートによる決定論的レイテンシ
  - JESD204B レシーバと互換
- 内部サンプリング クロック生成のオプション
  - PLL および VCO (7.2～8.2GHz) 内蔵
- SYSREF ウィンドウ処理により同期が簡単
- 4 つのクロック出力によりシステム クロック供給を簡素化
  - FPGA または隣接 ADC 用のリファレンス クロック
  - SerDes トランシーバ用のリファレンス クロック
- パルス式システム用のタイムスタンプ入力および出力
- 消費電力 (1GSPS):
  - クワッド チャネル:477mW/チャネル
  - デュアル チャネル:700mW/チャネル
  - シングル チャネル:1000 mW
- 電源:1.1V、1.9V

2 アプリケーション

- 光学検出および距離測定 (LiDAR)

3 概要

ADC12xJ1600-Q1 は、クワッド、デュアル、シングル チャネル、12 ビット、1.6GSPS の A/D コンバータ (ADC) ファミリです。ADC12xJ1600-Q1 は、低消費電力、高いサンプリング レート、12 ビットの分解能により、光検出および距離測定 (LiDAR) システムに理想的です。ADC12xJ1600-Q1 は車載用アプリケーション向けに認定済みです。

6GHz のフルパワー入力帯域幅 (-3dB) により、周波数変調連続波 (FMCW) LiDAR システムに適した平坦な周波数応答と、パルス ベースのシステムに適した狭いインパルス応答が得られます。このフルパワー入力帯域幅により、L バンドおよび S バンド直接 RF サンプリングも可能です。

システムのハードウェア要件を緩和するため、いくつかのクロック供給機能が内蔵されています (例:サンプリング クロックを生成するための電圧制御発振器 (VCO) を内蔵した内部フェーズ ロック ループ (PLL))。FPGA または ASIC のロジックと SerDes にクロックを供給するために 4 つのクロック出力を備えています。パルス式システムのためにタイムスタンプ入力および出力を備えています。

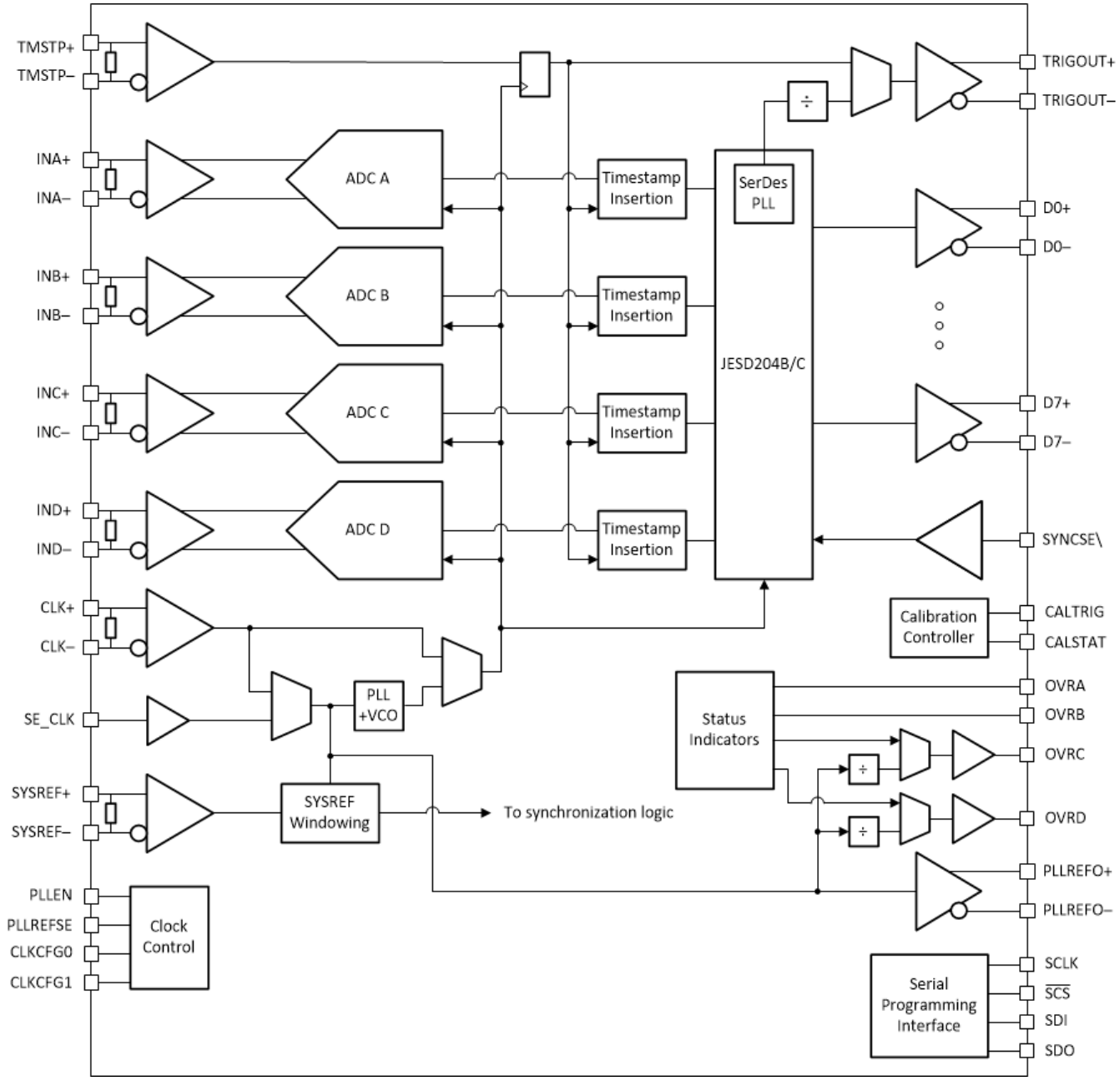
JESD204C シリアル インターフェイスにより、プリント基板 (PCB) の配線の量を減らすことで、システムを小型化できます。インターフェイス モードは、2～8 レーン (デュアル チャネルとクワッド チャネルのデバイスの場合)、または 1～4 レーン (シングル チャネル デバイスの場合) を最大 17.16Gbps の SerDes ボーレートでサポートしているため、各アプリケーションに最適な構成を実現できます。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
ADC12QJ1600-Q1 ADC12DJ1600-Q1 ADC12SJ1600-Q1	FCBGA (144)	10mm × 10mm

(1) 詳細については、セクション 10 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。



クワッド チャネルのブロック図

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4 Pin Configuration and Functions

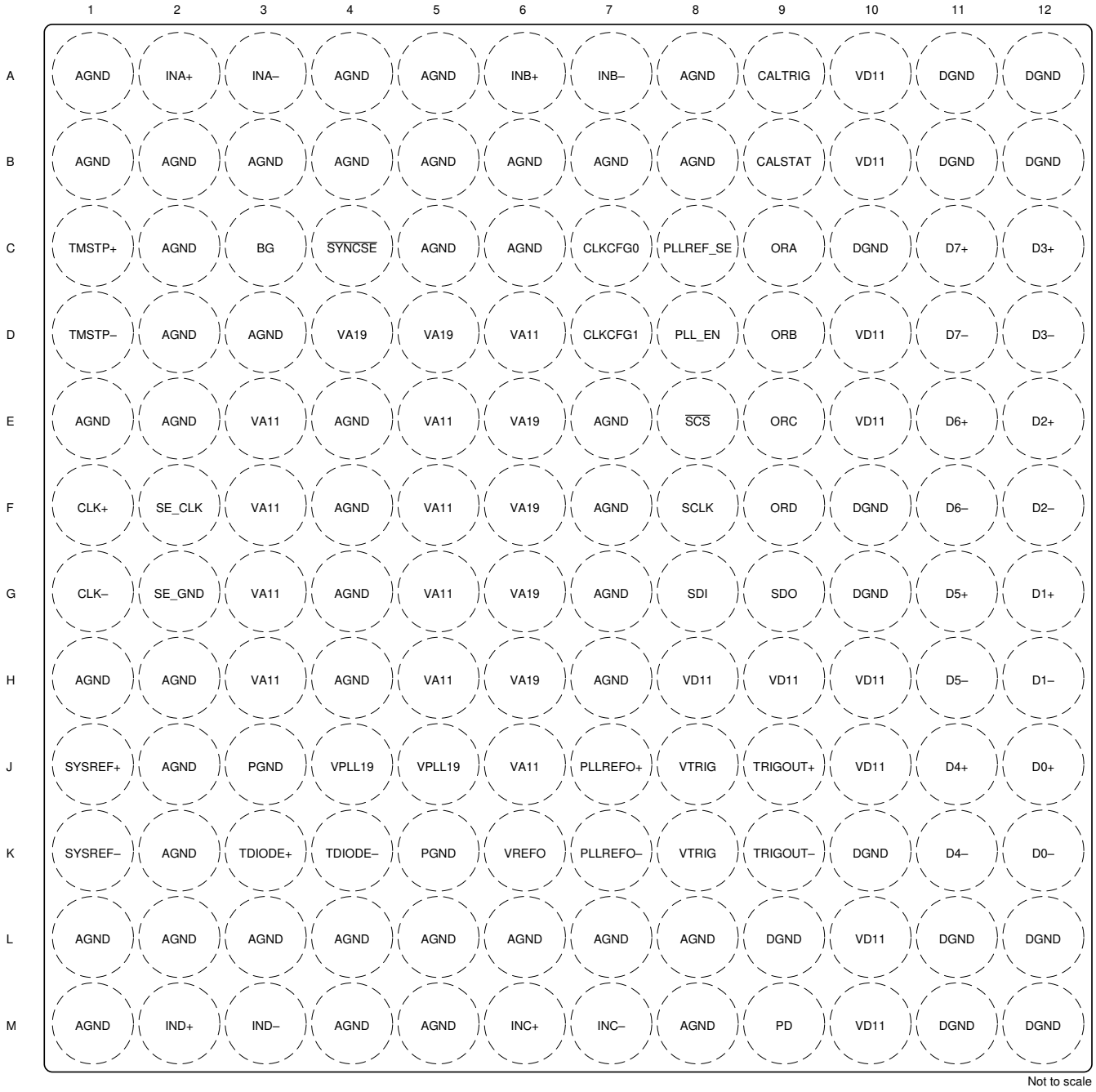

図 4-1. Quad Channel AAV Package, 144-Ball Flip Chip BGA (Top View)

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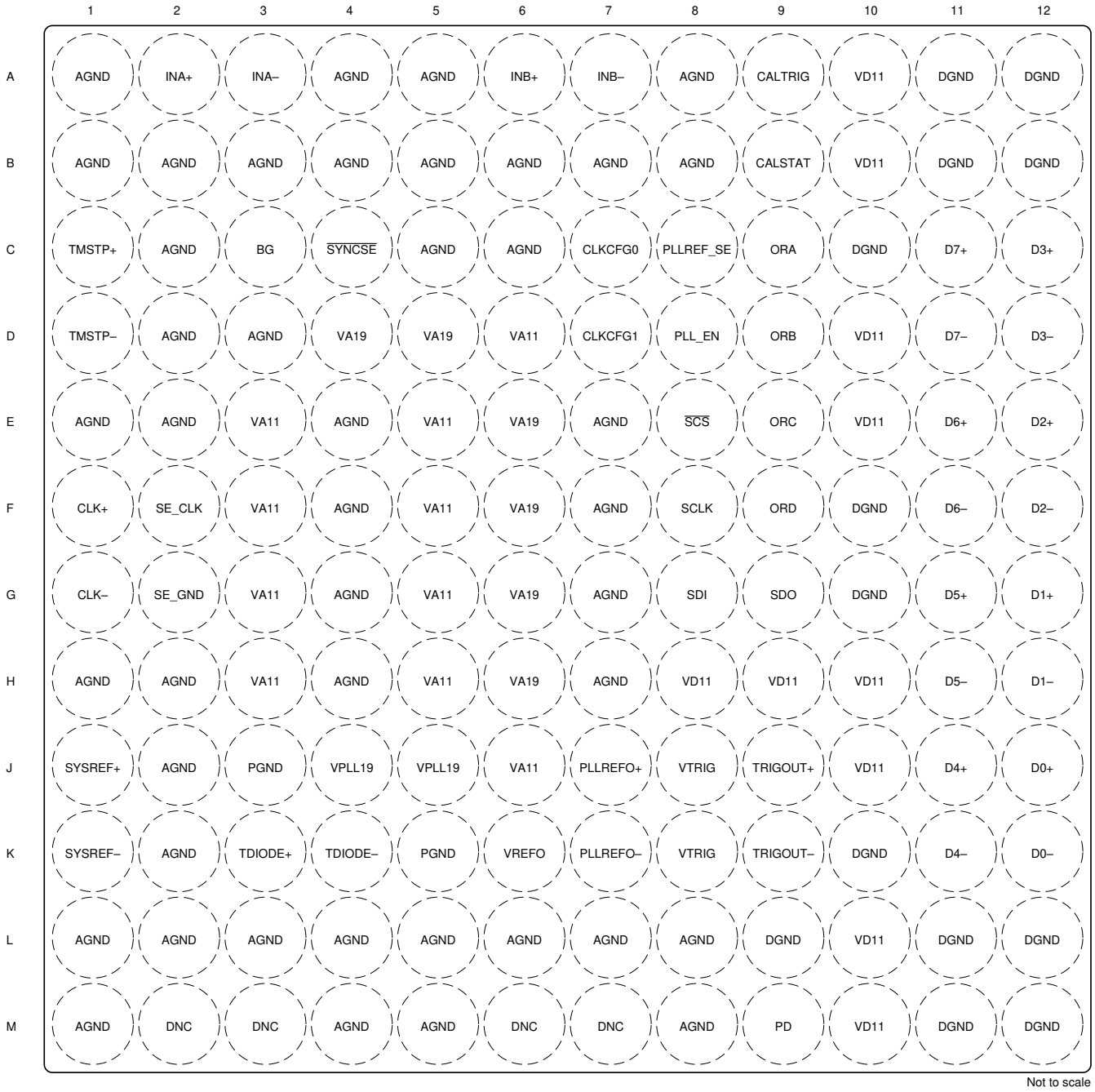

図 4-2. Dual Channel AAV Package, 144-Ball Flip Chip BGA (Top View)

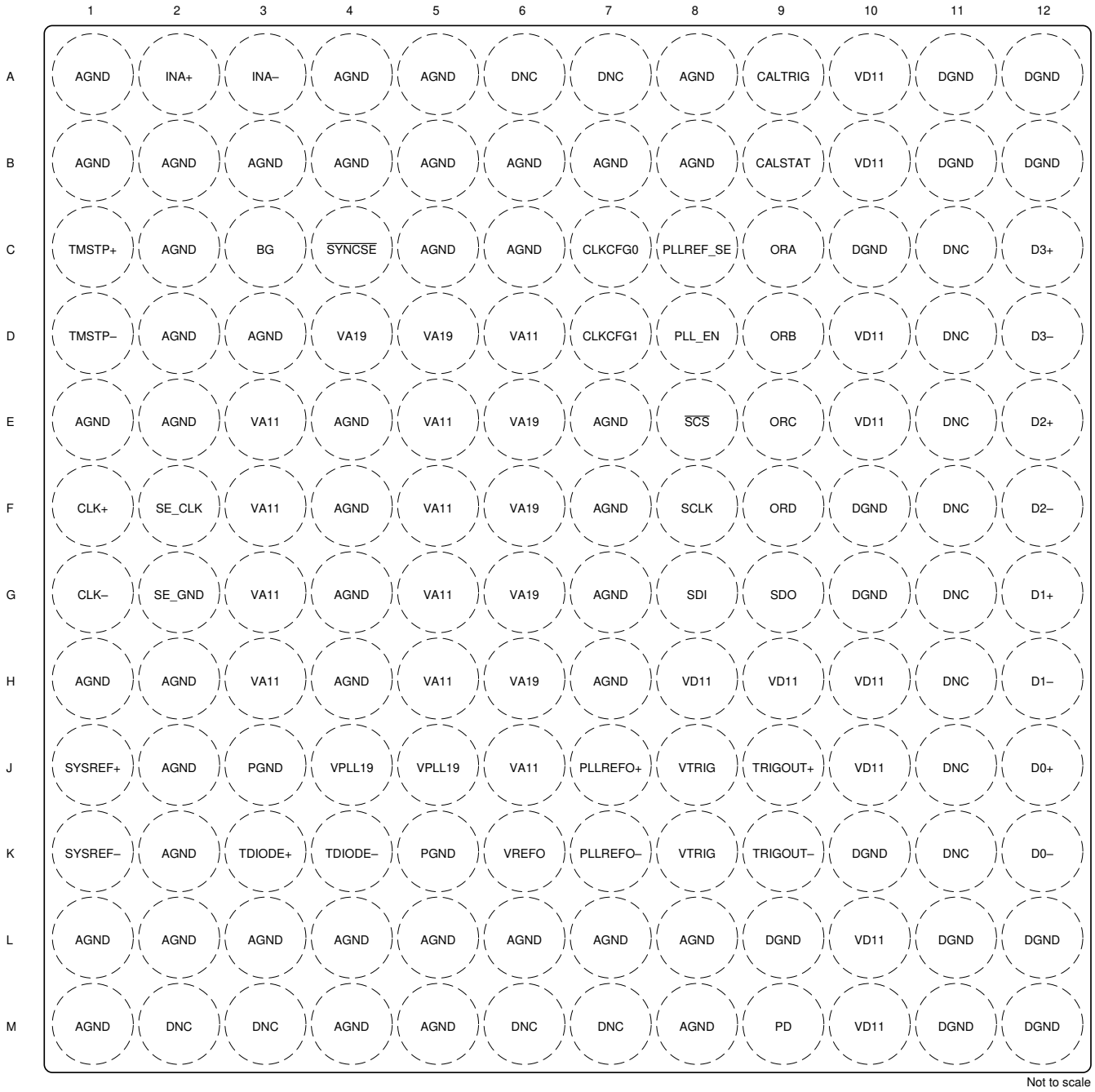

図 4-3. Single Channel AAV Package, 144-Ball Flip Chip BGA (Top View)

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表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1, A4, A5, A8, B1, B2, B3, B4, B5, B6, B7, B8, C2, C5, C6, D2, D3, E1, E2, E4, E7, F4, F7, G4, G7, H1, H2, H4, H7, J2, K2, L1, L2, L3, L4, L5, L6, L7, L8, M1, M4, M5, M8	AGND	—	Analog supply ground. Tie AGND, PGND, SE_GND and DGND to a common ground plane (GND) on the circuit board.
C3	BG	O	Band-gap voltage output. This pin is capable of sourcing only small currents and driving limited capacitive loads, as specified in the *Recommended Operating Conditions* table. This pin can be left disconnected if not used.
B9	CALSTAT	O	Foreground calibration status output or device alarm output. Functionality is programmed through CAL_STATUS_SEL. This pin can be left disconnected if not used.
A9	CALTRIG	I	Foreground calibration trigger input. This pin is only used if hardware calibration triggering is selected in CAL_TRIG_EN, otherwise software triggering is performed using CAL_SOFT_TRIG. Tie this pin to GND if not used.
G1	CLK–	I	Device (sampling) clock negative input or differential PLL reference clock negative input. TI strongly recommends using AC-coupling for best performance. This pin can be left disconnected if SE_CLK is used to apply the reference clock.
F1	CLK+	I	Device (sampling) clock positive input or differential PLL reference clock negative input. The clock signal is strongly recommended to be AC-coupled to this input for best performance. This differential input has an internal 100Ω differential termination and is self-biased to the optimal input common-mode voltage as long as DEVCLK_LVPECL_EN is set to 0. This pin can be left disconnected if SE_CLK is used to apply the reference clock when the PLL is used.
C7	CLKCFG0	I	CLKCFG0 and CLKCFG1 can be used enable additional clock outputs on ORC and ORD when the C-PLL is used (PLL_EN is set high). Tie this pin to ground if not used.
D7	CLKCFG1	I	CLKCFG0 and CLKCFG1 can be used enable additional clock outputs on ORC and ORD when the C-PLL is used (PLL_EN is set high). Tie this pin to ground if not used.
K12	D0–	O	High-speed serialized data output for lane 0, negative connection. This pin can be left disconnected if not used.
J12	D0+	O	High-speed serialized data output for lane 0, positive connection. This differential output must be AC-coupled and must always be terminated with a 100Ω differential termination at the receiver. This pin can be left disconnected if not used.
H12	D1–	O	High-speed serialized data output for lane 1, negative connection. This pin can be left disconnected if not used.
G12	D1+	O	High-speed serialized data output for lane 1, positive connection. This differential output must be AC-coupled and must always be terminated with a 100Ω differential termination at the receiver. This pin can be left disconnected if not used.
F12	D2–	O	High-speed serialized data output for lane 2, negative connection. This pin can be left disconnected if not used.
E12	D2+	O	High-speed serialized data output for lane 2, positive connection. This differential output must be AC-coupled and must always be terminated with a 100Ω differential termination at the receiver. This pin can be left disconnected if not used.
D12	D3–	O	High-speed serialized data output for lane 3, negative connection. This pin can be left disconnected if not used.
C12	D3+	O	High-speed serialized data output for lane 3, positive connection. This differential output must be AC-coupled and must always be terminated with a 100Ω differential termination at the receiver. This pin can be left disconnected if not used.
K11	D4-	O	High-speed serialized data output for lane 4, negative connection. Not used for single channel devices. This pin can be left disconnected if not used.
J11	D4+	O	High-speed serialized data output for lane 4, positive connection. Not used for single channel devices. This differential output must be AC-coupled and must always be terminated with a 100Ω differential termination at the receiver. This pin can be left disconnected if not used.
H11	D5-	O	High-speed serialized data output for lane 5, negative connection. Not used for single channel devices. This pin can be left disconnected if not used.
G11	D5+	O	High-speed serialized data output for lane 5, positive connection. Not used for single channel devices. This differential output must be AC-coupled and must always be terminated with a 100Ω differential termination at the receiver. This pin can be left disconnected if not used.
F11	D6-	O	High-speed serialized data output for lane 6, negative connection. Not used for single channel devices. This pin can be left disconnected if not used.
E11	D6+	O	High-speed serialized data output for lane 6, positive connection. Not used for single channel devices. This differential output must be AC-coupled and must always be terminated with a 100Ω differential termination at the receiver. This pin can be left disconnected if not used.

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表 4-1. Pin Functions (続き)

PIN		I/O	DESCRIPTION
NO.	NAME		
D11	D7-	O	High-speed serialized data output for lane 7, negative connection. Not used for single channel devices. This pin can be left disconnected if not used.
C11	D7+	O	High-speed serialized data output for lane 7, positive connection. Not used for single channel devices. This differential output must be AC-coupled and must always be terminated with a 100Ω differential termination at the receiver. This pin can be left disconnected if not used.
A11, A12, B11, B12, C10, F10, G10, K10, L9, L11, L12, M11, M12	DGND	—	Digital supply ground. Tie AGND, PGND, SE_GND and DGND to a common ground plane (GND) on the circuit board.
A3	INA–	I	Channel A analog input negative connection for quad, dual and single channel devices. See INA+ for detailed description. This input is terminated to VA11 through a 50-Ω termination resistor. This pin can be left disconnected if not used.
A2	INA+	I	Channel A analog input positive connection for quad, dual and single channel devices. The differential full-scale input voltage is determined by the FS_RANGE register (see the *Full-Scale Voltage (VFS) Adjustment* section). This input is terminated to VA11 through a 50Ω termination resistor. The input common-mode voltage is internally self-biased to VA11 (1.1 V nominally) and must follow the recommendations in the *Recommended Operating Conditions* table. This input can be AC coupled to the source if DC signals are not required. If DC signals are required then a DC-coupled fully differential driving amplifier must be used with its output common-mode voltage set to the VA11 supply voltage. This pin can be left disconnected if not used.
A7	INB–	I	Channel B analog input negative connection for quad and dual channel devices. Do not connect for single channel device. See INB+ for detailed description. This input is terminated to VA11 through a 50Ω termination resistor. This pin can be left disconnected if not used.
A6	INB+	I	Channel B analog input positive connection for quad and dual channel devices. Do not connect for single channel device. The differential full-scale input voltage is determined by the FS_RANGE register (see the *Full-Scale Voltage (VFS) Adjustment* section). This input is terminated to VA11 through a 50Ω termination resistor. The input common-mode voltage is internally self-biased to VA11 (1.1 V nominally) and must follow the recommendations in the *Recommended Operating Conditions* table. This input can be AC coupled to the source if DC signals are not required. If DC signals are required then a DC-coupled fully differential driving amplifier must be used with its output common-mode voltage set to the VA11 supply voltage. This pin can be left disconnected if not used.
M7	INC–	I	Channel C analog input negative connection for quad channel device. Do not connect for single and dual channel devices. See INC+ for detailed description. This input is terminated to VA11 through a 50Ω termination resistor. This pin can be left disconnected if not used.
M6	INC+	I	Channel C analog input positive connection for quad channel device. Do not connect for single and dual channel devices. The differential full-scale input voltage is determined by the FS_RANGE register (see the *Full-Scale Voltage (VFS) Adjustment* section). This input is terminated to VA11 through a 50Ω termination resistor. The input common-mode voltage is internally self-biased to VA11 (1.1V nominally) and must follow the recommendations in the *Recommended Operating Conditions* table. This input can be AC coupled to the source if DC signals are not required. If DC signals are required then a DC-coupled fully differential driving amplifier must be used with its output common-mode voltage set to the VA11 supply voltage. This pin can be left disconnected if not used.
M3	IND–	I	Channel D analog input negative connection for quad channel device. Do not connect for single and dual channel devices. See IND+ for detailed description. This input is terminated to VA11 through a 50Ω termination resistor. This pin can be left disconnected if not used.
M2	IND+	I	Channel D analog input positive connection for quad channel device. Do not connect for single and dual channel devices. The differential full-scale input voltage is determined by the FS_RANGE register (see the *Full-Scale Voltage (VFS) Adjustment* section). This input is terminated to VA11 through a 50Ω termination resistor. The input common-mode voltage is internally self-biased to VA11 (1.1V nominally) and must follow the recommendations in the *Recommended Operating Conditions* table. This input can be AC coupled to the source if DC signals are not required. If DC signals are required then a DC-coupled fully differential driving amplifier must be used with its output common-mode voltage set to the VA11 supply voltage. This pin can be left disconnected if not used.
C9	ORA	O	Fast over-range detection status output for channel A. When the analog input for channel A exceeds the threshold programmed into OVR_T, this status indicator goes high. The minimum pulse duration is set by OVR_N. See the *ADC Overrange Detection* section for more information. This pin can be left disconnected if not used.
D9	ORB	O	Fast over-range detection status output for channel B. Only used for quad and dual channel devices. Do not connect for single channel device. When the analog input for channel B exceeds the threshold programmed into OVR_T, this status indicator goes high. The minimum pulse duration is set by OVR_N. See the *ADC Overrange Detection* section for more information. This pin can be left disconnected if not used.

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表 4-1. Pin Functions (続き)

PIN		I/O	DESCRIPTION
NO.	NAME		
E9	ORC	O	Fast over-range detection status output for channel C or additional clock output. The fast over-range detection function is only available for quad channel device. When the analog input for channel C exceeds the threshold programmed into OVR_T, this status indicator goes high. The minimum pulse duration is set by OVR_N. See the *ADC Overrange Detection* section for more information. This pin can alternatively be used as an additional clock output (DIVREF_C) when enabled by CLKCFG[1:0] or through the SPI register configuration and when PLL_EN is high. When CLKCFG0 and CLKCFG1 are both set low (or disabled through SPI) the ORC output is used to output the over-range signal for ADC channel C.ORC can be programmed as a copy of PLLREFO (CLKCFG[1:0] = 0x1) or as a divide-by-2 (CLKCFG[1:0] = 0x2) or divide-by-4 (CLKCFG[1:0] = 0x3) copy of PLLREFO. The clock at ORC is available at device power up if PLL_EN is set high, PD is set low and CLKCFG[1:0] are configured appropriately. This pin can be left disconnected if not used.
F9	ORD	O	Fast over-range detection status output for channel D or additional clock output. The fast over-range detection function is only available for quad channel device. When the analog input for channel D exceeds the threshold programmed into OVR_T, this status indicator goes high. The minimum pulse duration is set by OVR_N. See the *ADC Overrange Detection* section for more information. This pin can alternatively be used as an additional clock output (DIVREF_D) when enabled by CLKCFG[1:0] or through the SPI register configuration and when PLL_EN is high. When CLKCFG0 and CLKCFG1 are both set low (or disabled through SPI) the ORD output is used to output the over-range signal for ADC channel D.ORD can be programmed as a copy of PLLREFO when any or both of CLKCFG[1:0] are set which will be available at start up if PLL_EN is set high and PD is held low. ORD can be set as a divide-by-2 or divide-by-4 copy of PLLREFO when overridden through the SPI register. A clock out of ORD is only available if a clock is also output from ORC. If only one clock is required then use ORC. This pin can be left disconnected if not used.
M9	PD	I	CMOS input to power down the device for power savings or temperature diode calibration. Setting PD high disables PLLREFO and the ORC and ORD clock outputs and therefore this pin should not be used if these clocks are critical for system operation. Tie this pin to GND if not used.
J3, K5	PGND	—	PLL supply ground. Tie AGND, PGND, SE_GND and DGND to a common ground plane (GND) on the circuit board.
D8	PLL_EN	I	CMOS input to enable the internal PLL for sampling clock generation if set high or to disable and bypass the PLL if set low. Tie this pin to GND if PLL is not used.
C8	PLLREF_SE	I	CMOS input to select the single-ended PLL reference clock input (SE_CLK) if set high or the differential clock input (CLK±) if set low. Only CLK± can be used for the sampling clock if the PLL is disabled. Tie this pin to GND if the PLL is not used or if CLK± is used as the reference clock input.
K7	PLLREFO–	O	Negative LVDS PLL reference clock output. The clock is repeated from the selected PLL reference clock input (CLK± or SE_CLK). It is available at device power up to clock other devices when PLL_EN is set high and PD is held low. This pin can be left disconnected if not used.
J7	PLLREFO+	O	Positive LVDS PLL reference clock output. The clock is repeated from the selected PLL reference clock input (CLK± or SE_CLK). It is available at device power up to clock other devices when PLL_EN is set high and PD is held low. This pin can be left disconnected if not used.
F8	SCLK	I	Serial interface clock. This pin functions as the serial-interface clock input that clocks the serial programming data in and out. The *Using the Serial Interface* section describes the serial interface in more detail. Supports 1.1V to 1.9V CMOS levels.
E8	$\overline{\text{SCS}}$	I	Serial interface chip select active low input. The *Using the Serial Interface* section describes the serial interface in more detail. Supports 1.1V to 1.9V CMOS levels. This pin has a 82kΩ pull-up resistor to VD11.
G8	SDI	I	Serial interface data input. The *Using the Serial Interface* section describes the serial interface in more detail. Supports 1.1V to 1.9V CMOS levels.
G9	SDO	O	Serial interface data output. The *Using the Serial Interface* section describes the serial interface in more detail. This pin is high impedance during normal device operation. This pin outputs 1.9V CMOS levels during serial interface read operations. This pin can be left disconnected if not used.
F2	SE_CLK	I	Single-ended PLL reference clock input. This input is selected when PLL_EN is held high and PLLREF_SE is held high. When PLLREF_SE is set low, CLK± is used as the differential PLL reference input. This pin should be tied to GND if not used.
G2	SE_GND	—	Ground reference for single-ended PLL reference clock input. Tie AGND, PGND, SE_GND and DGND to a common ground plane (GND) on the circuit board.
C4	$\overline{\text{SYNCSE}}$	I	Single-ended JESD204C SYNC signal. This input is an active low input that is used to initialize the JESD204C serial link in 8B/10B modes when SYNC_SEL is set to 0. The 64B/66B modes do not use the SYNC signal. When toggled low in 8B/10B modes this input initiates code group synchronization (see the *Code Group Synchronization (CGS)* section). After code group synchronization, this input must be toggled high to start the initial lane alignment sequence (see the *Initial Lane Alignment Sequence (ILAS)* section). Tie this pin to ground if TMSTP± or JSYNC_N is used as the JESD204C SYNC signal or for 64B/66B encoded JESD204C modes.
K1	SYSREF–	I	SYSREF negative input. Leave this pin disconnected if not used and power down the SYSREF± receiver using SYSREF_RECV_EN.

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表 4-1. Pin Functions (続き)

PIN		I/O	DESCRIPTION
NO.	NAME		
J1	SYSREF+	I	The SYSREF positive input is used to achieve synchronization and deterministic latency across the JESD204C interface. This differential input (SYSREF+ to SYSREF–) has an internal untrimmed 100Ω differential termination and can be AC-coupled when SYSREF_LVPECL_EN is set to 0. This input is self-biased when SYSREF_LVPECL_EN is set to 0. The termination changes to 50Ω to ground on each input pin (SYSREF+ and SYSREF–) and can be DC-coupled when SYSREF_LVPECL_EN is set to 1. This input is not self-biased when SYSREF_LVPECL_EN is set to 1 and must be biased externally to the input common-mode voltage range provided in the *Recommended Operating Conditions* table. Leave this pin disconnected if not used and power down the SYSREF± receiver using SYSREF_RECV_EN.
K4	TDIODE–	I	Temperature diode negative (cathode) connection. This pin can be left disconnected if not used.
K3	TDIODE+	I	Temperature diode positive (anode) connection. An external temperature sensor can be connected to TDIODE+ and TDIODE– to monitor the junction temperature of the device. This pin can be left disconnected if not used.
D1	TMSTP–	I	Timestamp input negative connection. This pin can be left disconnected and the TMSTP receiver powered down (TMSTP_RECV_EN = 0) if timestamp is not required.
C1	TMSTP+	I	Timestamp input positive connection. This input is a timestamp input, used to mark a specific sample, when TIME_STAMP_EN is set to 1. For additional usage information, see the *Timestamp* section. TMSTP_RECV_EN must be set to 1 to use this input. This differential input (TMSTP+ to TMSTP–) has an internal untrimmed 100-Ω differential termination and can be AC-coupled when TMSTP_LVPECL_EN is set to 0. The termination changes to 50Ω to ground on each input pin (TMSTP+ and TMSTP–) and can be DC coupled when TMSTP_LVPECL_EN is set to 1. This pin is not self-biased and therefore must be externally biased for both AC- and DC-coupled configurations. The common-mode voltage must be within the range provided in the *Recommended Operating Conditions* table when both AC and DC coupled. Can also be used as a differential $\overline{\text{SYNC}}$ input for the JESD204C interface with 8b/10b encoding. This pin can be left disconnected and the TMSTP receiver powered down (TMSTP_RECV_EN = 0) if timestamp is not required.
K9	TRIGOUT–	O	Negative LVDS output for trigger repeated from TMSTP± or clock output generated from the SerDes PLL. This output can be enabled by setting TRIGOUT_EN to 1 and configured by TRIGOUT_MODE. Setting the PD pin high disables this output. This pin can be left disconnected if not used.
J9	TRIGOUT+	O	Positive LVDS output for trigger repeated from TMSTP± or clock output generated from the SerDes PLL. This output can be enabled by setting TRIGOUT_EN to 1 and configured by TRIGOUT_MODE. Setting the PD pin high disables this output. This pin can be left disconnected if not used.
D6, E3, E5, F3, F5, G3, G5, H3, H5, J6	VA11	—	1.1V analog supply
D4, D5, E6, F6, G6, H6	VA19	—	1.9V analog supply
A10, B10, D10, E10, H8, H9, H10, J10, L10, M10	VD11	—	1.1V digital supply
J4, J5	VPLL19	—	1.9V supply for internal PLL and VCO
K6	VREFO	—	1.9V supply for PLLREFO± output driver and PLL charge pump
J8, K8	VTRIG	—	1.1V to 1.9V supply for TRIGOUT± output driver

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage range	VA19(2)	–0.3	2.35	V
	VPLL19(3)	–0.3	2.35	
	VREFO(2)	–0.3	2.35	
	VTRIG(5)	–0.3	2.35	
	VA11(2)	–0.3	1.32(11)	
	VD11(5)	–0.3	1.32(11)	
	Voltage difference between any 1.9 V supply (VA19, VPLL19 or VREFO)	–0.5	0.5	
Voltage between AGND, DGND, PGND and SE_GND		–0.1	0.1	V
Pin voltage range	D[7 :0]+, D[7 :0]–, TMSTP+, TMSTP–(5)	–0.5	VD11 + 0.5(7)	V
	CLK+, CLK–, SYSREF+, SYSREF–(2)	–0.5	VA11 + 0.5(6)	
	SE_CLK(4)	–0.5	VA19 + 0.5(8)	
	PLLREFO+, PLLREFO–(2)	–0.5	VREFO + 0.5(9)	
	TRIGOUT+,TRIGOUT–(5)	–0.5	VTRIG + 0.5(10)	
	BG, TDIODE+, TDIODE–(2)	–0.5	VA19 + 0.5(8)	
	INA+, INA–, INB+, INB– , INC+, INC–, IND+, IND– (2)	VA11 – 1.0	VA11 + 1.0	
	CALSTAT, CALTRIG, CLKCFG0, CLKCFG1, PLL_EN, PLLREF_SE, ORA, ORB, ORC, ORD, PD, SCLK, $\overline{SCS}$, SDI, SDO, $\overline{SYNCSE}$ (2)	–0.5	VA19 + 0.5(8)	
Peak input current (any input except INA+, INA–, INB+, INB– , INC+, INC–, IND+, IND–)		–25	25	mA
Peak input current (INA+, INA–, INB+, INB– , INC+, INC–, IND+, IND–)		–50	50	mA
Peak RF input power (INA+, INA–, INB+, INB– , INC+, INC–, IND+, IND–)	Single-ended with Z_{S-SE} = 50 Ω		16.4	dBm
Peak total input current (sum of absolute value of all currents forced in or out, not including power-supply current)			100	mA
Operating junction temperature, T_j		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Measured to AGND.
(3) Measured to PGND.
(4) Measured to SE_GND.
(5) Measured to DGND.
(6) Maximum voltage not to exceed VA11 absolute maximum rating.
(7) Maximum voltage not to exceed VD11 absolute maximum rating.
(8) Maximum voltage not to exceed VA19 absolute maximum rating.
(9) Maximum voltage not to exceed VREFO absolute maximum rating.
(10) Maximum voltage not to exceed VTRIG absolute maximum rating.
(11) The 1.1-V supplies (VA11, VD11) must not be more than 0.5 V above any of the 1.9-V supplies (VA19, VPLL19, VREFO) or VTRIG (1.1 V or 1.9 V) during power up, normal operation or power down. See *Power Sequencing* section.

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5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	4000	V
		Charged-device model (CDM), per AEC Q100-011	750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage range	VA19, analog 1.9-V supply(2)	1.8	1.9	2.0	V
		VPLL19, PLL supply(3)	1.8	1.9	2.0	
		VREFO, PLLREFO± and PLL charge pump supply(2)	1.8	1.9	2.0	
		VTRIG, TRIGOUT± supply(4)	1.05	1.1 or 1.9	2.0	
		VA11, analog 1.1-V supply(2)	1.05	1.1	1.15	
		VD11, digital 1.1-V supply(4)	1.05	1.1	1.15	
V_{CMI}	Input common-mode voltage	INA+, INA–, INB+, INB– , INC+, INC–, IND+, IND– (2)	1.05	1.1	1.15	V
		CLK+, CLK–, SYSREF+, SYSREF–(2) (5)	0	0.3	0.55	
		TMSTP+, TMSTP–(4) (6)	0	0.3	0.55	
$V_{ID(DIFF)}$	Input voltage, peak-to-peak differential	CLK+ to CLK–, SYSREF+ to SYSREF–, TMSTP+ to TMSTP–	0.4	1.0	2.0	$V_{PP-DIFF}$
		INA+, INA–, INB+, INB– , INC+, INC–, IND+, IND–			1.0(7)	
V_{IH}	High-level input voltage	SE_CLK	0.9	1.8		V
V_{IL}	Low-level input voltage	SE_CLK		0	0.3	V
I_{C_TD}	Temperature diode input current	TDIODE+ to TDIODE–		100		µA
C_L	BG maximum load capacitance				50	pF
I_O	BG maximum output current	Current at -2% drop from nominal voltage		140		µA
T_A	Operating free-air temperature		–40		125	°C
Tj	Operating junction temperature				140(1)	°C

(1) Prolonged use above a junction temperature of 105°C may increase the device failure-in-time (FIT) rate.
(2) Measured to AGND.
(3) Measured to PGND.
(4) Measured to DGND.
(5) TI strongly recommends that CLK± be AC-coupled with DEVCLK_LVPECL_EN set to 0 to allow CLK± to self-bias to the optimal input common-mode voltage for best performance. TI recommends AC-coupling for SYSREF± unless DC-coupling is required, in which case, the LVPECL input mode must be used (SYSREF_LVPECL_EN = 1).
(6) TMSTP± does not have internal biasing that requires TMSTP± to be biased externally whether AC-coupled with TMSTP_LVPECL_EN = 0 or DC-coupled with TMSTP_LVPECL_EN= 1.
(7) The ADC output code saturates when V_{ID} for INA± or INB± exceeds the programmed full-scale voltage(V_{FS}) set by FS_RANGE_A for INA± or FS_RANGE_B for INB±.

5.4 Thermal Information

THERMAL METRIC(1)		ADC12QJ1600-Q1 AAV (FCBGA) 144 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	20.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	1.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.54	°C/W

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THERMAL METRIC(1)		ADC12QJ1600-Q1 AAV (FCBGA) 144 PINS	UNIT
ψ_{JT}	Junction-to-top characterization parameter	0.21	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.52	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance (n/a)	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics: DC Specifications

typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *セクション 5.3* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DC ACCURACY						
	Resolution	Resolution with no missing codes		12		Bits
DNL	Differential nonlinearity	Maximum positive excursion from ideal step size		0.2		LSB
		Maximum negative excursion from ideal step size		–0.19		
INL	Integral nonlinearity	Maximum positive excursion from ideal transfer function		1.9		LSB
		Maximum negative excursion from ideal transfer function		–1.6		
ANALOG INPUTS (INA+, INA–, INB+, INB– , INC+, INC–, IND+, IND–)						
V_{OFF}	Offset error	CAL_OS = 0		±0.4		mV
		CAL_OS = 1		±0.4		mV
V_{OFF_ADJ}	Input offset voltage adjustment range	Available offset correction range (see OFSx or OFSxCh registers)		±33		mV
V_{OFF_DRIFT}	Offset drift	Foreground calibration at nominal temperature only, CAL_OS = 1		-1.2		µV/°C
		Foreground calibration at each temperature, CAL_OS = 1		0.25		
V_{FS}	Analog differential input full-scale range	Default full-scale voltage (FS_RANGE = 0xA000), measured at DC	750	800	850	mV_{PP}
		Maximum full-scale voltage (FS_RANGE = 0xFFFF), measured at DC	980	1040		
		Minimum full-scale voltage (FS_RANGE = 0x2000), measured at DC		480	500	
V_{FS_DRIFT}	Analog differential input full-scale range drift	Default FS_RANGE setting, foreground calibration at nominal temperature only, inputs driven by a 50-Ω source, includes effect of R_{IN} drift		–0.0015		%/°C
		Default FS_RANGE setting, foreground calibration at each temperature, inputs driven by a 50-Ω source, includes effect of R_{IN} drift		-.000018		
V_{FS_MATCH}	Analog differential input full-scale range matching	Matching between any two channels (e.g. INA± and INB±), default full-scale voltage, measured at DC		1%		
R_{IN}	Differential input resistance	Center of differential resistance is terminated to V_{CM}, measured at T_A = 25°C	92	100	108	Ω
R_{IN_TEMPCO}	Input termination linear temperature coefficient			38		mΩ/°C
C_{IN}	Single-ended input capacitance	Measured at DC		0.6		pF
TEMPERATURE DIODE CHARACTERISTICS (TDIODE+, TDIODE–)						
ΔV_{BE}	Temperature diode voltage slope	Forced forward current of 100 µA. Offset voltage (approximately 0.792 V at 0°C) varies with process and must be measured for each part. Offset measurement must be done with the device unpowered or with the PD pin asserted to minimize device self-heating.		–1.6		mV/°C
BAND-GAP VOLTAGE OUTPUT (BG)						

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typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *セクション 5.3* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BG}	Internal band-gap reference and V_{CM} reference output voltage	I_L ≤ 100 µA		1.1		V
V_{BG_DRIFT}	V_{BG} output temperature drift	I_L ≤ 100 µA		–117		µV/°C
DIFFERENTIAL CLOCK AND TIMESTAMP INPUTS (CLK+, CLK–, SYSREF+, SYSREF–, TMSTP+, TMSTP–)						
Z_T	Internal termination	Differential termination with DEVCLK_LVPECL_EN = 0, SYSREF_LVPECL_EN = 0, and TMSTP_LVPECL_EN = 0		100		Ω
		Single-ended termination to GND (per pin) with DEVCLK_LVPECL_EN = 0, SYSREF_LVPECL_EN = 0, and TMSTP_LVPECL_EN = 0		50		
V_{CM}	Input common-mode voltage, self-biased	Self-biasing common-mode voltage for CLK± when AC-coupled (DEVCLK_LVPECL_EN must be set to 0)		0.3		V
		Self-biasing common-mode voltage for SYSREF± when AC-coupled (SYSREF_LVPECL_EN must be set to 0) and with receiver enabled (SYSREF_RECV_EN = 1)		0.3		
		Self-biasing common-mode voltage for SYSREF± when AC-coupled (SYSREF_LVPECL_EN must be set to 0) and with receiver disabled (SYSREF_RECV_EN = 0)		VA11		
C_{L_DIFF}	Differential input capacitance	Between positive and negative differential input pins		0.1		pF
C_{L_SE}	Single-ended input capacitance	Each input to ground		0.5		pF
CLOCK AND TRIGGER OUTPUTS (PLLREFO+, PLLREFO–, TRIGOUT+, TRIGOUT–)						
V_{DIFF}	Differential output voltage, peak-to-peak, DC measurement	100-Ω load	400	720	900	$mV_{PP-DIFF}$
$V_{CM(PLLREFO)}$	PLLREFO± output common-mode voltage			1.37[1]		V
$V_{CM(TRIGOUT)}$	TRIGOUT± output common-mode voltage, tracks with VTRIG	VTRIG = 1.9		1.34[2]		V
		VTRIG = 1.1		0.5[2]		
Z_{DIFF}	Differential output impedance	Measured at DC		300		Ω
SERDES OUTPUTS (D[7 :0]+, D[7 :0]–)						
V_{OD}	Differential output voltage, peak-to-peak	100-Ω load		600		$mV_{PP-DIFF}$
V_{CM}	Output common-mode voltage	AC coupled		.5		V
Z_{DIFF}	Differential output impedance			100		Ω
CMOS INTERFACE (SCLK, SDI, SDO, $\overline{SCS}$, PD, CALSTAT, CALTRIG, CLKCFG0, CLKCFG1, PLL_EN, PLLREF_SE, ORA, ORB, ORC, ORD, $\overline{SYNCSE}$)						
V_{IH}	High-level input voltage		0.7			V
V_{IL}	Low-level input voltage				0.45	V
I_{IH}	High-level input current				40	µA
I_{IL}	Low-level input current		–40			µA

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typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *セクション 5.3* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_I	Input capacitance			2		pF
V_{OH}	High-level output voltage	I_{LOAD} = –400 µA	1.65			V
V_{OL}	Low-level output voltage	I_{LOAD} = 400 µA			150	mV

(1) TI recommends AC-coupling PLLREFO± to the load device when PLLREFO± is enabled.
(2) TI recommends AC-couping TRIGOUT± to the load device when TRIGOUT± is enabled and used as a clock output (from S-PLL). TRIGOUT± can be DC-coupled to the load device when TRIGOUT± is used as a trigger output (from TMSTP±).

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5.6 ADC12xJ1600-Q1: Electrical Characteristics: Power Consumption

Typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *セクション 5.3* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VA19}	1.9-V analog supply current	Power mode 1a: Quad channel, JMODE 0 (12-bit, 8 lanes, 8B/10B encoding), FG calibration, PLL_EN = 0, f_S = 1.6 GSPS, High Performance Mode		645		mA
I_{VPLL19}	PLL analog supply current			0		mA
I_{VREFO}	PLLREFO± analog supply current			0		mA
I_{VTRIG}	TRIGOUT± analog supply current			0		mA
I_{VA11}	1.1-V analog supply current			628		mA
I_{VD11}	1.1-V digital supply current			719		mA
P_{DIS}	Power dissipation			2.71		W
I_{VA19}	1.9-V analog supply current	Power mode 1b: Dual channel, JMODE 0 (12-bit, 4 lanes, 8B/10B encoding), FG calibration, PLL_EN = 0, f_S = 1.6 GSPS, High Performance Mode		385		mA
I_{VPLL19}	PLL analog supply current			0		mA
I_{VREFO}	PLLREFO± analog supply current			0		mA
I_{VTRIG}	TRIGOUT± analog supply current			0		mA
I_{VA11}	1.1-V analog supply current			506		mA
I_{VD11}	1.1-V digital supply current			431		mA
P_{DIS}	Power dissipation			1.76		W
I_{VA19}	1.9-V analog supply current	Power mode 1c: Single channel, JMODE 0 (12-bit, 2 lanes, 8B/10B encoding), FG calibration, PLL_EN = 0, f_S = 1.6 GSPS, High Performance Mode		253		mA
I_{VPLL19}	PLL analog supply current			0		mA
I_{VREFO}	PLLREFO± analog supply current			0		mA
I_{VTRIG}	TRIGOUT± analog supply current			0		mA
I_{VA11}	1.1-V analog supply current			471		mA
I_{VD11}	1.1-V digital supply current			265		mA
P_{DIS}	Power dissipation			1.29		W
I_{VA19}	1.9-V analog supply current	Power mode 2a: Quad channel, JMODE 8 (12-bit, 4 lanes, 64B/66B encoding), LPBG calibration, PLL_EN = 0, f_S = 1.0 GSPS, Low Power Mode		558		mA
I_{VPLL19}	PLL analog supply current			0		mA
I_{VREFO}	PLLREFO± analog supply current			0		mA
I_{VTRIG}	TRIGOUT± analog supply current			0		mA
I_{VA11}	1.1-V analog supply current			394		mA
I_{VD11}	1.1-V digital supply current			384		mA
P_{DIS}	Power dissipation			1.91(1)		W
I_{VA19}	1.9-V analog supply current	Power mode 2b: Dual channel, JMODE 8 (12-bit, 2 lanes, 64B/66B encoding), LPBG calibration, PLL_EN = 0, f_S = 1.0 GSPS, Low Power Mode		339		mA
I_{VPLL19}	PLL analog supply current			0		mA
I_{VREFO}	PLLREFO± analog supply current			0		mA
I_{VTRIG}	TRIGOUT± analog supply current			0		mA
I_{VA11}	1.1-V analog supply current			340		mA
I_{VD11}	1.1-V digital supply current			235		mA
P_{DIS}	Power dissipation			1.28(1)		W

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Typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *セクション 5.3* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VA19}	1.9-V analog supply current	Power mode 2c: Single channel, JMODE 8 (12-bit, 1 lanes, 64B/66B encoding), LPBG calibration, PLL_EN = 0, f_S = 1.0 GSPS, Low Power Mode		235		mA
I_{VPLL19}	PLL analog supply current			0		mA
I_{VREFO}	PLLREFO± analog supply current			0		mA
I_{VTRIG}	TRIGOUT± analog supply current			0		mA
I_{VA11}	1.1-V analog supply current			319		mA
I_{VD11}	1.1-V digital supply current			179		mA
P_{DIS}	Power dissipation			1.0(1)		W
I_{VA19}	1.9-V analog supply current	Power mode 3a: Quad channel, JMODE 8 (12-bit, 4 lanes, 64B/66B encoding), LPBG calibration, PLL_EN = 1, PLLREF_SE = 1, f_{REF}= 50 MHz, TRIGOUT± enabled, f_S = 1.0 GSPS, Low Power Mode		558		mA
I_{VPLL19}	PLL analog supply current			60		mA
I_{VREFO}	PLLREFO± analog supply current			13		mA
I_{VTRIG}	TRIGOUT± analog supply current			5		mA
I_{VA11}	1.1-V analog supply current			367		mA
I_{VD11}	1.1-V digital supply current			384		mA
P_{DIS}	Power dissipation			2.03(1)		W
I_{VA19}	1.9-V analog supply current	Power mode 3b: Dual channel, JMODE 8 (12-bit, 2 lanes, 64B/66B encoding), LPBG calibration, PLL_EN = 1, PLLREF_SE = 1, f_{REF}= 50 MHz, TRIGOUT± enabled, f_S = 1.0 GSPS, Low Power Mode		339		mA
I_{VPLL19}	PLL analog supply current			60		mA
I_{VREFO}	PLLREFO± analog supply current			13		mA
I_{VTRIG}	TRIGOUT± analog supply current			5		mA
I_{VA11}	1.1-V analog supply current			339		mA
I_{VD11}	1.1-V digital supply current			240		mA
P_{DIS}	Power dissipation			1.36(1)		W
I_{VA19}	1.9-V analog supply current	Power mode 3c: Single channel, JMODE 8 (12-bit, 1 lanes, 64B/66B encoding), LPBG calibration, PLL_EN = 1, PLLREF_SE = 1, f_{REF}= 50 MHz, TRIGOUT± enabled, f_S = 1.0 GSPS, Low Power Mode		234		mA
I_{VPLL19}	PLL analog supply current			60		mA
I_{VREFO}	PLLREFO± analog supply current			13		mA
I_{VTRIG}	TRIGOUT± analog supply current			5		mA
I_{VA11}	1.1-V analog supply current			314		mA
I_{VD11}	1.1-V digital supply current			180		mA
P_{DIS}	Power dissipation			1.15(1)		W
I_{VA19}	1.9-V analog supply current	Power mode 4a: Quad channel, JMODE 7 (8-bit, 4 lanes, 64B/66B encoding), FG calibration, PLL_EN = 0, f_S = 1.0 GSPS, Low Power Mode		533		mA
I_{VPLL19}	PLL analog supply current			0		mA
I_{VREFO}	PLLREFO± analog supply current			0		mA
I_{VTRIG}	TRIGOUT± analog supply current			0		mA
I_{VA11}	1.1-V analog supply current			364		mA
I_{VD11}	1.1-V digital supply current			301		mA
P_{DIS}	Power dissipation			1.74		W
I_{VA19}	1.9-V analog supply current	Power mode 4b: Dual channel, JMODE 7 (8-bit, 2 lanes, 64B/66B encoding), FG calibration, PLL_EN = 0, f_S = 1.0 GSPS, Low Power Mode		327		mA
I_{VPLL19}	PLL analog supply current			0		mA
I_{VREFO}	PLLREFO± analog supply current			0		mA
I_{VTRIG}	TRIGOUT± analog supply current			0		mA
I_{VA11}	1.1-V analog supply current			317		mA
I_{VD11}	1.1-V digital supply current			188		mA
P_{DIS}	Power dissipation			1.17		W

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Typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *セクション 5.3* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{VA19}	1.9-V analog supply current	Power mode 4c: Single channel, JMODE 7 (8-bit, 1 lanes, 64B/66B encoding), FG calibration, PLL_EN = 0, f_S = 1.0 GSPS, Low Power Mode		226		mA
I_{VPLL19}	PLL analog supply current			0		mA
I_{VREFO}	PLLREFO± analog supply current			0		mA
I_{VTRIG}	TRIGOUT± analog supply current			0		mA
I_{VA11}	1.1-V analog supply current			294		mA
I_{VD11}	1.1-V digital supply current			135		mA
P_{DIS}	Power dissipation			0.9		W
I_{VA19}	1.9-V analog supply current	Power mode 5a: Quad channel, JMODE 0 (12-bit, 8 lanes, 8B/10B encoding), BG calibration, PLL_EN = 1, PLLREF_SE = 0, f_{REF}= 50 MHz, TRIGOUT± enabled, f_S = 1.6 GSPS, High Performance Mode		788		mA
I_{VPLL19}	PLL analog supply current			60		mA
I_{VREFO}	PLLREFO± analog supply current			13		mA
I_{VTRIG}	TRIGOUT± analog supply current			7		mA
I_{VA11}	1.1-V analog supply current			702		mA
I_{VD11}	1.1-V digital supply current			734		mA
P_{DIS}	Power dissipation			3.22		W
I_{VA19}	1.9-V analog supply current	Power mode 5b: Dual channel, JMODE 0 (12-bit, 4 lanes, 8B/10B encoding), BG calibration, PLL_EN = 1, PLLREF_SE = 0, f_{REF}= 50 MHz, TRIGOUT± enabled, f_S = 1.6 GSPS, High Performance Mode		525		mA
I_{VPLL19}	PLL analog supply current			58		mA
I_{VREFO}	PLLREFO± analog supply current			13		mA
I_{VTRIG}	TRIGOUT± analog supply current			5		mA
I_{VA11}	1.1-V analog supply current			557		mA
I_{VD11}	1.1-V digital supply current			485		mA
P_{DIS}	Power dissipation			2.22		W
I_{VA19}	1.9-V analog supply current	Power mode 5c: Single channel, JMODE 0 (12-bit, 2 lanes, 8B/10B encoding), BG calibration, PLL_EN = 1, PLLREF_SE = 0, f_{REF}= 50 MHz, TRIGOUT± enabled, f_S = 1.6 GSPS, High Performance Mode		393		mA
I_{VPLL19}	PLL analog supply current			60		mA
I_{VREFO}	PLLREFO± analog supply current			13		mA
I_{VTRIG}	TRIGOUT± analog supply current			5		mA
I_{VA11}	1.1-V analog supply current			546		mA
I_{VD11}	1.1-V digital supply current			304		mA
P_{DIS}	Power dissipation			1.76		W
I_{VA19}	1.9-V analog supply current	Power mode 6: Power-down enabled (PD = 1)		47		mA
I_{VPLL19}	PLL analog supply current			0		mA
I_{VREFO}	PLLREFO± analog supply current			0		mA
I_{VTRIG}	TRIGOUT± analog supply current			0		mA
I_{VA11}	1.1-V analog supply current			32		mA
I_{VD11}	1.1-V digital supply current			27		mA
P_{DIS}	Power dissipation			0.15		W

(1) Low-power background (LPBG) calibration supply current and power dissipation numbers are in the calibration sleep state. The power dissipation in this mode increases to the background (BG) calibration power consumption during the calibration state. The sleep period can be controlled by the user and long sleep periods will average out the calibration state power dissipation contribution.

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5.7 ADC12xJ1600-Q1: Electrical Characteristics: AC Specifications

typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *セクション 5.3* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
FPBW	Full-power input bandwidth (–3 dB)(1)	Foreground calibration			6		GHz
		Background calibration			6		
XTALK	Channel-to-channel crosstalk (Quad and dual channel only)	Aggressor = 400 MHz, –1 dBFS			–73		dB
		Aggressor = 1 GHz, –1 dBFS			–65		
		Aggressor = 3 GHz, –1 dBFS			–59		
CER	Code error rate	Maximum CER, does not include JESD204C interface BER			10^{-18}		Errors/ sample
t_{ORR}	Overrange recovery time	Time from an overdriven input to accurate conversion after a step from a ±1.2 $V_{PP-DIFF}$ overdriven input stepped to 0 $V_{PP-DIFF}$.			1		t_{CLK} cycles
$NOISE_{DC}$	DC input noise standard deviation	No input, foreground calibration, excludes DC offset			1.8		LSB
NSD	Noise spectral density	Maximum full-scale voltage (V_{FS} = 1.0 V_{PP}), A_{IN} = –20 dBFS			–148		dBFS/Hz
		Default full-scale voltage (V_{FS} = 0.8 V_{PP}), A_{IN} = –20 dBFS			–147		
NF	Noise figure, Z_S = 100 Ω	Maximum full-scale voltage (V_{FS} = 1.0 V_{PP}), A_{IN} = –20 dBFS			26.2		dB
		Default full-scale voltage (V_{FS} = 0.8 V_{PP}), A_{IN} = –20 dBFS			25.8		
SNR	Signal-to-noise ratio, excluding DC, HD2 to HD9	f_{IN} = 97 MHz	A_{IN} = –1 dBFS		57.4		dBFS
			A_{IN} = –3 dBFS		57.6		
			A_{IN} = –12 dBFS		57.8		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		58.7		
		f_{IN} = 497 MHz	A_{IN} = –1 dBFS		57.2		
			A_{IN} = –3 dBFS		57.5		
			A_{IN} = –12 dBFS		57.5		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS	54	56.8		
			A_{IN} = –3 dBFS		57.3		
			A_{IN} = –12 dBFS		57.8		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		57.9		
		f_{IN} = 1797 MHz	A_{IN} = –1 dBFS		56.7		
			A_{IN} = –3 dBFS		57.2		
			A_{IN} = –12 dBFS		57.8		
		f_{IN} = 2697 MHz	A_{IN} = –1 dBFS		55.9		
			A_{IN} = –3 dBFS		56.7		
			A_{IN} = –12 dBFS		57.7		
		f_{IN} = 3497 MHz	A_{IN} = –1 dBFS		55.3		
			A_{IN} = –3 dBFS		56.1		
			A_{IN} = –12 dBFS		57.6		

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typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the セクション 5.3 table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SINAD	Signal-to-noise and distortion ratio, excluding DC offset	f_{IN} = 97 MHz	A_{IN} = –1 dBFS		55.8		dBFS
			A_{IN} = –3 dBFS		56.7		
			A_{IN} = –12 dBFS		57.7		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		57.4		
		f_{IN} = 497 MHz	A_{IN} = –1 dBFS		55.8		
			A_{IN} = –3 dBFS		56.7		
			A_{IN} = –12 dBFS		57.9		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS	53	56		
			A_{IN} = –3 dBFS		56.8		
			A_{IN} = –12 dBFS		57.7		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		57.5		
		f_{IN} = 1797 MHz	A_{IN} = –1 dBFS		54.6		
			A_{IN} = –3 dBFS		56		
			A_{IN} = –12 dBFS		57.8		
		f_{IN} = 2697 MHz	A_{IN} = –1 dBFS		51.3		
			A_{IN} = –3 dBFS		54.6		
			A_{IN} = –12 dBFS		57.6		
		f_{IN} = 3497 MHz	A_{IN} = –1 dBFS		48.3		
			A_{IN} = –3 dBFS		52.7		
			A_{IN} = –12 dBFS		57.5		
ENOB	Effective number of bits, excluding DC offset	f_{IN} = 97 MHz	A_{IN} = –1 dBFS		9		bits
			A_{IN} = –3 dBFS		9.1		
			A_{IN} = –12 dBFS		9.3		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		9.2		
		f_{IN} = 497 MHz	A_{IN} = –1 dBFS		9		
			A_{IN} = –3 dBFS		9.1		
			A_{IN} = -12 dBFS		9.3		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS	8.5	9		
			A_{IN} = –3 dBFS		9.1		
			A_{IN} = –12 dBFS		9.3		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		9.3		
		f_{IN} = 1797 MHz	A_{IN} = –1 dBFS		8.8		
			A_{IN} = –3 dBFS		9		
			A_{IN} = –12 dBFS		9.3		
		f_{IN} = 2697 MHz	A_{IN} = –1 dBFS		8.2		
			A_{IN} = –3 dBFS		8.8		
			A_{IN} = –12 dBFS		9.3		
		f_{IN} = 3497 MHz	A_{IN} = –1 dBFS		7.7		
			A_{IN} = –3 dBFS		8.5		
			A_{IN} = –12 dBFS		9.3		

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typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *セクション 5.3* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
SFDR	Spurious-free dynamic range	f_{IN} = 97 MHz	A_{IN} = –1 dBFS		64		dBFS
			A_{IN} = –3 dBFS		66		
			A_{IN} = –12 dBFS		77		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		66		
		f_{IN} = 497 MHz	A_{IN} = –1 dBFS		64		
			A_{IN} = –3 dBFS		66		
			A_{IN} = –12 dBFS		79		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS	58	66		
			A_{IN} = –3 dBFS		67		
			A_{IN} = –12 dBFS		77		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		68		
		f_{IN} = 1797 MHz	A_{IN} = –1 dBFS		61		
			A_{IN} = –3 dBFS		65		
			A_{IN} = –12 dBFS		76		
		f_{IN} = 2697 MHz	A_{IN} = –1 dBFS		54		
			A_{IN} = –3 dBFS		61		
			A_{IN} = –12 dBFS		75		
		f_{IN} = 3497 MHz	A_{IN} = –1 dBFS		51		
			A_{IN} = –3 dBFS		57		
			A_{IN} = –12 dBFS		76		
HD2	2nd-order harmonic distortion	f_{IN} = 97 MHz	AIN = –1 dBFS		–64		dBFS
			A_{IN} = –3 dBFS		–66		
			A_{IN} = –12 dBFS		–77		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–66		
		f_{IN} = 497 MHz	A_{IN} = –1 dBFS		–65		
			A_{IN} = –3 dBFS		–66		
			A_{IN} = –12 dBFS		–83		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		–66	–58	
			A_{IN} = –3 dBFS		–67		
			A_{IN} = –12 dBFS		–79		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–68		
		f_{IN} = 1797 MHz	A_{IN} = –1 dBFS		–64		
			A_{IN} = –3 dBFS		–66		
			A_{IN} = –12 dBFS		–76		
		f_{IN} = 2697 MHz	A_{IN} = –1 dBFS		–61		
			A_{IN} = –3 dBFS		–64		
			A_{IN} = –12 dBFS		–78		
		f_{IN} = 3497 MHz	A_{IN} = –1 dBFS		–55		
			A_{IN} = –3 dBFS		–60		
			A_{IN} = –12 dBFS		–76		

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typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the セクション 5.3 table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
HD3	3rd-order harmonic distortion	f_{IN} = 97 MHz	AIN = –1 dBFS		–67		dBFS
			A_{IN} = –3 dBFS		–73		
			A_{IN} = –12 dBFS		–85		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–68		
		f_{IN} = 497 MHz	A_{IN} = –1 dBFS		–67		
			A_{IN} = –3 dBFS		–76		
			A_{IN} = –12 dBFS		–81		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		–70	–58	
			A_{IN} = –3 dBFS		–80		
			A_{IN} = –12 dBFS		–80		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–76		
		f_{IN} = 1797 MHz	A_{IN} = –1 dBFS		–61		
			A_{IN} = –3 dBFS		–67		
			A_{IN} = –12 dBFS		–84		
		f_{IN} = 2697 MHz	A_{IN} = –1 dBFS		–54		
			A_{IN} = –3 dBFS		–61		
			A_{IN} = –12 dBFS		–77		
		f_{IN} = 3497 MHz	A_{IN} = –1 dBFS		–51		
			A_{IN} = –3 dBFS		–57		
			A_{IN} = –12 dBFS		–85		
SPUR	Worst spur, excluding DC, HD2, HD3	f_{IN} = 97 MHz	AIN = –1 dBFS		–77		dBFS
			A_{IN} = –3 dBFS		–79		
			A_{IN} = –12 dBFS		–84		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–79		
		f_{IN} = 497 MHz	A_{IN} = –1 dBFS		–73		
			A_{IN} = –3 dBFS		–75		
			A_{IN} = –12 dBFS		–82		
		f_{IN} = 997 MHz	A_{IN} = –1 dBFS		–74	–65	
			A_{IN} = –3 dBFS		–77		
			A_{IN} = –12 dBFS		–83		
			A_{IN} = –3 dBFS, V_{FS} = 1.0 V_{PP}		–77		
		f_{IN} = 1797 MHz	A_{IN} = –1 dBFS		–74		
			A_{IN} = –3 dBFS		–78		
			A_{IN} = –12 dBFS		–84		
		f_{IN} = 2697 MHz	A_{IN} = –1 dBFS		–71		
			A_{IN} = –3 dBFS		–76		
			A_{IN} = –12 dBFS		–84		
		f_{IN} = 3497 MHz	A_{IN} = –1 dBFS		–75		
			A_{IN} = –3 dBFS		–77		
			A_{IN} = –12 dBFS		–83		

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typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *セクション 5.3* table

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
IMD3	3rd-order intermodulation distortion	f_1 = 93 MHz, f_2 = 103 MHz	A_{IN} = –7 dBFS per tone		–80		dBFS
			A_{IN} = –9 dBFS per tone		–87		
			A_{IN} = –18 dBFS per tone		–91		
			A_{IN} = –9 dBFS per tone, V_{FS} = 1.0 V_{PP}		–86		
		f_1 = 493 MHz, f_2 = 503 MHz	A_{IN} = –7 dBFS per tone		–84		
			A_{IN} = –9 dBFS per tone		–84		
			A_{IN} = –18 dBFS per tone		–88		
		f_1 = 993 MHz, f_2 = 1003 MHz	A_{IN} = –7 dBFS per tone		–77		
			A_{IN} = –9 dBFS per tone		–80		
			A_{IN} = –18 dBFS per tone		–85		
			A_{IN} = –9 dBFS per tone, V_{FS} = 1.0 V_{PP}		–78		
		f_1 = 1793 MHz, f_2 = 1803 MHz	A_{IN} = –7 dBFS per tone		–68		
			A_{IN} = –9 dBFS per tone		–73		
			A_{IN} = –18 dBFS per tone		–91		
		f_1 = 2693 MHz, f_2 = 2703 MHz	A_{IN} = –7 dBFS per tone		–56		
			A_{IN} = –9 dBFS per tone		–63		
			A_{IN} = –18 dBFS per tone		–83		
		f_1 = 3493 MHz, f_2= 3503 MHz	A_{IN} = –7 dBFS per tone		–52		
			A_{IN} = –9 dBFS per tone		–57		
			A_{IN} = –18 dBFS per tone		–90		

(1) Full-power input bandwidth (FPBW) is defined as the input frequency where the reconstructed output of the ADC has dropped 3 dB below the power of a full-scale input signal at a low input frequency. Useable bandwidth may exceed the –3-dB, full-power input bandwidth.

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5.8 Timing Requirements

			MIN	NOM	MAX	UNIT
ADC SAMPLING CLOCK						
f_S	ADC core sampling clock frequency	High Performance Mode	500(1)		1600(1)	MHz
		Low Power Mode			1000(1)	
	ADC core minimum sampling clock frequency	Low Power Mode		500(1)		
t_S	ADC core sampling clock period	High Performance Mode	625(1)		2000(1)	ps
		Low Power Mode	1000(1)			ps
	ADC core maximum sampling clock period	Low Power Mode		2000(1)		ps
CLOCK INPUTS (CLK+, CLK–, SE_CLK)						
f_{CLK}	CLK± input frequency	PLL Disabled	500		1600	MHz
		PLL Enabled, PLLREF_SE = 0	50		500	
f_{SE_CLK}	SE_CLK input frequency	PLL Enabled, PLLREF_SE = 1	50		500	MHz
$DC_{(CLKMIN)}$	Minimum Input clock duty cycle (CLK± and SE_CLK)	Input clock duty cycle (CLK± and SE_CLK)		40%		
$DC_{(CLKMAX)}$	Maximum Input clock duty cycle (CLK± and SE_CLK)			60%		
PHASE-LOCKED LOOP (PLL) AND VOLTAGE-CONTROLLED OSCILLATOR (VCO)						
f_{PLLPFD}	PLL phase-frequency detector (PFD) frequency	PLL Enabled	50		500	MHz
f_{VCO}	Closed-loop voltage-controlled oscillator (VCO) frequency	PLL Enabled	7200		8200	MHz
SYSREF (SYSREF+, SYSREF–)						
$t_{INV(SYSREF)}$	Width of invalid SYSREF capture region of CLK± period, indicating setup or hold time violation, as measured by SYSREF_POS status register(2)			250		ps
$t_{INV(TEMP)}$	Drift of invalid SYSREF capture region over temperature, positive number indicates a shift toward MSB of SYSREF_POS register			0.05		ps/°C
$t_{INV(VA11)}$	Drift of invalid SYSREF capture region over VA11 supply voltage, positive number indicates a shift toward MSB of SYSREF_POS register			-0.17		ps/mV
$t_{STEP(SP)}$	Delay of SYSREF_POS LSB	SYSREF_ZOOM = 0		125		ps
		SYSREF_ZOOM = 1		69		
$DC_{(SYSREF)}$	SYSREF duty cycle (asserted) when using a periodic SYSREF signal			50%	55%	
$t_{(PH_SYS)}$	Minimum SYSREF± assertion duration after SYSREF± rising edge event			4		ns
JESD204C SYNC TIMING ($\overline{SYNCSE}$)						
SERIAL PROGRAMMING INTERFACE (SCLK, SDI, $\overline{SCS}$)						
$f_{CLK(SCLK)}$	Serial clock frequency		0		15.625	MHz
$t_{(PH)}$	Serial clock high value pulse duration			32		ns
$t_{(PL)}$	Serial clock low value pulse duration			32		ns
$t_{SU(\overline{SCS})}$	Setup time from $\overline{SCS}$ to rising edge of SCLK			25		ns
$t_{H(\overline{SCS})}$	Hold time from rising edge of SCLK to $\overline{SCS}$			3		ns
$t_{SU(SDI)}$	Setup time from SDI to rising edge of SCLK			25		ns
$t_{H(SDI)}$	Hold time from rising edge of SCLK to SDI			3		ns

(1) Unless functionally limited to a smaller range in the tables Operating Modes for Quad Channel Device through Operating Modes for Single Channel Device based on programmed JMODE.

(2) Use SYSREF_POS to select an optimal SYSREF_SEL value for the SYSREF capture, see the section SYSREF Windowingfor more information on SYSREF windowing. The invalid region, specified by $t_{INV(SYSREF)}$, indicates the portion of the CLK± period(t_{CLK}), as measured by SYSREF_SEL, that may result in a setup and hold violation. Verify that the timing skew between SYSREF± and CLK± over system operating conditions from the nominal conditions (that used to find optimal SYSREF_SEL) does not result in the invalid

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region occurring at the selected SYSREF_SEL position in SYSREF_POS, otherwise a temperature dependent SYSREF_SEL selection may be needed to track the skew between CLK± and SYSREF±.

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5.9 Switching Characteristics

typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration, SER_PE = 4 (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *セクション 5.3* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC SAMPLING CLOCK						
t_{AD}	Sampling (aperture) delay from the clock falling edge to sampling instant	PLL disabled, CLK±		305		ps
		PLL enabled, CLK±		314		ps
		PLL enabled, SE_CLK		332		ps
t_{AJ}	Aperture jitter, rms	Dither disabled (ADC_DITH_EN = 0)		50		fs
		Dither enabled (ADC_DITH_EN = 1)		60		fs
$t_{J(PLL)}$	PLL additive jitter, rms	PLL enabled (PLL_EN = 1), f_{PLLREF} = 50 MHz		710		fs
$t_{J(PLL)}$	PLL additive jitter, rms	PLL enabled (PLL_EN = 1), f_{PLLREF} = 200 MHz		810		fs
CLOCK AND TRIGGER OUTPUTS (PLLREFO±, TRIGOUT±, ORC, ORD)						
$f_{PLLREFO}$	PLLREFO± frequency range	PLL Enabled, PLLREFO± enabled	50		500	MHz
$f_{DIVREFO}$	ORC and ORD frequency range when programmed to output divided PLL reference clock	PLL Enabled, DIVREF_C_MODE > 0, DIVREF_D_MODE > 0	12.5		100	MHz
$t_{PW(TRIGOUT)}$	Minimum TRIGOUT± pulse width	TRIGOUT_SRC = 0 (TMSTP±)		1		t_{CLK}
$f_{TRIGOUT}$	TRIGOUT± frequency range	TRIGOUT_SRC = 1 (S-PLL)			800	MHz
$t_{PD(REF)}$	Input clock to PLLREFO± propagation delay	PLLREF_SE = 0 (CLK± used), nominal supply voltage, T_A = 25°C	280	359	440	ps
		PLLREF_SE = 1 (SE_CLK used), nominal supply voltage, T_A = 25°C	380	469	560	
$t_{PD-TEMPCO}$	Input clock to PLLREFO± propagation delay temperature coefficient	PLLREF_SE = 0 (CLK± used), nominal supply voltage	250	330	420	fs/°C
		PLLREF_SE = 1 (SE_CLK used), nominal supply voltage	280	365	450	
$t_{PD-VOLTCO}$	Input clock to PLLREFO± propagation delay supply voltage coefficient	PLLREF_SE = 0 (CLK± used), T_A = 25°C	–533	–397	–186	fs/mV
		PLLREF_SE = 1 (SE_CLK used), T_A = 25°C	–480	–372	–180	
SERIAL DATA OUTPUTS (D[7 :0]+, D[7 :0]–)						
f_{SERDES}	Serialized output bit rate		2.5		17.16	Gbps
UI	Serialized output unit interval		58.3		400	ps
t_{TLH}	Low-to-high transition time (differential)	20% to 80%, 8H8L test pattern, 16.5 Gbps		28		ps
t_{THL}	High-to-low transition time (differential)	20% to 80%, 8H8L test pattern, 16.5 Gbps		28		ps
DDJ	Data dependent jitter, peak-to-peak	PRBS-7 test pattern, JMODE = 0, 12.8 Gbps		8.56		ps
		PRBS-9 test pattern, JMODE = 4, 16.5 Gbps		6.9		
		PRBS-9 test pattern, JMODE = 8, 17.16 Gbps		9.28		
DCD	Even-odd jitter, peak-to-peak	PRBS-7 test pattern, JMODE = 0, 12.8 Gbps		0.2		ps
		PRBS-9 test pattern, JMODE = 4, 16.5 Gbps		0.01		
		PRBS-9 test pattern, JMODE = 8, 17.16 Gbps		0.05		
EBUJ	Effective bounded uncorrelated jitter, peak-to-peak	PRBS-7 test pattern, JMODE = 0, 12.8 Gbps		1.63		ps
		PRBS-9 test pattern, JMODE = 4, 16.5 Gbps		0.85		
		PRBS-9 test pattern, JMODE = 8, 17.16 Gbps		3.12		

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typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration, SER_PE = 4 (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *セクション 5.3* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RJ	Unbounded random jitter, RMS	8H8L test pattern, JMODE = 0, 12.8 Gbps		0.88		ps
		8H8L test pattern, JMODE = 4, 16.5 Gbps		0.72		
		8H8L test pattern, JMODE = 8, 17.16 Gbps		1		
TJ	Total jitter, peak-to-peak, with unbounded random jitter portion defined with respect to a BER = 1e-15 (Q = 7.94)	PRBS-7 test pattern, JMODE = 0, 12.8 Gbps		21.35		ps
		PRBS-9 test pattern, JMODE = 4, 16.5 Gbps		18.01		
		PRBS-9 test pattern, JMODE = 8, 17.16 Gbps		23.78		
ADC CORE LATENCY						
t_{ADC}	Deterministic delay from the CLK± edge that samples the reference sample to the CLK± edge that samples SYSREF going high(1)	JMODE = 0		–2		t_{CLK} cycles
		JMODE = 1		1		
		JMODE = 2		–1		
		JMODE = 3		–1		
		JMODE = 4		–1		
		JMODE = 5		–1		
		JMODE = 6		1		
		JMODE = 7		–1		
		JMODE = 8		–1		
		JMODE = 9		–1		
		JMODE = 10		–2		
		JMODE = 11		–2		
		JMODE = 12		–1		
		JMODE = 13		2		
		JMODE = 14		–2		
		JMODE = 15		–2		
JESD204C AND SERIALIZER LATENCY						
t_{TX}	Delay from the CLK± rising edge that samples SYSREF high to the first bit of the multiframe (8B/10B encoding) or extended multiblock (64B/66B encoding) on the JESD204C serial output lane corresponding to the reference sample of t_{ADC} (2)	JMODE = 0	49.8	56.6		t_{CLK} cycles
		JMODE = 1	45.5	52.8		
		JMODE = 2	45.5	52.8		
		JMODE = 3	44.3	50.5		
		JMODE = 4	42.1	48		
		JMODE = 5	42.1	48		
		JMODE = 6	53.3	60.2		
		JMODE = 7	53.3	60.2		
		JMODE = 8	47.1	54.2		
		JMODE = 9	58.4	65		
		JMODE = 10	56.2	63.1		
		JMODE = 11	66.3	74.5		
		JMODE = 12	87.2	94.8		
		JMODE = 13	72.9	83.9		
		JMODE = 14	61.7	68.1		
		JMODE = 15	94	103.3		
SERIAL PROGRAMMING INTERFACE (SDO)						

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typical values at T_A = 25°C, VA19 = 1.9 V, VPLL19 = 1.9 V, VREFO = 1.9 V, VTRIG = 1.1V, VA11 = 1.1 V, VD11 = 1.1 V, default full-scale voltage (V_{FS} = 0.8 V_{PP}), f_{IN} = 97 MHz, A_{IN} = –1 dBFS, f_{CLK} = 1.6 GHz, filtered 1-V_{PP} sine-wave clock applied to CLK±, PLL disabled, JMODE = 0, High Performance Mode and foreground calibration, SER_PE = 4 (unless otherwise noted); minimum and maximum values are at nominal supply voltages and over the operating free-air temperature range provided in the *セクション 5.3* table

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(OZD)}$	Delay from the falling edge of the 16th SCLK cycle during read operation for SDO transition from tri-state to valid data		1			ns
$t_{(ODZ)}$	Delay from the $\overline{SCS}$ rising edge for SDO transition from valid data to tri-state				10	ns
$t_{(OD)}$	Delay from the falling edge of SCLK during read operation to SDO valid		1		10	ns

(1) t_{ADC} is an exact, unrounded, deterministic delay. The delay can be negative if the reference sample is sampled after the SYSREF high capture point, in which case the total latency is smaller than the delay given by t_{TX}.

(2) The values given for t_{TX} include deterministic and non-deterministic delays. Over process, temperature, and voltage, the delay will vary. JESD204B accounts for these variations when operating in subclass-1 mode in order to achieve deterministic latency. Proper receiver RBD values must be chosen such that the elastic buffer release point does not occur within the invalid region of the local multiframe clock (LMFC) cycle.

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5.10 Typical Characteristics

Typical values at 25°C, A_{IN} = -1dBFS, F_{IN} = 347MHz, F_S = 1600MSPS, High power mode, FG calibration, JMODE 0, C-PLL off, C-PLL$_{REF}$ = 50MHz and VA11Q and VCLK11 noise suppression on when C-PLL on, Quad Channel operation, nominal supply voltages, unless otherwise noted. SNR results exclude DC and HD2 to HD9; SINAD, ENOB, and SFDR results exclude DC.

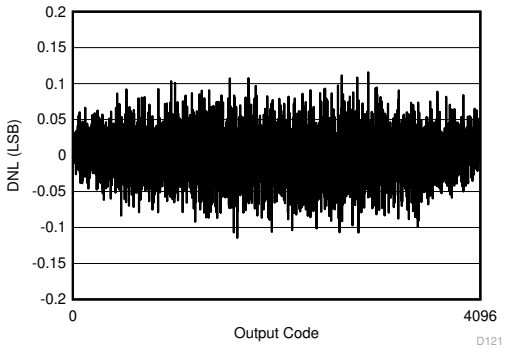


図 5-1. DNL vs Code

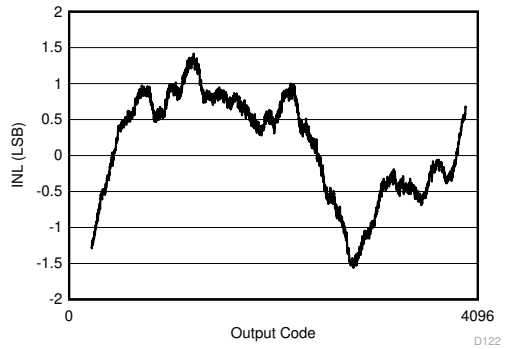
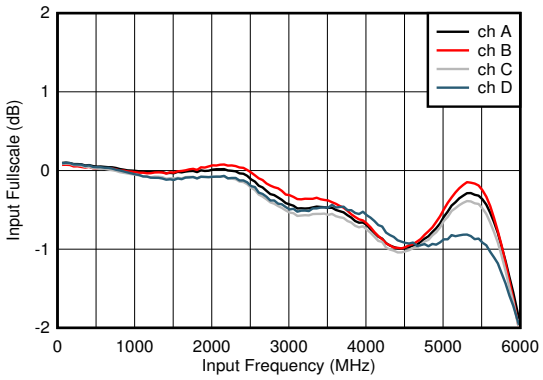
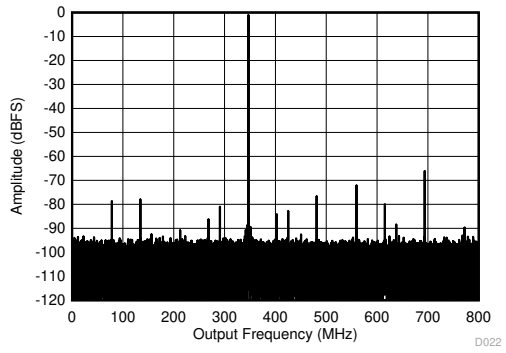


図 5-2. INL vs Code



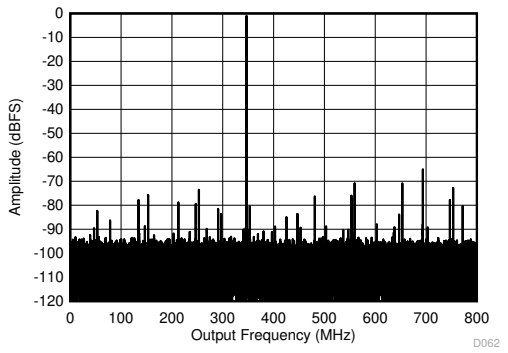
Relative to 0Hz

図 5-3. Input Fullscale vs Frequency



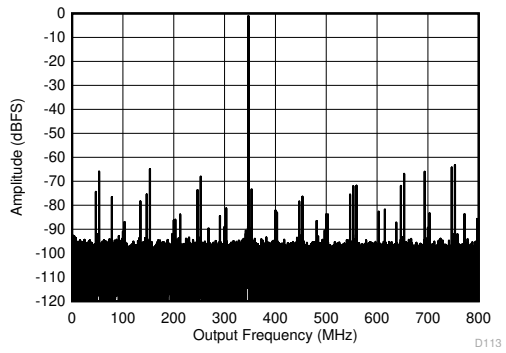
High power mode

図 5-4. Single Tone FFT at 347MHz and -1dBFS



High power mode, C-PLL on

図 5-5. Single Tone FFT at 347MHz and -1dBFS



High power mode, C-PLL on, Noise suppression off

図 5-6. Single Tone FFT at 347MHz and -1dBFS

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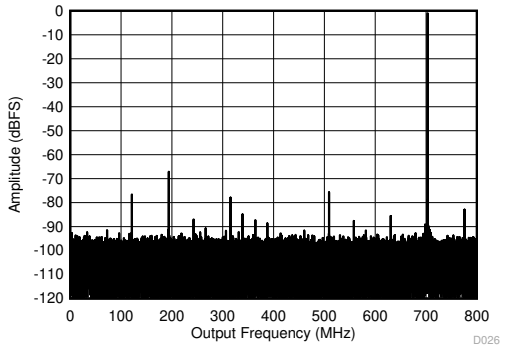
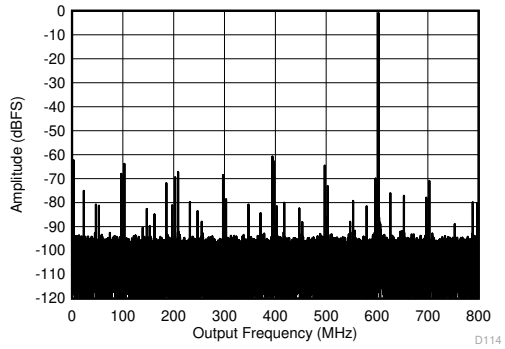


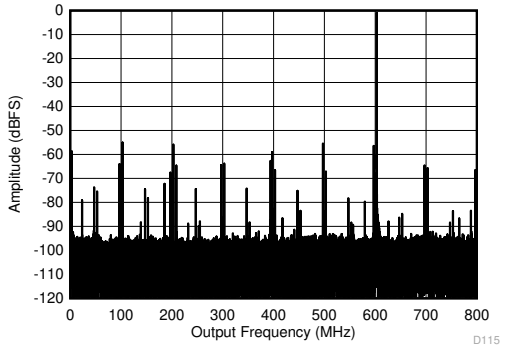
High power mode

図 5-7. Single Tone FFT at 847MHz and -1dBFS



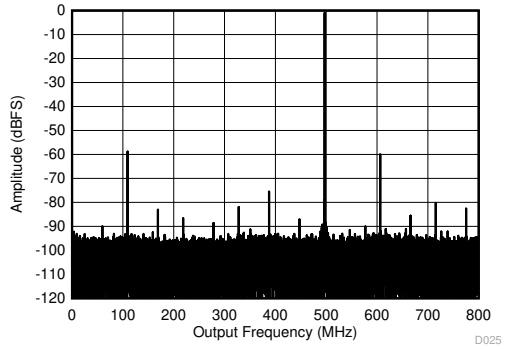
High power mode, C-PLL on

図 5-8. Single Tone FFT at 997MHz and -1dBFS



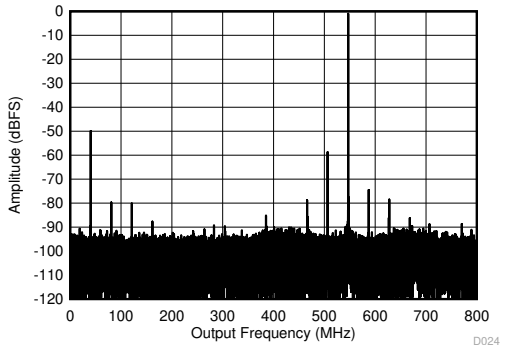
High power mode, C-PLL on, Noise suppression off

図 5-9. Single Tone FFT at 997MHz and -1dBFS



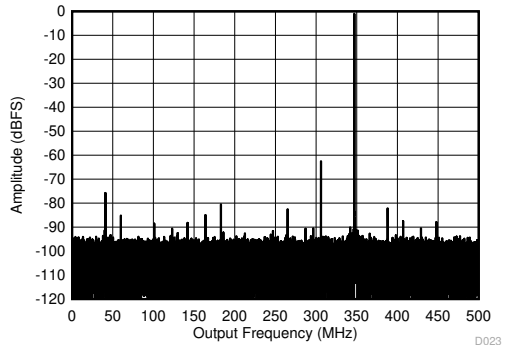
High power mode

図 5-10. Single Tone FFT at 2097MHz and -1dBFS



High power mode

図 5-11. Single Tone FFT at 3797MHz and -1dBFS



Low power mode, F_S = 1000MSPS

図 5-12. Single Tone FFT at 347MHz and -1dBFS

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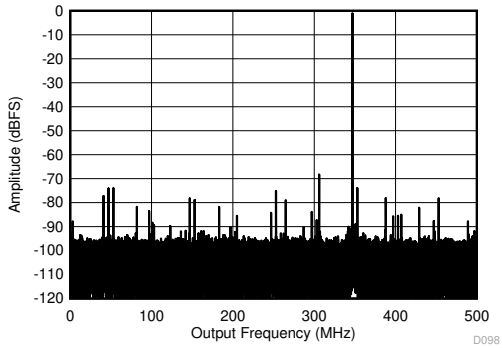
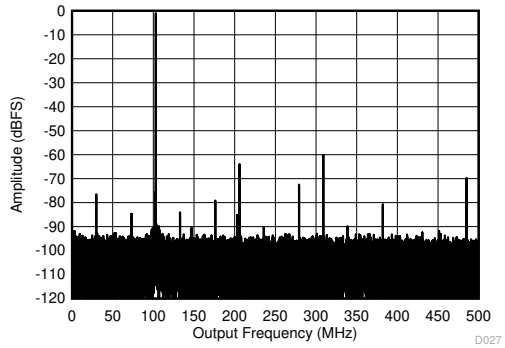


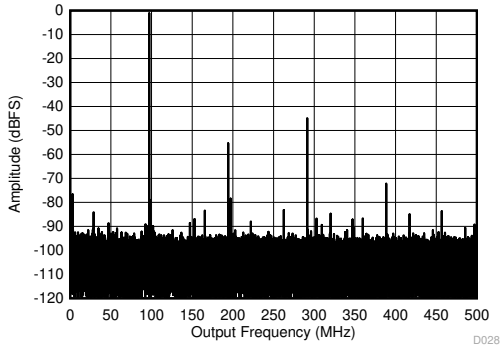
C-PLL on, Low power mode, F_S = 1000MSPS

図 5-13. Single Tone FFT at 347MHz and -1dBFS



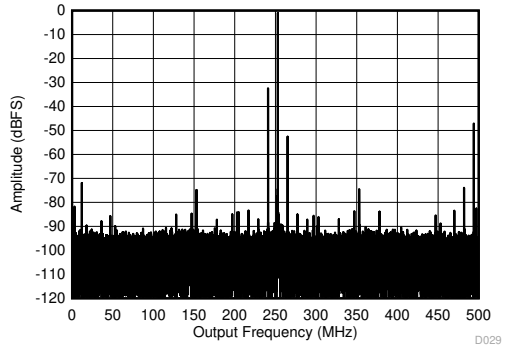
Low power mode, F_S = 1000MSPS

図 5-14. Single Tone FFT at 897MHz and -1dBFS



Low power mode, F_S = 1000MSPS

図 5-15. Single Tone FFT at 2097MHz and -1dBFS



Low power mode, F_S = 1000MSPS

図 5-16. Single Tone FFT at 3797MHz and -1dBFS

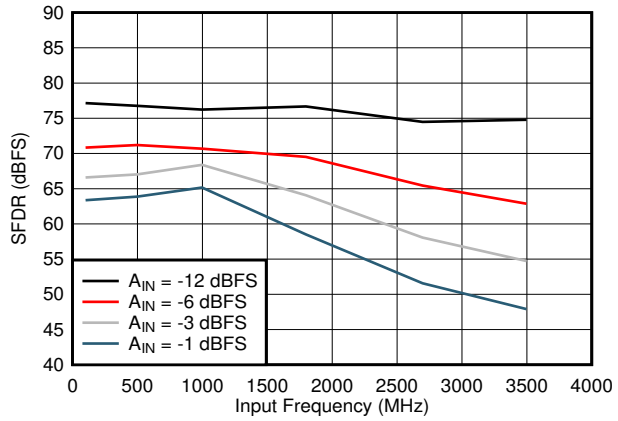


図 5-17. SFDR vs Input Frequency

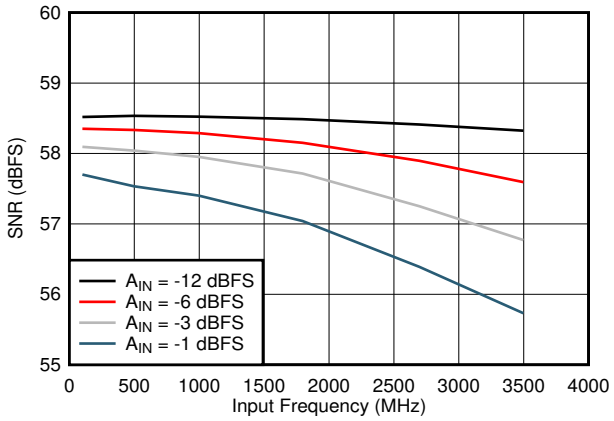


図 5-18. SNR vs Input Frequency

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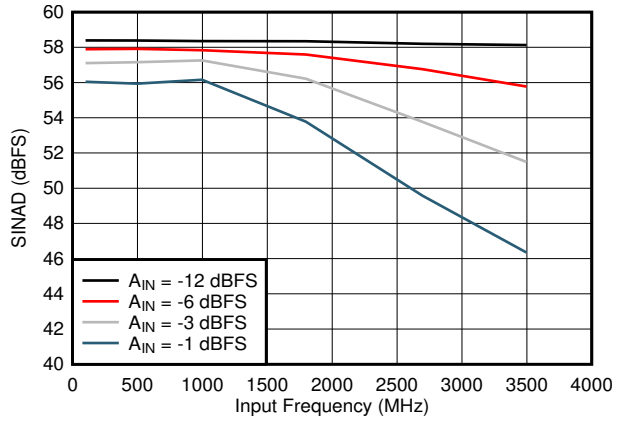

図 5-19. SINAD vs Input Frequency

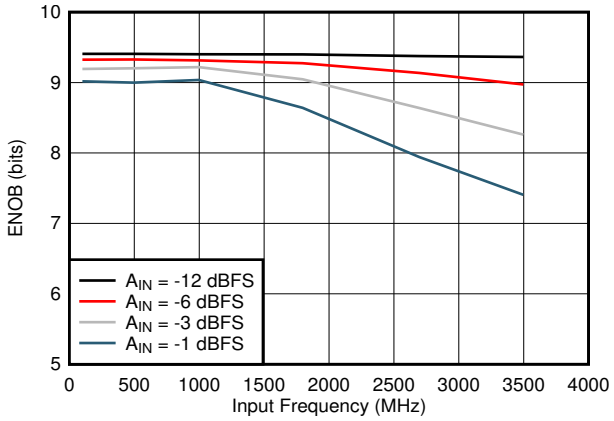

図 5-20. ENOB vs Input Frequency

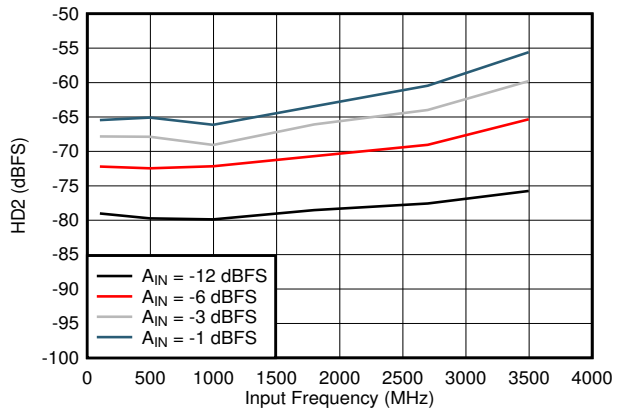

図 5-21. HD2 vs Input Frequency

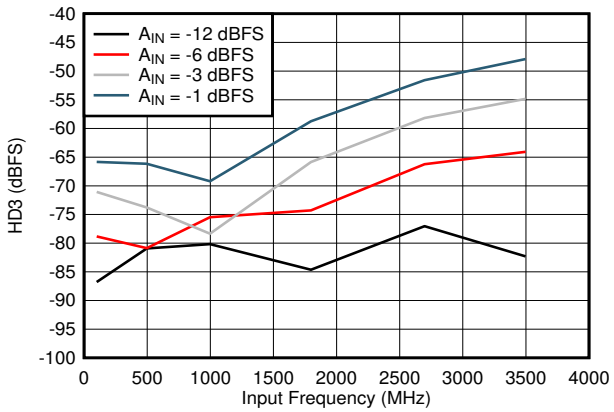

図 5-22. HD3 vs Input Frequency

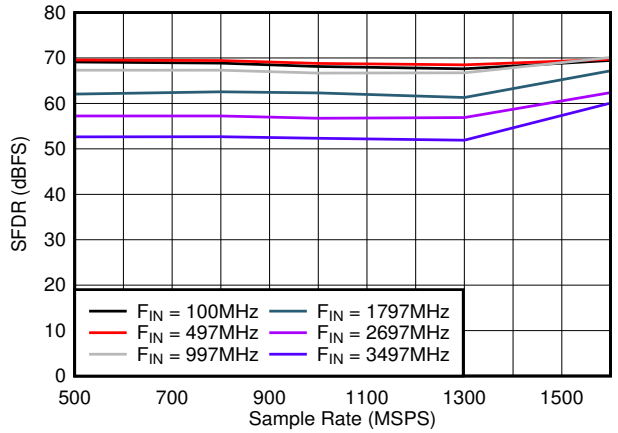

図 5-23. SFDR vs Sample Rate

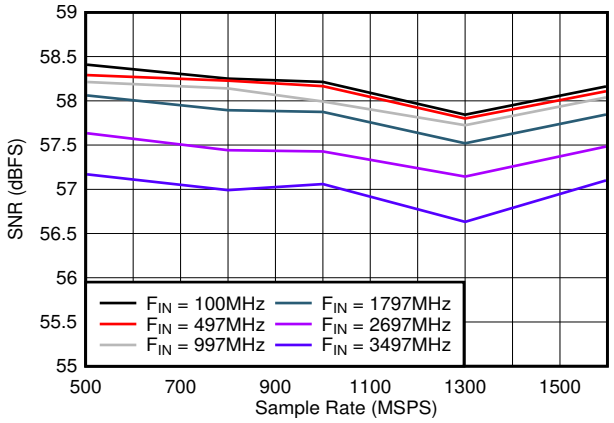

図 5-24. SNR vs Sample Rate

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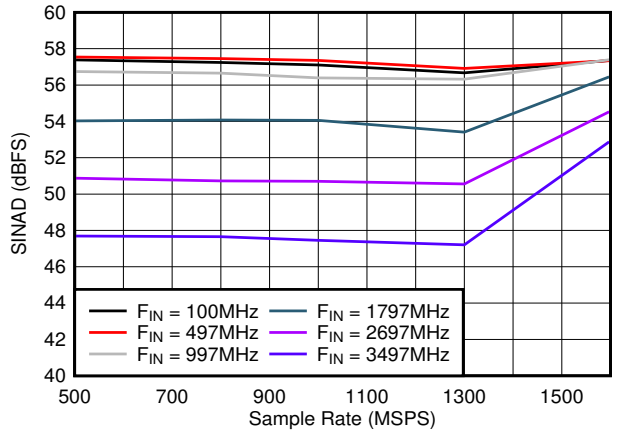

図 5-25. SINAD vs Sample Rate

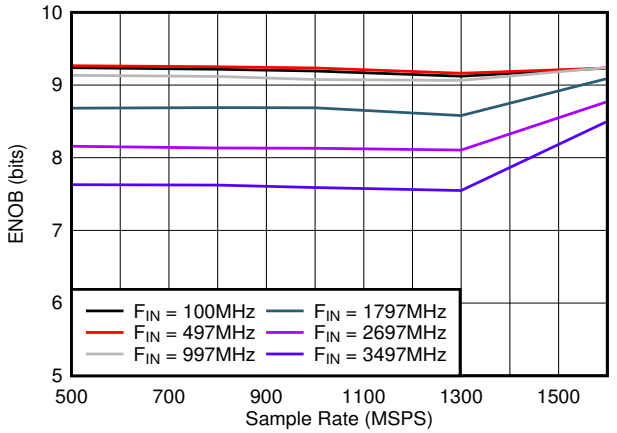

図 5-26. ENOB vs Sample Rate

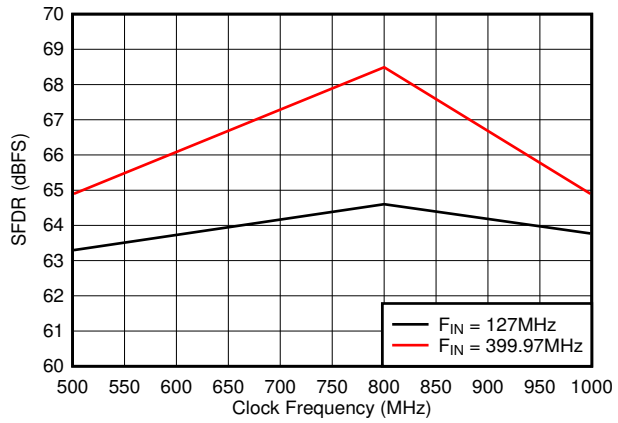

図 5-27. SFDR vs Sample Rate

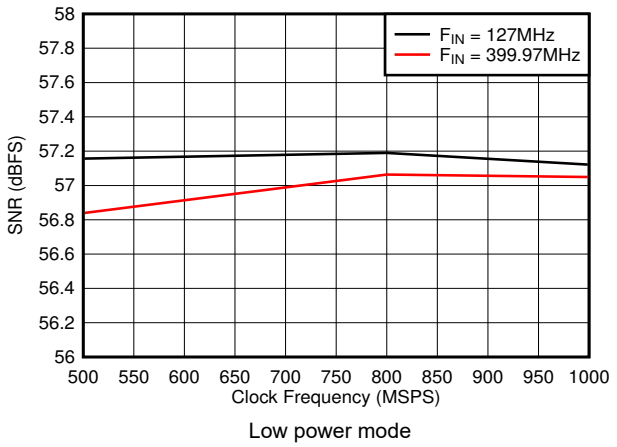

図 5-28. SNR vs Sample Rate

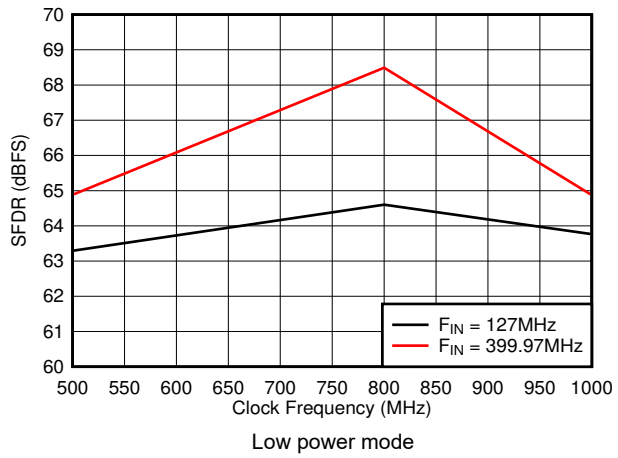

図 5-29. SFDR vs Sample Rate

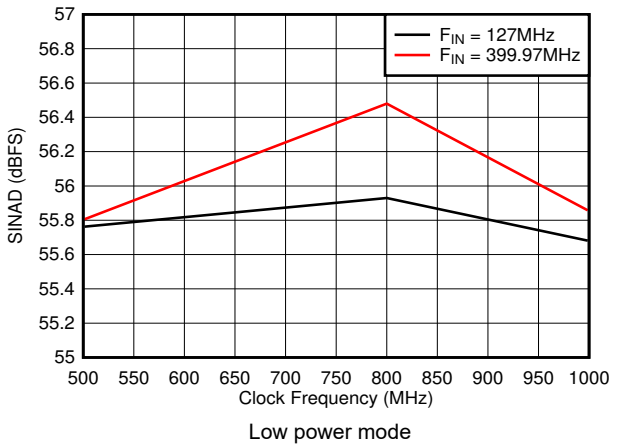

図 5-30. SINAD vs Sample Rate

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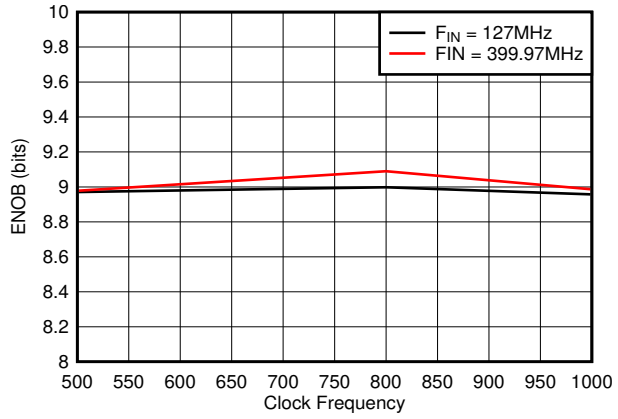


Low power mode

図 5-31. ENOB vs Sample Rate

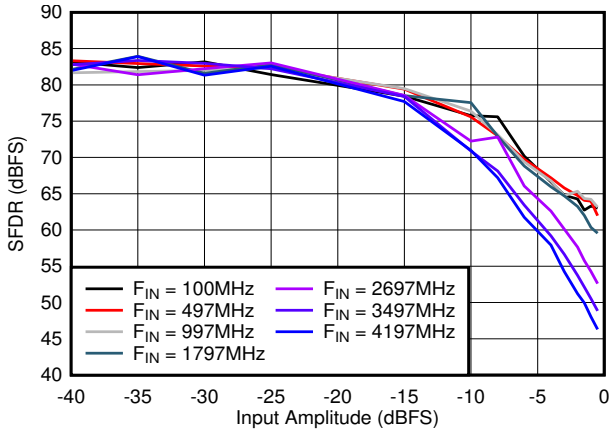


図 5-32. SFDR vs A_{IN}

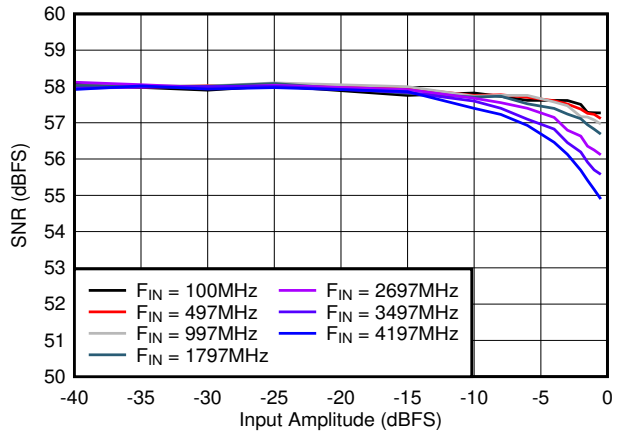
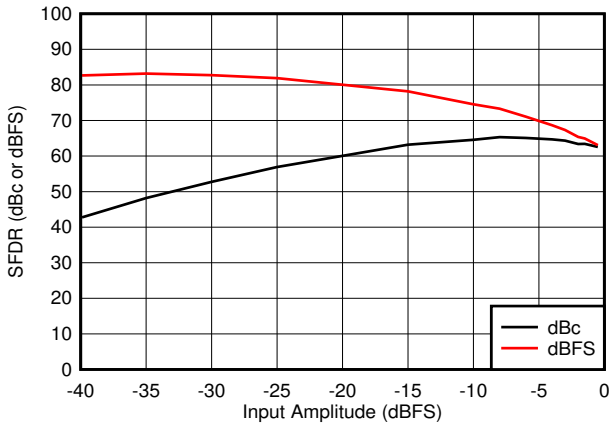
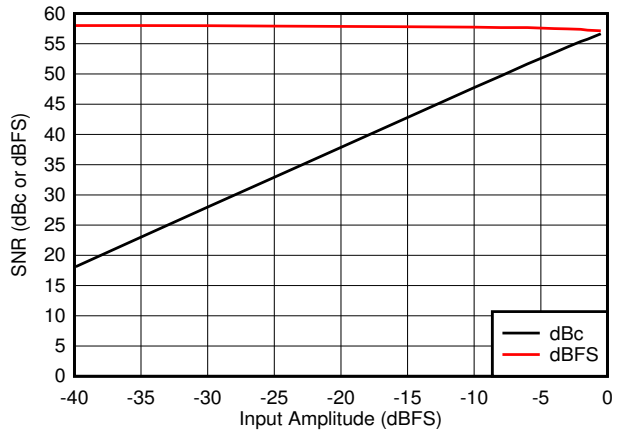


図 5-33. SNR vs A_{IN}



F_{IN} = 100MHz, Low power mode

図 5-34. SFDR vs A_{IN}



F_{IN} = 100MHz, Low power mode

図 5-35. SNR vs A_{IN}

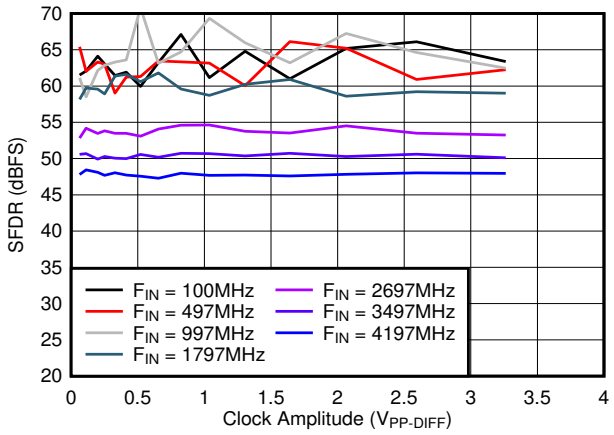


図 5-36. SFDR vs A_{CLK}

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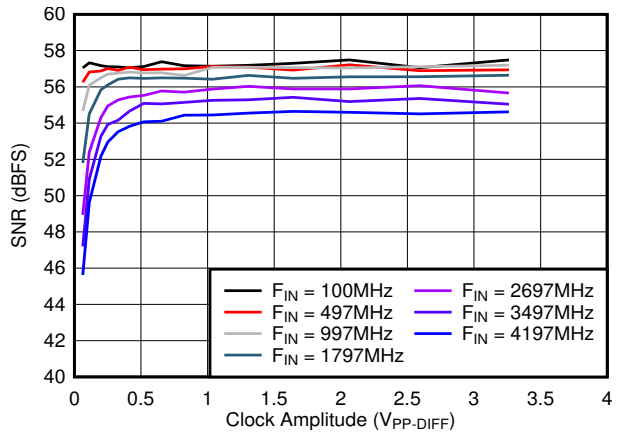
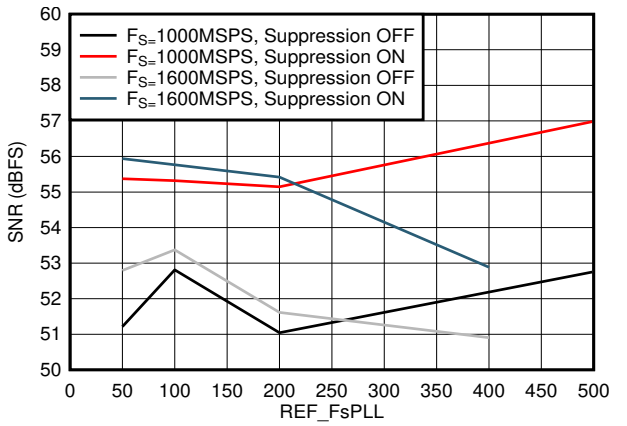
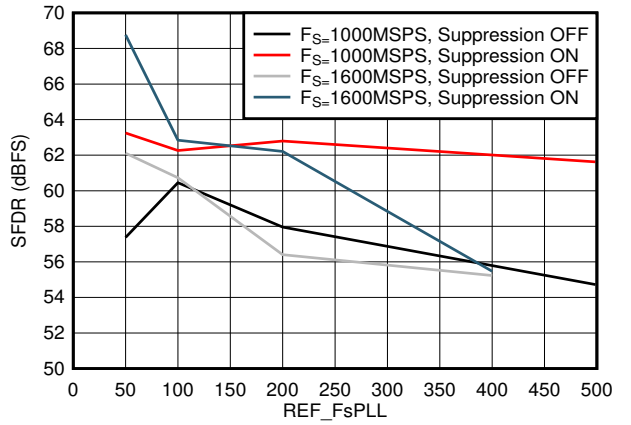


図 5-37. SNR vs A_{CLK}



F_{IN} = 397MHz

図 5-38. SNR vs F_{REF} and Suppression



F_{IN} = 397MHz

図 5-39. SFDR vs F_{REF} and Suppression

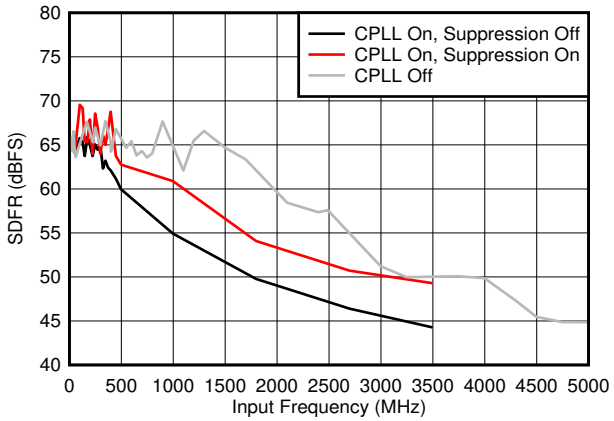


図 5-40. SFDR vs F_{IN} and C-PLL modes

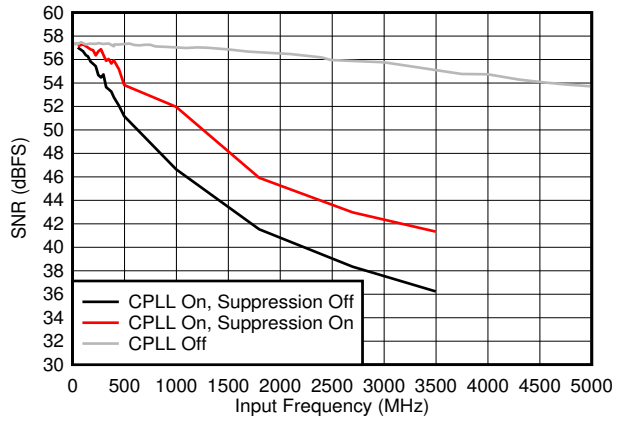


図 5-41. SNR vs F_{IN} and C-PLL modes

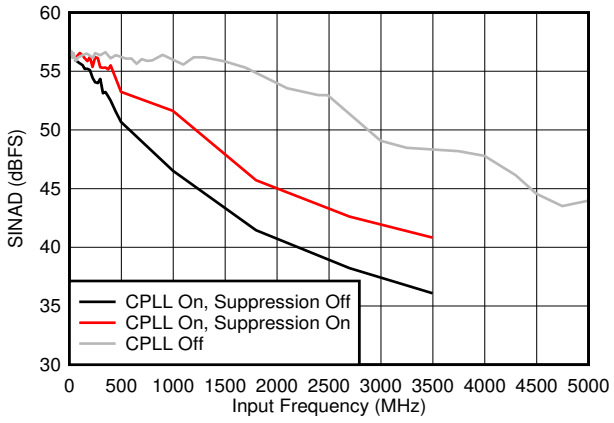


図 5-42. SINAD vs F_{IN} and C-PLL modes

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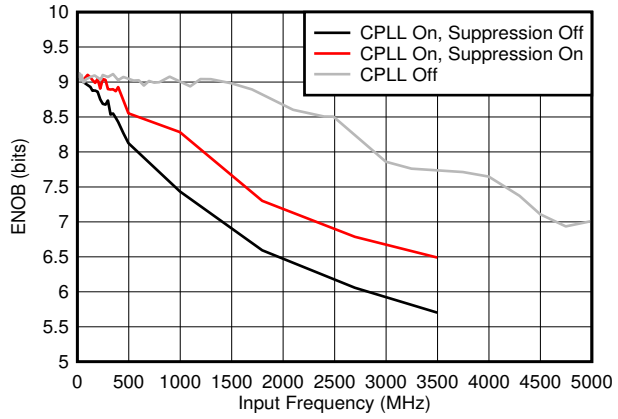
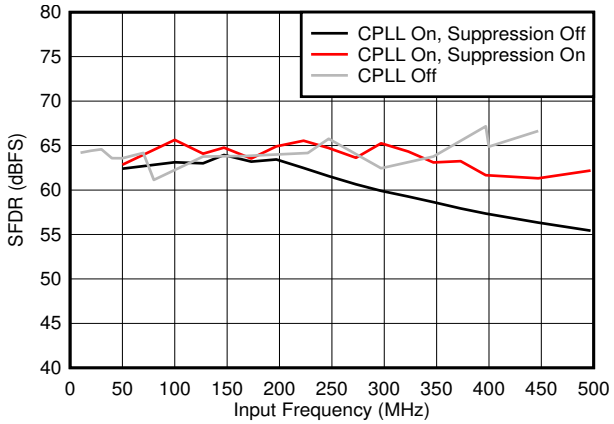
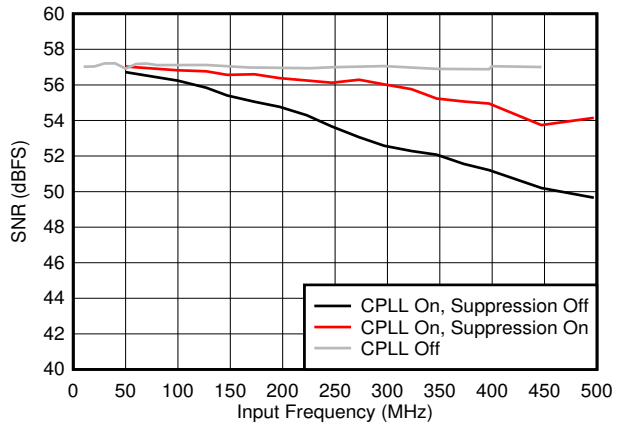


図 5-43. ENOB vs F_{IN} and C-PLL modes



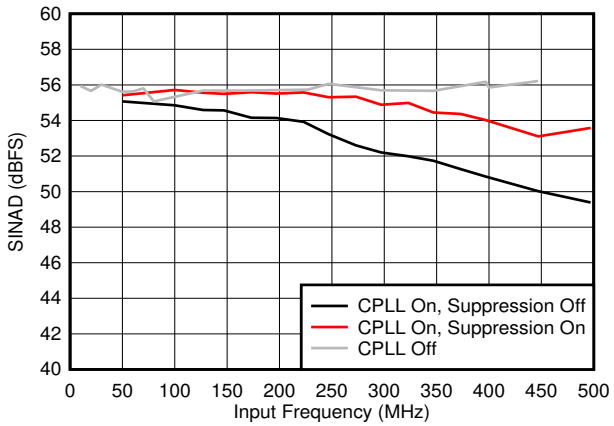
Low power mode

図 5-44. SFDR vs F_{IN} and C-PLL modes



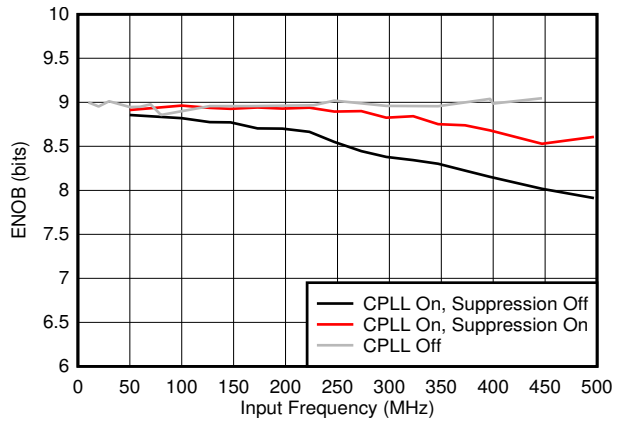
Low power mode

図 5-45. SNR vs F_{IN} and C-PLL modes



Low power mode

図 5-46. SINAD vs F_{IN} and C-PLL modes



Low power mode

図 5-47. ENOB vs F_{IN} and C-PLL modes

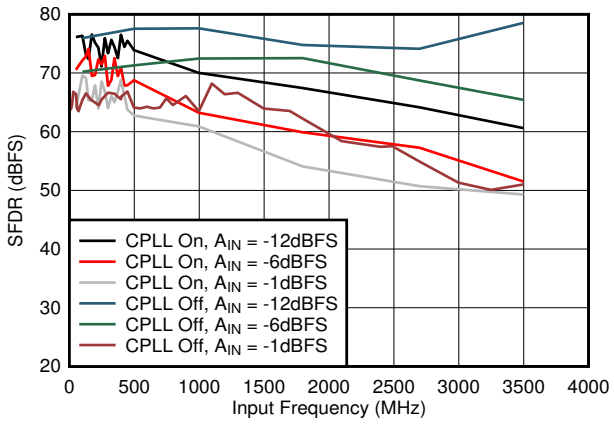


図 5-48. SFDR vs A_{IN} and C-PLL

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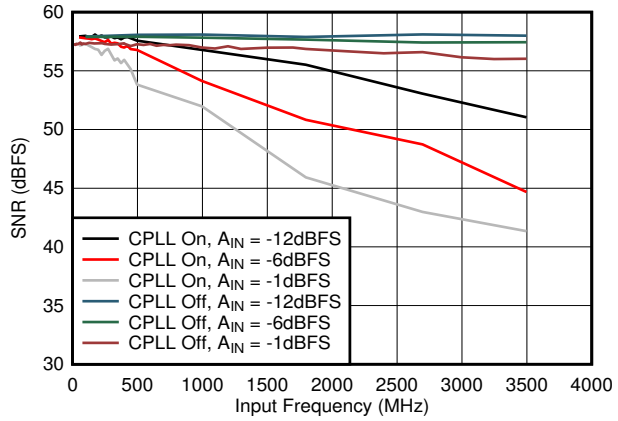


図 5-49. SNR vs A_{IN} and C-PLL

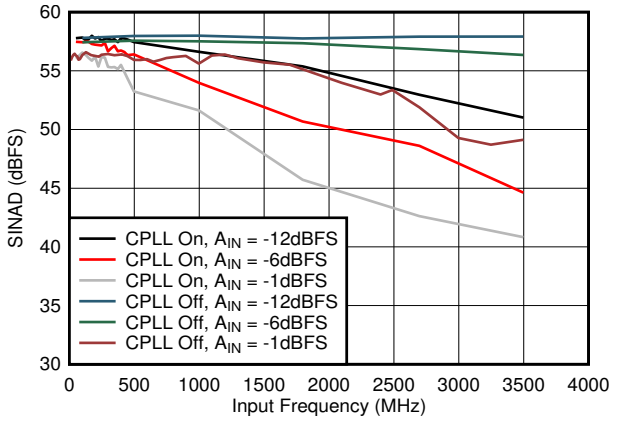


図 5-50. SINAD vs A_{IN} and C-PLL

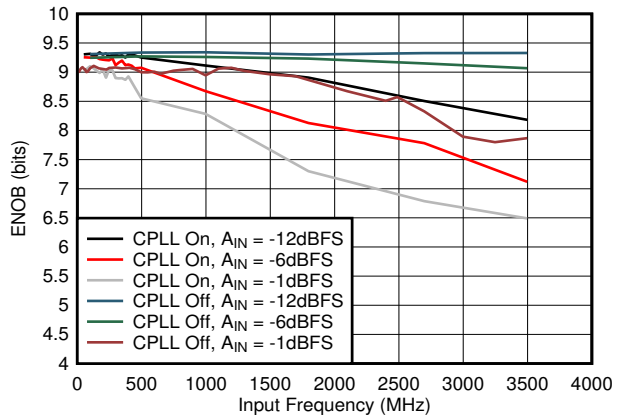


図 5-51. ENOB vs A_{IN} and C-PLL

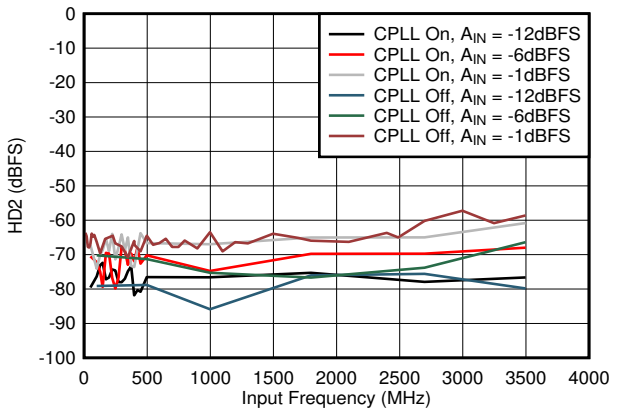


図 5-52. HD2 vs A_{IN} and C-PLL

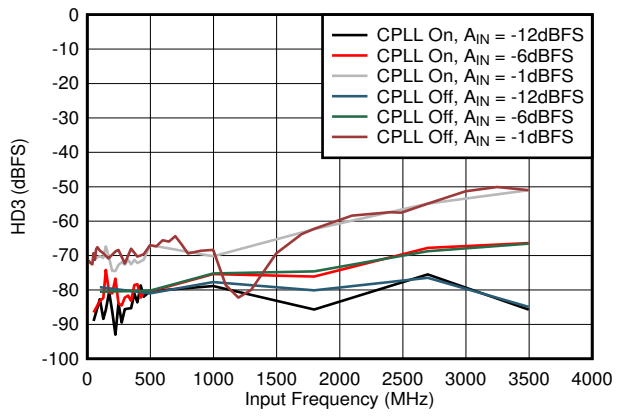
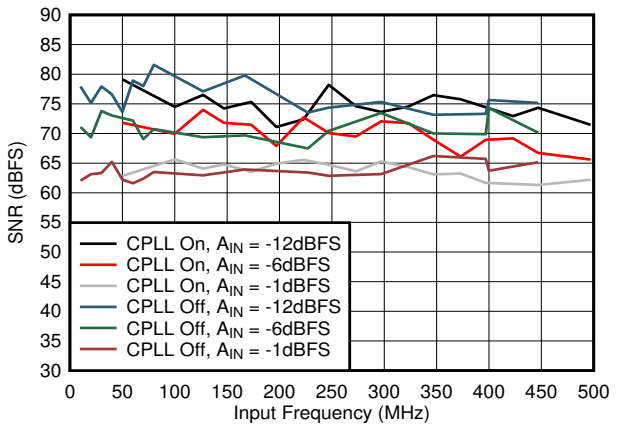


図 5-53. HD3 vs A_{IN} and C-PLL



Low power mode

図 5-54. SFDR vs A_{IN} and C-PLL

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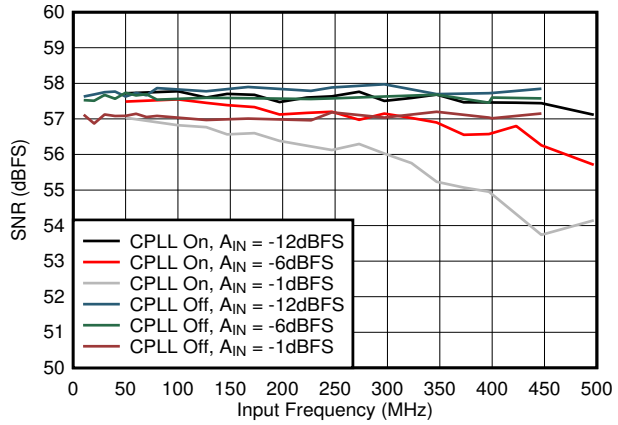
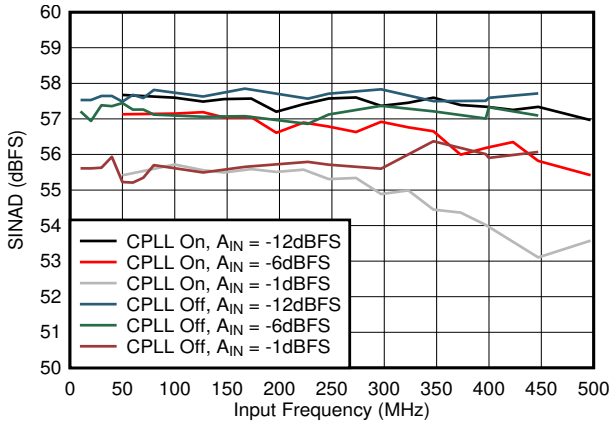


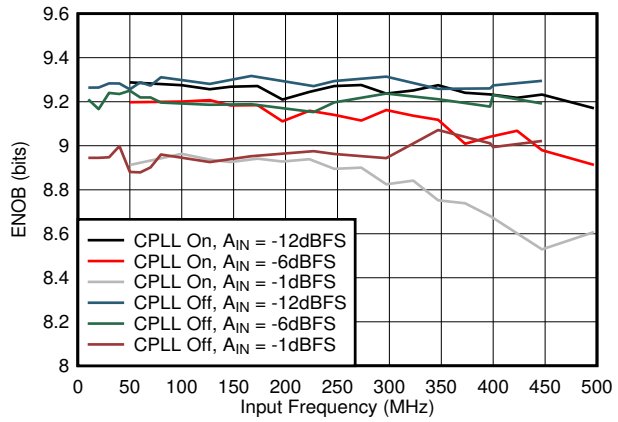
Low power mode

図 5-55. SNR vs A_{IN} and C-PLL



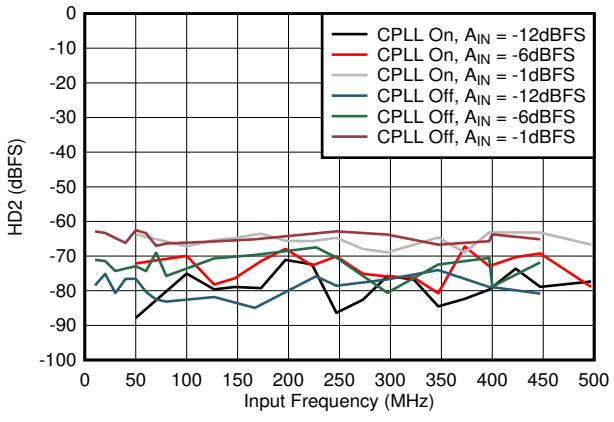
Low power mode

図 5-56. SINAD vs A_{IN} and C-PLL



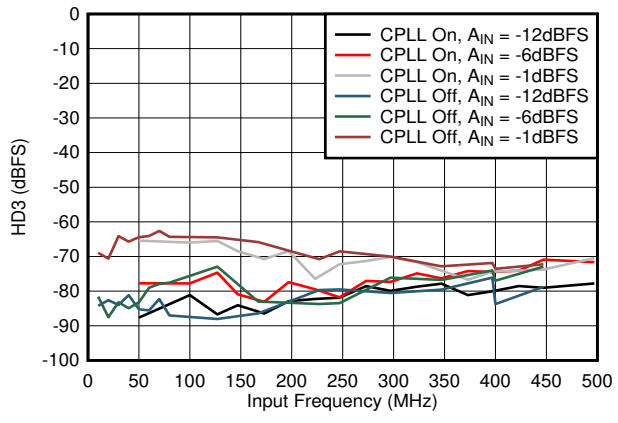
Low power mode

図 5-57. ENOB vs A_{IN} and C-PLL



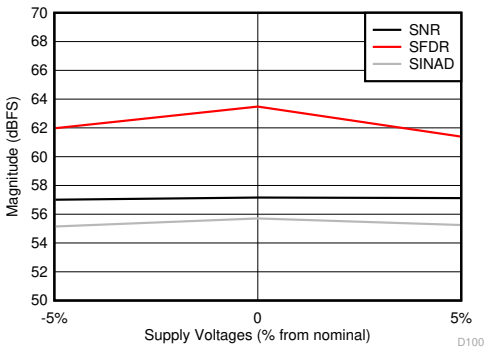
Low power mode

図 5-58. HD2 vs A_{IN} and C-PLL



Low power mode

図 5-59. HD3 vs A_{IN} and C-PLL



All supplies changed together, high power mode

図 5-60. SNR, SFDR and SINAD vs Supply Voltage

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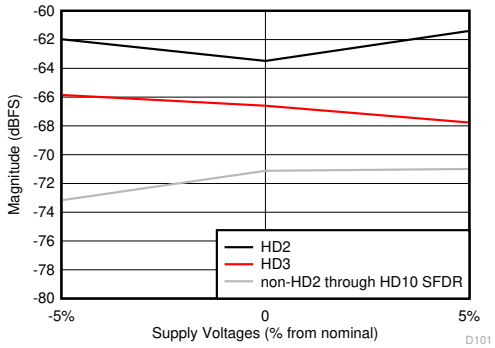
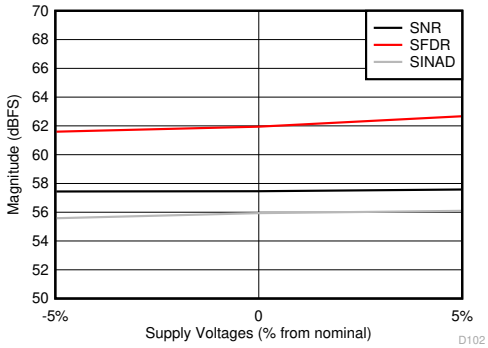


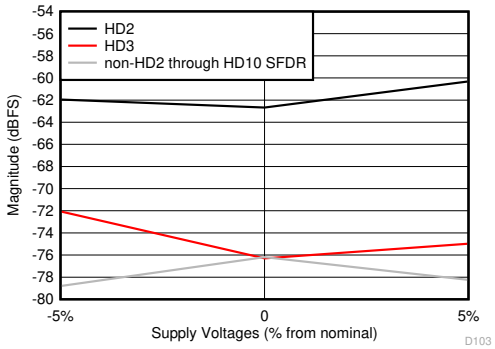
All supplies changed together, high power mode

図 5-61. HD2, HD3 and Worst non-HD Spur vs Supply Voltage



All supplies changed together, low power mode, F_S = 1000MSPS

図 5-62. SNR, SFDR and SINAD vs Supply Voltages



All supplies changed together, low power mode, F_S = 1000MSPS

図 5-63. HD2, HD3 and Worst non-HD Spur vs Supply Voltage

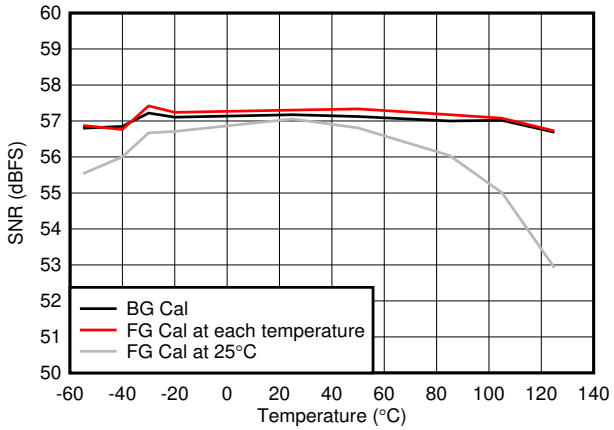


図 5-64. SNR vs Temperature

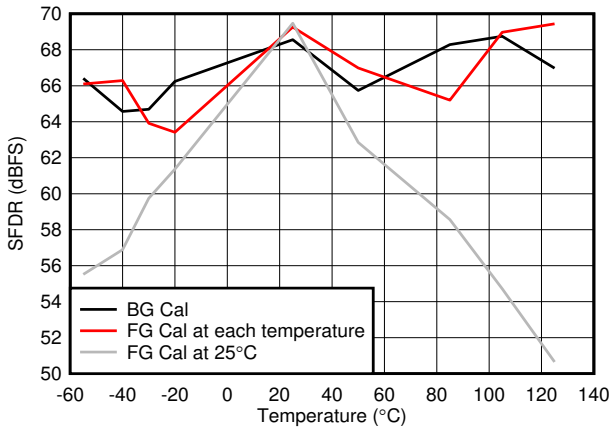


図 5-65. SFDR vs Temperature

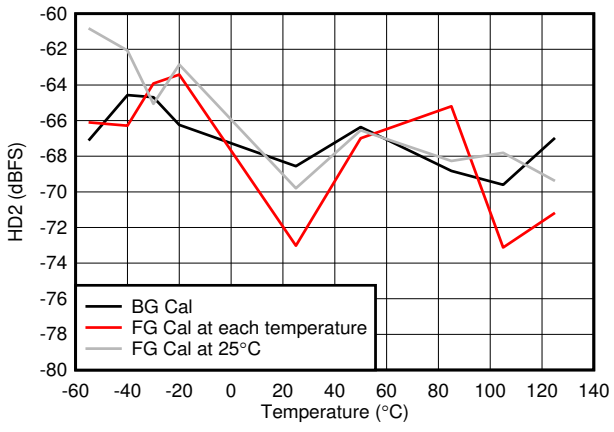


図 5-66. HD2 vs Temperature

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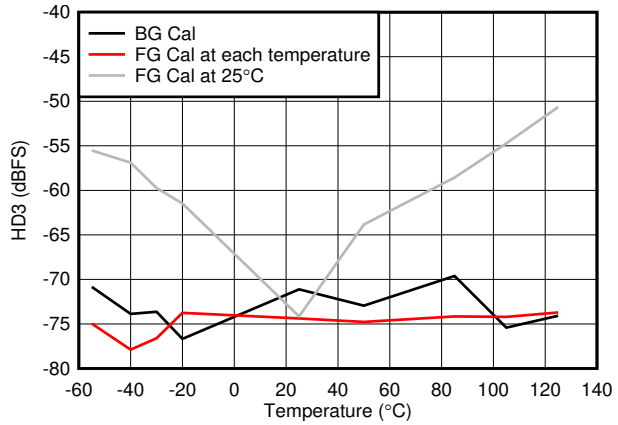
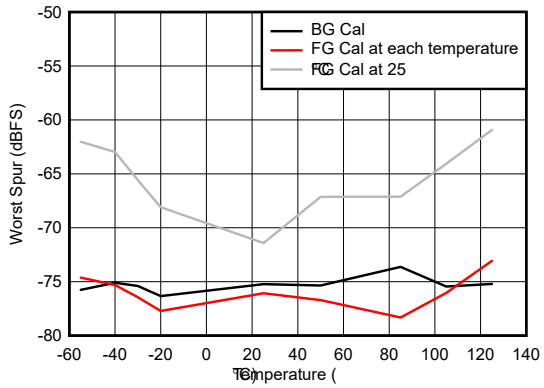
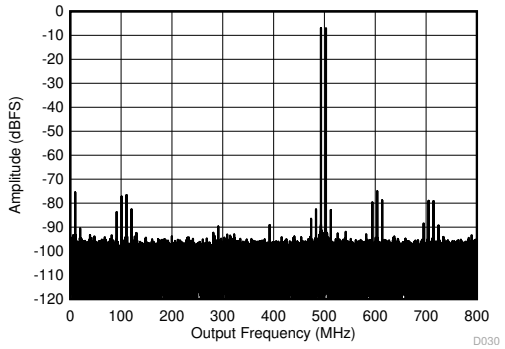


図 5-67. HD3 vs Temperature



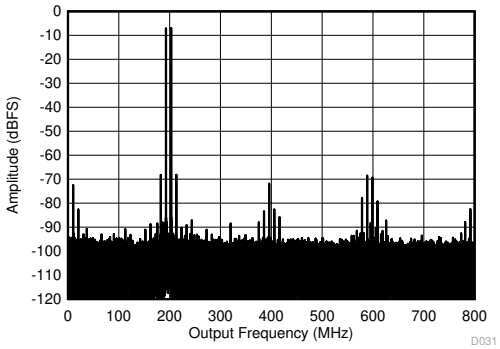
Worst spur is non-HD2 though -HD10 SDFR

図 5-68. Worst Spur vs Temperature



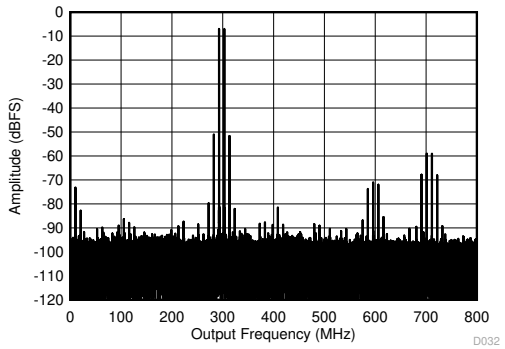
10MHz tone spacing

図 5-69. Two Tone FFT at 498MHz



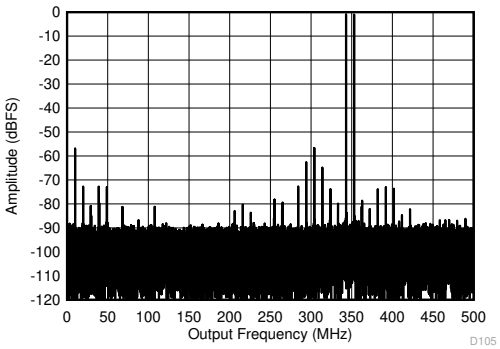
10MHz tone spacing

図 5-70. Two Tone FFT at 1798MHz



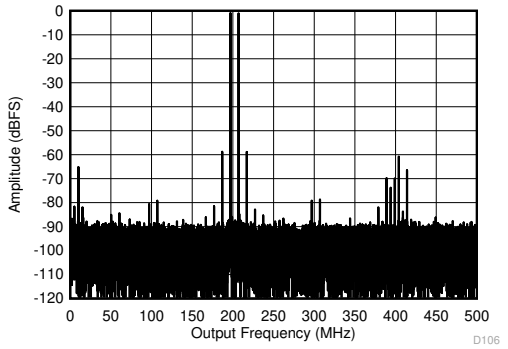
10MHz tone spacing

図 5-71. Two Tone FFT at 3498MHz



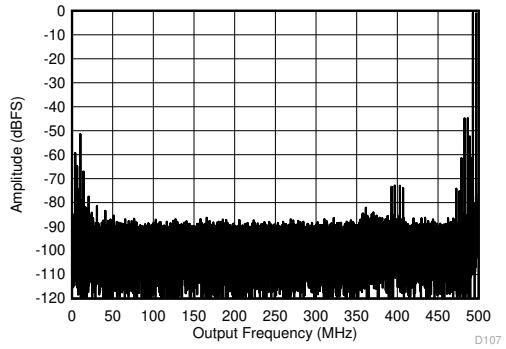
10 MHz tone spacing, -7dBFS per tone, Low power mode, 1000MSPS

図 5-72. Two Tone FFT at 348 MHz



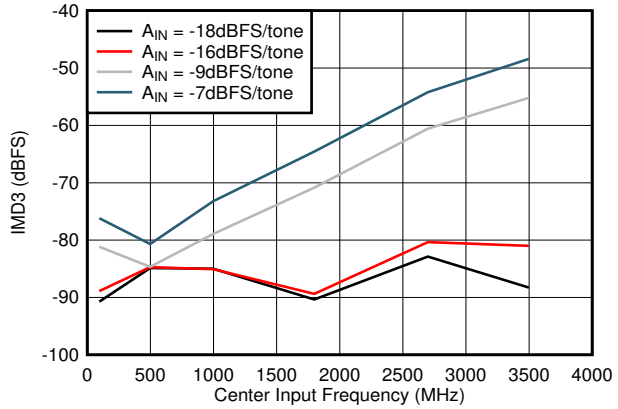
10 MHz tone spacing, -7dBFS per tone, Low power mode, 1000MSPS

図 5-73. Two Tone FFT at 1798 MHz



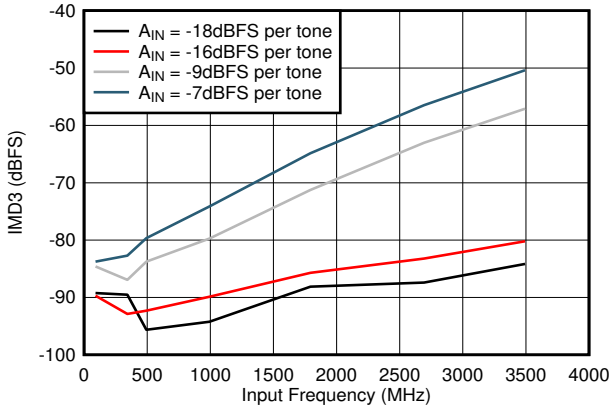
10 MHz tone spacing, -7dBFS per tone, Low power mode, 1000MSPS

図 5-74. Two Tone FFT at 3498 MHz



10MHz tone spacing

図 5-75. IMD3 vs F_{IN}



10MHz tone spacing, Low power mode, 1000MSPS

図 5-76. IMD3 vs F_{IN}

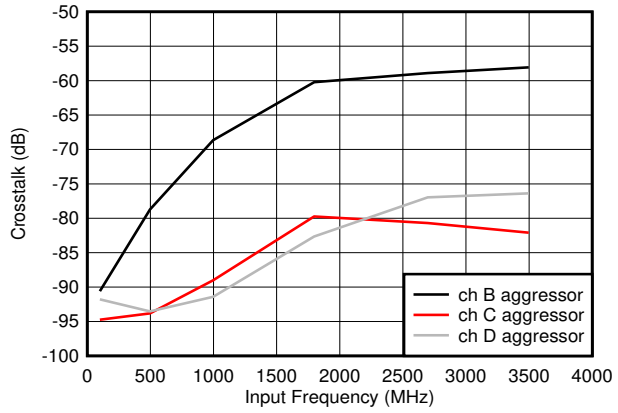


図 5-77. Crosstalk to Channel A vs F_{IN}

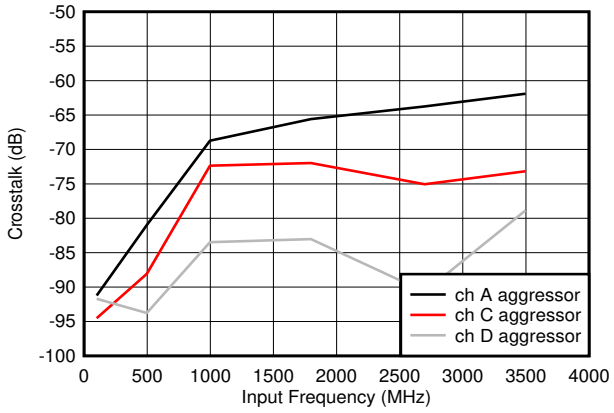


図 5-78. Crosstalk to Channel B vs F_{IN}

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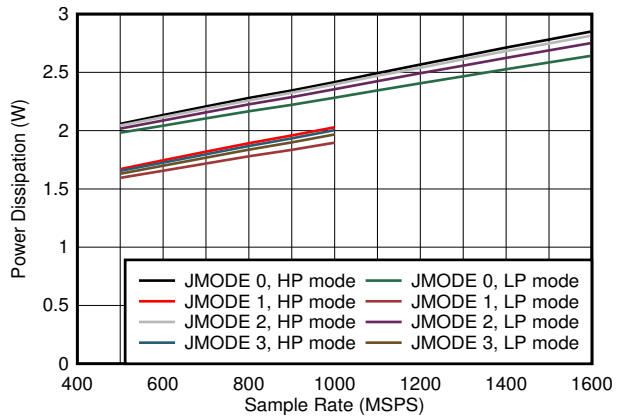
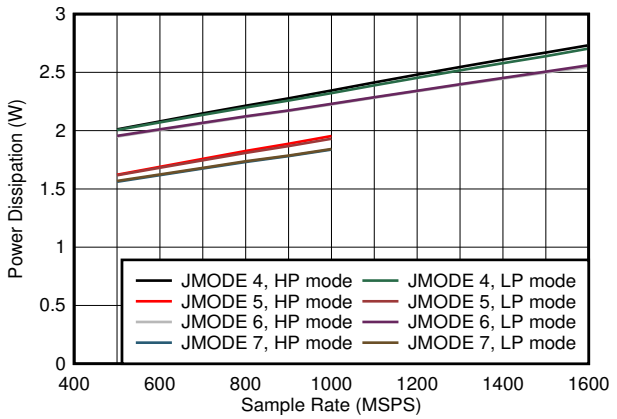


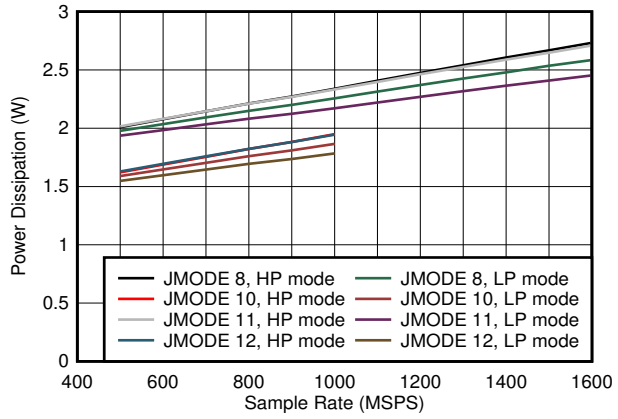
Low power background calibration mode

図 5-79. Quad Channel, Power Dissipation vs F_S and JMODES 0 - 3



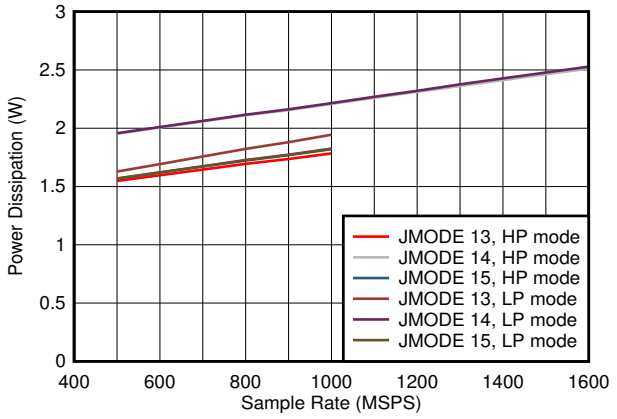
Low power background calibration mode

図 5-80. Quad Channel, Power Dissipation vs F_S and JMODE 4 - 7



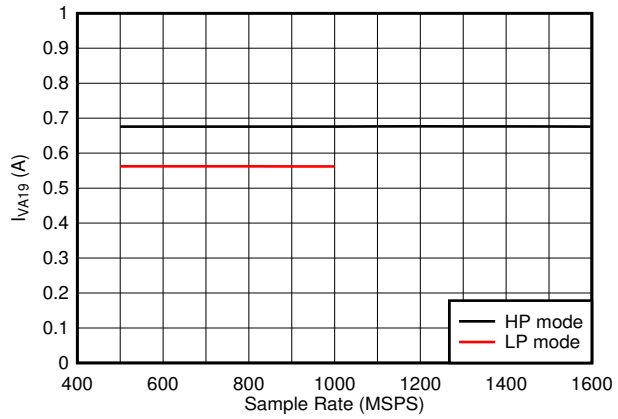
Low power background calibration mode

図 5-81. Quad Channel, Power Dissipation vs F_S and JMODE 8 - 12



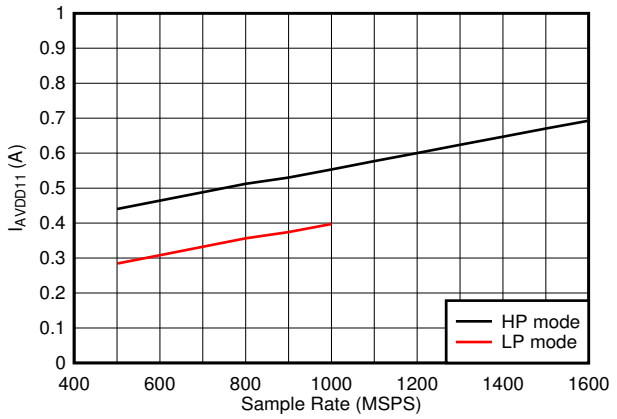
Low power background calibration mode

図 5-82. Quad Channel, Power Dissipation vs F_S and JMODE 13 - 15



Low power background calibration mode, independent of JMODE

図 5-83. Quad Channel, I_{VA19} vs F_S



Low power background calibration mode, independent of JMODE

図 5-84. Quad Channel, I_{VA11} vs F_S

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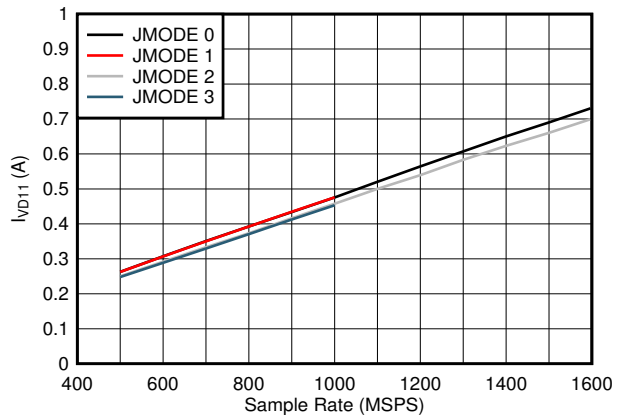
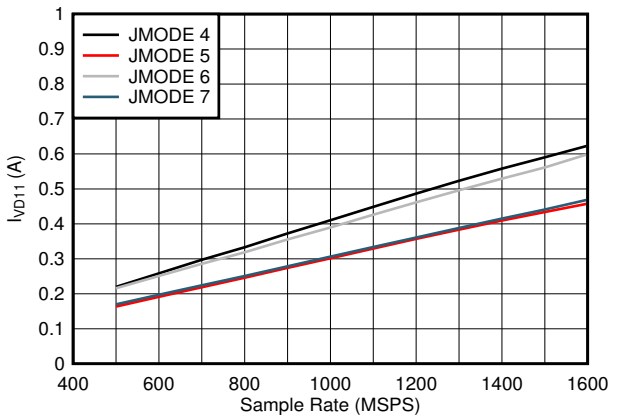


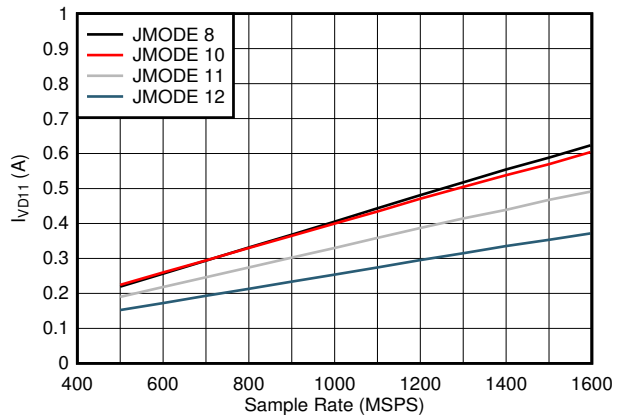
Low power background calibration mode, independent of power mode

図 5-85. Quad Channel, I_{VD11} vs F_S and JMODE 0 - 3



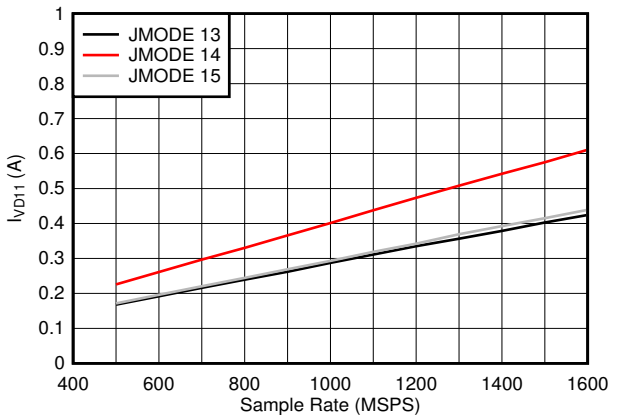
Low power background calibration mode, independent of power mode

図 5-86. Quad Channel, I_{VD11} vs F_S and JMODE 4 - 7



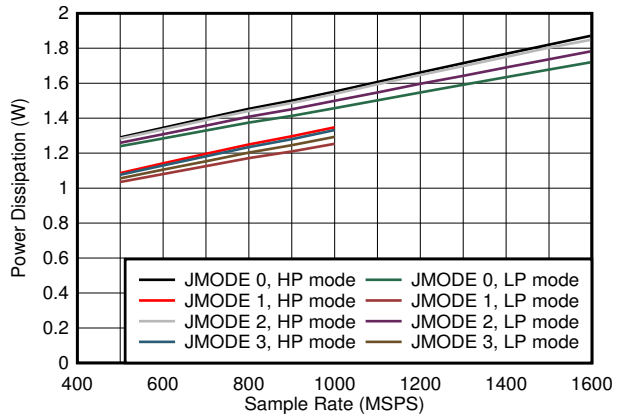
Low power background calibration mode, independent of power mode

図 5-87. Quad Channel, I_{VD11} vs F_S and JMODE 8 - 12



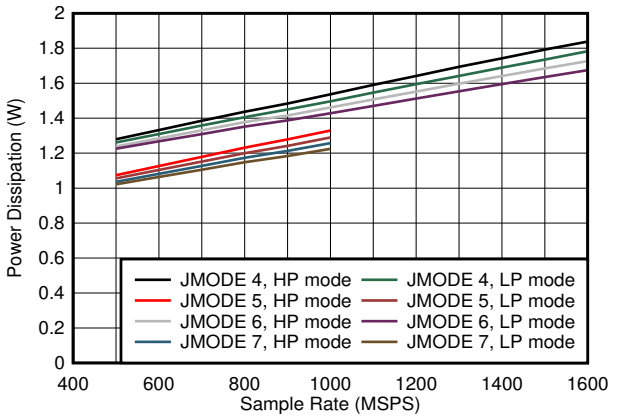
Low power background calibration mode, independent of power mode

図 5-88. Quad Channel, I_{VD11} vs F_S and JMODE 13 - 15



Low power background calibration mode

図 5-89. Dual Channel, Power Dissipation vs F_S and JMODE 0 - 3



Low power background calibration mode

図 5-90. Dual Channel, Power Dissipation vs F_S and JMODE 4 - 7

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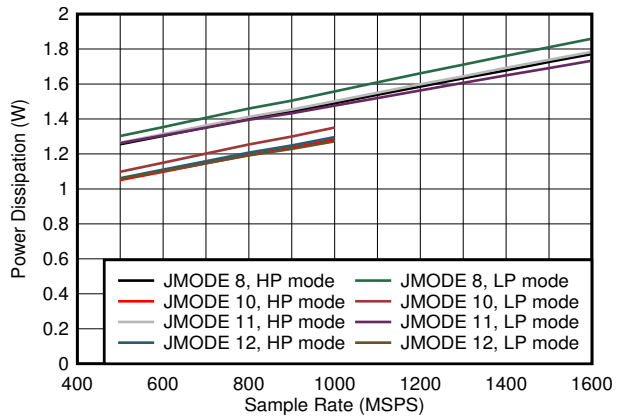
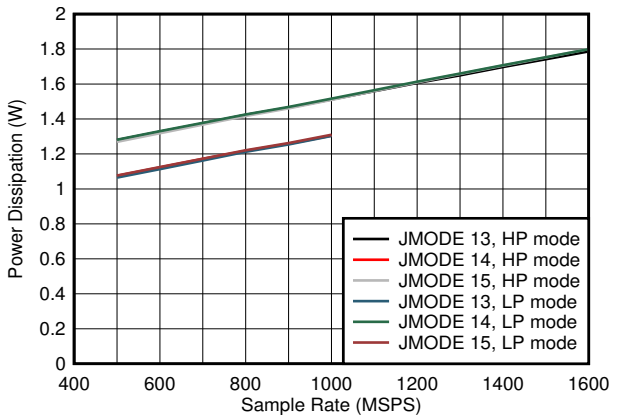


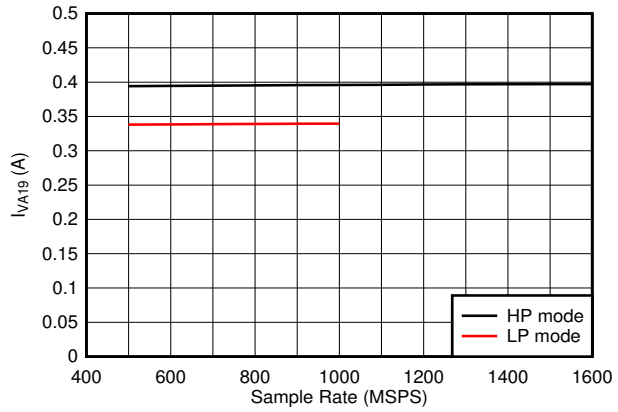
Low power background calibration mode

図 5-91. Dual Channel, Power Dissipation vs F_S and JMODE 8 - 12



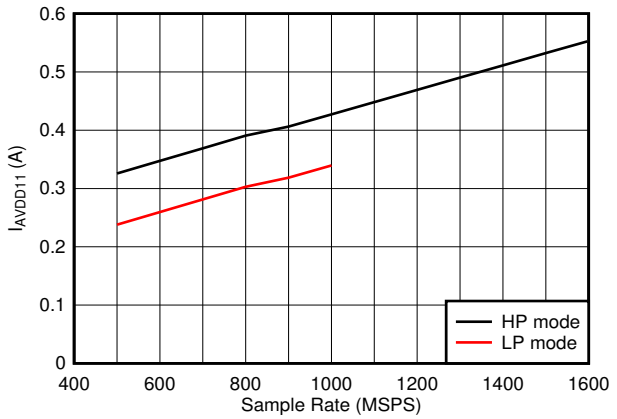
Low power background calibration mode

図 5-92. Dual Channel, Power Dissipation vs F_S and JMODE 13 - 15



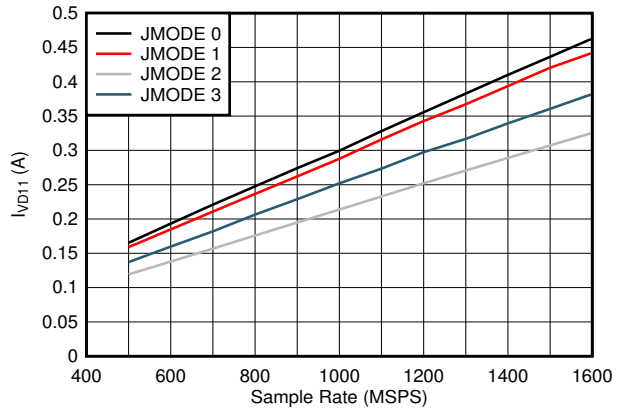
Low power background calibration mode, independent of JMODE

図 5-93. Dual Channel, I_{VA19} vs F_S



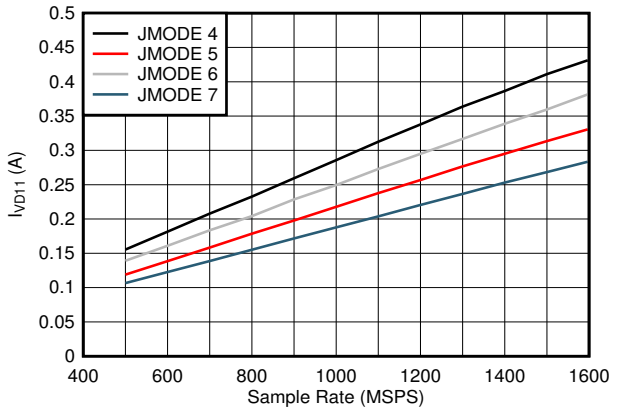
Low power background calibration mode, independent of JMODE

図 5-94. Dual Channel, I_{VA11} vs F_S



Low power background calibration mode, independent of power mode

図 5-95. Dual Channel, Power Dissipation vs F_S and JMODE 0 - 3



Low power background calibration mode, independent of power mode

図 5-96. Dual Channel, Power Dissipation vs F_S and JMODE 4 - 7

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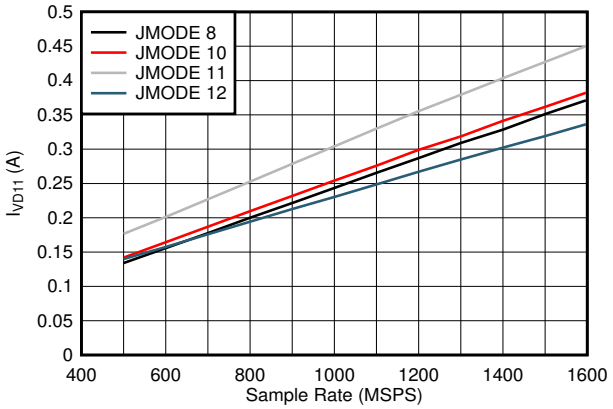
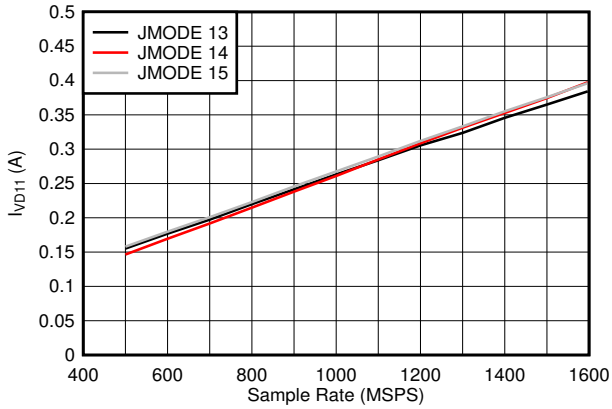


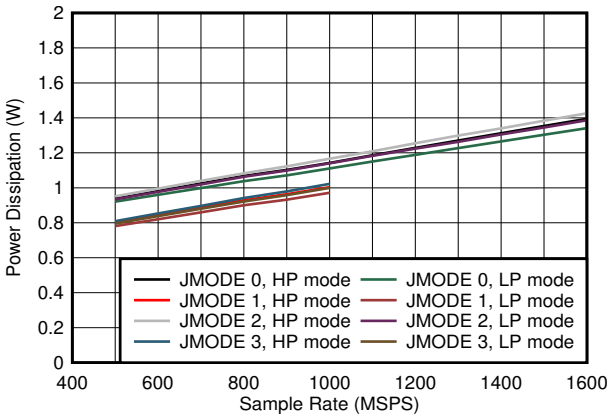
Low power background calibration mode, independent of power mode

図 5-97. Dual Channel, Power Dissipation vs F_S and JMODE 8 - 12



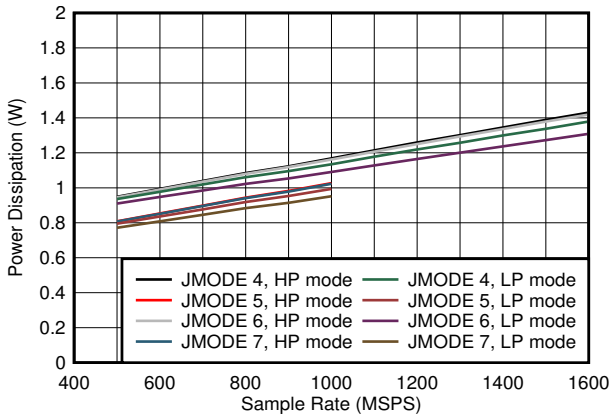
Low power background calibration mode, independent of power mode

図 5-98. Dual Channel, Power Dissipation vs F_S and JMODE 13 - 15



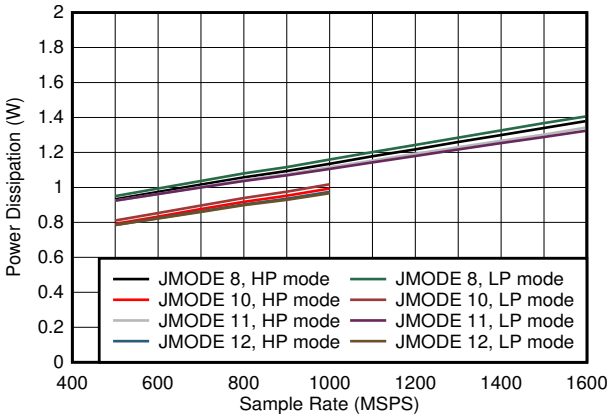
Low power background calibration mode

図 5-99. Single Channel, Power Dissipation vs F_S and JMODE 0 - 3



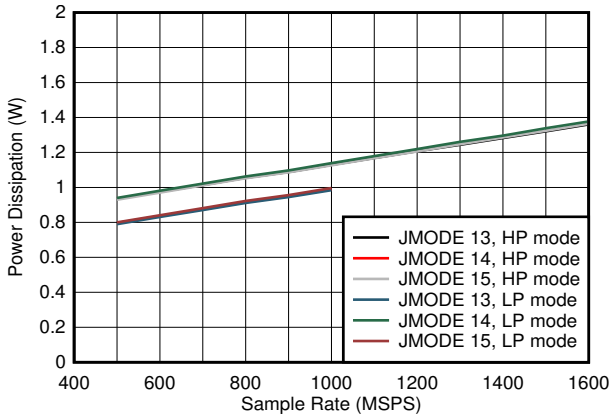
Low power background calibration mode

図 5-100. Single Channel, Power Dissipation vs F_S and JMODE 4 - 7



Low power background calibration mode

図 5-101. Single Channel, Power Dissipation vs F_S and JMODE 8 - 12



Low power background calibration mode

図 5-102. Single Channel, Power Dissipation vs F_S and JMODE 13 - 15

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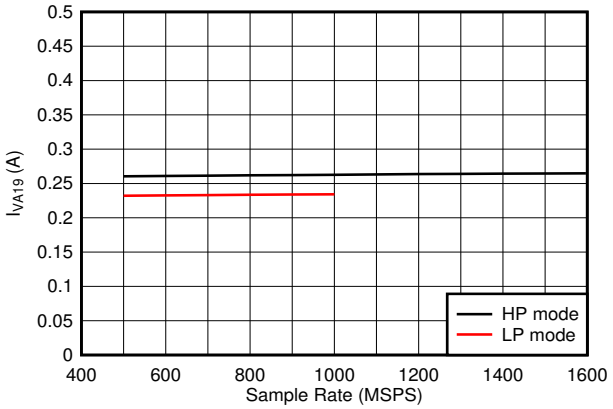
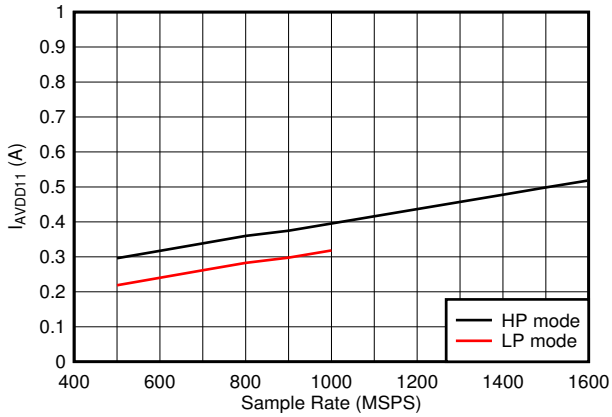


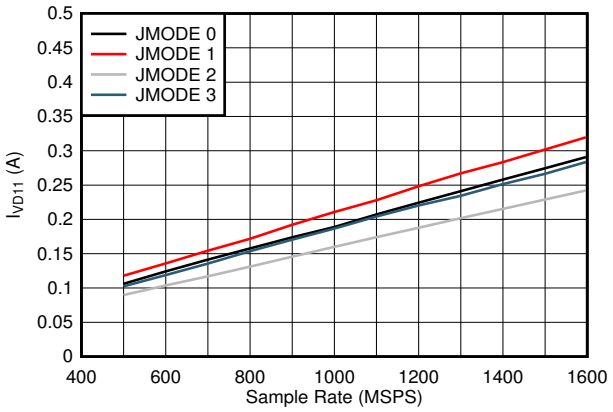
Low power background calibration mode, independent of JMODE

図 5-103. Single Channel, I_{VA19} vs F_S



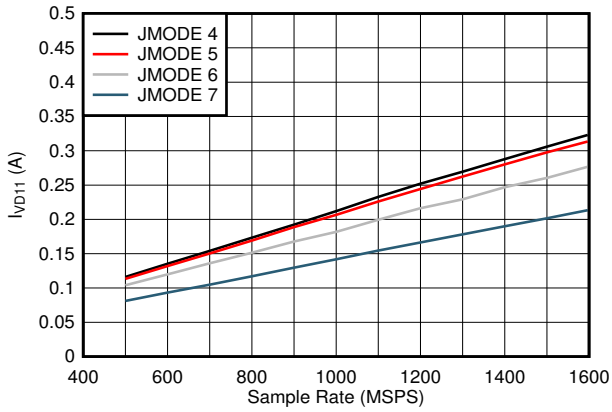
Low power background calibration mode, independent of JMODE

図 5-104. Single Channel, I_{VA11} vs F_S



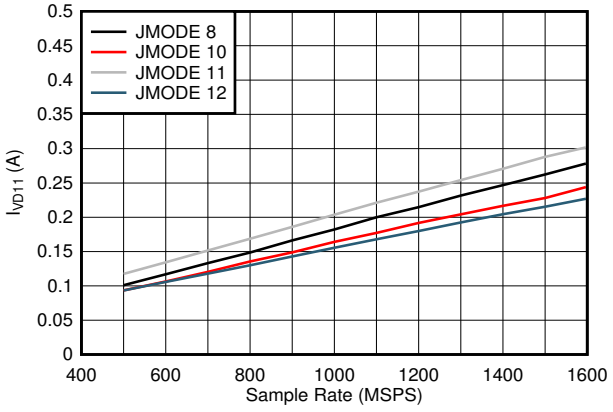
Low power background calibration mode

図 5-105. Single Channel, I_{VD11} vs F_S and JMODE 0 - 3



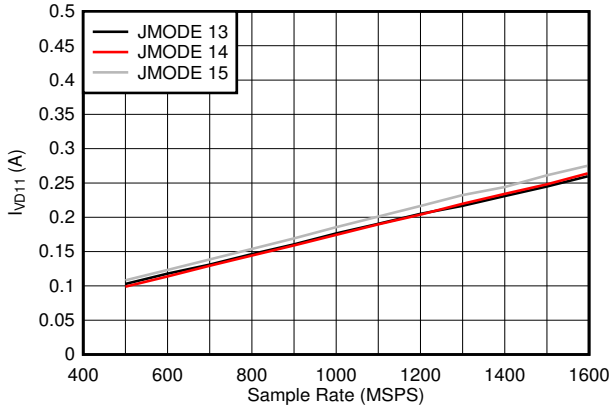
Low power background calibration mode

図 5-106. Single Channel, I_{VD11} vs F_S and JMODE 4 - 7



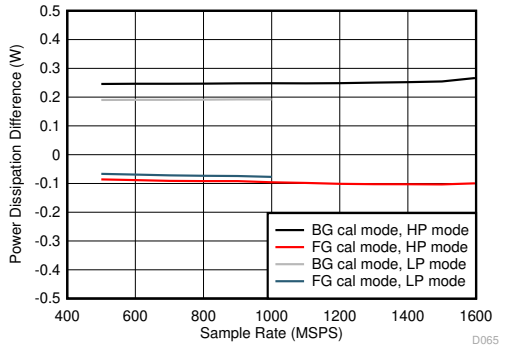
Low power background calibration mode

図 5-107. Single Channel, I_{VD11} vs F_S and JMODE 8 - 12



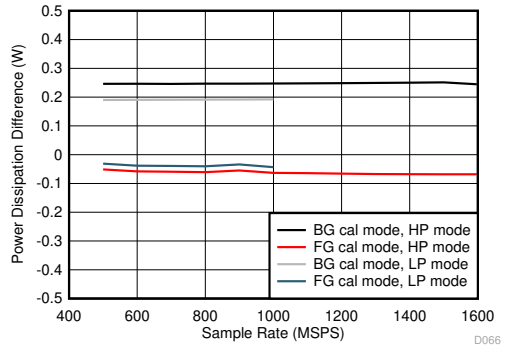
Low power background calibration mode

図 5-108. Single Channel, I_{VD11} vs F_S and JMODE 13 - 15



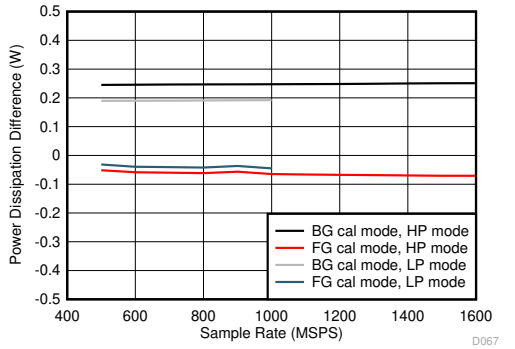
Difference to lower power background calibration, JMODE independent

図 5-109. Quad Channel, Power Dissipation Change with Calibration Mode



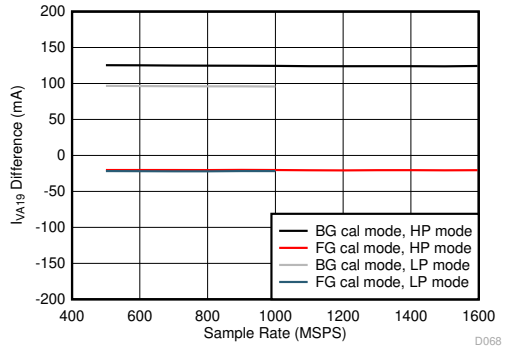
Difference to lower power background calibration, JMODE independent

図 5-110. Dual Channel, Power Dissipation Change with Calibration Mode



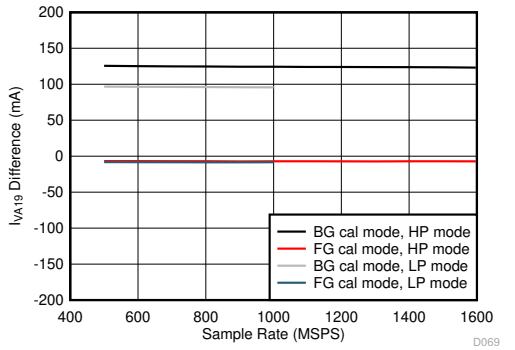
Difference to lower power background calibration, JMODE independent

図 5-111. Single Channel, Power Dissipation Change with Calibration Mode



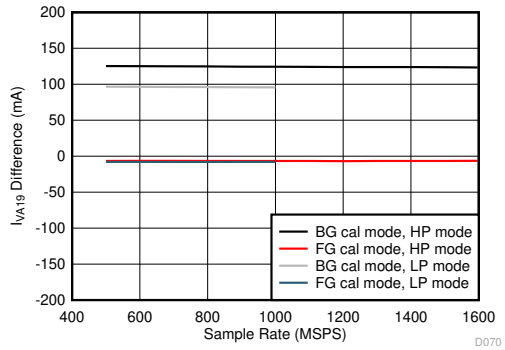
Difference to lower power background calibration, JMODE independent

図 5-112. Quad Channel, I_{VA19} Change with Calibration Mode



Difference to lower power background calibration, JMODE independent

図 5-113. Dual Channel, I_{VA19} Change with Calibration Mode



Difference to lower power background calibration, JMODE independent

図 5-114. Single Channel, I_{VA19} Change with Calibration Mode

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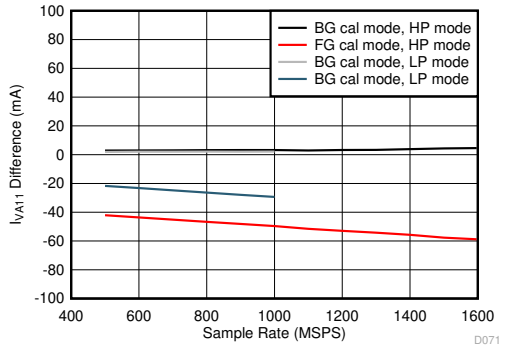
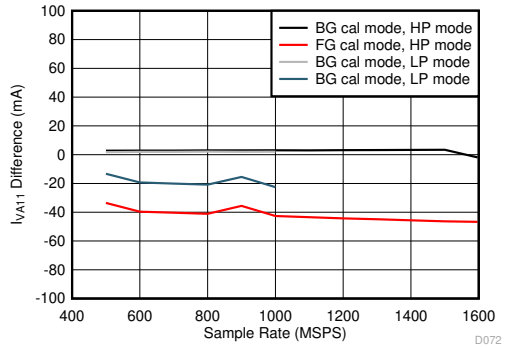


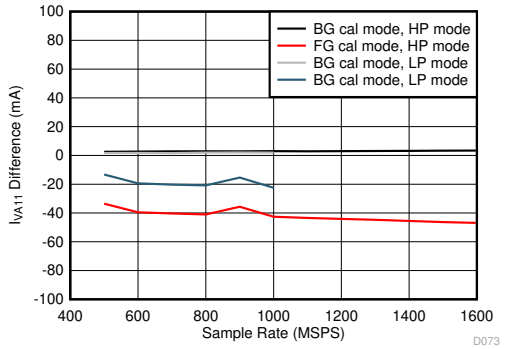
Difference to lower power background calibration, JMODE independent

図 5-115. Quad Channel, I_{VA11} Change with Calibration Mode



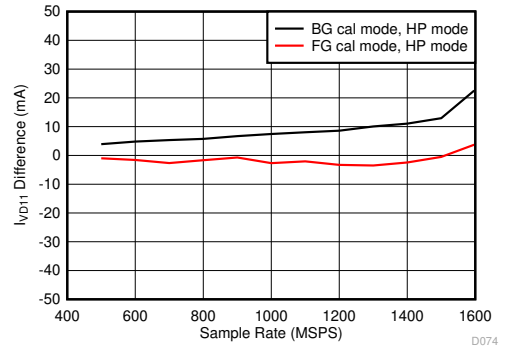
Difference to lower power background calibration, JMODE independent

図 5-116. Dual Channel, I_{VA11} Change with Calibration Mode



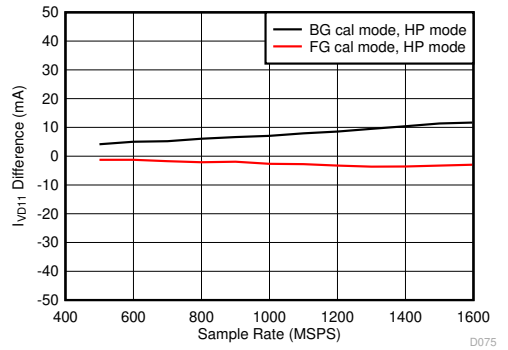
Difference to lower power background calibration, JMODE independent

図 5-117. Single Channel, I_{VA11} Change with Calibration Mode



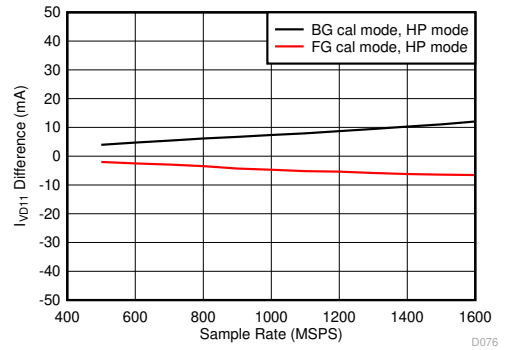
Difference to lower power background calibration, JMODE independent

図 5-118. Quad Channel, I_{VD11} Change with Calibration Mode



Difference to lower power background calibration, JMODE independent

図 5-119. Dual Channel, I_{VD11} Change with Calibration Mode



Difference to lower power background calibration, JMODE independent

図 5-120. Single Channel, I_{VD11} Change with Calibration Mode

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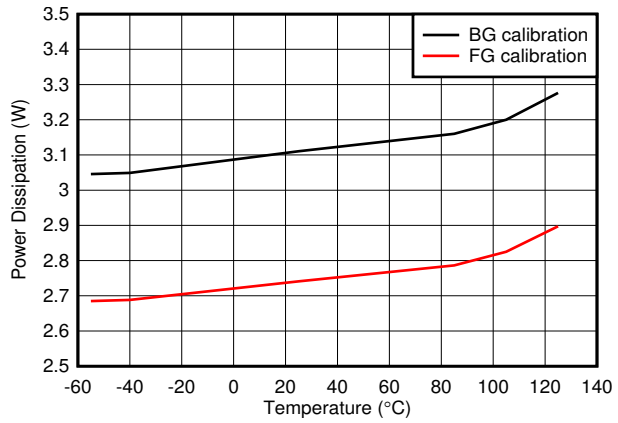


図 5-121. Quad Channel, Power Dissipation vs Temperature

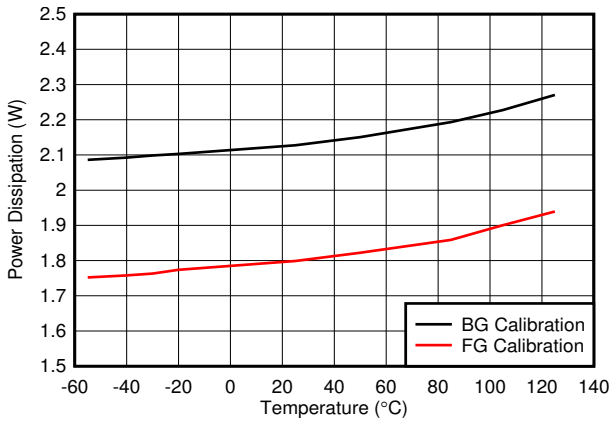


図 5-122. Dual Channel, Power Dissipation vs Temperature

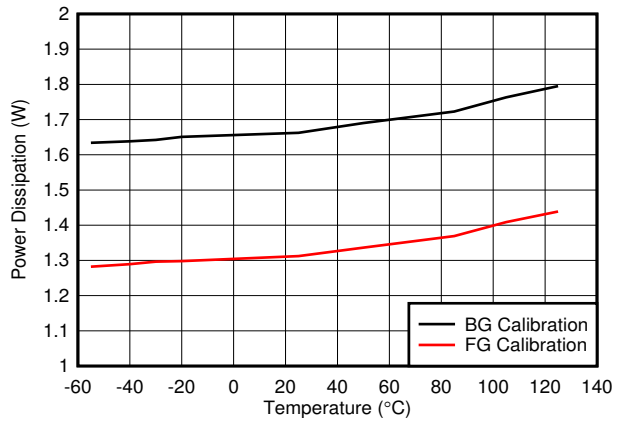
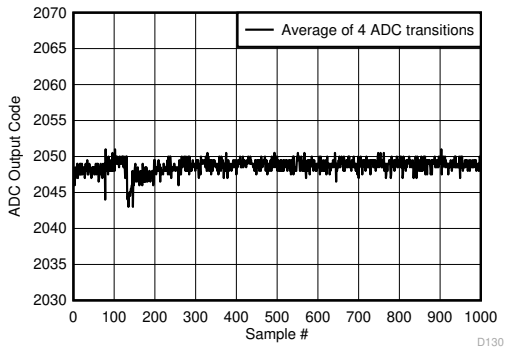
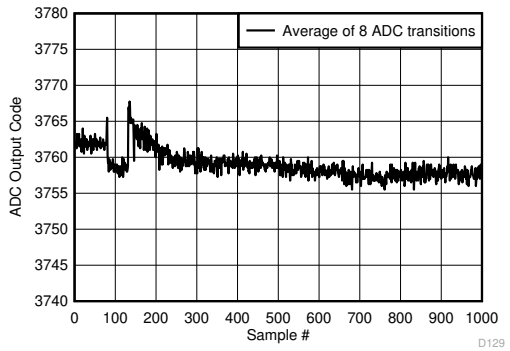


図 5-123. Single Channel, Power Dissipation vs Temperature



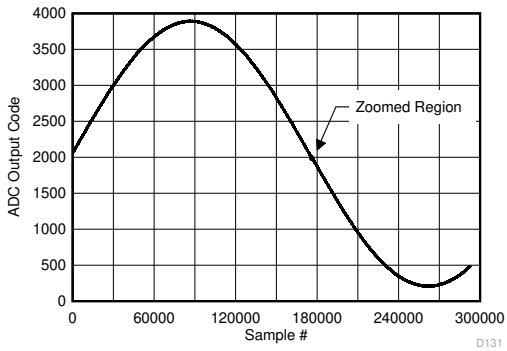
BG Calibration, midscale input voltage, ADC_SRC_DLY=31, MUX_DLY=30

図 5-124. Background Calibration Core Transition (midscale voltage)



BG Calibration, input voltage offset ~ 90% of fullscale, ADC_SRC_DLY=31, MUX_DLY=30

図 5-125. Background Calibration Core Transition (offset voltage)



BG Calibration, ADC_SRC_DLY=31, MUX_DLY=30, zoomed region shown in next plot

図 5-126. Background Calibration Core Transition (AC Signal)

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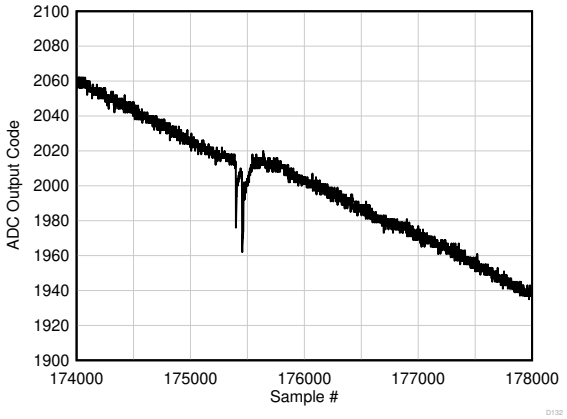

BG Calibration, ADC_SRC_DLY=31, MUX_DLY=30, unzoomed region shown in previous plot

図 5-127. Background Calibration Core Transition (AC Signal Zoomed)

6 Detailed Description

6.1 Overview

The ADC12QJ1600-Q1 is a family of quad, dual and single channel 12-bit, 1.6GSPS analog-to-digital converters (ADC). The devices have been optimized for low power consumption while maintaining high sampling rate and performance. The combination of power consumption, sampling rate and 12-bit resolution makes the device is ideally suited for light detection and ranging (LiDAR) systems. The ADC12QJ1600-Q1 is AEC-Q100 grade 1 (-40°C to 125°C) qualified for automotive applications.

The device has a buffered input with full-power input bandwidth (-3dB) of 6GHz. The wide input bandwidth provides flat frequency response for frequency domain applications, such as frequency modulated continuous wave (FMCW) LiDAR systems, and provides a narrow impulse response for time domain applications, such as and pulse-based LiDAR to achieve increased spatial resolution.

A number of clocking features are included to relax system timing requirements and simplify system architectures. The device has an internal phase-locked loop (PLL) with integrated voltage-controlled oscillator (VCO) to generate the sampling clock from a low frequency reference eliminating the need for an external high frequency clock generator. The low frequency PLL reference also relaxes timing of the SYSREF timing reference to achieve deterministic latency and multi-device synchronization. The internal PLL can be bypassed in favor of sending the high frequency sampling clock directly to the device for highest performance. A SYSREF Windowing feature relaxes the setup and hold requirement of SYSREF by directly measuring and adjusting the SYSREF delay inside of the device without the need to meet external timing requirements. The PLL reference clock can be output from the device to clock the digital logic FPGA or ASIC or an adjacent device to eliminate external clock buffer and distribution devices. Two additional CMOS outputs can send copies or divided copies of the PLL reference clock to clock additional devices in the system. A fourth clock output can output a SerDes reference clock for the transceiver block in the FPGA or ASIC to provide a complete system clocking solution. A timestamp input can be used to mark a specific sample using an external trigger. The timestamp is output over the JESD204C interface to mark the sample in the FPGA or ASIC. The timestamp signal can optionally be output from the device instead of the SerDes reference clock to replicate the retimed trigger to other devices, such as the pulse driver for a laser diode.

The JESD204C serialized interface decreases system size by reducing the amount of printed circuit board (PCB) routing by increasing the SerDes bitrate per lane and therefore decreasing the number of lanes required. JESD204C interface modes support from one to four lanes (single channel device) or two to eight lanes (dual and quad channel devices) and SerDes baud-rates up to 17.16Gbps to allow each application to choose the optimal configuration. Both 8B/10B and 64B/66B data encoding options are available. The 8B/10B encoding modes are backwards compatible with JESD204B receivers while the 64B/66B encoding modes provide higher efficiency by reducing link overhead.

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6.2 Functional Block Diagram

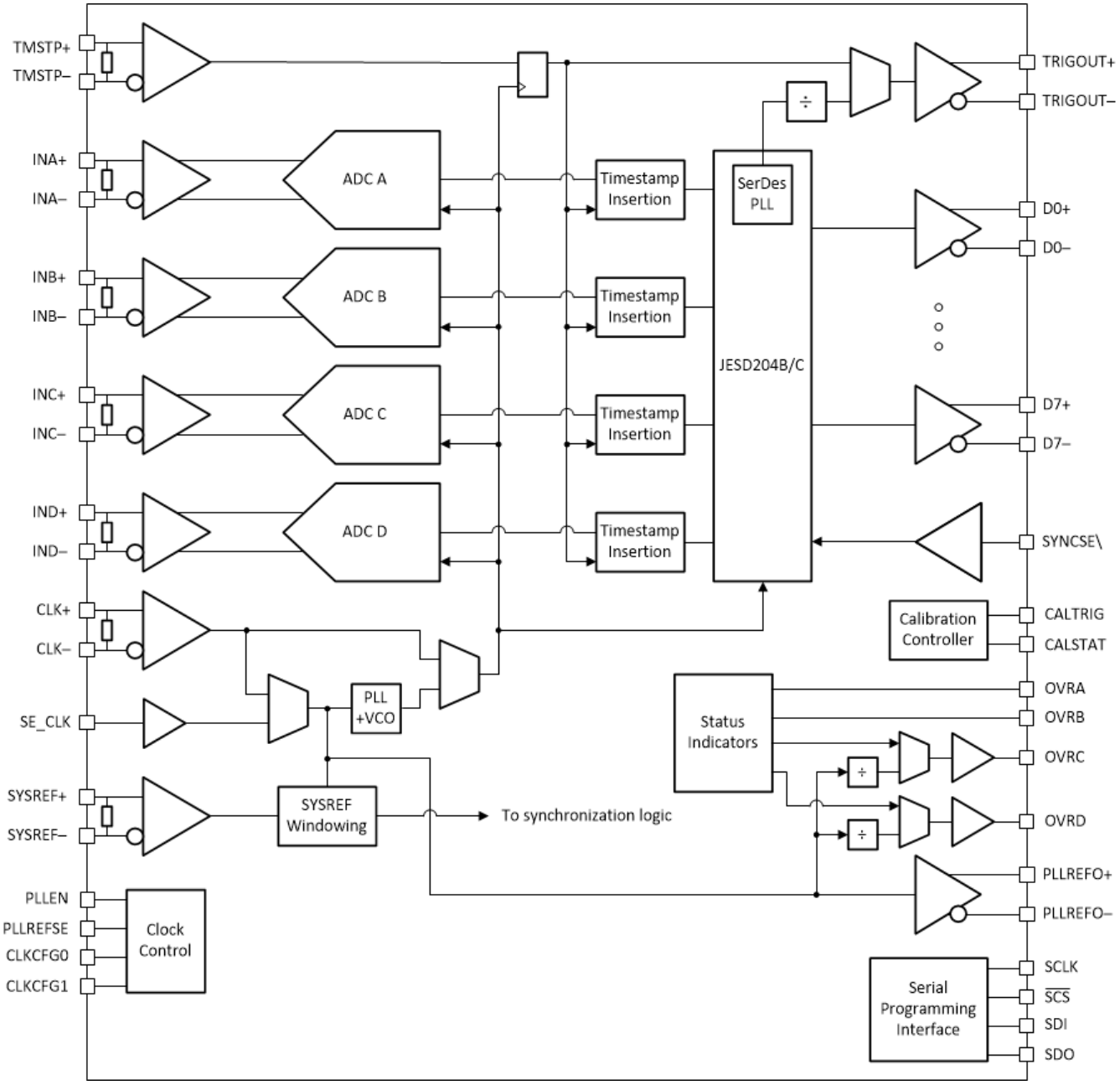

図 6-1. Quad Channel Functional Block Diagram

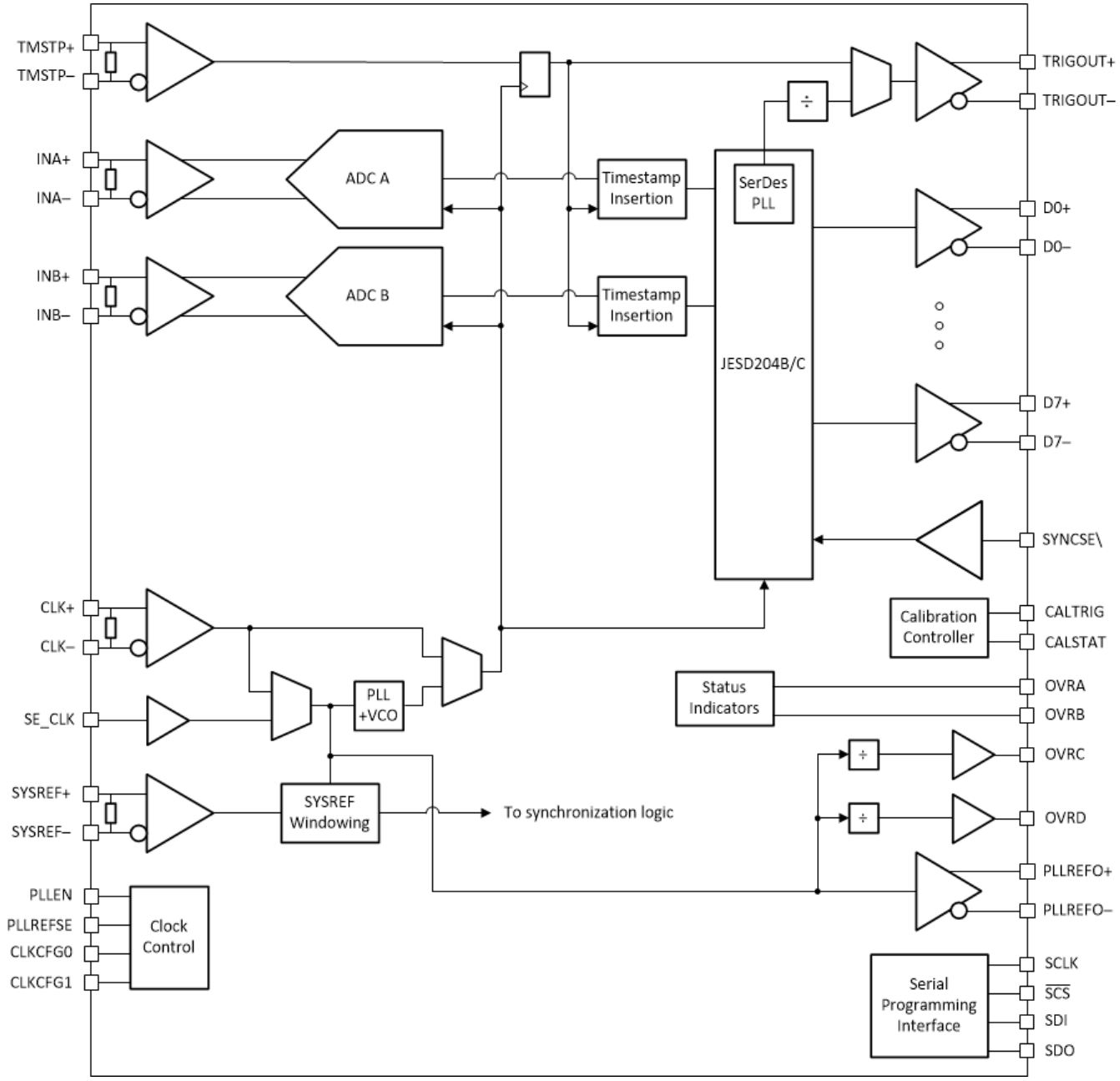

図 6-2. Dual Channel Functional Block Diagram

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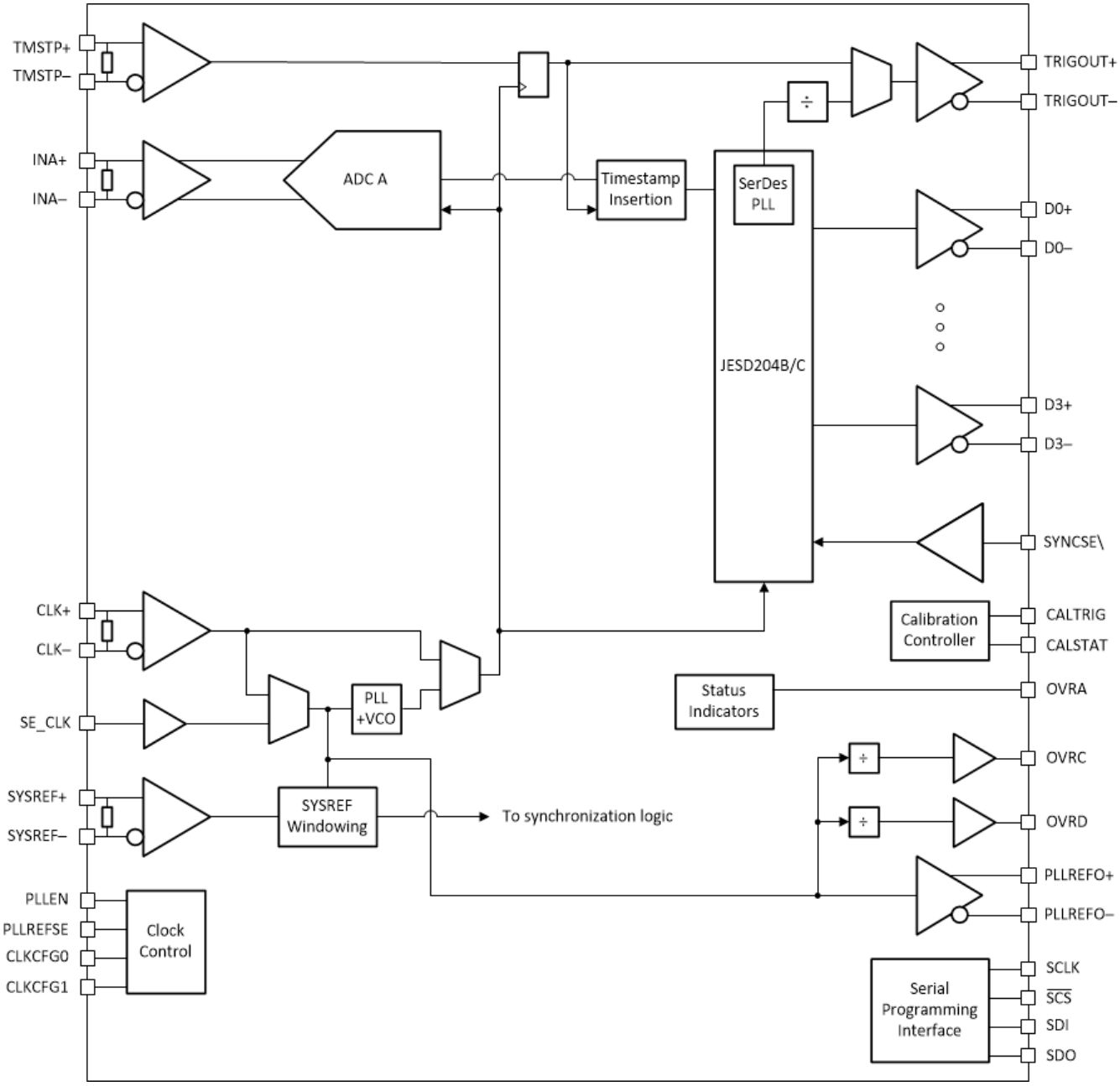

図 6-3. Single Channel Functional Block Diagram

6.3 Feature Description

6.3.1 Device Comparison

The devices listed in 表 6-1 are pin-to-pin compatible, providing a scalable family of devices for varying levels of performance, speed, and signal bandwidth.

表 6-1. Device Family Comparison

PART NUMBER (x= Q, D, S)	MAXIMUM SAMPLING RATE	RESOLUTION
ADC12xJ1600-Q1	1.6GSPS	12-bit
ADC09xJ1300-Q1	1.3GSPS	9-bit
ADC12xJ800-Q1	800MSPS	12-bit
ADC09xJ800-Q1	800MSPS	9-bit

6.3.2 Analog Input

The analog input of the device has an internal buffer to enable high input bandwidth and to isolate sampling capacitor glitch noise from the input circuit. The analog input must be driven differentially because operation with a single-ended signal results in degraded performance. Both AC-coupling and DC-coupling of the analog input is supported. The analog input is designed for an input common-mode voltage (V_{CMI}) of 1.1 V, which is terminated internally through single-ended, 50-Ω resistors to the VA11 supply on each input pin. DC-coupled input signals must have a common-mode voltage that meets the device input common-mode requirements specified as V_{CMI} in the *Recommended Operating Conditions* table. The device includes internal analog input protection to protect the ADC input during over-range input conditions; see the *Analog Input Protection* section. 図 6-4 provides a simplified analog input model.

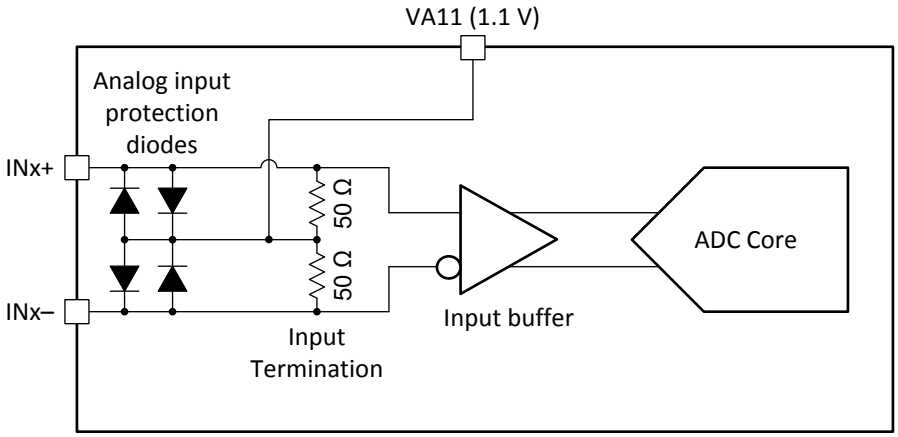

図 6-4. Analog Input Internal Termination and Protection Diagram

6.3.2.1 Analog Input Protection

6.3.2.2 Full-Scale Voltage (V_{FS}) Adjustment

Input full-scale voltage (V_{FS}) adjustment is available, in fine increments, through FS_RANGE. All inputs are set to the same full-scale voltage setting. The available adjustment range is specified in the *Recommended Operating Conditions* table. Larger full-scale voltages improve SNR and noise floor (in dBFS/Hz) performance.

6.3.2.3 Analog Input Offset Adjust

The input offset voltage for each analog input of the quad channel device can be adjusted through the OFSxy registers, where x represents the ADC core (0, 1, 2, 3, 4 or 5) and y represents the analog input for ADC core 2 (A or B) and core 3 (C or D). The y parameter is omitted for ADC core 0, 1, 4 and 5 since these cores always sample the same analog input. For the dual channel device, x represents the ADC core (0, 1, or 2) and y

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represents the analog input for ADC core 2 (A or B). The y parameter is omitted for ADC core 0 and 1 since these cores always sample the same analog input. For the single channel device, x represents the ADC core (0 or 2) and the y parameter is omitted for ADC core 0 since this core always samples the same analog input. The adjustment range is approximately 33 mV to –33 mV differential. See the *Calibration Modes and Trimming* section for more information.

6.3.2.4 ADC Core

The device consists of a total of six ADC cores for the quad channel device, three ADC cores for the dual channel device and two ADC cores for the single channel device. The cores are swapped on-the-fly for calibration as required by the operating mode. This section highlights the theory and key features of the ADC cores.

6.3.2.4.1 ADC Theory of Operation

The differential voltages at the analog inputs are captured by the rising edge of CLK±. After capturing the input signal the ADC converts the analog voltage to a digital value by comparing the voltage to the internal reference voltage. If the voltage on the negative input (that is, INA–) is higher than the voltage on the positive input (that is, INA+) then the digital output is a negative 2's complement value. If the voltage on the positive input is higher than the voltage on the negative input then the digital output is a positive 2's complement value. Equation 1 can calculate the differential voltage at the input pins from the digital output.

$$V_{IN} = \frac{Code}{2^N} V_{FS} \quad (1)$$

where

- Code is the signed decimal output code (for example, –2048 to +2047)
- N is the ADC resolution
- and V_{FS} is the full-scale input voltage of the ADC as specified in the *Recommended Operating Conditions* table, including any adjustment performed by programming FS_RANGE

6.3.2.4.2 ADC Core Calibration

ADC core calibration is required to optimize the analog performance of the ADC cores. Calibration must be repeated when operating conditions change significantly, namely temperature, in order to maintain optimal performance. The device has a built-in calibration routine that can be run as a foreground operation or a background operation. Foreground operation requires ADC downtime, where the ADC is no longer sampling the input signal, to complete the process. Background calibration can be used to overcome this limitation and allow constant operation of the ADC. See the *Calibration Modes and Trimming* section for detailed information on each mode.

6.3.2.4.3 Analog Reference Voltage

The reference voltage for the device is derived from an internal band-gap reference. A buffered version of the reference voltage is available at the BG pin for user convenience. This output has an output-current capability of ±100 µA. The BG output must be buffered if more current is required. No provision exists for the use of an external reference voltage, but the full-scale input voltage can be adjusted through the full-scale-range register settings. Note that the VA11 supply voltage should be used to set the output common-mode voltage of a front-end fully-differential amplifier and the BG output should not be used for this purpose.

6.3.2.4.4 ADC Over-range Detection

For the system gain management to have the best possible response time, a low-latency configurable over-range function is included. The over-range function works by monitoring the converted 12-bit samples at the ADC to quickly detect if the ADC is near saturation or already in an over-range condition. The absolute value of the upper 8 bits of the ADC data are checked against a programmable threshold, OVR_TH. The threshold programmed into OVR_TH is used for all analog inputs. 表 6-2 lists how an ADC sample is converted to an absolute value for a comparison of the thresholds.

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表 6-2. Conversion of ADC Sample for Over-range Comparison

ADC SAMPLE (Offset Binary)	ADC SAMPLE (2's Complement)	ABSOLUTE VALUE	UPPER 8 BITS USED FOR COMPARISON
1111 1111 1111 (4095)	0111 1111 1111 (+2047)	111 1111 1111 (2047)	1111 1111 (255)
1111 1111 0000 (4080)	0111 1111 0000 (+2032)	111 1111 0000 (2032)	1111 1110 (254)
1000 0000 0000 (2048)	0000 0000 0000 (0)	000 0000 0000 (0)	0000 0000 (0)
0000 0001 0000 (16)	1000 0001 0000 (–2032)	111 1111 0000 (2032)	1111 1110 (254)
0000 0000 0000 (0)	1000 0000 0000 (–2048)	111 1111 1111 (2047)	1111 1111 (255)

Over-range detection is enabled by setting OVR_EN to 1. If the upper 8 bits of the absolute value equal or exceed the OVR_TH threshold during the monitoring period, then the over-range bit associated with the over-ranged ADC channel is set to 1, otherwise the over-range bit is 0. For the Quad channel device, the over-range status can be monitored on the ORA, ORB, ORC or ORD output pins for ADC channels A, B, C and D, respectively. For the dual channel device, the over-range status can be monitored on the ORA or ORB output pins for ADC channels A and B, respectively. For the single channel device, the over-range status can be monitored on the ORA output pins. OVR_N can be used to set the output pulse duration from the last over-range event. 表 6-3 lists the over-range pulse lengths for the various OVR_N settings.

表 6-3. Over-range Monitoring Period

OVR_N	over-range PULSE LENGTH SINCE LAST over-range EVENT (DEVCLK Cycles)
0	8
1	16
2	32
3	64
4	128
5	256
6	512
7	1024

Typically, the OVR_TH threshold is set near the 8-bit full-scale value (228 for example). When the threshold is triggered, a typical system turns down the system gain to avoid clipping. The downstream logic device then monitors the output samples to determine when the over-range condition no longer exists and then increases the system gain as desired.

6.3.2.4.5 Code Error Rate (CER)

ADC cores can generate bit errors within a sample, often called *code errors (CER)* or referred to as *sparkle codes*, resulting from meta-stability caused by non-ideal comparator limitations. The device uses a unique ADC architecture that inherently allows significant code error rate improvements from traditional pipelined flash or successive approximation register (SAR) ADCs. The code error rate of the device is multiple orders of magnitude better than what can be achieved in alternative architectures at equivalent sampling rates providing significant signal reliability improvements.

6.3.3 Temperature Monitoring Diode

A built-in thermal monitoring diode is made available on the TDIODE+ and TDIODE– pins. This diode facilitates temperature monitoring and characterization of the device in higher ambient temperature environments. Although the on-chip diode is not highly characterized, the diode can be used effectively by performing a baseline measurement (offset) at a known ambient or board temperature and creating a linear equation with the diode voltage slope provided in the *Recommended Operating Conditions* table. Perform offset measurement with the device unpowered or with the PD pin asserted to minimize device self-heating. Only assert the PD pin long enough to take the offset measurement. Recommended monitoring devices include the LM95233 device and similar remote-diode temperature monitoring products from Texas Instruments.

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6.3.4 Timestamp

The TMSTP+ and TMSTP– differential input can be used as a time-stamp input to mark a specific sample based on the timing of an external trigger event relative to the sampled signal. The TMSTP± input is retimed to the internal sampling clock and can be repeated out of the TRIGOUT± output to trigger external devices, such as a laser driver, when TRIGOUT_EN is set to 1 to enable the TRIGOUT± output and TRIGOUT_MODE is set to 3. The TMSTP± input can also be sent over the JESD204C interface to mark a specific ADC sample. TIME_STAMP_EN must be set in order to output the timestamp data. When enabled, the timestamp signal is sent over the JESD204C interface in place of the LSB of the JESD204C mode sample size (based on N' parameter in 表 6-16, 表 6-17 and 表 6-18). For example, in JMODE 0 the JESD204C sample size (N') is 12 and therefore the timestamp information is sent at LSB ([0]) bit location and the 12-bit sample (truncated to 11-bits) is sent in the [11:1] bit location. The input applied to TMSTP± can be asynchronous to the ADC sampling clock and is sampled at approximately the same time as the analog input. Effectively, the TMSTP± input acts as a 1-bit ADC sampled in parallel with the ADC cores and both have matched latency through the device. The TMSTP± input must be enabled (TMSTP_RECV_EN) to use the timestamp feature.

6.3.5 Clocking

The input to the clocking subsystem of the device includes two clock inputs (CLK± and SE_CLK) and a synchronization signal (SYSREF±). An internal phase-locked loop (PLL) and voltage-controlled oscillator (VCO) can optionally be used to generate the ADC sampling clock from a low frequency reference by setting the PLL_EN pin high. The sampling clock PLL is called the converter PLL (C-PLL). The C-PLL reference can be provided to either the CLK± differential input or the SE_CLK single-ended input. The single-ended C-PLL reference input is selected by setting the PLLREF_SE pin high. For highest performance, the internal C-PLL can be bypassed and the sampling clock provided directly to the CLK± input when PLL_EN and PLLREF_SE are held low. Note that SE_CLK cannot be used if the C-PLL is disabled. The C-PLL reference clock can be sent to either an FPGA or ASIC or to an adjacent device through the PLLREFO± LVDS output when the PLL is enabled. Two additional copies or divided copies of PLLREFO can be output on ORC and ORD when enabled through the CLKCFG[1:0] pins or through SPI. PLLREFO and the ORC and ORD clock outputs are available at device power up when the CMOS control pins (PLL_EN, CLKCFG0 and CLKCFG1) are set appropriately and if PD is held low. Toggling PD high to power down the device also powers down the clock outputs.

In addition, the SerDes block contains a PLL, called S-PLL, that generates the SerDes output clock from the ADC sampling clock. The S-PLL generated clock can be divided and output from the TRIGOUT± LVDS output and sent to an FPGA or ASIC to clock the SerDes receivers. The SYSREF signal is captured by the chosen clock input (CLK± or SE_CLK). A SYSREF Windowing block is used to measure and optimize the setup and hold timing of the SYSREF signal relative to the selected clock input. SYSREF Windowing relaxes the timing requirement of the external signals. 図 6-5 shows the clocking subsystem.

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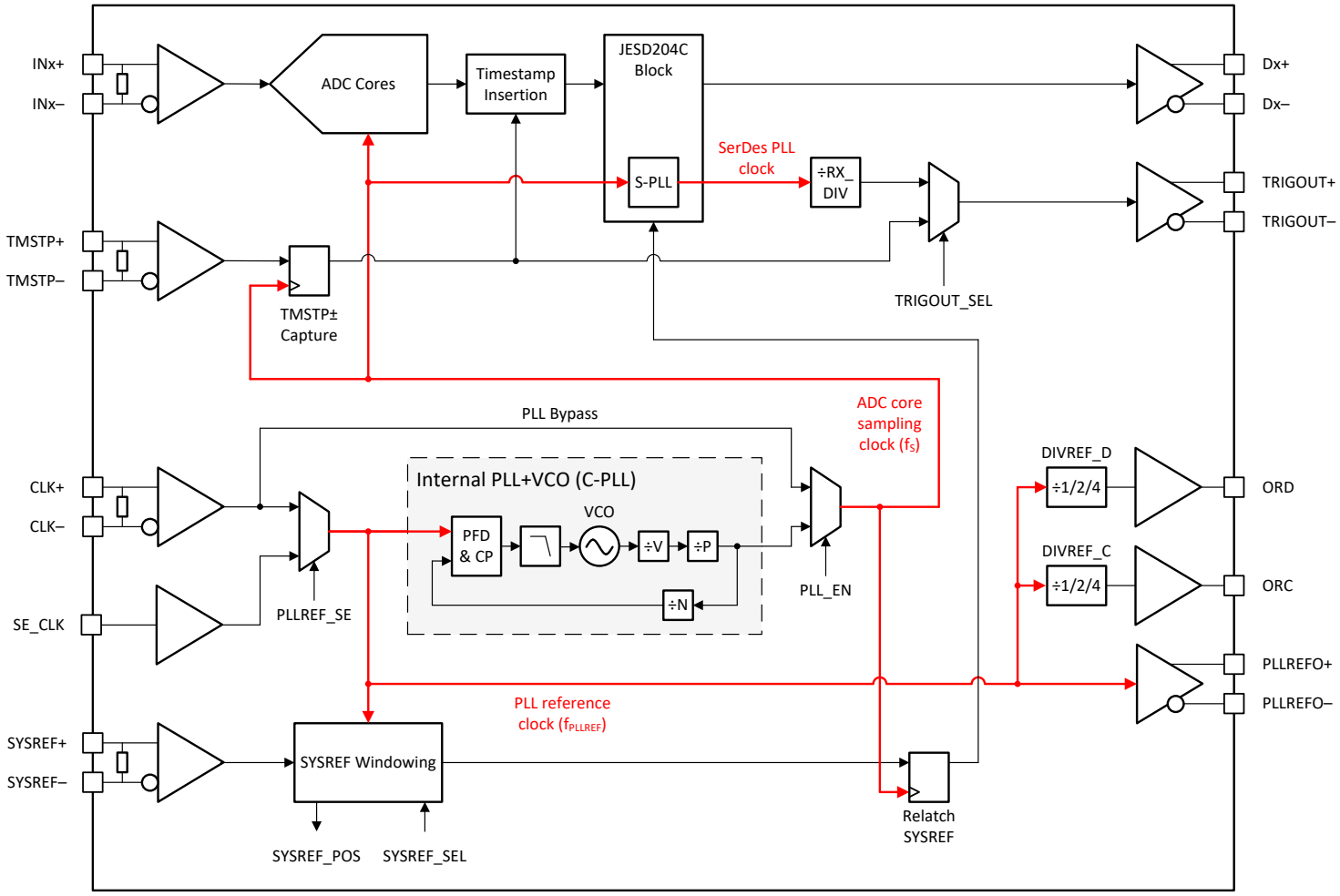

図 6-5. Clocking Subsystem

The clock generated by the C-PLL when the PLL is enabled or the clock provided to CLK± when the PLL is disabled is used as the sampling clock for the ADC core as well as the clocking for the digital processing and serializer S-PLL. Use a low-noise (low jitter) clock input, whether the PLL is enabled or disabled, to maintain high signal-to-noise ratio (SNR) within the ADC.

6.3.5.1 Converter PLL (C-PLL) for Sampling Clock Generation

An internal PLL with integrated VCO, called the converter PLL (C-PLL), is available for the high-speed sampling clock generation from a low-frequency reference signal to simplify system clocking architectures and to avoid routing of high speed clocks around the circuit board. The C-PLL architecture is shown in 図 6-6. The PLL is enabled by setting the PLL_EN pin high.

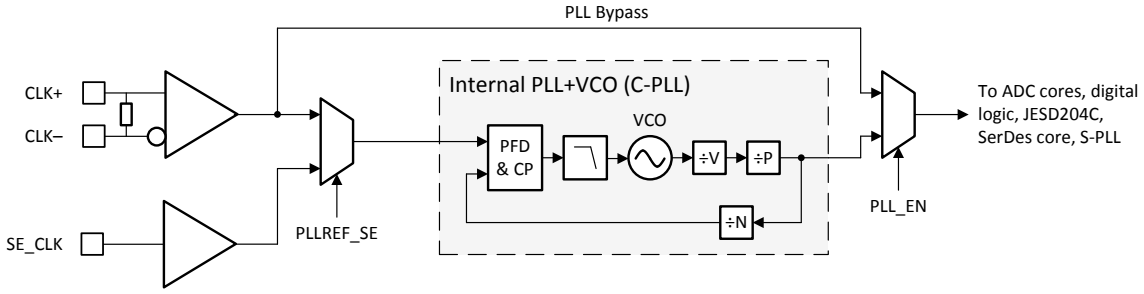

図 6-6. Converter PLL (C-PLL) Architecture

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The PLL takes a low-frequency reference clock from the CLK± pins if the PLLREF_SE pin is set low or the SE_CLK pin if the PLLREF_SE pin is set high. The reference clock is applied directly to the phase-frequency detector (PFD). The PFD compares the reference clock phase to the phase of the clock divided-down from the VCO. Therefore, the VCO frequency (f_{VCO}) divided by all of the dividers in the path (V, P, N) must be equal to the reference clock frequency (f_{REF}). The sampling frequency (f_S) is then the reference frequency times the N divider or the VCO frequency divided by the V and P dividers. The equations governing the PLL operation are given by 式 2 and 式 3.

$$f_S = f_{VCO} \div (V \times P) \quad (2)$$

where

- f_S is the ADC core sampling rate
- f_{VCO} is the VCO frequency
- V is the VCO divider
- P is the VCO prescalar

$$f_{REF} \times N = f_S \quad (3)$$

where

- f_{REF} is the PLL reference frequency
- N is the PLL feedback divider

式 4 can be used to calculate the product of the V and P dividers (V × P). Simply choose V and P such that their product equals the calculated product. 式 5 can be used to calculate the N divider based on the desired sampling rate and reference frequency.

$$V \times P = f_{VCO} \div f_S \quad (4)$$

$$N = f_S \div f_{REF} \quad (5)$$

The VCO in the device has a limited tuning range which limits the ADC sampling rates that can be generated by the PLL. The available VCO divisors (product of P and V) and resulting sampling rates are provided in 表 6-4. Only the sampling rates in 表 6-4 are available in the device when the PLL is enabled. If the desired sampling rate is not supported by the PLL then the PLL must be disabled and the desired sampling clock provided to the CLK± pins.

表 6-4. Available VCO Divisors and Achievable ADC Sampling Rates

VCO Divisor (P × V)	Minimum ADC Core Sampling Rate	Maximum ADC Core Sampling Rate
5	1440 MSPS	1600 MSPS
6	1200 MSPS	1367 MSPS
8	900 MSPS	1025 MSPS
10	720 MSPS	820 MSPS
12	600 MSPS	683 MSPS
16	500 MSPS	513 MSPS

The C-PLL should be held in reset before changing any of the C-PLL settings by setting register CPLL_RESET to 1 (address = 0x5C CPLL_RESET). The C-PLL dividers can be programmed using registers PLL_P_DIV (address = 0x3D CPLL_FBDIV1), PLL_V_DIV (address = 0x03D CPLL_FBDIV1) and PLL_N_DIV (address = 0x3E CPLL_FBDIV2). After programming the dividers the VCO calibration should be run by first setting register VCO_CAL_EN to 1 (address = 0x5D VCO_CAL_CNTL). The VCO calibration is run when register CPLL_RESET (address = 0x5C CPLL_RESET) is set to 0 to take the C-PLL out of reset. Calibration is finished

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and the C-PLL is locked when register VCO_CAL_DONE (address = 0x5E VCO_CAL_STATUS) returns 1 and register CPLL_LOCKED (address = 0x208 JESD_STATUS) is 1.

The C-PLL includes noise suppression options for the VA11Q and VCLK11 that reduce the sampling jitter and reference clock input spur at the expense of approximately 20mA of current each. The control bits are found in the CLK_CTRL2 register (address = 0x2B CLK_CTRL2).

6.3.5.2 LVDS Clock Outputs (PLLREFO±, TRIGOUT±)

Two LVDS clock outputs are provided to simplify system clocking architectures. These outputs are shown in 図 6-5. The first LVDS clock output is PLLREFO±. PLLREFO± repeats the PLL reference clock directly from the selected reference clock input (CLK± or SE_CLK) as determined by PLLREF_SE. The PLLREFO± output is automatically enabled when the C-PLL is enabled, but can be disabled by setting PLLREFO_EN to 0. This output is only available when the PLL_EN pin is set high and when PD is set low. Setting PD high disables this output; and therefore, PD should not be used if PLLREFO± is necessary for system operation. Example use cases for PLLREFO± include driving the digital core fabric of an FPGA or ASIC or it can be daisy chained to the CLK± input pins of an additional device to provide the PLL reference clock for the second device. The PLLREFO± outputs can be daisy chained to the CLK± inputs of as many ADC12QJ1600-Q1 devices as required by the system. Note that SYSREF must be provided from a separate clock source (clock chip, FPGA, ASIC, etc) and setup and hold times must be met at each device relative to the reference clock input in order to achieve deterministic latency and synchronization.

The second LVDS clock output is TRIGOUT±. This output can come from either the TMSTP± input (as a timestamp or trigger output) or from the JESD204C SerDes PLL (S-PLL). This clock output is not available at device startup and must be enabled through the SPI interface. The S-PLL can be divided by the RX_DIV divider and output from the TRIGOUT± pins as a reference clock for FPGA or ASIC transceiver block. Enable the TRIGOUT± output and set the TRIGOUT± operating mode (including RX_DIV divider) through the TRIGOUT_CTRL register. The TRIGOUT± clock output frequency can be calculated by Equation 6 when the S-PLL is chosen as the TRIGOUT± source.

$$f_{TRIGOUT} = f_{LINERATE} \div RX_DIV \quad (6)$$

where

- $f_{TRIGOUT}$ is the TRIGOUT± output clock frequency (MHz)
- $f_{LINERATE}$ is the SerDes linerate (Mbps)
- RX_DIV is the S-PLL output divider

6.3.5.3 Optional CMOS Clock Outputs (ORC, ORD)

Additional CMOS PLL reference clock outputs are available on ORC and ORD when configured through CLKCFG[1:0] or through SPI. The clock outputs are available at device power up when CLKCFG[1:0] are used to enable the clock outputs and when PD is held low. Setting the PD pin high disables these outputs; and therefore, the PD pin should not be used when these clocks are necessary for system operation. SPI register overrides are available for the CLKCFG[1:0] pins through the DIVREF_C_MODE and DIVREF_D_MODE SPI register settings. Note that CLKCFG[1:0] can be used to enable or disable ORC and ORD and set the output divider for ORC, but cannot set the output divider for ORD (enable or disable only). The DIVREF_C and DIVREF_D functionality has higher priority than over-range as reflected in 表 6-5 and 表 6-6. Using these outputs as clock outputs results in spurs in the ADC output spectrum at the output frequency and harmonics of the output frequency. Limit the capacitive loading on these outputs to less than 10 pF to limit the noise impact.

注

The DIVREF_D function is only available if DIVREF_C is also enabled (DIVREF_C_MODE > 0). If only one clock output is required connect the external device to ORC and enable the DIVREF_C function.

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表 6-5. Setting ORC Functionality

CPLL_OVR_EN	CLKCFG1	CLKCFG0	DIVREF_C_MODE	OVR_EN	ORC Function
0	0	0	X	0	Disabled
0	0	0	X	1	Quad channel: Over-range for channel C Dual/single channel: Disabled
0	0	1	X	X	PLL Reference
0	1	0	X	X	PLL Reference / 2
0	1	1	X	X	PLL Reference / 4
1	X	X	0x0	0	Disabled
1	X	X	0x0	1	Quad channel: Over-range for channel C Dual/single channel: Disabled
1	X	X	0x1	X	PLL Reference
1	X	X	0x2	X	PLL Reference / 2
1	X	X	0x3	X	PLL Reference / 4

表 6-6. Setting ORD Functionality

CPLL_OVR_EN	CLKCFG1	CLKCFG0	DIVREF_D_MODE	OVR_EN	ORD Function
0	0	0	X	0	Disabled
0	0	0	X	1	Quad channel: Over-range for channel D Dual/single channel: Disabled
0	0	1	X	X	PLL Reference
0	1	0	X	X	PLL Reference
0	1	1	X	X	PLL Reference
0	0	0	0x0	0	Disabled
1	X	X	0x0	1	Quad channel: Over-range for channel D Dual/single channel: Disabled
1	X	X	0x1	X	PLL Reference
1	X	X	0x2	X	PLL Reference / 2
1	X	X	0x3	X	PLL Reference / 4

6.3.5.4 SYSREF for JESD204C Subclass-1 Deterministic Latency

SYSREF is a system timing reference used for JESD204C subclass-1 implementations of deterministic latency. SYSREF is used to achieve deterministic latency and for multi-device synchronization. SYSREF must be captured by the correct device clock edge in order to achieve repeatable latency and synchronization. The device includes a SYSREF Windowing feature to ease the requirements on the external clocking circuits and to simplify the synchronization process. SYSREF Windowing replaces the traditional setup and hold times as these are no longer required when SYSREF Windowing is used. SYSREF can be implemented as a single pulse or as a periodic clock. In periodic implementations, SYSREF must be equal to, or an integer division of, the local multiframe clock frequency in 8B/10B encoding modes or the local extended multiblock clock frequency in 64B/66B encoding modes. Equation 7 is used to calculate valid SYSREF frequencies in 8B/10B encoding modes. In 64B/66B modes, the denominator changes to 66 × 32 × E × n, where E is the number of multiblocks in an extended multiblock.

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$$f_{SYSREF} = \frac{R \times f_{CLK}}{10 \times F \times K \times n} \quad (7)$$

where

- R and F are set by the JMODE setting (see 表 6-16, 表 6-17 and 表 6-18)
- f_{CLK} is the device clock frequency (CLK±)
- K is the programmed multiframe length (see 表 6-16, 表 6-17 and 表 6-18 for valid K settings)
- and n is any positive integer

6.3.5.4.1 SYSREF Capture for Multi-Device Synchronization and Deterministic Latency

The clocking subsystem is largely responsible for achieving multi-device synchronization and deterministic latency. The device uses the JESD204C subclass-1 method to achieve deterministic latency and synchronization. Subclass 1 requires that the SYSREF signal be captured by a deterministic clock (CLK± or SE_CLK) edge at each system power-on and at each device in the system. This requirement imposes setup and hold constraints on SYSREF relative to CLK±, which can be difficult to meet at giga-sample clock rates over all system operating conditions. The device includes a number of features to simplify this synchronization process and to relax system timing constraints:

- The ADC12QJ1600-Q1 includes an integrated PLL and VCO to generate the high frequency sampling clock, relaxing the timing requirement by requiring timing to only be met relative to a low frequency reference clock.
- A SYSREF position detector (relative to CLK± or SE_CLK) and selectable SYSREF sampling position aid the user in meeting setup and hold times over all conditions; see the *SYSREF Windowing* section

6.3.5.4.2 SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing)

The SYSREF Windowing block is used to first detect the position of SYSREF relative to the input clock (CLK± or SE_CLK) rising edge and then to select a desired SYSREF sampling instance, which is a delayed version of the input clock, to maximize setup and hold timing margins. In many cases a single SYSREF sampling position (SYSREF_SEL) is sufficient to meet timing for all systems (device-to-device variation) and conditions (temperature and voltage variations). However, this feature can also be used by the system to expand the timing window by tracking the movement of SYSREF as operating conditions change or to remove system-to-system variation at production test by finding a unique optimal value at nominal conditions for each system.

This section describes proper usage of the SYSREF Windowing block. First, apply the device clock and SYSREF to the device. The location of SYSREF relative to the device clock cycle is determined and stored in the SYSREF_POS field. Each bit of SYSREF_POS represents a potential SYSREF sampling position. If a bit in SYSREF_POS is set to 1, then the corresponding SYSREF sampling position has a potential setup or hold violation. Upon determining the valid SYSREF sampling positions (the positions of SYSREF_POS that are set to 0) the desired sampling position can be chosen by setting SYSREF_SEL to the value corresponding to that SYSREF_POS position. In general, the middle sampling position between two setup and hold instances is chosen. Ideally, SYSREF_POS and SYSREF_SEL are performed at the nominal operating conditions of the system (temperature and supply voltage) to provide maximum margin for operating condition variations. This process can be performed at final test and the optimal SYSREF_SEL setting can be stored for use at every system power up. Further, SYSREF_POS can be used to characterize the skew between CLK± and SYSREF± over operating conditions for a system by sweeping the system temperature and supply voltages. For systems that have large variations in CLK± to SYSREF± skew, this characterization can be used to track the optimal SYSREF sampling position as system operating conditions change. In general, a single value can be found that meets timing over all conditions for well-matched systems, such as those where CLK± and SYSREF± come from a single clocking device.

The step size between each SYSREF_POS sampling position can be adjusted using SYSREF_ZOOM. When SYSREF_ZOOM is set to 0, the delay steps are coarser. When SYSREF_ZOOM is set to 1, the delay steps are finer. See the *Recommended Operating Conditions* table for delay step sizes when SYSREF_ZOOM is enabled and disabled. In general, SYSREF_ZOOM is recommended to always be used (SYSREF_ZOOM = 1) unless a transition region (defined by 1's in SYSREF_POS) is not observed, which can be the case for low clock rates.

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Bits 0 and 23 of SYSREF_POS are always be set to 1 because there is insufficient information to determine if these settings are close to a timing violation, although the actual valid window can extend beyond these sampling positions. The value programmed into SYSREF_SEL is the decimal number representing the desired bit location in SYSREF_POS. 表 6-7 lists some example SYSREF_POS readings and the optimal SYSREF_SEL settings. Although 24 sampling positions are provided by the SYSREF_POS status register, SYSREF_SEL only allows selection of the first 16 sampling positions, corresponding to SYSREF_POS bits 0 to 15. The additional SYSREF_POS status bits are intended only to provide additional knowledge of the SYSREF valid window. In general, lower values of SYSREF_SEL are selected because of delay variation over supply voltage, however in the fourth example a value of 15 provides additional margin and can be selected instead.

表 6-7. Examples of SYSREF_POS Readings and SYSREF_SEL Selections

SYSREF_POS[23:0]			OPTIMAL SYSREF_SEL SETTING
0x02E[7:0] (Largest Delay)	0x02D[7:0](1)	0x02C[7:0](1) (Smallest Delay)	
b10000000	b01100000	b00011001	8 or 9
b10011000	b00000000	b00110001	12
b10000000	b01100000	b00000001	6 or 7
b10000000	b00000011	b00000001	4 or 15
b10001100	b01100011	b00011001	6

(1) Red coloration indicates the bits that are selected, as given in the last column of this table.

6.3.6 JESD204C Interface

The device uses a JESD204C high-speed serial interface for data converters to transfer data from the ADC to the receiving logic device. The device serialized lanes are capable of operating with both 8B/10B encoding and 64B/66B encoding. The JESD204C output formats using 8B/10B encoding are backwards compatible with existing JESD204B receivers. A maximum of 8 lanes can be used to lower lane rates for interfacing with speed-limited logic devices. There are a few differences between 8B/10B and 64B/66B encoded JESD204C, which is highlighted throughout this section. 図 6-7 shows a simplified block diagram of the 8B/10B encoded JESD204C interface and 図 6-8 shows a simplified block diagram of the 64B/66B encoded JESD204C interface.

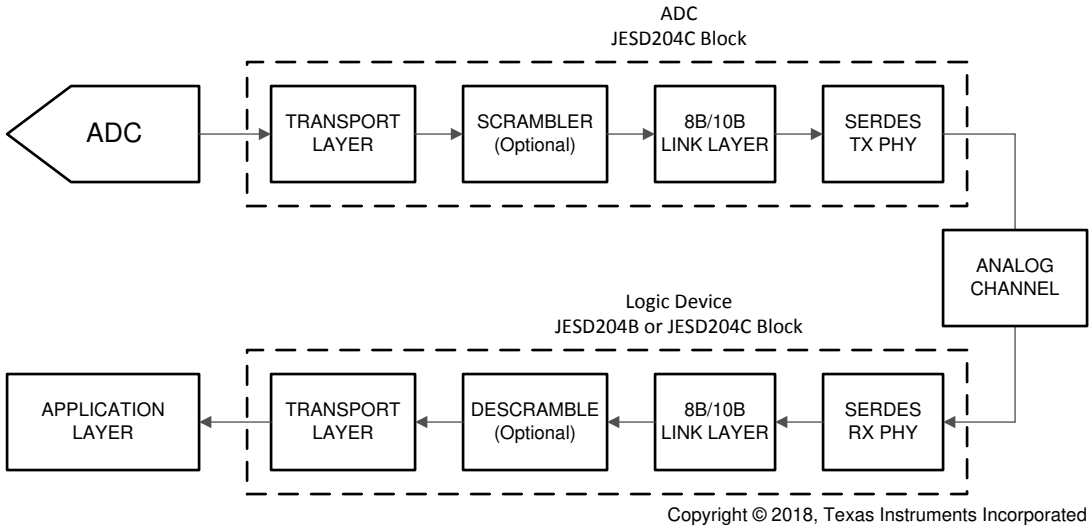

図 6-7. Simplified 8B/10B Encoded JESD204C Interface Diagram

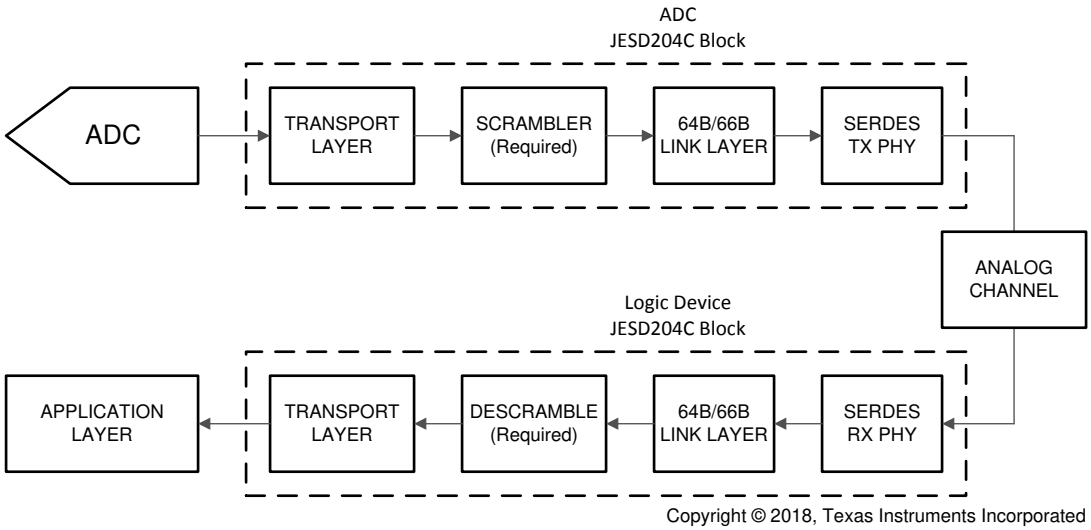

図 6-8. Simplified 64B/66B Encoded JESD204C Interface Diagram

The various signals used in the JESD204C interface and the associated ADC12QJ1600-Q1 pin names are summarized briefly in 表 6-8 for reference. Most of the signals are common between 8B/10B and 64B/66B encoded JESD204C, except for $\overline{\text{SYNC}}$ which is not needed to achieve block synchronization for 64B/66B encoding. The sync header encoded into the data stream is used for block synchronization instead of the $\overline{\text{SYNC}}$ signal.

表 6-8. Summary of JESD204C Signals

SIGNAL NAME	PIN NAMES	8B/10B	64B/66B	DESCRIPTION
Data	Quad/dual channel: D[7:0]+, D[7:0]– Single channel: D[3:0]+, D[3:0]–	Yes	Yes	High-speed serialized data after 8B/10B or 64B/66B encoding
$\overline{\text{SYNC}}$	$\overline{\text{SYNCSE}}$	Yes	No	Link initialization signal (handshake), toggles low to start code group synchronization (CGS) process. Not used for 64B/66B encoding modes, unless it is used for NCO synchronization purposes.
Device clock	CLK+, CLK– or SE_CLK	Yes	Yes	ADC sampling clock or PLL reference clock, also used for clocking digital logic and output serializers
SYSREF	SYSREF+, SYSREF–	Yes	Yes	System timing reference used to deterministically reset the internal local multiframe clock (LMFC) or local extended multiblock clock (LEMC) counters in each JESD204C device

Not all optional features of JESD204C are supported by ADC12QJ1600-Q1. The list of features that are supported and the features that are not supported is provided in 表 6-9.

表 6-9. Declaration of Supported JESD204C Features

LETTER IDENTIFIER	REFERENCE CLAUSE	FEATURE	SUPPORT IN ADC12QJ1600-Q1
a	clause 8	8B/10B link layer	Supported

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表 6-9. Declaration of Supported JESD204C Features (続き)

LETTER IDENTIFIER	REFERENCE CLAUSE	FEATURE	SUPPORT IN ADC12QJ1600-Q1
b	clause 7	64B/66B link layer	Supported
c	clause 7	64B/80B link layer	Not supported
d	clause 7	The command channel when using the 64B/66B or 64B/80B link layer	Not supported
e	clause 7	Forward error correction (FEC) when using the 64B/66B or 64B/80B link layer	Supported
f	clause 7	CRC3 when using the 64B/66B or 64B/80B link layer	Not supported
g	clause 8	A physical $\overline{\text{SYNC}}$ pin when using the 8B/10B link layer	Supported
h	clause 7, clause 8	Subclass 0	Not supported, but subclass 1 transmitter is compatible with subclass 0 receiver
i	clause 7, clause 8	Subclass 1	Supported
j	clause 8	Subclass 2	Not supported
k	clause 7, clause 8	Lane alignment within a single link	Supported
l	clause 7, clause 8	Subclass 1 with support for a lane alignment on a multipoint link by means of the MULTIREF signal	Not supported
m	clause 8	$\overline{\text{SYNC}}$ interface timing is compatible with JESD204A	Supported
n	clause 8	$\overline{\text{SYNC}}$ interface timing is compatible with JESD204B	Supported

6.3.6.1 Transport Layer

The transport layer takes samples from the ADC output and maps the samples into octets inside of frames. These frames are then mapped onto the available lanes. The mapping of octets into frames and frames onto lanes is defined by the transport layer settings such as L, M, F, S, N and N'. An octet is 8 bits (before 8B/10B or 64B/66B encoding), a frame consists of F octets and the frames are mapped onto L lanes. Samples are N bits, but sent as N' bits across the link. The samples come from M converters and there are S samples per converter per frame cycle. M is sometimes artificially increased in order to obtain a more desirable mapping, for instance lower latency may be achieved with a larger M value for long frames.

There are a number of predefined transport layer modes in the device that are defined in 表 6-16, 表 6-17 and 表 6-18. The high level configuration parameters for the transport layer in the device are described in 表 6-14. The transport layer mode is chosen by simply setting the JMODE register setting. For reference, the various configuration parameters for JESD204C are defined in 表 6-15.

The link layer further maps the frames into multiframes when using 8B/10B encoding or blocks, multiblocks and extended multiblocks when using 64B/66B encoding.

6.3.6.2 Scrambler

A data scrambler is available to scramble the data before transmission across the channel. Scrambling is used to remove the possibility of spectral peaks in the transmitted data due to repetitive data streams. The scrambler is optional for 8B/10B encoded modes, however it is mandatory for 64B/66B encoded modes in order to have sufficient spectral content for clock recovery and adaptive equalization. The scrambler operates on the data before encoding, such that the 8B/10B scrambler scrambles the 8-bit octets before 10-bit encoding and the 64B/66B scrambler scrambles the 64-bit block before the sync header insertion (66-bit encoding). The JESD204C receiver automatically synchronizes its descrambler to the incoming scrambled data stream. For 8B/10B encoding, the initial lane alignment sequence (ILA) is never scrambled. Scrambling can be enabled by setting SCR for 8B/10B encoding modes, but it is automatically enabled in 64B/66B modes. The scrambling

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polynomial is different for 8B/10B encoding and 64B/66B encoding schemes as defined by the JESD204C standard.

6.3.6.3 Link Layer

The link layer serves multiple purposes in JESD204C for both 8B/10B and 64B/66B encoding schemes, however there are some differences in implementation for each encoding scheme. In general, the link layer responsibilities include scrambling of the data (see Scrambler), establishing the code (8B/10B) or block (64B/66B) boundaries and the multiframe (8B/10B) or multiblock (64B/66B) boundaries, initializing the link, encoding the data, and monitoring the health of the link. This section is split into an 8B/10B section (8B/10B Link Layer) and a 64B/66B section (64B/66B Link Layer) in order to cover the specific implementation for each encoding scheme.

6.3.6.4 8B/10B Link Layer

This section covers the link layer for the 8B/10B encoding operating modes including initialization of the character, frame and multiframe boundaries, alignment of the lanes, 8B/10B encoding and monitoring of the frame and multiframe alignment during operation.

6.3.6.4.1 Data Encoding (8B/10B)

The data link layer converts the 8-bit octets from the transport layer into 10-bit characters for transmission across the link using 8B/10B encoding. 8B/10B encoding ensures DC balance to allow use of AC-coupling between the SerDes transmitter and receiver and specify a sufficient number of edge transitions for the receiver to reliably recover the data clock. 8B/10B encoding also provides some error detection since a single bit error in a character likely results in either not being able to find the 10-bit character in the 8B/10B decoder lookup table or an incorrect character disparity.

6.3.6.4.2 Multiframes and the Local Multiframe Clock (LMFC)

The frames from the transport layer are combined into multiframes which are used in the process of achieving deterministic latency in subclass 1 implementations. The length of a multiframe is set by the K parameter which defines the number of frames in a multiframe. JESD204C increases the maximum allowed number of frames per multiframe (K) from 32 in JESD204B to 256 in JESD204C to allow a longer multiframe to ease deterministic latency requirements. The total allowed range of K is defined by the inequality ceil(17/F) ≤ K ≤ min(256, floor(1024/F)) where ceil() and floor() are the ceiling and floor function, respectively. The local multiframe clock (LMFC) keeps track of the start and end of a multiframe for deterministic latency and data synchronization purposes. The LMFC is reset by the SYSREF signal to a deterministic phase in both the transmitter and receiver in order to act as a timing reference for deterministic latency. The LMFC clock frequency is given in Equation 8 where f_{BIT} is the serialized bit rate (line rate) of the SerDes interface and F and K are as defined above. The frequency of SYSREF must equal to or an integer division of f_{LMFC} when using 8B/10B encoding modes if SYSREF is a continuous signal.

$$f_{LMFC} = f_{BIT} / (10 \times F \times K) \quad (8)$$

6.3.6.4.3 Code Group Synchronization (CGS)

The first step in initializing the JESD204C link, after the LMFC is deterministically reset by SYSREF, is for the receiver to find the boundaries of the encoded 10-bit characters sent across each SerDes lane. This process is called code group synchronization (CGS). The receiver first asserts the $\overline{\text{SYNC}}$ signal (set to logic '0') when ready to initialize the link. The transmitter responds to the request by sending a stream of K28.5 comma characters. The receiver aligns its character clock to the K28.5 character sequence and CGS is achieved after successfully receiving four consecutive K28.5 characters. The receiver deasserts $\overline{\text{SYNC}}$ (set to logic '1') on the next LMFC edge after CGS is achieved and waits for the transmitter to start the initial lane alignment sequence (ILAS).

6.3.6.4.4 Initial Lane Alignment Sequence (ILAS)

After the transmitter detects the $\overline{\text{SYNC}}$ signal deassert (logic '0' to logic '1' transition), the transmitter waits until its next LMFC edge to start sending the initial lane alignment sequence (ILAS). The ILAS consists of four multiframes each containing a predetermined sequence. The receiver searches for the start of the ILAS to

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determine the frame and multiframe boundaries. Each multiframe of the ILAS starts with a /R/ character (K28.0) and ends with a /A/ character (K28.3) and either can be used to detect the boundary of a multiframe. Each lane starts buffering its data in the elastic buffer once the ILAS reaches the receiver, starting with the /R/ character, until all receivers have received the ILAS and subsequently release the ILAS from all lanes at the same time in order to align the lanes. The elastic buffer release point is chosen to avoid ambiguity in the release of the data caused by variation in the data delay (arrival of the ILAS at the receiver for each lane). The second multiframe of the ILAS contains configuration parameters for the JESD204C link configuration that can be used by the receiver to verify that the transmitter and receiver configurations match.

6.3.6.4.5 Frame and Multiframe Monitoring

The device supports frame and multiframe monitoring for verifying the health of the JESD204C link when using 8B/10B encoding. The scheme changes depending on the use of scrambling. The implementation when scrambling is disabled is covered first. If the last octet of the current frame matches the last octet of the previous frame, then the last octet of the current frame is encoded as an /F/ (K28.7) character. If the current frame is also the last frame of a multiframe, then an /A/ (K28.3) character is used instead. Neither an /F/ or /A/ character should occur in a normal data stream, except when replaced by the transmitter for alignment monitoring. When the receiver detects an /F/ or /A/ character in the normal data stream the receiver checks to see if the character occurs at the location expected to be the end of a frame or multiframe. If the character occurs at a location other than the end of a frame or multiframe then either the transmitter or receiver has become misaligned. The receiver replaces the alignment character with the appropriate data character upon reception of a properly aligned /F/ or /A/ character. The appropriate data character is the last octet of the previously received frame. This scheme increases the probability of an alignment character for non-scrambled data streams.

The implementation when scrambling is enabled is slightly different since the octets are randomized. If the last octet of a frame is 0xFC (before 8B/10B encoding) then the transmitter encodes the octet as an /F/ (/K28.7/) character. If the last octet of a multiframe is 0x7C (before 8B/10B encoding) then the transmitter encodes the octet as an /A/ (/K28.3/) character. The location of the /A/ and /F/ characters is monitored to verify proper frame and multiframe alignment. The receiver replaces the alignment characters by simply replacing an /F/ character with the 0xFC octet and an /A/ character with the 0x7C octet.

The receiver can report an error if multiple alignment characters occur in the incorrect location or do not occur when expected. Upon detection of a frame or multiframe misalignment, the receiver should trigger a link realignment by asserting $\overline{\text{SYNC}}$. SYSREF should also be reissued to verify that the LMFC in the transmitter and receiver have proper alignment before restarting the link.

6.3.6.5 64B/66B Link Layer

This section covers the link layer for the 64B/66B encoding operating modes which includes scrambling of the data, addition of the sync headers (64B/66B encoding), the structure of the block and multiblock, the sync header, cyclic redundancy checking (CRC), forward error correction (FEC) and link alignment.

6.3.6.5.1 64B/66B Encoding

The frames formed by the transport layer are packed into 8-octet long blocks (64 bits). This 64-bit block is scrambled and then a 2-bit sync header (SH) is appended to form a 66-bit transmission block. The sync header is used for block synchronization by marking the end of a block as well as allowing for cyclic redundancy checking (CRC), forward error correction (FEC) or a command channel. The structure of a block is given in 表 6-10 where SH represents the appended 2-bit sync header.

表 6-10. Structure of 64B/66B Block with Sync Header

SH	OCTET0	OCTET1	OCTET2	OCTET3	OCTET4	OCTET5	OCTET6	OCTET7
[0:1]	[2:9]	[10:17]	[18:25]	[26:33]	[34:41]	[42:49]	[50:57]	[58:65]

6.3.6.5.2 Multiblocks, Extended Multiblocks and the Local Extended Multiblock Clock (LEMC)

A multiblock is a 32 block container which consists of a concatenation of 32 blocks. An extended multiblock is a concatenation of multiple multiblocks, where E defines the number of multiblocks in an extended multiblock. A

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frame can be split between blocks and multiblocks, but there must be an integer number of frames in an extended multiblock. An extended multiblock is only necessary when a multiblock does not have an integer number of frames. If an extended multiblock is not used, because a multiblock contains an integer number of frames, then the E parameter is equal to 1 to indicate that there is one multiblock in an extended multiblock.

An extended multiblock is analogous to a multiframe in the 8B/10B transport layer. The local extended mutiblock clock (LEMC) keeps track of the start and end of a multiblock for deterministic latency and data synchronization purposes in the same way the LMFC tracks the start and end of a multiframe in 8B/10B encoding. The LEMC is reset by the SYSREF signal to a deterministic phase in both the transmitter and receiver in order to act as a timing reference for deterministic latency. The LEMC clock frequency is defined by Equation 9 where f_{BIT} is the serialized bit rate (line rate) of the SerDes interface. The frequency of SYSREF must equal to or an integer division of f_{LMFC} when using 64B/66B encoding modes if SYSREF is a continuous signal.

$$f_{LEMC} = f_{BIT} / (66 \times 32 \times E) \quad (9)$$

6.3.6.5.2.1 Block, Multiblock and Extended Multiblock Alignment using Sync Header

The sync header contains two bits that are always opposite of each other (either 01 or 10). The JESD204C receiver can find the block boundaries by looking for a 66-bit boundary that always contains a 0 to 1 or 1 to 0 transition. Although 0 to 1 and 1 to 0 transitions occur at other locations in a block, it is impossible for the sequence to appear at a fixed location, other than the proper sync header location, in successive blocks for a long period of time. The sync header indicates the start of a block and can be used for block alignment monitoring. If a 00 or a 11 bit sequence is seen at the assumed sync header location of a block, then block alignment may have been lost. Multiple occurrences of incorrect sync header bits should trigger a search for the sync header after sending SYSREF to all devices to reset LEMC alignment.

A sync header ([0:1]) of 01 corresponds to transmission of a 1 while a sync header of 10 corresponds to a transmission of a 0. The transmitted bit from the sync header of each block of a multiblock are combined into a 32-bit word called the sync header stream. The sync header stream is used to transmit data in parallel with the user data in order to synchronize the link by marking the borders of multiblocks and extended multiblocks. In addition, the sync header stream provides one of either CRC, FEC or a command channel. ADC12QJ1600-Q1 supports CRC-12 and FEC and does not support CRC-3 or the command channel.

The 32-bit sync header stream always ends with a 00001 bit sequence, called the end-of-multiblock (EoMB) signal, that indicates the end of a multiblock. For CRC and command channel modes, a 00001 sequence never occur in any other location in the sync header stream. For FEC mode, it is possible for a 00001 sequence to appear in another location within the sync header stream, however it is improbable to see the 00001 sequence in the same location within a sequence of multiple multiblocks. Therefore, in FEC mode it may take more than one multiblock to find the end of a multiblock. The end of an extended multiblock is found for all modes by monitoring bit 22 of the sync header stream, the EoEMB bit, which indicates the end of an extended multiblock when set to a 1. The EoMB (00001) and EoEMB signals, as well as fixed 1s in the sync header stream for CRC and command channel modes, form the pilot signal of the sync header stream.

The defined format for each form of the sync header stream are defined in the following sections.

6.3.6.5.2.1.1 Cyclic Redundancy Check (CRC) Mode

The cyclic redundancy check (CRC) mode is available to allow detection of potential bit errors during transmission. Support for the 12-bit word CRC-12 mode is required by JESD204C, while a 3-bit word CRC-3 mode is optional. The device does not support the CRC-3 mode and therefore this section is specific to the CRC-12 mode only. The transmitter computes the CRC-12 parity bits from the scrambled data bits of the 32 blocks of a multiblock. The 12-bit CRC parity word is then transmitted in the sync header stream of the next multiblock. The receiver computes the 12-bit parity word of the received multiblock and compares it against the received 12-bit parity word of the next multiblock. A difference indicates that there is at least one error in the received data bits or in the received 12-bit parity word. The minimum latency to the detection of a bit error in the first data bit of a multiblock is 46 blocks. Enable CRC-12 mode by setting SHMODE to 0.

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The mapping of the sync header stream when using the CRC-12 mode is shown in 表 6-11. CRC[x] corresponds to bit x of the 12-bit CRC word. Cmd[x] corresponds to bit x of the 7 bit command word, which are always set to 0s in the device. The 00001 bit sequence at the end of the sync header stream is the pilot signal that is used to identify the end of a multiblock. The 1s that occur throughout the sync header ensure that the pilot signal can only be seen at the end of the sync header, allowing multiblock alignment after only a single multiblock has been received. EoEMB is the end-of-extended-multiblock bit, which is set to 1 for the last multiblock of an extended multiblock.

表 6-11. Sync Header Stream Bit Mapping for CRC-12 Mode

Bit	Function	Bit	Function	Bit	Function	Bit	Function
0	CRC[11]	8	CRC[5]	16	Cmd[6]	24	Cmd[2]
1	CRC[10]	9	CRC[4]	17	Cmd[5]	25	Cmd[1]
2	CRC[9]	10	CRC[3]	18	Cmd[4]	26	Cmd[0]
3	1	11	1	19	1	27	0
4	CRC[8]	12	CRC[2]	20	Cmd[3]	28	0
5	CRC[7]	13	CRC[1]	21	1	29	0
6	CRC[6]	14	CRC[0]	22	EoEMB	30	0
7	1	15	1	23	1	31	1

The CRC-12 encoder takes in a multiblock of 32 scrambled blocks (2048 bits) and computes the 12-bit parity word using the generator polynomial given by Equation 10. The polynomial is sufficient to detect all 2-bit errors in a multiblock, spanning any distance, and burst error sequences of up to 12-bits in length. The probability of not detecting a 3-bit error spanning any distance in a multiblock is approximately 0.004%.

$$0x987 == x^{12}+x^{9}+x^{8}+x^{3}+x^{2}+x+1 \quad (10)$$

The full parity bit generation for CRC-12 is shown in 図 6-9. The input is a 2048 bit sequence, built from the 32 scrambled blocks of a multiblock (sync header is not included). The 12-bit parity word, CRC[11:0], is taken from the S_x blocks after the full 2048 bit sequence is processed. The S_x blocks are initialized with 0s before processing each multiblock. For more information on the CRC-12 parity word generation, refer to the JESD204C standard.

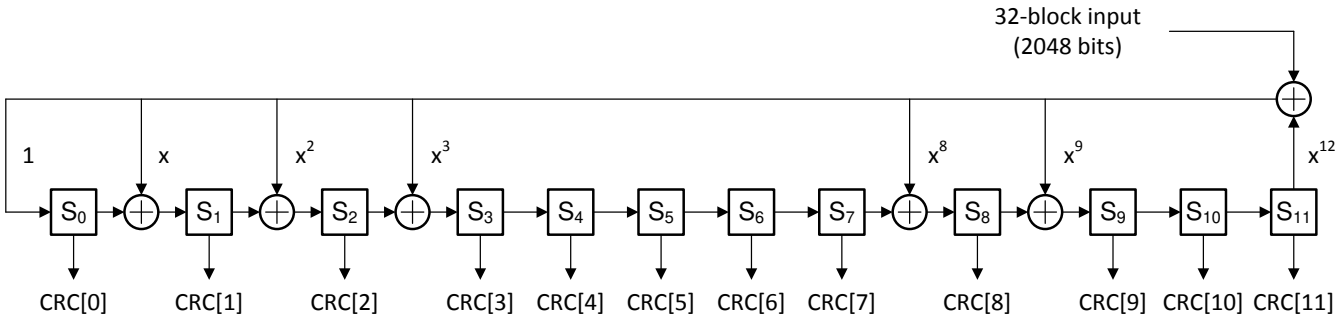

図 6-9. CRC-12 Parity Bit Generator

6.3.6.5.2.1.2 Forward Error Correction (FEC) Mode

Forward error correction (FEC) is an optional feature in JESD204C and is supported by ADC12QJ1600-Q1. Whereas CRC-12 mode can only detect errors on the link, FEC is able to detect and correct errors in order to improve the bit error rate (BER) for error-sensitive applications. Many applications can tolerate random bit errors, however some applications, such as an oscilloscope, rely on long error-free measurements in order to detect a certain response from the device under test (DUT). An error in these applications may result in a false-positive detection of the response. Enable FEC mode by setting SHMODE to 2.

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A scrambled multiblock of 32 blocks (2048 bits) is input into the FEC parity bit generator to generate the 26-bit parity word. The parity word is sent in the sync header stream of the next multiblock. The receiver then calculates its own 26-bit parity word and calculates the difference between the locally generated and received parity word, called the syndrome of the received bits. If the syndrome is 0, then all bits are assumed to have been received correctly, while any value other than 0 indicates at least one error in either the data bits or the parity word. If the syndrome is non-zero, then it can be used to determine the most likely error and then correct the error. The minimum latency from a bit error to detection and correct of a bit error in the first bit of a multiblock is 58 blocks.

The mapping of the sync header stream when using FEC mode is shown in 表 6-12. FEC[x] corresponds to bit x of the 26-bit FEC word. The 00001 bit sequence at the end of the sync header stream is the pilot signal that is used to identify the end of a multiblock. It is possible for a 00001 sequence to appear in another location within the sync header stream in FEC mode, however it is improbable to see the 00001 sequence in the same location within a sequence of multiple multiblocks. Therefore, in FEC mode it may take more than one multiblock to find the end of a multiblock. EoEMB is the end-of-extended-multiblock bit, which is set to 1 for the last multiblock of an extended multiblock.

表 6-12. Sync Header Stream Bit Mapping for FEC Mode

Bit	Function	Bit	Function	Bit	Function	Bit	Function
0	FEC[25]	8	FEC[17]	16	FEC[9]	24	FEC[2]
1	FEC[24]	9	FEC[16]	17	FEC[8]	25	FEC[1]
2	FEC[23]	10	FEC[15]	18	FEC[7]	26	FEC[0]
3	FEC[22]	11	FEC[14]	19	FEC[6]	27	0
4	FEC[21]	12	FEC[13]	20	FEC[5]	28	0
5	FEC[20]	13	FEC[12]	21	FEC[4]	29	0
6	FEC[19]	14	FEC[11]	22	EoEMB	30	0
7	FEC[18]	15	FEC[10]	23	FEC[3]	31	1

The FEC encoder takes in a multiblock of 32 scrambled blocks (2048 bits) and computes the 26-bit parity word using the generator polynomial given by Equation 11. The 2048 scrambled input bits plus 26 parity bits forms a shortened (2074, 2048) binary cyclic code. The (2074, 2048) binary cyclic code is shortened from the cyclic Fire code (8687, 8661). This polynomial can correct up to a 9-bit burst error per multiblock.

$$g(x) = (x^{17}+1)(x^9+x^4+1) == x^{26}+x^{21}+x^{17}+x^9+x^4+1 \quad (11)$$

The full 26-bit FEC parity word generation is shown in 図 6-10. The input is a 2048 bit sequence, built from the 32 scrambled blocks of a multiblock (sync header is not included). The 26-bit parity word, FEC[25:0], is taken from the S_x blocks after the full 2048 bit sequence is processed. The S_x blocks are initialized with 0s before processing each multiblock. For more information on the FEC parity word generation, refer to the JESD204C standard.

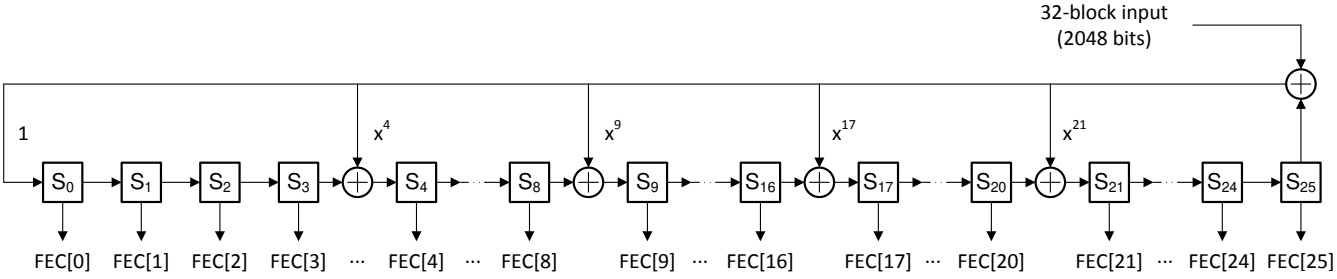

図 6-10. FEC Parity Bit Generator

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FEC decoding and error correction are not covered here. For full details on FEC decoding and error correction, refer to the JESD204C standard.

6.3.6.5.3 Initial Lane Alignment

The 64B/66B link layer does not use an initial lane alignment sequence (ILAS) like the 8B/10B link layer. Therefore, the receiver must use a different scheme to align lanes using the elastic buffer. In 8B/10B mode, the ILAS triggers the elastic buffer to start buffering the data for each lane. After all lanes have started buffering the data, the elastic buffers for each lane are released at a release point determined by the release buffer delay (RBD) parameter and the phase of the LMFC. In 64B/66B mode, the process starts by having all lanes achieve block, multiblock and extended multiblock alignment. Once all lanes have achieved alignment, the receiver can begin buffering data in the elastic buffers at the start of the next extended multiblock on each lane. The data is released at the next release point after all lanes have seen the start of an extended multiblock and have started buffering the data. The release point is defined relative to the LEMC edge and the programmed RBD value, the most intuitive of which is to release on the LEMC edge itself. The release point must be chosen to avoid the region of the LEMC containing variation in the data delay on each lane from startup to startup.

6.3.6.5.4 Block, Multiblock and Extended Multiblock Alignment Monitoring

Synchronization of blocks, multiblocks and extended multiblocks by monitoring the sync header of each block and EoMB and EoEMB bit of the sync header stream. A block always begins with a 0 to 1 or 1 to 0 transition (sync header). A single missed sync header can occur due to a bit error, however if there are a number of sync header errors within a set number of blocks, then block synchronization has been lost and block synchronization should be reinitialized. It is possible to still have block synchronization, but to lose multiblock or extended multiblock synchronization. Multiblock synchronization is monitored by looking for the EoMB signal, 00001, at the end of the sync header stream for each multiblock. If multiple EoMB signals are erroneous within a number of blocks, multiblock synchronization has been lost and multiblock synchronization should be reinitialized. If an erroneous EoEMB bit is received for multiple extended multiblocks within a number of extended multiblocks, such as a 1 for a multiblock that is not the end of an extended multiblock or a 0 for a multiblock that is the end of an extended multiblock, then multiblock synchronization is lost and extended multiblock synchronization should be reinitialized. If multiblock or extended multiblock synchronizaton is lost, SYSREF should be applied to the erroneous devices in order to reestablish the LEMC before the synchronization process begins.

6.3.6.6 Physical Layer

The JESD204C physical layer consists of a current mode logic (CML) output driver and receiver. The receiver consists of a clock detection and recovery (CDR) unit to extract the data clock from the serialized data stream and can contain a continuous time linear equalizer (CTLE) and/or discrete feedback equalizer (DFE) to correct for the low-pass response of the physical transmission channel. Likewise, the transmitter can contain pre-equalization to account for frequency dependent losses across the channel. The total reach of the SerDes links depends on the data rate, board material, connectors, equalization, noise and jitter, and required bit-error performance. The SerDes lanes do not have to be matched in length because the receiver aligns the lanes during the initial lane alignment sequence.

6.3.6.6.1 SerDes Pre-Emphasis

The ADC12QJ1600-Q1 high-speed output drivers can pre-equalize the transmitted data stream by using pre-emphasis in order to compensate for the low-pass response of the transmission channel. Configurable pre-emphasis settings allow the output drive waveform to be optimized for different PCB materials and signal transmission distances. The pre-emphasis setting is adjusted through the serializer pre-emphasis setting SER_PE. Higher values increase the pre-emphasis to compensate for more lossy PCB materials. This adjustment is best used in conjunction with an eye-diagram analysis capability in the receiver. Adjust the pre-emphasis setting to optimize the eye-opening for the specific hardware configuration and line rates needed.

6.3.6.7 JESD204C Enable

The JESD204C interface must be disabled through JESD_EN while any of the other JESD204C parameters are being changed. When JESD_EN is set to 0 the block is held in reset and the serializers are powered down. The

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clocks for this section are also gated off to further save power. When the parameters are set as desired, the JESD204C block can be enabled (JESD_EN is set to 1).

6.3.6.8 Multi-Device Synchronization and Deterministic Latency

JESD204C subclass 1 outlines a method to achieve deterministic latency across the serial link. If two devices achieve the same deterministic latency then they can be considered synchronized. This latency must be achieved from system startup to startup to be deterministic. There are two key requirements to achieve deterministic latency. The first is proper capture of SYSREF for which the device provides a number of features to simplify this requirement at giga-sample clock rates (see the *SYSREF Capture* section for more information). SYSREF resets either the LMFC in 8B/10B encoding mode or the LEMC is 64B/66B encoding mode. The LMFC and LEMC are analogous between the two modes and is now referred to as LMFC/LEMC.

The second requirement is to choose a proper elastic buffer release point in the receiver. Because the device is an ADC, the device is the transmitter (TX) in the JESD204C link and the logic device is the receiver (RX). The elastic buffer is the key block for achieving deterministic latency, and does so by absorbing variations in the propagation delays of the serialized data as the data travels from the transmitter to the receiver. A proper release point is one that provides sufficient margin against delay variations. An incorrect release point results in a latency variation of one LMFC/LEMC period. Choosing a proper release point requires knowing the average arrival time of data at the elastic buffer, referenced to an LMFC/LEMC edge, and the total expected delay variation for all devices. With this information the region of invalid release points within the LMFC/LEMC period can be defined, which stretches from the minimum to maximum delay for all lanes. Essentially, the designer must ensure that the data for all lanes arrives at all devices after the previous release point occurs and before the next release point occurs.

図 6-11 provides a timing diagram that demonstrates this requirement. In this figure, the data for two ADCs is shown. The second ADC has a longer routing distance (t_{PCB}) and results in a longer link delay. First, the invalid region of the LMFC/LEMC period is marked off as determined by the data arrival times for all devices. Then, the release point is set by using the release buffer delay (RBD) parameter to shift the release point an appropriate number of frame clocks from the LMFC/LEMC edge so that the release point occurs within the valid region of the LMFC/LEMC cycle. In the case of 図 6-11, the LMFC/LEMC edge (RBD = 0) is a good choice for the release point because there is sufficient margin on each side of the valid region.

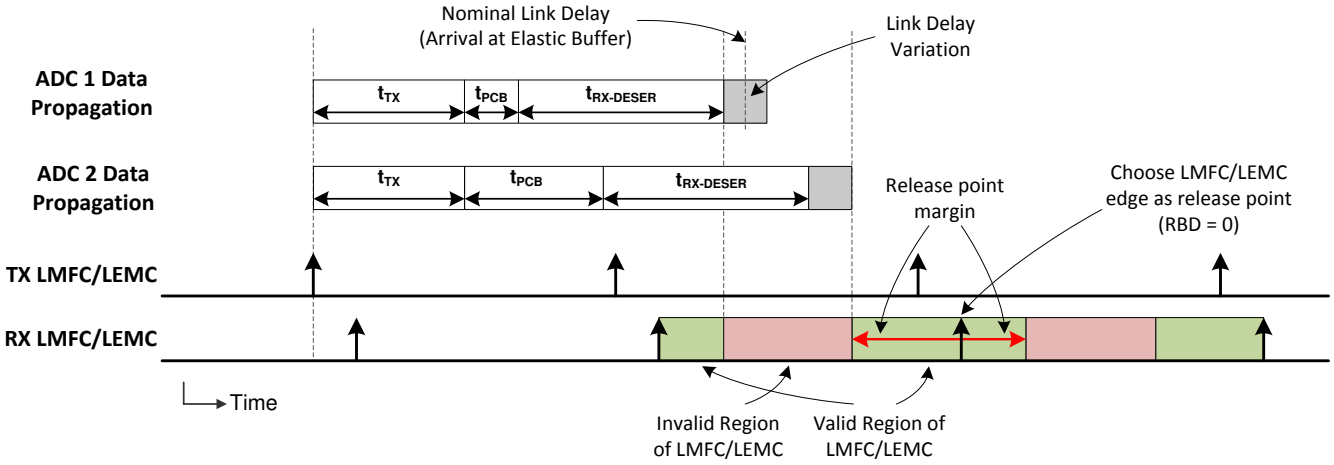

図 6-11. LMFC/LEMC Valid Region Definition for Elastic Buffer Release Point Selection

The TX and RX LMFC/LEMCs do not necessarily need to be phase aligned, but knowledge of their phase is important for proper elastic buffer release point selection. Also, the elastic buffer release point occurs within every LMFC/LEMC cycle, but the buffers only release when all lanes have arrived. Therefore, the total link delay can exceed a single LMFC/LEMC period; see *JESD204B multi-device synchronization: Breaking down the requirements* for more information.

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6.3.6.9 Operation in Subclass 0 Systems

The device can operate with subclass 0 compatibility provided that multi-ADC synchronization and deterministic latency are not required. With these limitations, the device can operate without the application of SYSREF. The internal LMFC/LEMC is automatically self-generated with unknown timing. SYNC is used as normal to initiate the CGS and ILAS in 8B/10B mode.

6.3.6.10 Alarm Monitoring

A number of built-in alarms are available to monitor internal events. Several types of alarms and upsets are detected by this feature:

1. C-PLL is not locked
2. S-PLL is not locked
3. JESD204C link is not transmitting data (not in the data transmission state)
4. SYSREF causes internal clocks to be realigned
5. An upset that impacts the internal clocks
6. A read or write error generated by the digital to serializer synchronizing FIFO

When an alarm occurs, a bit for each specific alarm is set in ALM_STATUS. Each alarm bit remains set until the host system writes a 1 to clear the alarm. If the alarm type is not masked (see the ALM_MASK register), then the alarm is also indicated by the ALARM register. The CALSTAT output pin can be configured as an alarm output that goes high when an alarm occurs; see CAL_STATUS_SEL.

6.3.6.10.1 Clock Upset Detection

The CLK_ALM register bit indicates if the internal clocks have been upset. The clocks in channel A are continuously compared to channel B. If the clocks differ for even one DEVCLK / 2 cycle, the CLK_ALM register bit is set and remains set until cleared by the host system by writing a 1. For the CLK_ALM register bit to function properly, follow these steps:

1. Program JESD_EN = 0
2. Ensure the part is configured to use both channels (PD_ACH = 0, PD_BCH = 0)
3. Program JESD_EN = 1
4. Write CLK_ALM = 1 to clear CLK_ALM
5. Monitor the CLK_ALM status bit or the CALSTAT output pin if CAL_STATUS_SEL is properly configured
6. When exiting global power-down (via MODE or the PD pin), the CLK_ALM status bit may be set and must be cleared by writing a 1 to CLK_ALM

6.3.6.10.2 FIFO Upset Detection

The FIFO_LANE_ALM register bits indicate if an error has occurred in the synchronizing FIFO between the digital logic block and serializer outputs. If the FIFO pointers are upset due to an undesired clock shift or other single event or incorrect clocking frequencies the FIFO_LANE_ALM bit for the erroneous lane is set to 1. Toggling JESD_EN to 0 and then 1 resets the FIFO logic.

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6.4 Device Functional Modes

The device can be configured to operate in a number of functional modes. These modes are described in this section.

6.4.1 Low Power Mode and High Performance Mode

Device power consumption can be reduced at the tradeoff of performance by programming the device into the Low Power Mode. This mode is only available when operating at 1 GSPS or less and is recommended to only be used for 1st Nyquist zone applications. The default operating mode is High Performance Mode which is enabled by the default register values. 表 6-13 shows the register writes to switch between the lowest power configuration of Low Power Mode and High Performance Mode. These writes should only be performed when CAL_EN is set to 0 and JESD_EN is set to 0.

表 6-13. Low Power Mode Register Writes

Register Name (Address)	Low Power Mode Value	High Performance Mode Value (Default Mode)
LOW_POWER1 (0x037)	0x46	0x4B
LOW_POWER2 (0x29A)	0x06	0x0F
LOW_POWER3 (0x29B)	0x00	0x04
LOW_POWER4 (0x29C)	0x14	0x1B

The magnitude of the glitch during the transition between ADC cores during background calibration and low power background calibration is affected by the setting of the LOW_POWER3 register setting (Address = 0x29B). A lower power can be traded off vs larger glitch magnitude. The ADC output during the transition between ADC cores for low power mode is shown in 図 6-12 and the power dissipation change vs LOW_POWER3 setting is shown in 図 6-13. A setting of 4 reduces the glitch to the same magnitude as high performance mode.

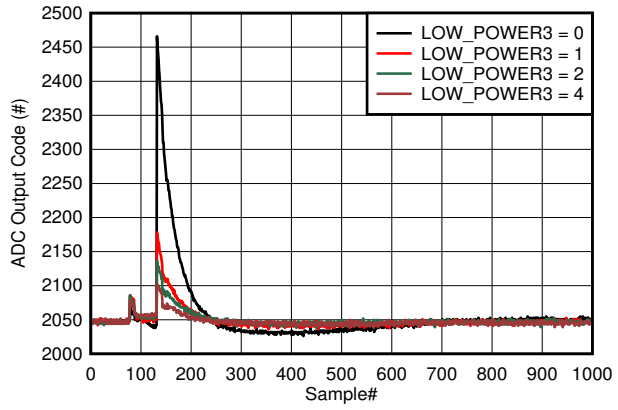

図 6-12. Background Calibration Core Transition In Low Power Mode

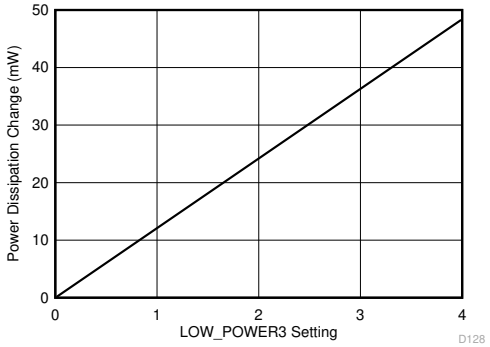

図 6-13. Power Dissipation Change vs LOW_POWER3 register setting

In low power background calibration mode, the timing of the ADC transition can be controlled by setting register LP_TRIG = 1. The ADC transition will occur in the ADC output data between 500 and 1000 ADC sample clocks after triggering by the CALTRIG ball or SPI write to CAL_SOFT_TRIG register (Address = 0x6C).

Foreground calibration mode has no ADC core transitions and no glitch.

6.4.2 JESD204C Modes

The device can be programmed for a number JESD204C output formats. 表 6-14 summarizes the basic operating mode configuration parameters and whether they are user configured or derived.

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表 6-14. ADC12QJ1600-Q1 Operating Mode Configuration Parameters

PARAMETER	DESCRIPTION	USER CONFIGURED OR DERIVED	VALUE
JMODE	JESD204C operating mode, automatically derives the rest of the JESD204C parameters	User configured	Set by JMODE
R	Number of bits transmitted per lane per ADC core sampling clock cycle. The JESD204C line rate is the sampling clock frequency (f_S) times R. This parameter sets the SerDes PLL multiplication factor.	Derived	See 表 6-16, 表 6-17 and 表 6-18
K	Number of frames per multiframe (8B/10B mode)	User configured	Set by KM1, see the allowed values in 表 6-16, 表 6-17 and 表 6-18. This parameter is ignored in 64B/66B modes.
E	Number of multiblocks per extended multiblock (64B/66B mode)	Derived	Always set to '1' in ADC12QJ1600-Q1. This parameter is ignored in 8B/10B modes.

There are a number of parameters required to define the JESD204C transport layer format, all of which are sent across the link during the initial lane alignment sequence in 8B/10B mode. 64B/66B mode does not use the ILAS, however the transport layer uses the same parameters. In the device, most parameters are automatically derived based on the selected JMODE; however, a few are configured by the user. 表 6-15 describes these parameters.

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表 6-15. JESD204C Initial Lane Alignment Sequence Parameters

PARAMETER	DESCRIPTION	USER CONFIGURED OR DERIVED	VALUE
ADJCNT	LMFC adjustment amount (not applicable)	Derived	Always 0
ADJDIR	LMFC adjustment direction (not applicable)	Derived	Always 0
BID	Bank ID	Derived	Always 0
CF	Number of control words per frame	Derived	Always 0
CS	Control bits per sample	Derived	Always set to 0 in ILAS, see 表 6-16, 表 6-17 and 表 6-18 for actual usage
DID	Device identifier, used to identify the link	User configured	Set by DID, see 表 6-19
F	Number of octets (bytes) per frame (per lane)	Derived	See 表 6-16, 表 6-17 and 表 6-18
HD	High-density format (samples split between lanes)	Derived	Always 0
JESDV	JESD204 standard revision	Derived	Always 1
K	Number of frames per multiframe	User configured	Set by the KM1 register
L	Number of serial output lanes per link	Derived	See 表 6-16, 表 6-17 and 表 6-18
LID	Lane identifier for each lane	Derived	See 表 6-19
M	Number of converters used to determine lane bit packing; may not match number of ADC channels in the device	Derived	See 表 6-16, 表 6-17 and 表 6-18
N	Sample resolution (before adding control and tail bits)	Derived	See 表 6-16, 表 6-17 and 表 6-18
N'	Bits per sample after adding control and tail bits	Derived	See 表 6-16, 表 6-17 and 表 6-18
S	Number of samples per converter (M) per frame	Derived	See 表 6-16, 表 6-17 and 表 6-18
SCR	Scrambler enabled	User configured	Set by SCR
SUBCLASSV	Device subclass version	Derived	Always 1
RES1	Reserved field 1	Derived	Always 0
RES2	Reserved field 2	Derived	Always 0
CHKSUM	Checksum for ILAS checking (sum of all above parameters modulo 256)	Derived	Computed based on parameters in this table

Configuring the device is made easy by using a single configuration parameter called JMODE. Using 表 6-16 for the quad channel device, 表 6-17 for the dual channel device or 表 6-18 for the single channel device, the correct JMODE value can be found for the desired operating mode. The modes listed are the only available operating modes. This tables also gives a range and allowable step size for the K parameter (set by KM1), which sets the multiframe length in number of frames.

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表 6-16. Quad Channel Modes (supported by Quad Channel Device)

OPERATING MODE	USER-SPECIFIED PARAMETER		DERIVED PARAMETERS												INPUT CLOCK RANGE (MHz)
	JMODE	K [Min:Step:Max]	Encoding	N	CS	N'	CF	L	M	F	S	HD	E	R (Fbit / Fclk)	
12-Bit, 8B/10B, 8 Lanes	0	4:4:256	8B/10B	12	0	12	0	8	8(1)	8	5	0	—	8	500-1600
12-Bit, 8B/10B, 6 Lanes	1	16:16:256	8B/10B	12	0	12	0	6	4	2	2	1	—	10	500-1600
8-Bit, 8B/10B, 4 Lanes	2	32:32:256	8B/10B	8	0	8	0	4	4	1	1	0	—	10	500-1600
10-Bit, 8B/10B, 4 Lanes	3	32:32:256	8B/10B	10	0	10	0	4	4	5	4	0	—	12.5	500-1372.8
12-Bit, 64B/66B, 3 Lanes	4	128(2)	64B/66B	12	0	12	0	3	4	2	1	1	1	16.5	500-1040
8-Bit, 64B/66B, 2 Lanes	5	128(2)	64B/66B	8	0	8	0	2	4	2	1	0	1	16.5	500-1040
12-Bit, 64B/66B, 6 Lanes	6	128(2)	64B/66B	12	0	12	0	6	4	2	2	1	1	8.25	500-1600
8-Bit, 64B/66B, 4 Lanes	7	256(2)	64B/66B	8	0	8	0	4	4	1	1	0	1	8.25	500-1600
12-Bit, 64B/66B, 4 Lanes	8	256(2)	64B/66B	12	0	12	0	4	4	3	2	0	3	12.375	500-1386.7
8-Bit, 8B/10B, 8 Lanes	9	32:32:256	8B/10B	8	0	8	0	8	4	1	2	0	—	5	500-1600
10-Bit, 8B/10B, 8 Lanes	10	32:32:256	8B/10B	10	0	10	0	8	8(1)	5	4	0	—	6.25	500-1600
12-Bit, 64B/66B, 8 Lanes	14	256(2)	64B/66B	12	0	12	0	8	8(1)	3	2	0	3	6.1875	500-1600

(1) M equals L in these modes to allow the samples to be sent in time-order over L lanes without unnecessary buffering. The M parameter does not represent the actual number of converters. Interleave the M sample streams from each link in the receiver to produce the correct sample data; see mode diagrams for more details.
(2) In the 64B/66B modes, the K parameter is not directly programmable. K is related to E and F according to the equation K = 8 x 32 x E/F. K is not an actual parameter of the 64B/66B link layer.

表 6-17. Dual Channel Modes (supported by Quad and Dual-Channel Devices)

OPERATING MODE	USER-SPECIFIED PARAMETER		DERIVED PARAMETERS												INPUT CLOCK RANGE (MHz)
	JMODE	K [Min:Step:Max]	Encoding	N	CS	N'	CF	L	M	F	S	HD	E	R (Fbit / Fclk)	
12-Bit, 8B/10B, 4 Lanes	0	4:4:256	8B/10B	12	0	12	0	4	4(1)	8	5	0	—	8	500-1600
12-Bit, 8B/10B, 3 Lanes	1	16:16:256	8B/10B	12	0	12	0	3	2	2	2	1	—	10	500-1600
8-Bit, 8B/10B, 2 Lanes	2	32:32:256	8B/10B	8	0	8	0	2	2	1	1	0	—	10	500-1600
10-Bit, 8B/10B, 2 Lanes	3	32:32:256	8B/10B	10	0	10	0	2	2	5	4	0	—	12.5	500-1372.8
12-Bit, 64B/66B, 2 Lanes	4	128(2)	64B/66B	12	0	12	0	2	2	2	1	1	1	16.5	500-1040
8-Bit, 64B/66B, 1 Lane	5	128(2)	64B/66B	8	0	8	0	1	2	2	1	0	1	16.5	500-1040
12-Bit, 64B/66B, 3 Lanes	6	128(2)	64B/66B	12	0	12	0	3	2	2	2	1	1	8.25	500-1600
8-Bit, 64B/66B, 2 Lanes	7	256(2)	64B/66B	8	0	8	0	2	2	1	1	0	1	8.25	500-1600
12-Bit, 64B/66B, 2 Lanes	8	256(2)	64B/66B	12	0	12	0	2	2	3	2	0	3	12.375	500-1386.7
8-Bit, 8B/10B, 4 Lanes	9	32:32:256	8B/10B	8	0	8	0	3	2	1	2	0	—	5	500-1600
10-Bit, 8B/10B, 4 Lanes	10	32:32:256	8B/10B	10	0	10	0	4	4(1)	5	4	0	—	6.25	500-1600
12-Bit, 8B/10B, 8 Lanes	11	4:4:256	8B/10B	12	0	12	0	8	8(1)	8	5	0	—	4	500-1600
8-Bit, 8B/10B, 8 Lanes	12	32:32:256	8B/10B	8	0	8	0	8	2	1	4	0	—	2.5	500-1600
10-Bit, 8B/10B, 8 Lanes	13	32:32:256	8B/10B	10	0	10	0	8	8(1)	5	4	0	—	3.125	500-1600
12-Bit, 64B/66B, 4 Lanes	14	256(2)	64B/66B	12	0	12	0	4	4(1)	3	2	0	3	6.1875	500-1600
12-Bit, 64B/66B, 8 Lanes	15	256(2)	64B/66B	12	0	12	0	8	8(1)	3	2	2	3	3.09375	500-1600

(1) M equals L in these modes to allow the samples to be sent in time-order over L lanes without unnecessary buffering. The M parameter does not represent the actual number of converters. Interleave the M sample streams from each link in the receiver to produce the correct sample data; see mode diagrams for more details.
(2) In the 64B/66B modes, the K parameter is not directly programmable. K is related to E and F according to the equation K = 8 x 32 x E/F. K is not an actual parameter of the 64B/66B link layer.

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表 6-18. Single Channel Modes (supported by Quad, Dual and Single Channel Devices)

OPERATING MODE	USER-SPECIFIED PARAMETER		DERIVED PARAMETERS												INPUT CLOCK RANGE (MHz)
	JMODE	K [Min:Step:Max]	Encoding	N	CS	N'	CF	L	M	F	S	HD	E	R (Fbit / Fclk)	
12-Bit, 8B/10B, 2 Lanes	0	4:4:256	8B/10B	12	0	12	0	2	2(1)	8	5	0	—	8	500-1600
12-Bit, 8B/10B, 2 Lanes	1	16:16:256	8B/10B	12	0	12	0	2	1	2	2	1	—	10	500-1600
8-Bit, 8B/10B, 2 Lanes	2	32:32:256	8B/10B	8	0	8	0	1	4	1	1	0	—	10	500-1600
10-Bit, 8B/10B, 1 Lane	3	32:32:256	8B/10B	10	0	10	0	1	4	5	4	0	—	12.5	500-1372.8
12-Bit, 64B/66B, 1 Lane	4	128(2)	64B/66B	12	0	12	0	1	4	2	1	1	1	16.5	500-1040
8-Bit, 64B/66B, 1 Lanes	5	128(2)	64B/66B	8	0	8	0	1	4	2	1	0	1	16.5	500-1040
12-Bit, 64B/66B, 2 Lanes	6	128(2)	64B/66B	12	0	12	0	2	4	2	2	1	1	8.25	500-1600
8-Bit, 64B/66B, 1 Lane	7	256(2)	64B/66B	8	0	8	0	1	4	1	1	0	1	8.25	500-1600
12-Bit, 64B/66B, 1 Lane	8	256(2)	64B/66B	12	0	12	0	1	4	3	2	0	3	12.375	500-1386.7
8-Bit, 8B/10B, 2 Lanes	9	32:32:256	8B/10B	8	0	8	0	2	4	1	2	0	—	5	500-1600
10-Bit, 8B/10B, 2 Lanes	10	32:32:256	8B/10B	10	0	10	0	2	2(1)	5	4	0	—	6.25	500-1600
12-Bit, 8B/10B, 4 Lanes	11	4:4:256	8B/10B	12	0	12	0	4	4(1)	8	5	0	—	4	500-1600
8-Bit, 8B/10B, 4 Lanes	12	32:32:256	8B/10B	8	0	8	0	4	1	1	4	0	—	2.5	500-1600
10-Bit, 8B/10B, 4 Lanes	13	32:32:256	8B/10B	10	0	10	0	4	4(1)	5	4	0	—	3.125	500-1600
12-Bit, 64B/66B, 2 Lanes	14	256(2)	64B/66B	12	0	12	0	2	2(1)	3	2	0	3	6.1875	500-1600
12-Bit, 64B/66B, 4 Lanes	15	256(2)	64B/66B	12	0	12	0	4	4(1)	3	2	2	3	3.09375	500-1600

(1) M equals L in these modes to allow the samples to be sent in time-order over L lanes without unnecessary buffering. The M parameter does not represent the actual number of converters. Interleave the M sample streams from each link in the receiver to produce the correct sample data; see mode diagrams for more details.

(2) In the 64B/66B modes, the K parameter is not directly programmable. K is related to E and F according to the equation K = 8 x 32 x E/F. K is not an actual parameter of the 64B/66B link layer.

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The quad and dual channel devices have a total of 8 high-speed output drivers and the single channel device a total of 4 high-speed output drivers. The lanes and their derived configuration parameters are described in 表 6-19. For a specified JMODE, the lowest indexed lanes are used and the higher indexed lanes are automatically powered down. Always route the lowest indexed lanes to the logic device.

表 6-19. ADC12QJ1600-Q1 Lane Assignment and Parameters

DEVICE PIN DESIGNATION	Devices	DID (User Configured)	LID (Derived)
D0±	All	Set by DID	0
D1±	All	Set by DID	1
D2±	All	Set by DID	2
D3±	All	Set by DID	3
D4±	Quad/Dual only	Set by DID	4
D5±	Quad/Dual only	Set by DID	5
D6±	Quad/Dual only	Set by DID	6
D7±	Quad/Dual only	Set by DID	7

6.4.2.1 JESD204C Transport Layer Data Formats

The ADC core output samples are formatted in a specific fashion for each JMODE setting based on the transport layer settings for that JMODE. The following tables show the specific mapping formats for a single frame for each JMODE. The symbol definitions used in the JMODE tables is provided in 表 6-20. In all mappings the tail bits (T) are 0 (zero). All samples are formatted as MSB first, LSB last.

表 6-20. JMODE Table Symbol Definitions

NOTATION	DESCRIPTION
A_n	Sample n from channel A
B_n	Sample n from channel B
C_n	Sample n from channel C
D_n	Sample n from channel D
T	Tail bits, always set to 0

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表 6-21. JMODE 0 (12-bit, 8/4/2 lanes, 8B/10B)

OCTET	0		1		2		3		4		5		6		7	
NIBBLE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
D0	A_0			A_2			A_4			A_6			A_8			T
D1	A_1			A_3			A_5			A_7			A_9			T
D2	B_0			B_2			B_4			B_6			B_8			T
D3	B_1			B_3			B_5			B_7			B_9			T
D4 (Quad only)	C_0			C_2			C_4			C_6			C_8			T
D5 (Quad only)	C_1			C_3			C_5			C_7			C_9			T
D6 (Quad only)	D_0			D_2			D_4			D_6			D_8			T
D7 (Quad only)	D_1			D_3			D_5			D_7			D_9			T

表 6-22. JMODE 1 (12-bit, 6/3/2 lanes, 8B/10B)

OCTET	0		1	
NIBBLE	0	1	2	3
D0	A_0[11:0]			A_1[11:8]
D1	A_1[7:0]		Dual or Quad: B_0[11:4] Single: 0x00	
D2 (Quad or Dual only)	B_0[3:0]	B_1[11:0]		
D3 (Quad only)	C_0[11:0]			C_1[11:8]
D4 (Quad only)	C_1[7:0]		D_0[11:4]	
D5 (Quad only)	D_0[3:0]	D_1[11:0]		

表 6-23. JMODE 2 (8-bit, 4/2/1 lanes, 8B/10B)

OCTET	0	
NIBBLE	0	1
D0	A_0	
D1 (Dual or Quad only)	B_0	
D2 (Quad only)	C_0	
D3 (Quad only)	D_0	

表 6-24. JMODE 3 (10-bit, 4/2/1 lanes, 8B/10B)

OCTET	0		1		2		3		4	
NIBBLE	0	1	2	3	4	5	6	7	8	9
D0	A_0		A_1		A_2		A_3			
D1 (Dual or Quad only)	B_0		B_1		B_2		B_3			
D2 (Quad only)	C_0		C_1		C_2		C_3			
D3 (Quad only)	D_0		D_1		D_2		D_3			

表 6-25. JMODE 4 (12-bit, 3/2/1lanes, 64B/66B)

OCTET	0		1	
NIBBLE	0	1	2	3
D0	A_0[11:0]			Quad or Dual: B_0[11:8] Single: 0x0

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表 6-25. JMODE 4 (12-bit, 3/2/1lanes, 64B/66B) (続き)

OCTET	0		1	
NIBBLE	0	1	2	3
D1 (Dual or Quad only)	B_0[7:0]		Quad: C_0[11:4] Dual: 0x00	
D2 (Quad only)	C_0[3:0]	D_0[11:0]		

表 6-26. JMODE 5 (8-bit, 2/1/1 lanes, 64B/66B)

OCTET	0		1	
NIBBLE	0	1	2	3
D0	A_0		Quad or Dual: B_0 Single: 0x00	
D1 (Quad Only)	C_0		D_0	

表 6-27. JMODE 6 (12-bit, 6/3/2 lanes, 64B/66B)

OCTET	0		1	
NIBBLE	0	1	2	3
D0	A_0[11:0]			A_1[11:8]
D1	A_1[7:0]		Dual or Quad: B_0[11:4] Single: 0x00	
D2 (Dual or Quad only)	B_0[3:0]	B_1[11:0]		
D3 (Quad only)	C_0[11:0]			C_1[11:8]
D4 (Quad only)	C_1[7:0]		D_0[11:4]	
D5 (Quad only)	D_0[3:0]	D_1[11:0]		

表 6-28. JMODE 7 (8-bit, 4/2/1 lanes, 64B/66B)

OCTET	0	
NIBBLE	0	1
D0	A_0	
D1 (Dual or Quad only)	B_0	
D2 (Quad only)	C_0	
D3 (Quad only)	D_0	

表 6-29. JMODE 8 (12-bit, 4/2/1 lanes, 64B/66B)

OCTET	0		1		2	
NIBBLE	0	1	2	3	4	5
D0	A_0		A_1			
D1 (Dual or Quad only)	B_0		B_1			
D2 (Quad only)	C_0		C_1			
D3 (Quad only)	D_0		D_1			

表 6-30. JMODE 9 (8-bit, 8/4/2lanes, 8B/10B)

OCTET	0	
NIBBLE	0	1
D0	A_0	
D1	A_1	
D2 (Dual or Quad only)	B_0	
D3 (Dual or Quad only)	B_1	
D4 (Quad only)	C_0	
D5 (Quad only)	C_1	

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表 6-30. JMODE 9 (8-bit, 8/4/2lanes, 8B/10B) (続き)

OCTET	0	
NIBBLE	0	1
D6 (Quad only)	D_0	
D7 (Quad only)	D_1	

表 6-31. JMODE 10 (10-bit, 8/4/2 lanes, 8B/10B)

OCTET	0		1		2		3		4	
NIBBLE	0	1	2	3	4	5	6	7	8	9
D0	A_0		A_2		A_4		A_6			
D1	A_1		A_3		A_5		A_7			
D2 (Dual or Quad only)	B_0		B_2		B_4		B_6			
D3 (Dual or Quad only)	B_1		B_3		B_5		B_7			
D4 (Quad only)	C_0		C_2		C_4		C_6			
D5 (Quad only)	C_1		C_3		C_5		C_7			
D6 (Quad only)	D_0		D_2		D_4		D_6			
D7 (Quad only)	D_1		D_3		D_5		D_7			

表 6-32. JMODE 11 (12-bit, Dual/Single channel only, 8/4 lanes, 8B/10B)

OCTET	0		1		2		3		4		5		6		7	
NIBBLE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
D0	A_0		A_4		A_8		A_{12}		A_{16}							T
D1	A_1		A_5		A_9		A_{13}		A_{17}							T
D2	A_2		A_6		A_{10}		A_{14}		A_{18}							T
D3	A_3		A_7		A_{11}		A_{15}		A_{19}							T
D4 (Dual only)	B_0		B_4		B_8		B_{12}		B_{16}							T
D5 (Dual only)	B_1		B_5		B_9		B_{13}		B_{17}							T
D6 (Dual only)	B_2		B_6		B_{10}		B_{14}		B_{18}							T
D7 (Dual only)	B_3		B_7		B_{11}		B_{15}		B_{19}							T

表 6-33. JMODE 12 (8-bit, Dual/Single channel only, 8/4 lanes, 64B/66B)

OCTET	0	
NIBBLE	0	1
D0	A_0	
D1	A_1	
D2	A_2	
D3	A_3	
D4 (Dual only)	B_0	
D5 (Dual only)	B_1	
D6 (Dual only)	B_2	
D7 (Dual only)	B_3	

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表 6-34. JMODE 13 (10-bit, Dual/Single channel only, 8/4lanes, 8B/10B)

OCTET	0		1		2		3		4	
NIBBLE	0	1	2	3	4	5	6	7	8	9
D0	A_0		A_4		A_8		A_{12}			
D1	A_1		A_5		A_9		A_{13}			
D2	A_2		A_6		A_{10}		A_{14}			
D3	A_3		A_7		A_{11}		A_{15}			
D4 (Dual only)	B_0		B_4		B_8		B_{12}			
D5 (Dual only)	B_1		B_5		B_9		B_{13}			
D6 (Dual only)	B_2		B_6		B_{10}		B_{14}			
D7 (Dual only)	B_3		B_7		B_{11}		B_{15}			

表 6-35. JMODE 14 (12-bit, 8/4/2 lanes, 64B/66B)

OCTET	0		1		2	
NIBBLE	0	1	2	3	4	5
D0	A_0			A_2		
D1	A_1			A_3		
D2 (Dual or Quad only)	B_0			B_2		
D3 (Dual or Quad only)	B_1			B_3		
D4 (Quad only)	C_0			C_2		
D5 (Quad only)	C_1			C_3		
D6 (Quad only)	D_0			D_2		
D7 (Quad only)	D_1			D_3		

表 6-36. JMODE 15 (12-bit, Dual/Single channel only, 8/4 lanes, 64B/66B)

OCTET	0		1		2	
NIBBLE	0	1	2	3	4	5
D0	A_0			A_4		
D1	A_1			A_5		
D2	A_2			A_6		
D3	A_3			A_7		
D4 (Dual only)	B_0			B_4		
D5 (Dual only)	B_1			B_5		
D6 (Dual only)	B_2			B_6		
D7 (Dual only)	B_3			B_7		

6.4.2.2 64B/66B Sync Header Stream Configuration

The sync header stream can be used to identify bit errors on the link or to correct bit errors. Two modes of operation are available in ADC12QJ1600-Q1. Cyclic redundancy checking (CRC) can be used to identify bit errors. ADC12QJ1600-Q1 only supports 12-bit CRC (CRC-12) and does not support the optional 3-bit CRC-3 described by JESD204C. Alternatively, forward error correction (FEC) can be used to identify bit errors and then correct bit errors. For information on CRC-12, see Cyclic Redundancy Check (CRC Mode). For information on FEC, see Forward Error Correction (FEC) Mode.

6.4.2.3 Redundant Data Mode (Alternate Lanes)

JMODEs that use four or less lanes allow the use of redundancy on the JESD204C output. For instance, a system may have two FPGAs or ASICs connected to a single device, if the FPGA or ASIC is deemed the weak point in system reliability. In this example system, only one FPGA or ASIC operates at a time with the redundant FPGA or ASIC only being enabled if a fault is detected in the default FPGA or ASIC. To use this mode, the lower

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four SerDes lanes (D3-D0) must be routed to a single FPGA or ASIC and the upper four SerDes lanes (D7-D4) routed to the redundant FPGA or ASIC. The lower four lanes are the "default" lanes and the upper four lanes are the "alternate" lanes. The desired lanes are chosen by setting ALT_LANES parameter to 0 for the default lanes or 1 for the alternate lanes. Only one set of SerDes outputs can be operated at a time.

6.4.3 Power-Down Modes

The PD input pin allows the device devices to be entirely powered down. Power-down can also be controlled by MODE. The serial data output drivers are disabled when PD is high. When the device returns to normal operation, the JESD204 link must be re-established and the ADC pipelines contain meaningless information so the system must wait a sufficient time for the data to be flushed. The register configuration and calibration data is maintained during power down. A calibration cycle (foreground or background calibration) may be needed to return to optimal performance if the temperature changes drastically during the duration of power down. Pairs of channels can also be powered down using the CH_EN register. Do not use CH_EN to power down all four channels, use MODE or the PD pin instead.

6.4.4 Test Modes

A number of device test modes are available. These modes insert known patterns of information into the device data path for assistance with system debug, development, or characterization.

6.4.4.1 Serializer Test-Mode Details

Test modes are enabled by setting JTEST to the desired test mode. Each test mode is described in detail in the following sections. Regardless of the test mode, the serializer outputs (number of lanes, rate) are powered up based on JMODE. Only enable the test modes when the JESD204C link is disabled. 図 6-14 provides a diagram showing the various test mode insertion points.

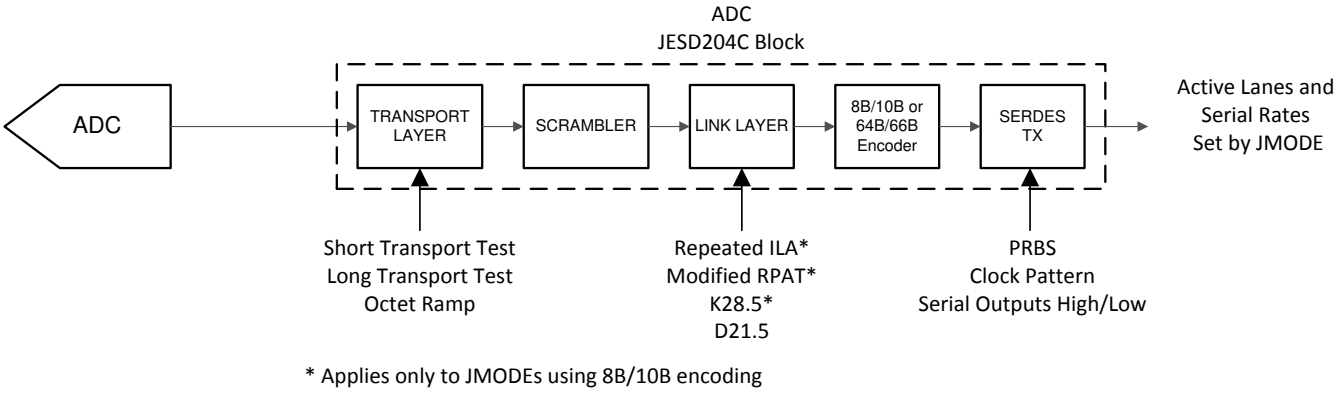

図 6-14. Test Mode Insertion Points

6.4.4.2 PRBS Test Modes

The PRBS test modes bypass the JESD204C transport layer and link layer and are therefore neither scrambled nor encoded. These test modes produce pseudo-random bit streams that comply with the ITU-T O.150 specification. These bit streams are used with lab test equipment or logic devices that can self-synchronize to the bit pattern. The initial phase of the pattern is not defined since the receiver self synchronizes.

The sequences are defined by a recursive equation. For example, Equation 12 defines the PRBS7 sequence.

$$y[n] = y[n - 6] \oplus y[n - 7] \quad (12)$$

where

- bit n is the XOR of bit [n – 6] and bit [n – 7], which are previously transmitted bits

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表 6-37 lists equations and sequence lengths for the available PRBS test modes where ⊕ is the XOR operation and y[n] represents bit n in the PRBS sequence. The initial phase of the pattern is unique for each lane.

表 6-37. PBRS Mode Equations

PRBS TEST MODE	SEQUENCE	SEQUENCE LENGTH (bits)
PRBS7	y[n] = y[n – 6]⊕y[n – 7]	127
PRBS9	y[n] = y[n – 5]⊕y[n – 9]	511
PRBS15	y[n] = y[n – 14]⊕y[n – 15]	32,767
PRBS23	y[n] = y[n – 18]⊕y[n – 23]	8,388,607
PRBS31	y[n] = y[n – 28]⊕y[n – 31]	2,147,483,647

6.4.4.3 Clock Pattern Mode

In the clock pattern mode, the JESD204C transport layer and link layer are bypassed, so the test sequence is neither scrambled nor encoded. The pattern consists of a 16-bit long sequence of 8 ones and 8 zeros (1111 1111 0000 0000) that repeats indefinitely.

6.4.4.4 Ramp Test Mode

In the ramp test mode, the JESD204C link layer operates normally, but the transport layer is disabled and the input from the formatter is ignored. In 8B/10B modes, the pattern begins after the ILA sequence finishes. In 64B/66B mode, the pattern begins after the serializers are initialized. Each lane transmits an identical octet stream that is encoded and scrambled by the link layer. The octet stream increments from 0x00 to 0xFF and repeats. This mode is available for both 8B/10B and 64B/66B modes.

6.4.4.5 Short and Long Transport Test Mode

JESD204C defines both short and long transport test modes to verify that the transport layers in the transmitter and receiver are operating correctly. The short transport test pattern used by device is dependent on the JMODE and are provided in Short Transport Test Pattern. The device does not support long transport test modes.

6.4.4.5.1 Short Transport Test Pattern

Short transport test patterns send a predefined octet format that repeats every frame. The short transport test patterns for each JMODE are defined in this section.

表 6-38. Short Transport Test Pattern for JMODE 0

OCTET	0		1		2		3		4		5		6		7	
NIBBLE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
D0	0xF01		0xF02				0xF03			0xF04			0xF05			T
D1	0xE11		0xE12				0xE13			0xE14			0xE15			T
D2 (Dual or Quad only)	0xD21		0xD22				0xD23			0xD24			0xD25			T
D3 (Dual or Quad only)	0xC31		0xC32				0xC33			0xC34			0xC35			T
D4 (Quad only)	0xB41		0xB42				0xB43			0xB44			0xB45			T
D5 (Quad only)	0xA51		0xA52				0xA53			0xA54			0xA55			T
D6 (Quad only)	0x961		0x962				0x963			0x964			0x965			T
D7 (Quad only)	0x871		0x872				0x873			0x874			0x875			T

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表 6-39. Short Transport Test Pattern for JMODE 1

OCTET	0		1	
NIBBLE	0	1	2	3
D0	0xF01			0xF
D1	0x02		0xE1	
D2 (Dual or Quad only)	0x1	0xE12		
D3 (Quad only)	0xD21			0xD
D4 (Quad only)	0x22		0xC3	
D5 (Quad only)	0x1	0xC32		

表 6-40. Short Transport Test Pattern for JMODE 2

OCTET	0	
NIBBLE	0	1
D0	0x01	
D1 (Dual or Quad only)	0x11	
D2 (Quad only)	0x21	
D3 (Quad only)	0x31	

表 6-41. Short Transport Test Pattern for JMODE 3

OCTET	0		1		2		3		4	
NIBBLE	0	1	2	3	4	5	6	7	8	9
D0	0x301		0x302		0x303		0x304			
D1 (Dual or Quad only)	0x211		0x212		0x213		0x214			
D2 (Quad only)	0x121		0x122		0x123		0x124			
D3 (Quad only)	0x031		0x032		0x033		0x034			

表 6-42. Short Transport Test Pattern for JMODE 4

OCTET	0		1	
NIBBLE	0	1	2	3
D0	0xF01			0xE
D1 (Dual or Quad only)	0x11		0xD2	
D2 (Quad only)	0x1	0xC31		

表 6-43. Short Transport Test Pattern for JMODE 5

OCTET	0		1	
NIBBLE	0	1	2	3
D0	0x01		0x11	
D1 (Quad only)	0x21		0x31	

表 6-44. Short Transport Test Pattern for JMODE 6

OCTET	0		1	
NIBBLE	0	1	2	3
D0	0xF01			0xF
D1	0x02		0xE1	
D2 (Dual or Quad only)	0x1	0xE12		
D3 (Quad only)	0xD21			0xD
D4 (Quad only)	0x22		0xC3	

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表 6-44. Short Transport Test Pattern for JMODE 6 (続き)

OCTET	0		1	
NIBBLE	0	1	2	3
D5 (Quad only)	0x1	0xC32		

表 6-45. Short Transport Test Pattern for JMODE 7

OCTET	0	
NIBBLE	0	1
D0	0x01	
D1 (Dual or Quad only)	0x11	
D2 (Quad only)	0x21	
D3 (Quad only)	0x31	

表 6-46. Short Transport Test Pattern for JMODE 8

OCTET	0		1		2	
NIBBLE	0	1	2	3	4	5
D0	0xF01		0xF02			
D1 (Dual or Quad only)	0xE11		0xE12			
D2 (Quad only)	0xD21		0xD22			
D3 (Quad only)	0xC31		0xC32			

表 6-47. Short Transport Test Pattern for JMODE 9

OCTET	0	
NIBBLE	0	1
D0	0x01	
D1	0x02	
D2 (Dual or Quad only)	0x11	
D3 (Dual or Quad only)	0x12	
D4 (Quad only)	0x21	
D5 (Quad only)	0x22	
D6 (Quad only)	0x31	
D7 (Quad only)	0x32	

表 6-48. Short Transport Test Pattern for JMODE 10

OCTET	0		1		2		3		4	
NIBBLE	0	1	2	3	4	5	6	7	8	9
D0	0x301		0x302		0x303		0x304			
D1	0x211		0x212		0x213		0x214			
D2 (Dual or Quad only)	0x121		0x122		0x123		0x124			
D3 (Dual or Quad only)	0x031		0x032		0x033		0x034			
D4 (Quad only)	0x341		0x342		0x343		0x344			
D5 (Quad only)	0x251		0x252		0x253		0x254			
D6 (Quad only)	0x161		0x162		0x163		0x164			
D7 (Quad only)	0x071		0x072		0x073		0x074			

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表 6-49. Short Transport Test Pattern for JMODE 11

OCTET	0		1		2		3		4		5		6		7	
NIBBLE	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
D0	0xF01		0xF02		0xF03		0xF04		0xF05							T
D1	0xE11		0xE12		0xE13		0xE14		0xE15							T
D2	0xD21		0xD22		0xD23		0xD24		0xD25							T
D3	0xC31		0xC32		0xC33		0xC34		0xC35							T
D4 (Dual only)	0xB41		0xB42		0xB43		0xB44		0xB45							T
D5 (Dual only)	0xA51		0xA52		0xA53		0xA54		0xA55							T
D6 (Dual only)	0x961		0x962		0x963		0x964		0x965							T
D7 (Dual only)	0x871		0x872		0x873		0x874		0x875							T

表 6-50. Short Transport Test Pattern for JMODE 12

OCTET	0	
NIBBLE	0	1
D0	0x01	
D1	0x02	
D2	0x03	
D3	0x04	
D4 (Dual only)	0x11	
D5 (Dual only)	0x12	
D6 (Dual only)	0x13	
D7 (Dual only)	0x14	

表 6-51. Short Transport Test Pattern for JMODE 13

OCTET	0		1		2		3		4	
NIBBLE	0	1	2	3	4	5	6	7	8	9
D0	0x301		0x302		0x303		0x304			
D1	0x211		0x212		0x213		0x214			
D2	0x121		0x122		0x123		0x124			
D3	0x031		0x032		0x033		0x034			
D4 (Dual only)	0x341		0x342		0x343		0x344			
D5 (Dual only)	0x251		0x252		0x253		0x254			
D6 (Dual only)	0x161		0x162		0x163		0x164			
D7 (Dual only)	0x071		0x072		0x073		0x074			

表 6-52. Short Transport Test Pattern for JMODE 14

OCTET	0		1		2	
NIBBLE	0	1	2	3	4	5
D0	0xF01		0xF02			
D1	0xE11		0xE12			
D2 (Dual or Quad only)	0xD21		0xD22			
D3 (Dual or Quad only)	0xC31		0xC32			
D4 (Quad only)	0xB41		0xB42			
D5 (Quad only)	0xA51		0xA52			

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表 6-52. Short Transport Test Pattern for JMODE 14 (続き)

OCTET	0		1		2	
NIBBLE	0	1	2	3	4	5
D6 (Quad only)	0x961		0x962			
D7 (Quad only)	0x871		0x872			

表 6-53. Short Transport Test Pattern for JMODE 15

OCTET	0		1		2	
NIBBLE	0	1	2	3	4	5
D0	0xF01		0xF02			
D1	0xE11		0xE12			
D2	0xD21		0xD22			
D3	0xC31		0xC32			
D4 (Dual only)	0xB41		0xB42			
D5 (Dual only)	0xA51		0xA52			
D6 (Dual only)	0x961		0x962			
D7 (Dual only)	0x871		0x872			

6.4.4.6 D21.5 Test Mode

In this test mode, the controller transmits a continuous stream of D21.5 characters (alternating 0s and 1s). This mode applies to 8B/10B and 64B/66B modes.

6.4.4.7 K28.5 Test Mode

In this test mode, the controller transmits a continuous stream of K28.5 characters. This mode only applies to 8B/10B modes.

6.4.4.8 Repeated ILA Test Mode

In this test mode, the JESD204C link layer operates normally, except that the ILA sequence (ILAS) repeats indefinitely instead of starting the data phase. Whenever the receiver issues a synchronization request, the transmitter initiates code group synchronization. Upon completion of code group synchronization, the transmitter repeatedly transmits the ILA sequence. This mode only applies to 8B/10B modes.

6.4.4.9 Modified RPAT Test Mode

A 12-octet repeating pattern is defined in INCITS TR-35-2004. The purpose of this pattern is to generate white spectral content for JESD204C compliance and jitter testing. 表 6-54 lists the pattern before and after 8B/10B encoding. This mode only applies to 8B/10B modes.

表 6-54. Modified RPAT Pattern Values

OCTET NUMBER	Dx.y NOTATION	8-BIT INPUT TO 8B/10B ENCODER	20b OUTPUT OF 8B/10B ENCODER (Two Characters)
0	D30.5	0xBE	0x86BA6
1	D23.6	0xD7	
2	D3.1	0x23	0xC6475
3	D7.2	0x47	
4	D11.3	0x6B	0xD0E8D
5	D15.4	0x8F	
6	D19.5	0xB3	0xCA8B4
7	D20.0	0x14	
8	D30.2	0x5E	0x7949E
9	D27.7	0xFB	

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表 6-54. Modified RPAT Pattern Values (続き)

OCTET NUMBER	Dx.y NOTATION	8-BIT INPUT TO 8B/10B ENCODER	20b OUTPUT OF 8B/10B ENCODER (Two Characters)
10	D21.1	0x35	0xAA665
11	D25.2	0x59	

6.4.5 Calibration Modes and Trimming

The device has two calibration modes available: foreground calibration and background calibration. When foreground calibration is initiated the ADCs are taken offline to calibrate and the output data becomes mid-code (0x000 in 2's complement) until calibration is finished. Background calibration allows the ADC to continue normal operation while the ADC cores are calibrated in the background by swapping in a different ADC core to take its place. Additional offset calibration features are available in both foreground and background calibration modes. Further, a number of ADC parameters can be trimmed to optimize performance in a user system.

The device consists of a total of six ADC cores. In foreground calibration mode ADC 0 samples INA±, ADC 1 samples INB±, ADC 4 samples INC± and ADC 5 samples IND±. In the background calibration modes, ADC core 2 is swapped in periodically for ADC 0 and ADC 1 and ADC core 3 is swapped in periodically for ADC 4 and 5 so that they can be calibrated without disrupting operation. 図 6-15 through 図 6-17 provide a diagrams of the calibration system including labeling of the ADC cores. When calibration is performed the linearity, gain, and offset voltage for each bank are calibrated to an internally generated calibration signal. The analog inputs can be driven during calibration, both foreground and background, except that when offset calibration (OS_CAL or BGOS_CAL) is used there must be no signals (or aliased signals) near DC for proper estimation of the offset (see the *Offset Calibration* section).

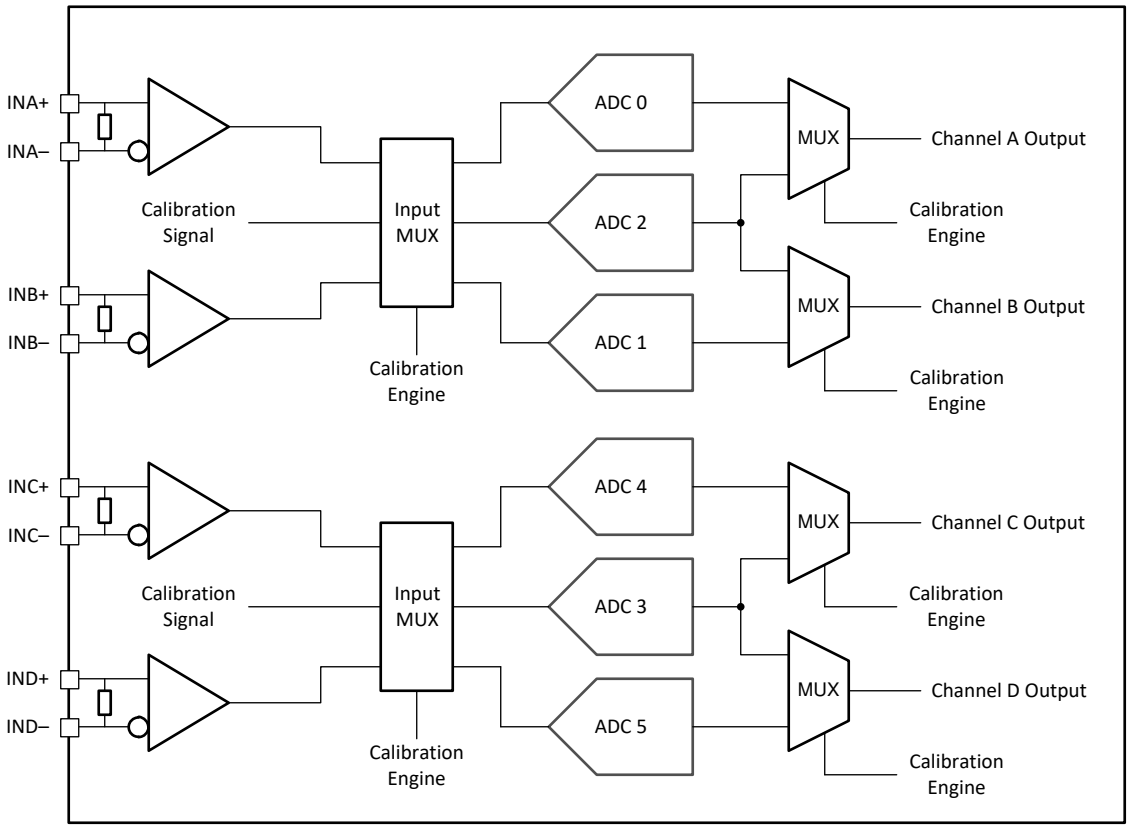

図 6-15. Quad Channel Calibration System Block Diagram

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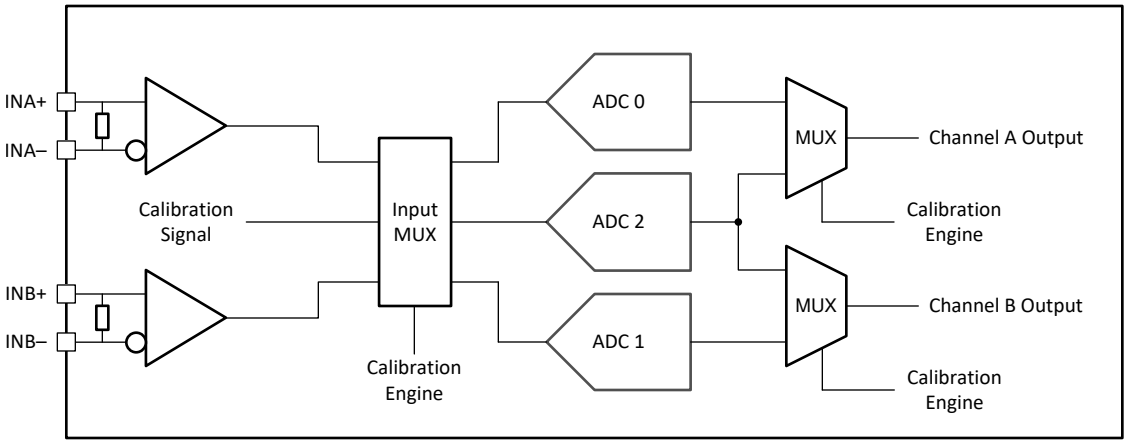

図 6-16. DualChannel Calibration System Block Diagram

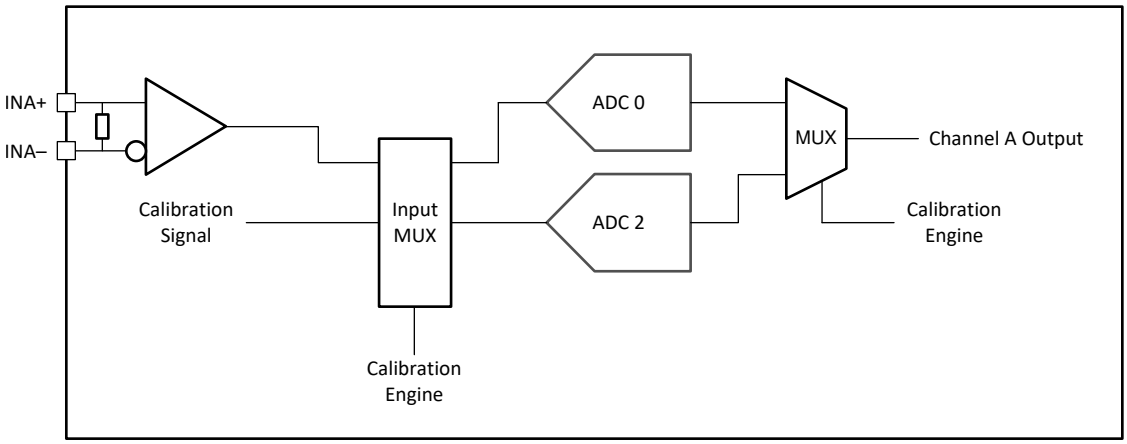

図 6-17. Single Channel Calibration System Block Diagram

In addition to calibration, a number of ADC parameters are user controllable to provide trimming for optimal performance. These parameters include input offset voltage, ADC gain and input termination resistance. The default trim values are programmed at the factory to unique values for each device that are determined to be optimal at the test system operating conditions. The user can read the factory-programmed values from the trim registers and adjust as desired. The register fields that control the trimming are labeled according to the input that is being sampled (INA±, INB±, INC± or IND±) and the ADC core that is being trimmed. The user is not expected to change the trim values as operating conditions change, however the user can change values as needed. Any custom trimming must be done on a per device basis because of process variations, meaning that there is no global optimal setting for all parts. See the *Trimming* section for information about the available trim parameters and associated registers.

6.4.5.1 Foreground Calibration Mode

Foreground calibration requires the ADC to stop converting the analog input signals during the procedure. Foreground calibration always runs on power-up and the user must wait a sufficient time before programming the device to make sure that the calibration is finished. Foreground calibration can be initiated by triggering the calibration engine. The trigger source can be either the CALTRIG pin or CAL_SOFT_TRIG and is chosen by setting CAL_TRIG_EN.

6.4.5.2 Background Calibration Mode

Background calibration mode allows the ADC to continuously operate, with no interruption of data. This continuous operation is accomplished by activating extra ADC cores that are calibrated to take over operation for

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one of the other previously active ADC cores. For the quad channel device, ADC cores 0 and 1 share one extra ADC core (ADC core 2) and ADC cores 4 and 5 share the other extra ADC core (ADC core 3). For the dual channel device, ADC cores 0 and 1 share one extra ADC core (ADC core 2). For the single channel device, ADC core 0 has one extra ADC core (ADC core 2). When an ADC core is taken off-line the ADC is then calibrated and then can in turn take over to allow the next ADC to be calibrated. This process operates continuously, ensuring the ADC cores always provide the optimum performance regardless of system operating condition changes. Only one of the cores is calibrated at a time to reduce power consumption, however the additional active ADC core does increase the power consumption in comparison to foreground calibration mode. The low-power background calibration (LPBG) mode discussed in the *Low-Power Background Calibration (LPBG) Mode* section provides reduced average power consumption in comparison with the standard background calibration mode. Background calibration can be enabled by setting CAL_BG. CAL_TRIG_EN must be set to 0 and CAL_SOFT_TRIG must be set to 1.

Great care has been taken to minimize effects on converted data as the core switching process occurs, however, small brief glitches may still occur on the converter data as the cores are swapped. It is recommended to set register ADC_SRC_DLY (address = 0x9A) to 0x1F and MUX_SEL_DLY (address = 0x9B) to 0x1E.

See the *Typical Characteristics* section for examples of possible glitches in sine-wave and DC signals.

6.4.5.3 Low-Power Background Calibration (LPBG) Mode

Low-power background calibration (LPBG) mode reduces the power-overhead of enabling additional ADC cores while still allowing background calibration of the ADC cores to maintain optimal performance as operating conditions change. LPBG calibration modifies the background calibration procedure by powering down the spare ADC cores until they are ready to be calibrated. Set LP_EN = 1 to enable the low-power background calibration feature. Calibration and swapping of ADC cores can be controlled either automatically by the device or manually by the system by setting LP_TRIG appropriately. Manual control (LP_TRIG=1) allows the system to trigger calibration in order to limit the number of calibration cycles that occur to avoid unnecessary core swaps or to keep power consumption at a minimum. For instance, the user may decide to run calibration only when the system temperature changes by some fixed temperature. If manual control is not necessary the automatic calibration control can be enabled (LP_TRIG=0) to calibrate at fixed time intervals.

In automatic calibration mode (LP_TRIG=0) the spare ADC core sleep time can be controlled by the LP_SLEEP_DLY register setting. LP_SLEEP_DLY is used to adjust the amount of time an ADC sleeps before waking up for calibration (when LP_EN=1 and LP_TRIG = 0). LP_WAKE_DLY sets how long the core is allowed to stabilize after being awoken before calibration begins. In automatic calibration control mode the freshly calibrated core is swapped in for an active core as soon as calibration finishes and the new spare core is powered down for the sleep duration before waking up and calibrating.

Manual calibration control is enabled by setting LP_TRIG high in order to use the calibration trigger (CAL_SOFT_TRIG or CALTRIG) to trigger calibrations and core swaps. When manual control is enabled (LP_TRIG=1) the spare ADC is held in sleep mode while the calibration trigger is high. Setting the calibration trigger low then wakes up the spare ADC core and starts the calibration routine after waiting for the specified wake delay (LP_WAKE_DLY). The spare ADC core is swapped in for an active core once calibration is complete and the calibration trigger is set high again. If the calibration trigger is held low, then the spare ADC core calibrates and powers until the calibration trigger goes high; therefore consuming power. ADC12QJ1600-Q1 can report when the spare ADC finishes calibration on the CALSTAT output pin by setting the CALSTAT pin to output the CAL_STOPPED signal (CAL_STATUS_SEL = 1). For lowest power consumption, set the calibration trigger high before calibration finishes to allow the spare ADC to swap in for an active ADC core as soon as calibration finishes. Otherwise, the ADC core swap can be timed manually by setting the calibration trigger high at the desired time to minimize system impact of potential glitches caused by the swapping procedure.

In LPBG mode there is an increase in power consumption during the ADC core calibration. The longer the spare ADC is held asleep the lower the average power consumption, however large shifts in operating conditions during the sleep cycle may cause degraded ADC performance due to non-optimized calibration data for the active ADC core. The power consumption roughly alternates between the power consumption in foreground calibration when the spare ADC core is sleeping to the power consumption in background calibration when the

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spare ADC is being calibrated. Design the power-supply network to handle the transient power requirements for this mode, including bulk capacitance after any power supply filtering network to help regulate the supply voltage during the supply transient.

6.4.6 Offset Calibration

Foreground calibration and background calibration modes inherently calibrate the offsets of the ADC cores; however, the input buffers sit outside of the calibration loop and therefore their offsets are not calibrated by the standard calibration process. A separate calibration is provided to correct the input buffer offsets.

There must be no signals at or near DC or aliased signals that fall at or near DC in order to properly calibration the offsets, requiring the system to specify this condition during normal operation or have the ability to mute the input signal during calibration. Foreground offset calibration is enabled via CAL_OS and only performs the calibration one time as part of the foreground calibration procedure. Background offset calibration is enabled via CAL_BGOS and continues to correct the offset as part of the background calibration routine to account for operating condition changes. When CAL_BGOS is set, the system must make sure that there are no DC or near DC signals or aliased signals that fall at or near DC during normal operation. Offset calibration can be performed as a foreground operation when using background calibration by setting CAL_OS to 1 before setting CAL_EN, but does not correct for variations as operating conditions change.

The offset calibration correction uses the input offset voltage trim registers (see OFS0 to OFS5) to correct the offset and therefore must not be written by the user when offset calibration is used. The user can read the calibrated values by reading the offset trim registers after calibration is completed and then use these values in the future to overwrite the factory trim values. Only read the values when FG_DONE is read as 1 when using foreground offset calibration (CAL_OS = 1) and do not read the values when using background offset calibration (CAL_BGOS = 1). Setting CAL_OS to 1 and CAL_BG to 1 performs an offset calibration of all six cores during the foreground calibration process.

Some systems, such as pulsed input systems, may purposefully apply a large external DC offset to the analog inputs to maximize the dynamic range for uni-polar signals. Standard offset calibration does not work for these systems because of the applied DC offset. These systems can instead set OSREF to use the spare ADC as the offset reference and then calibrate the main ADC cores to match the spare offset. This allows seamless offset transitions during background calibration swapping.

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6.4.7 Trimming

表 6-55 lists the parameters that can be trimmed and the associated registers.

表 6-55. Trim Register Descriptions

TRIM PARAMETER	TRIM REGISTER	NOTES
Band-gap reference	BG_TRIM	Measurement on BG output pin.
Input termination resistance	RTRIM_x, where x = A for INA±, B for INB±, etc.	The device must be powered on with a clock applied. The registers corresponding to the unused inputs for dual and single channel devices the have no affect.
Input offset voltage	OFSxy, where x = ADC core (0, 1, 2, 3, 4, or 5) and y = A for INA±, B for INB±, etc. or omitted (for ADC cores 0, 1, 4 and 5)	A different trim value is allowed for each ADC core (0, 1, 2, 3, 4 or 5) to allow more consistent offset performance in background calibration mode. Use CAL_OS with CAL_BG = 1 to get the trim values from these registers. The registers corresponding to the unused inputs for dual and single channel devices the have no affect.
Analog input gain	GAINxy, where x = ADC core (0, 1, 2, 3, 4, or 5) and y = A for INA±, B for INB±, etc. or omitted (for ADC cores 0, 1, 4 and 5)	Use this trim to match the gain for each ADC core. These registers are not affected by the calibration process. The registers corresponding to the unused inputs for dual and single channel devices the have no affect.
Full-scale input voltage	FS_RANGE	Full-scale input voltage adjustment that applies to all inputs. Use GAINxy to match the gain for each input.

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6.5 Programming

6.5.1 Using the Serial Interface

The serial interface is accessed using the following four pins: serial clock (SCLK), serial data in (SDI), serial data out (SDO), and serial interface chip-select ($\overline{SCS}$). Register access is enabled through the $\overline{SCS}$ pin.

6.5.2 $\overline{SCS}$

This signal must be asserted low to access a register through the serial interface. Setup and hold times with respect to the SCLK must be observed.

6.5.3 SCLK

Serial data input is accepted at the rising edge of this signal. SCLK has no minimum frequency requirement.

6.5.4 SDI

Each register access requires a specific 24-bit pattern at this input. This pattern consists of a read-and-write (R/W) bit, register address, and register value. The data are shifted in MSB first and multi-byte registers are always in little-endian format (least significant byte stored at the lowest address). Setup and hold times with respect to the SCLK must be observed (see the *Recommended Operating Conditions* table).

6.5.5 SDO

The SDO signal provides the output data requested by a read command. This output is high impedance during write bus cycles and during the read bit and register address portion of read bus cycles.

As shown in Serial Interface Protocol: Single Read/Write, each register access consists of 24 bits. The first bit is high for a read and low for a write.

The next 15 bits are the address of the register that is to be written to. During write operations, the last eight bits are the data written to the addressed register. During read operations, the last eight bits on SDI are ignored and, during this time, the SDO outputs the data from the addressed register. Serial Interface Protocol: Single Read/Write shows the serial protocol details.

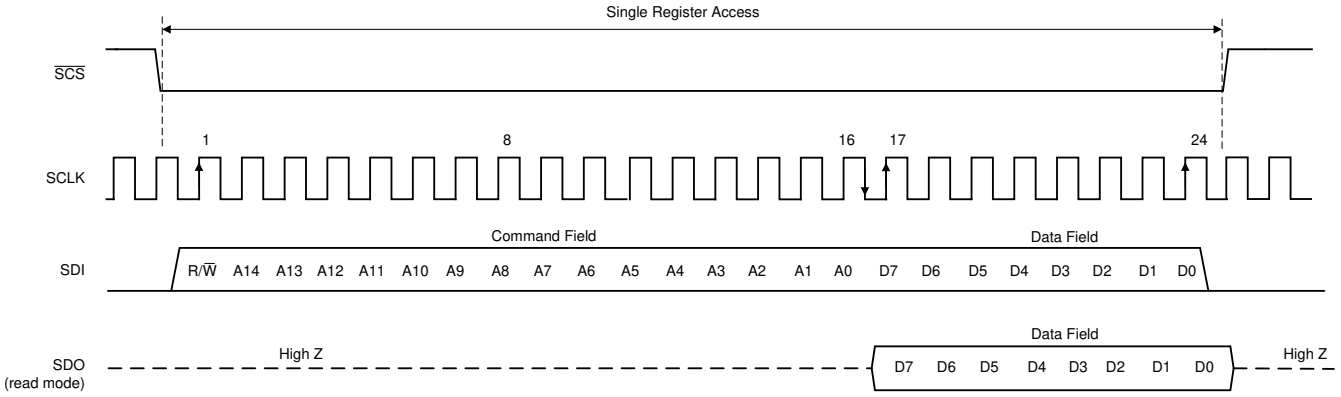

図 6-18. Serial Interface Protocol: Single Read/Write

6.5.6 Streaming Mode

The serial interface supports streaming reads and writes. In this mode, the initial 24 bits of the transaction specifics the access type, register address, and data value as normal. Additional clock cycles of write or read data are immediately transferred, as long as the $\overline{SCS}$ input is maintained in the asserted (logic low) state. The register address auto increments (default) or decrements for each subsequent 8-bit transfer of the streaming transaction. ASCEND controls whether the address value ascends (increments) or descends (decrements). Streaming mode can be disabled by setting the ADDR_HOLD bit. 図 6-19 shows the streaming mode transaction details.

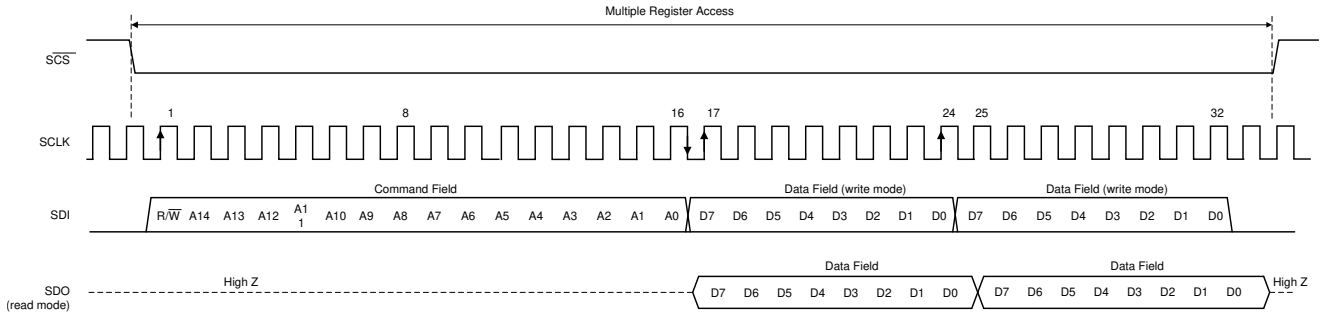

図 6-19. Serial Interface Protocol: Streaming Read/Write

See the SPI_Register_Map Registers section for detailed information regarding the registers

注

The serial interface must not be accessed during ADC calibration. Accessing the serial interface during this time impairs the performance of the device until the device is calibrated correctly. Writing or reading the serial registers also reduces dynamic ADC performance for the duration of the register access times.

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6.5.7 SPI_Register_Map Registers

表 6-56 lists the SPI_Register_Map registers. All register offset addresses not listed in 表 6-56 should be considered as reserved locations and the register contents should not be modified.

表 6-56. SPI_REGISTER_MAP Registers

Address	Acronym	Register Name	Section
0x0	CONFIG_A	Configuration A (default: 0x30)	Go
0x2	DEVICE_CONFIG	Device Configuration (default: 0x00)	Go
0xC	VENDOR_ID	Vendor Identification (Default = 0x0451)	Go
0x10	USR0	User SPI Configuration (Default: 0x00)	Go
0x29	CLK_CTRL0	Clock Control 0 (default: 0x80)	Go
0x2A	CLK_CTRL1	Clock Control 1 (default: 0x00)	Go
0x2B	CLK_CTRL2	Clock Control 2 (default: 0x10)	Go
0x2C	SYSREF_POS	SYSREF Capture Position (read-only status)	Go
0x30	FS_RANGE	FS_RANGE (default: 0xA000)	Go
0x37	LOW_POWER1	Low Power Mode 1 (default: 0x4B)	Go
0x3B	TMSTP_CTRL	TIMESTAMP (TMSTP) Control (default: 0x00)	Go
0x3C	PLLREFO_CTRL	PLL Reference Output Control (default: 0x01)	Go
0x3D	CPLL_FBDIV1	C-PLL Feedback Divider V and P (default: 0x00)	Go
0x3E	CPLL_FBDIV2	C-PLL Feedback Divider N (default: 0x20)	Go
0x3F	CPLL_VCOCTRL1	C-PLL Feedback Divider N (default: 0x4F)	Go
0x48	SER_PE	Serializer Pre-Emphasis Control (default: 0x00)	Go
0x57	TRIGOUT_CTRL	TRIGOUT Output Control (default: 0x00)	Go
0x58	CPLL_OVR	C-PLL Pin Override (default: 0x00)	Go
0x59	VCO_FREQ_TRIM	C-PLL VCO Frequency Trim (default: undefined)	Go
0x5C	CPLL_RESET	C-PLL / VCO Calibration Reset (default: 0x00)	Go
0x5D	VCO_CAL_CTRL	VCO Calibration Control (default: 0x40)	Go
0x5E	VCO_CAL_STATUS	VCO Calibration Status (read-only) (default: undefined)	Go
0x61	CAL_EN	Calibration Enable (Default: 0x01)	Go
0x62	CAL_CFG0	Calibration Configuration 0 (Default: 0x01)	Go
0x65	CAL_CFG1	Calibration Configuration 1 (Default: 0x01)	Go
0x68	CAL_AVG	Calibration Averaging (default: 0x61)	Go
0x6A	CAL_STATUS	Calibration Status (default: undefined) (read-only)	Go
0x6B	CAL_PIN_CFG	Calibration Pin Configuration (default: 0x00)	Go
0x6C	CAL_SOFT_TRIG	Calibration Software Trigger (default: 0x01)	Go
0x6E	CAL_LP	Low-Power Background Calibration (default: 0x88)	Go
0x7A	GAIN_TRIM	Gain DAC Trim (default from Fuse ROM)	Go
0x7C	BG_TRIM	Band-Gap Trim (default from Fuse ROM)	Go
0x7E	RTRIM_A	Resistor Trim for INA (default from Fuse ROM)	Go
0x7F	RTRIM_B	Resistor Trim for INB (default from Fuse ROM)	Go
0x80	RTRIM_C	Resistor Trim for INC (default from Fuse ROM)	Go
0x81	RTRIM_D	Resistor Trim for IND (default from Fuse ROM)	Go
0x9A	ADC_SRC_DLY	ADC Source Delay for Calibration	セクション 6.5.7.37
0x9B	MUX_SEL_DLY	MUX selection Delay for Calibration	セクション 6.5.7.38
0x9D	ADC_DITH	ADC Dither Control (default from Fuse ROM)	Go
0x160	LSB_CTRL	LSB Control Bit Output (default: 0x00)	Go
0x200	JESD_EN	JESD204C Subsystem Enable (default: 0x01)	Go

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表 6-56. SPI_REGISTER_MAP Registers (続き)

Address	Acronym	Register Name	Section
0x201	JMODE	JESD204C Mode (default: 0x00)	Go
0x202	KM1	JESD204C K Parameter (minus 1) (default: 0x1F)	Go
0x203	JSYNC_N	JESD204C Manual Sync Request (default: 0x01)	Go
0x204	JCTRL	JESD204C Control (default: 0x03)	Go
0x205	JTEST	JESD204C Test Control (default: 0x00)	Go
0x206	DID	JESD204C DID Parameter (default: 0x00)	Go
0x207	FCHAR	JESD204C Frame Character (default: 0x00)	Go
0x208	JESD_STATUS	JESD204C / System Status Register	Go
0x209	CH_EN	JESD204C Channel Enable (default: 0x03)	Go
0x20F	SHMODE	JESD204C Sync Word Mode (default: 0x00)	Go
0x210	SYNC_THRESH	JESD204C SYNC~ Threshold (default: 0x03)	Go
0x211	OVR_TH	Over-range Threshold (default: 0xF2)	Go
0x213	OVR_CFG	Over-range Enable / Hold Off (default: 0x07)	Go
0x270	INIT_STATUS	Initialization Status (read-only)	Go
0x29A	LOW_POWER2	Low Power Mode 2 (default: 0x0F)	Go
0x29B	LOW_POWER3	Low Power Mode 3 (default: 0x04)	Go
0x29C	LOW_POWER4	Low Power Mode 4 (default: 0x1B)	Go
0x2C0	ALARM	Alarm Interrupt (read-only)	Go
0x2C1	ALM_STATUS	Alarm Status (default: 0x3F, write to clear)	Go
0x2C2	ALM_MASK	Alarm Mask Register (default: 0x3F)	Go
0x2C4	FIFO_LANE_ALM	FIFO Overflow/Underflow Alarm (default: 0xFF)	Go
0x330	OFS0	Offset Adjustment for ADC0 (default from Fuse ROM)	Go
0x332	OFS1	Offset Adjustment for ADC1 (default from Fuse ROM)	Go
0x334	OFS2A	Offset Adjustment for ADC2 (INA±) (default from Fuse ROM)	Go
0x336	OFS2B	Offset Adjustment for ADC2 (INB±) (default from Fuse ROM)	Go
0x338	OFS3C	Offset Adjustment for ADC3 (INC±) (default from Fuse ROM)	Go
0x33A	OFS3D	Offset Adjustment for ADC3 (IND±) (default from Fuse ROM)	Go
0x33C	OFS4	Offset Adjustment for ADC4 (default from Fuse ROM)	Go
0x33E	OFS5	Offset Adjustment for ADC5 (default from Fuse ROM)	Go
0x360	GAIN0	Fine Gain Adjust for ADC0 (default from Fuse ROM)	Go
0x361	GAIN1	Fine Gain Adjust for ADC1 (default from Fuse ROM)	Go
0x362	GAIN2A	Fine Gain Adjust for ADC2 (INA±) (default from Fuse ROM)	Go
0x363	GAIN2B	Fine Gain Adjust for ADC2 (INB±) (default from Fuse ROM)	Go
0x364	GAIN3C	Fine Gain Adjust for ADC3 (INC±) (default from Fuse ROM)	Go
0x365	GAIN3D	Fine Gain Adjust for ADC3 (IND±) (default from Fuse ROM)	Go
0x366	GAIN4	Fine Gain Adjust for ADC4 (default from Fuse ROM)	Go
0x367	GAIN5	Fine Gain Adjust for ADC5 (default from Fuse ROM)	Go

Complex bit access types are encoded to fit into small table cells. 表 6-57 shows the codes that are used for access types in this section.

表 6-57. SPI_Register_Map Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read

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表 6-57. SPI_Register_Map Access Type Codes (続き)

Access Type	Code	Description
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value
Register Array Variables		
i,j,k,l,m,n		When these variables are used in a register name, an offset, or an address, they refer to the value of a register array where the register is part of a group of repeating registers. The register groups form a hierarchical structure and the array is represented with a formula.
y		When this variable is used in a register name, an offset, or an address it refers to the value of a register array.

6.5.7.1 CONFIG_A Register (Address = 0x0) [reset = 0x30]

CONFIG_A is shown in 図 6-20 and described in 表 6-58.

Return to the Summary Table.

Configuration A (default: 0x30)

図 6-20. CONFIG_A Register

7	6	5	4	3	2	1	0
SOFT_RESET	RESERVED	ASCEND	SDO_ACTIVE	RESERVED			
R/W-0x0	R/W-0x0	R/W-0x1	R-0x1	R/W-0x0			

表 6-58. CONFIG_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SOFT_RESET	R/W	0x0	Setting this bit causes a full reset of the chip and all SPI registers (including CONFIG_A). This bit is self-clearing. After writing this bit, the part may take up to 750ns to reset. During this time, do not perform any SPI transactions.
6	RESERVED	R/W	0x0	Must write default value.
5	ASCEND	R/W	0x1	0 : Address is decremented during streaming reads/writes 1 : Address is incremented during streaming reads/writes (default)
4	SDO_ACTIVE	R	0x1	Always returns 1. Always use SDO for SPI reads. No SDIO mode supported.
3:0	RESERVED	R/W	0x0	

6.5.7.2 DEVICE_CONFIG Register (Address = 0x2) [reset = 0x00]

DEVICE_CONFIG is shown in 図 6-21 and described in 表 6-59.

Return to the Summary Table.

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Device Configuration (default: 0x00)

図 6-21. DEVICE_CONFIG Register

7	6	5	4	3	2	1	0
RESERVED						MODE	
R/W-0x0						R/W-0x0	

表 6-59. DEVICE_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0x0	Must write default value.
1:0	MODE	R/W	0x0	0 : Normal operation (default) 1 : Reserved 2 : Reserved 3 : Power down (full device)

6.5.7.3 VENDOR_ID Register (Address = 0xC) [reset = 0x0]

VENDOR_ID is shown in 図 6-22 and described in 表 6-60.

Return to the Summary Table.

Vendor Identification (Default = 0x0451)

図 6-22. VENDOR_ID Register

15	14	13	12	11	10	9	8
VENDOR_ID							
R-0x0							
7	6	5	4	3	2	1	0
VENDOR_ID							
R-0x0							

表 6-60. VENDOR_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	VENDOR_ID	R	0x0	Always returns 0x0451 (Vendor ID for Texas Instruments)

6.5.7.4 USR0 Register (Address = 0x10) [reset = 0x00]

USR0 is shown in 図 6-23 and described in 表 6-61.

Return to the Summary Table.

User SPI Configuration (Default: 0x00)

図 6-23. USR0 Register

7	6	5	4	3	2	1	0
RESERVED							ADDR_HOLD
R/W-0x0							R/W-0x0

表 6-61. USR0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	Must write default value.

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表 6-61. USR0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	ADDR_HOLD	R/W	0x0	0 : Use ASCEND register to select address ascend/descend mode (default) 1 : Address stays constant throughout streaming operation; useful for reading and writing calibration vector information at the CAL_DATA register

6.5.7.5 CLK_CTRL0 Register (Address = 0x29) [reset = 0x80]

CLK_CTRL0 is shown in 図 6-24 and described in 表 6-62.

Return to the Summary Table.

Clock Control 0 (default: 0x80)

図 6-24. CLK_CTRL0 Register

7	6	5	4	3	2	1	0
RESERVED	SYSREF_PROC_EN	SYSREF_RECV_EN	SYSREF_ZOOM	SYSREF_SEL			
R/W-0x1	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0			

表 6-62. CLK_CTRL0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x1	Must write default value.
6	SYSREF_PROC_EN	R/W	0x0	This bit enables the SYSREF processor, which allows the device to process SYSREF events (default: disabled). SYSREF_RECV_EN must be set before setting SYSREF_PROC_EN.
5	SYSREF_RECV_EN	R/W	0x0	Set this bit to enable the SYSREF receiver circuit (default: disabled)
4	SYSREF_ZOOM	R/W	0x0	Set this bit to zoom in the SYSREF windowing status and delays (impacts SYSERF_POS and SYSREF_SEL). When set, the delays used in the SYSREF windowing feature (reported in the SYSREF_POS register) become smaller. Use SYSREF_ZOOM for high clock rates, specifically when multiple SYSREF valid windows are encountered in the SYSREF_POS register; see the SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) section.
3:0	SYSREF_SEL	R/W	0x0	Set this field to select which SYSREF delay to use. Set this field based on the results returned by SYSREF_POS; see the SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) section.

6.5.7.6 CLK_CTRL1 Register (Address = 0x2A) [reset = 0x00]

CLK_CTRL1 is shown in 図 6-25 and described in 表 6-63.

Return to the Summary Table.

Clock Control 1 (default: 0x00)

図 6-25. CLK_CTRL1 Register

7	6	5	4	3	2	1	0
RESERVED					DEVCLK_LVPECL_EN	SYSREF_LVPECL_EN	SYSREF_INVERTED
R/W-0x0					R/W-0x0	R/W-0x0	R/W-0x0

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表 6-63. CLK_CTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0x0	Must write default value.
2	DEVCLK_LVPECL_EN	R/W	0x0	Activate low voltage PECL mode for DEVCLK. The internal termination for each input pin (CLK+ and CLK–) becomes a 50-Ω resistor to ground. There is no input common-mode self-biasing for CLK± when DEVCLK_LVPECL_EN is set to 1.
1	SYSREF_LVPECL_EN	R/W	0x0	Activate low voltage PECL mode for SYSREF. The internal termination for each input pin (SYSREF+ and SYSREF–) becomes a 50-Ω resistor to ground. There is no input common-mode self-biasing for SYSREF± when SYSREF_LVPECL_EN is set to 1.
0	SYSREF_INVERTED	R/W	0x0	This bit inverts the SYSREF signal used for alignment.

6.5.7.7 CLK_CTRL2 Register (Address = 0x2B) [reset = 0x10]

CLK_CTRL2 is shown in 図 6-26 and described in 表 6-64.

Return to the Summary Table.

Clock Control 1 (default: 0x10)

図 6-26. CLK_CTRL2 Register

7	6	5	4	3	2	1	0
RESERVED					VA11Q_NOISESUPPR_EN	RESERVED	VCLK11_NOISESUPPR_EN
R/W-0x1					R/W-0x0	R/W-0x0	R/W-0x0

表 6-64. CLK_CTRL2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0x0	Must write default value.
2	VA11Q_NOISESUPPR_EN	R/W	0x0	When set, noise on VA11Q is suppressed while drawing ~ 20mA of current. This will reduce sampling jitter and reduce the reference clock spur in C-PLL modes and SYSREF spurs.
1	RESERVED	R/W	0x0	Must write default value.
0	VCLK11_NOISESUPPR_EN	R/W	0x0	When set, noise on VCLK11 is suppressed while drawing ~ 20mA of current. This will reduce sampling jitter and reduce the reference clock spur in C-PLL modes and SYSREF spurs.

6.5.7.8 SYSREF_POS Register (Address = 0x2C) [reset = 0x0]

SYSREF_POS is shown in 図 6-27 and described in 表 6-65.

Return to the Summary Table.

SYSREF Capture Position (read-only status)

図 6-27. SYSREF_POS Register

23	22	21	20	19	18	17	16
SYSREF_POS							
R-0x0							
15	14	13	12	11	10	9	8
SYSREF_POS							
R-0x0							
7	6	5	4	3	2	1	0

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図 6-27. SYSREF_POS Register (続き)

SYSREF_POS
R-0x0

表 6-65. SYSREF_POS Register Field Descriptions

Bit	Field	Type	Reset	Description
23:0	SYSREF_POS	R	0x0	Returns a 24-bit status value that indicates the position of the SYSREF edge with respect to CLK±. Use this to program SYSREF_SEL.

6.5.7.9 FS_RANGE Register (Address = 0x30) [reset = 0xA000]

FS_RANGE is shown in 図 6-28 and described in 表 6-66.

Return to the Summary Table.

FS_RANGE (default: 0xA000)

図 6-28. FS_RANGE Register

15	14	13	12	11	10	9	8
FS_RANGE							
R/W-0xA000							
7	6	5	4	3	2	1	0
FS_RANGE							
R/W-0xA000							

表 6-66. FS_RANGE Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	FS_RANGE	R/W	0xA000	These bits enable adjustment of the analog full-scale range for all channels. 0x0000: Settings below 0x2000 result in degraded performance 0x2000: 500 mVPP - Recommended minimum setting 0xA000: 800 mVPP (default) 0xFFFF: 1000 mVPP - Maximum setting, highest SNR

6.5.7.10 LOW_POWER1 Register (Address = 0x37) [reset = 0x4B]

LOW_POWER1 is shown in 図 6-29 and described in 表 6-67.

Return to the Summary Table.

Low Power Mode 1 (default: 0x4B)

図 6-29. LOW_POWER1 Register

7	6	5	4	3	2	1	0
LOW_POW_MODE1							
R/W-0x4B							

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表 6-67. LOW_POWER1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	LOW_POW_MODE1	R/W	0x4B	Set this register along with LOW_POWER2, LOW_POWER3 and LOW_POWER4 to enable Low Power Mode. All registers must be set together. Calibration must be performed after changing the operating mode: 0x46 : Low Power Mode (only valid when sampling rate is less than or equal to 1 GSPS) 0x4B : High Performance Mode (default) All other values are RESERVED Note: Must set CAL_EN to 0 and JESD_EN to 0 before changing this register.

6.5.7.11 TMSTP_CTRL Register (Address = 0x3B) [reset = 0x00]

TMSTP_CTRL is shown in 図 6-30 and described in 表 6-68.

Return to the Summary Table.

TIMESTAMP (TMSTP) Control (default: 0x00)

図 6-30. TMSTP_CTRL Register

7	6	5	4	3	2	1	0
RESERVED						TMSTP_LVPECL_EN	TMSTP_RECV_EN
R/W-0x0						R/W-0x0	R/W-0x0

表 6-68. TMSTP_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0x0	Must write default value.
1	TMSTP_LVPECL_EN	R/W	0x0	When set, activates the low voltage PECL mode for the differential TMSTP± input. The internal termination for each input pin (TMSTP+ and TMSTP–) becomes a 50-Ω resistor to ground. There is no input common-mode self-biasing for TMSTP± when TMSTP_LVPECL_EN is set to 1.
0	TMSTP_RECV_EN	R/W	0x0	Enables the differential differential TMSTP± input.

6.5.7.12 PLLREFO_CTRL Register (Address = 0x3C) [reset = 0x01]

PLLREFO_CTRL is shown in 図 6-31 and described in 表 6-69.

Return to the Summary Table.

PLL Reference Output Control (default: 0x01)

図 6-31. PLLREFO_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							PLLREFO_EN
R/W-0x0							R/W-0x1

表 6-69. PLLREFO_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	Must write default value.

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表 6-69. PLLREFO_CTRL Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	PLLREFO_EN	R/W	0x1	When set the reference clock output (PLLREFO±) is enabled whenever the PLL is enabled (PLL_EN=1). This bit defaults to 1 to cause PLLREFO± to enable automatically without SPI writes since PLLREFO± may be used to derive the SPI clock.

6.5.7.13 CPLL_FBDIV1 Register (Address = 0x3D) [reset = 0x00]

CPLL_FBDIV1 is shown in 図 6-32 and described in 表 6-70.

Return to the Summary Table.

C-PLL Feedback Divider V and P (default: 0x00)

図 6-32. CPLL_FBDIV1 Register

7	6	5	4	3	2	1	0
RESERVED				PLL_P_DIV		PLL_V_DIV	
R/W-0x0				R/W-0x0		R/W-0x0	

表 6-70. CPLL_FBDIV1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	Must write default value.
3:2	PLL_P_DIV	R/W	0x0	Controls the second feedback divider of C-PLL. The output of this divider is the sampling clock. Set CPLL_RESET=1 before changing PLL_P_DIV. 0 : divide-by-1 (default) 1 : divide-by-2 2 : divide-by-4 3 : RESERVED
1:0	PLL_V_DIV	R/W	0x0	Controls the first feedback divider of C-PLL. The output of this divider feeds the P divider. Set CPLL_RESET=1 before changing PLL_V_DIV. 0 : divide-by-5 (default) 1 : divide-by-4 2 : divide-by-3 3 : RESERVED

6.5.7.14 CPLL_FBDIV2 Register (Address = 0x3E) [reset = 0x20]

CPLL_FBDIV2 is shown in 図 6-33 and described in 表 6-71.

Return to the Summary Table.

C-PLL Feedback Divider N (default: 0x20)

図 6-33. CPLL_FBDIV2 Register

7	6	5	4	3	2	1	0
RESERVED		PLL_N_DIV					
R/W-0x0		R/W-0x20					

表 6-71. CPLL_FBDIV2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Must write default value.

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表 6-71. CPLL_FBDIV2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5:0	PLL_N_DIV	R/W	0x20	Controls the third feedback divider of C-PLL (default is divide-by-32). This divider divides the sampling clock to generate the PFD feedback clock. The value of PLL_N_DIV is the divider value. Values from 1 to 63 are supported. Set CPLL_RESET=1 before changing PLL_N_DIV.

6.5.7.15 CPLL_VCOCTRL1 Register (Address = 0x3F) [reset = 0x4F, recommended 0x4A]

CPLL_VCOCTRL1 is shown in 図 6-34 and described in 表 6-72.

Return to the Summary Table.

C-PLL Feedback Divider N (default: 0x4F)

図 6-34. CPLL_VCOCTRL1 Register

7	6	5	4	3	2	1	0
RESERVED	VCO_BIAS						
R/W-0x0	R/W-0x4F						

表 6-72. CPLL_VCOCTRL1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Must write default value.
6:0	VCO_BIAS	R/W	0x4F	Sets the bias levels for the C-PLL VCO. Write 0x4A to this field when using the C-PLL. Do not use the default value of 0x4F.

6.5.7.16 SER_PE Register (Address = 0x48) [reset = 0x00]

SER_PE is shown in 図 6-35 and described in 表 6-73.

Return to the Summary Table.

Serializer Pre-Emphasis Control (default: 0x00)

図 6-35. SER_PE Register

7	6	5	4	3	2	1	0
RESERVED				SER_PE			
R/W-0x0				R/W-0x0			

表 6-73. SER_PE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	Must write default value.
3:0	SER_PE	R/W	0x0	Sets the pre-emphasis for the SerDes output lanes. Pre-emphasis can be used to compensate for the high-frequency loss of the PCB trace. This is a global setting that affects all lanes (D[7:0]±).

6.5.7.17 TRIGOUT_CTRL Register (Address = 0x57) [reset = 0x00]

TRIGOUT_CTRL is shown in 図 6-36 and described in 表 6-74.

Return to the Summary Table.

TRIGOUT Output Control (default: 0x00)

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図 6-36. TRIGOUT_CTRL Register

7	6	5	4	3	2	1	0
TRIGOUT_EN	RESERVED					TRIGOUT	
R/W-0x0	R/W-0x0					R/W-0x0	

表 6-74. TRIGOUT_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	TRIGOUT_EN	R/W	0x0	0 : TRIGOUT± output buffer/divider is disabled. 1 : TRIGOUT± output buffer/divider is enabled. The RXCLK output can be used to provide a reference clock for the JESD204C receiver. Use the TRIGOUT_MODE field to adjust the output mode.
6:3	RESERVED	R/W	0x0	Must write default value.
2:0	TRIGOUT	R/W	0x0	Set the mode for the TRIGOUT± output. 0 : 16 UI clock (RX_DIV = 16) 1 : 32 UI clock (RX_DIV = 32) 2 : 64 UI clock (RX_DIV = 64) 3 : Resampled timestamp from TMSTP± 4-7 : RESERVED Note 1: Only change TRIGOUT_MODE when TRIGOUT_EN=0. Note 2: When TRIGOUT_MODE is 2 or less, TRIGOUT± is derived from the SerDes block. As a result, the TRIGOUT± output is briefly disrupted any time the serializer is re-initialized.

6.5.7.18 CPLL_OVR Register (Address = 0x58) [reset = 0x00]

CPLL_OVR is shown in 図 6-37 and described in 表 6-75.

Return to the Summary Table.

C-PLL Pin Override (default: 0x00)

図 6-37. CPLL_OVR Register

7	6	5	4	3	2	1	0
CPLL_OVR_EN	RESERVED	DIVREF_D_MODE		DIVREF_C_MODE		CPLLREF_SE_OVR_VALUE	CPLL_EN_OVR_VALUE
R/W-0x0	R/W-0x0	R/W-0x0		R/W-0x0		R/W-0x0	R/W-0x0

表 6-75. CPLL_OVR Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CPLL_OVR_EN	R/W	0x0	Set this bit to ignore the C-PLL configuration pins and use SPI registers instead. 0 : Pin Mode : The C-PLL is controlled by chip pins (PLL_EN, PLLREF_SE, CLKCFG0, CLKCFG1) 1 : SPI Mode : The C-PLL is controlled by SPI registers (CPLLREF_SE_OVR_VALUE, CPLL_EN_OVR_VALUE, DIVREF_C_MODE, DIVREF_D_MODE)
6	RESERVED	R/W	0x0	Must write default value.
5:4	DIVREF_D_MODE	R/W	0x0	When CPLL_OVR_EN=1, this field sets the ORD output function. When CPLL_OVR_EN=0, this field has no effect (CLKCFG0 and CLKCFG1 controls ORD functionality). 0 : Divided reference output is disabled. 1 : Output C-PLL reference clock divided by 1 on ORD. 2 : Output C-PLL reference clock divided by 2 on ORD. 3 : Output C-PLL reference clock divided by 4 on ORD. **Important Note: ORD cannot produce a clock unless ORC is also producing a clock).

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表 6-75. CPLL_OVR Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3:2	DIVREF_C_MODE	R/W	0x0	When CPLL_OVR_EN=1, this field sets the ORC output function. When CPLL_OVR_EN=0, this field has no effect (CLKCFG0 and CLKCFG1 controls ORC functionality). 0 : Divided reference output is disabled. 1 : Output C-PLL reference clock divided by 1 on ORC. 2 : Output C-PLL reference clock divided by 2 on ORC. 3 : Output C-PLL reference clock divided by 4 on ORC.
1	CPLLREF_SE_OVR_VALUE	R/W	0x0	When CPLL_OVR_EN=1, this bit enables the single-ended C-PLL reference clock input (SE_CLK) when set to 1 instead of the PLLREF_SE pin.
0	CPLL_EN_OVR_VALUE	R/W	0x0	When CPLL_OVR_EN=1, this bit enables the C-PLL when set to 1 instead of the PLL_EN pin.

6.5.7.19 VCO_FREQ_TRIM Register (Address = 0x59) [reset = 0x0]

VCO_FREQ_TRIM is shown in 図 6-38 and described in 表 6-76.

Return to the Summary Table.

C-PLL VCO Frequency Trim (default: undefined)

図 6-38. VCO_FREQ_TRIM Register

7	6	5	4	3	2	1	0
RESERVED	VCO_FREQ_TRIM						
R/W-0x0	R/W-0x0						

表 6-76. VCO_FREQ_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Must write default value.
6:0	VCO_FREQ_TRIM	R/W	0x0	Trims C-PLL VCO frequency. This field can be automatically set by the VCO calibration routine (see VCO_CAL_EN). After VCO calibration has been run the value can be read from this field and reprogrammed after future power-up cycles. If VCO calibration is running (VCO_CAL_EN=1 and VCO_CAL_DONE=0), you should not read or write this register since it will interfere with the calibration process.

6.5.7.20 CPLL_RESET Register (Address = 0x5C) [reset = 0x00]

CPLL_RESET is shown in 図 6-39 and described in 表 6-77.

Return to the Summary Table.

C-PLL / VCO Calibration Reset (default: 0x00)

図 6-39. CPLL_RESET Register

7	6	5	4	3	2	1	0
RESERVED							CPLL_RESET
R/W-0x0							R/W-0x0

表 6-77. CPLL_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	Must write default value.

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表 6-77. CPLL_RESET Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	CPLL_RESET	R/W	0x0	C-PLL / VCO calibration reset. Program CPLL_RESET=1 before programming the C-PLL (PLL_P_DIV, PLL_V_DIV, PLL_N_DIV, VCO_BIAS or VCO_CAL_CTRL). Program CPLL_RESET=0 after programming is completed.

6.5.7.21 VCO_CAL_CTRL Register (Address = 0x5D) [reset = 0x40]

VCO_CAL_CTRL is shown in 図 6-40 and described in 表 6-78.

Return to the Summary Table.

VCO Calibration Control (default: 0x40)

図 6-40. VCO_CAL_CTRL Register

7	6	5	4	3	2	1	0
RESERVED	VCO_CAL_STL			RESERVED			VCO_CAL_EN
R/W-0x0	R/W-0x4			R/W-0x0			R/W-0x0

表 6-78. VCO_CAL_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Must write default value.
6:4	VCO_CAL_STL	R/W	0x4	Program this field to adjust the settling time that the VCO calibration engine gives to the C-PLL each time it changes the VCO frequency trim (VCO_FREQ_TRIM). Larger numbers result in longer settling times.
3:1	RESERVED	R/W	0x0	Must write default value.
0	VCO_CAL_EN	R/W	0x0	Set this bit to enable the VCO calibration engine. The calibration commences once CPLL_RESET is programmed to 0. The calibration will automatically tune VCO_FREQ_TRIM to center the VCO frequency based on the reference frequency and PLL configuration. Note: The VCO_CAL_CTRL register should only be changed when CPLL_RESET=1.

6.5.7.22 VCO_CAL_STATUS Register (Address = 0x5E) [reset = 0x0]

VCO_CAL_STATUS is shown in 図 6-41 and described in 表 6-79.

Return to the Summary Table.

VCO Calibration Status (read-only) (default: undefined)

図 6-41. VCO_CAL_STATUS Register

7	6	5	4	3	2	1	0
RESERVED							VCO_CAL_DONE
R-0x0							R-0x0

表 6-79. VCO_CAL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	

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表 6-79. VCO_CAL_STATUS Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	VCO_CAL_DONE	R	0x0	This bit returns '1' once the VCO calibration engine has completed calibration (or calibration was skipped because VCO_CAL_EN=0). Once the calibration is completed, you can safely read or write the VCO_FREQ_TRIM register (never write VCO_FREQ_TRIM during calibration).

6.5.7.23 CAL_EN Register (Address = 0x61) [reset = 0x01]

CAL_EN is shown in 図 6-42 and described in 表 6-80.

Return to the Summary Table.

Calibration Enable (Default: 0x01)

図 6-42. CAL_EN Register

7	6	5	4	3	2	1	0
RESERVED							CAL_EN
R/W-0x0							R/W-0x1

表 6-80. CAL_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	Must write default value.
0	CAL_EN	R/W	0x1	Calibration Enable. Set high to run calibration. Set low to hold calibration in reset to program new calibration settings. Clearing CAL_EN also resets the clock dividers that clock the digital block and JESD204C interface. Some calibration registers require clearing CAL_EN before making any changes. All registers with this requirement contain a note in their descriptions. After changing the registers, set CAL_EN to re-run calibration with the new settings. Always set CAL_EN before setting JESD_EN. Always clear JESD_EN before clearing CAL_EN.

6.5.7.24 CAL_CFG0 Register (Address = 0x62) [reset = 0x01]

CAL_CFG0 is shown in 図 6-43 and described in 表 6-81.

Return to the Summary Table.

Calibration Configuration 0 (Default: 0x01)

図 6-43. CAL_CFG0 Register

7	6	5	4	3	2	1	0
RESERVED				CAL_BGOS	CAL_OS	CAL_BG	CAL_FG
R/W-0x0				R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x1

表 6-81. CAL_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	Must write default value.
3	CAL_BGOS	R/W	0x0	0 : Disable background offset calibration (default) 1 : Enable background offset calibration (requires CAL_BG to be set).
2	CAL_OS	R/W	0x0	0 : Disable foreground offset calibration (default) 1 : Enable foreground offset calibration (requires CAL_FG to be set).

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表 6-81. CAL_CFG0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1	CAL_BG	R/W	0x0	0 : Disable background calibration (default) 1 : Enable background calibration
0	CAL_FG	R/W	0x1	0 : Reset calibration values, skip foreground calibration. 1 : Reset calibration values, then run foreground calibration (default).

6.5.7.25 CAL_CFG1 Register (Address = 0x65) [reset = 0x01]

CAL_CFG1 is shown in 図 6-44 and described in 表 6-82.

Return to the Summary Table.

Calibration Configuration 1 (Default: 0x01)

図 6-44. CAL_CFG1 Register

7	6	5	4	3	2	1	0
RESERVED					OSREF	RESERVED	
R/W-0x0					R/W-0x0	R/W-0x1	

表 6-82. CAL_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0x0	Must write default value.
2	OSREF	R/W	0x0	Defines which reference is used for offset calibration: 0 : Use mid-code as the reference (calibrate to zero-offset). The analog input signal must have no offset during offset calibration (typically true if AC-coupled). 1 : Use the spare ADC output samples as the reference (calibrates primary ADC offsets to match the spare ADC that stands in for them). The analog input signal can have an offset (e.g. DC-coupled). Only use this mode when CAL_BG=1. Setting OSREF=1 while CAL_BG=0 will produce undefined results.
1:0	RESERVED	R/W	0x1	Must write default value.

6.5.7.26 CAL_AVG Register (Address = 0x68) [reset = 0x61]

CAL_AVG is shown in 図 6-45 and described in 表 6-83.

Return to the Summary Table.

Calibration Averaging (default: 0x61)

図 6-45. CAL_AVG Register

7	6	5	4	3	2	1	0
RESERVED	OS_AVG			RESERVED	CAL_AVG		
R/W-0x0	R/W-0x6			R/W-0x0	R/W-0x1		

表 6-83. CAL_AVG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	Must write default value.
6:4	OS_AVG	R/W	0x6	Select the amount of averaging used for the offset correction routine. A larger number corresponds to more averaging.
3	RESERVED	R/W	0x0	Must write default value.

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表 6-83. CAL_AVG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
2:0	CAL_AVG	R/W	0x1	Select the amount of averaging used for the linearity calibration routine. A larger number corresponds to more averaging.

6.5.7.27 CAL_STATUS Register (Address = 0x6A) [reset = 0x0]

CAL_STATUS is shown in 図 6-46 and described in 表 6-84.

Return to the Summary Table.

Calibration Status (default: undefined) (read-only)

図 6-46. CAL_STATUS Register

7	6	5	4	3	2	1	0
RESERVED			CAL_STAT			CAL_STOPPED	FG_DONE
R-0x0			R-0x0			R-0x0	R-0x0

表 6-84. CAL_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R	0x0	
4:2	CAL_STAT	R	0x0	Calibration status code
1	CAL_STOPPED	R	0x0	This bit returns a 1 when background calibration is successfully stopped at the requested phase. This bit returns a 0 when calibration starts operating again. If background calibration is disabled, this bit is set when foreground calibration is completed or skipped.
0	FG_DONE	R	0x0	This bit is high to indicate that foreground calibration has completed (or was skipped).

6.5.7.28 CAL_PIN_CFG Register (Address = 0x6B) [reset = 0x00]

CAL_PIN_CFG is shown in 図 6-47 and described in 表 6-85.

Return to the Summary Table.

Calibration Pin Configuration (default: 0x00)

図 6-47. CAL_PIN_CFG Register

7	6	5	4	3	2	1	0
RESERVED					CAL_STATUS_SEL		CAL_TRIG_EN
R/W-0x0					R/W-0x0		R/W-0x0

表 6-85. CAL_PIN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0x0	Must write default value.
2:1	CAL_STATUS_SEL	R/W	0x0	0 : CALSTAT output matches FG_DONE. 1 : CALSTAT output matches CAL_STOPPED. 2 : CALSTAT output matches ALARM. 3 : CALSTAT output is always low.

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表 6-85. CAL_PIN_CFG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	CAL_TRIG_EN	R/W	0x0	This bit selects the hardware or software trigger source. 0 : Use the CAL_SOFT_TRIG register for the calibration trigger. The CALTRIG input is disabled (ignored). 1 : Use the CALTRIG input for the calibration trigger. The CAL_SOFT_TRIG register is ignored.

6.5.7.29 CAL_SOFT_TRIG Register (Address = 0x6C) [reset = 0x01]

CAL_SOFT_TRIG is shown in 図 6-48 and described in 表 6-86.

Return to the Summary Table.

Calibration Software Trigger (default: 0x01)

図 6-48. CAL_SOFT_TRIG Register

7	6	5	4	3	2	1	0
RESERVED							CAL_SOFT_TRIG
R/W-0x0							R/W-0x1

表 6-86. CAL_SOFT_TRIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	Must write default value.
0	CAL_SOFT_TRIG	R/W	0x1	CAL_SOFT_TRIG is a software bit to provide the functionality of the CALTRIG input pin when there are no hardware resources to drive CALTRIG. Program CAL_TRIG_EN=0 to use CAL_SOFT_TRIG for the calibration trigger. Note: If no calibration trigger is needed, leave CAL_TRIG_EN=0 and CAL_SOFT_TRIG=1 (trigger set high).

6.5.7.30 CAL_LP Register (Address = 0x6E) [reset = 0x88]

CAL_LP is shown in 図 6-49 and described in 表 6-87.

Return to the Summary Table.

Low-Power Background Calibration (default: 0x88)

図 6-49. CAL_LP Register

7	6	5	4	3	2	1	0
LP_SLEEP_DLY			LP_WAKE_DLY		RESERVED	LP_TRIG	LP_EN
R/W-0x4			R/W-0x1		R/W-0x0	R/W-0x0	R/W-0x0

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表 6-87. CAL_LP Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	LP_SLEEP_DLY	R/W	0x4	These bits adjust how long an ADC sleeps before waking for calibration (only applies when LP_EN = 1 and LP_TRIG = 0). Values below 4 are not recommended because of limited overall power reduction benefits. 0: Sleep delay = 1,152 × tCLK 1: Sleep delay = 4,194,432 × tCLK 2: Sleep delay = 33,554,560 × tCLK 3: Sleep delay = 268,435,584 × tCLK 4: Sleep delay = 2,147,483,776 × tCLK (default, approximately 2.15 seconds with a 1.0-GHz clock) 5: Sleep delay = 17,179,869,312× tCLK 6: Sleep delay = 137,438,953,600 × tCLK 7: Sleep delay = 1,099,511,627,904 × tCLK
4:3	LP_WAKE_DLY	R/W	0x1	These bits adjust how much time is provided for settling before calibrating an ADC after the ADC wakes up (only applies when LP_EN = 1). Values lower than 1 are not recommended because there is insufficient time for the core to stabilize before calibration begins. 0: Wake delay = 1,152 × tCLK 1: Wake delay = 33,554,560 × tCLK (default, approximately 34 ms with a 1.0-GHz clock) 2: Wake delay = 268,435,584 × tCLK 3: Wake delay = 2,147,483,776 × tCLK
2	RESERVED	R/W	0x0	Must write default value.
1	LP_TRIG	R/W	0x0	0 : ADC sleep duration is set by LP_SLEEP_DLY (autonomous mode). 1 : ADCs sleep until awoken by a trigger. An ADC is awoken when the calibration trigger is low. The offline ADC is sleeping when the calibration trigger is high.
0	LP_EN	R/W	0x0	0 : Disable low-power background calibration (default) 1 : Enable low-power background calibration (only applies when CAL_BG=1).

6.5.7.31 GAIN_TRIM Register (Address = 0x7A) [reset = 0x0]

GAIN_TRIM is shown in 図 6-50 and described in 表 6-88.

Return to the Summary Table.

Gain DAC Trim (default from Fuse ROM)

図 6-50. GAIN_TRIM Register

7	6	5	4	3	2	1	0
GAIN_TRIM							
R/W-0x0							

表 6-88. GAIN_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	GAIN_TRIM	R/W	0x0	This register trims the gain of all ADC cores. FS_RANGE should be used for full-scale range adjustment instead of GAIN_TRIM.

6.5.7.32 BG_TRIM Register (Address = 0x7C) [reset = 0x0]

BG_TRIM is shown in 図 6-51 and described in 表 6-89.

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Band-Gap Trim (default from Fuse ROM)

図 6-51. BG_TRIM Register

7	6	5	4	3	2	1	0
RESERVED				BG_TRIM			
R/W-0x0				R/W-0x0			

表 6-89. BG_TRIM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	Must write default value.
3:0	BG_TRIM	R/W	0x0	This register enables trimming of the internal band-gap reference. After reset, the factory trimmed value can be read and adjusted as required.

6.5.7.33 RTRIM_A Register (Address = 0x7E) [reset = 0x0]

RTRIM_A is shown in 図 6-52 and described in 表 6-90.

Return to the Summary Table.

Resistor Trim for INA (default from Fuse ROM)

図 6-52. RTRIM_A Register

7	6	5	4	3	2	1	0
RTRIM_A							
R/W-0x0							

表 6-90. RTRIM_A Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RTRIM_A	R/W	0x0	This register controls the INA± ADC input termination trim. After reset, the factory trimmed value can be read and adjusted as required.

6.5.7.34 RTRIM_B Register (Address = 0x7F) [reset = 0x0]

RTRIM_B is shown in 図 6-53 and described in 表 6-91.

Return to the Summary Table.

Resistor Trim for INB (default from Fuse ROM)

図 6-53. RTRIM_B Register

7	6	5	4	3	2	1	0
RTRIM_B							
R/W-0x0							

表 6-91. RTRIM_B Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RTRIM_B	R/W	0x0	This register controls the INB± ADC input termination trim. After reset, the factory trimmed value can be read and adjusted as required.

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6.5.7.35 RTRIM_C Register (Address = 0x80) [reset = 0x0]

RTRIM_C is shown in 図 6-54 and described in 表 6-92.

Return to the Summary Table.

Resistor Trim for INC (default from Fuse ROM)

図 6-54. RTRIM_C Register

7	6	5	4	3	2	1	0
RTRIM_C							
R/W-0x0							

表 6-92. RTRIM_C Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RTRIM_C	R/W	0x0	This register controls the INC± ADC input termination trim. After reset, the factory trimmed value can be read and adjusted as required.

6.5.7.36 RTRIM_D Register (Address = 0x81) [reset = 0x0]

RTRIM_D is shown in 図 6-55 and described in 表 6-93.

Return to the Summary Table.

Resistor Trim for IND (default from Fuse ROM)

図 6-55. RTRIM_D Register

7	6	5	4	3	2	1	0
RTRIM_D							
R/W-0x0							

表 6-93. RTRIM_D Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	RTRIM_D	R/W	0x0	This register controls the IND± ADC input termination trim. After reset, the factory trimmed value can be read and adjusted as required.

6.5.7.37 ADC Source Control Delay (Address = 0x9A) [reset = 0x08]

ADC_SRC_DLY is shown in AC_SRC_DLY Register and described in ADC_SRC_DLY Register Field Descriptions. Only change this register while CAL_EN is 0.

Return to the Summary Table.

ADC Dither Control (default from Fuse ROM)

図 6-56. ADC_SRC_DLY Register

7	6	5	4	3	2	1	0
RESERVED							
R/W-0x0							

表 6-94. ADC_SRC_DLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.

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表 6-94. ADC_SRC_DLY Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4:0	ADC_SRC_DLY	R/W	0x08	Adjusts how long two ADCs will sample the same input at the same clock phase during background ADC swaps. The default value is appropriate for all ADCCLK frequencies. If using a reduced ADCCLK frequency, ADC_SRC_DLY can be set to 7 to reduce the glitch duration during fast background ADC swaps, however there is a greater risk of having a large glitch amplitude. Two ADCs will sample the same input for 4+2*ADC_SRC_DLY ADCCLK cycles. ADC_SRC_DLY can be programmed from 0 to 31.

6.5.7.38 MUX Select Delay Register (Address = 0x9B) [reset = 0x07]

MUX_SEL_DLY is shown in MUX_SEL_DLY Register and described in MUX_SEL_DLY Register Field Descriptions.

Return to the Summary Table.

図 6-57. MUX_SEL_DLY Register

7	6	5	4	3	2	1	0
RESERVED				MUX_SEL_DLY			
R/W-0x0				R/W-0x07			

表 6-95. MUX_SEL_DLY Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.
4:0	MUX_SEL_DLY	R/W	0x07	Adjusts the delay added to the internal mux selection signal. This signal controls multiplexors that steer ADC core output data into the encoders. This delay only applies during background ADC swaps. This delay needs to be tuned to swap between sample streams during a small window of time when both sample streams are valid. MUX_SEL_DLY can be programmed from 0 to 31.

6.5.7.39 ADC_DITH Register (Address = 0x9D) [reset = 0x0]

ADC_DITH is shown in 図 6-58 and described in 表 6-96.

Return to the Summary Table.

ADC Dither Control (default from Fuse ROM)

図 6-58. ADC_DITH Register

7	6	5	4	3	2	1	0
RESERVED					ADC_DITH_ERR	ADC_DITH_AMP	ADC_DITH_EN
R/W-0x0					R/W-0x0	R/W-0x0	R/W-0x0

表 6-96. ADC_DITH Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0x0	Must write default value.

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表 6-96. ADC_DITH Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
2	ADC_DITH_ERR	R/W	0x0	Small rounding errors may occur when subtracting the dither signal. The error can be chosen to either slightly degrade SNR or to slightly increase the DC offset and FS/2 spur. In addition, the FS/4 spur will also be increased slightly while in single channel mode. 0 : Rounding error degrades SNR 1 : Rounding error degrades DC offset, FS/2 spur and FS/4 spur
1	ADC_DITH_AMP	R/W	0x0	0 : Small dither for better SNR (default) 1 : Large dither for better spurious performance
0	ADC_DITH_EN	R/W	0x0	Set this bit to enable ADC dither. Dither can improve spurious performance at the expense of slightly degraded SNR. The dither amplitude (ADC_DITH_AMP) can be used to further tradeoff SNR and spurious performance.

6.5.7.40 LSB_CTRL Register (Address = 0x160) [reset = 0x00]

LSB_CTRL is shown in 図 6-59 and described in 表 6-97.

Return to the Summary Table.

LSB Control Bit Output (default: 0x00)

図 6-59. LSB_CTRL Register

7	6	5	4	3	2	1	0
RESERVED							TIME_STAMP_EN
R/W-0x0							R/W-0x0

表 6-97. LSB_CTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	Must write default value.
0	TIME_STAMP_EN	R/W	0x0	When set, the transport layer transmits the timestamp signal on the LSB of the output samples. The latency of the timestamp signal (through the entire chip) should match the latency of the analog ADC inputs. Please also set TMSTP_RECV_EN when using TIME_STAMP_EN. Note 1: The control bit is placed on the LSB of the JESD204C samples. In some cases, the JESD204C sample width (N) is greater than the sample width from the ADC. In these cases, the control bit does not replace the LSB of the ADC sample since it is placed at the LSB of the N-bit field). Note 2: The control bit that is enabled by this register is never advertised in the ILA (CS is 0 in the ILA).

6.5.7.41 JESD_EN Register (Address = 0x200) [reset = 0x01]

JESD_EN is shown in 図 6-60 and described in 表 6-98.

Return to the Summary Table.

JESD204C Subsystem Enable (default: 0x01)

図 6-60. JESD_EN Register

7	6	5	4	3	2	1	0
RESERVED							JESD_EN
R/W-0x0							R/W-0x1

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表 6-98. JESD_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	Must write default value.
0	JESD_EN	R/W	0x1	0 : Disable JESD204C interface 1 : Enable JESD204C interface Note: Before altering other JESD204C registers, you must clear JESD_EN. When JESD_EN is 0, the block is held in reset and the serializers are powered down. The clocks are gated off to save power. The LMFC/LEMC counter is also held in reset, so SYSREF will not align the LMFC/LEMC. Note: Always set CAL_EN before setting JESD_EN. Note: Always clear JESD_EN before clearing CAL_EN.

6.5.7.42 JMODE Register (Address = 0x201) [reset = 0x00]

JMODE is shown in 図 6-61 and described in 表 6-99.

Return to the Summary Table.

JESD204C Mode (default: 0x00)

図 6-61. JMODE Register

7	6	5	4	3	2	1	0
RESERVED				JMODE			
R/W-0x0				R/W-0x0			

表 6-99. JMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Must write default value.
5:0	JMODE	R/W	0x0	Specifies the JESD204C output mode. See JESD204C Mode table. Note: This register should only be changed when JESD_EN=0 and CAL_EN=0.

6.5.7.43 KM1 Register (Address = 0x202) [reset = 0x1F]

KM1 is shown in 図 6-62 and described in 表 6-100.

Return to the Summary Table.

JESD204C K Parameter (minus 1) (default: 0x1F)

図 6-62. KM1 Register

7	6	5	4	3	2	1	0
KM1							
R/W-0x1F							

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表 6-100. KM1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	KM1	R/W	0x1F	K is the number of frames per multiframe and this register must be programmed as K-1. Depending on the JMODE setting, there are constraints on the legal values of K (see K parameter in JESD204C Mode table). The default value is KM1=31, which corresponds to K=32. Note: For modes using the 64B/66B link layer, the KM1 register is ignored and the value of K is determined from E and F (which are derived from JMODE). The effective value of K is 256*E/F. Note: This register should only be changed when JESD_EN is 0.

6.5.7.44 JSYNC_N Register (Address = 0x203) [reset = 0x01]

JSYNC_N is shown in 図 6-63 and described in 表 6-101.

Return to the Summary Table.

JESD204C Manual Sync Request (default: 0x01)

図 6-63. JSYNC_N Register

7	6	5	4	3	2	1	0
RESERVED							JSYNC_N
R/W-0x0							R/W-0x1

表 6-101. JSYNC_N Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R/W	0x0	Must write default value.
0	JSYNC_N	R/W	0x1	Set this bit to 0 to request JESD204C synchronization (equivalent to the SYNC~ signal being asserted). For normal operation, leave this bit set to 1. Note: The JSYNC_N register can always generate a synchronization request, regardless of the SYNC_SEL register. However, if the selected sync pin is stuck low, you cannot de-assert the synchronization request unless you program SYNC_SEL=2.

6.5.7.45 JCTRL Register (Address = 0x204) [reset = 0x03]

JCTRL is shown in 図 6-64 and described in 表 6-102.

Return to the Summary Table.

JESD204C Control (default: 0x03)

図 6-64. JCTRL Register

7	6	5	4	3	2	1	0
RESERVED			ALT_LANES	SYNC_SEL		SFORMAT	SCR
R/W-0x0			R/W-0x0	R/W-0x0		R/W-0x1	R/W-0x1

表 6-102. JCTRL Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.

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表 6-102. JCTRL Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	ALT_LANES	R/W	0x0	0 : Normal lane mapping (default) as shown in the JESD204C output mode section. Lanes 0 thru L-1 are used. 1 : Alternate lane mapping (use upper lanes). Lanes 4 to 4+L-1 are used. Lanes 0 to 3 are unused. This option is only supported when JMODE selects a mode that uses 4 or less lanes per link (L<=4). The behavior is undefined for modes that use more than 4 lanes.
3:2	SYNC_SEL	R/W	0x0	0 : Use the SYNCSE input for SYNC~ function (default) 1 : Use the TMSTP± input for SYNC~ function. TMSTP_RECV_EN must also be set. 2 : Do not use any SYNC~ input pin (use JSYNC_N as a software SYNC~)
1	SFORMAT	R/W	0x1	Output sample format for JESD204C samples 0 : Offset binary 1 : Signed 2's complement (default)
0	SCR	R/W	0x1	0 : 8B/10B Scrambler disabled (applies only to 8B/10B modes) 1 : 8B/10B Scrambler enabled (default) Note 1: The 8b/10b scrambler is recommended to improve spurious noise and specify certain sample payloads cannot prevent the JESD204C receiver from detecting incorrect code-group or lane alignment. 64B/66B modes always use scrambling. This register does not apply to 64B/66B modes. Note: This register should only be changed when JESD_EN is 0.

6.5.7.46 JTEST Register (Address = 0x205) [reset = 0x00]

JTEST is shown in 図 6-65 and described in 表 6-103.

Return to the Summary Table.

JESD204C Test Control (default: 0x00)

図 6-65. JTEST Register

7	6	5	4	3	2	1	0
RESERVED			JTEST				
R/W-0x0			R/W-0x0				

表 6-103. JTEST Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.

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表 6-103. JTEST Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4:0	JTEST	R/W	0x0	0 : Test mode disabled. Normal operation (default) 1 : PRBS7 test mode 2 : PRBS15 test mode 3 : PRBS23 test mode 4 : Ramp test mode 5 : Transport Layer test mode 6 : D21.5 test mode 7 : K28.5 test mode* 8 : Repeated ILA test mode* 9 : Modified RPAT test mode* 10: Serial outputs held low 11: Serial outputs held high 12: RESERVED 13: PRBS9 test mode 14: PRBS31 test mode 15: Clock test pattern (0x00FF) 16: K28.7 test mode* 17-31: RESERVED * These test modes are only supported when JMODE is selecting a mode that utilizes 8B/10B encoding. Note: This register should only be changed when JESD_EN is 0.

6.5.7.47 DID Register (Address = 0x206) [reset = 0x00]

DID is shown in 図 6-66 and described in 表 6-104.

Return to the Summary Table.

JESD204C DID Parameter (default: 0x00)

図 6-66. DID Register

7	6	5	4	3	2	1	0
DID							
R/W-0x0							

表 6-104. DID Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	DID	R/W	0x0	Specifies the DID (Device ID) value that is transmitted during the second multiframe of the JESD204B ILA. Note: This register should only be changed when JESD_EN is 0.

6.5.7.48 FCHAR Register (Address = 0x207) [reset = 0x00]

FCHAR is shown in 図 6-67 and described in 表 6-105.

Return to the Summary Table.

JESD204C Frame Character (default: 0x00)

図 6-67. FCHAR Register

7	6	5	4	3	2	1	0
RESERVED						FCHAR	
R/W-0x0						R/W-0x0	

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表 6-105. FCHAR Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0x0	Must write default value.
1:0	FCHAR	R/W	0x0	Specify which comma character is used to denote end-of-frame. This character is transmitted opportunistically. This only applies to modes that utilize 8B/10B encoding. 0 : Use K28.7 (default) (JESD204C compliant) 1 : Use K28.1 (not JESD204C compliant) 2 : Use K28.5 (not JESD204C compliant) 3 : Reserved When using a JESD204C receiver, always use FCHAR=0. When using a general purpose 8B/10B receiver, the K28.7 character may cause issues. When K28.7 is combined with certain data characters, a false, misaligned comma character can result, and some receivers will re-align to the false comma. To avoid this, program FCHAR to 1 or 2. Note: This register should only be changed when JESD_EN is 0.

6.5.7.49 JESD_STATUS Register (Address = 0x208) [reset = 0x0]

JESD_STATUS is shown in 図 6-68 and described in 表 6-106.

Return to the Summary Table.

JESD204C / System Status Register

図 6-68. JESD_STATUS Register

7	6	5	4	3	2	1	0
RESERVED	LINK_UP	SYNC_STATUS	REALIGNED	ALIGNED	SPLL_LOCKED	RESERVED	CPLL_LOCKED
R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0	R/W-0x0

表 6-106. JESD_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0x0	
6	LINK_UP	R/W	0x0	When set, indicates that the JESD204C link is up.
5	SYNC_STATUS	R/W	0x0	Returns the state of the JESD204C SYNC~ signal. 0 : SYNC~ asserted 1 : SYNC~ de-asserted
4	REALIGNED	R/W	0x0	When high, indicates that the digital block clock, frame clock, or multiframe clock phase was realigned by SYSREF. Writing a 1 to this bit will clear it.
3	ALIGNED	R/W	0x0	When high, indicates that the multiframe (LMFC) clock phase has been established by SYSREF. The first SYSREF event after enabling the JESD204B encoder will set this bit. Writing a 1 to this bit will clear it.
2	SPLL_LOCKED	R/W	0x0	When high, indicates that the SerDes PLL (S-PLL) is locked.
1	RESERVED	R/W	0x0	
0	CPLL_LOCKED	R/W	0x0	When high, indicates that the converter PLL (C-PLL) is locked.

6.5.7.50 CH_EN Register (Address = 0x209) [reset = 0x03]

CH_EN is shown in 図 6-69 and described in 表 6-107.

Return to the Summary Table.

JESD204C Channel Enable (default: 0x03)

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図 6-69. CH_EN Register

7	6	5	4	3	2	1	0
RESERVED					SINGLE_CH_EN	CD_EN	AB_EN
R/W-0x0					R/W-0x0	R/W-0x1	R/W-0x1

表 6-107. CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7:3	RESERVED	R/W	0x0	Must write default value.
2	SINGLE_CH_EN	R/W	0x0	When set, single channel mode is enabled and channels B, C and D are disabled. AB_EN must be set to 1.
1	CD_EN	R/W	0x1	When set, the C and D channels are enabled. Set to 0 to disable channels C and D. Set this bit to enable dual channel operation.
0	AB_EN	R/W	0x1	When set, the A and B channels are enabled. Set to 0 to disable channel A and B. Important notes: 1. You must set CAL_EN=0 and JESD_EN=0 before changing CH_EN. 2. Do not use this register to disable (power down) all channels since this state is undefined. Instead use the MODE register to power down the full device. 3. When either pair of channels is disabled, the JESD204C link will scale down the number of lanes and converters: L = ceiling(Lx/2) and M = Mx/2. If Lx is odd, tail bits are added to the end of the highest lane to pad out the frame (as per the JESD204C standard). 4. When AB_EN=0, the samples for channels C & D are placed within the JESD204C frame where the A & B samples would normally be located.

6.5.7.51 SHMODE Register (Address = 0x20F) [reset = 0x00]

SHMODE is shown in 図 6-70 and described in 表 6-108.

Return to the Summary Table.

JESD204C Sync Word Mode (default: 0x00)

図 6-70. SHMODE Register

7	6	5	4	3	2	1	0
RESERVED						SHMODE	
R/W-0x0						R/W-0x0	

表 6-108. SHMODE Register Field Descriptions

Bit	Field	Type	Reset	Description
7:2	RESERVED	R/W	0x0	Must write default value.
1:0	SHMODE	R/W	0x0	Select the mode for the 64B/66B sync word (32 bits of data per multi-block). This only applies when JMODE is selecting a 64B/66B mode. 0 : Transmit CRC-12 signal (default setting) 1 : RESERVED 2 : Transmit FEC signal 3 : RESERVED Note: This device does not support any JESD204C command features. All command fields will be set to zero (idle headers). Note: This register should only be changed when JESD_EN is 0.

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6.5.7.52 SYNC_THRESH Register (Address = 0x210) [reset = 0x03]

SYNC_THRESH is shown in 図 6-71 and described in 表 6-109.

Return to the Summary Table.

JESD204C SYNC~ Threshold (default: 0x03)

図 6-71. SYNC_THRESH Register

7	6	5	4	3	2	1	0
RESERVED			SYNC_THRESH				
R/W-0x0			R/W-0x3				

表 6-109. SYNC_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.
4:0	SYNC_THRESH	R/W	0x3	This register defines how many times the SYNC~ signal must be sampled low before the JESD204C transmitter interprets it as a synchronization request. The SYNC~ signal is sampled by the link clock (fS/2). If SYNC~ is sampled low for SYNC_THRESH+1 consecutive clock cycles, it will be interpreted as a synchronization request. Refer to JESD204C section 8.8.2 for more details. If SYNC~ is sampled low for less than SYNC_THRESH+1 clock cycles, it is considered to be an error report and is ignored. Note: This register should only be changed when JESD_EN is 0. Note: Since this design does not do anything with an error reported on the SYNC~ interface, it is recommended that error reporting be disabled on the receiver and SYNC_THRESH programmed to 0. This provides the fastest response time for synchronization requests.

6.5.7.53 OVR_TH Register (Address = 0x211) [reset = 0xF2]

OVR_TH is shown in 図 6-72 and described in 表 6-110.

Return to the Summary Table.

Over-range Threshold (default: 0xF2)

図 6-72. OVR_TH Register

7	6	5	4	3	2	1	0
OVR_TH							
R/W-0xF2							

表 6-110. OVR_TH Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	OVR_TH	R/W	0xF2	This parameter defines the absolute sample level that causes the over-range outputs to be asserted. The detection level in dBFS (peak) is 20log10(OVR_TH/256) (Default: 0xF2 = 242-> -0.5dBFS)

6.5.7.54 OVR_CFG Register (Address = 0x213) [reset = 0x07]

OVR_CFG is shown in 図 6-73 and described in 表 6-111.

Return to the Summary Table.

Over-range Enable / Hold Off (default: 0x07)

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図 6-73. OVR_CFG Register

7	6	5	4	3	2	1	0
RESERVED				OVR_EN	OVR_N		
R/W-0x0				R/W-0x0	R/W-0x7		

表 6-111. OVR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7:4	RESERVED	R/W	0x0	Must write default value.
3	OVR_EN	R/W	0x0	Enables over-range status output pins when set high. The ORA, ORB, ORC and ORD outputs are held low when OVR_EN is set low.
2:0	OVR_N	R/W	0x7	Program this register to adjust the pulse extension for the ORA, ORB, ORC and ORD outputs. The minimum pulse duration of the over-range outputs is 4 * 2^{OVR_N} sampling cycles. Incrementing this field doubles the monitoring period.

6.5.7.55 INIT_STATUS Register (Address = 0x270) [reset = 0x0]

INIT_STATUS is shown in 図 6-74 and described in 表 6-112.

Return to the Summary Table.

Initialization Status (read-only)

図 6-74. INIT_STATUS Register

7	6	5	4	3	2	1	0
RESERVED							INIT_DONE
R-0x0							R-0x0

表 6-112. INIT_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	
0	INIT_DONE	R	0x0	Returns 1 when the initialization logic has finished initializing the device. This indicates that it is now safe to proceed with startup. No SPI transactions should be performed before INIT_DONE returns 1 (except SOFT_RESET).

6.5.7.56 LOW_POWER2 Register (Address = 0x29A) [reset = 0x0F]

LOW_POWER2 is shown in 図 6-75 and described in 表 6-113.

Return to the Summary Table.

Low Power Mode 2 (default: 0x0F)

図 6-75. LOW_POWER2 Register

7	6	5	4	3	2	1	0
LOW_POW_MODE2							
R/W-0xF							

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表 6-113. LOW_POWER2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	LOW_POW_MODE2	R/W	0xF	Set this register along with LOW_POWER1, LOW_POWER3 and LOW_POWER4 to enable Low Power Mode. All registers must be set together. Calibration must be performed after changing the operating mode: 0x06 : Low Power Mode (only valid when sampling rate is less than or equal to 1 GSPS) 0x0F : High Performance Mode (default) All other values are RESERVED Note: Must set CAL_EN to 0 and JESD_EN to 0 before changing this register.

6.5.7.57 LOW_POWER3 Register (Address = 0x29B) [reset = 0x04]

LOW_POWER3 is shown in 図 6-76 and described in 表 6-114.

Return to the Summary Table.

Low Power Mode 3 (default: 0x04)

図 6-76. LOW_POWER3 Register

7	6	5	4	3	2	1	0
LOW_POW_MODE3							
R/W-0x4							

表 6-114. LOW_POWER3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	LOW_POW_MODE3	R/W	0x4	Set this register along with LOW_POWER1, LOW_POWER2 and LOW_POWER4 to enable Low Power Mode. All registers must be set together. Calibration must be performed after changing the operating mode: 0x00 : Low Power Mode (only valid when sampling rate is less than or equal to 1 GSPS) 0x04 : High Performance Mode (default) All other values are RESERVED Note: Must set CAL_EN to 0 and JESD_EN to 0 before changing this register.

6.5.7.58 LOW_POWER4 Register (Address = 0x29C) [reset = 0x1B]

LOW_POWER4 is shown in 図 6-77 and described in 表 6-115.

Return to the Summary Table.

Low Power Mode 4 (default: 0x1B)

図 6-77. LOW_POWER4 Register

7	6	5	4	3	2	1	0
LOW_POW_MODE4							
R/W-0x1B							

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表 6-115. LOW_POWER4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	LOW_POW_MODE4	R/W	0x1B	Set this register along with LOW_POWER1, LOW_POWER2 and LOW_POWER3 to enable Low Power Mode. All registers must be set together. Calibration must be performed after changing the operating mode: 0x14 : Low Power Mode (only valid when sampling rate is less than or equal to 1 GSPS) 0x1B : High Performance Mode (default) All other values are RESERVED Note: Must set CAL_EN to 0 and JESD_EN to 0 before changing this register.

6.5.7.59 ALARM Register (Address = 0x2C0) [reset = 0x0]

ALARM is shown in 図 6-78 and described in 表 6-116.

Return to the Summary Table.

Alarm Interrupt (read-only)

図 6-78. ALARM Register

7	6	5	4	3	2	1	0
RESERVED							ALARM
R-0x0							R-0x0

表 6-116. ALARM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:1	RESERVED	R	0x0	
0	ALARM	R	0x0	This bit returns a '1' whenever any alarm occurs that is unmasked in the ALM_STATUS register. Use ALM_MASK to mask (disable) individual alarms. CAL_STATUS_SEL can be used to drive the ALARM bit onto the CALSTAT output pin to provide a hardware alarm interrupt signal.

6.5.7.60 ALM_STATUS Register (Address = 0x2C1) [reset = 0x3F]

ALM_STATUS is shown in 図 6-79 and described in 表 6-117.

Return to the Summary Table.

Alarm Status (default: 0x3F, write to clear)

図 6-79. ALM_STATUS Register

7	6	5	4	3	2	1	0
RESERVED		FIFO_ALM	SPLL_ALM	LINK_ALM	REALIGNED_ALM	RESERVED	CLK_ALM
R/W-0x0		R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1

表 6-117. ALM_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	
5	FIFO_ALM	R/W	0x1	FIFO overflow/underflow alarm: This bit is set whenever an active JESD204C lane FIFO experiences an underflow or overflow condition. Write a '1' to clear this bit. To inspect which lane generated the alarm, read FIFO_LANE_ALM.

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表 6-117. ALM_STATUS Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	SPLL_ALM	R/W	0x1	S-PLL Lock Lost Alarm: This bit is set whenever the SerDes S-PLL is not locked. Write a '1' to clear this bit.
3	LINK_ALM	R/W	0x1	Link Alarm: This bit is set whenever the JESD204C link is enabled, but is not in the DATA_ENC state (8B/10B modes). In 64B/66B modes, there is no DATA_ENC state, so this alarm will fire when the link first starts up, and will also fire if any event causes a FIFO/ Serializer realignment. Write a '1' to clear this bit.
2	REALIGNED_ALM	R/W	0x1	Realigned Alarm: This bit is set whenever SYSREF causes the internal clocks (including the LMFC/LEMC) to be realigned. Write a '1' to clear this bit.
1	RESERVED	R/W	0x1	
0	CLK_ALM	R/W	0x1	Clock Alarm: This bit can be used to detect an upset to the internal digital block and JESD204C clocks. This bit is set whenever the internal clock dividers for the A and B channels do not match the C and D channels. Write a '1' to clear this bit. Refer to the alarm section for the proper usage of this register. Note: After power-on reset or soft-reset, all alarm bits are set to '1.' Note: When JESD_EN=0, all alarms (except CLK_ALM) are undefined. It is recommended that the user clears the alarms after setting JESD_EN=1.

6.5.7.61 ALM_MASK Register (Address = 0x2C2) [reset = 0x3F]

ALM_MASK is shown in 図 6-80 and described in 表 6-118.

Return to the Summary Table.

Alarm Mask Register (default: 0x3F)

図 6-80. ALM_MASK Register

7	6	5	4	3	2	1	0
RESERVED		MASK_FIFO_ALM	MASK_PLL_ALM	MASK_LINK_ALM	MASK_REALIGNED_ALM	RESERVED	MASK_CLK_ALM
R/W-0x0		R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1	R/W-0x1

表 6-118. ALM_MASK Register Field Descriptions

Bit	Field	Type	Reset	Description
7:6	RESERVED	R/W	0x0	Must write default value.
5	MASK_FIFO_ALM	R/W	0x1	When set, FIFO_ALM is masked and will not impact the ALARM register bit.
4	MASK_PLL_ALM	R/W	0x1	When set, PLL_ALM is masked and will not impact the ALARM register bit.
3	MASK_LINK_ALM	R/W	0x1	When set, LINK_ALM is masked and will not impact the ALARM register bit.
2	MASK_REALIGNED_ALM	R/W	0x1	When set, REALIGNED_ALM is masked and will not impact the ALARM register bit.
1	RESERVED	R/W	0x1	Must write default value.
0	MASK_CLK_ALM	R/W	0x1	When set, CLK_ALM is masked and will not impact the ALARM register bit.

6.5.7.62 FIFO_LANE_ALM Register (Address = 0x2C4) [reset = 0xFF]

FIFO_LANE_ALM is shown in 図 6-81 and described in 表 6-119.

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Return to the Summary Table.

FIFO Overflow/Underflow Alarm (default: 0xFF)

図 6-81. FIFO_LANE_ALM Register

7	6	5	4	3	2	1	0
FIFO_LANE_ALM							
R/W-0xFF							

表 6-119. FIFO_LANE_ALM Register Field Descriptions

Bit	Field	Type	Reset	Description
7:0	FIFO_LANE_ALM	R/W	0xFF	FIFO_LANE_ALM[i] is set if the FIFO for lane i experiences overflow or underflow. Use this register to determine which lane(s) generated an alarm. Writing a '1' to any bit in this register will clear the alarm (the alarm may immediately trip again if the overflow/underflow condition persists). Writing a '1' to the FIFO_ALM register will clear all bits of this register.

6.5.7.63 OFS0 Register (Address = 0x330) [reset = 0x0]

OFS0 is shown in 図 6-82 and described in 表 6-120.

Return to the Summary Table.

Offset Adjustment for ADC0 (default from Fuse ROM)

図 6-82. OFS0 Register

15	14	13	12	11	10	9	8
RESERVED				OFS0			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
OFS0							
R/W-0x0							

表 6-120. OFS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	Must write default value.
11:0	OFS0	R/W	0x0	Offset adjustment value applied to ADC0. The format is unsigned. Important note: Do not access any OFS* registers if the calibration system is performing offset calibration. Case 1: If CAL_BGOS or CAL_BG is 0 and CAL_OS is 1, you may access OFS* registers after FG_DONE goes high. Case 2: If CAL_BG=1 and CAL_BGOS=1, you should not access the OFS* registers. For background calibration without continuous offset calibration, set CAL_OS to 1 and CAL_BG to 1, but keep CAL_BGOS set to 0. This will still calibrate the offset of the spare ADC cores during the foreground offset calibration step. Case 3: If none of the above conditions apply, you may access the OFS* registers without waiting.

6.5.7.64 OFS1 Register (Address = 0x332) [reset = 0x0]

OFS1 is shown in 図 6-83 and described in 表 6-121.

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Offset Adjustment for ADC1 (default from Fuse ROM)

図 6-83. OFS1 Register

15	14	13	12	11	10	9	8
RESERVED				OFS1			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
OFS1							
R/W-0x0							

表 6-121. OFS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	Must write default value.
11:0	OFS1	R/W	0x0	Offset adjustment value applied to ADC1.

6.5.7.65 OFS2A Register (Address = 0x334) [reset = 0x0]

OFS2A is shown in 図 6-84 and described in 表 6-122.

Return to the Summary Table.

Offset Adjustment for ADC2 (INA±) (default from Fuse ROM)

図 6-84. OFS2A Register

15	14	13	12	11	10	9	8
RESERVED				OFS2A			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
OFS2A							
R/W-0x0							

表 6-122. OFS2A Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	Must write default value.
11:0	OFS2A	R/W	0x0	Offset adjustment value applied to ADC2 when sampling INA±.

6.5.7.66 OFS2B Register (Address = 0x336) [reset = 0x0]

OFS2B is shown in 図 6-85 and described in 表 6-123.

Return to the Summary Table.

Offset Adjustment for ADC2 (INB±) (default from Fuse ROM)

図 6-85. OFS2B Register

15	14	13	12	11	10	9	8
RESERVED				OFS2B			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
OFS2B							

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図 6-85. OFS2B Register (続き)

R/W-0x0

表 6-123. OFS2B Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	Must write default value.
11:0	OFS2B	R/W	0x0	Offset adjustment value applied to ADC2 when sampling INB±.

6.5.7.67 OFS3C Register (Address = 0x338) [reset = 0x0]

OFS3C is shown in 図 6-86 and described in 表 6-124.

Return to the Summary Table.

Offset Adjustment for ADC3 (INC±) (default from Fuse ROM)

図 6-86. OFS3C Register

15	14	13	12	11	10	9	8
RESERVED				OFS3C			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
OFS3C							
R/W-0x0							

表 6-124. OFS3C Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	Must write default value.
11:0	OFS3C	R/W	0x0	Offset adjustment value applied to ADC3 when sampling INC±.

6.5.7.68 OFS3D Register (Address = 0x33A) [reset = 0x0]

OFS3D is shown in 図 6-87 and described in 表 6-125.

Return to the Summary Table.

Offset Adjustment for ADC3 (IND±) (default from Fuse ROM)

図 6-87. OFS3D Register

15	14	13	12	11	10	9	8
RESERVED				OFS3D			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
OFS3D							
R/W-0x0							

表 6-125. OFS3D Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	Must write default value.
11:0	OFS3D	R/W	0x0	Offset adjustment value applied to ADC3 when sampling IND±.

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6.5.7.69 OFS4 Register (Address = 0x33C) [reset = 0x0]

OFS4 is shown in 図 6-88 and described in 表 6-126.

Return to the Summary Table.

Offset Adjustment for ADC4 (default from Fuse ROM)

図 6-88. OFS4 Register

15	14	13	12	11	10	9	8
RESERVED				OFS4			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
OFS4							
R/W-0x0							

表 6-126. OFS4 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	Must write default value.
11:0	OFS4	R/W	0x0	Offset adjustment value applied to ADC4.

6.5.7.70 OFS5 Register (Address = 0x33E) [reset = 0x0]

OFS5 is shown in 図 6-89 and described in 表 6-127.

Return to the Summary Table.

Offset Adjustment for ADC5 (default from Fuse ROM)

図 6-89. OFS5 Register

15	14	13	12	11	10	9	8
RESERVED				OFS5			
R/W-0x0				R/W-0x0			
7	6	5	4	3	2	1	0
OFS5							
R/W-0x0							

表 6-127. OFS5 Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	RESERVED	R/W	0x0	Must write default value.
11:0	OFS5	R/W	0x0	Offset adjustment value applied to ADC5.

6.5.7.71 GAIN0 Register (Address = 0x360) [reset = 0x0]

GAIN0 is shown in 図 6-90 and described in 表 6-128.

Return to the Summary Table.

Fine Gain Adjust for ADC0 (default from Fuse ROM)

図 6-90. GAIN0 Register

7	6	5	4	3	2	1	0
RESERVED			GAIN0				

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図 6-90. GAIN0 Register (続き)

R/W-0x0	R/W-0x0

表 6-128. GAIN0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.
4:0	GAIN0	R/W	0x0	Fine gain adjustment for ADC0.

6.5.7.72 GAIN1 Register (Address = 0x361) [reset = 0x0]

GAIN1 is shown in 図 6-91 and described in 表 6-129.

Return to the Summary Table.

Fine Gain Adjust for ADC1 (default from Fuse ROM)

図 6-91. GAIN1 Register

7	6	5	4	3	2	1	0
RESERVED				GAIN1			
R/W-0x0				R/W-0x0			

表 6-129. GAIN1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.
4:0	GAIN1	R/W	0x0	Fine gain adjustment for ADC1.

6.5.7.73 GAIN2A Register (Address = 0x362) [reset = 0x0]

GAIN2A is shown in 図 6-92 and described in 表 6-130.

Return to the Summary Table.

Fine Gain Adjust for ADC2 (INA±) (default from Fuse ROM)

図 6-92. GAIN2A Register

7	6	5	4	3	2	1	0
RESERVED				GAIN2A			
R/W-0x0				R/W-0x0			

表 6-130. GAIN2A Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.
4:0	GAIN2A	R/W	0x0	Fine gain adjustment for ADC2 when sampling INA±.

6.5.7.74 GAIN2B Register (Address = 0x363) [reset = 0x0]

GAIN2B is shown in 図 6-93 and described in 表 6-131.

Return to the Summary Table.

Fine Gain Adjust for ADC2 (INB±) (default from Fuse ROM)

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図 6-93. GAIN2B Register

7	6	5	4	3	2	1	0
RESERVED				GAIN2B			
R/W-0x0				R/W-0x0			

表 6-131. GAIN2B Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.
4:0	GAIN2B	R/W	0x0	Fine gain adjustment for ADC2 when sampling INB±.

6.5.7.75 GAIN3C Register (Address = 0x364) [reset = 0x0]

GAIN3C is shown in 図 6-94 and described in 表 6-132.

Return to the Summary Table.

Fine Gain Adjust for ADC3 (INC±) (default from Fuse ROM)

図 6-94. GAIN3C Register

7	6	5	4	3	2	1	0
RESERVED				GAIN3C			
R/W-0x0				R/W-0x0			

表 6-132. GAIN3C Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.
4:0	GAIN3C	R/W	0x0	Fine gain adjustment for ADC3 when sampling INC±.

6.5.7.76 GAIN3D Register (Address = 0x365) [reset = 0x0]

GAIN3D is shown in 図 6-95 and described in 表 6-133.

Return to the Summary Table.

Fine Gain Adjust for ADC3 (IND±) (default from Fuse ROM)

図 6-95. GAIN3D Register

7	6	5	4	3	2	1	0
RESERVED				GAIN3D			
R/W-0x0				R/W-0x0			

表 6-133. GAIN3D Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.
4:0	GAIN3D	R/W	0x0	Fine gain adjustment for ADC3 when sampling IND±.

6.5.7.77 GAIN4 Register (Address = 0x366) [reset = 0x0]

GAIN4 is shown in 図 6-96 and described in 表 6-134.

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Fine Gain Adjust for ADC4 (default from Fuse ROM)

図 6-96. GAIN4 Register

7	6	5	4	3	2	1	0
RESERVED			GAIN4				
R/W-0x0			R/W-0x0				

表 6-134. GAIN4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.
4:0	GAIN4	R/W	0x0	Fine gain adjustment for ADC4.

6.5.7.78 GAIN5 Register (Address = 0x367) [reset = 0x0]

GAIN5 is shown in 図 6-97 and described in 表 6-135.

Return to the Summary Table.

Fine Gain Adjust for ADC5 (default from Fuse ROM)

図 6-97. GAIN5 Register

7	6	5	4	3	2	1	0
RESERVED			GAIN5				
R/W-0x0			R/W-0x0				

表 6-135. GAIN5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7:5	RESERVED	R/W	0x0	Must write default value.
4:0	GAIN5	R/W	0x0	Fine gain adjustment for ADC5.

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7 Application and Implementation

注

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7.1 Application Information

The ADC12QJ1600-Q1 can be used in a wide range of applications including light detection and ranging (LiDAR), RADAR, satellite communications, handheld test equipment (communications testers and oscilloscopes), and software-defined radios (SDR). The wide input bandwidth enables direct RF sampling to at least 4 GHz and the high sampling rate allows signal bandwidths of greater than 500 MHz. The *Typical Applications* section describes the use of the device in a LiDAR application using the integrated clocking features to reduce system cost, component count and solution size.

7.2 Typical Applications

7.2.1 Light Detection and Ranging (LiDAR) Digitizer

A LiDAR system uses a laser to send a light pulse toward a target and measures reflections off of the target using photodiodes. The photodiodes are connected to transimpedance amplifiers (TIA) to convert the current generated by the reflected light into a voltage. An ADC converts the voltage to a digital signal and extracts the pulse arrival time and reflected energy of the pulse. The device has a number of features that makes it ideal as the digitizer for a LiDAR system including high sampling rate, high performance, high input bandwidth and integrated clocking features. An example LiDAR system digitizer is shown in 図 7-1 which uses up to four ADC channels running at 1 GSPS and the on-chip clocking features of the device to reduce the component count, size and cost of the system.

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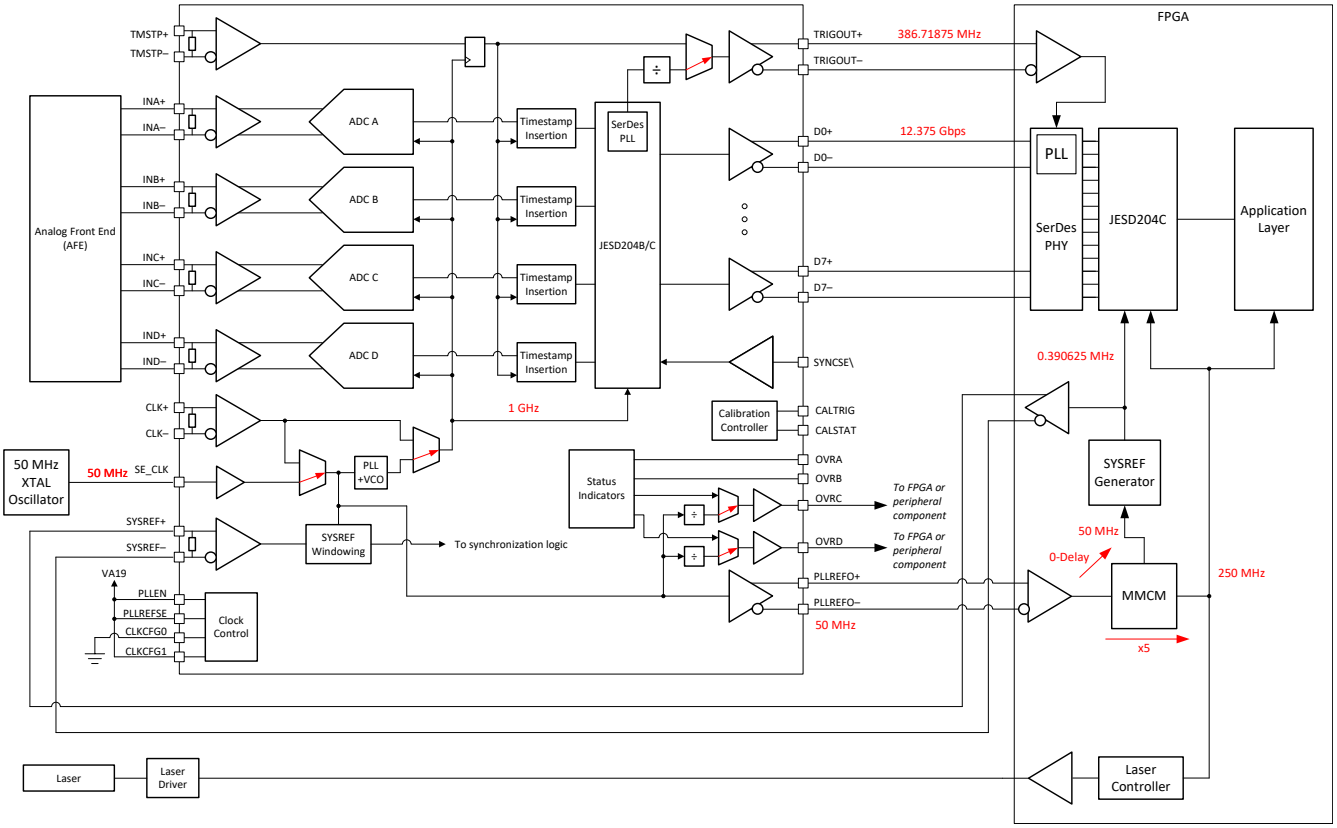

図 7-1. Typical Configuration for a LiDAR Digitizer

7.2.1.1 Design Requirements

An example list of LiDAR system requirements and the resulting digitizer requirements is given in 表 7-1. The example system requirements are for a mechanically rotating LiDAR system using a spinning mirror to cover the horizontal (azimuth) field-of-view and parallel receivers (photodiodes) to cover the vertical (elevation) field-of-view. The scan time requirement dictates that four vertical points are captured in parallel which requires four ADC channels and therefore a 16:1 photodiode to ADC mux ratio. The long 200 meter range for a 10% reflectivity target requires high performance and therefore a 12-bit ADC is chosen. The minimum pulse width of 5 ns, for high spatial resolution, requires a sampling rate of 1 GSPS in order to get 5 samples of each returning pulse. Low cost and small size are important to enable high volume production and a quad channel ADC with integrated clocking features help drive down these important metrics. Other considerations include the maximum SerDes rate supported by the FPGA and number of lanes. Assume the FPGA has 4 SerDes lanes that support up to 12.5 Gbps. For this reason, JMODE 8 is chosen.

表 7-1. LiDAR System and Digitizer Requirements

System Parameter	Example System Requirement	Example Digitizer Requirement
Maximum Target Range	200 meters at 10% reflectivity	12-bit ADC
Minimum Laser Pulse Width	5 ns	1 GSPS (5 samples per pulse)
Horizontal FOV	360°	See Full Scan Time
Vertical FOV	20°	See Vertical Scanning Method
Horizontal Resolution	0.1°	See Full Scan Time
Vertical Resolution	0.3125°	See Vertical Scanning Method
Horizontal Scanning Method	Spinning mirror	See Full Scan Time
Vertical Scanning Method	Parallel photodiodes	64 photodiodes
Full Scan Time	76.8 ms	16:1 mux ratio (4 ADC channels)

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表 7-1. LiDAR System and Digitizer Requirements (続き)

System Parameter	Example System Requirement	Example Digitizer Requirement
System Cost	Low cost	Clock features integrated in ADC
System Form Factor	Small form factor	Quad channel ADC with integrated clocking

7.2.1.2 Detailed Design Procedure

The details surrounding the LiDAR example design are provided in this section, including how to choose components and how to calculated the necessary clock frequencies.

7.2.1.2.1 Analog Front-End Requirements

The ADC channels are fed from an analog front end (AFE) which contains photodiodes, TIAs, fully-differential amplifiers (FDA) and analog muxes. The return pulse is collected by an optical lens which focuses the light to the corresponding photodiode. The photodiode generates a current which is converted to a voltage and amplified by a TIA. This single-ended voltage is converted to a differential voltage using a fully-differential amplifier which then drives the differential input of the ADC. The ADC common-mode voltage of 1.1V is easily interfaced to by unipolar supply FDAs for lowest cost. Analog muxing of parallel photodiode receivers can be done after the TIAs or after the FDAs depending on the chosen components.

The input network must have sufficient bandwidth to support the minimum pulse width required by the system. The required bandwidth to support a given rise time (10-90%) is given in Equation 13.

$$BW\ [MHz] = 350 / t_R[ns] \quad (13)$$

Assuming the laser has a rise and fall time of 1 ns (10-90%), then the input network bandwidth should be greater than 400 MHz to avoid excessive degradation of the pulse shape and spatial resolution.

7.2.1.2.2 Calculating Clock and SerDes Frequencies

The example LiDAR system uses four ADC channels running at 1 GSPS and the on-chip clock features of the device to reduce the system size and cost. The device is clocked by a 50-MHz crystal through the single-ended clock input (CLK_SE) and the integrated clock features are used to eliminate external clocking components. The internal PLL (C-PLL) generates the 1 GHz sampling clock for the ADC cores. The 50 MHz PLL reference is repeated through the PLLREFO output to the FPGA to generate the FPGA internal clocks including the application layer clock. The 50 MHz reference is divided down in the FPGA to generate the SYSREF signal which is sent to both the FPGA JESD204C core and to the device to achieve deterministic latency.

There are a number of clocking frequencies used in the example system shown in 図 7-1. The reference clock frequency (f_{REF}) is chosen by the designer and in this case is chosen as 50 MHz, which is the minimum supported reference frequency and which multiplies easily to 1 GHz. The sampling rate is set by the system requirements which is 1 GSPS (f_S). The V, P and N dividers of the C-PLL are chosen as described in the *Coverter PLL (C-PLL)* section which, along with the reference frequency, determines the VCO frequency (f_{VCO}). JMODE 8 was chosen to stay within the FPGA SerDes requirements (4 lanes, 12.5 Gbps max rate) which is a 64B/66B mode. TRIGOUT provides the FPGA SerDes PLL reference clock to the FPGA ($f_{TRIGOUT}$) and PLLREFO provides the reference clock for the FPGA core logic. ORC (f_{ORC}) and ORD (f_{ORD}) provide additional clock outputs, if needed, for the FPGA or peripheral devices. SYSREF is generated within the FPGA and sent to the ADC in order to achieve deterministic latency. This is not usually recommended due to timing constraints, however the low reference frequency (50 MHz) significantly relaxes the SYSREF setup and hold timing and the SYSREF Windowing feature allows verification of proper capture timing of SYSREF relative to the reference clock. The SYSREF frequency must divide evenly into the reference clock frequency, in addition to meeting the JESD204 protocol requirements, in order to achieve deterministic latency due to the use of the C-PLL. The frequency and rate calculations are summarized in 表 7-2.

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表 7-2. Clock and SerDes Frequency Calculations for Example LiDAR Digitizer

Clock	Symbol	Calculation	Frequency
Reference Clock	f_{REF}	Chosen by designer	50 MHz
Sampling Rate	f_S	System requirement	1 GSPS
C-PLL VCO	f_{VCO}	$f_{VCO} = f_S$x P x V where P is 2 and V is 4	8 GHz
SerDes Linerate	$f_{LINERATE}$	$f_{LINERATE} = f_S$x R where R is 12.375 for JMODE 8 (see 表 6-16, 表 6-17 and 表 6-18)	12.375 Gbps / Lane (4 lanes)
TRIGOUT Clock Output	$f_{TRIGOUT}$	$f_{TRIGOUT} = f_{LINERATE}$/ RX_DIV where RX_DIV is 32 (TRIGOUT_CTRL=0x81)	386.71875 MHz
SYSREF	f_{SYSREF}	$f_{SYSREF} = f_{LINERATE}$/(66 x 32 x E x n) where E is 3 for JMODE 8 (64B or 66B mode) and n is chosen such that f_{SYSREF} is an integer division of f_{REF} (n = 5)	390.625 kHz
ORC Clock Output	f_{ORC}	$f_{ORC} = f_{REF}$/2 (See 表 6-5)	25 MHz
ORD Clock Output	f_{ORD}	$f_{ORD} = f_{REF}$ (See 表 6-6)	50 MHz
FPGA Core Clock	f_{FPGA}	$f_{FPGA} = f_{REF}$ x M(1) (2) where M is an integer value, chosen as 5	250 MHz (4 samples per cycle)

(1) In the clock configuration shown, the FPGA clock which runs the JESD204C core must be an integer multiplication of f_{REF} in order to properly pass SYSREF from the reference clock domain to the core clock domain to achieve deterministic latency. In many cases the JESD204C IP may expect a clock rate of $f_{LINERATE}$/66, which results in 187.5 MHz for the example. Some JESD204C IP cores may not allow the JESD204C clock frequency to deviate from this requirement and therefore IP provider should be consulted. If the requirement described for the FPGA core clock cannot be met than deterministic latency cannot be achieved (operation without deterministic latency is still supported).

(2) If the application layer runs at a different clock rate than the JESD204C core, then some logic may be needed to pass data between clock domains while maintain timing information. Further, many JESD204C IP cores output 64 bits per clock cycle which may include fractions of a sample (such as in JMODE 8) and therefore gearbox logic may be needed to transition to the desired sample rate.

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7.2.1.3 Application Curves

An example pulse measurement using the device is shown in 図 7-2. The setup follows the example LiDAR system requirements with a 5-ns pulse captured at 1 GSPS . The applied pulse has a rise and fall time of approximately 1 ns. A sub-sampling technique is used to interpolate data points to form an equivalent 32 GSPS capture of the pulse for more accurate details and multiple capture averaging is used to suppress noise. A negative DC bias is applied to the ADC to enable use of the full dynamic range of the ADC for unipolar pulses. The pulse is spanning almost the full range of ADC codes. The extracted pulse parameters are given in 表 7-3. The analog front-end is not included in this measurement.

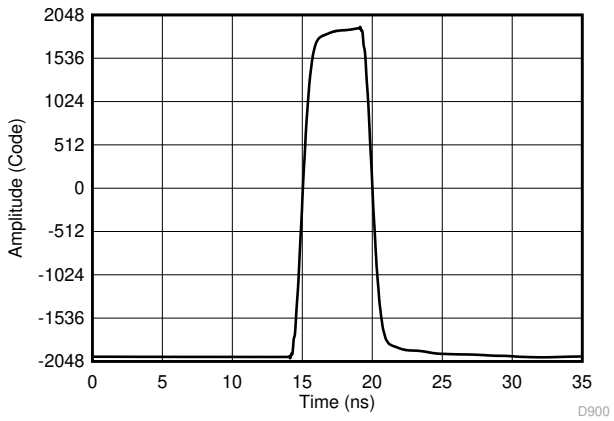

図 7-2. Measured Pulse using Sub-Sampling Technique for Equivalent 32 GSPS Measurement

表 7-3. Extracted Pulse Parameters for Example LiDAR System

Measured Parameter	Measured Value	Units
Rise Time (10-90%)	1.18	ns
Fall Time (90-10%)	1.19	ns
Pulse Width (50%)	4.99	ns
Equivalent Bandwidth(1)	295.3	MHz
Peak Amplitude (Codes)	3901	LSB
Peak Amplitude (Voltage)	750.5	mV
DC Offset (Codes)	-1994	LSB
DC Offset (Voltage)	-383.7	mV

(1) The equivalent bandwidth is calculated from the extracted rise time measurement. The bandwidth is limited by a 1-ns transition time converter used at the output of the pulse generator.

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7.3 Initialization Set Up

The device and JESD204 interface require a specific startup and alignment sequence. The general order of that sequence is listed in the following steps.

1. Tie PLL_EN high to enable the PLL or low to disable the PLL. Tie PLLREF_SE high to use the SE_CLK clock input (only valid if PLL_EN is high) or low to use CLK± clock input. Configure CLKCFG0 and CLKCFG1 pins to provide the required clocks from ORC and ORD outputs, if used.
2. Power-up the device and wait until voltages are within the recommended supply voltage range. The PD pin must be held low during power up and at all other times when PLLREFO, ORC or ORD clock outputs are necessary for system operation, if used.
3. Apply a stable clock signal at the desired frequency to CLK± or SE_CLK depending on the state of the PLLREF_SE input.
4. Reset the device using SOFT_RESET.
5. Verify device initialization is completed before continuing by reading INIT_DONE until a 1 is returned.
6. Program the C-PLL if the PLL is enabled (PLL_EN is set high). Skip to step 7 if the C-PLL is disabled (PLL_EN is set low).
   a. Program CPLL_RESET to 1 to reset the C-PLL.
   b. Program VCO_BIAS to 0x4A to set the C-PLL VCO bias settings.
   c. Program PLL_P_DIV, PLL_V_DIV and PLL_N_DIV to set the C-PLL dividers (see Converter PLL (C-PLL)).
   d. Program VCO_CAL_EN to 1 to enable VCO trim calibration or manually write the VCO trim to VCO_FREQ_TRIM (and set VCO_CAL_EN to 0). Skip to step 6.e. if manually loading VCO_FREQ_TRIM.
   e. Program CPLL_RESET to 0 to start VCO calibration and enable the C-PLL
7. Program JESD_EN = 0 to stop the JESD204C state machine and allow setting changes.
8. Program CAL_EN = 0 to stop the calibration state machine and allow setting changes.
9. Program Low Power Operating Mode, if desired, according to the *Low Power Mode and High Performance Mode* section.
10. Program the desired JMODE.
11. Program the desired KM1 value. KM1 = K–1. KM1 is only used if a JMODE is chosen that uses 8B/10B encoding.
12. Program SYNC_SEL as needed. Choose $\overline{\text{SYNCSE}}$ single-ended input or TMSTP± differential inputs.
13. Configure device calibration settings as desired (see the CAL_CFG0 and CAL_CFG1 registers). Select foreground or background calibration modes and offset calibration as needed.
14. Enable the TRIGOUT± clock output and configure the TRIGOUT output mode through the TRIGOUT_CTRL register, if desired.
15. If the C-PLL is used (PLL_EN is high) then verify that VCO calibration has finished (read VCO_CAL_DONE) and that the C-PLL is locked to the reference clock (read CPLL_LOCKED) before proceeding.
16. Program CAL_EN = 1 to enable the calibration state machine.
17. Enable over-range via OVR_EN and adjust settings if desired.
18. Program JESD_EN = 1 to re-start the JESD204C state machine and allow the link to restart.
19. Trigger a foreground calibration (if enabled) by setting CAL_SOFT_TRIG to 0 and then setting it back to 1. Alternatively, choose to use the CALTRIG pin by setting CAL_TRIG_EN to 1 and then toggling the CALTRIG pin low and then high. The CALSTAT pin and the FG_DONE register bit goes high to indicate that calibration has finished.
20. For JMODEs that use 8B/10B encoding the JESD204C interface now operates in response to the applied SYNC signal from the receiver (64B/66B does not use SYNC).
21. Data is valid when the JESD204C receiver finishes the initialization sequence (CGS and ILAS completes for 8B/10B modes or locks to SYNC header in 64B/66B modes) and the CALSTAT pin is high (if CAL_STATUS_SEL = 0) or FG_DONE is set to 1 to indicate that calibration is finished.

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7.4 Power Supply Recommendations

The device requires two different power-supply voltages. 1.9V DC is required for the VA19, VPLL19 and VREFO power buses and 1.1V DC is required for the VA11 and VD11 power buses. VTRIG can be set to either 1.1V or 1.9V and the TRIGOUT± common mode voltage shifts accordingly.

The power-supply voltages must be low noise and provide the needed current to achieve rated device performance. Certain supplies should be isolated from each other to prevent noise coupling into sensitive supplies. Isolation is best performed using separate regulators for each supply, but this is often not possible due to size and cost constraints. At a minimum a PI-type power supply filtering scheme should be used which includes a low-DC resistance ferrite bead (FB) with low-inductance decoupling capacitors on each side of the ferrite bead. These are demonstrated in the example power supply architectures drawings in 図 7-3 and 図 7-4.

There are two recommended power supply architectures:

1. Step down using high-efficiency switching converters, followed by a second stage of regulation to provide switching noise reduction and improved voltage accuracy as shown in 図 7-3.
2. Directly step down the final ADC supply voltage using high-efficiency switching converters as shown in 図 7-4. This approach provides the best efficiency, but care must be taken to minimize the switching noise preventing degraded ADC performance. In general, operate the DC/DC switching regulators in fixed-frequency mode at a high switching frequency to allow design of better power supply filtering networks and reduce low frequency noise that may not be able to be filtered.

The WEBENCH® Power Designer can be used to select and design the individual power supply elements as needed.

Recommended switching regulators include the TPS62290-Q1, TPS62812-Q1, TPS62065-Q1, TPS65268-Q1, and similar devices.

Recommended Low Drop-Out (LDO) linear regulators include the TPS74801-Q1, TPS7A88-Q1, TPS7A52-Q1 and similar devices.

For the switcher only approach, the ripple filter must be designed to provide sufficient filtering at the switching frequency of the DC-DC converter and harmonics of the switching frequency. Make a note of the switching frequency reported from WEBENCH® and design the EMI filter and capacitor combination to have the filter cutoff frequency set as needed. Each application has different tolerance for noise on the supply voltage and the impact to performance so strict ripple requirements are not provided. In general, the supply voltage must stay within the recommended operating conditions limits during all ripple and transient events. Any supply filtering must account for potential current transients, specifically when using low-power background calibration (see Low-Power Background Calibration (LPBG) Mode).

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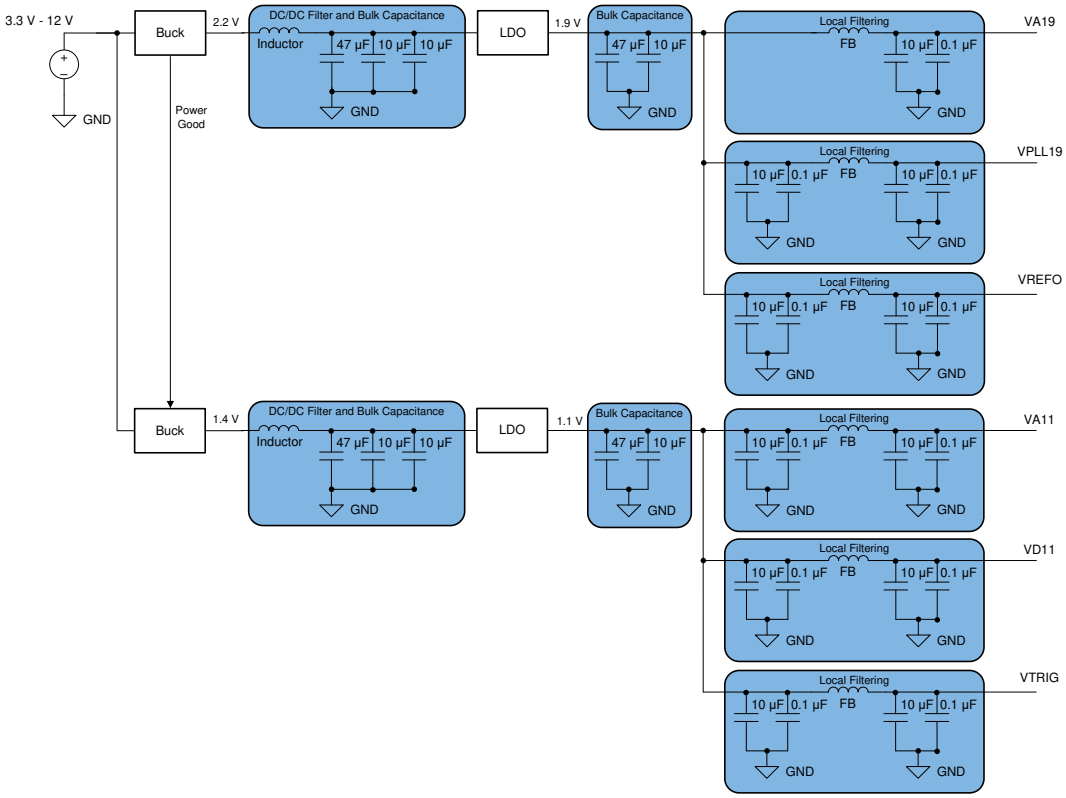
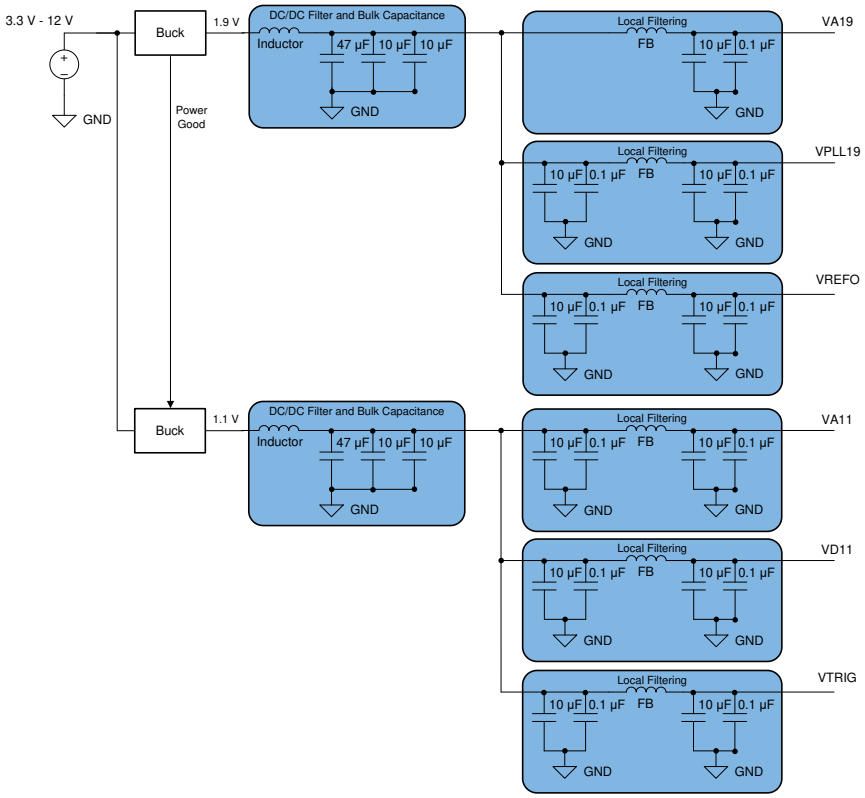


FB = ferrite bead filter.

図 7-3. LDO Linear Regulator Approach Example



FB = ferrite bead filter.

図 7-4. Switcher-Only Approach Example

7.4.1 Power Sequencing

The 1.1-V supplies (VA11, VD11) must not be more than 0.5 V above any of the 1.9-V supplies (VA19, VPLL19, VREFO) or VTRIG (1.1 V or 1.9 V) during power up, normal operation or power down. Further, all 1.9 V supplies should be within 0.5 V of each other at all times. VTRIG can be ramped with either the 1.9-V supplies or 1.1-V supplies, but must not be less than 0.5 V below VA11 or VD11 at any time. There is no sequencing requirement between VA11 and VD11.

The general recommendation is to have all 1.9-V supplies share a regulator. VTRIG is generally either 1.1 V or 1.9 V and should share a regulator with supplies of the same voltage. The sequencing requirement can then generally be met by tying the power good output of the 1.9-V regulator to the 1.1-V regulator(s). This specifies that the 1.1-V supplies are enabled after the 1.9-V supplies have come up (power is good) and that the 1.9-V supplies are always greater than the 1.1-V supplies on power up. During power down as soon as the 1.1-V supplies drop out of regulation then the 1.9-V supplies are disabled. The ramp rates must be designed such that the 1.9-V supplies never dip more than 0.5 V below the VA11 or VD11 supply.

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7.5 Layout

7.5.1 Layout Guidelines

There are many critical signals that require specific care during board design:

1. Analog input signals
2. CLK, SE_CLK and SYSREF
3. JESD204C data outputs
4. Power connections
5. Ground connections

The analog input signals, clock signals and JESD204C data outputs must be routed for excellent signal quality at high frequencies, but should also be routed for maximum isolation from each other. Use the following general practices:

1. Route using loosely coupled 100-Ω differential traces when possible. This routing minimizes impact of corners and length-matching serpentines on pair impedance. SE_CLK should be routed as a coplanar waveguide or as a stripline on an internal layer with sufficient via-fencing to prevent coupling.
2. Provide adequate pair-to-pair spacing to minimize crosstalk, especially with loosely coupled differential traces. Tightly coupled differential traces may be used to reduce self-radiated noise or to improve neighboring trace noise immunity when adequate spacing cannot be provided.
3. Provide adequate ground plane pour spacing to minimize coupling with the high-speed traces. Any ground plane pour must have sufficient via connections to the main ground plane of the board. Do not use floating or poorly connected ground pours.
4. Use smoothly radiused corners. Avoid 45- or 90-degree bends to reduce impedance mismatches.
5. Incorporate ground plane cutouts at component landing pads to avoid impedance discontinuities at these locations. Cut-out below the landing pads on one or multiple ground planes to achieve a pad size or stackup height that achieves the needed 50-Ω, single-ended impedance.
6. Avoid routing traces near irregularities in the reference ground planes. Irregularities include cuts in the ground plane or ground plane clearances associated with power and signal vias and through-hole component leads.
7. Provide symmetrically located ground tie vias adjacent to any high-speed signal vias at an appropriate spacing as determined by the maximum frequency the trace transports ($<< \lambda_{MIN}/8$).
8. When high-speed signals must transition to another layer using vias, transition as far through the board as possible (top to bottom is best case) to minimize via stubs on top or bottom of the vias. If layer selection is not flexible, use back-drilled or buried, blind vias to eliminate stubs. Always place ground vias close to the signal vias when transitioning between layers to provide a nearby ground return path.

Pay particular attention to potential coupling between JESD204C data output routing and the analog input routing. Switching noise from the JESD204C outputs can couple into the analog input traces and show up as wideband noise due to the high input bandwidth of the ADC. Ideally, route the JESD204C data outputs on a separate layer from the ADC input traces to avoid noise coupling (not shown in the *Layout Example* section). Tightly coupled traces can also be used to reduce noise coupling.

Impedance mismatch between the CLK± input pins and the clock source can result in reduced amplitude of the clock signal at the ADC CLK± pins due to signal reflections or standing waves. A reduction in the clock amplitude may degrade ADC noise performance, especially at high input frequencies. To avoid this, keep the clock source close to the ADC (as shown in the *Layout Example* section) or implement impedance matching at the ADC CLK± input pins.

In addition, TI recommends performing signal quality simulations of the critical signal traces before committing to fabrication. Insertion loss, return loss, and time domain reflectometry (TDR) evaluations should be done.

The power and ground connections for the device are also very important. These rules must be followed:

1. Provide low-resistance connection paths to all power and ground pins.
2. Use multiple power layers if necessary to access all pins.
3. Avoid narrow isolated paths that increase connection resistance.

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4. Use a signal-ground-power board stackup to maximum capacitance between the ground and power planes.

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7.5.2 Layout Example

図 7-5 to 図 7-7 provide examples of the critical traces routed on the device evaluation module (EVM).

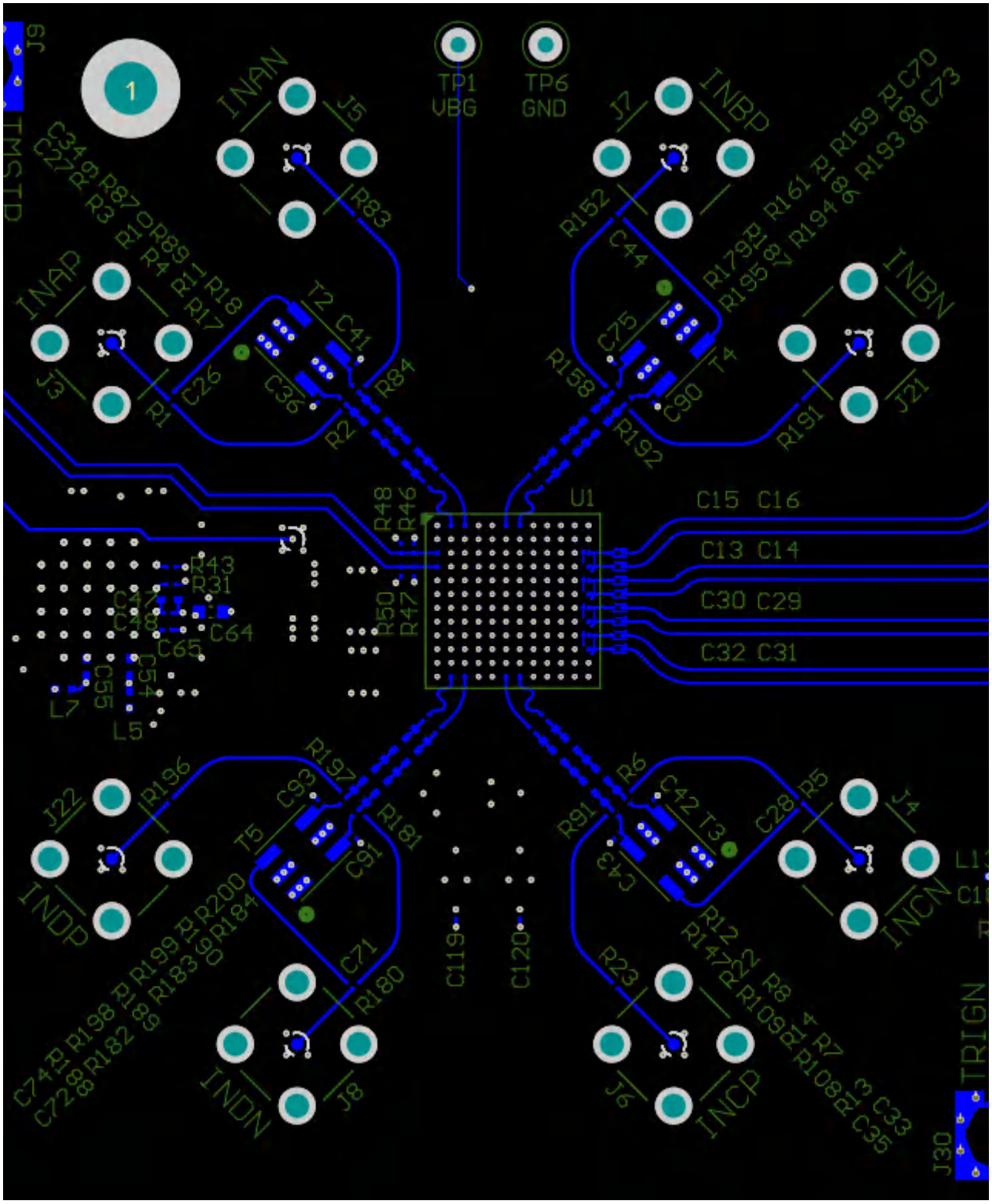

図 7-5. Top Layer Routing: Analog Inputs (INA±, INB±, INC±, IND±), TMSTP± and D[3:0]± Routing

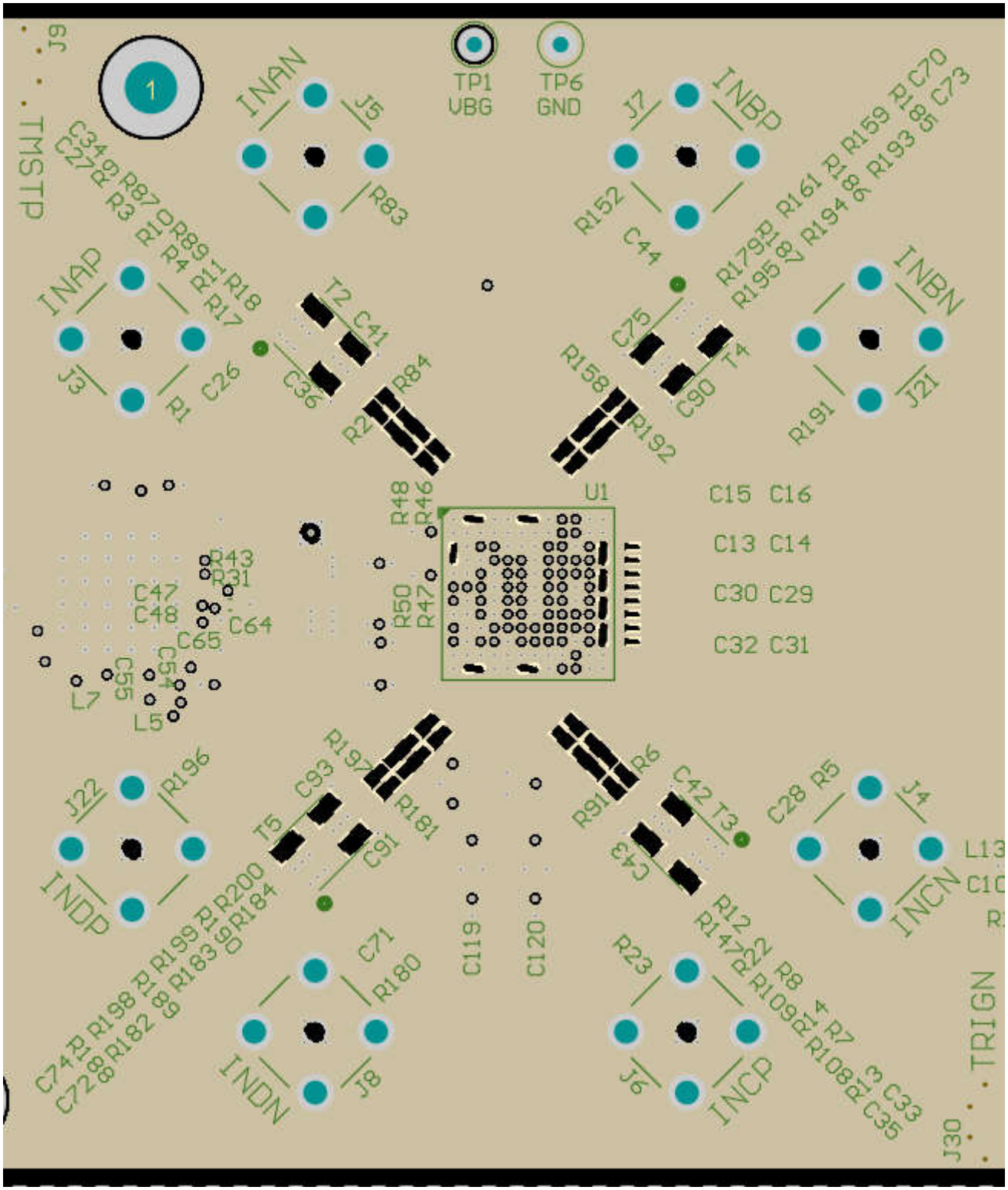

図 7-6. GND1 Cutouts to Optimize Impedance of Component Pads

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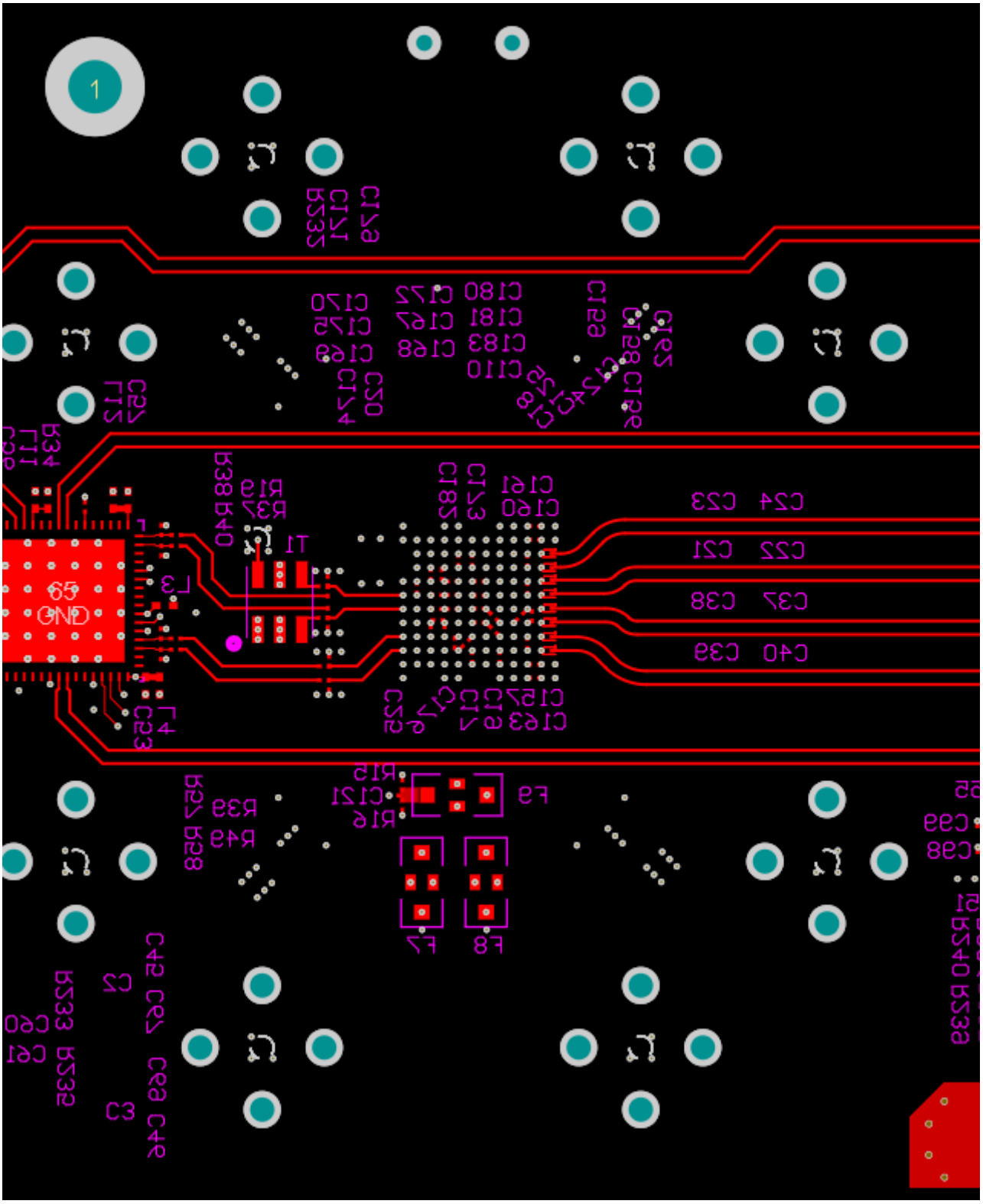

図 7-7. Bottom Layer Routing: CLK±, SYSREF and D[7:4]± Routing

8 Device and Documentation Support

8.1 Device Support

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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8.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from August 11, 2020 to October 17, 2024 (from Revision A (August 2020) to Revision B (October 2024)) **Page**

- 「製品情報」表を「パッケージ情報」表に変更 1
- Changed text from: Over-range for channel C to: *Over-range for channel D* in 表 6-6 62
- Changed the title of 表 6-16 76
- Changed the value for E in 表 6-16 for JMODEs 4 and 6 to 1 76
- Changed the value for E in 表 6-16 for JMODE 15 to 3 76
- Changed the title of 表 6-17 76
- Changed the value for E in 表 6-17 for JMODEs 4 and 6 to 1 76
- Changed the value for E in 表 6-17 for JMODE 15 to 3 76
- Changed the title for 表 6-18 76
- Changed the value for E in 表 6-18 for JMODEs 4 and 6 to 1 76
- Changed the value for E in 表 6-18 for JMODE 15 to 3 76

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Changes from Revision * (February 2020) to Revision A (August 2020) **Page**

- データシートにデバイス ADC12DJ1600-Q1 および ADC12SJ1600-Q1 を追加 1
- ADC12DJ1600-Q1 デバイスを「*事前情報*」から「*量産データ*」に変更 1
- Added //Operating free-air temperature// parameter to //Absolute Maximum Ratings// table 11

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC12DJ1600AAVQ1	Active	Production	FCCSP (AAV) | 144	168 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	ADC12DJ16 Q1
ADC12DJ1600AAVQ1.A	Active	Production	FCCSP (AAV) | 144	168 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	ADC12DJ16 Q1
ADC12DJ1600AAVTQ1	Active	Production	FCCSP (AAV) | 144	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	ADC12DJ16 Q1 YMZLLL9G1
ADC12DJ1600AAVTQ1.A	Active	Production	FCCSP (AAV) | 144	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	ADC12DJ16 Q1 YMZLLL9G1
ADC12QJ1600AAVQ1	Active	Production	FCCSP (AAV) | 144	168 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	ADC12QJ16 Q1
ADC12QJ1600AAVQ1.A	Active	Production	FCCSP (AAV) | 144	168 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	ADC12QJ16 Q1
ADC12QJ1600AAVTQ1	Active	Production	FCCSP (AAV) | 144	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	ADC12QJ16 Q1 YMZLLL9G1
ADC12QJ1600AAVTQ1.A	Active	Production	FCCSP (AAV) | 144	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	ADC12QJ16 Q1 YMZLLL9G1
ADC12SJ1600AAVQ1	Active	Production	FCCSP (AAV) | 144	168 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	ADC12SJ16 Q1
ADC12SJ1600AAVQ1.A	Active	Production	FCCSP (AAV) | 144	168 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	ADC12SJ16 Q1
ADC12SJ1600AAVTQ1	Active	Production	FCCSP (AAV) | 144	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	ADC12SJ16 Q1
ADC12SJ1600AAVTQ1.A	Active	Production	FCCSP (AAV) | 144	250 | SMALL T&R	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 125	ADC12SJ16 Q1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ADC12DJ1600-Q1, ADC12QJ1600-Q1, ADC12SJ1600-Q1 :

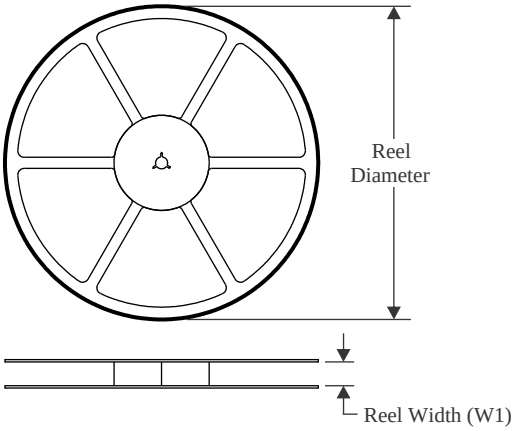
- Catalog : ADC12DJ1600, ADC12QJ1600, ADC12SJ1600
- Enhanced Product : ADC12QJ1600-EP
- Space : ADC12QJ1600-SP

NOTE: Qualified Version Definitions:

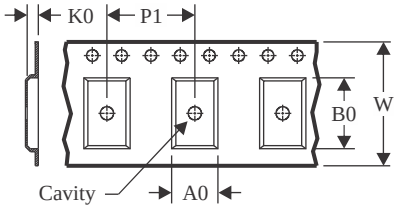
- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application

TAPE AND REEL INFORMATION

REEL DIMENSIONS

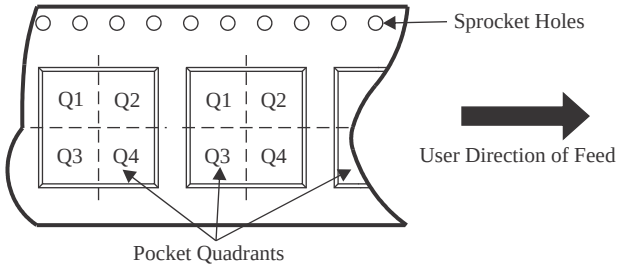


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

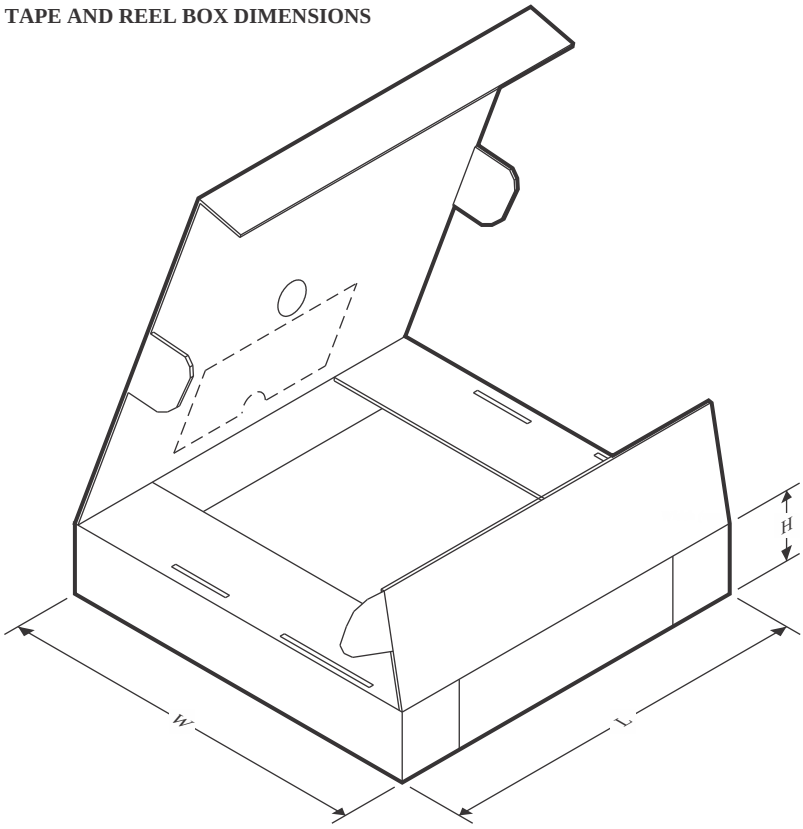
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC12DJ1600AAVTQ1	FCCSP	AAV	144	250	180.0	24.4	10.3	10.3	2.5	16.0	24.0	Q1
ADC12QJ1600AAVTQ1	FCCSP	AAV	144	250	180.0	24.4	10.3	10.3	2.5	16.0	24.0	Q1
ADC12SJ1600AAVTQ1	FCCSP	AAV	144	250	180.0	24.4	10.3	10.3	2.5	16.0	24.0	Q1

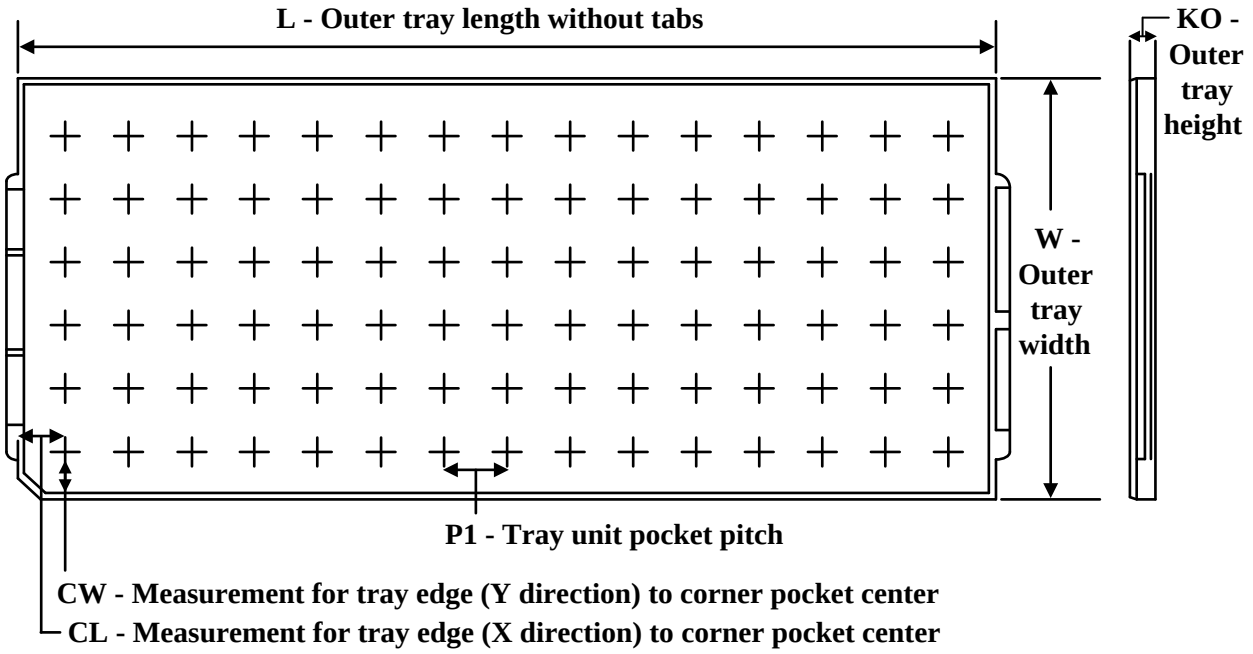
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC12DJ1600AAVTQ1	FCCSP	AAV	144	250	213.0	191.0	55.0
ADC12QJ1600AAVTQ1	FCCSP	AAV	144	250	213.0	191.0	55.0
ADC12SJ1600AAVTQ1	FCCSP	AAV	144	250	213.0	191.0	55.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

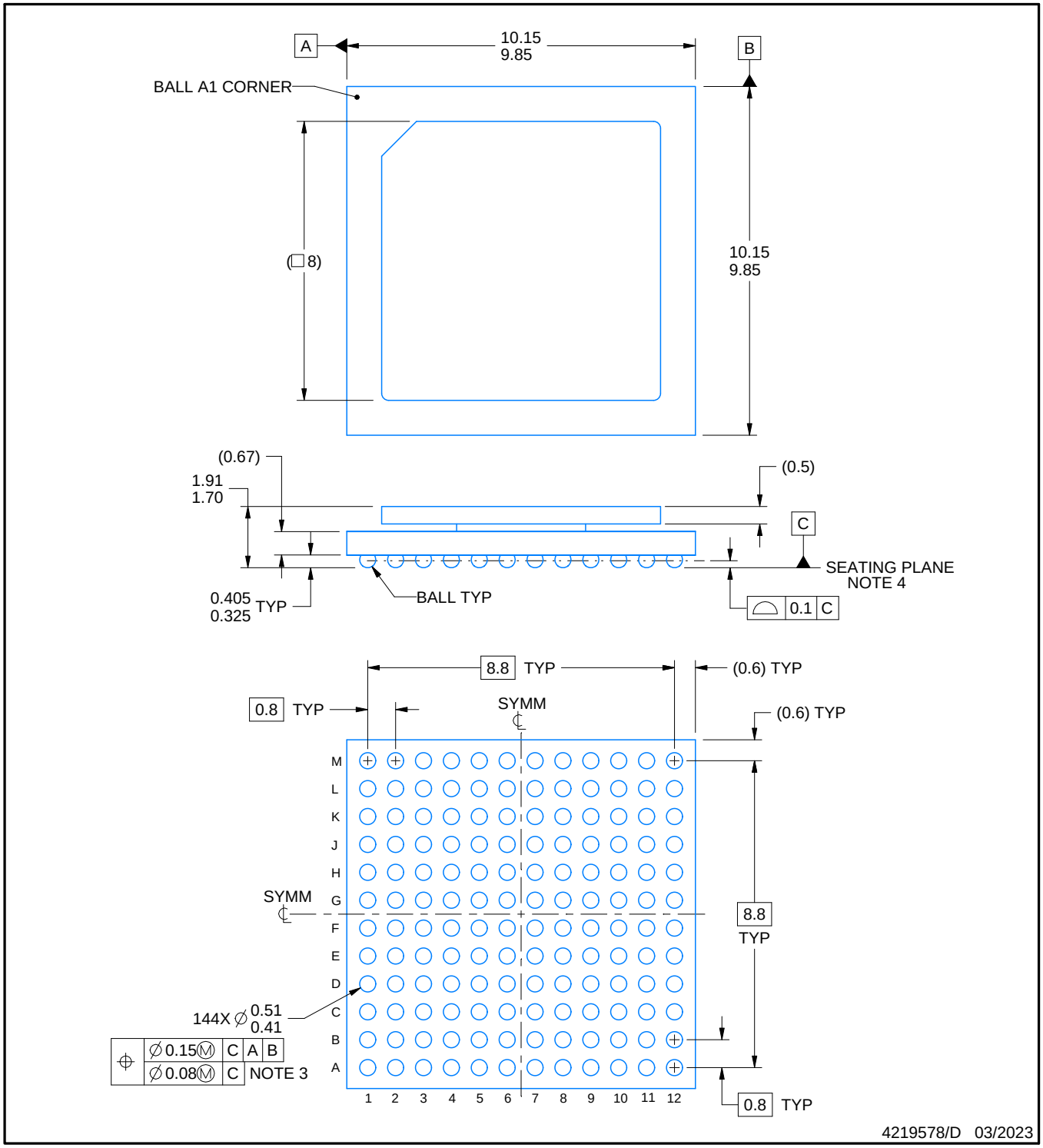
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
ADC12DJ1600AAVQ1	AAV	FCCSP	144	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
ADC12DJ1600AAVQ1.A	AAV	FCCSP	144	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
ADC12QJ1600AAVQ1	AAV	FCCSP	144	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
ADC12QJ1600AAVQ1.A	AAV	FCCSP	144	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
ADC12SJ1600AAVQ1	AAV	FCCSP	144	168	8 X 21	150	315	135.9	7620	14.65	11	11.95
ADC12SJ1600AAVQ1.A	AAV	FCCSP	144	168	8 X 21	150	315	135.9	7620	14.65	11	11.95

AAV0144A

PACKAGE OUTLINE

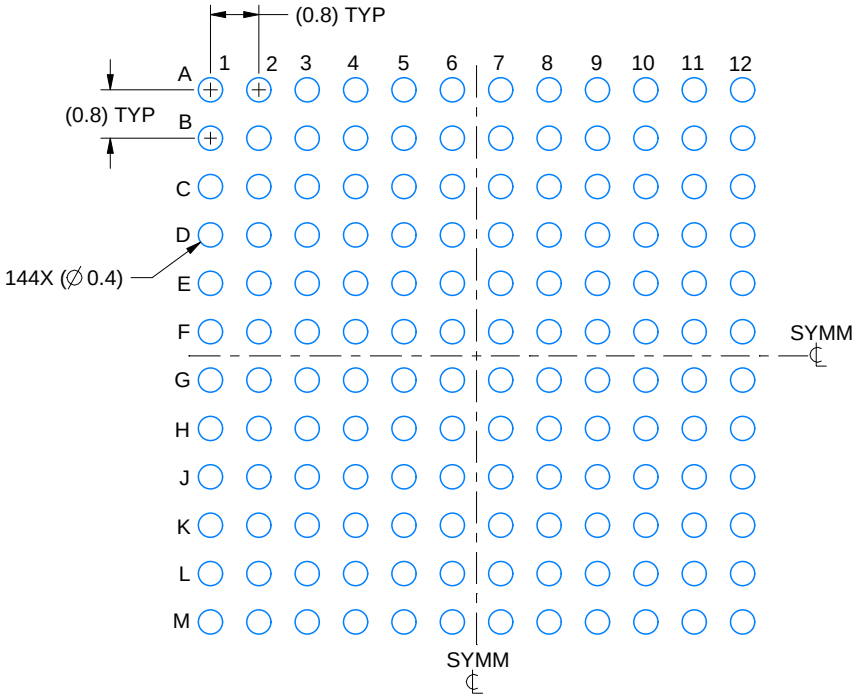
FCBGA - 1.91 mm max height

BALL GRID ARRAY

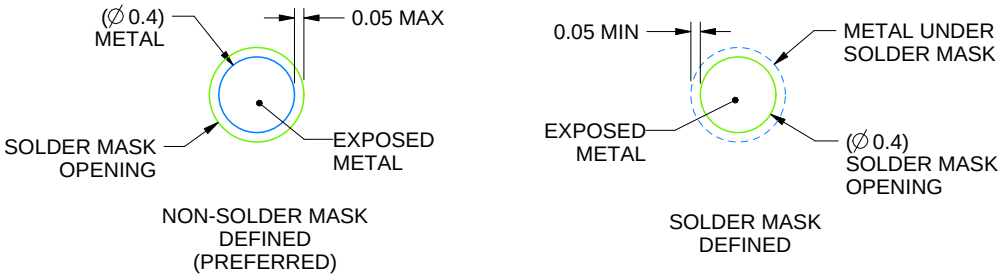


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

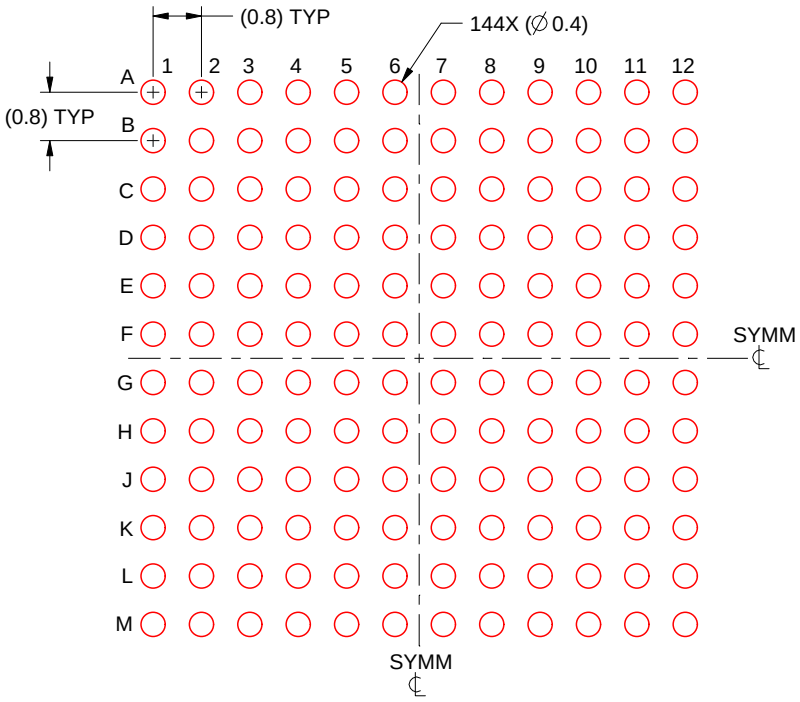


SOLDER MASK DETAILS
NOT TO SCALE

4219578/D 03/2023

NOTES: (continued)

6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

4219578/D 03/2023

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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