ADC084S021 4チャネル、50ksps～200ksps、8ビットA/Dコンバータ

1 特長

- サンプリング・レート範囲全体にわたって定格内
- 4つの入力チャネル
- 可変電力管理
- 2.7V～5.25Vの範囲の単一電源
- DNL: ±0.04LSB (標準値)
- INL: ±0.04LSB (標準値)
- SNR: 49.6dB (標準値)
- 消費電力:
  - 3V電源: 1.6mW (標準値)
  - 5V電源: 5.8mW (標準値)

2 アプリケーション

- ポータブル・システム
- リモート・データ収集
- 計測および制御システム

3 概要

ADC084S021デバイスは、低消費電力の4チャネルCMOS 8ビットA/Dコンバータで、高速のシリアル・インターフェイスが搭載されています。単一のサンプリング・レートのみでパフォーマンスを規定する従来の手法とは異なり、ADC084S021は50ksps～200kspsのサンプリング・レート範囲全体にわたって完全に規定されています。コンバータは逐次比較型のアーキテクチャをベースとし、内部的なトラック・アンド・ホールド回路を使用します。IN1からIN4までの入力を使用して、4つまでの入力信号を受け付けるように構成できます。

出力のシリアル・データはストレート・バイナリで、SPI™、QSPI™、MICROWIREなどいくつかの標準に加えて、多くの一般的なDPSシリアル・インターフェイスと互換性があります。

ADC084S021は2.7V～5.25Vの範囲の単一電源で動作します。3Vまたは5V電源を使用するときの通常の消費電力は、それぞれ 1.6mWおよび5.8mWです。パワー・ダウン機能により、消費電力は3V電源でわずか0.12µW、5V電源で0.35µWに低減されます。

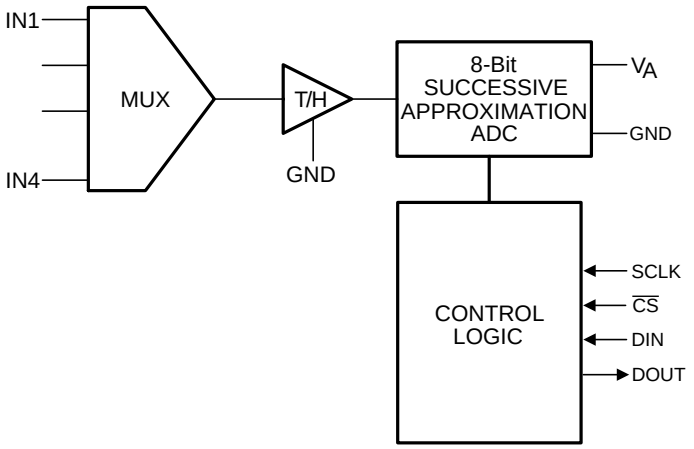
ADC084S021は10ピンのVSSOPパッケージで供給されます。工業用温度範囲の-40℃～85℃での動作が保証されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ADC084S021	VSSOP (10)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ブロック図



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision E (March 2013) から **Revision F** に変更 **Page**

- 「*ESD定格*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- Added Updated values in *Thermal Information* table ... 5

Revision D (March 2013) から **Revision E** に変更 **Page**

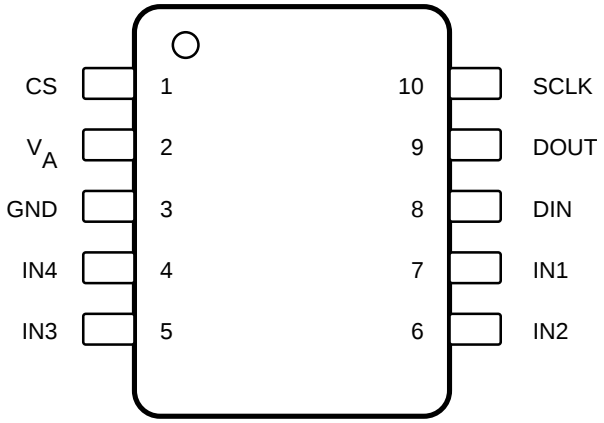
- ナショナル・セミコンダクターのデータシートのレイアウトをTIフォーマットへ 変更 ... 1

5 Device Comparison Table

RESOLUTION	SAMPLE RATE RANGE		
	50 TO 200 KSPS	200 TO 500 KSPS	500 KSPS TO 1 MSPS
12 Bit	ADC124S021	ADC124S051	ADC124S101
10 Bit	ADC104S021	ADC104S051	ADC104S101
8 Bit	*ADC084S021*	ADC084S051	ADC084S101

6 Pin Configuration and Functions

DGK Package
10-Pin VSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	$\overline{CS}$	I	Chip select. A conversion begins at the falling edge of $\overline{CS}$. Conversions continue as long as $\overline{CS}$ is held low.
2	V_A	—	Positive supply pin. This pin must be connected to a quiet 2.7-V to 5.25-V source and be bypassed to GND with a 0.1-µF monolithic capacitor located within 1 cm of the power pin and with a 1-µF capacitor.
3	GND	—	Device ground return for all signals.
4, 5, 6, 7	IN1 to IN4	I	Analog inputs. These signals can range from 0 V to V_A.
8	DIN	I	Digital data input. The ADC084S021's control register is loaded through this pin on rising edges of SCLK.
9	DOUT	O	Digital data output. The output samples are clocked out at this pin on falling edges of the SCLK pin.
10	SCLK	I	Digital clock input. This clock directly controls the conversion and readout processes.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
Supply voltage, V_A	–0.3	6.5	V
Voltage on any pin to GND	–0.3	V_A + 0.3	V
Input current at any pin(4)		±10	mA
Package input current(4)		±20	mA
Power consumption at T_A = 25°C	See (5)		
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = 0 V (unless otherwise specified).
(3) If Military/Aerospace specified devices are required, contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supply (that is, V_{IN} < GND or V_{IN} > V_A), the current at that pin must be limited to 10 mA. The 20-mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two. The *Absolute Maximum Ratings* does not apply to the V_A pin. The current into the V_A pin is limited by the analog supply voltage specification.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance ($R_{\theta JA}$), and the ambient temperature (T_A), and can be calculated using the formula P_DMAX = ($T_J$max − T_A) / $R_{\theta JA}$. The values for maximum power dissipation listed above is reached only when the device is operated in a severe fault condition (that is, when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions must always be avoided.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2500	V
		Machine model (MM)(3)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) Human-body model is 100-pF capacitor discharged through a 1.5-kΩ resistor.
(3) Machine model is 220-pF discharged through 0 Ω.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)(2)

		MIN	NOM	MAX	UNIT
V_A	Supply voltage	2.7		5.25	V
	Digital input voltage	–0.3		V_A	V
	Analog input voltage	0		V_A	V
	Clock frequency	0.8		3.2	MHz
T_A	Operating temperature	–40		85	°C

(1) *Recommended Operating Ratings* indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the *Electrical Characteristics*. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) All voltages are measured with respect to GND = 0 V (unless otherwise specified).

7.4 Thermal Information

THERMAL METRIC[1][2]		ADC084S021 DGK (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	190	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	90	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	88.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Reflow temperature profiles are different for lead-free and non-lead-free packages.

7.5 Electrical Characteristics

V_A = 2.7 V to 5.25 V, GND = 0 V, f_{SCLK} = 0.8 MHz to 3.2 MHz, f_{SAMPLE} = 50 ksps to 200 ksps, C_L = 50 pF, and T_A = 25°C (unless otherwise noted)[1]

PARAMETER		TEST CONDITIONS	MIN[2]	TYP	MAX[2]	UNIT
STATIC CONVERTER CHARACTERISTICS						
	Resolution with no missing codes				8	Bits
INL	Integral non-linearity			±0.04	±0.2	LSB
DNL	Differential non-linearity			±0.04	±0.2	LSB
V_{OFF}	Offset error			0.52	±0.7	LSB
OEM	Channel-to-channel offset error match			±0.01	±0.3	LSB
FSE	Full-scale error			0.51	±0.7	LSB
FSEM	Channel-to-channel full-scale error match			0.01	±0.3	LSB
DYNAMIC CONVERTER CHARACTERISTICS						
SINAD	Signal-to-noise plus distortion ratio	V_A = 2.7 V to 5.25 V f_{IN} = 39.9 kHz, –0.02 dBFS	49.1	49.6		dB
SNR	Signal-to-noise ratio	V_A = 2.7 V to 5.25 V f_{IN} = 39.9 kHz, –0.02 dBFS	49.2	49.6		dB
THD	Total harmonic distortion	V_A = 2.7 V to 5.25 V f_{IN} = 39.9 kHz, –0.02 dBFS		−76	−62	dB
SFDR	Spurious-free dynamic range	V_A = 2.7 V to 5.25 V f_{IN} = 39.9 kHz, −0.02 dBFS	63	68		dB
ENOB	Effective number of bits	V_A = 2.7 V to 5.25 V f_{IN} = 39.9 kHz, –0.02 dBFS		7.9		Bits
	Channel-to-channel crosstalk	V_A = 5.25 V f_{IN} = 39.9 kHz		−73		dB
IMD	Intermodulation distortion, second order terms	V_A = 5.25 V f_a = 40.161 kHz, f_b = 41.015 kHz		−78		dB
	Intermodulation distortion, third order terms	V_A = 5.25 V f_a = 40.161 kHz, f_b = 41.015 kHz		−73		
FPBW	Full power bandwidth, –3 dB	V_A = 5 V		11		MHz
		V_A = 3 V		8		
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Input range			0 to V_A		V
I_{DCL}	DC leakage current				±1	µA
C_{INA}	Input capacitance	Track mode		33		pF
		Hold mode		3		

(1) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).
(2) Minimum and maximum specification limits are specified by design, test, or statistical analysis.

Electrical Characteristics (continued)

V_A = 2.7 V to 5.25 V, GND = 0 V, f_{SCLK} = 0.8 MHz to 3.2 MHz, f_{SAMPLE} = 50 ksps to 200 ksps, C_L = 50 pF, and T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP	MAX(2)	UNIT
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input high voltage	V_A = 5.25 V	2.4			V
		V_A = 3.6 V	2.1			
V_{IL}	Input low voltage				0.8	V
I_{IN}	Input current	V_{IN} = 0 V or V_A			±10	µA
C_{IND}	Digital input capacitance			2	4	pF
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output high voltage	I_{SOURCE} = 200 µA	V_A – 0.5	V_A – 0.03		V
		I_{SOURCE} = 1 mA		V_A – 0.1		
V_{OL}	Output low voltage	I_{SINK} = 200 µA		0.03	0.4	V
		I_{SINK} = 1 mA		0.1		
I_{OZH}, I_{OZL}	TRI-STATE® leakage current				±1	µA
C_{OUT}	TRI-STATE® output capacitance			2	4	pF
	Output coding		Straight (natural) binary			
POWER SUPPLY CHARACTERISTICS (C_L = 10 pF)						
V_A	Supply voltage		2.7		5.25	V
I_A	Supply current, normal mode (operational, $\overline{CS}$ low)	V_A = 5.25 V, f_{SAMPLE} = 200 ksps, f_{IN} = 40 kHz		1.1	1.7	mA
		V_A = 3.6 V, f_{SAMPLE} = 200 ksps, f_{IN} = 40 kHz		0.45	0.8	
	Supply current, shutdown ($\overline{CS}$ high)	V_A = 5.25 V, f_{SAMPLE} = 0 ksps		200		nA
		V_A = 3.6 V, f_{SAMPLE} = 0 ksps		200		
P_D	Power consumption, normal mode (operational, $\overline{CS}$ low)	V_A = 5.25 V		5.8	8.9	mW
		V_A = 3.6 V		1.6	2.9	
	Power consumption, shutdown ($\overline{CS}$ high)	V_A = 5.25 V		1.05		µW
		V_A = 3.6 V		0.72		
AC ELECTRICAL CHARACTERISTICS						
f_{SCLK}	Clock frequency	(3)	0.8		3.2	MHz
f_S	Sample rate	(3)	50		200	ksps
t_{CONV}	Conversion time				13	SCLK cycles
DC	SCLK duty cycle	f_{SCLK} = 3.2 MHz	30%	50%	70%	
t_{ACQ}	Track or hold acquisition time	Full-scale step input			3	SCLK cycles
	Throughput time	Acquisition time + conversion time			16	SCLK cycles

(3) This is the frequency range over which the electrical performance is ensured. The device is functional over a wider range which is specified in *Recommended Operating Conditions*.

7.6 Timing Requirements

V_A = 2.7 V to 5.25 V, GND = 0 V, f_{SCLK} = 0.8 MHz to 3.2 MHz, f_{SAMPLE} = 50 ksps to 200 ksps, C_L = 50 pF, and T_A = 25°C (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		MIN	NOM	MAX	UNIT
t_{CSU}	Setup time SCLK high to $\overline{CS}$ falling edge(2)	V_A = 3 V		10			ns
		V_A = 5 V		10	–0.5		
t_{CLH}	Hold time SCLK low to $\overline{CS}$ falling edge(2)	V_A = 3 V		10	4.5		ns
		V_A = 5 V		10	1.5		
t_{EN}	Delay from $\overline{CS}$ until DOUT active	V_A = 3 V			4	30	ns
		V_A = 5 V			2	30	
t_{ACC}	Data access time after SCLK falling edge	V_A = 3 V			16.5	30	ns
		V_A = 5 V			15	30	
t_{SU}	Data setup time prior to SCLK rising edge			10	3		ns
t_H	Data valid SCLK hold time			10	3		ns
t_{CH}	SCLK high pulse width			0.3 × t_{SCLK}	0.5 × t_{SCLK}		ns
t_{CL}	SCLK low pulse width			0.3 × t_{SCLK}	0.5 × t_{SCLK}		ns
t_{DIS}	$\overline{CS}$ rising edge to DOUT high-impedance	Output falling	V_A = 3 V		1.7	20	ns
			V_A = 5 V		1.2	20	
		Output rising	V_A = 3 V		1	20	
			V_A = 5 V		1	20	

(1) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).
(2) Clock may be either high or low when $\overline{CS}$ is asserted as long as setup and hold times t_{CSU} and t_{CLH} are strictly observed.

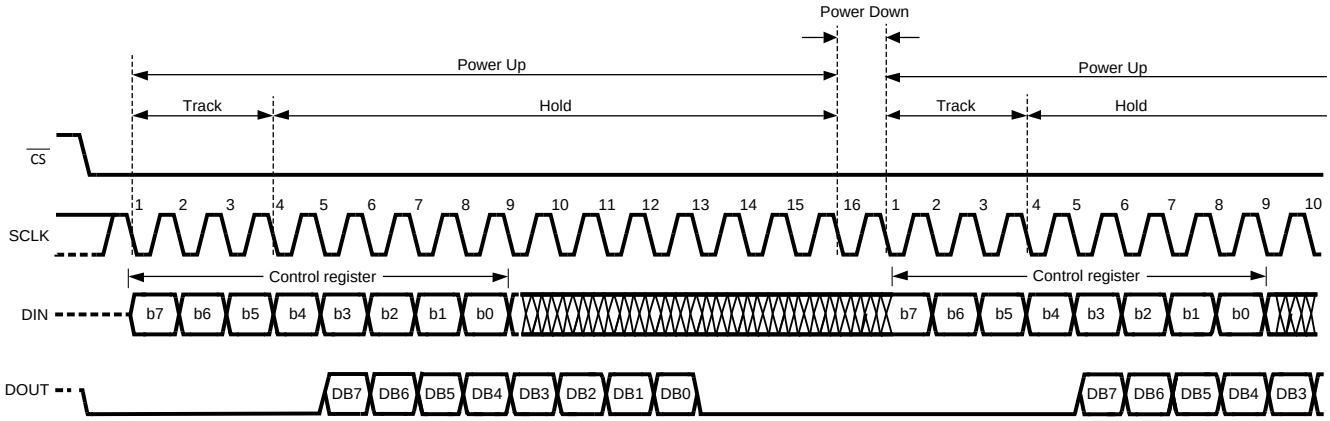


Figure 1. Operational Timing Diagram

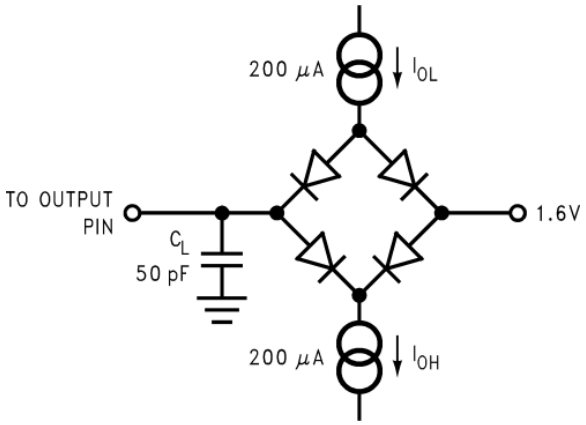


Figure 2. Timing Test Circuit

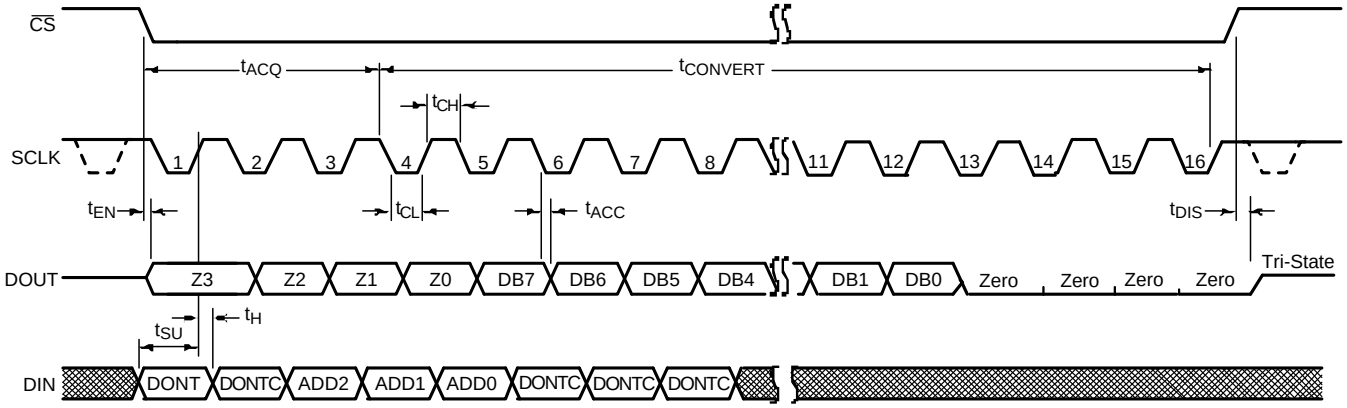


Figure 3. Serial Timing Diagram

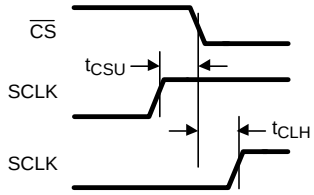


Figure 4. SCLK and $\overline{CS}$ Timing Parameters

7.7 Typical Characteristics

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

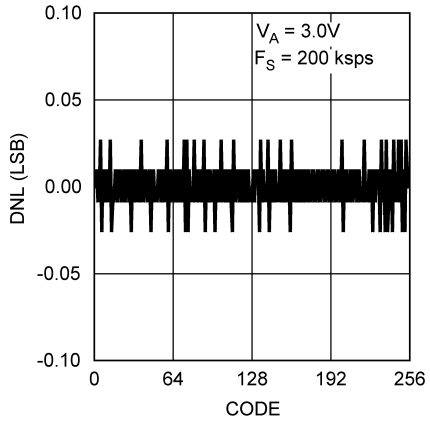


Figure 5. DNL – V_A = 3 V

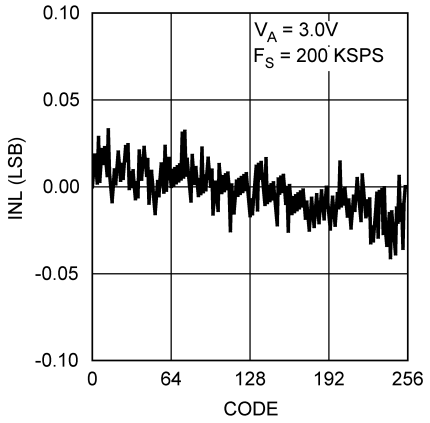


Figure 6. INL – V_A = 3 V

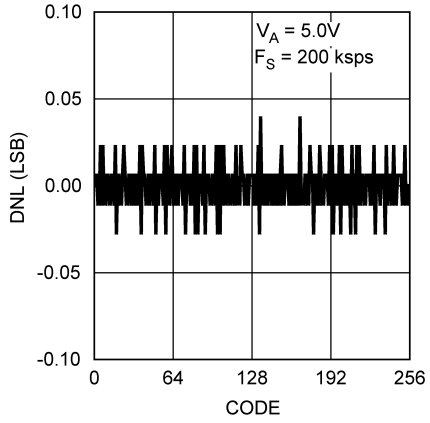


Figure 7. DNL – V_A = 5 V

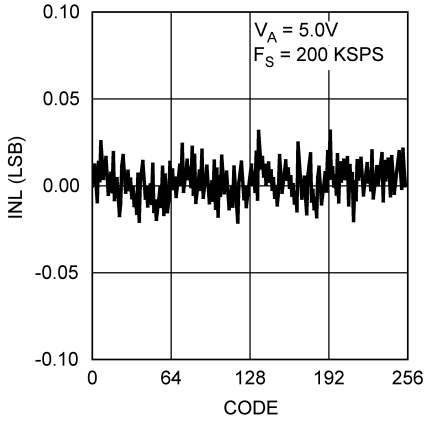


Figure 8. INL – V_A = 5 V

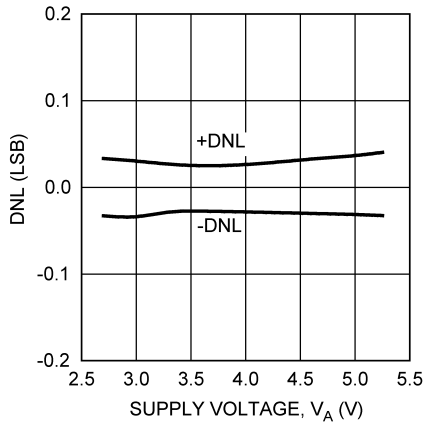


Figure 9. DNL vs Supply

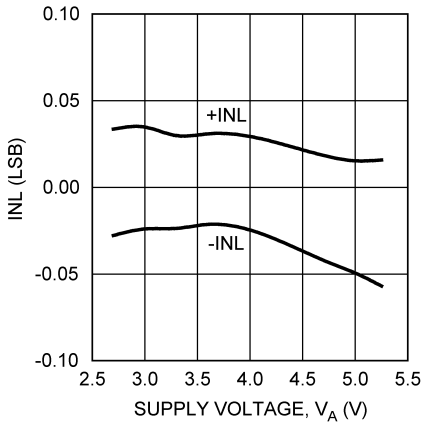


Figure 10. INL vs Supply

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

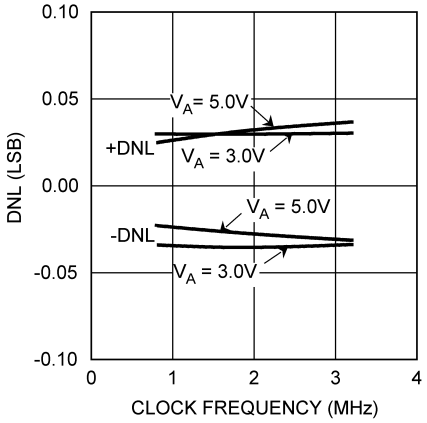


Figure 11. DNL vs Clock Frequency

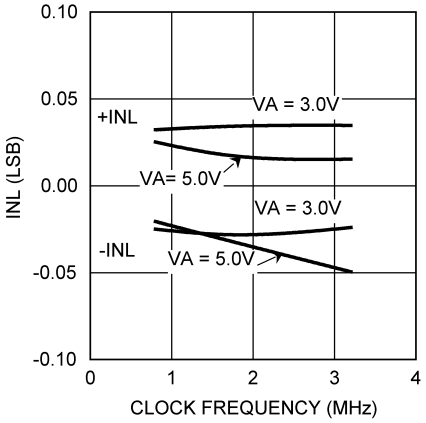


Figure 12. INL vs Clock Frequency

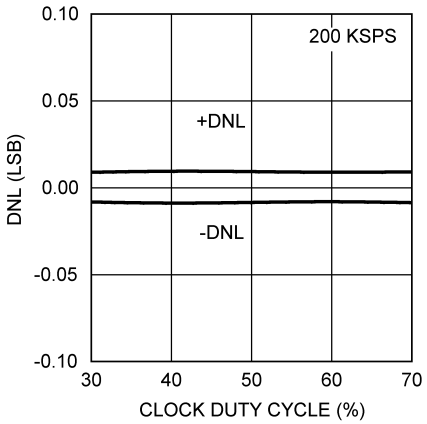


Figure 13. DNL vs Clock Duty Cycle

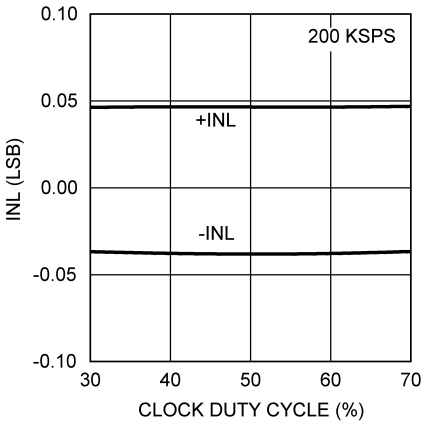


Figure 14. INL vs Clock Duty Cycle

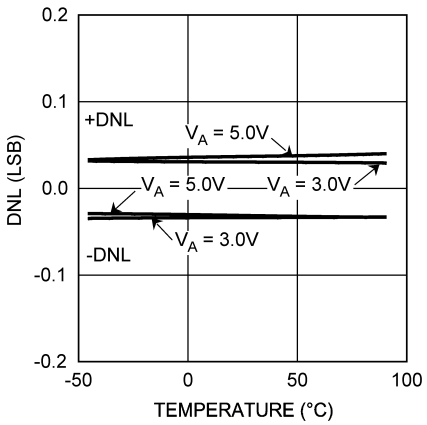


Figure 15. DNL vs Temperature

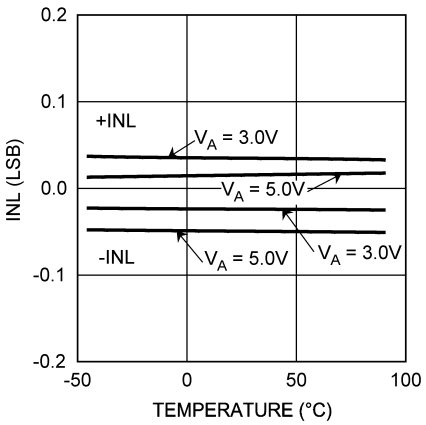


Figure 16. INL vs Temperature

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

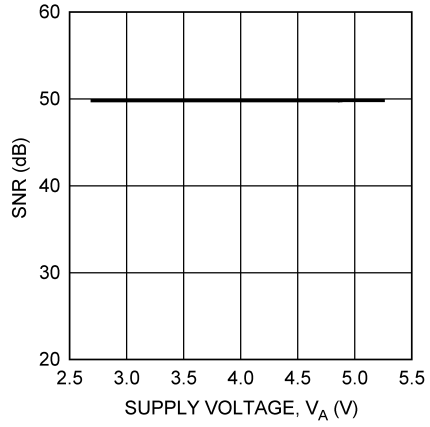


Figure 17. SNR vs Supply

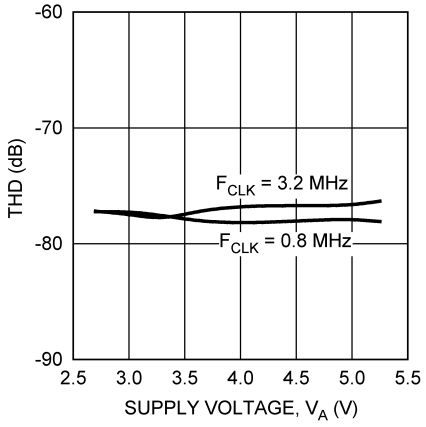


Figure 18. THD vs Supply

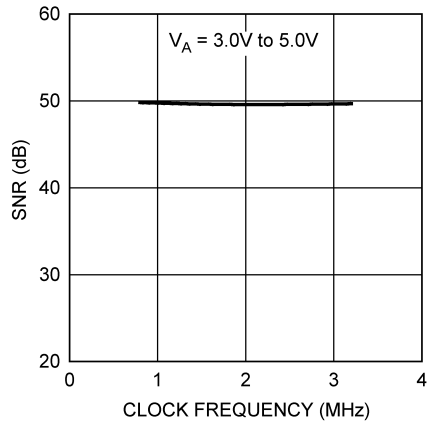


Figure 19. SNR vs Clock Frequency

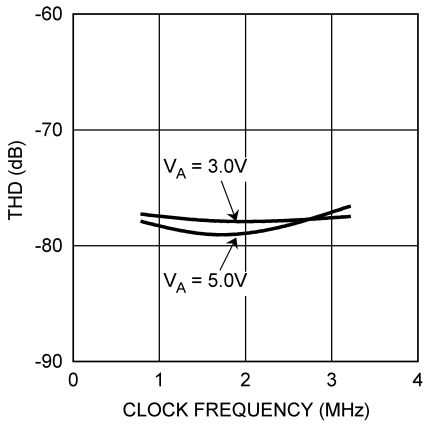


Figure 20. THD vs Clock Frequency

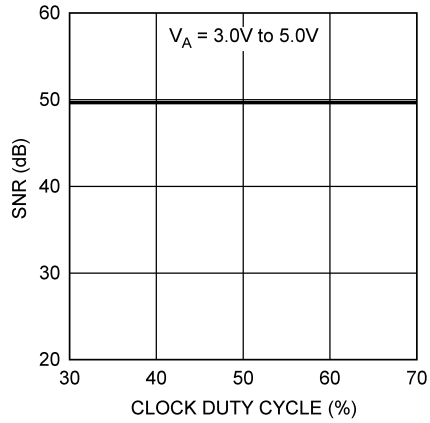


Figure 21. SNR vs Clock Duty Cycle

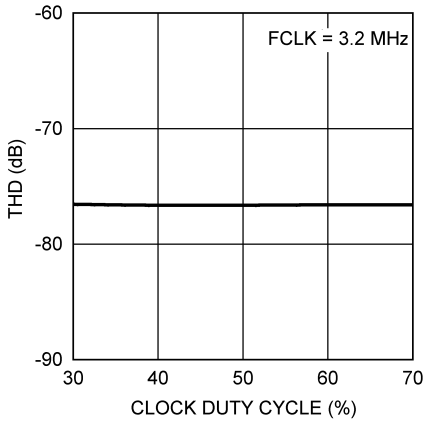


Figure 22. THD vs Clock Duty Cycle

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

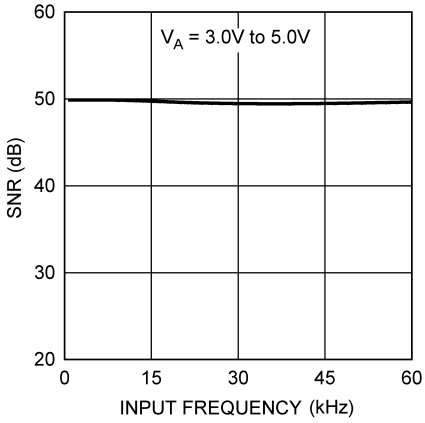


Figure 23. SNR vs Input Frequency

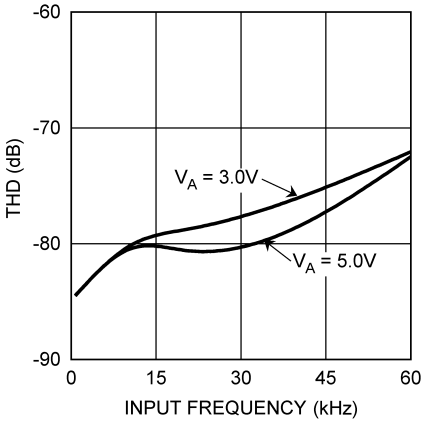


Figure 24. THD vs Input Frequency

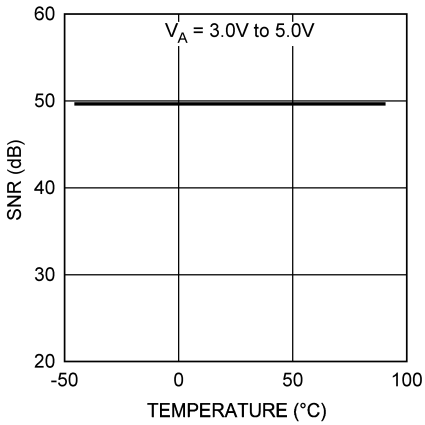


Figure 25. SNR vs Temperature

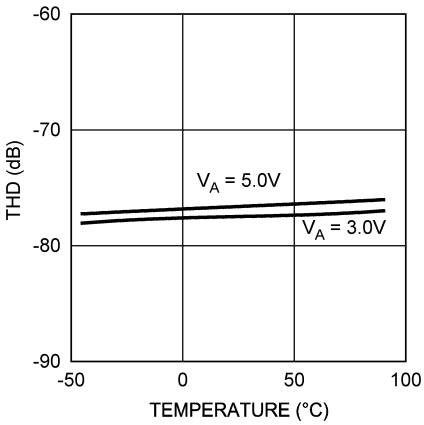


Figure 26. THD vs Temperature

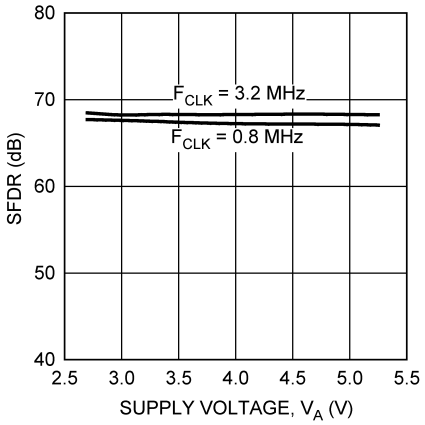


Figure 27. SFDR vs Supply

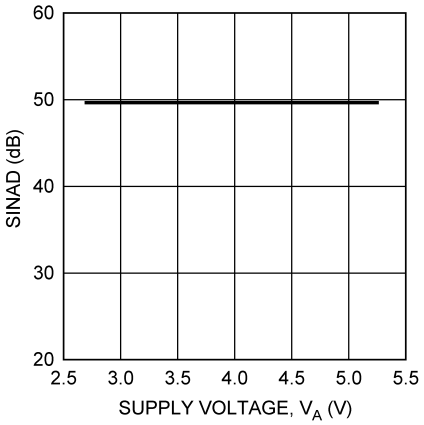


Figure 28. SINAD vs Supply

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

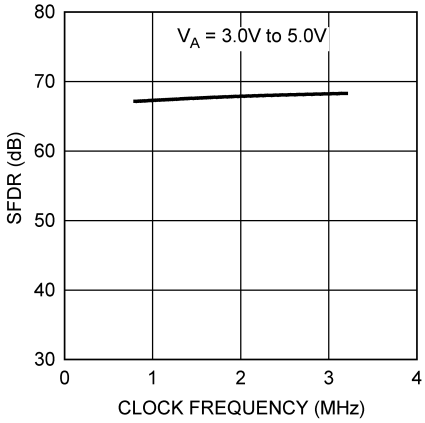


Figure 29. SFDR vs Clock Frequency

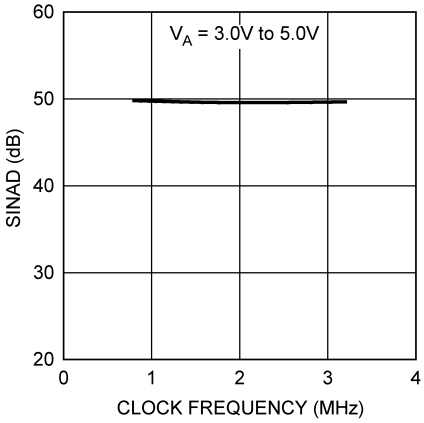


Figure 30. SINAD vs Clock Frequency

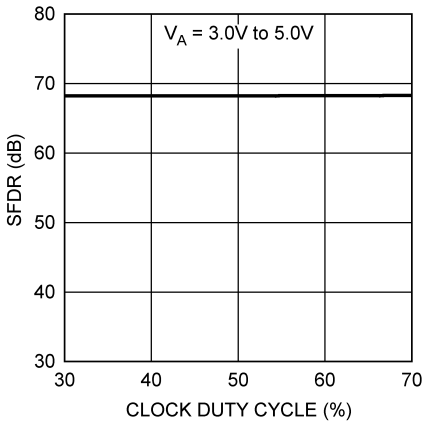


Figure 31. SFDR vs Clock Duty Cycle

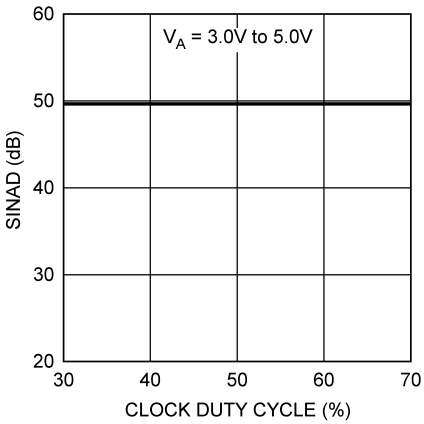


Figure 32. SINAD vs Clock Duty Cycle

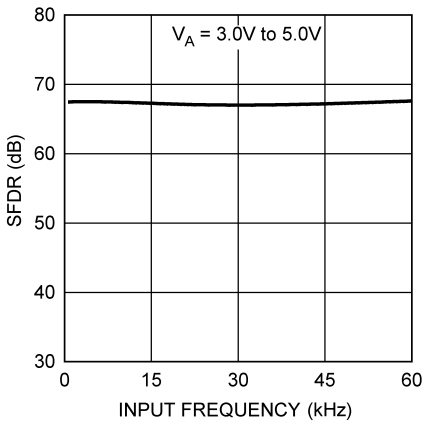


Figure 33. SFDR vs Input Frequency

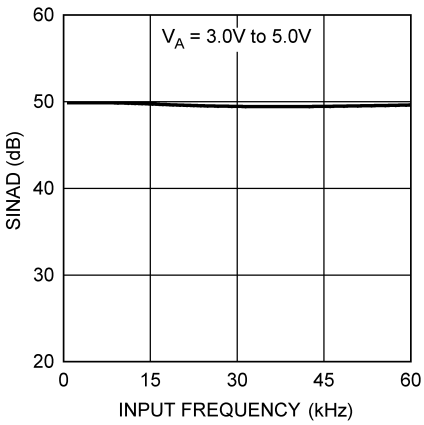


Figure 34. SINAD vs Input Frequency

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

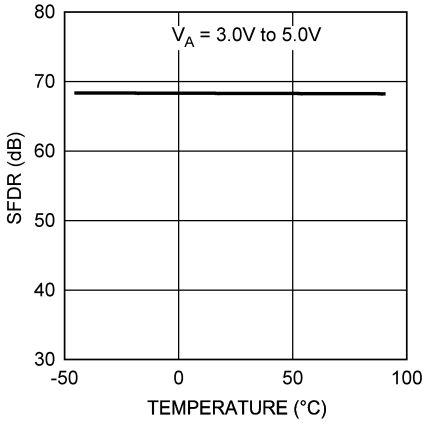


Figure 35. SFDR vs Temperature

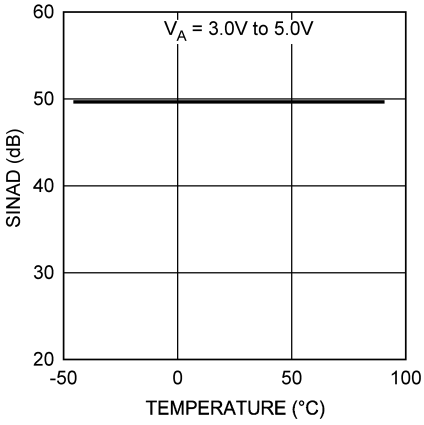


Figure 36. SINAD vs Temperature

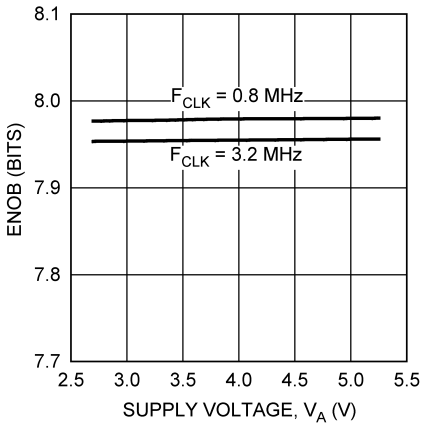


Figure 37. ENOB vs Supply

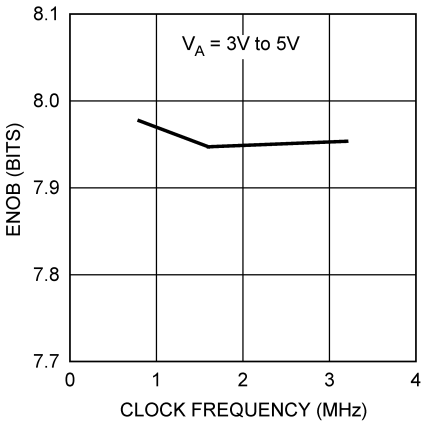


Figure 38. ENOB vs Clock Frequency

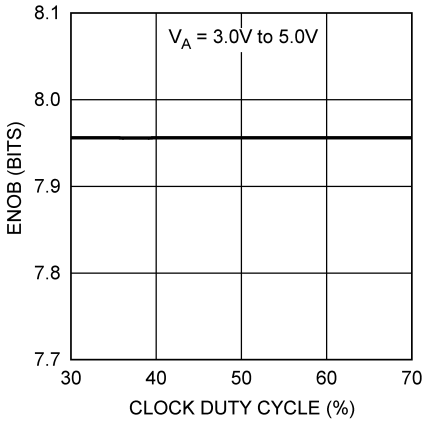


Figure 39. ENOB vs Clock Duty Cycle

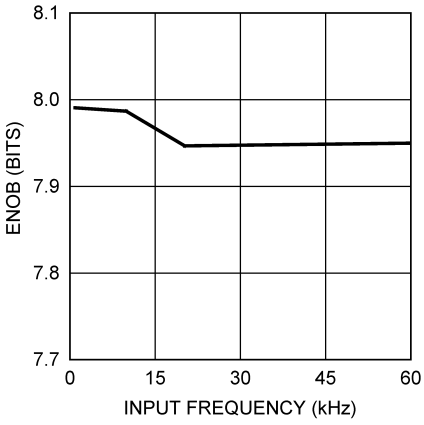


Figure 40. ENOB vs Input Frequency

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 0.8 MHz to 3.2 MHz, and f_{IN} = 39.9 kHz (unless otherwise noted)

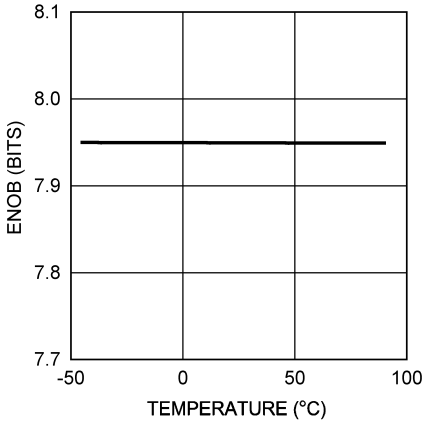


Figure 41. ENOB vs Temperature

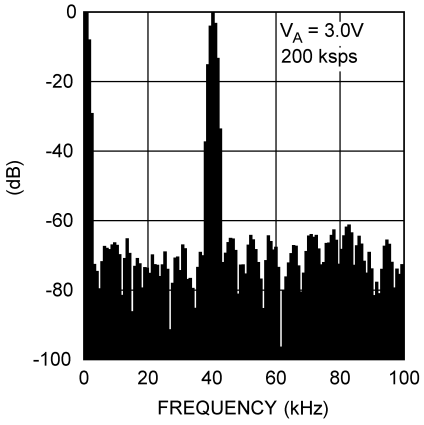


Figure 42. Spectral Response: 3 V, 200 ksps

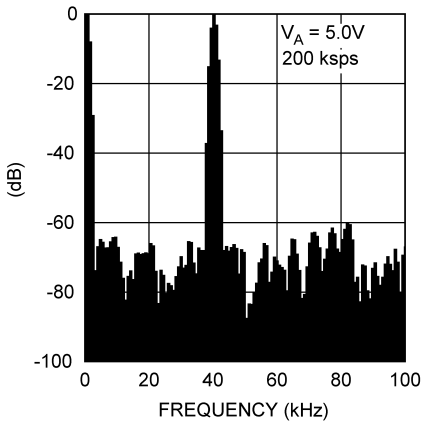


Figure 43. Spectral Response: 5 V, 200 ksps

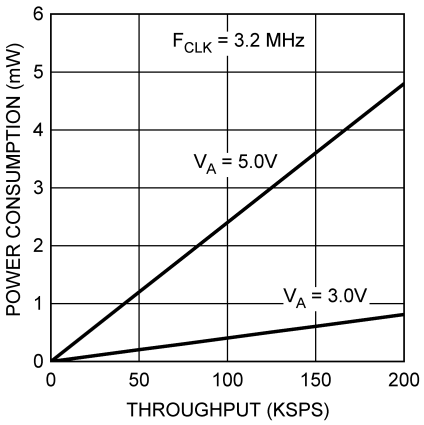


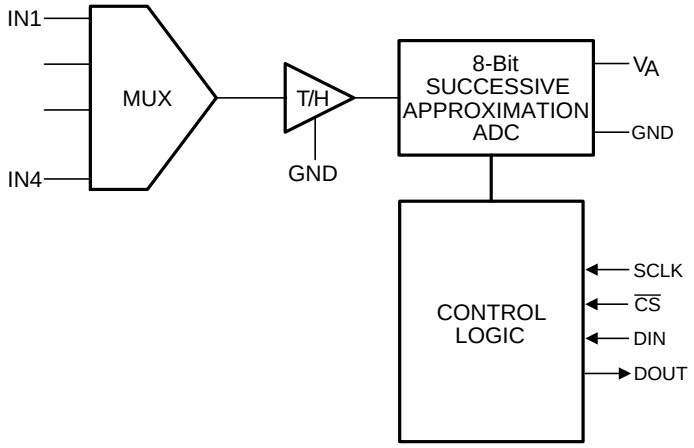
Figure 44. Power Consumption vs Throughput

8 Detailed Description

8.1 Overview

The ADC084S021 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter.

8.2 Functional Block Diagram



8.3 Feature Description

Figure 1 and Figure 3 for the ADC084S021 are shown in *Timing Requirements*. $\overline{CS}$ is chip select, which initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first. Data at DIN, the serial data input pin, is written to the control register of the ADC084S021. New data is written to DIN with each conversion.

A serial frame is initiated on the falling edge of $\overline{CS}$ and ends on the rising edge of $\overline{CS}$. Each frame must contain an integer multiple of 16 rising SCLK edges. The ADC output data (DOUT) is in a high impedance state when $\overline{CS}$ is high and is active when $\overline{CS}$ is low. $\overline{CS}$ thus acts as an output enable, in addition to being a start conversion input. Additionally, the device goes into a power-down state when $\overline{CS}$ is high and between continuous conversion cycles.

During the first 3 cycles of SCLK, the ADC is in the track mode, acquiring the input voltage. For the next 13 SCLK cycles the conversion is accomplished and the data is clocked out, MSB first, starting with the 5th clock. If there is more than one conversion in a frame, the ADC re-enters the track mode on the falling edge of SCLK after the N*16th rising edge of SCLK, and re-enter the hold/convert mode at the N*16+4th falling edge of SCLK, where *N* is an integer.

SCLK is internally gated off when $\overline{CS}$ is high. If SCLK is stopped in the low state while $\overline{CS}$ is high, the subsequent fall of $\overline{CS}$ generates a falling edge of the internal version of SCLK, putting the ADC into the track mode. This is seen by the ADC as the first falling edge of SCLK. If SCLK is stopped with SCLK high, the ADC enters the track mode at the first falling edge of SCLK after the falling edge of $\overline{CS}$.

During each conversion, data is clocked into the device at the DIN pin on the first 8 rising edges of SCLK after the fall of $\overline{CS}$. For each conversion, it is necessary to clock in the data indicating the input that is selected for the conversion after the current one. That is, the conversion that is started at the fall of $\overline{CS}$ is of the voltage at the channel that was selected when the last conversion was started. The first conversion after power up is of the first channel. See Table 1 and Table 3.

If $\overline{CS}$ and SCLK go low within the times defined by t_{CSU} and t_{CLH}, the rising edge of SCLK that begins clocking data in at DIN may be one clock cycle later than expected. It is, therefore, best to strictly observe the minimum t_{CSU} and t_{CLH} times given in *Timing Requirements*.

Feature Description (continued)

There are no power-up delays or dummy conversions required with the ADC084S021. The ADC is able to sample and convert an input to full conversion immediately following power up. The first conversion result after power up is that of IN1.

8.3.1 Transfer Function

The output format of the ADC084S021 is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC084S021 is V_A / 256, and Figure 45 shows the ideal transfer characteristic. The transition from an output code of 0000 0000 to a code of 0000 0001 is at 1/2 LSB, or a voltage of V_A / 512. Other code transitions occur at steps of one LSB.

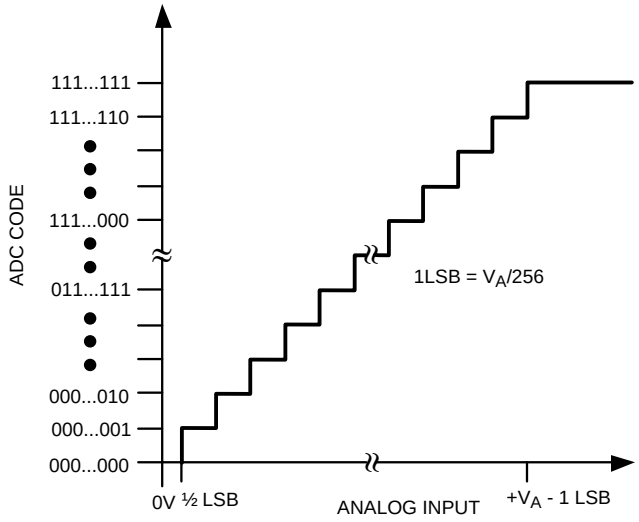


Figure 45. Ideal Transfer Characteristic

8.3.2 Analog Inputs

Figure 46 shows an equivalent circuit for one of the ADC084S021's input channels. Diodes D1 and D2 provide ESD protection for the analog inputs. At no time must any input go beyond (V_A + 300 mV) or (GND − 300 mV), as these ESD diodes begin conducting, which could result in erratic operation. For this reason, these ESD diodes must not be used to clamp the input signal.

The capacitor C1 in Figure 46 has a typical value of 3 pF, and is mainly the package pin capacitance. Resistor R1 is the on resistance of the multiplexer and track or hold switch, which is typically 500 Ω. Capacitor C2 is the ADC084S021 sampling capacitor, which is typically 30 pF. The ADC084S021 delivers the best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. This is especially important when using the ADC084S021 to sample AC signals. Also important when sampling dynamic signals is a band-pass or low-pass filter to reduce harmonics and noise, improving dynamic performance.

Feature Description (continued)

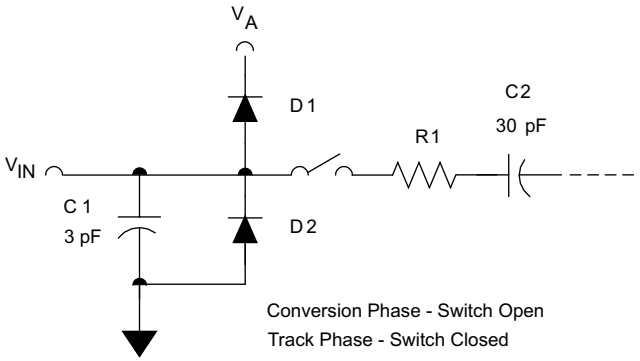


Figure 46. Equivalent Input Circuit

8.3.3 Digital Inputs and Outputs

The digital output of the ADC084S021, DOUT, is limited by and cannot exceed the supply voltage, V_A. The digital input pins are not prone to latch-up and, and although not recommended, SCLK, $\overline{CS}$, and DIN may be asserted before V_A without any latch-up risk.

8.4 Device Functional Modes

The ADC084S021 has two primary modes of operation necessary for capturing an analog signal: track mode and hold mode. Simplified schematics of the ADC084S021 in both track and hold modes are shown in Figure 47 and Figure 48, respectively.

8.4.1 Track Mode

Figure 47 shows the ADC084S021 in track mode: switch SW1 connects the sampling capacitor to one of four analog input channels through the multiplexer, and SW2 balances the comparator inputs. The ADC084S021 is in this state for the first three SCLK cycles after $\overline{CS}$ is brought low.

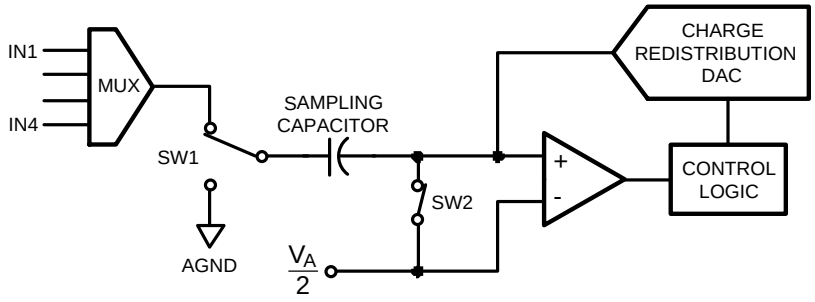


Figure 47. ADC084S021 in Track Mode

8.4.2 Hold Mode

Figure 48 shows the ADC084S021 in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add fixed amounts of charge to the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The ADC084S021 is in this state for the fourth through sixteenth SCLK cycles after $\overline{CS}$ is brought low.

The time when $\overline{CS}$ is low is considered a serial frame. Each of these frames must contain an integer multiple of 16 SCLK cycles, during which time a conversion is performed and clocked out at the DOUT pin and data is clocked into the DIN pin to indicate the multiplexer address for the next conversion.

Device Functional Modes (continued)

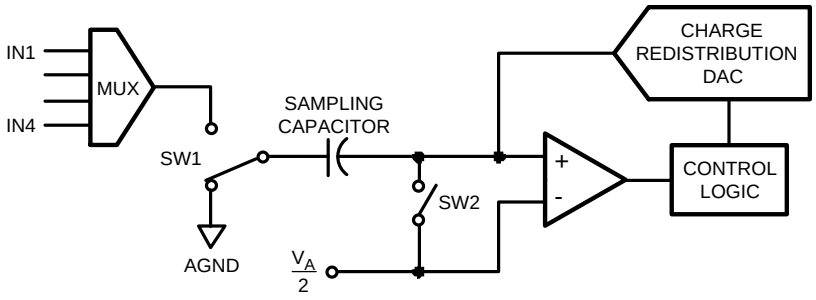


Figure 48. ADC084S021 in Hold Mode

8.5 Register Maps

Table 1 shows the control register bits for the ADC084S021.

Table 1. Control Register Bits

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
DONTC	DONTC	ADD2	ADD1	ADD0	DONTC	DONTC	DONTC

8.5.1 Register Description

Table 2 shows the register descriptions for bit 7 through bit 0.

Table 2. Control Register Bit Descriptions

BIT NO.	SYMBOL	DESCRIPTION
7 to 6, 2 to 0	DONTC	Don't care. The value of these bits do not affect device operation.
5	ADD2	These three bits determine which input channel will be sampled and converted in the next track/hold cycle. The mapping between codes and channels is shown in Table 3.
4	ADD1	
3	ADD0	

Table 3 shows the input channel selection for register bits ADD2, ADD1, and ADD0.

Table 3. Input Channel Selection

INPUT CHANNEL	ADD2	ADD1	ADD0
IN1 (Default)	×	0	0
IN2	×	0	1
IN3	×	1	0
IN4	×	1	1

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 49 shows a typical application of the ADC084S021. Power is provided, in this example, by the Texas Instruments LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The power supply pin is bypassed with a capacitor network located close to the ADC084S021.

Because the reference for the ADC084S021 is the supply voltage, any noise on the supply degrades device noise performance. Use a dedicated linear regulator for this device, or provide sufficient decoupling from other circuitry to keep noise off the ADC084S021 supply pin. Because of the low power requirements of the ADC084S021, it is also possible to use a precision reference as a power supply to maximize performance. The four-wire interface is also shown connected to a microprocessor or DSP.

9.2 Typical Application

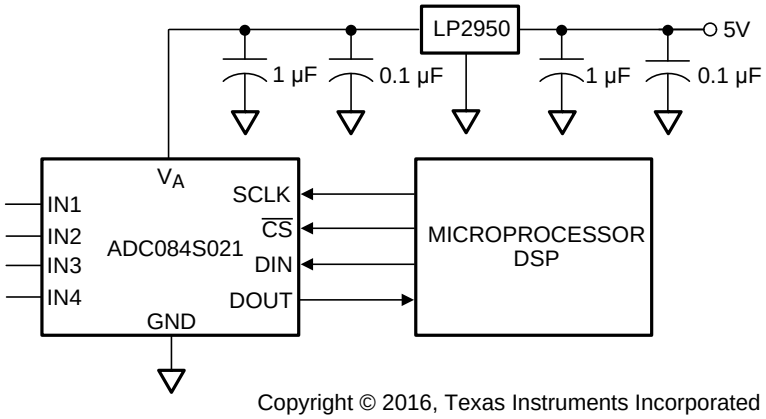


Figure 49. Typical Application Circuit

9.2.1 Design Requirements

In this application, the power consumption of the ADC084S021 must not exceed 1 mW and the throughput may range from 50 ksps to 200 ksps.

9.2.2 Detailed Design Procedure

The two largest factors that impact the power consumption of the ADC084S021 are the supply voltage and the throughput. According to Figure 50, a supply voltage of 3 V allows a throughput of up to 200 ksps at less than 1-mW power consumption. If a supply voltage of 5 V is chosen then the maximum throughput achievable is about 40 ksps, which does not meet the design requirements. Select a supply voltage of 3 V with a F_{CLK} of 3.2 MHz to meet all of the design requirements.

Typical Application (continued)

9.2.3 Application Curve

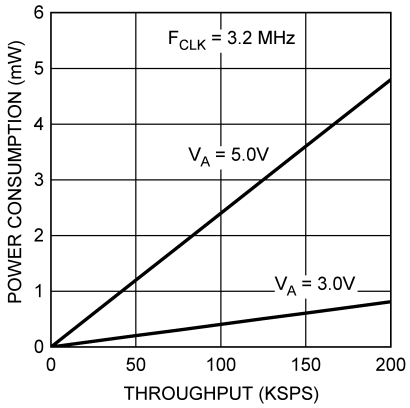


Figure 50. Power Consumption vs Throughput

10 Power Supply Recommendations

The ADC084S021 is fully powered up whenever $\overline{CS}$ is low, and fully powered down when $\overline{CS}$ is high, with one exception: the ADC084S021 automatically enters power-down mode between the 16th falling edge of a conversion and the 1st falling edge of the subsequent conversion (see *Timing Requirements*).

The ADC084S021 can perform multiple conversions back to back; each conversion requires 16 SCLK cycles. The ADC084S021 performs conversions continuously as long as $\overline{CS}$ is held low.

10.1 Power Management

When the ADC084S021 is operated continuously in normal mode, the maximum throughput is $f_{SCLK}/16$. Performance remains as stated in *Electrical Characteristics* as long as the SCLK frequency remains within the range stated at the heading of those tables. Throughput may be traded for power consumption by running f_{SCLK} at its maximum 3.2 MHz and performing fewer conversions per unit time, putting the ADC084S021 into shutdown mode between conversions. See Figure 44 in *Typical Characteristics*. To calculate the power consumption for a given throughput, multiply the fraction of time spent in the normal mode by the normal mode power consumption and add the fraction of time spent in shutdown mode multiplied by the shutdown mode power consumption. Generally, the user places the part into normal mode and then put the part back into shutdown mode. Note that the curve of Figure 44 is nearly linear. This is because the power consumption in the shutdown mode is so small that it can be ignored for all practical purposes.

10.2 Noise Considerations

The charging of any output load capacitance requires current from the power supply, V_A. The current pulses required from the supply to charge the output capacitance causes voltage variations of the supply voltage. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, discharging the output capacitance when the digital output goes from a logic high to a logic low dumps current into the die substrate. Load discharge currents causes *ground bounce* noise in the substrate that degrades noise performance if that current is large enough. The larger is the output capacitance, the more current flows through the die supply line and substrate, causing more noise to be coupled into the analog channel and degrading noise performance.

To keep noise out of the power supply, keep the output load capacitance as small as practical. If the load capacitance is greater than 50 pF, use a 100-Ω series resistor at the ADC output, located as close to the ADC output pin as practical. This limits the charge and discharge current of the output capacitance and improve noise performance.

11 Layout

11.1 Layout Guidelines

For optimum performance, take care with the physical layout of the ADC084S021 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply and ground connections that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an *n-bit* SAR converter, there are n *windows* in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices.

With this in mind, power to the ADC084S021 must be clean and well-bypassed. A 0.1-µF ceramic bypass capacitor must be placed as close to the device as possible. A 1-µF to 10-µF capacitor may also be needed if the impedance of the connection between VA and the power supply is high. Routing of the analog inputs must be kept short and separate from the digital lines. To keep unwanted coupling to a minimum, input traces must also be routed away from noisy components or planes that could crosstalk or interfere with the signal.

11.2 Layout Example

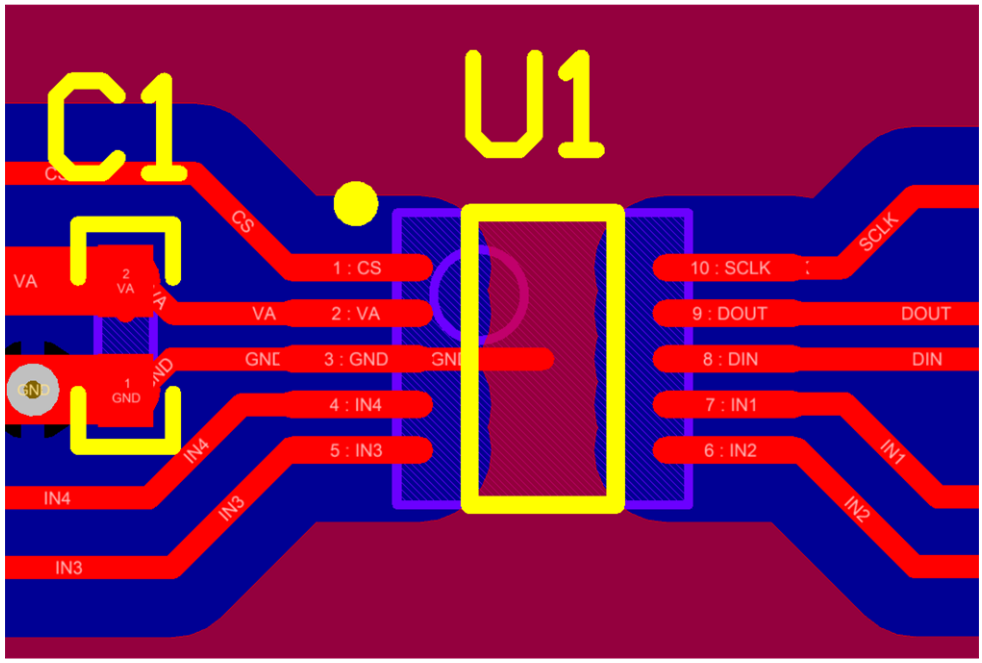


Figure 51. ADC Layout

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの関連用語

アクイジション時間 は、入力電圧を取得するため必要な時間です。これは、ホールド・コンデンサが入力電圧まで充電されるため必要な時間です。

アパーチャ遅延 は、変換の4番目のSLCK立ち下がりエッジから、入力信号が取得されるか、変換用にホールドされるまでの時間です。

変換時間 は、入力電圧が取得されてから、ADCによって入力電圧がデジタルのワードへ変換されるまでに必要な時間です。

クロストーク は、あるチャネルから他のチャネルへのエネルギーのカップリング、またはあるアナログ入力から、測定される別のアナログ入力に出現する信号のエネルギー量です。

差動非直線性(DNL) は、理想的なステップ・サイズである1 LSBからの最大偏差の測定値です。

デューティ・サイクル は、繰り返しのデジタル波形が1周期の合計時間のうちHIGHになる時間の割合です。ここでは、SCLKを基準とします。

実効ビット数(ENOBまたはEFFECTIVE BITS) は、信号対ノイズ+歪み比率(SINAD)を規定する別の方法です。ENOBは(SINAD - 1.76) / 6.02で定義され、コンバータがこの(ENOB)ビット数を持つ完全なADCと等価であることを示します。

フルパワー帯域幅 は、再構築された出力基本波が、フルスケール入力について、低周波数の値より3dB低下する周波数の測定値です。

フルスケール誤差(FSE) は、最後のコード遷移が、理想値(V_{REF^+} - 1½ LSB)とどれだけ差異があるかの測定値で、式 1により定義されます。

$$V_{FSE} = V_{max} + 1.5\ LSB - V_{REF^+} \quad (1)$$

ここで

- V_{max}は、最大のコードへの遷移が発生する電圧です。
- FSEはボルト、LSB、またはフル・スケール範囲に対するパーセンテージで表現できます。

ゲイン誤差 は、最後のコード遷移[(111...110)から(111...111)]が、オフセット誤差の調整後に、理想値(V_{REF} - 1.5 LSB)とどれだけ差異があるかを示します。

積分非直線性(INL) は、それぞれのコードが、負のフルスケール(最初のコード遷移より½ LSBだけ下)と正のフルスケール(最後のコード遷移より½ LSBだけ上)との間に引かれた直線との間にどれだけ差異があるかの測定値です。任意のコードについて、この直線からの差異は、そのコード値の中間から測定されます。

相互変調歪み(IMD) は、2つの正弦周波数が同時にADC入力へ印加されたとき、その結果として新たなスペクトル成分が発生することです。2次および3次相互変調積の電力と、元の周波数における両方の電力の合計との比率と定義されます。IMDは通常、dB単位で表記されます。

欠損コード は、ADCの出力に一切出現しない出力コードです。これらのコードは、どのような入力値からも発生しません。ADC084S021には、欠損コードが存在しないことが保証されています。

オフセット誤差 は、最初のコード遷移[(000...000)から(000...001)]と、理想値(すなわち、GND + 0.5 LSB)との差異です。

信号対ノイズ比(SNR) は、コンバータの出力における入力信号のrms値と、サンプリング周波数の半分より低い他のすべてのスペクトル成分(THD仕様に含まれるDCや高調波は含まれません)の合計のrms値との比率で、dB単位で表記されます。

デバイス・サポート (continued)

信号対ノイズ+歪み比率**(S/N+DまたはSINAD)** は、入力信号のrms値と、クロック周波数の半分より低い他のすべてのスペクトル成分(高調波を含みますが、DCは含まれません)のrms値との比率で、dB単位で表記されます。

スプリアス・フリー・ダイナミック・レンジ**(SFDR)** は、入力信号のrms値と、ピーク・スプリアス信号との差で、dB単位で表記されます。このスプリアス信号には、出力スペクトラムに存在し、入力には存在しないすべての信号が含まれます(DCは除きます)。

全高調波歪み**(THD)** は、出力における最初の5つの高調波成分の合計rmsと、出力において観測される入力信号周波数のrmsレベルとの比率で、dBまたはdBc単位で表記されます。THDは、式 2で計算されます。

$$THD = 20 \bullet \log_{10} \sqrt{\frac{Af_2^2 + \bullet\bullet\bullet + Af_6^2}{Af_1^2}} \quad (2)$$

ここで

- Af_1は、出力における入力周波数のRMS電力です。
- Af_2からAf_6までは、最初の5つの高調波周波数のRMS電力です。

スループット時間 は、2つの連続する変換の開始の間に必要な最小時間です。これは、アクイジション時間と変換および読み出し時間の和です。ADC084S021では、この値は16 SCLK周期です。

12.2 ドキュメントの更新通知を受け取る方法

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12.3 コミュニティ・リソース

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商標

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC084S021CIMM/NO.A	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X19C
ADC084S021CIMM/NO.B	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	-	Call TI	Call TI	-40 to 85	
ADC084S021CIMM/NOPB	Active	Production	VSSOP (DGS) | 10	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X19C
ADC084S021CIMMX/NO.A	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X19C
ADC084S021CIMMX/NOPB	Active	Production	VSSOP (DGS) | 10	3500 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X19C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

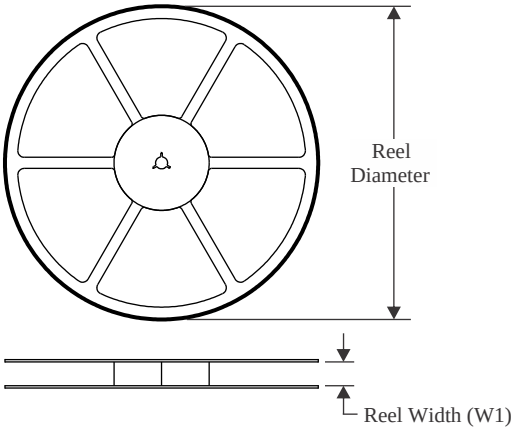
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

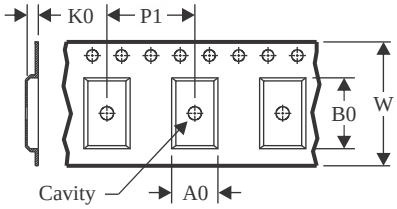
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

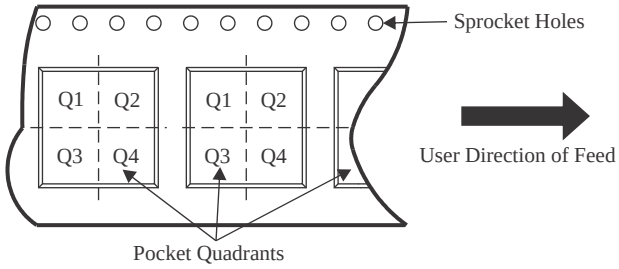


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

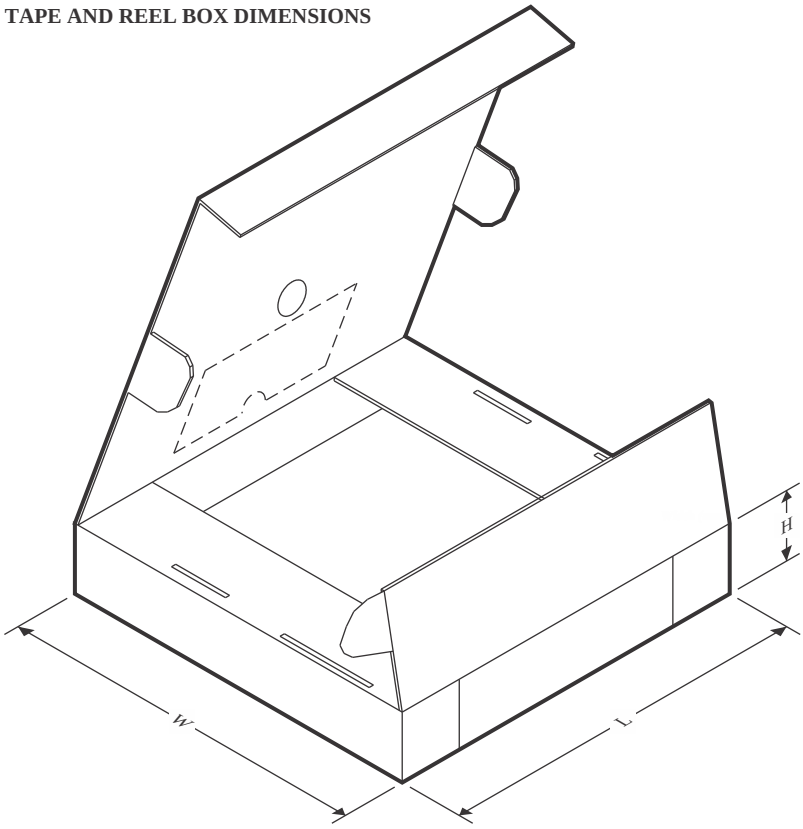
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC084S021CIMM/NOPB	VSSOP	DGS	10	1000	177.8	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADC084S021CIMMX/ NOPB	VSSOP	DGS	10	3500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

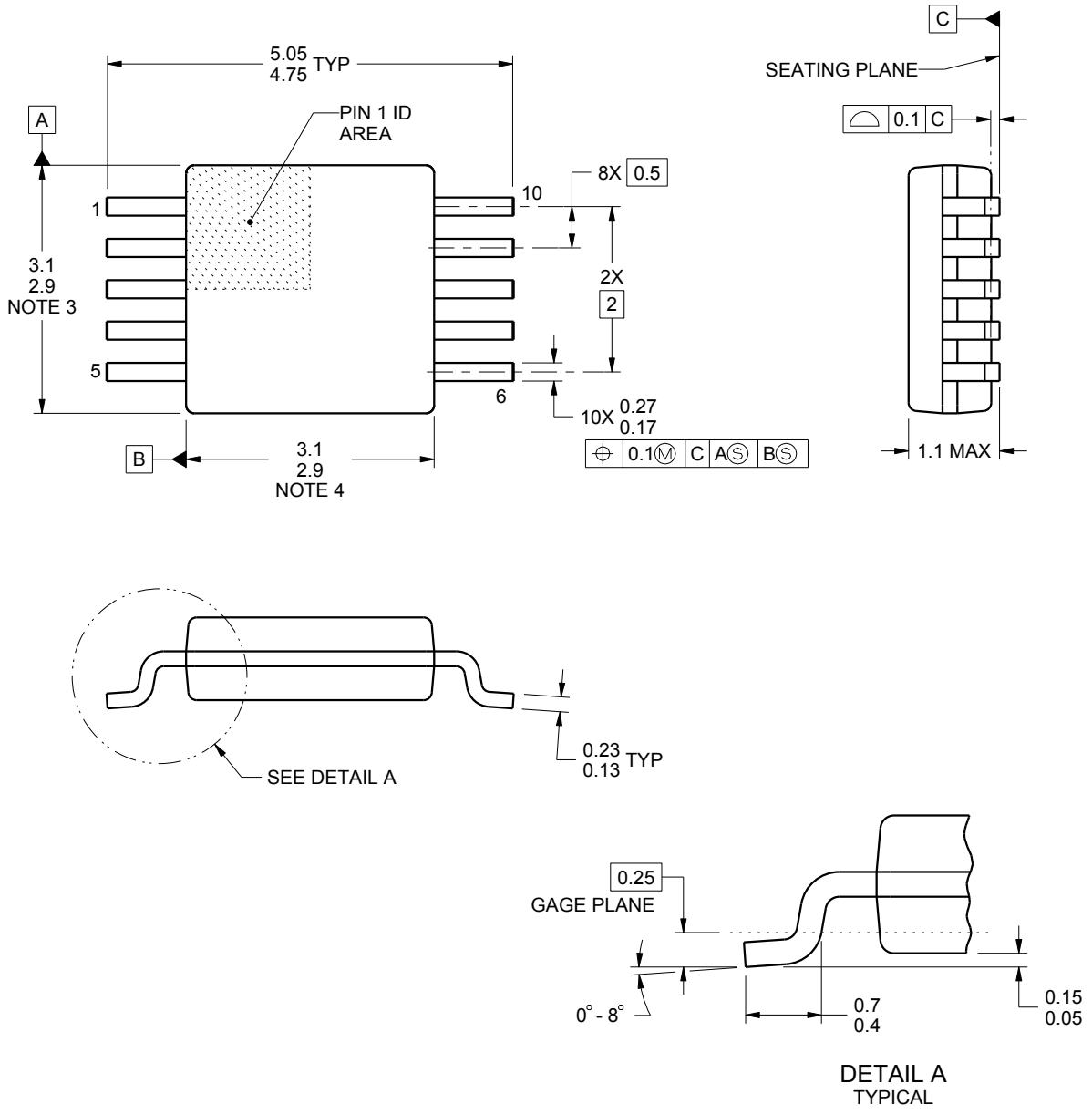
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC084S021CIMM/NOPB	VSSOP	DGS	10	1000	210.0	185.0	35.0
ADC084S021CIMMX/ NOPB	VSSOP	DGS	10	3500	367.0	367.0	35.0

PACKAGE OUTLINE

DGS0010A

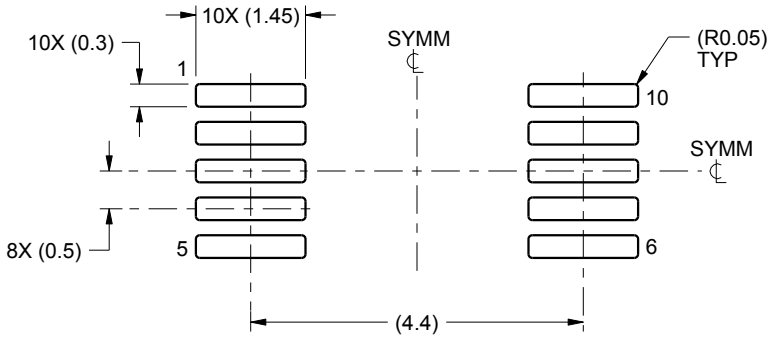
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

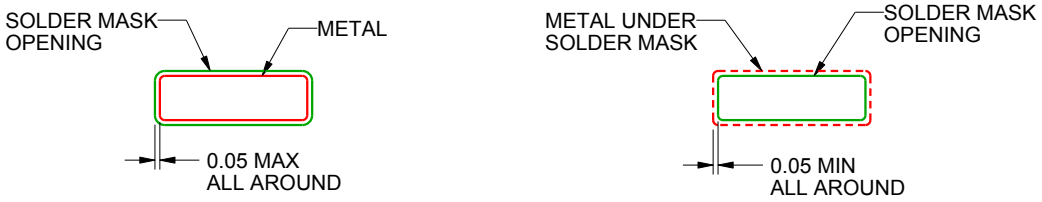


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

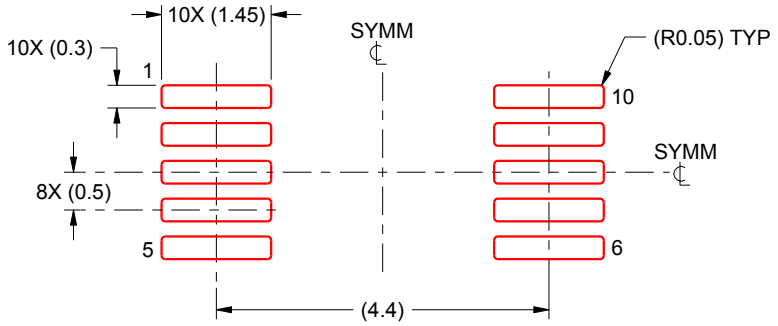


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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最終更新日：2025 年 10 月