ADC081S021シングル・チャネル、50ksps～200ksps、8ビットA/Dコンバータ

1 特長

- 複数のサンプリング・レートについて特性および仕様を規定
- 6ピンのWSONおよびSOT-23パッケージ
- 可変電力管理
- 2.7V～5.25Vの範囲の単一電源
- 対応規格: SPI™、 QSPI™、 MICROWIRE™、およびDSP
- DNL: +0.04/-0.03 LSB (標準値)
- INL: +0.04/–0.03 LSB (標準値)
- SNR: 49.6dB (標準値)
- 消費電力:
  - 3.6V電源: 1.3mW (標準値)
  - 5.25V電源: 7.7mW (標準値)

2 アプリケーション

- ポータブル・システム
- リモート・データ収集
- 計測および制御システム

3 概要

ADC081S021デバイスは低消費電力のシングル・チャネルCMOS 8ビットA/Dコンバータで、高速のシリアル・インターフェイスが搭載されています。単一のサンプリング・レートのみでパフォーマンスを規定する従来の手法とは異なり、ADC081S021は50ksps～200kspsのサンプリング・レート範囲全体にわたって完全に規定されています。コンバータは逐次比較型のアーキテクチャをベースとし、内部的なトラック・アンド・ホールド回路を使用します。

出力のシリアル・データはストレート・バイナリで、SPI、QSPI、MICROWIREなどいくつかの標準、および多くの一般的なDPSシリアル・インターフェイスと互換性があります。

ADC081S021は2.7V～5.25Vの範囲の単一電源で動作します。3.6Vまたは5.25V電源を使用するときの通常の消費電力は、それぞれ1.3mWおよび7.7mWです。

パワーダウン機能により、消費電力は5.25V電源の使用時に約2.6µWまで削減されます。

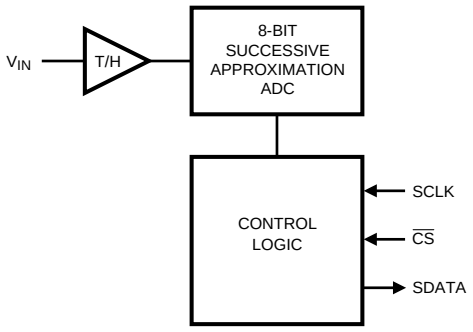
ADC081S021は、6ピンのWSONおよびSOT-23パッケージで提供されます。工業用温度範囲の-40°C～85℃での動作が保証されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
ADC081S021	SOT-23 (6)	2.50mm×2.20mm
	WSON (6)	1.60mm×2.90mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

ブロック図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision F (November 2013) から **Revision G** に変更 **Page**

- 「*ESD定格*」の表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- Changed table title *Pin-Compatible Alternatives by Resolution and Speed* to *Device Comparison Table* ... 3

Revision E (March 2013) から **Revision F** に変更 **Page**

- Changed sentence in the "Using the ADC081S021" section ... 12

Revision D (March 2013) から **Revision E** に変更 **Page**

- ナショナル セミコンダクターのデータシートのレイアウトをTIフォーマットへ変更 変更 ... 1

5 Device Comparison Table

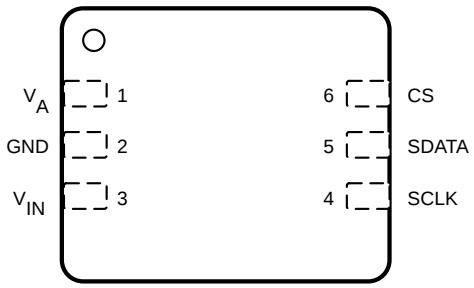
RESOLUTION	SPECIFIED SAMPLE RATE RANGE(1)		
	50 TO 200 KSPS	200 TO 500 KSPS	500 KSPS TO 1 MSPS
12 Bits	ADC081S021121S021	ADC081S021121S051	ADC081S021121S101
10 Bits	ADC081S021101S021	ADC081S021101S051	ADC081S021101S101
8 Bits	ADC081S021	ADC081S021081S051	ADC081S021081S101

(1) All devices are fully pin and function compatible.

6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View

NGF Package
6-Pin WSON
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	V_A	P	Positive supply pin. This pin must be connected to a quiet 2.7-V to 5.25-V source and bypassed to GND with a 1-µF capacitor and a 0.1-µF monolithic capacitor placed within 1 cm of the power pin.
2	GND	G	The ground return for the supply and signals.
3	V_{IN}	I	Analog input. This signal can range from 0 V to V_A.
4	SCLK	I	Digital clock input. This clock directly controls the conversion and readout processes.
5	SDATA	O	Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.
6	$\overline{CS}$	I	Chip select. On the falling edge of $\overline{CS}$, a conversion process begins.

(1) G = Ground, I = Input, O = Output, P = Power

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

	MIN	MAX	UNIT
Analog supply voltage, V_A	–0.3	6.5	V
Voltage on any analog pin to GND	–0.3	V_A + 0.3	V
Voltage on any digital pin to GND	–0.3	6.5	V
Input current at any pin(4)		±10	mA
Package input current(4)		±20	mA
Power consumption at T_A = 25°C	See(5)		
Junction temperature, T_J		150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are measured with respect to GND = 0 V, unless otherwise specified.
(3) If Military/Aerospace specified devices are required, please contact the TI Office/Distributors for availability and specifications.
(4) When the input voltage at any pin exceeds the power supply (that is, V_{IN} < GND or V_{IN} > V_A), the current at that pin must be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two. These specifications do not apply to the V_A pin. The current into the V_A pin is limited by the analog supply voltage specification.
(5) The absolute maximum junction temperature ($T_J$max) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_J$max, the junction-to-ambient thermal resistance (θ_{JA}), and the ambient temperature (T_A), and can be calculated using the formula $P_D MAX = (T_J max - T_A) / \theta_{JA}$. The values for maximum power dissipation listed above is reached only when the device is operated in a severe fault condition (that is, when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions must always be avoided.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge(1)	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(2)	±3500	V
		Machine model (MM)	±300	

(1) Human body model is 100-pF capacitor discharged through a 1.5-kΩ resistor. Machine model is 220 pF discharged through 0 Ω.
(2) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_A	Supply voltage	2.7	5.25	V
	Digital input pins voltage (regardless of supply voltage)	–0.3	5.25	V
	Analog input pins voltage	0	V_A	V
	Clock frequency	25	20000	kHz
	Sample rate		1	Msps
T_A	Operating temperature	–40	85	°C

(1) All voltages are measured with respect to GND = 0 V, unless otherwise specified.

7.4 Thermal Information

THERMAL METRIC[1]		ADC081S021		UNIT
		DBV (SOT-23)	NGF (WSON)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	184.5	99.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	151.2	118.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	29.7	68.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	29.8	6.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	29.1	69.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	14.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

7.5 Electrical Characteristics

Typical values correspond to T_A = 25°C, and minimum and maximum limits apply over –40°C to 85°C operating temperature range (unless otherwise noted). V_A = 2.7 V to 5.25 V, f_{SCLK} = 1 MHz to 4 MHz, f_{SAMPLE} = 50 ksps to 200 ksps, and C_L = 15 pF (unless otherwise noted).[1]

PARAMETER		TEST CONDITIONS		MIN[2]	TYP	MAX[2]	UNIT
STATIC CONVERTER CHARACTERISTICS							
	Resolution with no missing codes					8	Bits
INL	Integral non-linearity	V_A = 2.7 V to 3.6 V			±0.03	±0.3	LSB
		V_A = 4.75 V to 5.25 V	T_A = 25°C	–0.03		0.04	LSB
			T_A = –40°C to 85°C	±0.3		±0.3	
DNL	Differential non-linearity	V_A = 2.7 V to 3.6 V			±0.03	±0.2	LSB
		V_A = 4.75 V to 5.25 V	T_A = 25°C	–0.03		0.04	LSB
			T_A = –40°C to 85°C	±0.2		±0.2	
V_{OFF}	Offset error	V_A = 2.7 V to 3.6 V			–0.01	±0.2	LSB
		V_A = 4.75 V to 5.25 V			0.03	±0.2	LSB
GE	Gain error	V_A = 2.7 V to 3.6 V			0.04	±0.4	LSB
		V_A = 4.75 V to 5.25 V			0.1	±0.4	LSB
TUE	Total unadjusted error	V_A = 2.7 V to 3.6 V	T_A = 25°C	–0.065		0.055	LSB
			T_A = –40°C to 85°C	±0.3		±0.3	
		V_A = 4.75 V to 5.25 V	T_A = 25°C	–0.06		0.03	LSB
			T_A = –40°C to 85°C	±0.3		±0.3	
DYNAMIC CONVERTER CHARACTERISTICS							
SINAD	Signal-to-noise plus distortion ratio	V_A = 2.7 V to 5.25 V, f_{IN} = 100 kHz, –0.02 dBFS		49	49.5		dBFS
SNR	Signal-to-noise ratio	V_A = 2.7 V to 5.25 V, f_{IN} = 100 kHz, –0.02 dBFS		49	49.6		dBFS
THD	Total harmonic distortion	V_A = 2.7 V to 5.25 V, f_{IN} = 100 kHz, –0.02 dBFS			–77	–65	dBFS
SFDR	Spurious-free dynamic range	V_A = 2.7 V to 5.25 V, f_{IN} = 100 kHz, –0.02 dBFS		65	68		dBFS
ENOB	Effective number of bits	V_A = 2.7 V to 5.25 V, f_{IN} = 100 kHz, –0.02 dBFS		7.8	7.9		Bits
IMD	Intermodulation distortion, second order terms	V_A = 5.25 V, f_a = 103.5 kHz, f_b = 113.5 kHz			–83		dBFS
	Intermodulation distortion, third order terms	V_A = 5.25 V, f_a = 103.5 kHz, f_b = 113.5 kHz			–82		dBFS

(1) Tested limits are ensured to TI's AOQL (Average Outgoing Quality Level).
(2) Data sheet minimum and maximum specification limits are specified by design, test, or statistical analysis.

Electrical Characteristics (continued)

Typical values correspond to T_A = 25°C, and minimum and maximum limits apply over –40°C to 85°C operating temperature range (unless otherwise noted). V_A = 2.7 V to 5.25 V, f_{SCLK} = 1 MHz to 4 MHz, f_{SAMPLE} = 50 ksps to 200 ksps, and C_L = 15 pF (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN(2)	TYP	MAX(2)	UNIT
FPBW	–3 dB full power bandwidth	V_A = 5 V		11		MHz
		V_A = 3 V		8		MHz
ANALOG INPUT CHARACTERISTICS						
V_{IN}	Input range			0 to V_A		V
I_{DCL}	DC leakage current				±1	µA
C_{INA}	Input capacitance	Track mode		30		pF
		Hold mode		4		pF
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	Input high voltage	V_A = 5.25 V	2.4			V
		V_A = 3.6 V	2.1			V
V_{IL}	Input low voltage	V_A = 5 V			0.8	V
		V_A = 3 V			0.4	V
I_{IN}	Input current	V_{IN} = 0 V or V_A		±0.1	±1	µA
C_{IND}	Digital input capacitance			2	4	pF
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	Output high voltage	I_{SOURCE} = 200 µA	V_A – 0.2	V_A – 0.07		V
		I_{SOURCE} = 1 mA		V_A – 0.1		V
V_{OL}	Output low voltage	I_{SINK} = 200 µA		0.03	0.4	V
		I_{SINK} = 1 mA		0.1		V
I_{OZH}, I_{OZL}	TRI-STATE leakage current			±0.1	±10	µA
C_{OUT}	TRI-STATE output capacitance			2	4	pF
	Output coding			Straight (natural) binary		
POWER SUPPLY CHARACTERISTICS						
V_A	Supply voltage		2.7		5.25	V
I_A	Supply current, normal mode (operational, $\overline{CS}$ low)	V_A = 5.25 V, f_{SAMPLE} = 200 ksps		1.47	2.2	mA
		V_A = 3.6 V, f_{SAMPLE} = 200 ksps		0.36	0.9	mA
	Supply current, shutdown ($\overline{CS}$ high)	f_{SCLK} = 0 MHz, V_A = 5.25 V, f_{SAMPLE} = 0 ksps		500		nA
		V_A = 5.25 V, f_{SCLK} = 4 MHz, f_{SAMPLE} = 0 ksps		60		µA
P_D	Power consumption, normal mode (operational, $\overline{CS}$ low)	V_A = 5.25 V		7.7	11.6	mW
		V_A = 3.6 V		1.3	3.24	mW
	Power consumption, shutdown ($\overline{CS}$ high)	f_{SCLK} = 0 MHz, V_A = 5.25 V, f_{SAMPLE} = 0 ksps		2.6		µW
		f_{SCLK} = 4 MHz, V_A = 5.25 V, f_{SAMPLE} = 0 ksps		315		µW
AC ELECTRICAL CHARACTERISTICS						
f_{SCLK}	Clock frequency	See(3)	1		4	MHz
f_S	Sample rate	See(3)	50		200	ksps
t_{HOLD}	Hold time, falling edge				13	SCLK
DC	SCLK duty cycle	f_{SCLK} = 4 MHz	40%	50%	60%	
t_{ACQ}	Minimum time required for acquisition				350	ns
t_{QUIET}	Quiet time	See(4)	50			ns
t_{AD}	Aperture delay			3		ns
t_{AJ}	Aperture jitter			30		ps

(3) This is the frequency range over which the electrical performance is ensured. The device is functional over a wider range which is specified under Operating Ratings.
(4) Minimum quiet time required by bus relinquish and the start of the next conversion.

7.6 Timing Requirements

The following specifications apply for V_A = 2.7 V to 5.25 V, GND = 0 V, f_{SCLK} = 1.0 MHz to 4.0 MHz, C_L = 25 pF, f_{SAMPLE} = 50 ksps to 200 ksps, and T_A = –40°C to 85°C (unless otherwise noted).(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{CS}	Minimum $\overline{CS}$ pulse width		10			ns
t_{CSSU}	$\overline{CS}$ setup time prior to SCLK falling edge		10			ns
t_{CSH}	$\overline{CS}$ hold time after SCLK falling edge		1			ns
t_{EN}	Delay from $\overline{CS}$ until SDATA TRI-STATE disabled(2)				20	ns
t_{ACC}	Data access time after SCLK falling edge(3)	V_A = 2.7 V to 3.6 V			40	ns
		V_A = 4.75 V to 5.25 V			20	ns
t_{CL}	SCLK low pulse width		0.4 × t_{SCLK}			ns
t_{CH}	SCLK high pulse width		0.4 × t_{SCLK}			ns
t_H	SCLK to data valid hold time	V_A = 2.7 V to 3.6 V	7			ns
		V_A = 4.75 V to 5.25 V	5			ns
t_{DIS}	SCLK falling edge to SDATA high impedance(4)	V_A = 2.7 V to 3.6 V	6		25	ns
		V_A = 4.75 V to 5.25 V	5		25	ns
$t_{POWER-UP}$	Power-up time from full power down	T_A = 25°C		1		µs

(1) Data sheet minimum and maximum specification limits are specified by design, test, or statistical analysis.
(2) Measured with the timing test circuit and defined as the time taken by the output signal to cross 1 V.
(3) Measured with the timing test circuit and defined as the time taken by the output signal to cross 1 V or 2 V.
(4) t_{DIS} is derived from the time taken by the outputs to change by 0.5 V with the timing test circuit. The measured number is then adjusted to remove the effects of charging or discharging the output capacitance. This means that t_{DIS} is the true bus relinquish time, independent of the bus loading.

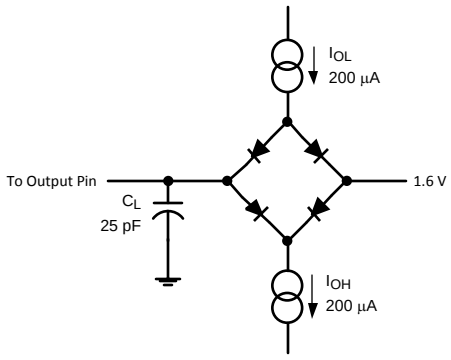


Figure 1. Timing Test Circuit

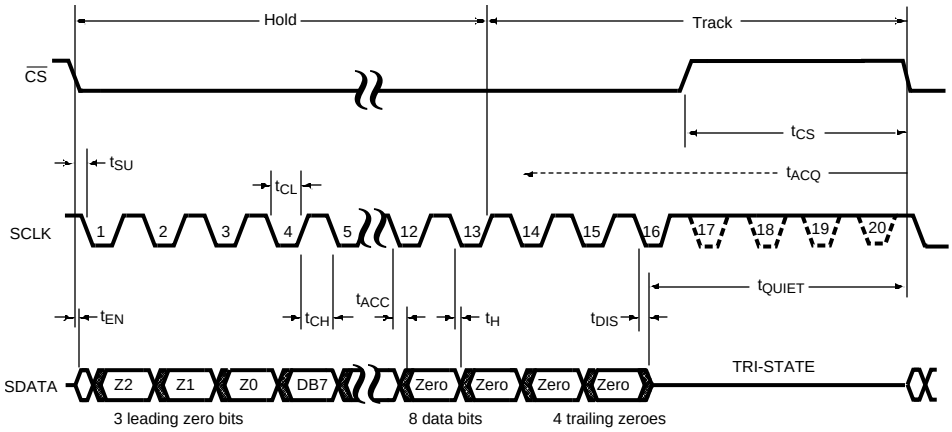


Figure 2. Serial Timing Diagram

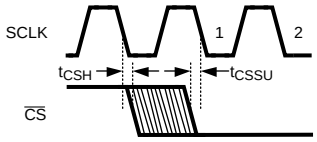


Figure 3. SCLK and $\overline{CS}$ Timing Parameters

7.7 Typical Characteristics

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 1 MHz to 4 MHz, f_{IN} = 100 kHz (unless otherwise noted)

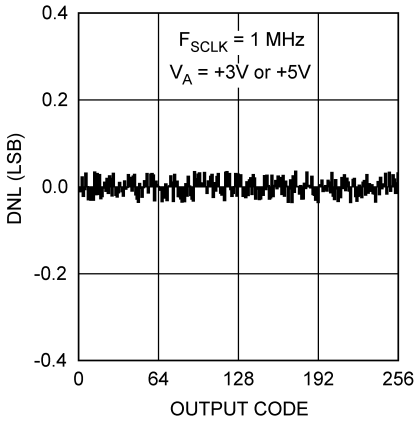


Figure 4. DNL f_{SCLK} = 1 MHz

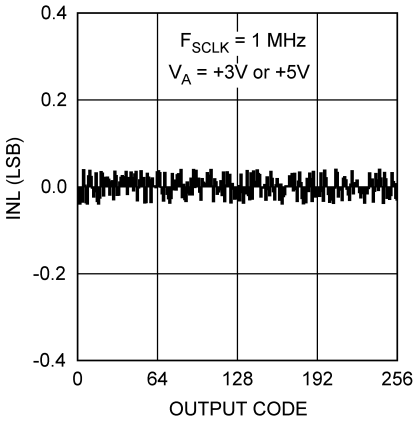


Figure 5. INL f_{SCLK} = 1 MHz

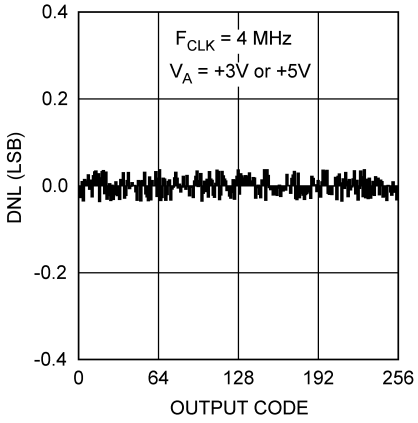


Figure 6. DNL f_{SCLK} = 4 MHz

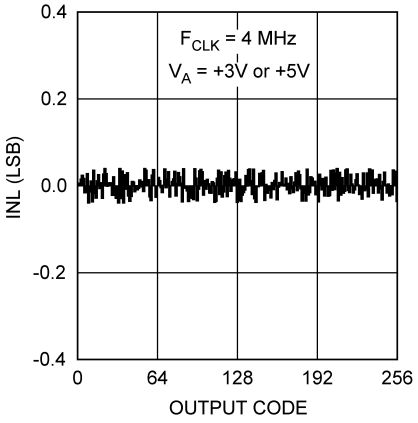


Figure 7. INL f_{SCLK} = 4 MHz

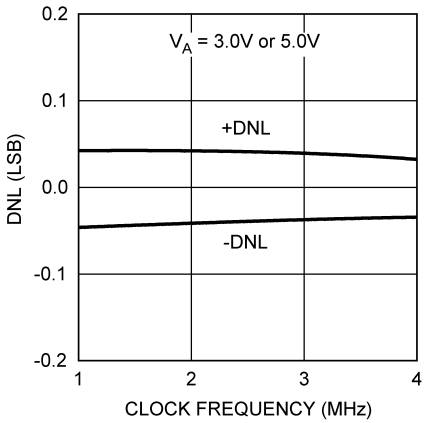


Figure 8. DNL vs Clock Frequency

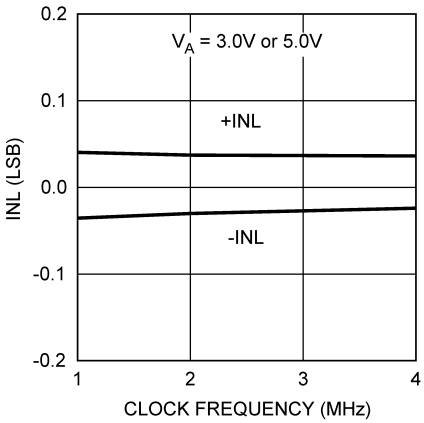


Figure 9. INL vs Clock Frequency

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 1 MHz to 4 MHz, f_{IN} = 100 kHz (unless otherwise noted)

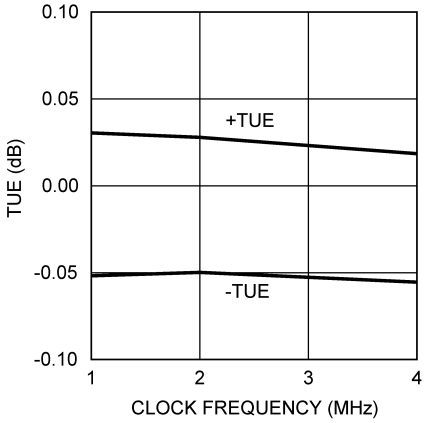


Figure 10. Total Unadjusted Error vs Clock Frequency V_A = 3 V or 5 V

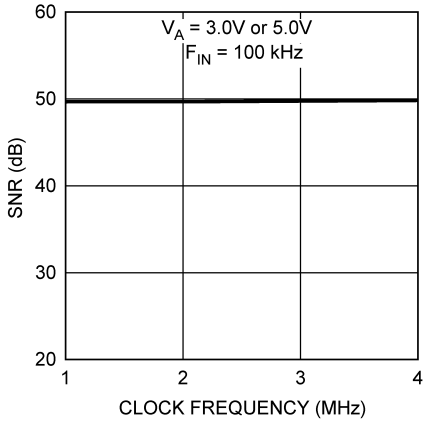


Figure 11. SNR vs Clock Frequency

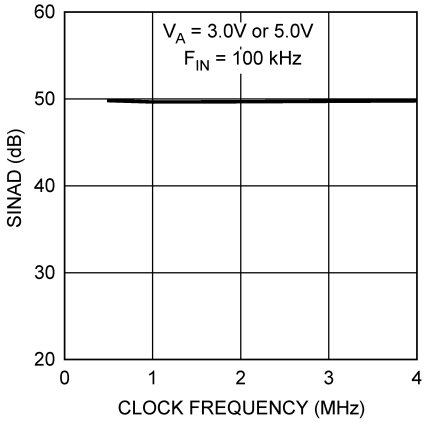


Figure 12. SINAD vs Clock Frequency

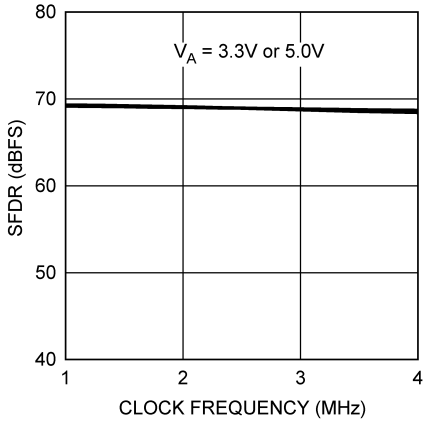


Figure 13. SFDR vs Clock Frequency

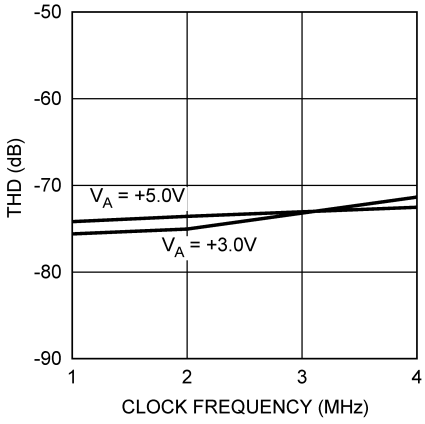


Figure 14. THD vs Clock Frequency

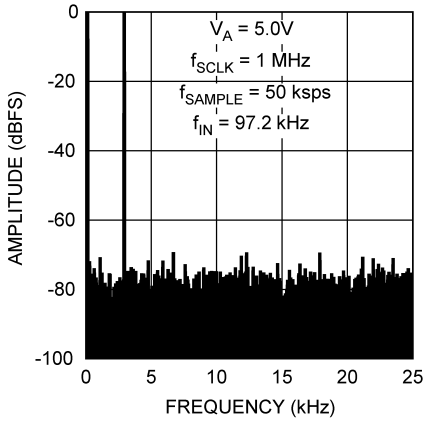


Figure 15. Spectral Response, V_A = 5 V f_{SCLK} = 1 MHz

Typical Characteristics (continued)

T_A = 25°C, f_{SAMPLE} = 50 ksps to 200 ksps, f_{SCLK} = 1 MHz to 4 MHz, f_{IN} = 100 kHz (unless otherwise noted)

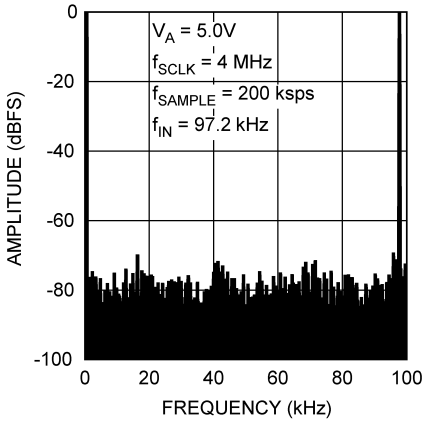


Figure 16. Spectral Response, V_A = 5 V f_{SCLK} = 4 MHz

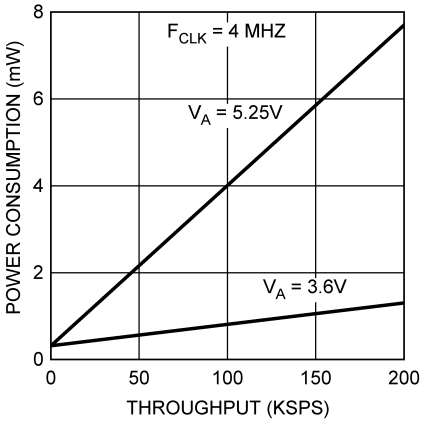


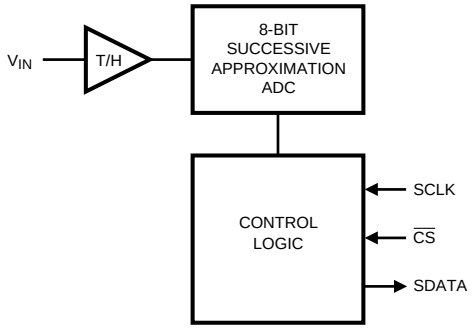
Figure 17. Power Consumption vs Throughput f_{SCLK} = 4 MHz

8 Detailed Description

8.1 Overview

The ADC081S021 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter core. Simplified schematics of the ADC081S021 in both track and hold modes are shown in Figure 19 and Figure 18, respectively. In Figure 19, the device is in track mode: switch SW1 connects the sampling capacitor to the input, and SW2 balances the comparator inputs. The device is in this state until $\overline{CS}$ is brought low, at which point the device moves to hold mode.

8.2 Functional Block Diagram



8.3 Feature Description

The serial interface timing diagram for the ADC is shown in *Timing Requirements*. $\overline{CS}$ is chip select, which initiates conversions on the ADC and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. SDATA is the serial data out pin, where a conversion result is found as a serial data stream.

Basic operation of the ADC begins with $\overline{CS}$ going low, which initiates a conversion process and data transfer. Subsequent rising and falling edges of SCLK are labelled with reference to the falling edge of $\overline{CS}$; for example, *the third falling edge of SCLK* shall refer to the third falling edge of SCLK after $\overline{CS}$ goes low.

At the fall of $\overline{CS}$, the SDATA pin comes out of TRI-STATE and the converter moves from track mode to hold mode. The input signal is sampled and held for conversion on the falling edge of $\overline{CS}$. The converter moves from hold mode to track mode on the 13th rising edge of SCLK (see *Timing Requirements*). It is at this point that the interval for the T_{ACQ} specification begins. At least 350 ns must pass between the 13th rising edge of SCLK and the next falling edge of $\overline{CS}$. The SDATA pin is placed back into TRI-STATE after the 16th falling edge of SCLK, or at the rising edge of $\overline{CS}$, whichever occurs first. After a conversion is completed, the quiet time (t_{QUIET}) must be satisfied before bringing $\overline{CS}$ low again to begin another conversion.

Sixteen SCLK cycles are required to read a complete sample from the ADC. The sample bits (including leading or trailing zeroes) are clocked out on falling edges of SCLK, and are intended to be clocked in by a receiver on subsequent rising edges of SCLK. The ADC produces three leading zero bits on SDATA, followed by eight data bits, most significant first. After the data bits, the ADC clocks out four trailing zeros.

If $\overline{CS}$ goes low before the rising edge of SCLK, an additional (fourth) zero bit may be captured by the next falling edge of SCLK.

8.3.1 Determining Throughput

Throughput depends on the frequency of SCLK and how much time is allowed to elapse between the end of one conversion and the start of another. At the maximum specified SCLK frequency, the maximum ensured throughput is obtained by using a 20 SCLK frame. As shown in *Timing Requirements*, the minimum allowed time between $\overline{CS}$ falling edges is determined by:

1. 12.5 SCLKs for Hold mode.
2. The larger of two quantities: either the minimum required time for Track mode (t_{ACQ}) or 2.5 SCLKs to finish reading the result.

Feature Description (continued)

3. 0, 1/2, or 1 SCLK padding to ensure an even number of SCLK cycles so there is a falling SCLK edge when $\overline{CS}$ next falls.

For example, at the fastest rate for this family of parts, SCLK is 20 MHz and 2.5 SCLKs are 125 ns, so the minimum time between $\overline{CS}$ falling edges is calculated by Equation 1.

$$12.5 \times 50 \text{ ns} + 350 \text{ ns} + 0.5 \times 50 \text{ ns} = 1000 \text{ ns} \quad (1)$$

(12.5 SCLKs + t_{ACQ} + 1/2 SCLK) which corresponds to a maximum throughput of 1 MSPS. At the slowest rate for this family, SCLK is 1 MHz. Using a 20 cycle conversion frame as shown in *Timing Requirements* yields a 20-μs time between $\overline{CS}$ falling edges for a throughput of 50 KSPS. It is possible, however, to use fewer than 20 clock cycles provided the timing parameters are met. With a 1-MHz SCLK, there are 2500 ns in 2.5 SCLK cycles, which is greater than t_{ACQ}. After the last data bit has come out, the clock needs one full cycle to return to a falling edge. Thus the total time between falling edges of $\overline{CS}$ is 12.5 × 1 μs + 2.5 × 1 μs + 1 × 1 μs = 16 μs which is a throughput of 62.5 KSPS.

8.4 Device Functional Modes

Figure 18 shows the device in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The device moves from hold mode to track mode (Figure 19) on the 13th rising edge of SCLK.

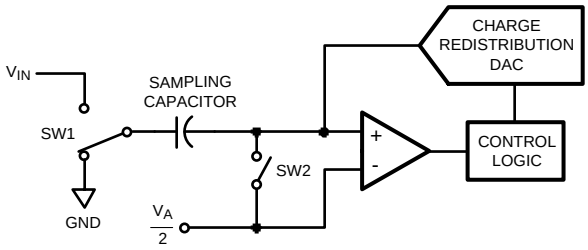


Figure 18. Hold Mode

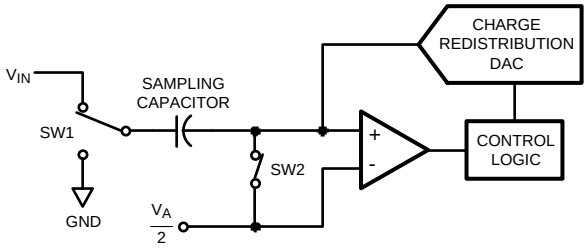


Figure 19. Track Mode

8.4.1 Transfer Function

The output format of the ADC is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC is $V_A/256$. The ideal transfer characteristic is shown in Figure 20. The transition from an output code of 0000 0000 to a code of 0000 0001 is at 1/2 LSB, or a voltage of $V_A/512$. Other code transitions occur at steps of one LSB.

Device Functional Modes (continued)

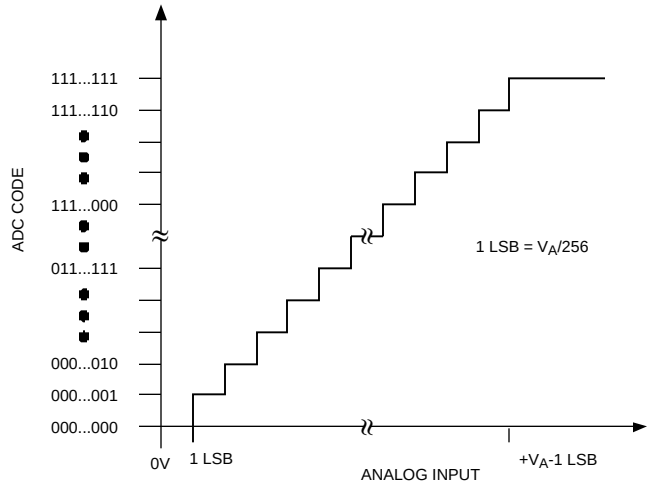


Figure 20. Ideal Transfer Characteristic

8.4.2 Modes of Operation

The ADC has two possible modes of operation: normal mode and shutdown mode. The ADC enters normal mode (and a conversion process is begun) when $\overline{CS}$ is pulled low. The device enters shutdown mode if $\overline{CS}$ is pulled high before the tenth falling edge of SCLK after $\overline{CS}$ is pulled low, or stays in normal mode if $\overline{CS}$ remains low. Once in shutdown mode, the device stays there until $\overline{CS}$ is brought low again. By varying the ratio of time spent in the normal and shutdown modes, a system may trade off throughput for power consumption, with a sample rate as low as zero.

8.4.2.1 Normal Mode

The fastest possible throughput is obtained by leaving the ADC in normal mode at all times, so there are no power-up delays. To keep the device in normal mode continuously, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK after the start of a conversion (remember that a conversion is initiated by bringing $\overline{CS}$ low).

If $\overline{CS}$ is brought high after the 10th falling edge, but before the 16th falling edge, the device remains in normal mode, but the current conversion is aborted and the SDATA returns to TRI-STATE (truncating the output word).

Sixteen SCLK cycles are required to read all of a conversion word from the device. After sixteen SCLK cycles have elapsed, $\overline{CS}$ may be idled either high or low until the next conversion. If $\overline{CS}$ is idled low, it must be brought high again before the start of the next conversion, which begins when $\overline{CS}$ is again brought low.

After sixteen SCLK cycles, SDATA returns to TRI-STATE. Another conversion may be started, after t_{QUIET} has elapsed, by bringing $\overline{CS}$ low again.

8.4.2.2 Shutdown Mode

Shutdown mode is appropriate for applications that either do not sample continuously, or it is acceptable to trade throughput for power consumption. When the ADC is in shutdown mode, all of the analog circuitry is turned off.

To enter shutdown mode, a conversion must be interrupted by bringing $\overline{CS}$ high anytime between the second and tenth falling edges of SCLK, as shown in Figure 21. Once $\overline{CS}$ has been brought high in this manner, the device enters shutdown mode, the current conversion is aborted and SDATA enters TRI-STATE. If $\overline{CS}$ is brought high before the second falling edge of SCLK, the device does not change mode; this is to avoid accidentally changing mode as a result of noise on the $\overline{CS}$ line.

Device Functional Modes (continued)

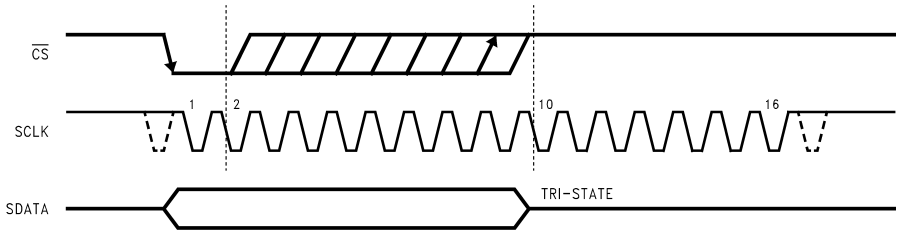


Figure 21. Entering Shutdown Mode

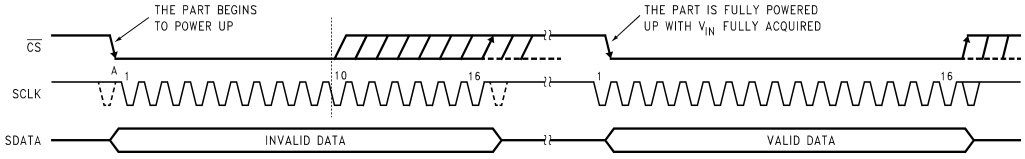


Figure 22. Entering Normal Mode

To exit shutdown mode, bring $\overline{CS}$ back low. Upon bringing $\overline{CS}$ low, the ADC begins powering up (power-up time is specified in *Timing Requirements*). This microsecond of power-up delay results in the first conversion result being unusable. The second conversion performed after power up, however, is valid, as shown in Figure 22.

If $\overline{CS}$ is brought back high before the 10th falling edge of SCLK, the device returns to shutdown mode. This is done to avoid accidentally entering normal mode as a result of noise on the $\overline{CS}$ line. To exit shutdown mode and remain in normal mode, $\overline{CS}$ must be kept low until after the 10th falling edge of SCLK. The ADC is fully powered up after 16 SCLK cycles.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application of the ADC is shown in *Typical Application*. Power is provided in this example by the Texas Instruments LP2950 low-dropout voltage regulator (see *LP295x-N Series of Adjustable Micropower Voltage Regulators*, SNVS764), available in a variety of fixed and adjustable output voltages. The power supply pin is bypassed with a capacitor network placed close to the ADC. Because the reference for the ADC is the supply voltage, any noise on the supply degrades device noise performance. To keep noise off the supply, use a dedicated linear regulator for this device, or provide sufficient decoupling from other circuitry to keep noise off the ADC supply pin. Because of the ADC's low power requirements, it is also possible to use a precision reference as a power supply to maximize performance. The three-wire interface is shown connected to a microprocessor or DSP.

9.1.1 Analog Inputs

An equivalent circuit for the ADC's input is shown in Figure 23. Diodes D1 and D2 provide ESD protection for the analog inputs. At no time must the analog input go beyond (V_A + 300 mV) or (GND − 300 mV), as these ESD diodes begin to conduct, which could result in erratic operation. For this reason, the ESD diodes must not be used to clamp the input signal.

The capacitor C1 in Figure 23 has a typical value of 4 pF, and is mainly the package pin capacitance. Resistor R1 is the ON resistance of the track or hold switch, and is typically 500 Ω. Capacitor C2 is the ADC sampling capacitor and is typically 26 pF. The ADC delivers best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. This is especially important when using the ADC to sample AC signals. Also important when sampling dynamic signals is an anti-aliasing filter.

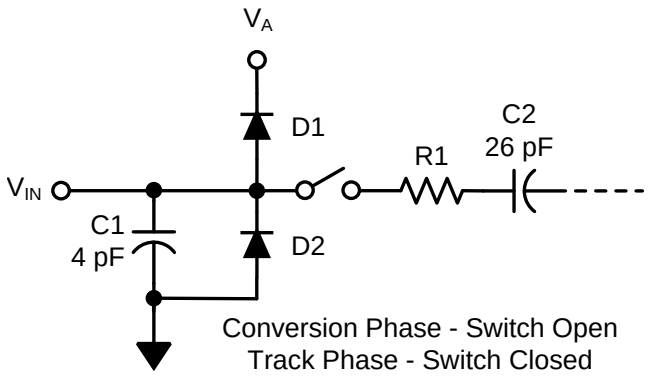


Figure 23. Equivalent Input Circuit

9.1.2 Digital Inputs and Outputs

The ADC digital inputs (SCLK and $\overline{CS}$) are not limited by the same maximum ratings as the analog inputs. The digital input pins are instead limited to 5.25 V with respect to GND, regardless of V_A, the supply voltage. This allows the ADC to be interfaced with a wide range of logic levels, independent of the supply voltage.

9.2 Typical Application

The ADC081S021 is a low-power, single-channel CMOS 8-bit analog-to-digital converter that uses the supply voltage as a reference, enabling the devices to operate with a full-scale input range of 0 to VA. An example low power application with the LMT87 which is a wide range ±0.3°C (typical) accurate temperature sensor is shown in Figure 24.

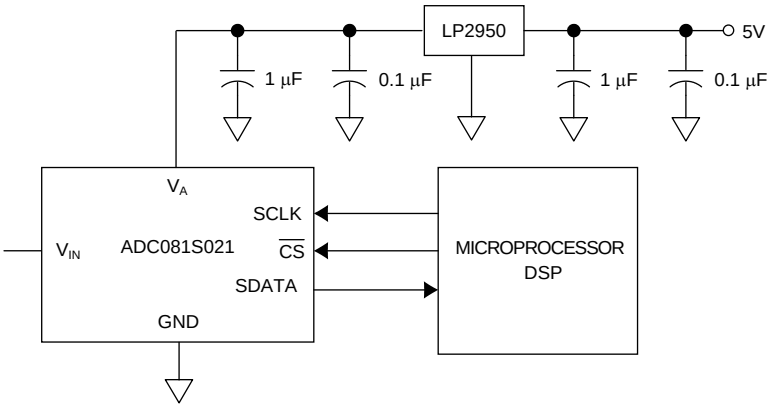


Figure 24. Typical Application Circuit

9.2.1 Design Requirements

A successful ADC081S021 and LMT87 design is contrained by the following factors:

- VIN range needs to be 0 V to VA where VA can range from 2.7 V to 5.25 V
- Output level of the LMT87 can range from 538 mV to 3277 mV (which satisfies the VIN condition)

9.2.2 Detailed Design Procedure

Designing for an accurate measurement requires careful attention to timing requirements for the ADC081S021.

Because the ADC081S021 uses the supply voltage as a reference, it is important to make sure that the supply voltage is settled to its final level before exiting the shutdown mode and beginning a conversion. After the supply voltage is settled, the $\overline{CS}$ is brought to a low level (ideally 0 V) to start a conversion.

It is also important to ensure that any noise on the power supply must be less than ½ LSB in amplitude. The supply voltage must be regarded as a precise voltage reference.

After the $\overline{CS}$ is brought low, the user needs to wait for one complete conversion cycle (approximately 1 µs) for meaningful data. The dummy conversion cycle can be considered the start-up time of the ADC081S021.

The ADC081S021 digital output can then be correlated to the LMT87 output level to get an accurate temperature reading. At VDD = 2.7 V, 1 LSB of ADC081S021 is 10.54 mV. This information can be used to calculate the output level of LMT87 which can then be correlated to temperature.

Typical Application (continued)

9.2.3 Application Curves

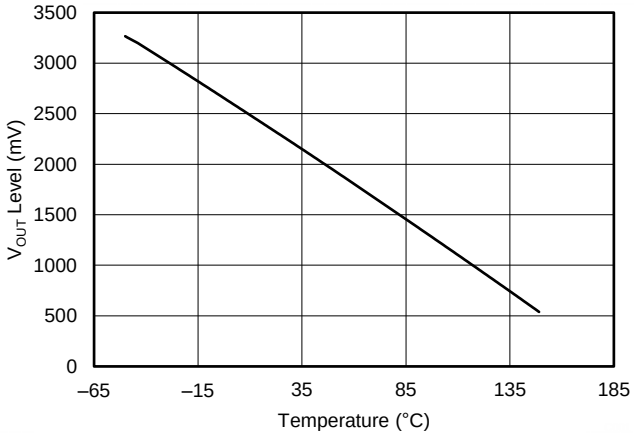


Figure 25. LMT87 Output Voltage vs Temperature

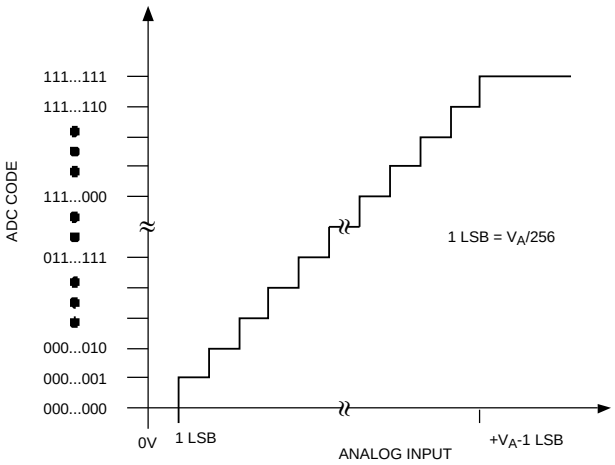


Figure 26. Ideal Transfer Characteristic

10 Power Supply Recommendations

The ADC takes time to power up, either after first applying V_A, or after returning to normal mode from shutdown mode. This corresponds to one *dummy* conversion for any SCLK frequency within the specifications in this document. After this first dummy conversion, the ADC performs conversions properly.

NOTE

The t_{QUIET} time must still be included between the first dummy conversion and the second valid conversion.

When the V_A supply is first applied, the ADC may power up in either of the two modes: normal or shutdown. As such, one dummy conversion must be performed after start-up, as described in the previous paragraph. The part may then be placed into either normal mode or the shutdown mode, as described in *Normal Mode* and *Shutdown Mode*.

When the ADC is operated continuously in normal mode, the maximum ensured throughput is f_{SCLK} / 20 at the maximum specified f_{SCLK}. Throughput may be traded for power consumption by running f_{SCLK} at its maximum specified rate and performing fewer conversions per unit time, raising the ADC $\overline{CS}$ line after the 10th and before the 15th fall of SCLK of each conversion. A plot of typical power consumption versus throughput is shown in *Typical Characteristics*. To calculate the power consumption for a given throughput, multiply the fraction of time spent in the normal mode by the normal mode power consumption and add the fraction of time spent in shutdown mode multiplied by the shutdown mode power consumption. The curve of power consumption vs throughput (Figure 17) is essentially linear. This is because the power consumption in the shutdown mode is so small that it can be ignored for all practical purposes.

10.1 Noise Considerations

The charging of any output load capacitance requires current from the power supply, V_A. The current pulses required from the supply to charge the output capacitance causes voltage variations on the supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, discharging the output capacitance when the digital output goes from a logic high to a logic low dumps current into the die substrate, which is resistive. Load discharge currents cause *ground bounce* noise in the substrate that degrades noise performance if that current is large enough. The larger the output capacitance, the more current flows through the die substrate and the greater is the noise coupled into the analog channel, degrading noise performance.

To keep noise out of the power supply, keep the output load capacitance as small as practical. It is good practice to use a 100-Ω series resistor at the ADC output, placed as close to the ADC output pin as practical. This limits the charge and discharge current of the output capacitance and maintain noise performance.

11 Layout

11.1 Layout Guidelines

Capacitive coupling between noisy digital circuitry and sensitive analog circuitry can lead to poor performance. TI strongly recommends keeping the analog and digital circuitry separated from each other and the clock line as short as possible.

Digital circuits create substantial supply and ground current transients. This digital noise could have significant impact upon system noise performance. To avoid performance degradation due to supply noise, do not use the same supply for the ADC081S021 that is used for digital logic.

Generally, analog and digital lines must cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether. It is important to keep clock lines as short as possible and isolated from ALL other lines, including other digital lines. In addition, the clock line must also be treated as a transmission line and be properly terminated.

The analog input must be isolated from noisy signal lines to avoid coupling of spurious signals into the input. Any external component (that is, a filter capacitor) connected between the converter's input pins and ground or to the reference input pin and ground must be connected to a very clean point in the ground plane.

Layout Guidelines (continued)

TI recommends the use of a single, uniform ground plane and the use of split power planes. The power planes must be placed within the same board layer. All analog circuitry (input amplifiers, filters, reference components, and so on) must be placed over the analog power plane. All digital circuitry and I/O lines must be placed over the digital power plane. In addition, all components in the reference circuitry and the input signal chain that are connected to ground must be connected together with short traces and enter the analog ground plane at a single, quiet point.

11.2 Layout Example

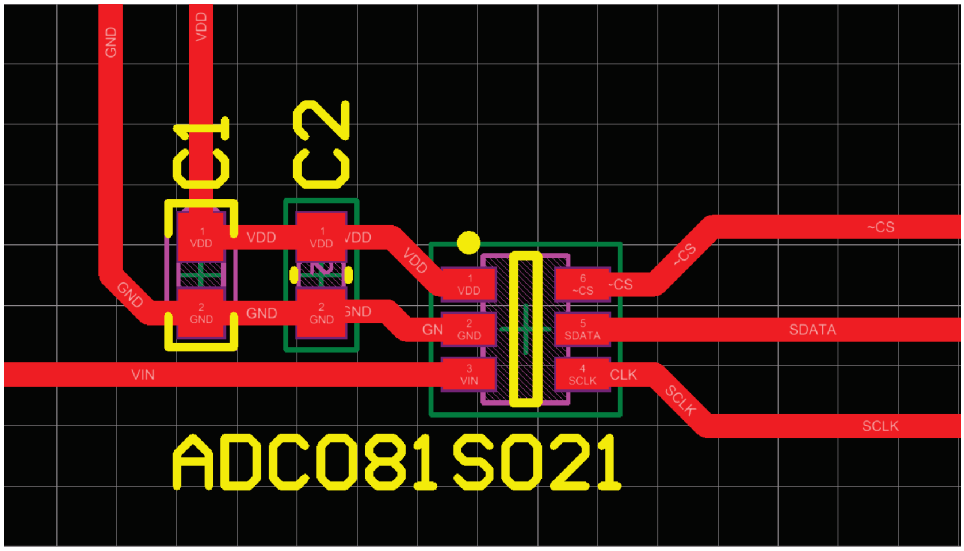


Figure 27. DBV Package Layout

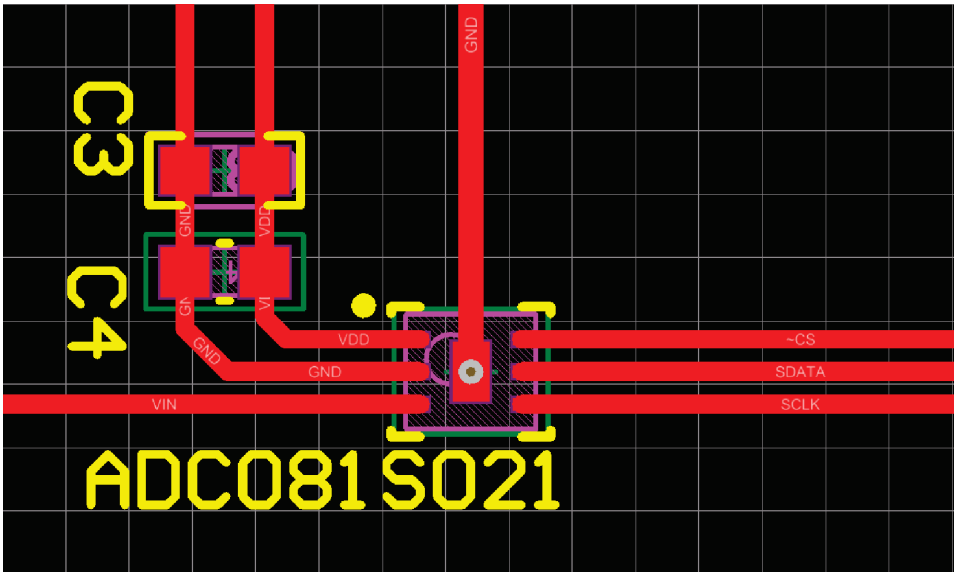


Figure 28. NGF Package Layout

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デバイスの関連用語

アクイジション時間 は、入力電圧を取得するため必要な時間です。これは、ホールド・コンデンサが入力電圧まで充電されるため必要な時間です。アクイジション時間は、信号がサンプリングされ、その部分がトラックからホールドへ移動するとき、$\overline{CS}$の立ち下がりエッジから逆方向に測定されます。T_{ACQ}を含む時間インターバルの開始は、その部分がホールドからトラックへ移動するときの、前の変換におけるSCLKの13番目の立ち上がりエッジです。ユーザーは、パフォーマンス仕様を満たすため、SCLKの13番目の立ち上がりエッジと、次の$\overline{CS}$の立ち下がりエッジとの間の時間がT_{ACQ}を下回らないことを保証する必要があります。

アパーチャ遅延 は、入力信号が取得されるか、変換用にホールドされるときの、$\overline{CS}$の立ち下がりエッジ以後の時間です。

アパーチャ・ジッタ(アパーチャの不安定性) は、サンプル間でのアパーチャ遅延の偏差です。アパーチャ・ジッタは、出力にノイズとして現れます。

変換時間 は、入力電圧が取得されてから、ADC081S021によって入力電圧がデジタルのワードへ変換されるまでに必要な時間です。これは、入力信号がサンプリングされる$\overline{CS}$の立ち下がりエッジから、SDATA出力がTRI-STATEへ移行するSCLKの16番目の立ち下がりエッジまでを意味します。

差動非直線性(DNL) は、理想的なステップ・サイズである1 LSBからの最大偏差の測定値です。

デューティ・サイクル は、繰り返しのデジタル波形が1周期の合計時間のうちHIGHになる時間の割合です。ここでは、SCLKを基準とします。

実効ビット数(ENOBまたはEFFECTIVE BITS) は、信号対ノイズ+歪み比率(SINAD)を規定する別の方法です。ENOBは(SINAD - 1.76) / 6.02で定義され、コンバータがこの(ENOB)ビット数を持つ完全なADC081S021と等価であることを示します。

フルパワー帯域幅 は、再構築された出力基本波が、フルスケール入力について、低周波数の値より3dB低下する周波数の測定値です。

ゲイン誤差 は、最後のコード遷移[(111...110)から(111...111)]が、オフセット誤差の調整後に、理想値(V_{REF} - 1 LSB)とどれだけ差異があるかを示します。

積分非直線性(INL) は、それぞれのコードが、負のフルスケール(最初のコード遷移より½ LSBだけ下)と正のフルスケール(最後のコード遷移より½ LSBだけ上)との間に引かれた直線との間にどれだけ差異があるかの測定値です。任意のコードについて、この直線からの差異は、そのコード値の中間から測定されます。

相互変調歪み(IMD) は、2つの正弦周波数が同時にADC081S021の入力へ印加されたとき、その結果として新たなスペクトル成分が発生することです。2次および3次相互変調積の電力と、元の周波数における両方の電力の合計との比率と定義されます。IMDは通常、dB単位で表記されます。

欠損コード は、ADC081S021の出力に一切出現しない出力コードです。ADC081S021には、欠損コードが存在しないことが保証されています。

オフセット誤差 は、最初のコード遷移[(000...000)から(000...001)]と、理想値(すなわち、GND + 1 LSB)との差異です。

信号対ノイズ比(SNR) は、入力信号のRMS値と、サンプリング周波数の半分より低い他のすべてのスペクトル成分(高調波やDCは含まれません)の合計のRMS値との比率で、dB単位で表記されます。

信号対ノイズ+歪み比率(S/N+DまたはSINAD) は、入力信号のRMS値と、クロック周波数の半分より低い他のすべてのスペクトル成分(高調波を含みますが、DCは含まれません)のRMS値との比率で、dB単位で表記されます。

デバイス・サポート (continued)

スプリアス・フリー・ダイナミック・レンジ（**SFDR**）は、信号の望ましい振幅と、ピークのスプリアス・スペクトル成分の振幅との差で、dB単位で表記されます。ここでのスプリアス・スペクトル成分は、出力スペクトルに存在し、入力には存在しないすべての信号を指し、高調波の場合も、そうでない場合も含まれます。

全高調波歪み**(THD)** は、出力における最初の5つの高調波成分の合計RMSと、出力において観測される入力信号周波数のRMSレベルとの比で、dBまたはdBc単位で表記されます。THD

$$THD = 20 \cdot \log_{10} \sqrt{\frac{A_{f2}^2 + \cdots + A_{f6}^2}{A_{f1}^2}}$$

は で計算されます。ここで、A_{f1}は出力における入力周波数のRMS電力、A_{f2}からA_{f6}までは最初の5つの高調波周波数のRMS電力です。

スループット時間 は、2つの連続する変換の開始の間に必要な最小時間です。これは、アクイジション時間と変換時間の和です。

全未調整誤差 は、理想的な伝達関数からの、検出された最大の偏差です。このため、この値はフルスケール誤差、直線性誤差、オフセット誤差を含む包括的な仕様です。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください：

『LP295x-Nシリーズ 可変マイクロパワー電圧レギュレータ』、SNVS764

12.3 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 商標

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12.5 静電気放電に関する注意事項

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12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADC081S021CIMF/NO.A	Active	Production	SOT-23 (DBV) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X09C
ADC081S021CIMF/NOPB	Active	Production	SOT-23 (DBV) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X09C
ADC081S021CIMFX/NO.A	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X09C
ADC081S021CIMFX/NOPB	Active	Production	SOT-23 (DBV) | 6	3000 | LARGE T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X09C
ADC081S021CISD/NO.A	Active	Production	WSON (NGF) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X9C
ADC081S021CISD/NOPB	Active	Production	WSON (NGF) | 6	1000 | SMALL T&R	Yes	SN	Level-1-260C-UNLIM	-40 to 85	X9C

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

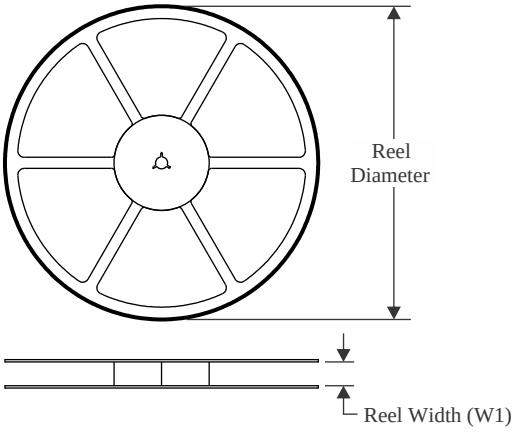
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

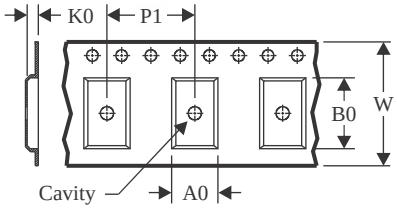
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

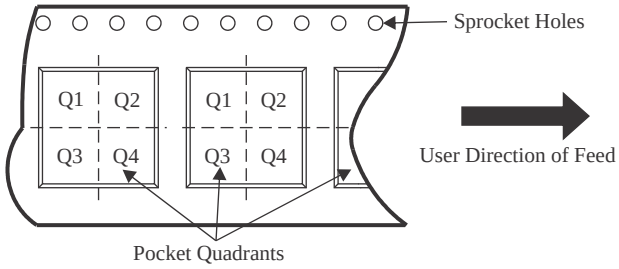


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

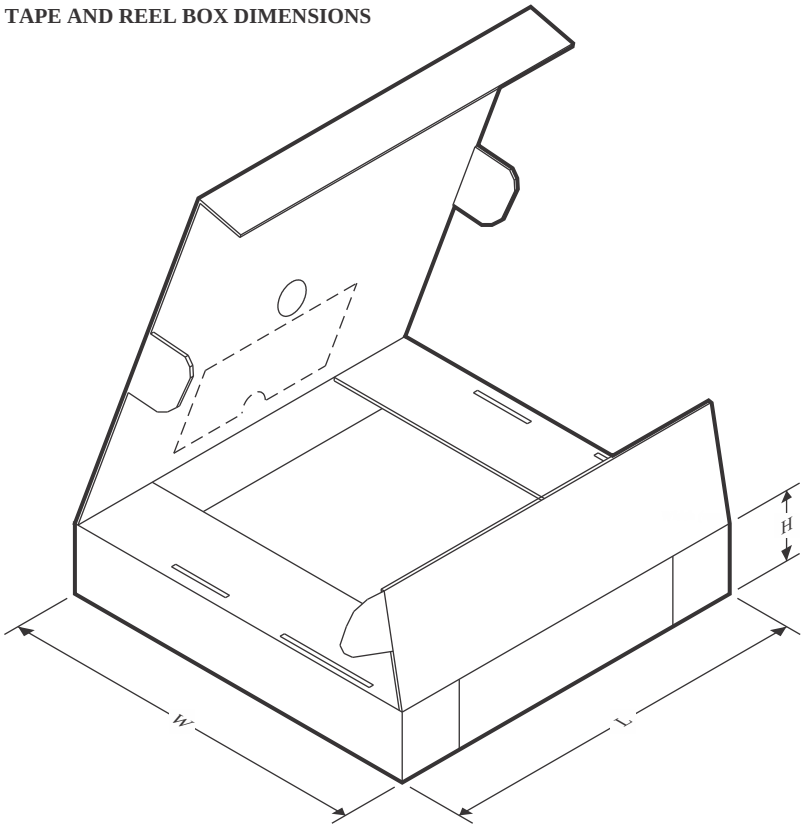
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADC081S021CIMF/NOPB	SOT-23	DBV	6	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADC081S021CIMFX/ NOPB	SOT-23	DBV	6	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
ADC081S021CISD/NOPB	WSON	NGF	6	1000	177.8	12.4	2.8	2.5	1.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

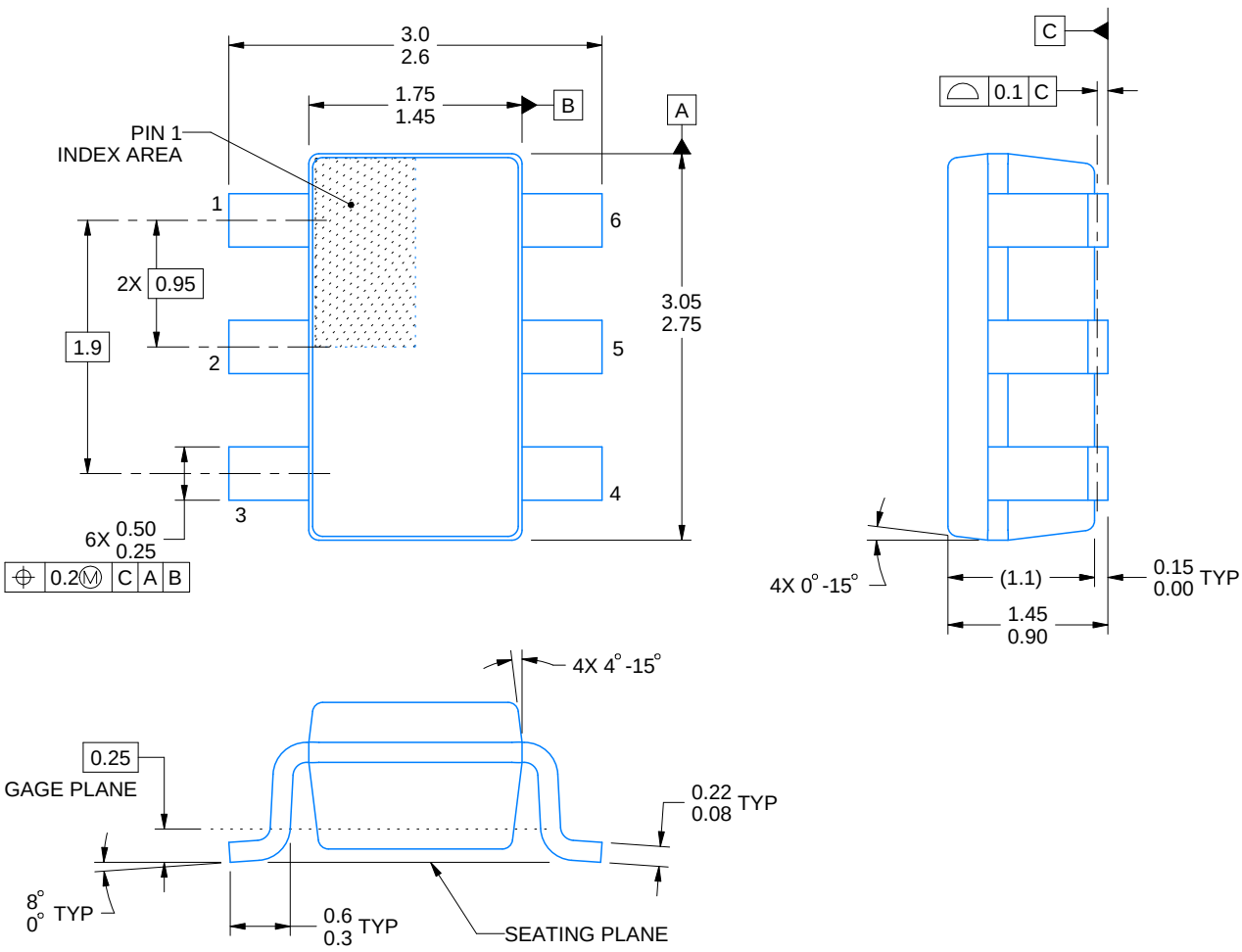
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADC081S021CIMF/NOPB	SOT-23	DBV	6	1000	210.0	185.0	35.0
ADC081S021CIMFX/ NOPB	SOT-23	DBV	6	3000	210.0	185.0	35.0
ADC081S021CISD/NOPB	WSON	NGF	6	1000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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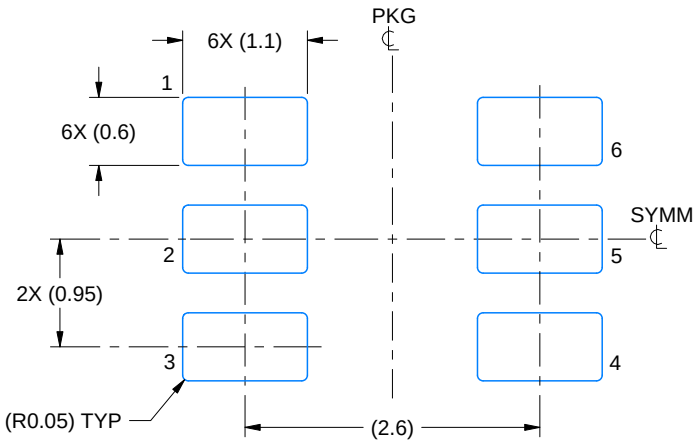
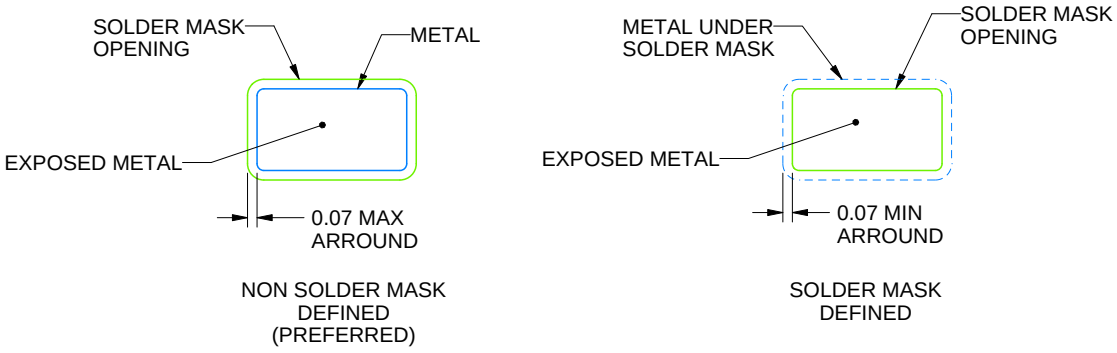
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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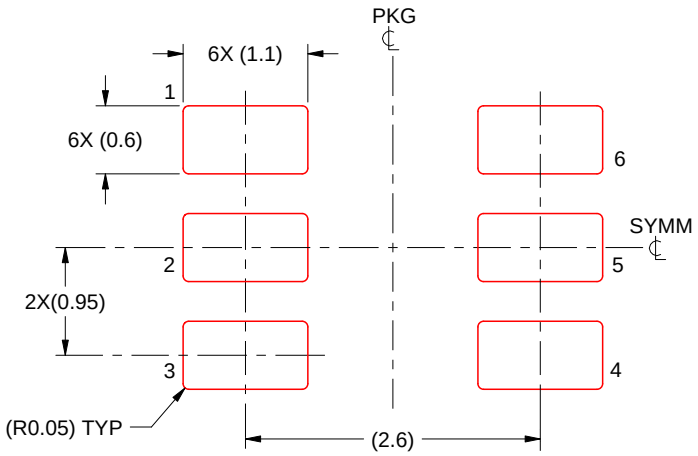
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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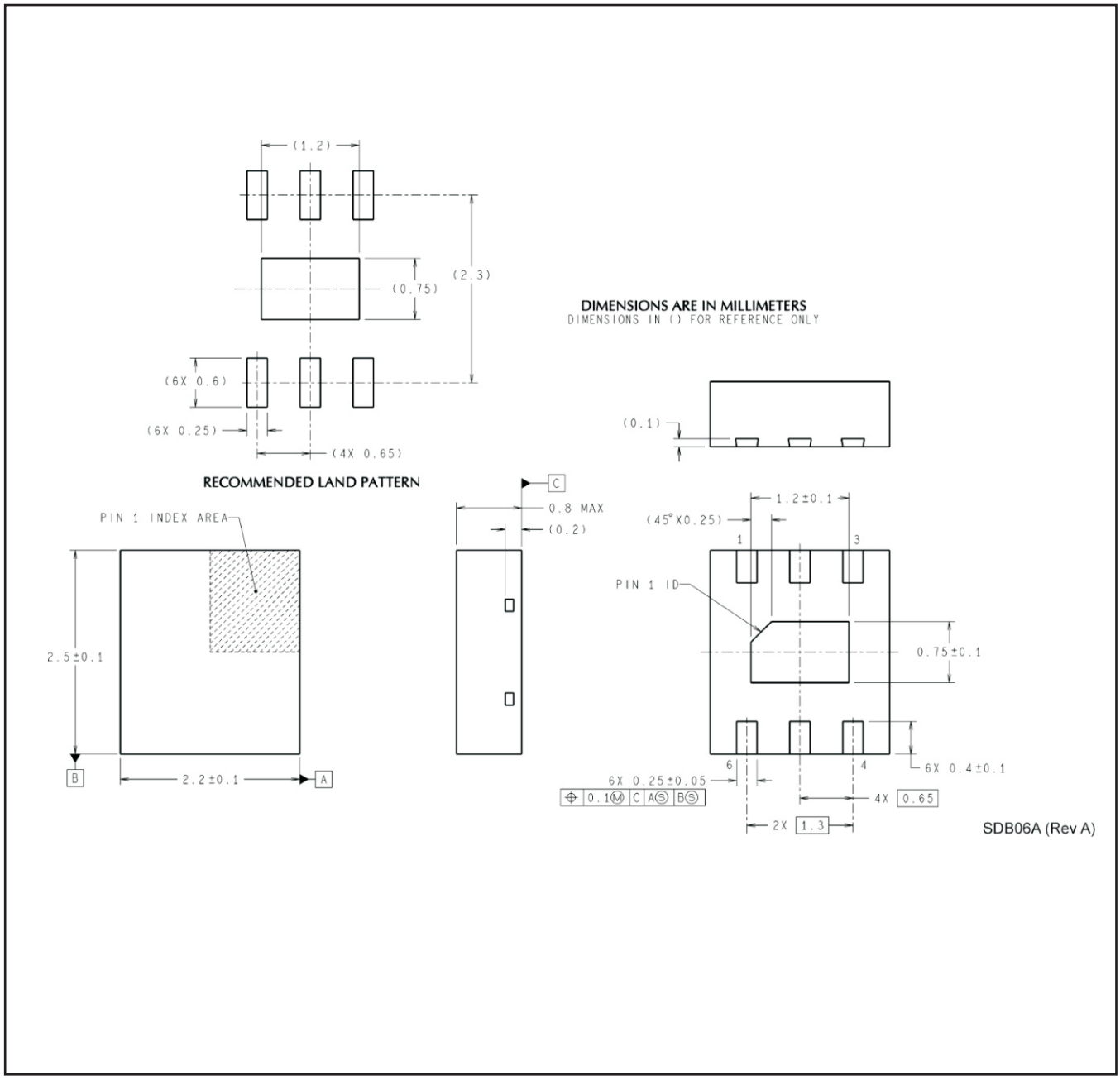
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

NGF0006A


(1.2)
(2.3)
(0.75)
(6X 0.6)
(6X 0.25)
(4X 0.65)
RECOMMENDED LAND PATTERN
DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY
(0.1)
PIN 1 INDEX AREA
2.5±0.1
2.2±0.1
B
A
C
0.8 MAX
(0.2)
1.2±0.1
(45°X0.25)
1
3
PIN 1 ID
0.75±0.1
6
4
6X 0.4±0.1
6X 0.25±0.05
0.10 M C A S B S
4X 0.65
2X 1.3
SDB06A (Rev A)

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