TEXAS INSTRUMENTS
TIC10024-Q1
JAJSDS2A – SEPTEMBER 2017 – REVISED FEBRUARY 2022

# TIC10024-Q1 24 入力マルチ・スイッチ検出インターフェイス (MSDI) デバイス 車載システム向け、可変ウェット電流対応

## 1 特長

- 車載アプリケーション認定済み
- 下記内容で AEC-Q100 認定済み
  - デバイス温度グレード 1:–40℃～125℃の動作時周囲温度範囲
  - デバイス HBM ESD 分類レベル H2
  - デバイス CDM ESD 分類レベル C4B
- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 過電圧および低電圧警告により、12V 車載システムをサポートするように設計
- 最大 24 の直接スイッチ入力を監視し、そのうち 10 の入力はグランドまたはバッテリに接続されているスイッチを監視するよう構成可能
- スイッチ入力耐性は 40V (ロードダンプ状態)～–24V (逆極性状態)
- 設定可能な 6 つのウェット電流設定:
  (0mA、1mA、2mA、5mA、10mA、15mA)
- デジタル・スイッチ監視用に 4 つのプログラマブル・スレッショルドを備えた内蔵コンパレータ
- 非常に小さいポーリング・モード動作電流:
  68µA (標準値、$t_{POLL}$ = 64ms、$t_{POLL\_ACT}$ = 128µs、24 の全入力がアクティブ、コンパレータ・モード、全スイッチがオープン)
- 3.3V/5V のシリアル・ペリフェラル・インターフェイス (SPI) プロトコルを使用して MCU に直接接続
- 割り込み生成により、すべての入力でウェークアップ動作をサポート
- 適切な外付け部品を使うことで、ISO-10605 に準拠した ESD 保護 (入力ピン、±8kV の接触放電) を実現可能
- 38 ピン TSSOP パッケージ

## 2 アプリケーション

- ボディ・コントロール・モジュールとゲートウェイ
- 車載ライティング
- 冷 暖房
- パワー・シート
- ミラー

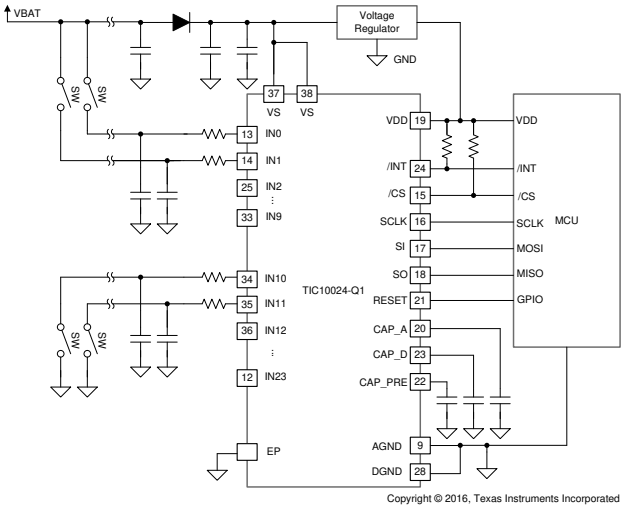
## 3 概要

TIC10024-Q1 は、12V 車載システムで外付けスイッチの状態を検出するように設計された、先進的なマルチ・スイッチ検出インターフェイス (MSDI) です。TIC10024-Q1 は、可変スレッショルドを備えたコンパレータにより、MCU から独立してデジタル・スイッチを監視します。このデバイスは、最大 24 の直接スイッチ入力を監視し、そのうち 10 の入力はグランドまたはバッテリに接続されているスイッチを監視するよう構成できます。各種のアプリケーション・シナリオに対応するため、各入力に 6 つの固有のウェット電流設定をプログラムできます。このデバイスは、すべてのスイッチ入力でウェークアップ動作をサポートするため、MCU を継続的にアクティブにしておく必要がなくなり、システムの消費電力を削減できます。また TIC10024-Q1 には、フォルト検出機能と ESD 保護機能が統合されているため、システムの安定性も向上します。TIC10024-Q1 は、連続モードとポーリング・モードという 2 つの動作モードをサポートしています。連続モードでは、ウェット電流が連続的に供給されます。ポーリング・モードでは、プログラマブル・タイマに基づいてウェット電流が定期的にオンになり、入力状態をサンプリングするため、システムの消費電力を大幅に削減できます。

**製品情報**

| 部品番号 | パッケージ(1) | 本体サイズ (公称) |
|---|---|---|
| TIC10024-Q1 | TSSOP (38) | 9.70mm × 4.40mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**概略回路図**

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## 4 Revision History

| Changes from Revision * (September 2017) to Revision A (February 2022) | Page |
|---|---|
| • 「*特長*」に「機能安全対応」を追加 | 1 |
| • すべての古い用語をコントローラおよびレスポンダに変更 | 1 |
| • Changed the paragraph following 表 8-3 for CRC calculations | 25 |

# 5 Pin Configuration and Functions

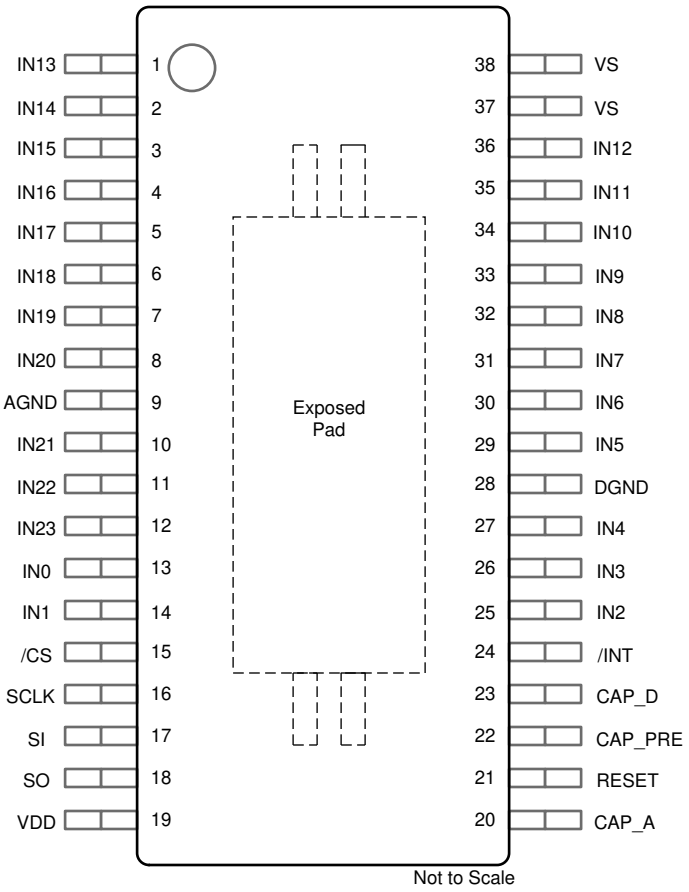



**図 5-1. DCP (TSSOP) Package, 38-Pin, Top View**

**表 5-1. Pin Functions**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | IN13 | I/O | Ground switch monitoring input with current source |
| 2 | IN14 | I/O | Ground switch monitoring input with current source |
| 3 | IN15 | I/O | Ground switch monitoring input with current source |
| 4 | IN16 | I/O | Ground switch monitoring input with current source |
| 5 | IN17 | I/O | Ground switch monitoring input with current source |
| 6 | IN18 | I/O | Ground switch monitoring input with current source |
| 7 | IN19 | I/O | Ground switch monitoring input with current source |
| 8 | IN20 | I/O | Ground switch monitoring input with current source |
| 9 | AGND | P | Ground for analog circuitry |
| 10 | IN21 | I/O | Ground switch monitoring input with current source |
| 11 | IN22 | I/O | Ground switch monitoring input with current source |
| 12 | IN23 | I/O | Ground switch monitoring input with current source |
| 13 | IN0 | I/O | Ground/$V_{BAT}$ switch monitoring input with configurable current sink or source. |
| 14 | IN1 | I/O | Ground/$V_{BAT}$ switch monitoring input with configurable current sink or source. |
| 15 | $\overline{CS}$ | I | Active-low input. Chip select from the commander for the SPI Interface. |
| 16 | SCLK | I | Serial clock output from the commander for the SPI Interface |

**表 5-1. Pin Functions (continued)**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 17 | SI | I | Serial data input for the SPI Interface. |
| 18 | SO | O | Serial data output for the SPI Interface |
| 19 | $V_{DD}$ | P | 3.3 V to 5 V logic supply for the SPI communication. The SPI I/Os are not fail-safe protected: VDD needs to be present during any SPI traffic to avoid excessive leakage currents and corrupted SPI I/O logic levels. |
| 20 | CAP_A | I/O | External capacitor connection for the analog LDO. Use capacitance value of 100nF. |
| 21 | RESET | I | Keep RESET low for normal operation and drive RESET high and release it to perform a hardware reset of the device. The RESET pin is connected to ground via a 1MΩ pull-down resistor. If not used, the RESET pin shall be grounded to avoid any accidental device reset due to coupled noise onto this pin. |
| 22 | CAP_Pre | I/O | External capacitor connection for the pre-regulator. Use capacitance value of 1 µF. |
| 23 | CAP_D | I/O | External capacitor connection for the digital LDO. Use capacitance value of 100 nF. |
| 24 | $\overline{INT}$ | O | Open drain output. Pulled low (internally) upon change of state on the input or occurrence of a special event. |
| 25 | IN2 | I/O | Ground/$V_{BAT}$ switch monitoring input with configurable current sink or source. |
| 26 | IN3 | I/O | Ground/$V_{BAT}$ switch monitoring input with configurable current sink or source. |
| 27 | IN4 | I/O | Ground/$V_{BAT}$ switch monitoring input with configurable current sink or source. |
| 28 | DGND | P | Ground for digital circuitry |
| 29 | IN5 | I/O | Ground/$V_{BAT}$ switch monitoring input with configurable current sink or source. |
| 30 | IN6 | I/O | Ground/$V_{BAT}$ switch monitoring input with configurable current sink or source. |
| 31 | IN7 | I/O | Ground/$V_{BAT}$ switch monitoring input with configurable current sink or source. |
| 32 | IN8 | I/O | Ground/$V_{BAT}$ switch monitoring input with configurable current sink or source. |
| 33 | IN9 | I/O | Ground/$V_{BAT}$ switch monitoring input with configurable current sink or source. |
| 34 | IN10 | I/O | Ground switch monitoring input with current source |
| 35 | IN11 | I/O | Ground switch monitoring input with current source |
| 36 | IN12 | I/O | Ground switch monitoring input with current source |
| 37 | $V_S$ | P | Power supply input pin. |
| 38 | $V_S$ | P | Power supply input pin. |
| --- | EP | P | Exposed Pad. The exposed pad is not electrically connected to AGND or DGND. Connect EP to the board ground to achieve rated thermal and ESD performance. |

(1) I = input, O = output, I/O = input and output, P = power.

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Input voltage | $V_S$, $\overline{INT}$ | -0.3 | 40(2) | V |
| | $V_{DD}$, SCLK, SI, SO, $\overline{CS}$, RESET | -0.3 | 6 | V |
| | IN0- IN23 | -24 | 40(2) | V |
| | CAP_Pre | -0.3 | 5.5 | V |
| | CAP_A | -0.3 | 5.5 | V |
| | CAP_D | -0.3 | 2 | V |
| Operating junction temperature, $T_J$ | | -40 | 150 | °C |
| Storage temperature, $T_{stg}$ | | -55 | 155 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Tested for load dump and jump start conditions with nominal operating voltage no greater than 16 V for the life of a 12-V automotive system. Refer to Using TIC10024-Q1 in a 12 V Automotive System for more details.

## 6.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002(1) | All pins | ±2000 | V |
| | | | Pins IN0-IN23(2) | ±4000 | |
| | | Charged-device model (CDM), per AEC Q100-011 | All pins | ±500 | |
| | | | Corner pins (pin 1, 19, 20 and 38) | ±750 | |
| | | Contact discharge, un-powered, per ISO- 10605(3) (5) | Pins IN0-IN23 | ±8000 | |
| | | Contact discharge, powered-up, per ISO- 10605 (4) (6) | Pins IN0-IN23 | ±8000 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.
(2) ±4kV rating on pins IN0-IN23 are stressed with respect to GND (with AGND, DGND, and EP tied together).
(3) External components: capacitor = 15 nF; resistor = 10 Ω
(4) External components: capacitor = 15 nF; resistor = 33 Ω
(5) ESD generator parameters: storage capacitance = 150 pF; discharge resistance = 330 Ω or 2000 Ω
(6) ESD generator parameters: storage capacitance = 150 pF or 330pF; discharge resistance = 330 Ω or 2000 Ω

## 6.3 Recommended Operating Conditions

over operating free-air temperature range and $V_S$ = 12 V (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_S$ | Power supply voltage | 4.5 | | 35 (2) | V |
| $V_{DD}$ | Logic supply voltage | 3.0 | | 5.5 | V |
| $V_{/INT}$ | $\overline{INT}$ pin voltage | 0 | | 35(2) | V |
| $V_{INX}$ | IN0 to IN23 input voltage | 0 | | 35(2) | V |
| $V_{RESET}$ | RESET pin voltage | 0 | | 5.5 | V |
| $V_{SPI\_IO}$ | SPI input/output logic level | 0 | | $V_{DD}$ | V |
| $f_{SPI}$ | SPI communication frequency | 20(1) | | 4M | Hz |
| $T_A$ | Operating free-air temperature | -40 | | 125 | °C |

(1) Lowest frequency characterized.
(2) Tested for load dump and jump start conditions with nominal operating voltage no greater than 16 V for the life of a 12-V automotive system. Refer to Using TIC10024-Q1 in a 12 V Automotive System for more details.

## 6.4 Thermal Information

| THERMAL METRIC(1) | | TIC10024-Q1 DCP (TSSOP) 38 PINS | UNIT |
|---|---|---|---|
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 33.6 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 18.4 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 15.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 0.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 15.0 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 1.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

## 6.5 Electrical Characteristics

over operating free-air temperature range, $V_S$ = 4.5 V to 35 V, and $V_{DD}$ = 3 V to 5.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **POWER SUPPLY** | | | | | | | |
| $I_{S\_CONT}$ | Continuous mode $V_S$ power supply current | Continuous mode, $I_{WETT}$= 10 mA, all switches open, no active comparator operation, no unserviced interrupt | | | 5.6 | 7 | mA |
| $I_{S\_POLL\_COMP\_25}$ | Polling mode $V_S$ power supply average current | $T_A$= 25° | Polling mode, $t_{POLL}$= 64 ms, $t_{POLL}$_ACT= 128 µs, all switches open, $I_{WETT}$= 10 mA, no unserviced interrupt | | 68 | 100 | µA |
| $I_{S\_POLL\_COMP\_85}$ | | $T_A$= -40° to 85°C | | | 68 | 110 | µA |
| $I_{S\_POLL\_COMP}$ | | $T_A$= -40° to 125°C | | | 68 | 170 | µA |
| $I_{S\_RESET}$ | Reset mode $V_S$ power supply current | Reset mode, $V_{RESET}$= $V_{DD}$. $V_S$= 12 V, all switches open, $T_A$=25°C | | | 12 | 17 | µA |
| $I_{S\_IDLE\_25}$ | $V_S$ power supply average current in idle state | TRIGGER bit in CONFIG register = logic 0, $T_A$= 25°C, no unserviced interrupt | | | 50 | 75 | µA |
| $I_{S\_IDLE\_85}$ | | TRIGGER bit in CONFIG register = logic 0, $T_A$= -40°C to 85°C, no unserviced interrupt | | | 50 | 95 | µA |
| $I_{S\_IDLE}$ | | TRIGGER bit in CONFIG register = logic 0, $T_A$= -40°C to 125°C, no unserviced interrupt | | | 50 | 145 | µA |
| $I_{DD}$ | Logic supply current from $V_{DD}$ | SCLK = SI = 0 V, $\overline{CS}$ = $\overline{INT}$ = $V_{DD}$, no SPI communication | | | 1.5 | 10 | µA |
| $V_{POR\_R}$ | Power on reset (POR) voltage for $V_S$ | Threshold for rising $V_S$ from device OFF condition resulting in $\overline{INT}$ pin assertion and a flagged POR bit in the INT_STAT register | | 3.85 | | 4.5 | V |
| $V_{POR\_F}$ | | Threshold for falling $V_S$ from device normal operation to reset mode and loss of SPI communication | | 1.95 | | 2.8 | V |
| $V_{OV\_R}$ | Over-voltage (OV) condition for $V_S$ | Threshold for rising $V_S$ from device normal operation resulting in $\overline{INT}$ pin assertion and a flagged OV bit in the INT_STAT register | | 35 | | 40 | V |
| $V_{OV\_HYST}$ | Over-voltage (OV) condition hysteresis for $V_S$ | | | 1 | | 3.5 | V |
| $V_{UV\_R}$ | Under-voltage (UV) condition for $V_S$ | Threshold for rising $V_S$ from under-voltage condition resulting in $\overline{INT}$ pin assertion and a flagged UV bit in the INT_STAT register | | 3.85 | | 4.5 | V |
| $V_{UV\_F}$ | | Threshold for falling $V_S$ from under-voltage condition resulting in $\overline{INT}$ pin assertion and a flagged UV bit in the INT_STAT register | | 3.7 | | 4.4 | V |
| $V_{UV\_HYST}$ | Under-voltage (UV) condition hysteresis for $V_S$ (1) | | | 75 | | 275 | mV |
| $V_{DD\_F}$ | | Threshold for falling $V_{DD}$ resulting in loss of SPI communication | | 2.5 | | 2.9 | V |
| $V_{DD\_HYST}$ | Valid $V_{DD}$ voltage hysteresis | | | 50 | | 150 | mV |

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range, $V_S$ = 4.5 V to 35 V, and $V_{DD}$ = 3 V to 5.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **WETTING CURRENT ACCURACY (DIGITAL SWITCHES, MAXIMUM RESISTANCE VALUE WITH SWITCH CLOSED ≤ 100Ω , MINIMUM RESISTANCE VALUE WITH SWITCH OPEN ≥ 5000 Ω)** | | | | | | | |
| $I_{WETT}$ (CSO) | Wetting current accuracy for CSO (switch closed) | 1 mA setting | 4.5 V ≤ $V_S$ ≤ 35 V | 0.84 | 1 | 1.14 | mA |
| | | 2 mA setting | | 1.71 | 2 | 2.32 | |
| | | 5 mA setting | 4.5 V ≤ $V_S$ < 5 V | 2.39 | | 5.5 | |
| | | | 5 V ≤ $V_S$ ≤ 35 V | 4.3 | 5 | 5.6 | |
| | | 10 mA setting | 4.5 V ≤ $V_S$ < 6 V | 2.4 | | 11 | |
| | | | 6 V ≤ $V_S$ ≤ 35 V | 8.4 | 10 | 11.4 | |
| | | 15 mA setting | 4.5 V ≤ $V_S$ < 6.5 V | 2.4 | | 16.5 | |
| | | | 6.5 V ≤ $V_S$ ≤ 35 V | 12.5 | 15 | 17 | |
| $I_{WETT}$ (CSI) | Wetting current accuracy for CSI (switch closed) | 1 mA setting | 4.5 V ≤ $V_S$ ≤ 35 V | 0.75 | 1.1 | 2.05 | mA |
| | | 2 mA setting | | 1.6 | 2.2 | 3.3 | |
| | | 5 mA setting | | 4.3 | 5.6 | 7.1 | |
| | | 10 mA setting | | 9.2 | 11.5 | 13.4 | |
| | | 15 mA setting | 4.5 V ≤ $V_S$ < 6 V | 11 | 16.5 | 19.2 | |
| | | | 6 V ≤ $V_S$ ≤ 35V | 13.7 | 16.5 | 19.2 | |
| $V_{CSI\_DROP\_OPEN}$ | Voltage drop from $IN_x$ pin to AGND across CSI (switch open) | 10 mA setting, $R_{SW}$= 5kΩ | 4.5 V ≤ $V_S$ ≤ 35V | | | 1.7 | V |
| | | 15 mA setting, $R_{SW}$= 5kΩ | | | | 1.7 | |
| $V_{CSI\_DROP\_CLOSED}$ | Voltage drop from INx pin to ground across CSI (switch closed) | 2mA setting, $I_{IN}$= 1mA (4.5V ≤ VS ≤ 35V) | 4.5 V ≤ $V_S$ ≤ 35V | | | 1.2 | V |
| | | 5mA setting, $I_{IN}$= 1mA or 2mA | | | | 1.3 | V |
| | | 10mA setting, $I_{IN}$= 1mA, 2mA, or 5mA | | | | 1.5 | V |
| | | 15mA setting, $I_{IN}$= 1mA, 2mA, 5mA, or 10mA | | | | 2.1 | V |
| **LEAKAGE CURRENTS** | | | | | | | |
| $I_{IN\_LEAK\_OFF}$ | Leakage current at input INx when channel is disabled | 0 V ≤ $V_{INx}$ ≤ $V_S$ , channel disabled (EN_INx register bit= logic 0) | | -4 | | 5.3 | µA |
| $I_{IN\_LEAK\_OFF\_25}$ | | 0 V ≤ $V_{INx}$ ≤ $V_S$ , channel disabled (EN_INx register bit= logic 0), $T_A$ = 25°C | | -0.5 | | 0.5 | |
| $I_{IN\_LEAK\_0mA}$ | Leakage current at input INx when wetting current setting is 0mA | 0 V ≤ $V_{INx}$ ≤ 6 V, 6 V ≤ $V_S$ ≤ 35 V , $I_{WETT}$ setting = 0 mA | | -110 | | 110 | µA |
| | | | | | | | µA |
| $I_{IN\_LEAK\_LOSS\_OF\_GND}$ | Leakage current at input INx under loss of GND condition | $V_S$ = 24 V, 0 V ≤ $V_{INx}$ ≤ 24 V, all grounds (AGND, DGND, and EP) = 24 V, $V_{DD}$ shorted to the grounds(1) | | -5 | | | µA |
| $I_{IN\_LEAK\_LOSS\_OF\_VS}$ | Leakage current at input INx under loss of $V_S$ condition | 0 V ≤ $V_{INx}$ ≤ 24 V, $V_S$ shorted to the grounds = 0 V, $V_{DD}$ = 0 V | | | | 5 | µA |
| **LOGIC LEVELS** | | | | | | | |
| $V_{/INT\_L}$ | $\overline{INT}$ output low voltage | $I_{/INT}$ = 2 mA | | | | 0.35 | V |
| | | $I_{/INT}$ = 4 mA | | | | 0.6 | |
| $V_{SO\_L}$ | SO output low voltage | $I_{SO}$ = 2 mA | | | | 0.2$V_{DD}$ | V |
| $V_{SO\_H}$ | SO output high voltage | $I_{SO}$ = -2 mA | | 0.8$V_{DD}$ | | | V |
| $V_{IN\_L}$ | SI, SCLK, and $\overline{CS}$ input low voltage | | | | | 0.3$V_{DD}$ | V |
| $V_{IN\_H}$ | SI, SCLK, and $\overline{CS}$ input high voltage | | | 0.7$V_{DD}$ | | | V |
| $V_{RESET\_L}$ | RESET input low voltage | | | | | 0.8 | V |

## 6.5 Electrical Characteristics (continued)

over operating free-air temperature range, $V_S$ = 4.5 V to 35 V, and $V_{DD}$ = 3 V to 5.5 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{RESET\_H}$ | RESET input high voltage | | 1.6 | | | V |
| $R_{RESET\_25}$ | RESET pin internal pull-down resistor | $V_{RESET}$= 0 to 5.5V, $T_A$ = 25°C | 0.85 | 1.25 | 1.7 | MΩ |
| $R_{RESET}$ | | $V_{RESET}$= 0 to 5.5V, $T_A$ = –40° to 125°C | 0.2 | | 2.1 | |
| **COMPARATOR PARAMETERS** | | | | | | |
| $V_{TH\_COMP\_2V}$ | Comparator threshold for 2 V | THRES_COMP = 2 V | 1.85 | | 2.25 | V |
| $V_{TH\_COMP\_2p7V}$ | Comparator threshold for 2.7 V | THRES_COMP = 2.7 V | 2.4 | | 2.9 | V |
| $V_{TH\_COMP\_3V}$ | Comparator threshold for 3 V | THRES_COMP = 3 V | 2.85 | | 3.3 | V |
| $V_{TH\_COMP\_4V}$ | Comparator threshold for 4 V | THRES_COMP = 4 V | 3.7 | | 4.35 | V |
| $V_{S\_COMP}$ | Minimum $V_S$ requirement for proper detection | THRES_COMP = 2 V | 4.5 | | | V |
| | | THRES_COMP = 2.7 V | 5 | | | |
| | | THRES_COMP = 3 V | 5.5 | | | |
| | | THRES_COMP = 4 V | 6.5 | | | |
| $R_{IN,\ COMP}$ | Comparator equivalent input resistance | THRES_COMP = 2 V | 30 | 130 | | kΩ |
| | | THRES_COMP = 2.7 V | 35 | 130 | | |
| | | THRES_COMP = 3 V | 35 | 105 | | |
| | | THRES_COMP = 4 V | 43 | 95 | | |

(1) Specified by design.

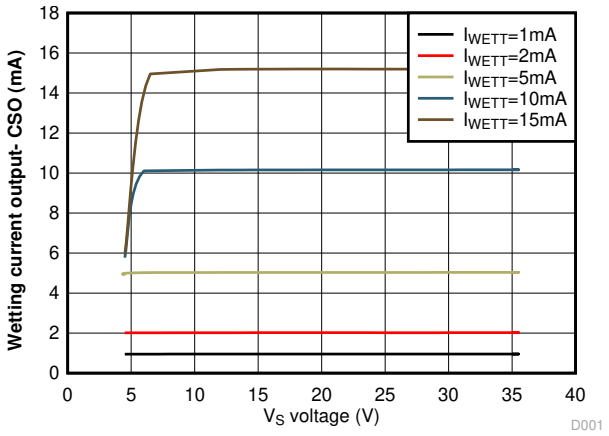
## 6.6 Timing Requirements

$V_S$= 4.5 V to 35 V, $V_{DD}$= 3 V to 5.5 V, and 10 pF capacitive load on SO unless otherwise noted; verified by design and characterization

| | | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SWITCH MONITORING, INTERRUPT, STARTUP AND RESET** | | | | | | |
| $t_{POLL\_ACT}$ | Polling active time accuracy | Polling mode | -12% | | 12% | |
| $t_{POLL}$ | Polling time accuracy | Polling mode | -12% | | 12% | |
| $t_{COMP}$ | Comparator detection time | | | 18 | | µs |
| $t_{CCP\_TRAN}$ | Transition time between last input sampling and start of clean current | | | 20 | | µs |
| $t_{CCP\_ACT}$ | Clean current active time | | -12% | | 12% | |
| $t_{STARTUP}$ | Polling startup time | | 200 | 300 | 400 | µs |
| $t_{INT\_ACTIVE}$ | Active $\overline{INT}$ assertion duration | | 1.5 | 2 | 2.5 | ms |
| $t_{INT\_INACTIVE}$ | $\overline{INT}$ de-assertion duration during a pending interrupt | | 3 | 4 | 5 | ms |
| $t_{INT\_IDLE}$ | Interrupt idle time | | 80 | 100 | 120 | µs |
| $t_{RESET}$ | Time required to keep the RESET pin high to successfully reset the device (no pending interrupt)(1) | | 2 | | | µs |
| $t_{REACT}$ | Delay between a fault event (OV, UV, TW, or TSD) to a high to low transition on the $\overline{INT}$ pin | See 図 7-2 for OV example. | | | 20 | µs |
| **SPI INTERFACE** | | | | | | |
| $t_{LEAD}$ | Falling edge of $\overline{CS}$ to rising edge of SCLK setup time | | 100 | | | ns |
| $t_{LAG}$ | Falling edge of SCLK to rising edge of $\overline{CS}$ setup time | | 100 | | | ns |
| $t_{SU}$ | SI to SCLK falling edge setup time | | 30 | | | ns |
| $t_{HOLD}$ | SI hold time after falling edge of SCLK | | 20 | | | ns |
| $t_{VALID}$ | Time from rising edge of SCLK to valid SO data | | | | 70 | ns |
| $t_{SO(EN)}$ | Time from falling edge of $\overline{CS}$ to SO low-impedance | | | | 60 | ns |
| $t_{SO(DIS)}$ | Time from rising edge of $\overline{CS}$ to SO high-impedance | Loading of 1 kΩ to GND. See 図 7-3. | | | 60 | ns |
| $t_R$ | SI, $\overline{CS}$, and SCLK signals rise time | | | 5 | 30 | ns |
| $t_F$ | SI, $\overline{CS}$, and SCLK signals fall time | | | 5 | 30 | ns |
| $t_{INTER\_FRAME}$ | Delay between two SPI communication ( $\overline{CS}$ low) sequences | | 1.5 | | | µs |
| $t_{CKH}$ | SCLK High time | | 120 | | | ns |
| $t_{CKL}$ | SCLK Low time | | 120 | | | ns |
| $t_{INITIATION}$ | Delay between valid $V_{DD}$ voltage and initial SPI communication | | 45 | | | µs |

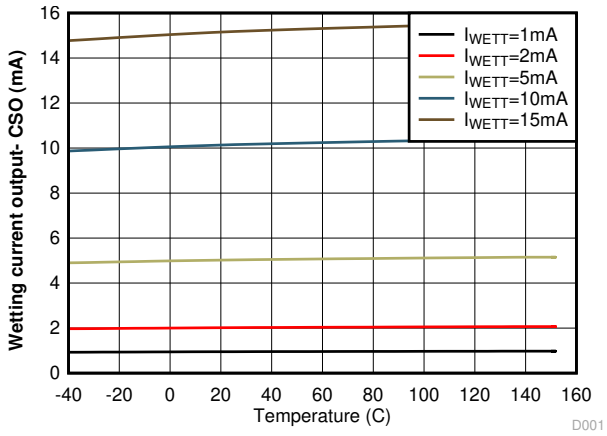
(1) If there is a pending interrupt (/INT pin asserted low), it can take up to 1ms for the device to complete the reset.

## 6.7 Typical Characteristics



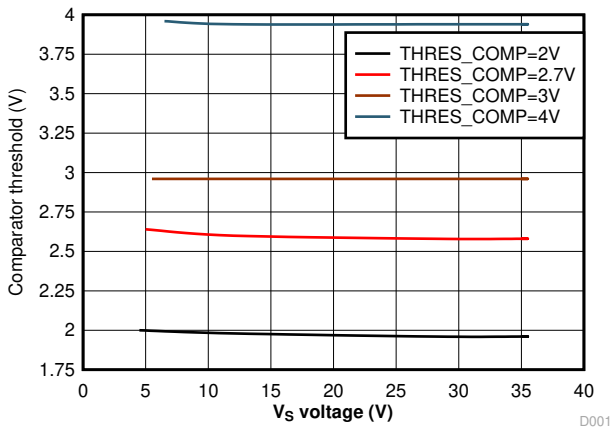

$T_A$ = 25°C

**図 6-1. Wetting Current Output - CSO vs. $V_S$ Voltage**




$V_S$ = 12 V

**図 6-2. Wetting Current Output - CSO vs. Temperature**




$T_A$ = 25°C

**図 6-3. Comparator Threshold vs. $V_S$ Voltage**

# 7 Parameter Measurement Information

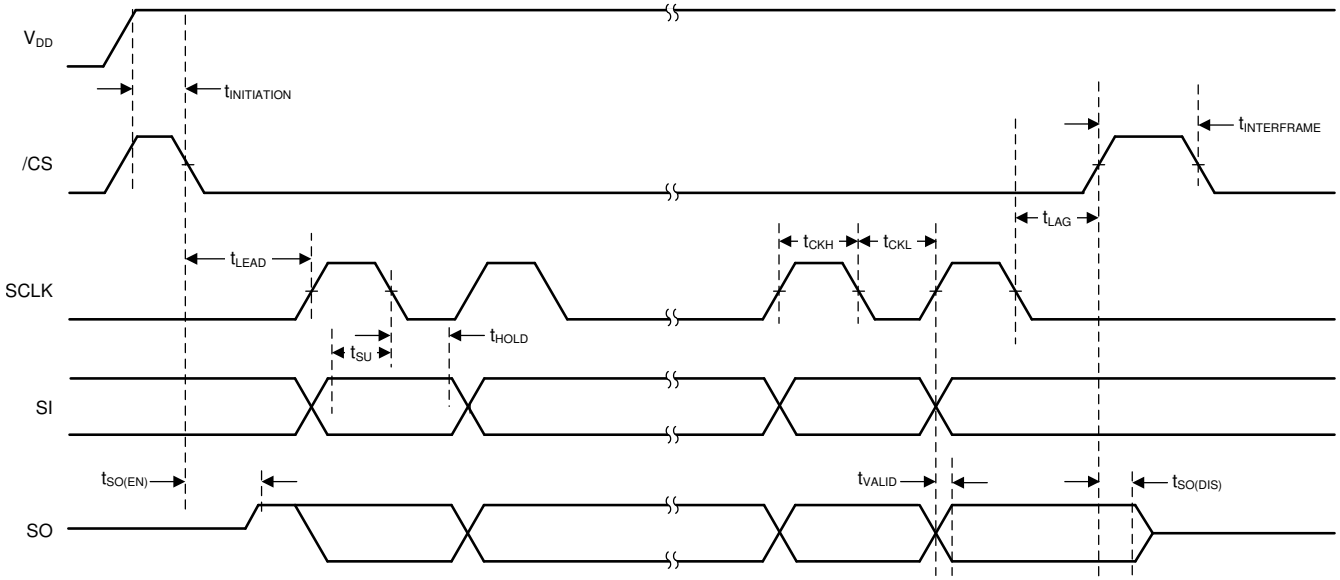



**図 7-1. SPI Timing Parameters**

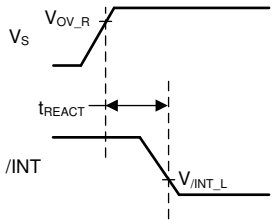



**図 7-2. $t_{REACT}$ Timing Parameters**

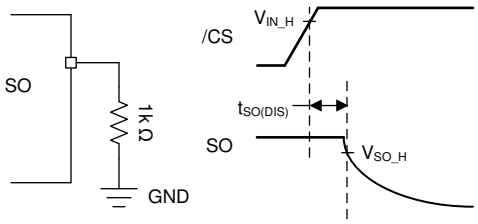



**図 7-3. $t_{SO(DIS)}$ Timing Parameters**

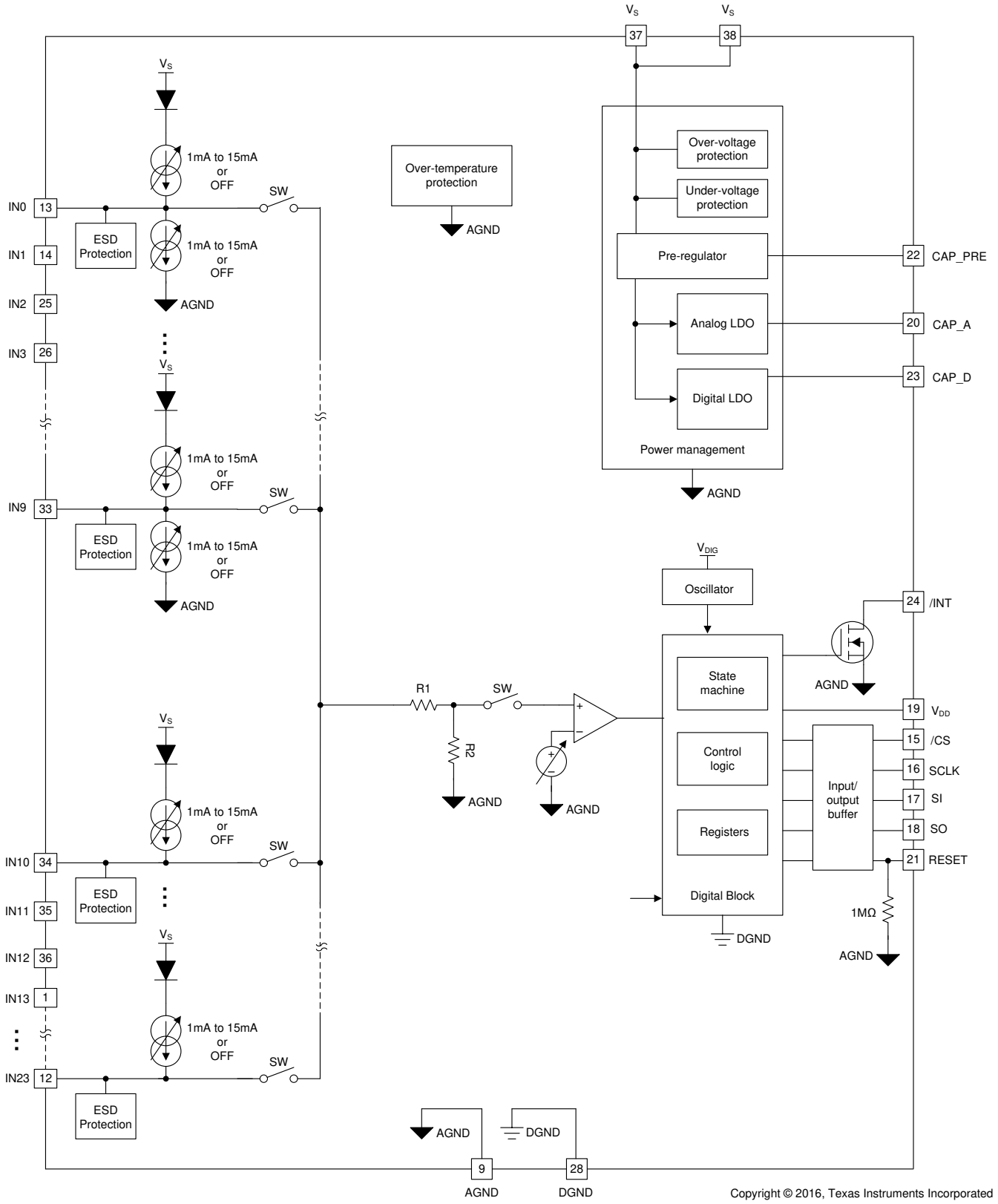
# 8 Detailed Description

## 8.1 Overview

The TIC10024-Q1 is an advanced 24-input Multiple Switch Detection Interface (MSDI) device designed to detect external mechanical switch status in a 12-V automotive system by acting as an interface between the switches and the low-voltage microcontroller. The TIC10024-Q1 is an integrated solution that replaces many discrete components and provides integrated protection, input serialization, and system wake-up capability.

The device monitors 14 switches to GND and 10 additional switches that can be programmed to be connected to either GND or $V_{BAT}$. It features SPI interface to report individual switch status and provides programmability to control the device operation. The TIC10024-Q1 features an integrated comparator that can be used to monitor external digital switch input status. The device has 2 modes of operation: continuous mode and polling mode. The polling mode is a low-power mode that can be activated to reduce current drawn in the system by only turning on the wetting current for a small duty cycle to detect switch status changes. An interrupt is generated upon detection of switch status change and it can be used to wake up the microcontroller to bring the entire system back to operation.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 $V_S$ Pin

The $V_S$ supply provides power to the entire chip and it is designed to be connected directly to a 12-V automotive battery through a reverse-polarity blocking diode.

### 8.3.2 $V_{DD}$ Pin

The $V_{DD}$ supply is used to determine the logic level on the SPI communication interface, source the current for the SO driver, and sets the pull-up voltage for the $\overline{CS}$ pin. It can also be used as a possible external pull-up supply for the $\overline{INT}$ pin in addition to the $V_S$ and it shall be connected to a 3 V to 5.5-V logic supply. Removing $V_{DD}$ from the device disables SPI communications but does not reset the register configurations.

### 8.3.3 Device Initialization

When the device is powered up for the first time, the condition is called Power-On Reset (POR), which sets the registers to their default values and initializes the device state machine. The internal POR controller holds the device in a reset condition until $V_S$ has reached $V_{POR\_R}$, at which the reset condition is released with the device registers and state machine initialized to their default values. After the initialization process is completed, the $\overline{INT}$ pin is asserted low to notify the microcontroller, and the register bit POR in the INT_STAT register is asserted to logic 1. The SPI flag bit POR is also asserted at the SPI output (SO).

During device initialization, factory settings are programmed into the device to allow accurate device operation. The device performs a self-check after the device is programmed to ensure correct settings are loaded. If the self-check returns an error, the CHK_FAIL bit in the INT_STAT register will be flagged to logic 1 along with the POR bit. If this event occurs the microcontroller is recommended to initiate software reset (see section *Software Reset*) to re-initialize the device to allow the correct settings to be re-programmed.

### 8.3.4 Device Trigger

After device initialization, the TIC10024-Q1 is ready to be configured. The microcontroller can use SPI commands to program desired settings to the configuration registers. Once the device configuration is completed, the microcontroller is required to set the bit TRIGGER in the CONFIG register to logic 1 in order to activate wetting current and start external switch monitoring.

After switch monitoring initiates, the configuration registers turn into read-only registers (with the exception of the TRIGGER, CRC_T, and RESET bits in the CONFIG register and all bits in the CCP_CFG1 register). If at any time the device setting needs to be re-configured, the microcontroller is required to first set the bit TRIGGER in the CONFIG register to logic 0 to stop wetting current and switch monitoring. The microcontroller can then program configuration registers to the desired settings. Once the re-configuration is completed the microcontroller can set the TRIGGER bit back to logic 1 to re-start switch monitoring.

Note the cyclic redundancy check (CRC) feature stays accessible when TRIGGER bit is in logic 1, allowing the microcontroller to verify device settings at all time. Refer to section *Cyclic Redundancy Check (CRC)* for more details of the CRC feature.

### 8.3.5 Device Reset

There are 3 ways to reset the TIC10024-Q1 and re-initialize all registers to their default values:

#### *8.3.5.1 $V_S$ Supply POR*

The device is turned off and all register contents are lost if the $V_S$ voltage drops below $V_{POR\_F}$. To turn the device back on, the $V_S$ voltage must be raised back above $V_{POR\_R}$, as illustrated in 図 8-1. The device then starts the initialization process as described in section *Device Initialization*.

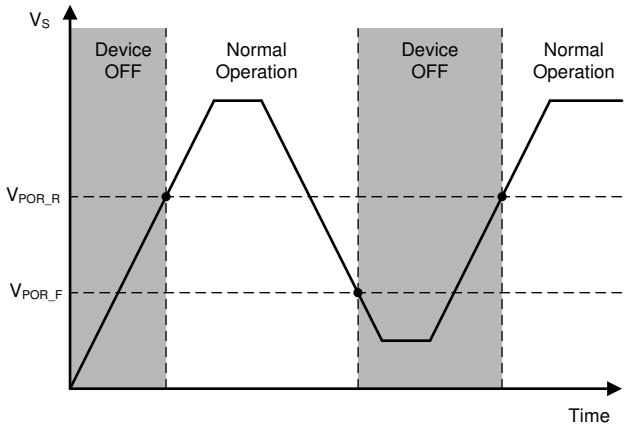



**図 8-1. $V_S$ is Lowered Below The POR threshold, Then Ramped Back Up To Complete A POR Cycle**

#### *8.3.5.2 Hardware Reset*

Microcontroller can toggle the RESET pin to perform a hardware reset to the device. The RESET pin is internally pulled-down by a resistor (1.25MΩ typical) and must be kept low for normal operation. When the RESET pin is toggled high, the device enters the reset state with most of the internal blocks turned off and consumes very little current of $I_{S\_RESET}$. Switch monitoring and SPI communications are stopped in the reset state, and all register contents are cleared. When RESET pin is toggled back low, all the registers are set to their default values and the device state machine is re-initialized, similar to a POR event. When the re-initialization process is completed the $\overline{INT}$ pin is asserted low, and the interrupt register bit POR and the SPI status flag POR are both asserted to notify the microcontroller that the device has completed the reset process.

Note in order to successfully reset the device, the RESET pin needs to be kept high for a minimum duration of $t_{RESET}$. The pin is required to be driven with a stable input (below $V_{RESET\_L}$ for logic low or above $V_{RESET\_H}$ for logic H) to prevent the device from accidental reset.

#### *8.3.5.3 Software Reset*

In addition to hardware reset the microcontroller can also issue a SPI command to initiate software reset. Software reset is triggered by setting the RESET bit in the register CONFIG to logic 1, which re-initializes the device with all registers set to their default values. Once the re-initialization process is completed, the $\overline{INT}$ pin is asserted low, and the interrupt register bit POR and the SPI status flag POR are both asserted to notify the microcontroller that the device has completed the reset process.

### 8.3.6 $V_S$ Under-Voltage (UV) Condition

During normal operation of a typical 12 V automotive system, the $V_S$ voltage is usually quite stable and stays well above 11 V. However, the $V_S$ voltage may drop temporarily during certain vehicle operations, such as cold cranking. If the $V_S$ voltage drops below $V_{UV\_F}$, the TIC10024-Q1 enters the under-voltage (UV) condition since there is not enough voltage headroom for the device to accurately generate wetting currents. The following describes the behavior of the TIC10024-Q1 under UV condition:

1. All current sources and sinks de-activate and switch monitoring stops.
2. Interrupt is generated by asserting the $\overline{INT}$ pin low and the bit UV in the interrupt register (INT_STAT) is flagged to logic 1. The bit UV_STAT is asserted to logic 1 in the register IN_STAT_MISC. The OI SPI flag is asserted during any SPI transactions. The $\overline{INT}$ pin is released and the interrupt register (INT_STAT) is cleared on the rising edge of $\overline{CS}$ provided that the interrupt register has been read during the SPI transaction.
3. SPI communication stays active, and all register settings stay intact without resetting. Previous switch status, if needed, can be retrieved without interruption.
4. The device continues to monitor the $V_S$ voltage, and the UV condition sustains if the $V_S$ voltage continues to stay below $V_{UV\_R}$. No further interrupt is generated once cleared.

Note the device resets as described in section *VS Supply POR* if the $V_S$ voltage drops below $V_{POR\_F}$.

When the $V_S$ voltage rises above $V_{UV\_R}$, the $\overline{INT}$ pin is asserted low to notify the microcontroller that the UV condition no longer exists. The UV bit in the register INT_STAT is flagged to logic 1 and the bit UV_STAT bit is de-asserted to logic 0 in the register IN_STAT_MISC to reflect the clearance of the UV condition. The device resumes operation using current register settings (regardless of the $\overline{INT}$ pin and SPI communication status) with polling restarted from the first enabled channel. The Switch State Change (SSC) interrupt is generated at the end of the first polling cycle and the detected switch status becomes the baseline switch status for subsequent polling cycles. The content of the INT_STAT register, once read by the microcontroller, is cleared, and the $\overline{INT}$ pin is released afterwards.

The following diagram describes the TIC10024-Q1 operation at various different $V_S$ voltages. If the $V_S$ voltage stays above $V_{UV\_F}$ (Case 1), the device stays in normal operation. If the $V_S$ voltage drops below $V_{UV\_F}$ but stays above $V_{POR\_F}$ (Case 2), the device enters the UV condition. If $V_S$ voltage drops below $V_{POR\_F}$ (Case 3), the device resets and all register settings are cleared. The microcontroller is then required to re-program all the configuration registers in order to resume normal operation after the $V_S$ voltage recovers.

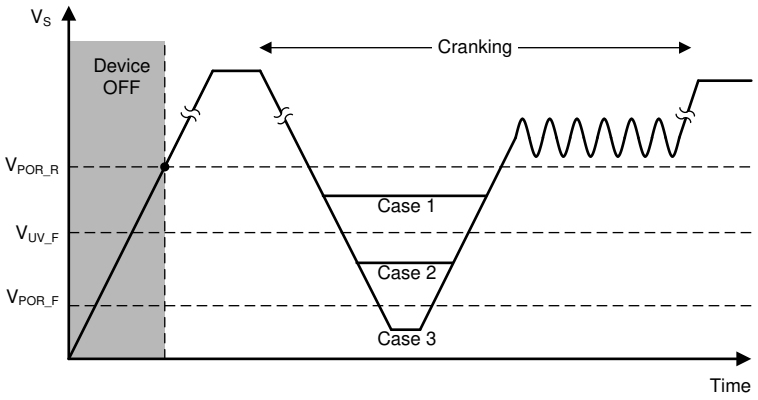



**図 8-2. TIC10024-Q1 Operation At Various $V_S$ Voltage Levels**

### 8.3.7 $V_S$ Over-Voltage (OV) Condition

If $V_S$ voltage rises above $V_{OV\_R}$, the TIC10024-Q1 enters the over-voltage (OV) condition to prevent damage to internal structures of the device on the $V_S$ and INx (for battery-connected switches) pins. The following describes the behavior of the TIC10024-Q1 under OV condition:

1. All current sources and sinks de-activate and switch monitoring stops.
2. Interrupt is generated by asserting the $\overline{INT}$ pin low and the bit OV in the interrupt register (INT_STAT) is flagged to logic 1. The bit OV_STAT is asserted to logic 1 in the register IN_STAT_MISC. The OI SPI flag is asserted during any SPI transactions. The $\overline{INT}$ pin is released and the interrupt register (INT_STAT) is cleared on the rising edge of $\overline{CS}$ provided that the interrupt register has been read during the SPI transaction.
3. SPI communication stays active, and all register settings stay intact without resetting. Previous switch status, if needed, can be retrieved without any interruption.
4. The device continues to monitor the $V_S$ voltage, and the OV condition sustains if the $V_S$ voltage continues to stay above $V_{OV\_R}$- $V_{OV\_HYST}$. No further interrupt is generated once cleared.

When the $V_S$ voltage drops below $V_{OV\_R}$ - $V_{OV\_HYST}$, the $\overline{INT}$ pin is asserted low to notify the microcontroller that the over-voltage condition no longer exists. The OV bit in the register INT_STAT is flagged to logic 1 and the bit OV_STAT bit is de-asserted to logic 0 in the register IN_STAT_MISC to reflect the clearance of the OV condition. The device resumes operation using current register settings (regardless of the $\overline{INT}$ pin and SPI communication status) with polling restarted from the first enabled channel. The Switch State Change (SSC) interrupt is generated at the end of the first polling cycle and the detected switch status becomes the baseline status for subsequent polling cycles. The content of the INT_STAT register, once read by the microcontroller, is cleared and the $\overline{INT}$ pin is released afterwards.

### 8.3.8 Switch Inputs Settings

IN0 to IN23 are inputs connected to external mechanical switches. The switch status of each input, whether open or closed, is indicated by the status registers. 表 8-1 below describes various settings that can be configured for each input. Note some settings are shared between multiple inputs. It is required to first stop device operation by setting the TRIGGER bit low in the register CONFIG before making any configuration changes, as described in *Device Trigger*.

**表 8-1. TIC10024-Q1 Wetting Current and Threshold Setting Details**

| Input | Threshold | Wetting Current | Current Source (CSO) / Current Sink (CSI) | Supported Switch Type |
|---|---|---|---|---|
| IN0 | THRES_COMP_IN0_IN3 | WC_IN0_IN1 | CSO<br>CSI | Switch to GND<br>Switch to VBAT |
| IN1 | | | CSO<br>CSI | Switch to GND<br>Switch to VBAT |
| IN2 | | WC_IN2_IN3 | CSO<br>CSI | Switch to GND<br>Switch to VBAT |
| IN3 | | | CSO<br>CSI | Switch to GND<br>Switch to VBAT |
| IN4 | THRES_COMP_IN4_IN7 | WC_IN4 | CSO<br>CSI | Switch to GND<br>Switch to VBAT |
| IN5 | | WC_IN5 | CSO<br>CSI | Switch to GND<br>Switch to VBAT |
| IN6 | | WC_IN6_IN7 | CSO<br>CSI | Switch to GND<br>Switch to VBAT |
| IN7 | | | CSO<br>CSI | Switch to GND<br>Switch to VBAT |
| IN8 | THRES_COMP_IN8_IN11 | WC_IN8_IN9 | CSO<br>CSI | Switch to GND<br>Switch to VBAT |
| IN9 | | | CSO<br>CSI | Switch to GND<br>Switch to VBAT |
| IN10 | | WC_IN10 | CSO | Switch to GND |
| IN11 | | WC_IN11 | CSO | Switch to GND |
| IN12 | THRES_COMP_IN12_IN15 | WC_IN12_13 | CSO | Switch to GND |
| IN13 | | | CSO | Switch to GND |
| IN14 | | WC_IN14_15 | CSO | Switch to GND |
| IN15 | | | CSO | Switch to GND |
| IN16 | THRES_COMP_IN16_IN19 | WC_IN16_17 | CSO | Switch to GND |
| IN17 | | | CSO | Switch to GND |
| IN18 | | WC_IN18_19 | CSO | Switch to GND |
| IN19 | | | CSO | Switch to GND |
| IN20 | THRES_COMP_IN20_IN23 | WC_IN20_21 | CSO | Switch to GND |
| IN21 | | | CSO | Switch to GND |
| IN22 | | WC_IN22 | CSO | Switch to GND |
| IN23 | | WC_IN23 | CSO | Switch to GND |

#### *8.3.8.1 Input Current Source and Sink Selection*

Among the 24 inputs, IN10 to IN23 are intended for monitoring only ground-connected switches and are connected to current sources. IN0 to IN9 can be programmed to monitor either ground-connected switches or battery-connected switches by configuring the *CS_SELECT* register. The default configuration of the IN0-IN9 inputs after POR is to monitor ground-connected switches (current sources are selected). To set an input to monitor battery-connected switches, set the corresponding bit to logic 1.

#### *8.3.8.2 Input Enable Selection*

The TIC10024-Q1 provides switch status monitoring for up to 24 inputs, but there might be circumstances in which not all inputs need to be constantly monitored. The microcontroller may choose to enable or disable monitoring of certain inputs by configuring the *IN_EN* register. Setting the corresponding bit to logic 0 de-

activates the wetting current source and sink and stops switch status monitoring for the input. Disabling monitoring of unused inputs reduces overall power consumption of the device.

All inputs are disabled by default upon device reset.

#### *8.3.8.3 Thresholds Adjustment*

The threshold level for interrupt generation can be programmed by setting the *THRES_COMP* register. The threshold level settings can be set for each individual input groups and each group consists of 4 inputs. Four threshold levels are available: 2 V, 2.7 V, 3 V, and 4 V.

Remember to use caution when setting up the threshold for switches that are connected externally to the battery as there is a finite voltage drop (as high as $V_{CSI\_DROP\_OPEN}$ for 10mA and 15mA settings) across the current sinks. Therefore, even for an open switch, then voltage on the INx pin can be as high as $V_{CSI\_DROP\_OPEN}$ and the detection threshold shall be configured above it. It shall also be noted that a lower wetting current sink setting may not be strong enough to pull the INx pin close to ground in the presence of a leaky open external switch, as illustrated in the diagram below (see 図 8-3). In this example, the external switch, although in the open state, has large leakage current and can be modelled as an equivalent resistor ($R_{DIRT}$) of 5kΩ. The 2mA current sink is only able to pull the INx pin voltage down to 4 V, even if the switch is in the open state.

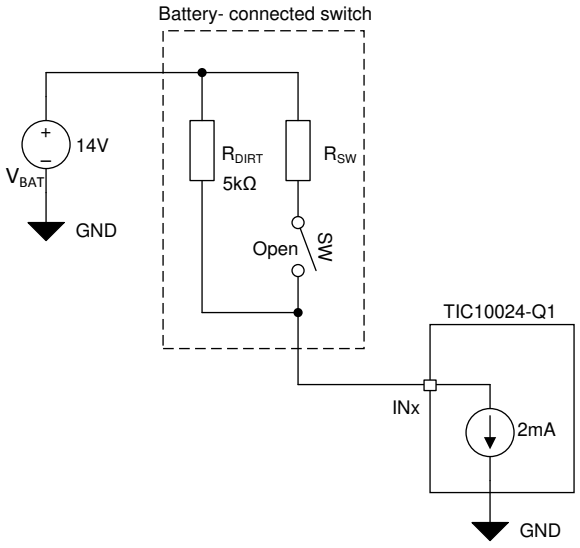





**図 8-3. Example Showing The Calculation of The INx Pin Voltage For A Leaky Battery-Connected Switch**

#### *8.3.8.4 Wetting Current Configuration*

There are 6 different wetting current settings (0 mA, 1 mA, 2 mA, 5 mA, 10 mA, and 15mA) that can be programmed by configuring the *WC_CFG0* and WC_CFG1 registers. 0 mA is selected by default upon device reset.

The accuracy of the wetting current has stronger dependency on the $V_S$ voltage when $V_S$ voltage is low. The lower the $V_S$ voltage falls, the more deviation on the wetting currents from their nominal values. Refer to $I_{WETT\ (CSO)}$ and $I_{WETT\ (CSI)}$ specifications for more details.

### 8.3.9 Interrupt Generation and $\overline{INT}$ Assertion

The $\overline{INT}$ pin is an active-low, open-drain output that asserts low when an event (switch input state change, temperature warning, over-voltage shut down etc.) is detected by the TIC10024-Q1. An external pull-up resistor to $V_{DD}$ is needed on the $\overline{INT}$ pin (see 図 8-4). The $\overline{INT}$ pin can also be connected directly to a 12-V automotive battery to support the microcontroller wake-up feature, as describe in *セクション 8.3.9.3*.

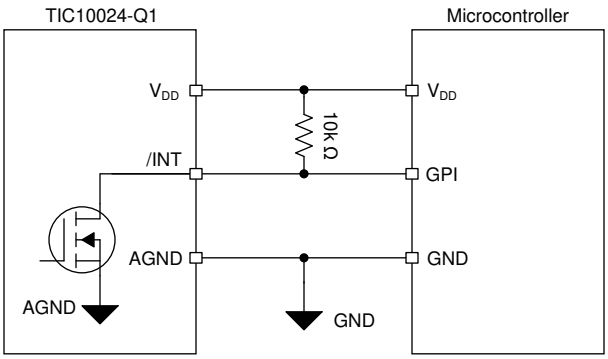





**図 8-4. $\overline{\text{INT}}$ Connection Example #1**

### *8.3.9.1 $\overline{\text{INT}}$ Pin Assertion Scheme*

TIC10024-Q1 supports two configurable schemes for $\overline{\text{INT}}$ assertion: static and dynamic. The scheme can be adjusted by configuring the INT_CONFIG bit in the *CONFIG* register.

If the static $\overline{\text{INT}}$ assertion scheme is used (INT_CONFIG = 0 in the CONFIG register), the $\overline{\text{INT}}$ pin is asserted low upon occurrence of an event. The $\overline{\text{INT}}$ pin is released on the rising edge of $\overline{\text{CS}}$ only if a READ command has been issued to read the INT_STAT register while $\overline{\text{CS}}$ is low, otherwise the $\overline{\text{INT}}$ will be kept low indefinitely. The content of the INT_STAT interrupt register is latched on the first rising edge of SCLK after $\overline{\text{CS}}$ goes low for every SPI transaction, and the content is cleared upon a READ command issued to the INT_STAT register, as illustrated in 図 8-5.

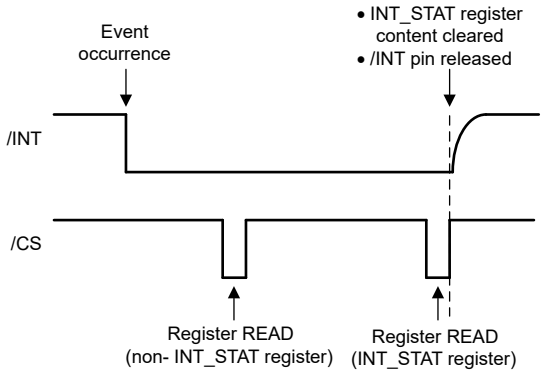



**図 8-5. Static $\overline{\text{INT}}$ Assertion Scheme**

In some system implementations an edge-triggered based microcontroller might potentially miss the $\overline{\text{INT}}$ assertion if it is configured to the static scheme, especially when the microcontroller is in the process of waking up. To prevent missed $\overline{\text{INT}}$ assertion and improve robustness of the interrupt behavior, the TIC10024-Q1 provides the option to use the dynamic assertion scheme for the $\overline{\text{INT}}$ pin. When the dynamic scheme is used (INT_CONFIG= 1 in the CONFIG register), the $\overline{\text{INT}}$ pin is asserted low for a duration of $t_{INT\_ACTIVE}$ and is de-asserted back to high if the INT_STAT register has not been read after $t_{INT\_ACTIVE}$ has elapsed. The $\overline{\text{INT}}$ is kept high for a duration of $t_{INT\_INACTIVE}$, and is re-asserted low after $t_{INT\_INACTIVE}$ has elapsed. The $\overline{\text{INT}}$ pin continues to toggle until the INT_STAT register is read.

If the INT_STAT register is read when $\overline{\text{INT}}$ pin is asserted low, the $\overline{\text{INT}}$ pin is released on the READ command's $\overline{\text{CS}}$ rising edge and the content of the INT_STAT register is also cleared, as shown in 図 8-6. If the INT_STAT register is read when $\overline{\text{INT}}$ pin is de-asserted, the content of the INT_STAT register is cleared on the READ command's $\overline{\text{CS}}$ rising edge, and the $\overline{\text{INT}}$ pin is not re-asserted back low, as shown in 図 8-7.

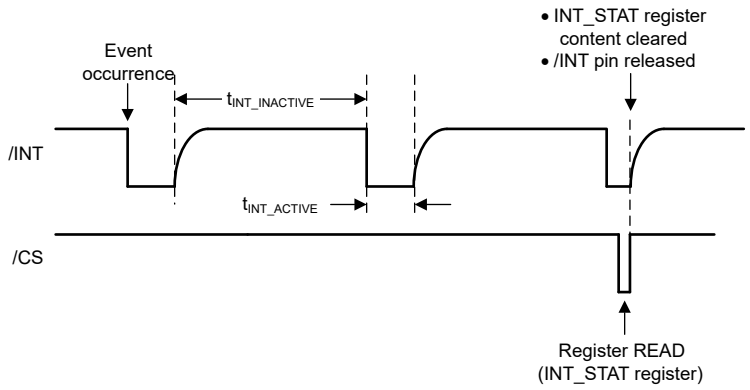



**図 8-6. Dynamic $\overline{\text{INT}}$ Assertion Scheme With INT_STAT Register Read During $t_{INT\_ACTIVE}$**

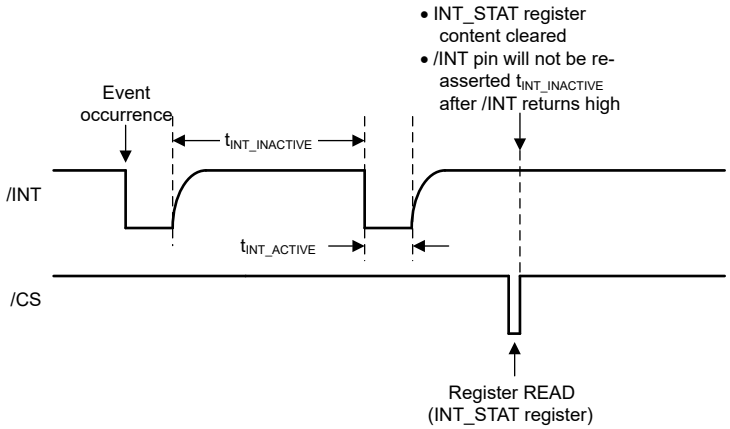



**図 8-7. Dynamic $\overline{\text{INT}}$ Assertion Scheme With INT_STAT Register Read During $t_{INT\_INACTIVE}$**

The static $\overline{\text{INT}}$ assertion scheme is selected by default upon device reset. The $\overline{\text{INT}}$ pin assertion scheme can only be changed when bit TRIGGER is logic 0 in the CONFIG register.

### *8.3.9.2 Interrupt Idle Time ($t_{INT\_IDLE}$) Time*

Interrupt idle time ($t_{INT\_IDLE}$) is implemented in TIC10024-Q1 to:

- Allow the $\overline{\text{INT}}$ pin enough time to be pulled back high by the external pull-up resistor and allow the next assertion to be detectable by an edge-triggered microcontroller.
- Minimize the chance of glitching on the $\overline{\text{INT}}$ pin if back-to-back events occur.

When there is a pending interrupt event and the interrupt event is not masked, $t_{INT\_IDLE}$ is applied after the READ command is issued to the INT_STAT register. If another event occurs during the interrupt idle time the INT_STAT register content is updated instantly but the $\overline{\text{INT}}$ pin is not asserted low until $t_{INT\_IDLE}$ has elapsed. If another READ command is issued to the INT_STAT register during $t_{INT\_IDLE}$, the INT_STAT register content is cleared immediately, but the $\overline{\text{INT}}$ pin is not re-asserted back low after $t_{INT\_IDLE}$ has elapsed. An example of the interrupt idle time is given below to illustrate the $\overline{\text{INT}}$ pin behavior under the static $\overline{\text{INT}}$ assertion schemes:

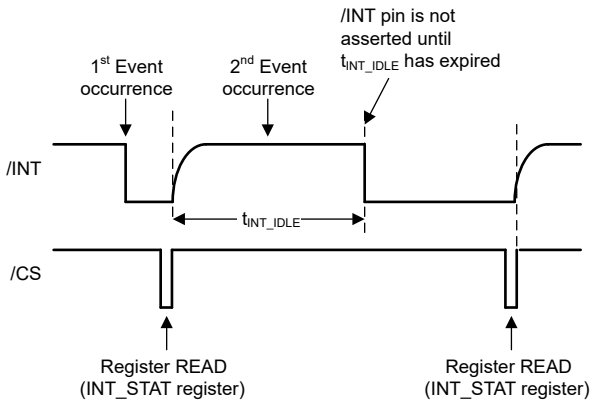



**図 8-8. $\overline{INT}$ Assertion Scheme With $t_{INT\_IDLE}$**

#### *8.3.9.3 Microcontroller Wake-Up*

Using a few external components, the $\overline{INT}$ pin can be used for wake-up purpose to activate a voltage regulator through its inhibit inputs. An implementation example is shown in 図 8-9. This implementation is especially useful for waking up a microcontroller in sleep mode to allow significant system-level power savings.

Before the wake-up event, the $\overline{INT}$ pin is in high impedance state on the TIC10024-Q1. The microcontroller can be kept in sleep state with all its GPIOs in logic low. Hence, Q2 remains off with its based in logic low state and the base of Q1 is weakly pulled-high to the $V_S$ level. This causes Q1 to remain off, and the LDO_EN signal is pulled-down to logic low to disable the regulator's output. $V_{DD}$ is therefore unavailable to both the TIC10024-Q1 device and the microcontroller and SPI communication is not supported. Switch status monitoring, however, is still active in the TIC10024-Q1.

When an event, such as switch status change, temperature warning, or overvoltage, occurs, the $\overline{INT}$ pin is asserted low by TIC10024-Q1, causing Q1 to turn on to activate the voltage regulator. The microcontroller is then reactivated, and the communication between the microcontroller and the TIC10024-Q1 is reestablished. The microcontroller can then access stored event information using SPI communication. Note since the $\overline{INT}$ pin is de-asserted after the INT_STAT register is read, the microcontroller is required to keep the regulator on by driving the µC_LDO_EN signal high. This allows $V_{DD}$ to stay high to provide power to the microcontroller and support SPI communications.

The wake-up implementation is applicable only when the device is configured to use the static $\overline{INT}$ assertion scheme.

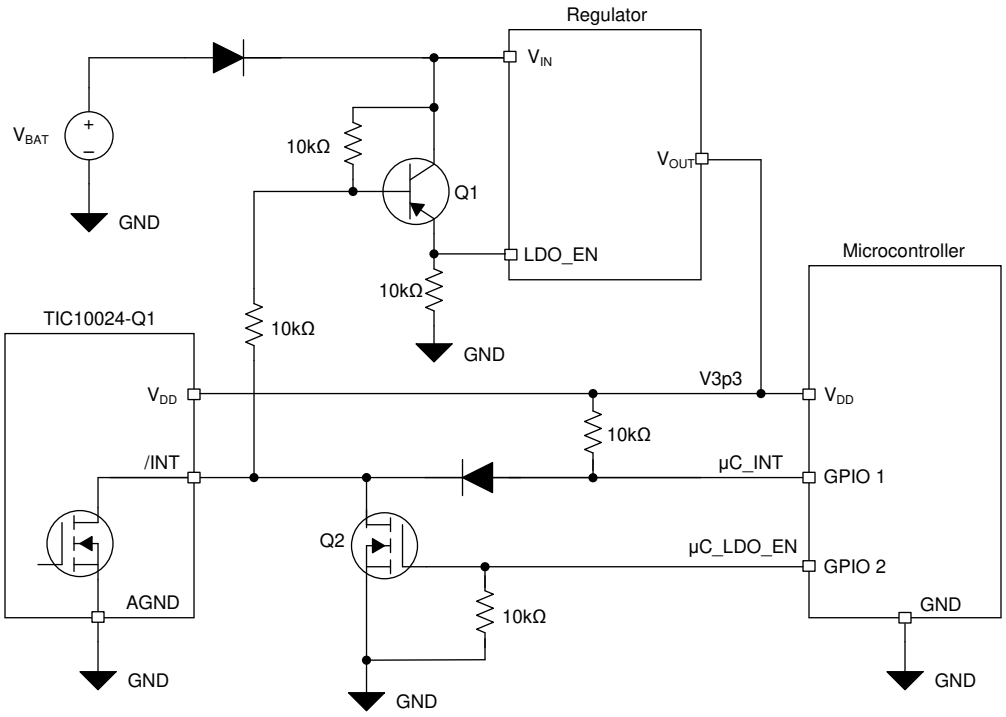



**図 8-9. $\overline{\text{INT}}$ Connection to Support Microcontroller Wake-Up**

### *8.3.9.4 Interrupt Enable / Disable And Interrupt Generation Conditions*

Each switch input can be programmed to enable or disable interrupt generation upon status change by configuring registers *INT_EN_COMP1* to *INT_EN_COMP2* .

The abovementioned registers can also be used to control interrupt generation condition based on the following settings:

1. **Rising edge**: an interrupt is generated if the current input measurement is above the corresponding threshold and the previous measurement was below.
2. **Falling edge:** an interrupt is generated if the current input measurement is below the corresponding threshold and the previous measurement was above.
3. **Both edges**: changes of the input voltage in either direction results in an interrupt generation.

Note interrupt generation from switch status change is disabled for all inputs by default upon device reset.

#### 8.3.9.5 Detection Filter

When monitoring the switch input status, a detection filter can be configured by setting the DET_FILTER bits in the *CONFIG* register to generate Switch Status Change (SSC) interrupt only if the same input status (w.r.t the threshold) is sampled consecutively. This detection filter can be useful to debounce inputs during a switch toggle event. Four different filtering schemes are available:

1. Generate an SSC interrupt if the voltage level at an input crossed its threshold
2. Generate an SSC interrupt if the voltage level at an input crossed its threshold and the status is stable (w.r.t. the threshold) for at least 2 consecutive polling cycles
3. Generate an SSC interrupt if the voltage level at an input crossed its threshold and the status is stable (w.r.t. the threshold) for at least 3 consecutive polling cycles
4. Generate an SSC interrupt if the voltage level at an input crossed its threshold and the status is stable (w.r.t. the threshold) for at least 4 consecutive polling cycles

The default value of switch status is stored internally after the 1st detection cycle, even if detection filter (by configure the DET_FILTER in the *CONFIG* register) is used. An example is illustrated below with the assumption that DET_FILTER in register *CONFIG* is set to 11 (SSC interrupt is generated if the input crosses the threshold and the status is stable w.r.t. the threshold for at least 4 consecutive detection cycles). Assume switch status change is detected in the 3rd detection cycle and stays the same for the next 3 cycles.

| DETECTION CYCLE | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| **Event** | • Default Switch status stored<br>• $\overline{\text{INT}}$ asserted<br>• SSC flagged | — | Switch status change detected | — | — | • $\overline{\text{INT}}$ asserted<br>• SSC flagged |

The detection filter counter is reset to 0 when the TRIGGER bit in the *CONFIG* register is de-asserted to logic 0. Upon device reset, the default setting for the detection filter is set to generating an SSC interrupt at every threshold crossing.

### 8.3.10 Temperature Monitor

With multiple switch inputs are closed and high wetting current setting is enabled, considerable power can be dissipated by the device and raise the device temperature. TIC10024-Q1 has integrated temperature monitoring and protection circuitry to put the device in low power mode to prevent damage due to overheating. Two types of temperature protection mechanisms are integrated in the device: Temperature Warning (TW) and Temperature Shutdown (TSD). The triggering temperatures and hysteresis are specified in 表 8-2 below:

**表 8-2. Temperature Monitoring Characteristics of TIC10024-Q1**

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| Temperature warning trigger temperature ($T_{TW}$) | 130 | 140 | 155 | °C |
| Temperature shutdown trigger temperature ($T_{TSD}$) | 150 | 160 | 175 | °C |
| Temperature hysteresis ($T_{HYS}$) for $T_{TW}$ and $T_{TSD}$ | | 15 | | °C |

#### 8.3.10.1 Temperature Warning (TW)

When the device temperature goes above the temperature warning trigger temperature ($T_{TW}$), the TIC10024-Q1 performs the following operations:

1. Generate an interrupt by asserting the $\overline{\text{INT}}$ pin low and flag the TW bit in INT_STAT register to logic 1. The TEMP bit in the SPI flag is also flagged to logic 1 for all SPI transactions.
2. The TW_STAT bit of the IN_STAT_MISC register is flagged to logic 1.
3. If the TW_CUR_DIS_CSO or TW_CUR_DIS_CSO bit in *CONFIG* register is set to logic 0 (default), the wetting current is adjusted down to 2 mA for 10 mA or 15 mA settings. The wetting current stays at its pre-configured value if 0 mA, 1 mA, 2 mA, or 5 mA setting is used.
4. Maintain the low wetting current as long as the device junction temperature stays above $T_{TW}$ - $T_{HYS}$.

The $\overline{INT}$ pin is released and the INT_STAT register content is cleared on the rising edge of $\overline{CS}$ provided the INT_STAT register has been read during $\overline{CS}$ low. The TIC10024-Q1 continues to monitor the temperature, but does not issue further interrupts if the temperature continues to stay above $T_{TW}$- $T_{HYS}$. The status bit TW_STAT in register IN_STAT_MISC continues to stay at logic 1 as long as the temperature warning condition exists.

If desired, the reduction of wetting current down to 2mA setting (from 10 mA or 15 mA) can be disabled by setting the TW_CUR_DIS_CSO or TW_CUR_DIS_CSI bit in the *CONFIG* register to 1. The interrupt is still generated ( $\overline{INT}$ asserted low and INT_STAT interrupt register is updated) when the temperature warning event occurs but the wetting current is not reduced. This setting applies to both the polling and continuous mode operation. Note if the feature is enabled, switch detection result might be impacted upon $T_{TW}$ event if the wetting current is reduced to 2mA from 10mA or 15mA.

When the temperature drops below $T_{TW}$- $T_{HYS}$, the $\overline{INT}$ pin is asserted low (if released previously) to notify the microcontroller that the temperature warning condition no longer exists. The TW bit of the interrupt register INT_STAT is flagged logic 1. The TW_STAT bit in the IN_STAT_MISC register is de-asserted back to logic 0. The device resumes operation using the current programmed settings (regardless of the $\overline{INT}$ and $\overline{CS}$ status).

#### *8.3.10.2 Temperature Shutdown (TSD)*

After the device enters TW condition, if the junction temperature continues to rise and goes above the temperature shutdown threshold ($T_{TSD}$), the TIC10024-Q1 enters the Temperature Shutdown (TSD) condition and performs the following operations:

1. Opens all the switches connected to the current sources or sinks to prevent any further heating due to excessive current flow.
2. Generate an interrupt by asserting the $\overline{INT}$ pin (if not already asserted) low and flag the TSD bit in the INT_STAT register to logic 1. The TEMP bit in the SPI flag is also flagged to logic 1 for all SPI transactions.
3. The TSD_STAT bit of the IN_STAT_MISC register is flagged to logic 1. The TW_STAT bit also stays at logic 1.
4. SPI communication stays on and all register settings stay intact without resetting. Previous switch status, if needed, can be retrieved without any interruption.
5. Maintain the setting as long as the junction temperature stays above $T_{TSD}$- $T_{HYS}$.

The $\overline{INT}$ pin is released and the INT_STAT register content is cleared on the rising edge of $\overline{CS}$ provided the INT_STAT register has been read during $\overline{CS}$ low. The TIC10024-Q1 continues to monitor the temperature, but does not issue further interrupts if the temperature continues to stay above $T_{TSD}$ - $T_{HYS}$. The status bit TSD_STAT in register IN_STAT_MISC continues to stay at logic 1 as long as the temperature shutdown condition exists.

When the temperature drops below $T_{TSD}$ - $T_{HYS}$, the $\overline{INT}$ pin is asserted low (if released previously) to notify the microcontroller that the temperature shutdown condition no longer exists. The TSD bit of the interrupt register INT_STAT is flagged logic 1. In the IN_STAT_MISC register, the TSD_STAT bit is de-asserted back to logic 0, while the TW_STAT bit stays at logic 1. The device resumes operation using the wetting current setting described in section *Temperature Warning* if the temperature stays above $T_{TW}$ - $T_{HYS}$. Note the polling restarts from the first enabled channel and the SSC interrupt is generated at the end of the first polling cycle. The detected switch status from the first polling cycle becomes the default switch status for subsequent polling.

### 8.3.11 Parity Check And Parity Generation

The TIC10024-Q1 uses parity bit check to ensure error-free data transmission from/to the SPI commander.

The device uses odd parity, for which the parity bit is set so that the total number of ones in the transmitted data on SO (including the parity bit) is an odd number (i.e. Bit0 ⊕ Bit1 ⊕ … ⊕ Bit30 ⊕ Bit31⊕ Parity = 1).

The device also uses odd parity check after receiving data on SI from the SPI commander. If the total number of ones in the received data (including the parity bit) is an even number the received data is discarded. The $\overline{INT}$ will be asserted low and the PRTY_FAIL bit in the interrupt register (INT_STAT) is flagged to logic 1 to notify the host that transmission error occurred. The PRTY_FAIL flag is also asserted during SPI communications.

### 8.3.12 Cyclic Redundancy Check (CRC)

The TIC10024-Q1 includes a CRC module to support redundancy checks on the configuration registers to ensure the integrity of data. The CRC calculation is based on the ITU-T X.25 implementation, and the CRC polynomial (0x1021) used is popularly known as CRC-CCITT-16 since it was initially proposed by the ITU-T (formerly CCITT) committee. The CRC calculation rule is defined in 表 8-3:

**表 8-3. CRC Calculation Rule**

| CRC RULE | VALUE |
|---|---|
| CRC result width | 16 bits |
| Polynomial | $x^{16} + x^{12} + x^5 + 1$ (1021h) |
| Initial (seed) value | FFFFh |
| Input data reflected | No |
| Result data reflected | No |
| XOR value | 0000h |

The CRC calculation is done on all the configuration registers starting from register *CONFIG* and ending at register INT_EN_CFG0 (address 1Ah through 24h). The device substitutes a "zero" for each reserved configuration register bit during the CRC calculation. The CRC calculation can be triggered by asserting the CRC_T bit in the CONFIG register. Once completed, the CRC_CALC interrupt bit in the INT_STAT register is asserted and an interrupt is issued. The 16-bit CRC calculation result is stored in the register CRC. This interrupt can be disabled by de-asserting the CRC_CALC_EN bit in the INT_EN_CFG0 register. It is important to avoid writing data to the configuration registers when the device is undergoing CRC calculations to prevent false calculation results.

図 8-10 shows the block diagram of the CRC module. The module consists of 16 shift-registers and 3 exclusive-OR gates. The registers start with 1111-1111-1111-1111 (or FFFFh) and the module performs an XOR function and shifts its content until the last bit of the register string is used. The final register's content after the last data bit is the calculated CRC value of the data set and the content is stored in the CRC register.

Note the CRC_T bit self-clears after the CRC calculation is completed. Logic 1 is used for CRC_T bit during CRC calculation.

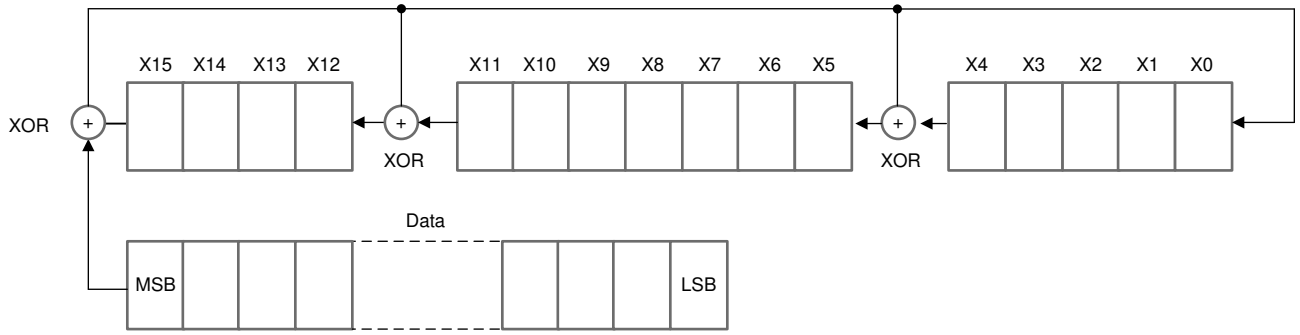



**図 8-10. CCITT-16 CRC Module Block Diagram**

## 8.4 Device Functional Modes

The TIC10024-Q1 has 2 modes of operation: continuous mode and polling mode. The following sections describe the two operation modes in details as well as some of the advanced features that could be activated during normal operations.

### 8.4.1 Continuous Mode

In continuous mode, wetting current is continuously applied to each enabled input channel, and the status of each channel is sampled sequentially (starting from the IN0 to IN23). The TIC10024-Q1 monitors enabled inputs and issues an interrupt (if enabled) if a switch status change event is detected. The wetting current setting for each input can be individually adjusted by configuring the *WC_CFG0* and *WC_CFG1* to the 0mA, 1mA, 2mA, 5mA, 10mA, or 15mA setting.

図 8-11 below illustrates an example of the timing diagram of the detection sequence in continuous mode. After the TRIGGER bit in register *CONFIG* is set to logic 1, it takes $t_{STARTUP}$ to activate the wetting current for all enabled inputs. The wetting currents stay on continuously, while each input is routed to the comparator for sampling in a sequential fashion. After detection is done for an input, the switch status (below or above detection threshold) is stored in the register (*IN_STAT_COMP*) to be used as the default state for subsequent detection cycles. After the end of the first polling cycle, the $\overline{INT}$ pin is asserted low to notify the microcontroller that the default switch status is ready to be read. The SSC bit in INT_STAT register and the SPI status flag SSC are also asserted to logic 1. The polling cycle time ($t_{POLL}$) determines how frequently each input is sampled and can be configured in the register CONFIG.

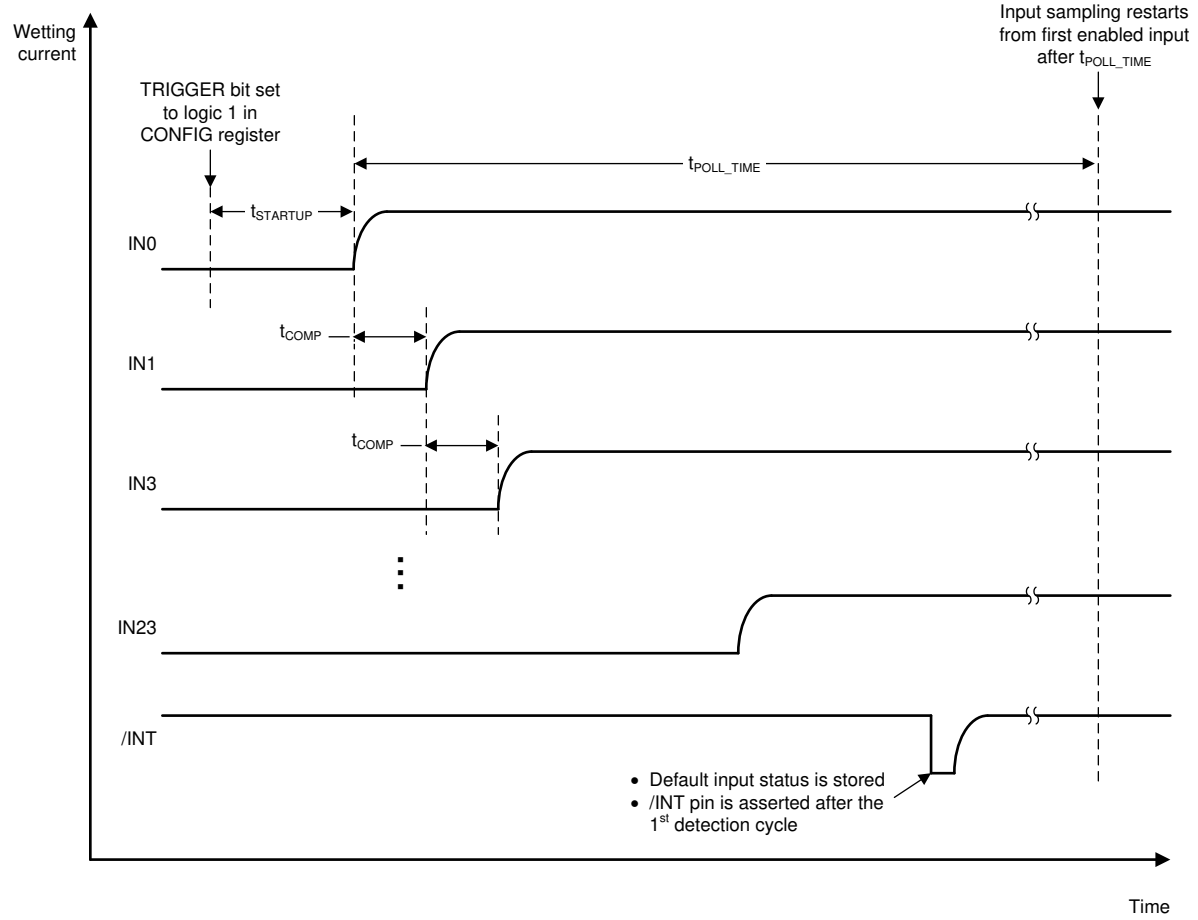



**図 8-11. An Example Of The Detection Sequence In Continuous Mode**

The *INT_STAT* register is cleared and $\overline{\text{INT}}$ pin de-asserted if a SPI READ command is issued to the register. Note the interrupt is always generated after the 1st detection cycle (after the TRIGGER bit in register *CONFIG* is set to logic 1). In subsequent detection cycles, the interrupt is generated only if switch status change is detected.

No wetting currents are applied to 0mA- configured inputs, although some biasing current (as specified by $I_{IN\_LEAK\_0mA}$) may still flow in and out of the input. Threshold crossing monitoring is still performed for the input using the defined threshold(s). The 0mA setting is useful to utilize the integrated comparator to measure applied voltage on a specific input without being affected by the device wetting current.

### 8.4.2 Polling Mode

The polling mode can be activated to reduce current drawn in ignition-off condition to conserve battery charge. Unlike the continuous mode, the current sources/sinks do not stay on continuously in the polling mode. Instead, they are turned on/off sequentially from IN0 to IN23 and cycled through each individual input channel. The microcontroller can be put to sleep to reduce overall system power. If a switch status change (SSC) is detected by the TIC10024-Q1, the $\overline{\text{INT}}$ pin (if enabled for the input channel) is asserted low (and the SSC bit in INT_STAT register and the SPI status flag SSC are also asserted to logic 1). The $\overline{\text{INT}}$ pin assertion can be used to wake up the system regulator which, in turn, wakes up the microcontroller as described in section *Microcontroller Wake-Up*. The microcontroller can then use SPI communication to read the switch status information.

The polling is activated when the TRIGGER bit in the *CONFIG* register is set to logic 1.

In polling mode, wetting current is applied to each input for a pre-programmed polling active time between 64 µs and 2048 µs, set by the POLL_ACT_TIME bits in the *CONFIG* register . At the end of the wetting current application, the input voltage is sampled by the comparator. Each input is cycled through in sequential order from IN0 to IN23. Sampling is repeated at a frequency from 2 ms to 4096 ms, set by the POLL_TIME bits in the *CONFIG* register . Wetting currents are applied to closed switches only during the polling active time; hence the overall system current consumption can be greatly reduced.

Similar to continuous mode, after the first polling cycle, the switch status of each input (below or above detection threshold) is stored in the register (*IN_STAT_COMP*) to be used as the default state for subsequent polling cycles. The $\overline{\text{INT}}$ pin is asserted low to notify the microcontroller that the default switch status is ready to be read. The SSC bit in INT_STAT register and the SPI status flag SSC are also asserted to logic 1. The *INT_STAT* register is cleared and $\overline{\text{INT}}$ pin de-asserted if a SPI READ command is issued to the register. Note the interrupt is always generated after the 1st polling cycle (after the TRIGGER bit in register *CONFIG* is set to logic 1). In subsequent polling cycles the interrupt is generated only if switch status change is detected.

An example of the timing diagram of the polling mode operation is shown in 図 8-12.

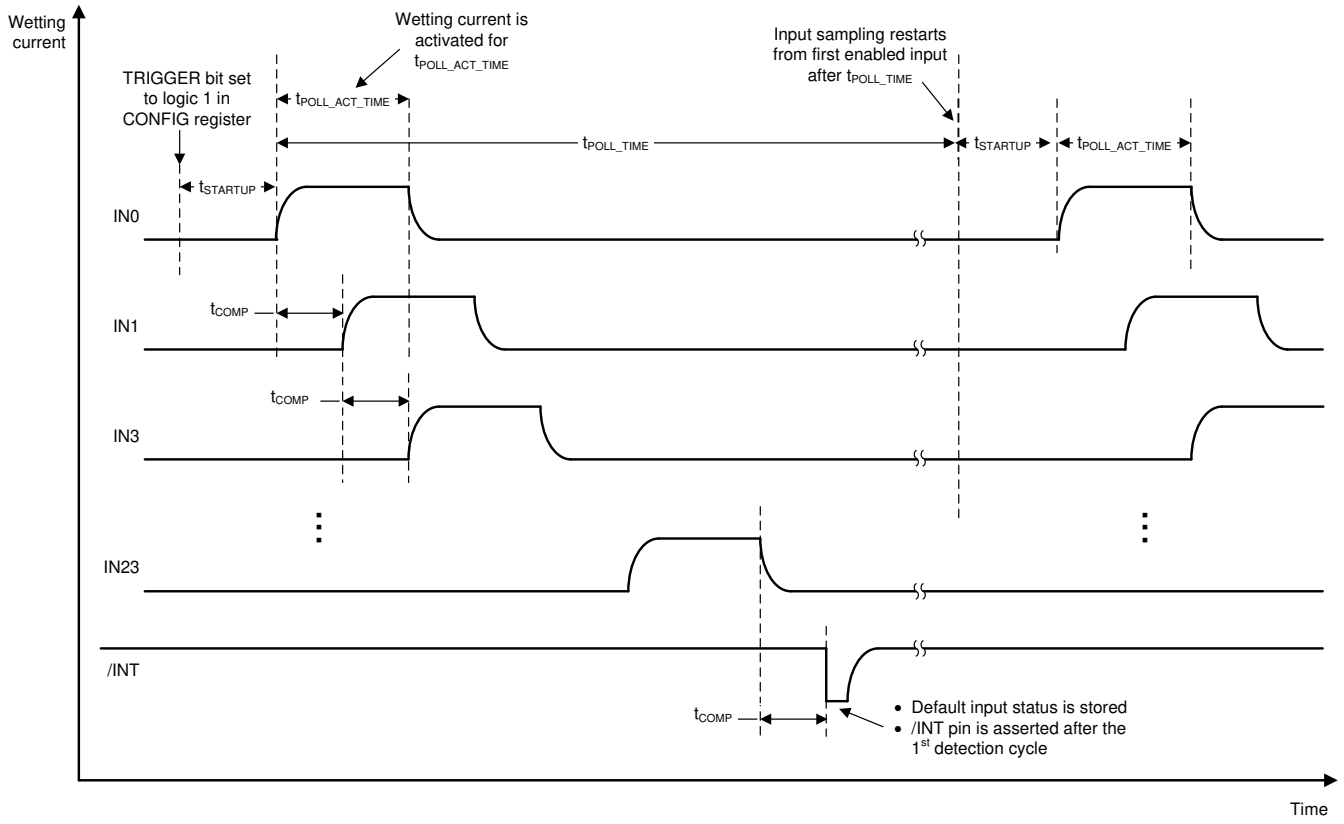



**図 8-12. An Example Of The Polling Sequence In Standard Polling Mode**

If the switch position changes between two active polling times, no interrupt will be generated and the status register (*IN_STAT_COMP*) will not reflect such a change. An example is shown in 図 8-13.

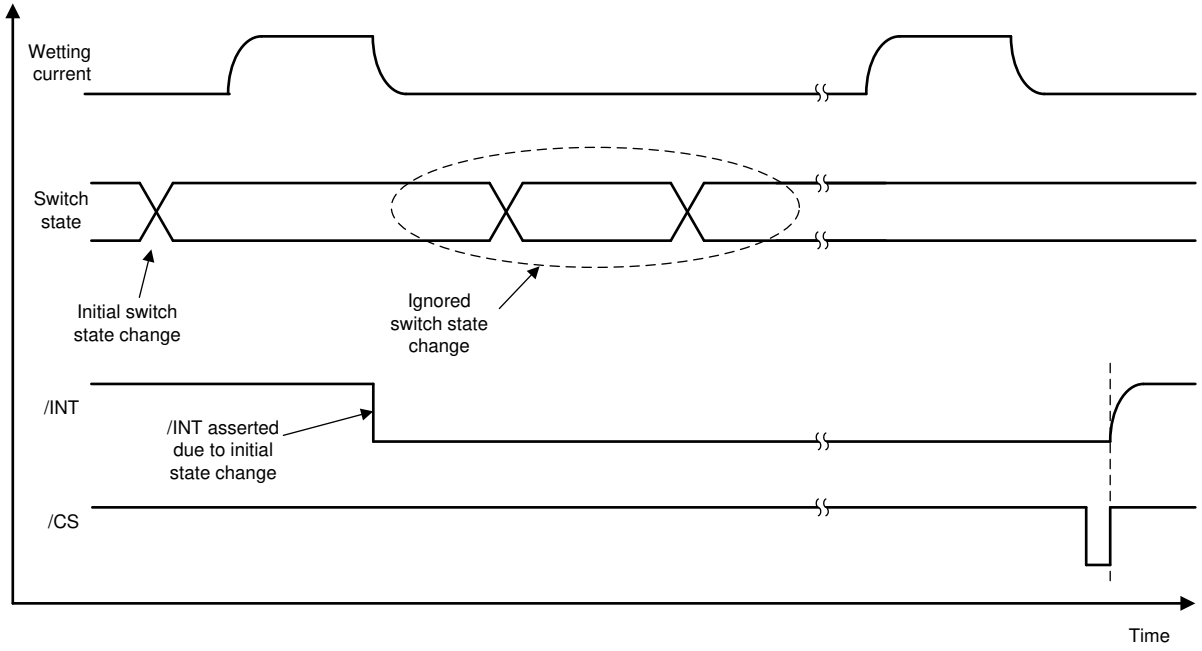



**図 8-13. Example For Ignored Switch Position Change Between 2 Wetting Current Cycles**

### 8.4.3 Additional Features

There are additional features that can be enabled during continuous and polling mode to increase robustness of device operation or provide more system information. These features are described in detail in the following sections.

#### *8.4.3.1 Clean Current Polling (CCP)*

In real automotive system, lower wetting current is generally desired to reduce the system's overall power consumption. However, certain system design requires 10 mA or higher cleaning current to clear oxide build-up on the mechanical switch contact surface when the current is applied to closed switches. A special type of polling, called the Clean Current Polling (CCP), can be used for this application.

If CCP is enabled each polling cycle consists of two wetting current activation steps. The first step uses the wetting current setting configured in the *WC_CFG0* and *WC_CFG1* registers as in the continuous mode or polling mode. The second step (cleaning cycle) is activated simultaneously for all CCP enabled inputs at a time $t_{CCP\_TRAN}$ after the normal polling step of the last enabled input. Interrupt generation and $\overline{INT}$ pin assertion is not impacted by the clean current pulses.

The wetting current and its active time for the cleaning cycle can be configured in the *CCP_CFG0* register. The cleaning cycle can be disabled, if desired, for each individual input by programming the *CCP_CFG1* register. CCP is available for both continuous mode and polling mode. To use the CCP feature, at least one input has to be enabled.

図 8-14 illustrates the operation of the CCP when the device is configured to the polling mode.

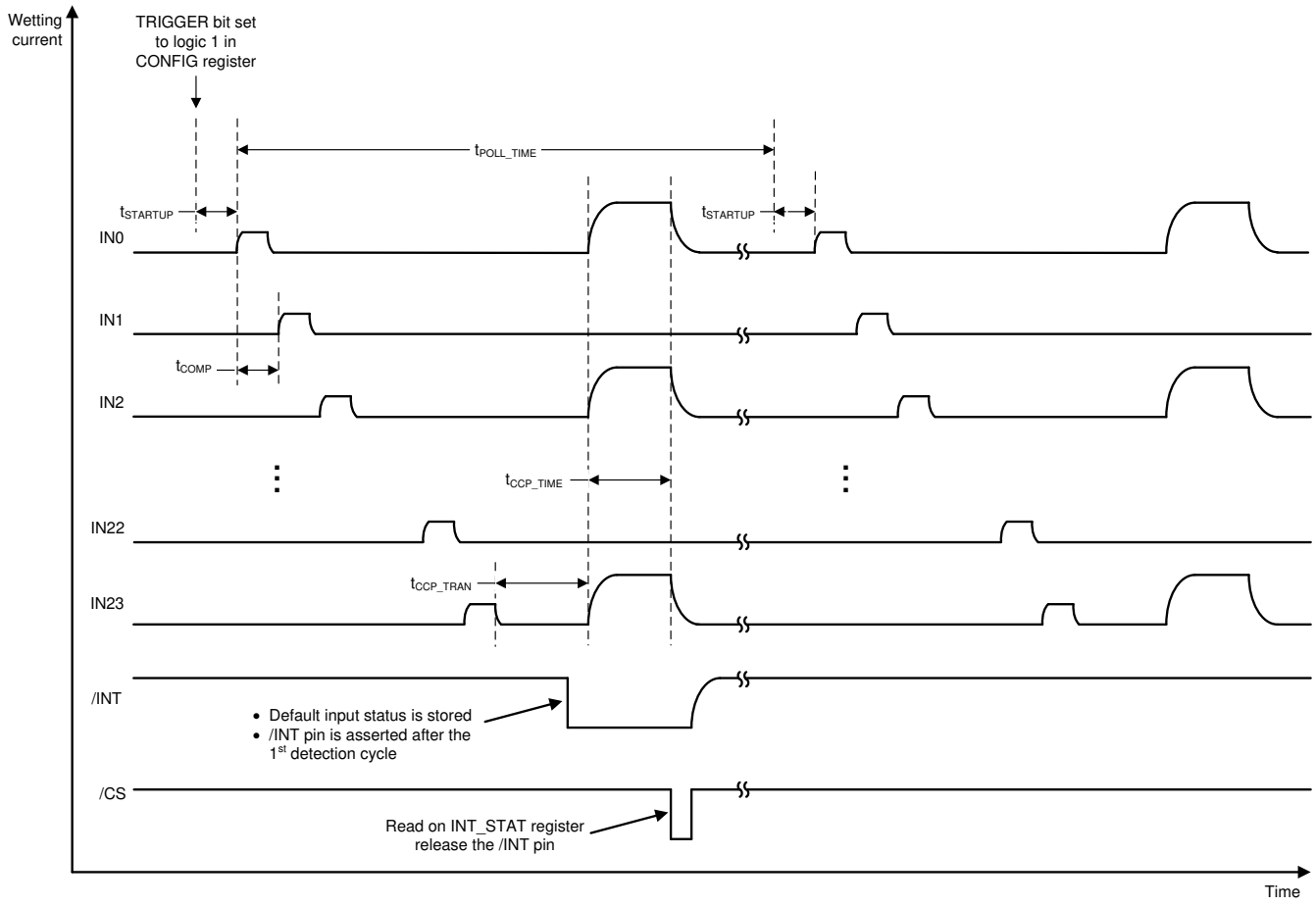



**図 8-14. Polling With CCP Enabled**

図 8-15 illustrates the operation of the CCP when the device is configured to the continuous mode:

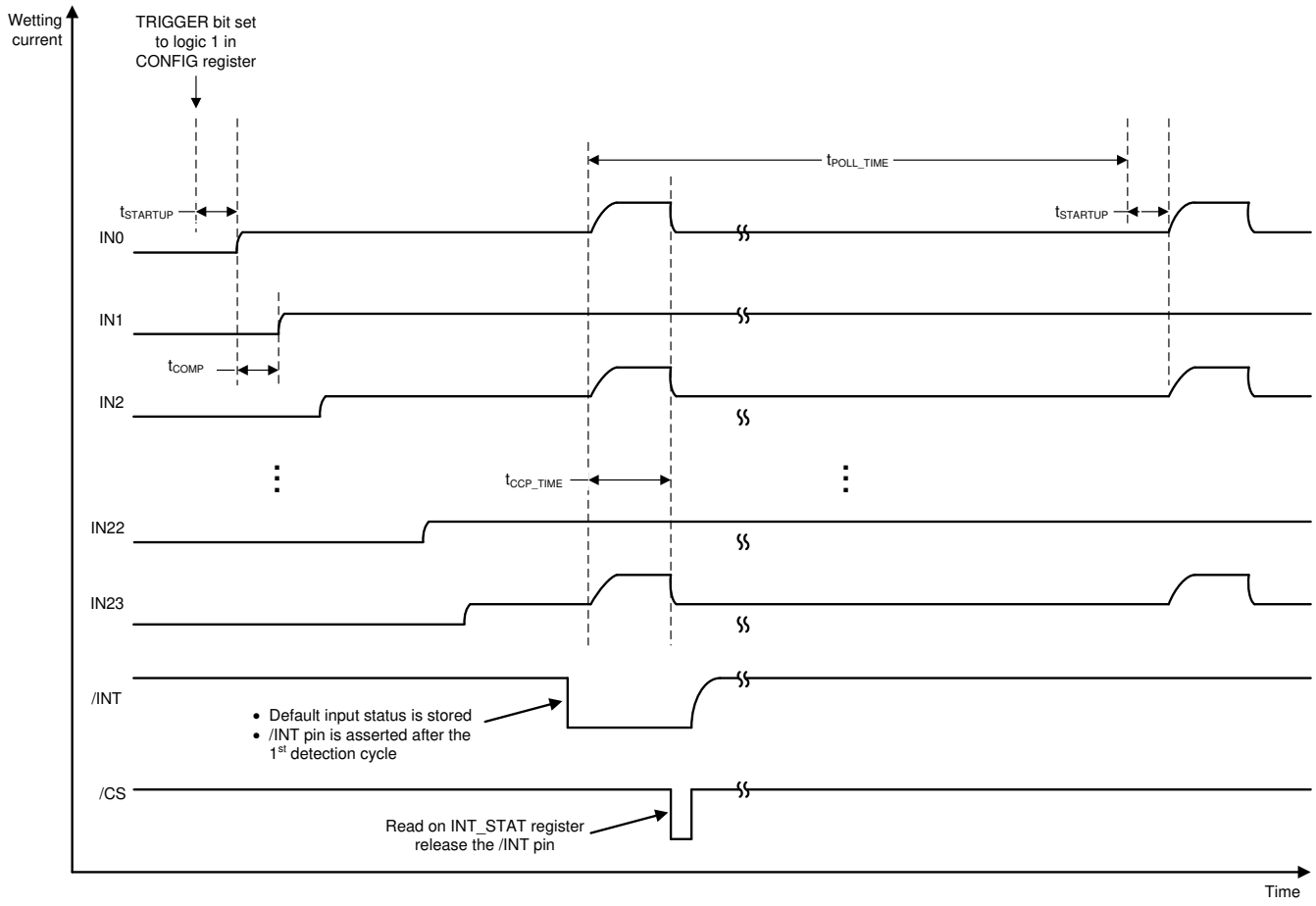



**図 8-15. Continue Mode With CCP Enabled**

### *8.4.3.2 Wetting Current Auto-Scaling*

The 10 mA and 15 mA wetting current settings are useful to clean oxide build-up on the mechanical switch contact surface when the switch changes state from open to close. After the switch is closed, it is undesirable to keep the wetting current level at high level if only digital switches are monitored since it results in high current consumption and could potentially heat up the device quickly if multiple inputs are monitored. The wetting current auto-scaling feature helps mitigate this issue.

When enabled (AUTO_SCALE_DIS_CSO or AUTO_SCALE_DIS_CSI bit = logic 0 in the *WC_CFG1* register), wetting current is reduced to 2 mA from 10 mA or 15 mA setting after switch closure is detected. The threshold used to determine a switch closure is the threshold configured in the *THRES_COMP* register.

The current reduction takes place N cycles after switch closure is detected on an input, where N depends on the setting of the DET_FILTER bits in the *CONFIG* register:

- DET_FILTER= 00: wetting current is reduced immediately in the next detection cycle after a closed switch is detected.
- DET_FILTER= 01: wetting current is reduced when a closed switch is detected and the switch status is stable for at least 2 consecutive detection cycles.
- DET_FILTER= 10: wetting current is reduced when a closed switch is detected and the switch status is stable for at least 3 consecutive detection cycles.
- DET_FILTER= 11: wetting current is reduced when a closed switch is detected and the switch status is stable for at least 4 consecutive detection cycles.

The wetting current is adjusted back to the original setting of 10 mA or 15 mA at a time of N cycles after an open switch is detected, where N again depends on the DET_FILTER bit setting in the *CONFIG* register. 図 8-16 depicts the behavior of the wetting current auto-scaling feature.

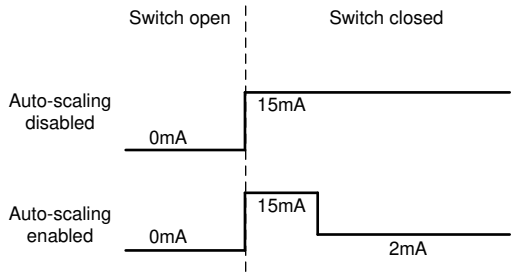



**図 8-16. Wetting Current Auto-scaling Behavior**

The wetting current auto-scaling only applies to 10 mA and 15 mA settings and is only available in continuous mode. If AUTO_SCALE_DIS_CSO or AUTO_SCALE_DIS_CSI bit is set to logic 1 in the *WC_CFG1* registers, the wetting current stays at its original setting when a closed switch is detected. Power dissipation needs to be closely monitored when wetting current auto-scaling is disabled for multiple inputs as the device could heat up quickly when high wetting current settings are used. If the auto-scaling feature is disabled in continuous mode, the total power dissipation can be approximated using 式 1.

$$P_{TOTAL} = V_S \times \left(I_{S\_CONT} + I_{WETT\,(TOTAL)}\right) \quad (1)$$

where $I_{WETT\ (TOTAL)}$ is the sum of all wetting currents from all input channels. Increase in device junction temperature can be calculated based on $P \times R_{\theta JA}$. The junction temperature must be below $T_{TSD}$ for proper device operation. An interrupt will be issued when the junction temperature exceeds $T_{TW}$ or $T_{TSD}$. For detailed description of the temperature monitoring, please refer to sections *Temperature Warning (TW)* and *Temperature Shutdown (TSD)*.

# 9 Programming

The SPI interface communication consists of the 4 pins: $\overline{CS}$, SCLK, SI, and SO. The interface can work with SCLK frequency up to 4 MHz.

## 9.1 SPI Communication Interface Buses

### 9.1.1 Chip Select ( $\overline{CS}$)

The system microcontroller selects the TIC10024-Q1 to receive communication using the $\overline{CS}$ pin. With the $\overline{CS}$ pin in a logic LOW state, command words may be sent to the TIC10024-Q1 through the serial input (SI) pin, and the device information can be retrieved by the microcontroller through the serial output (SO) pin. The falling edge of the $\overline{CS}$ enables the SO output and latches the content of the interrupt register INT_STAT. The microcontroller may issue a READ command to retrieve information stored in the registers. Rising edge on the $\overline{CS}$ pin initiates the following operations:

1. Disable the output driver and makes SO high-impedance.
2. $\overline{INT}$ pin is reset to logic HIGH if a READ command to the INT_STAT register was issued during $\overline{CS}$ = LOW.

To avoid corrupted data, it is essential the HIGH-to-LOW and LOW-to-HIGH transitions of the $\overline{CS}$ signal occur only when SCLK is in a logic LOW state. A clean $\overline{CS}$ signal is needed to ensure that no incomplete SPI words are sent to the device. The $\overline{CS}$ pin should be externally pulled up to VDD by a 10 kΩ resistor.

### 9.1.2 System Clock (SCLK)

The system clock (SCLK) input is used to clock the internal shift register of the TIC10024-Q1. The SI data is latched into the input shift register on the falling edge of the SCLK signal. The SO pin shifts the device stored information out on the rising edge of SCLK. The SO data is available for the microcontroller to read on the falling edge of SCLK.

False clocking of the shift register must be avoided to ensure validity of data and it is essential the SCLK pin be in a logic LOW state whenever $\overline{CS}$ makes any transition. Therefore, it is recommended that the SCLK pin gets pulled to a logic LOW state as long as the device is not accessed and $\overline{CS}$ is in a logic HIGH state. When the $\overline{CS}$ is in a logic HIGH state, any signal on the SCLK and SI pins will be ignored and the SO pin remains as a high impedance output. Refer to 図 9-1 and 図 9-2 for examples of typical SPI read and write sequence.

### 9.1.3 Slave In (SI)

The SI pin is used for serial instruction data input. SI information is latched into the input register on the falling edge of the SCLK. To program a complete word, 32 bits of information must be entered into the device. The SPI logic counts the number of bits clocked into the IC and enables data latching only if exactly 32 bits have been clocked in. In case the word length exceeds or does not meet the required length, the SPI_FAIL bit of the INT_STAT register is asserted to logic 1 and the $\overline{INT}$ pin will be asserted low. The data received is considered invalid. Note the SPI_FAIL bit is not flagged if SCLK is not present.

### 9.1.4 Slave Out (SO)

The SO pin is the output from the internal shift register. The SO pin remains high-impedance until the $\overline{CS}$ pin transitions to a logic LOW state. The negative transition of $\overline{CS}$ enables the SO output driver and drives the SO output to the HIGH state (by default). The first positive transition of SCLK makes the status data bit 31 available on the SO pin. Each successive positive clock makes the next status data bit available for the microcontroller to read on the falling edge of SCLK. The SI/SO shifting of the data follows a first-in, first-out scheme, with both input and output words transferring the most significant bit (MSB) first.

## 9.2 SPI Sequence

図 9-1 and 図 9-2 depict the SPI communication sequence during read and write operations for the TIC10024-Q1.

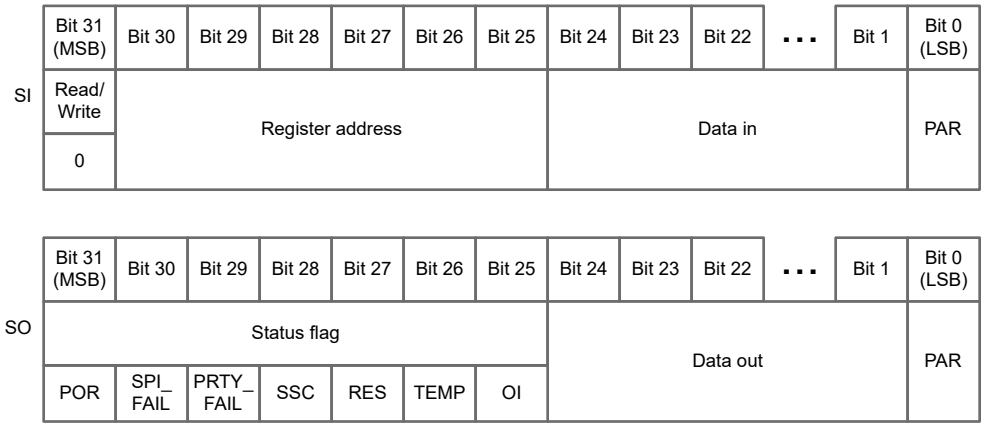



**図 9-1. TIC10024-Q1 Read SPI Sequence**

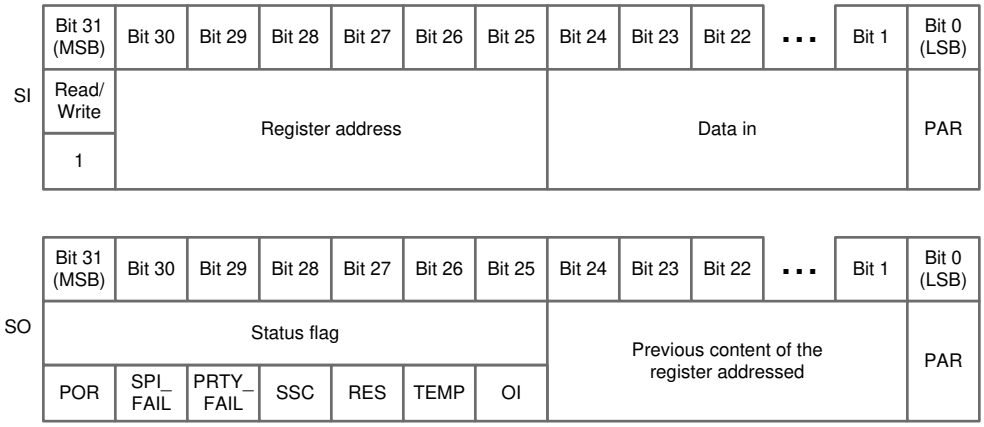



**図 9-2. TIC10024-Q1 Write SPI Sequence**

### 9.2.1 Read Operation

The Read/Write bit (bit 31) of the SI bus needs to be set to logic 0 for a READ operation. The 6-bits address of the register to be accessed follows next on the SI bus. The content from bit 24 to bit 1 does not represent a valid command for a read operation and will be ignored. The LSB (bit 0) is the parity bit used to detect communication errors.

On the SO bus, the status flags will be outputted from the TIC10024-Q1, followed by the data content in the register that was requested. The LSB is the parity bit used to detect communication errors.

Note there are several test mode registers used in the TIC10024-Q1 in addition to the normal functional registers, and a READ command to these test registers returns the register content. If a READ command is issued to an invalid register address, the TIC10024-Q1 returns all 0's.

### 9.2.2 Write Operation

The Read/Write bit (bit 31) on the SI bus needs to be set to 1 for a write operation. The 6-bits address of the register to be accessed follows next on the SI bus. Note the register needs to be a writable configuration register, or otherwise the command will be ignored. The content from bit 24 to bit 1 represents the data to be written to the register. The LSB (bit 0) is the parity bit used to detect communication errors.

On the SO bus, the status flags will be output from the TIC10024-Q1, followed by the previous data content of the written register. The previous content of the register is latched after the full register address is decoded in the SI command (after bit 25 is transmitted). The new data will replace the previous data content at the end of the SPI transaction if the SI write is a valid command (valid register address and no SPI/parity error). If the write command is invalid, the new data will be ignored and the register content will remain unchanged. The LSB is the parity bit used to detect communication errors.

Note there are several test mode registers used in the TIC10024-Q1 in addition to the normal functional registers. A WRITE command to these test registers has no effect on the register content, even though the register content is returned on the SO output. If a WRITE command is issued to an invalid register address, the SO output returns all 0's.

### 9.2.3 Status Flag

The status flags are output from SO during every READ or WRITE SPI transaction to indicate system conditions. These bits do not belong to an actual register, but their content is mirrored from the interrupt register INT_STAT. A READ command executed on the INT_STAT would clear both the bits inside the register and the status flag. The following table describes the information that can be obtained from each SPI status flag:

**表 9-1. TIC10024-Q1 SPI Status Flag Description**

| SYMBOL | NAME | DESCRIPTION |
|---|---|---|
| POR | Power-on Reset | This flag mirrors the POR bit in the interrupt register INT_STAT, and it indicates, if set to 1, that a reset event has occurred. This bit is asserted after a successful power-on-reset, hardware reset, or software reset. Refer to *セクション 8.3.5* for more details. |
| SPI_FAIL | SPI Error | This flag mirrors the SPI_FAIL bit in the interrupt register INT_STAT and it indicates, if set to 1, that the last SPI responder in (SI) transaction is invalid. To program a complete word, 32 bits of information must be entered into the device. The SPI logic counts the number of bits clocked into the IC and enables data latching only if exactly 32 bits have been clocked in. In case the word length exceeds or does not meet the required size, the SPI_FAIL bit, which mirrors its value to this SPI_FAIL status flag, of the interrupt register INT_STAT will be set to 1 and the $\overline{INT}$ pin will be asserted low. The data received will be considered invalid. Once the INT_STAT register is read, its content will be cleared on the rising edge of $\overline{CS}$. The SPI_FAIL status flag, which mirrors the SPI_FAIL bit in the INT_STAT register, will also be de-asserted. Note the SPI_FAIL bit is not flagged if SCLK is not present. |
| PRTY_FAIL | Parity Fail | This flag mirrors the PRTY_FAIL bit in the interrupt register INT_STAT and it indicates, if set to 1, that the last SPI responder in (SI) transaction has a parity error. The device uses odd parity. If the total number of ones in the received data (including the parity bit) is an even number, the received data is discarded. The $\overline{INT}$ will be asserted low and the PRTY_FAIL bit in the interrupt register (INT_STAT) is flagged to logic 1, and the PRTY_FAIL status flag, which mirrors the PRTY_FAIL bit in the INT_STAT register, is also set to 1. Once the INT_STAT register is read, its content will be cleared on the rising edge of $\overline{CS}$. The PRTY_FAIL status flag, which mirrors the PRTY_FAIL bit in the INT_STAT register, will also be de-asserted. |
| SSC | Switch State Change | This flag mirrors the SSC bit in the interrupt register INT_STAT and it indicates, if set to 1, that one or more switch inputs crossed a threshold. To determine the origin of the state change, the microcontroller can read the content of the register IN_STAT_COMP. Once the interrupt register (INT_STAT) is read, its content will be cleared on the rising edge of $\overline{CS}$. The SSC status flag, which mirrors the SSC bit in the INT_STAT register, will also be de-asserted. |
| RES | Reserved | This flag is reserved and is always at logic 0. |
| TEMP | Temperature Event | This flag is set to 1 if either Temperature Warning (TW) or Temperature Shutdown (TSD) bit in the interrupt register INT_STAT is flagged to 1. It indicates a TW event or a TSD event has occurred. It is also flagged to 1 if a TW event or a TSD event is cleared. The interrupt register INT_STAT should be read to determine which event occurred. The SPI commander can also read the IN_STAT_MISC register to get information on the temperature status of the device. Once the interrupt register (INT_STAT) is read, its content will be cleared on the rising edge of $\overline{CS}$, and the TEMP status flag will also be de-asserted. |
| OI | Other Interrupt | Other interrupt include interrupts such as OV, UV, CRC_CALC and CHK_FAIL. This flag will be asserted 1 when any of the above mentioned bits is flagged in the interrupt register INT_STAT. The interrupt register INT_STAT should be read to determine which event(s) occurred. The SPI commander can also read the IN_STAT_MISC register to get information on the latest status of the device. Once the INT_STAT register is read, its content will be cleared on the rising edge of $\overline{CS}$, and the OI status flag will also be de-asserted. |

## 9.3 Programming Guidelines

When configuring the TIC10024-Q1, it is critical to follow the programming guideline summarized below (see 表 9-2) to ensure proper behavior of the device:

**表 9-2. TIC10024-Q1 Programming Guidelines**

| Category | Programming Requirement |
|---|---|
| Clean Current Polling (if CCP_INx = 1 in the CCP_CFG1 register) | At least one input has to be enabled: IN_EN_x = 1 in the IN_EN register |
| Wetting current auto-scaling (if WC_CFG1 [22:21] != 2b'11) | • The wetting current auto-scaling feature is only activated in the continuous mode: POLL_EN = 0 (1)<br>• The wetting current auto-scaling only applies to 10mA or 15mA wetting currents: WC_INx bits = 3'b100, 3'b101, 3'b110, or 3'b111 in the WC_CFG0 and WC_CFG1 registers.(1) |
| Continuous mode<br>Polling mode | $t_{POLL\_TIME}$ and $t_{POLL\_ACT\_TIME}$ settings have to meet the below requirement: $t_{POLL\_TIM\ E} \geq 1.3 \times [\ t_{POLL\_ACT\_TIME} + n \times 24\ \mu s + 10\ \mu s]$(2)<br>• n: the number of enabled channels configured in register IN_EN<br>• $t_{POLL\_TIME}$: timing setting configured in CONFIG[4:1]<br>• $t_{POLL\_ACT\_TIME}$: timing setting configured in CONFIG[8:5] |

(1) These are soft requirements to take advantage of the wetting current auto-scaling feature. The feature takes no effect otherwise.
(2) If CCP is enabled, add tCCP_TRAN +tCCP_TIME, where tCCP_TIME is the timing setting configured in CCP_CFG0[6:4]

## 9.4 Register Maps

表 9-3 lists the memory-mapped registers for the TIC10024-Q1. All register offset addresses not listed in 表 9-3 should be considered as reserved locations and the register contents should not be modified.

**表 9-3. TIC10024-Q1 Registers**

| OFFSET | TYPE | RESET | ACRONYM | REGISTER NAME | SECTION |
|---|---|---|---|---|---|
| 1h | R | 120h | DEVICE_ID | Device ID Register | Go |
| 2h | RC | 1h | INT_STAT | Interrupt Status Register | Go |
| 3h | R | FFFFh | CRC | CRC Result Register | Go |
| 4h | R | 0h | IN_STAT_MISC | Miscellaneous Status Register | Go |
| 5h | R | 0h | IN_STAT_COMP | Comparator Status Register | Go |
| 6h-19h | — | — | RESERVED | RESERVED | — |
| 1Ah | R/W | 0h | CONFIG | Device Global Configuration Register | Go |
| 1Bh | R/W | 0h | IN_EN | Input Enable Register | Go |
| 1Ch | R/W | 0h | CS_SELECT | Current Source/Sink Selection Register | Go |
| 1Dh-1Eh | R/W | 0h | WC_CFG0, WC_CFG1 | Wetting Current Configuration Register | Go |
| 1Fh-20h | R/W | 0h | CCP_CFG0, CCP_CFG1 | Clean Current Polling Register | Go |
| 21h | R/W | 0h | THRES_COMP | Comparator Threshold Control Register | Go |
| 22h-23h | R/W | 0h | INT_EN_COMP1, INT_EN_COMP2 | Comparator Input Interrupt Generation Control Register | Go |
| 24h | R/W | 0h | INT_EN_CFG0 | Global Interrupt Generation Control Register | Go |
| 25h-32h | — | — | RESERVED | RESERVED | — |

### 9.4.1 DEVICE_ID register (Offset = 1h) [reset = 20h]

DEVICE_ID is shown in 図 9-3 and described in 表 9-4.

Return to Summary Table.

This register represents the device ID of the TIC10024-Q1.

**図 9-3. DEVICE_ID Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | | | | | |
| R-0h | | | | | | | | | | | |
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | MAJOR | | | | | | | MINOR | | | |
| R-0h | R-12h | | | | | | | R-0h | | | |

LEGEND: R = Read only

**表 9-4. DEVICE_ID Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23-11 | RESERVED | R | 0h | RESERVED |
| 10-4 | MAJOR | R | 12h | These 7 bits represents major revision ID. For TIC10024-Q1 the major revision ID is 12h. |
| 3-0 | MINOR | R | 0h | These 4 bits represents minor revision ID. For TIC10024-Q1 the minor revision ID is 0h. |

### 9.4.2 INT_STAT Register (Offset = 2h) [reset = 1h]

INT_STAT is shown in 図 9-4 and described in 表 9-5.

Return to Summary Table.

This register records the information of the event as it occurs in the device. A READ command executed on this register clears its content and resets the register to its default value. The $\overline{INT}$ pin is released at the rising edge of the $\overline{CS}$ pin from the READ command.

**図 9-4. INT_STAT Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | CHK_FAIL | RESERVED | | | | CRC_CALC |
| R-0h | | RC-0h | R-0h | | | | RC-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| UV | OV | TW | TSD | SSC | PRTY_FAIL | SPI_FAIL | POR |
| RC-0h | RC-0h | RC-0h | RC-0h | RC-0h | RC-0h | RC-0h | RC-1h |

LEGEND: R = Read only; RC = Read to clear

**表 9-5. INT_STAT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23-14 | RESERVED | R | 0h | RESERVED |
| 13 | CHK_FAIL | RC | 0h | 0h = Default factory setting is successfully loaded upon device initialization or the event status got cleared after a READ command was executed on the INT_STAT register.<br>1h = An error is detected when loading factory settings into the device upon device initialization.<br>During device initialization, factory settings are programmed into the device to allow proper device operation. The device performs a self-check after the device is programmed to diagnose whether correct settings are loaded. If the self-check returns an error, the CHK_FAIL bit is flagged to logic 1 along with the POR bit. The host controller is then recommended to initiate a software reset (see section Software Reset) to re-initialize the device and allow correct settings to be re-programmed. |
| 12-9 | RESERVED | R | 0h | RESERVED |
| 8 | CRC_CALC | RC | 0h | 0h = CRC calculation is running, not started, or was acknowledged after a READ command was executed on the INT_STAT register.<br>1h = CRC calculation is finished.<br>CRC calculation (see section Cyclic Redundancy Check (CRC)) can be triggered to make sure correct register values are programmed into the device. Once the calculation is completed, the CRC_CALC bit is flagged to logic 1 to indicate completion of the calculation, and the result can then be accessed from the CRC (offset = 3h) register. |

**表 9-5. INT_STAT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | UV | RC | 0h | 0h = No under-voltage condition occurred or cleared on the $V_S$ pin, or the event status got cleared after a READ command was executed on the INT_STAT register.<br>1h = Under-voltage condition occurred or cleared on the $V_S$ pin.<br>When the UV bit is flagged to logic 1, it indicates the Under-Voltage (UV) event has occurred. The bit is also flagged to logic 1 when the event clears. For more details about the UV operation, please refer to section VS under-voltage (UV) condition. |
| 6 | OV | RC | 0h | 0h = No over-voltage condition occurred or cleared on the $V_S$ pin, or the event status got cleared after a READ command was executed on the INT_STAT register.<br>1h = Over-voltage condition occurred or cleared on the $V_S$ pin.<br>When the OV bit is flagged to logic 1, it indicates the Over-Voltage (OV) event has occurred. The bit is also flagged to logic 1 when the event clears. For more details about the OV operation, please refer to section VS over-voltage (OV) condition. |
| 5 | TW | RC | 0h | 0h = No temperature warning event occurred or the event status got cleared after a READ command was executed on the INT_STAT register.<br>1h = Temperature warning event occurred or cleared.<br>When the TW bit is flagged to logic 1, it indicates the temperature warning event has occurred. The bit is also flagged to logic 1 when the event clears. For more details about the temperature warning operation, please refer to section Temperature Warning (TW) |
| 4 | TSD | RC | 0h | 0h = No temperature Shutdown event occurred or the event status got cleared after a READ command was executed on the INT_STAT register.<br>1h = Temperature Shutdown event occurred or cleared.<br>When the TSD bit is flagged to logic 1, it indicates the temperature shutdown event has occurred. The bit is also flagged to logic 1 when the event clears. For more details about the temperature shutdown operation, please refer to section Temperature shutdown (TSD) |
| 3 | SSC | RC | 0h | 0h = No switch state change occurred or the status got cleared after a READ command was executed on the INT_STAT register.<br>1h = Switch state change occurred.<br>The Switch State Change (SSC) bit indicates whether input threshold crossing has occurred from switch inputs IN0 to IN23. This bit is also flagged to logic 1 after the first polling cycle is completed after device polling is triggered. |
| 2 | PRTY_FAIL | RC | 0h | 0h = No parity error occurred in the last received SI stream or the error status got cleared after a READ command was executed on the INT_STAT register.<br>1h = Parity error occurred.<br>When the PRTY_FAIL bit is flagged to logic 1, it indicates the last SPI responder in (SI) transaction has a parity error. The device uses odd parity. If the total number of ones in the received data (including the parity bit) is an even number, the received data is discarded. The value of this register bit is mirrored to the PRTY_FLAG SPI status flag. |

**表 9-5. INT_STAT Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 1 | SPI_FAIL | RC | 0h | 0h = 32 clock pulse during a $\overline{CS}$ = low sequence was detected or the error status got cleared after a READ command was executed on the INT_STAT register.<br>1h = SPI error occurred<br>When the SPI_FAIL bit is flagged to logic 1, it indicates the last SPI responder in (SI) transaction is invalid. To program a complete word, 32 bits of information must be entered into the device. The SPI logic counts the number of bits clocked into the IC and enables data latching only if exactly 32 bits have been clocked in. In case the word length exceeds or does not meet the required length, the SPI_FAIL bit is flagged to logic 1, and the data received is considered invalid. The value of this register bit is mirrored to the SPI_FLAG SPI status flag. Note the SPI_FAIL bit is not flagged if SCLK is not present. |
| 0 | POR | RC | 1h | 0h = no Power-On-Reset (POR) event occurred or the status got cleared after a READ command was executed on the INT_STAT register.<br>1h = Power-On-Reset (POR) event occurred.<br>The Power-On-Reset (POR) interrupt bit indicates whether a reset event has occurred. A reset event sets the registers to their default values and re-initializes the device state machine. This bit is asserted after a successful power-on-reset, hardware reset, or software reset. The value of this register bit is mirrored to the POR SPI status flag. |

### 9.4.3 CRC Register (Offset = 3h) [reset = FFFFh]

CRC is shown in 図 9-5 and described in 表 9-6.

Return to Summary Table.

This register returns the CRC-16-CCCIT calculation result. The microcontroller can compare this value with its own calculated value to ensure correct register settings are programmed to the device.

**図 9-5. CRC Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | | CRC | | | | | | | | | | | | | | | |
| R-0h | | | | | | | | R-FFFFh | | | | | | | | | | | | | | | |

LEGEND: R = Read only

**表 9-6. CRC Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23-16 | RESERVED | R | 0h | Reserved |
| 15-0 | CRC | R | FFFFh | CRC-16-CCITT calculation result: Bit1: LSB of CRC Bit16: MSB or CRC |

### 9.4.4 IN_STAT_MISC Register (Offset = 4h) [reset = 0h]

IN_STAT_MISC is shown in 図 9-6 and described in 表 9-7.

Return to Summary Table.

This register indicates current device status unrelated to switch input monitoring.

**図 9-6. IN_STAT_MISC Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | UV_STAT | OV_STAT | TW_STAT | TSD_STAT |
| R-0h | | | | R-0h | R-0h | R-0h | R-0h |

**表 9-7. IN_STAT_MISC Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23-4 | RESERVED | R | 0h | Reserved |
| 3 | UV_STAT | R | 0h | 0h = $V_S$ voltage is above the under-voltage condition threshold.<br>1h = $V_S$ voltage is below the under-voltage condition threshold. |
| 2 | OV_STAT | R | 0h | 0h = $V_S$ voltage is below the over-voltage condition threshold.<br>1h = $V_S$ voltage is above the over-voltage condition threshold. |
| 1 | TW_STAT | R | 0h | 0h = Device junction temperature is below the temperature warning threshold $T_{TW}$.<br>1h = Device junction temperature is above the temperature warning threshold $T_{TW}$. |
| 0 | TSD_STAT | R | 0h | 0h = Device junction temperature is below the temperature shutdown threshold $T_{TSD}$.<br>1h = Device junction temperature is above the temperature shutdown threshold $T_{TSD}$. |

### 9.4.5 IN_STAT_COMP Register (Offset = 5h) [reset = 0h]

IN_STAT_COMP is shown in 図 9-7 and described in 表 9-8.

Return to Summary Table.

This register indicates whether an input is below or above the comparator threshold.

**図 9-7. IN_STAT_COMP Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| INC_23 | INC_22 | INC_21 | INC_20 | INC_19 | INC_18 | INC_17 | INC_16 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| INC_15 | INC_14 | INC_13 | INC_12 | INC_11 | INC_10 | INC_9 | INC_8 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INC_7 | INC_6 | INC_5 | INC_4 | INC_3 | INC_2 | INC_1 | INC_0 |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R = Read only

**表 9-8. IN_STAT_COMP Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23 | INC_23 | R | 0h | 0h = Input IN23 is below the comparator threshold.<br>1h = Input IN23 is above the comparator threshold. |
| 22 | INC_22 | R | 0h | 0h = Input IN22 is below the comparator threshold.<br>1h = Input IN22 is above the comparator threshold. |
| 21 | INC_21 | R | 0h | 0h = Input IN21 is below the comparator threshold.<br>1h = Input IN21 is above the comparator threshold. |
| 20 | INC_20 | R | 0h | 0h = Input IN20 is below the comparator threshold.<br>1h = Input IN20 is above the comparator threshold. |
| 19 | INC_19 | R | 0h | 0h = Input IN19 is below the comparator threshold.<br>1h = Input IN19 is above the comparator threshold. |
| 18 | INC_18 | R | 0h | 0h = Input IN18 is below the comparator threshold.<br>1h = Input IN18 is above the comparator threshold. |
| 17 | INC_17 | R | 0h | 0h = Input IN17 is below the comparator threshold.<br>1h = Input IN17 is above the comparator threshold. |
| 16 | INC_16 | R | 0h | 0h = Input IN16 is below the comparator threshold.<br>1h = Input IN16 is above the comparator threshold. |
| 15 | INC_15 | R | 0h | 0h = Input IN15 is below the comparator threshold.<br>1h = Input IN15 is above the comparator threshold. |
| 14 | INC_14 | R | 0h | 0h = Input IN14 is below the comparator threshold.<br>1h = Input IN14 is above the comparator threshold. |
| 13 | INC_13 | R | 0h | 0h = Input IN13 is below the comparator threshold.<br>1h = Input IN13 is above the comparator threshold. |
| 12 | INC_12 | R | 0h | 0h = Input IN12 is below the comparator threshold.<br>1h = Input IN12 is above the comparator threshold. |
| 11 | INC_11 | R | 0h | 0h = Input IN11 is below the comparator threshold.<br>1h = Input IN11 is above the comparator threshold. |

表 9-8. IN_STAT_COMP Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 10 | INC_10 | R | 0h | 0h = Input IN10 is below the comparator threshold.<br>1h = Input IN10 is above the comparator threshold. |
| 9 | INC_9 | R | 0h | 0h = Input IN9 is below the comparator threshold.<br>1h = Input IN9 is above the comparator threshold. |
| 8 | INC_8 | R | 0h | 0h = Input IN8 is below the comparator threshold.<br>1h = Input IN8 is above the comparator threshold. |
| 7 | INC_7 | R | 0h | 0h = Input IN7 is below the comparator threshold.<br>1h = Input IN7 is above the comparator threshold. |
| 6 | INC_6 | R | 0h | 0h = Input IN6 is below the comparator threshold.<br>1h = Input IN6 is above the comparator threshold. |
| 5 | INC_5 | R | 0h | 0h = Input IN5 is below the comparator threshold.<br>1h = Input IN5 is above the comparator threshold. |
| 4 | INC_4 | R | 0h | 0h = Input IN4 is below the comparator threshold.<br>1h = Input IN4 is above the comparator threshold. |
| 3 | INC_3 | R | 0h | 0h = Input IN3 is below the comparator threshold.<br>1h = Input IN3 is above the comparator threshold. |
| 2 | INC_2 | R | 0h | 0h = Input IN2 is below the comparator threshold.<br>1h = Input IN2 is above the comparator threshold. |
| 1 | INC_1 | R | 0h | 0h = Input IN1 is below the comparator threshold.<br>1h = Input IN1 is above the comparator threshold. |
| 0 | INC_0 | R | 0h | 0h = Input IN0 is below the comparator threshold.<br>1h = Input IN0 is above the comparator threshold. |

### 9.4.6 CONFIG Register (Offset = 1Ah) [reset = 0h]

CONFIG is shown in 図 9-8 and described in 表 9-9.

Return to Summary Table.

**図 9-8. CONFIG Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | TW_CUR_DIS_CSI |
| R-0h | | | | | | | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| DET_FILTER | | TW_CUR_DIS_CSO | INT_CONFIG | TRIGGER | POLL_EN | CRC_T | POLL_ACT_TIME |
| R/W-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| POLL_ACT_TIME | | | POLL_TIME | | | | RESET |
| R/W-0h | | | R/W-0h | | | | R/W-0h |

LEGEND: R/W = Read/Write

**表 9-9. CONFIG Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23-17 | RESERVED | R | 0h | Reserved |
| 16 | TW_CUR_DIS_CSI | R/W | 0h | 0h = Enable wetting current reduction (to 2 mA) for 10mA and 15mA settings upon TW event for all inputs enabled with CSI.<br>1h = Disable wetting current reduction (to 2 mA) for 10mA and 15mA settings upon TW event for all inputs enabled with CSI. |
| 15-14 | DET_FILTER | R/W | 0h | For detailed descriptions for the detection filter, refer to section Detection Filter.<br>0h = every sample is valid and taken for threshold evaluation<br>1h = 2 consecutive and equal samples required to be valid data<br>2h = 3 consecutive and equal samples required to be valid data<br>3h = 4 consecutive and equal samples required to be valid data |
| 13 | TW_CUR_DIS_CSO | R/W | 0h | 0h = Enable wetting current reduction (to 2mA) for 10mA and 15mA settings upon TW event for all inputs enabled with CSO.<br>1h = Disable wetting current reduction (to 2mA) for 10mA and 15mA settings upon TW event for all inputs enabled with CSO. |
| 12 | INT_CONFIG | R/W | 0h | For detailed descriptions for the $\overline{\text{INT}}$ pin assertion scheme, refer to section Interrupt Generation and /INT Assertion.<br>0h = $\overline{\text{INT}}$ pin assertion scheme set to static<br>1h = $\overline{\text{INT}}$ pin assertion scheme set to dynamic |

**表 9-9. CONFIG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 11 | TRIGGER | R/W | 0h | When the TRIGGER bit is set to logic 1, normal device operation (wetting current activation and polling) starts. To stop device operation and keep the device in an idle state, de-assert this bit to 0. After device normal operation is triggered, if at any time the device setting needs to be re-configured, the microcontroller is required to first set the bit TRIGGER to logic 0 to stop device operation. Once the re-configuration is completed, the microcontroller can set the TRIGGER bit back to logic 1 to re-start device operation. If re-configuration is done on the fly without first stopping the device operation, false switch status could be reported and accidental interrupt might be issued. The following register bits are the exception and can be configured when TRIGGER bit is set to logic 1:<br>– TRIGGER (bit 11 of the CONFIG register)<br>– CRC_T (bit 9 of the CONFIG register)<br>– RESET (bit 0 of the CONFIG register)<br>– The CCP_CFG1 register<br>0h = Stop TIC10024-Q1 from normal operation.<br>1h = Trigger TIC10024-Q1 normal operation |
| 10 | POLL_EN | R/W | 0h | 0h = Polling disabled. Device operates in continuous mode.<br>1h = Polling enabled and the device operates in one of the polling modes. |
| 9 | CRC_T | R/W | 0h | Set this bit to 1 to trigger a CRC calculation on all the configuration register bits. Once triggered, it is strongly recommended the SPI commander does not change the content of the configuration registers until the CRC calculation is completed to avoid erroneous CRC calculation result. The TIC10024-Q1 sets the CRC_CALC interrupt bit and asserts the $\overline{INT}$ pin low when the CRC calculation is completed. The calculated result will be available in the CRC register. This bit self-clears back to 0 after CRC calculation is executed.<br>0h = no CRC calculation triggered<br>1h = trigger CRC calculation |
| 8-5 | POLL_ACT_TIME | R/W | 0h | 0h = 64µs<br>1h = 128µs<br>2h = 192µs<br>3h = 256µs<br>4h = 320µs<br>5h = 384µs<br>6h = 448µs<br>7h = 512µs<br>8h = 640µs<br>9h = 768µs<br>Ah = 896µs<br>Bh = 1024µs<br>Ch = 2048µs<br>Dh-15h = 512µs (most frequently-used setting) |

**表 9-9. CONFIG Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 4-1 | POLL_TIME | R/W | 0h | 0h = 2ms<br>1h = 4ms<br>2h = 8ms<br>3h = 16ms<br>4h = 32ms<br>5h = 48ms<br>6h = 64ms<br>7h = 128ms<br>8h = 256ms<br>9h = 512ms<br>Ah = 1024ms<br>Bh = 2048ms<br>Ch = 4096ms<br>Dh-15h = 8ms (most frequently-used setting) |
| 0 | RESET | R/W | 0h | 0h = No reset<br>1h = Trigger software reset of the device. |

### 9.4.7 IN_EN Register (Offset = 1Bh) [reset = 0h]

IN_EN is shown in 図 9-9 and described in 表 9-10.

Return to Summary Table.

**図 9-9. IN_EN Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| IN_EN_23 | IN_EN_22 | IN_EN_21 | IN_EN_20 | IN_EN_19 | IN_EN_18 | IN_EN_17 | IN_EN_16 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| IN_EN_15 | IN_EN_14 | IN_EN_13 | IN_EN_12 | IN_EN_11 | IN_EN_10 | IN_EN_9 | IN_EN_8 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| IN_EN_7 | IN_EN_6 | IN_EN_5 | IN_EN_4 | IN_EN_3 | IN_EN_2 | IN_EN_1 | IN_EN_0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write

**表 9-10. IN_EN Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23 | IN_EN_23 | R/W | 0h | 0h = Input channel IN23 disabled. Polling sequence skips this channel<br>1h = Input channel IN23 enabled. |
| 22 | IN_EN_22 | R/W | 0h | 0h = Input channel IN22 disabled. Polling sequence skips this channel<br>1h = Input channel IN22 enabled. |
| 21 | IN_EN_21 | R/W | 0h | 0h = Input channel IN21 disabled. Polling sequence skips this channel<br>1h = Input channel IN21 enabled. |
| 20 | IN_EN_20 | R/W | 0h | 0h = Input channel IN20 disabled. Polling sequence skips this channel<br>1h = Input channel IN20 enabled. |
| 19 | IN_EN_19 | R/W | 0h | 0h = Input channel IN19 disabled. Polling sequence skips this channel<br>1h = Input channel IN19 enabled. |
| 18 | IN_EN_18 | R/W | 0h | 0h = Input channel IN18 disabled. Polling sequence skips this channel<br>1h = Input channel IN18 enabled. |
| 17 | IN_EN_17 | R/W | 0h | 0h = Input channel IN17 disabled. Polling sequence skips this channel<br>1h = Input channel IN17 enabled. |
| 16 | IN_EN_16 | R/W | 0h | 0h = Input channel IN16 disabled. Polling sequence skips this channel<br>1h = Input channel IN16 enabled. |
| 15 | IN_EN_15 | R/W | 0h | 0h = Input channel IN15 disabled. Polling sequence skips this channel<br>1h = Input channel IN15 enabled. |

**表 9-10. IN_EN Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 14 | IN_EN_14 | R/W | 0h | 0h = Input channel IN14 disabled. Polling sequence skips this channel<br>1h = Input channel IN14 enabled. |
| 13 | IN_EN_13 | R/W | 0h | 0h = Input channel IN13 disabled. Polling sequence skips this channel<br>1h = Input channel IN13 enabled. |
| 12 | IN_EN_12 | R/W | 0h | 0h = Input channel IN12 disabled. Polling sequence skips this channel<br>1h = Input channel IN12 enabled. |
| 11 | IN_EN_11 | R/W | 0h | 0h = Input channel IN11 disabled. Polling sequence skips this channel<br>1h = Input channel IN11 enabled. |
| 10 | IN_EN_10 | R/W | 0h | 0h = Input channel IN10 disabled. Polling sequence skips this channel<br>1h = Input channel IN10 enabled. |
| 9 | IN_EN_9 | R/W | 0h | 0h = Input channel IN9 disabled. Polling sequence skips this channel<br>1h = Input channel IN9 enabled. |
| 8 | IN_EN_8 | R/W | 0h | 0h = Input channel IN8 disabled. Polling sequence skips this channel<br>1h = Input channel IN8 enabled. |
| 7 | IN_EN_7 | R/W | 0h | 0h = Input channel IN7 disabled. Polling sequence skips this channel<br>1h = Input channel IN7 enabled. |
| 6 | IN_EN_6 | R/W | 0h | 0h = Input channel IN6 disabled. Polling sequence skips this channel<br>1h = Input channel IN6 enabled. |
| 5 | IN_EN_5 | R/W | 0h | 0h = Input channel IN5 disabled. Polling sequence skips this channel<br>1h = Input channel IN5 enabled. |
| 4 | IN_EN_4 | R/W | 0h | 0h = Input channel IN4 disabled. Polling sequence skips this channel<br>1h = Input channel IN4 enabled. |
| 3 | IN_EN_3 | R/W | 0h | 0h = Input channel IN3 disabled. Polling sequence skips this channel<br>1h = Input channel IN3 enabled. |
| 2 | IN_EN_2 | R/W | 0h | 0h = Input channel IN2 disabled. Polling sequence skips this channel<br>1h = Input channel IN2 enabled. |
| 1 | IN_EN_1 | R/W | 0h | 0h = Input channel IN1 disabled. Polling sequence skips this channel<br>1h = Input channel IN1 enabled. |
| 0 | IN_EN_0 | R/W | 0h | 0h = Input channel IN0 disabled. Polling sequence skips this channel<br>1h = Input channel IN0 enabled. |

### 9.4.8 CS_SELECT Register (Offset = 1Ch) [reset = 0h]

CS_SELECT is shown in 図 9-10 and described in 表 9-11.

Return to Summary Table.

**図 9-10. CS_SELECT Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | | | | | |
| R-0h | | | | | | | | | | | |
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | CS_IN9 | CS_IN8 | CS_IN7 | CS_IN6 | CS_IN5 | CS_IN4 | CS_IN3 | CS_IN2 | CS_IN1 | CS_IN0 |
| R-0h | | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; R = Read only

**表 9-11. CS_SELECT Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23-10 | RESERVED | R | 0h | Reserved |
| 9 | CS_IN9 | R/W | 0h | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 8 | CS_IN8 | R/W | 0h | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 7 | CS_IN7 | R/W | 0h | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 6 | CS_IN6 | R/W | 0h | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 5 | CS_IN5 | R/W | 0h | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 4 | CS_IN4 | R/W | 0h | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 3 | CS_IN3 | R/W | 0h | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 2 | CS_IN2 | R/W | 0h | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 1 | CS_IN1 | R/W | 0h | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |
| 0 | CS_IN0 | R/W | 0h | 0h = Current Source (CSO) selected<br>1h = Current Sink (CSI) selected |

### 9.4.9 WC_CFG0 Register (Offset = 1Dh) [reset = 0h]

WC_CFG0 is shown in 図 9-11 and described in 表 9-12.

Return to Summary Table.

**図 9-11. WC_CFG0 Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| WC_IN11 | | | WC_IN10 | | | WC_IN8_IN9 | | | WC_IN6_IN7 | | |
| R/W-0h | | | R/W-0h | | | R/W-0h | | | R/W-0h | | |
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WC_IN5 | | | WC_IN4 | | | WC_IN2_IN3 | | | WC_IN0_IN1 | | |
| R/W-0h | | | R/W-0h | | | R/W-0h | | | R/W-0h | | |

LEGEND: R/W = Read/Write

**表 9-12. WC_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23-21 | WC_IN11 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |
| 20-18 | WC_IN10 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |
| 17-15 | WC_IN8_IN9 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |
| 14-12 | WC_IN6_IN7 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |
| 11-9 | WC_IN5 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |

表 9-12. WC_CFG0 Register Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 8-6 | WC_IN4 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |
| 5-3 | WC_IN2_IN3 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |
| 2-0 | WC_IN0_IN1 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |

### 9.4.10 WC_CFG1 Register (Offset = 1Eh) [reset = 0h]

WC_CFG1 is shown in 図 9-12 and described in 表 9-13.

Return to Summary Table.

**図 9-12. WC_CFG1 Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | AUTO_SCALE_DIS_CSI | AUTO_SCALE_DIS_CSO | WC_IN23 | | | WC_IN22 | | | WC_IN20_IN21 | | |
| R-0h | R/W-0h | R/W-0h | R/W-0h | | | R/W-0h | | | R/W-0h | | |
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WC_IN18_IN19 | | | WC_IN16_IN17 | | | WC_IN14_IN15 | | | WC_IN12_IN13 | | |
| R/W-0h | | | R/W-0h | | | R/W-0h | | | R/W-0h | | |

LEGEND: R/W = Read/Write; R = Read only

**表 9-13. WC_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23 | RESERVED | R | 0h | Reserved |
| 22 | AUTO_SCALE_DIS_CSI | R/W | 0h | 0h = Enable wetting current auto-scaling (to 2mA) in continuous mode for 10mA and 15mA settings upon switch closure for all inputs enabled with CSI<br>1h = Disable wetting current auto-scaling (to 2mA) in continuous mode for 10mA and 15mA settings upon switch closure for all inputs enabled with CS<br>For detailed descriptions for the wetting current auto-scaling, refer to section Wetting Current Auto-Scaling. |
| 21 | AUTO_SCALE_DIS_CSO | R/W | 0h | 0h = Enable wetting current auto-scaling (to 2mA) in continuous mode for 10mA and 15mA settings upon switch closure for all inputs enabled with CSO<br>1h = Disable wetting current auto-scaling (to 2mA) in continuous mode for 10mA and 15mA settings upon switch closure for all inputs enabled with CSO<br>For detailed descriptions for the wetting current auto-scaling, refer to section Wetting Current Auto-Scaling. |
| 20-18 | WC_IN23 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |
| 17-15 | WC_IN22 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |

**表 9-13. WC_CFG1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 14-12 | WC_IN20_IN21 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |
| 11-9 | WC_IN18_IN19 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |
| 8-6 | WC_IN16_IN17 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |
| 5-3 | WC_IN14_IN15 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |
| 2-0 | WC_IN12_IN13 | R/W | 0h | 0h = no wetting current<br>1h = 1mA (typ.) wetting current<br>2h = 2mA (typ.) wetting current<br>3h = 5mA (typ.) wetting current<br>4h = 10mA (typ.) wetting current<br>5h-7h = 15mA (typ.) wetting current |

### 9.4.11 CCP_CFG0 Register (Offset = 1Fh) [reset = 0h]

CCP_CFG0 is shown in 図 9-13 and described in 表 9-14.

Return to Summary Table.

**図 9-13. CCP_CFG0 Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | | | | | |
| R-0h | | | | | | | | | | | |
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED | | | | | CCP_TIME | | | WC_CCP3 | WC_CCP2 | WC_CCP1 | WC_CCP0 |
| R-0h | | | | | R-0h | | | R-0h | R-0h | R-0h | R-0h |

LEGEND: R/W = Read/Write; R = Read only

**表 9-14. CCP_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23-7 | RESERVED | R | 0h | Reserved |
| 6-4 | CCP_TIME | R/W | 0h | Wetting current activation time in CCP mode<br>0h = 64µs<br>1h = 128µs<br>2h = 192µs<br>3h = 256µs<br>4h = 320µs<br>5h = 384µs<br>6h = 448µs<br>7h = 512µs |
| 3 | WC_CCP3 | R/W | 0h | Wetting current setting for IN18 to IN23 in CCP mode<br>0h = 10mA (typ.) wetting current<br>1h = 15mA (typ.) wetting current |
| 2 | WC_CCP2 | R/W | 0h | Wetting current setting for IN12 to IN17 in CCP mode<br>0h = 10mA (typ.) wetting current<br>1h = 15mA (typ.) wetting current |
| 1 | WC_CCP1 | R/W | 0h | Wetting current setting for IN6 to IN11 in CCP mode<br>0h = 10mA (typ.) wetting current<br>1h = 15mA (typ.) wetting current |
| 0 | WC_CCP0 | R/W | 0h | Wetting current setting for IN0 to IN5 in CCP mode<br>0h = 10mA (typ.) wetting current<br>1h = 15mA (typ.) wetting current |

### 9.4.12 CCP_CFG1 Register (Offset = 20h) [reset = 0h]

CCP_CFG1 is shown in 図 9-14 and described in 表 9-15.

Return to Summary Table.

**図 9-14. CCP_CFG1 Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| CCP_IN23 | CCP_IN22 | CCP_IN21 | CCP_IN20 | CCP_IN19 | CCP_IN18 | CCP_IN17 | CCP_IN16 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| CCP_IN15 | CCP_IN14 | CCP_IN13 | CCP_IN12 | CCP_IN11 | CCP_IN10 | CCP_IN9 | CCP_IN8 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CCP_IN7 | CCP_IN6 | CCP_IN5 | CCP_IN4 | CCP_IN3 | CCP_IN2 | CCP_IN1 | CCP_IN0 |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write

**表 9-15. CCP_CFG1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23 | CCP_IN23 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 22 | CCP_IN22 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 21 | CCP_IN21 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 20 | CCP_IN20 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 19 | CCP_IN19 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 18 | CCP_IN18 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 17 | CCP_IN17 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 16 | CCP_IN16 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 15 | CCP_IN15 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 14 | CCP_IN14 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 13 | CCP_IN13 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 12 | CCP_IN12 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 11 | CCP_IN11 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 10 | CCP_IN10 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |

**表 9-15. CCP_CFG1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 9 | CCP_IN9 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 8 | CCP_IN8 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 7 | CCP_IN7 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 6 | CCP_IN6 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 5 | CCP_IN5 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 4 | CCP_IN4 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 3 | CCP_IN3 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 2 | CCP_IN2 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 1 | CCP_IN1 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |
| 0 | CCP_IN0 | R/W | 0h | 0h = no CCP wetting current<br>1h = CCP wetting current activated |

### 9.4.13 THRES_COMP Register (Offset = 21h) [reset = 0h]

THRES_COMP is shown in 図 9-15 and described in 表 9-16.

Return to Summary Table.

**図 9-15. THRES_COMP Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | THRES_COMP_IN20_IN23 | | THRES_COMP_IN16_IN19 | |
| R-0h | | | | R/W-0h | | R/W-0h | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| THRES_COMP_IN12_IN15 | | THRES_COMP_IN8_IN11 | | THRES_COMP_IN4_IN7 | | THRES_COMP_IN0_IN3 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

LEGEND: R/W = Read/Write; R = Read only

**表 9-16. THRES_COMP Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23-12 | RESERVED | R | 0h | Reserved |
| 11-10 | THRES_COMP_IN20_IN23 | R/W | 0h | These 2 bits configures the comparator thresholds for input channels IN20 to IN23<br>0h = comparator threshold set to 2V<br>1h = comparator threshold set to 2.7V<br>2h = comparator threshold set to 3V<br>3h = comparator threshold set to 4V |
| 9-8 | THRES_COMP_IN16_IN19 | R/W | 0h | These 2 bits configures the comparator thresholds for input channels IN16 to IN19<br>0h = comparator threshold set to 2V<br>1h = comparator threshold set to 2.7V<br>2h = comparator threshold set to 3V<br>3h = comparator threshold set to 4V |
| 7-6 | THRES_COMP_IN12_IN15 | R/W | 0h | These 2 bits configures the comparator thresholds for input channels IN12 to IN15<br>0h = comparator threshold set to 2V<br>1h = comparator threshold set to 2.7V<br>2h = comparator threshold set to 3V<br>3h = comparator threshold set to 4V |
| 5-4 | THRES_COMP_IN8_IN11 | R/W | 0h | These 2 bits configures the comparator thresholds for input channels IN8 to IN11<br>0h = comparator threshold set to 2V<br>1h = comparator threshold set to 2.7V<br>2h = comparator threshold set to 3V<br>3h = comparator threshold set to 4V |
| 3-2 | THRES_COMP_IN4_IN7 | R/W | 0h | These 2 bits configures the comparator thresholds for input channels IN4 to IN7<br>0h = comparator threshold set to 2V<br>1h = comparator threshold set to 2.7V<br>2h = comparator threshold set to 3V<br>3h = comparator threshold set to 4V |

**表 9-16. THRES_COMP Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 1-0 | THRES_COMP_IN0_IN3 | R/W | 0h | These 2 bits configures the comparator thresholds for input channels IN0 to IN3<br>0h = comparator threshold set to 2V<br>1h = comparator threshold set to 2.7V<br>2h = comparator threshold set to 3V<br>3h = comparator threshold set to 4V |

### 9.4.14 INT_EN_COMP1 Register (Offset = 22h) [reset = 0h]

INT_EN_COMP1 is shown in 図 9-16 and described in 表 9-17.

Return to Summary Table.

**図 9-16. INT_EN_COMP1 Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| INC_EN_11 | | INC_EN_10 | | INC_EN_9 | | INC_EN_8 | | INC_EN_7 | | INC_EN_6 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INC_EN_5 | | INC_EN_4 | | INC_EN_3 | | INC_EN_2 | | INC_EN_1 | | INC_EN_0 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

LEGEND: R/W = Read/Write

**表 9-17. INT_EN_COMP1 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23-22 | INC_EN_11 | R/W | 0h | 0h = no interrupt generation for IN11<br>1h = interrupt generation on rising edge above THRES_COMP_IN8_IN11 for IN11<br>2h = interrupt generation on falling edge below THRES_COMP_IN8_IN11 for IN11<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN8_IN11 for IN11 |
| 21-20 | INC_EN_10 | R/W | 0h | 0h = no interrupt generation for IN10<br>1h = interrupt generation on rising edge above THRES_COMP_IN8_IN11 for IN10<br>2h = interrupt generation on falling edge below THRES_COMP_IN8_IN11 for IN10<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN8_IN11 for IN10 |
| 19-18 | INC_EN_9 | R/W | 0h | 0h = no interrupt generation for IN9<br>1h = interrupt generation on rising edge above THRES_COMP_IN8_IN11 for IN9<br>2h = interrupt generation on falling edge below THRES_COMP_IN8_IN11 for IN9<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN8_IN11 for IN9 |
| 17-16 | INC_EN_8 | R/W | 0h | 0h = no interrupt generation for IN8<br>1h = interrupt generation on rising edge above THRES_COMP_IN8_IN11 for IN8<br>2h = interrupt generation on falling edge below THRES_COMP_IN8_IN11 for IN8<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN8_IN11 for IN8 |
| 15-14 | INC_EN_7 | R/W | 0h | 0h = no interrupt generation for IN7<br>1h = interrupt generation on rising edge above THRES_COMP_IN4_IN7 for IN7<br>2h = interrupt generation on falling edge below THRES_COMP_IN4_IN7 for IN7<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN4_IN7 for IN7 |

**表 9-17. INT_EN_COMP1 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 13-12 | INC_EN_6 | R/W | 0h | 0h = no interrupt generation for IN6<br>1h = interrupt generation on rising edge above THRES_COMP_IN4_IN7 for IN6<br>2h = interrupt generation on falling edge below THRES_COMP_IN4_IN7 for IN6<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN4_IN7 for IN6 |
| 11-10 | INC_EN_5 | R/W | 0h | 0h = no interrupt generation for IN5<br>1h = interrupt generation on rising edge above THRES_COMP_IN4_IN7 for IN5<br>2h = interrupt generation on falling edge below THRES_COMP_IN4_IN7 for IN5<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN4_IN7 for IN5 |
| 9-8 | INC_EN_4 | R/W | 0h | 0h = no interrupt generation for IN4<br>1h = interrupt generation on rising edge above THRES_COMP_IN4_IN7 for IN4<br>2h = interrupt generation on falling edge below THRES_COMP_IN4_IN7 for IN4<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN4_IN7 for IN4 |
| 7-6 | INC_EN_3 | R/W | 0h | 0h = no interrupt generation for IN3<br>1h = interrupt generation on rising edge above THRES_COMP_IN0_IN3 for IN3<br>2h = interrupt generation on falling edge below THRES_COMP_IN0_IN3 for IN3<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN0_IN3 for IN3 |
| 5-4 | INC_EN_2 | R/W | 0h | 0h = no interrupt generation for IN2<br>1h = interrupt generation on rising edge above THRES_COMP_IN0_IN3 for IN2<br>2h = interrupt generation on falling edge below THRES_COMP_IN0_IN3 for IN2<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN0_IN3 for IN2 |
| 3-2 | INC_EN_1 | R/W | 0h | 0h = no interrupt generation for IN1<br>1h = interrupt generation on rising edge above THRES_COMP_IN0_IN3 for IN1<br>2h = interrupt generation on falling edge below THRES_COMP_IN0_IN3 for IN1<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN0_IN3 for IN1 |
| 1-0 | INC_EN_0 | R/W | 0h | 0h = no interrupt generation for IN0<br>1h = interrupt generation on rising edge above THRES_COMP_IN0_IN3 for IN0<br>2h = interrupt generation on falling edge below THRES_COMP_IN0_IN3 for IN0<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN0_IN3 for IN0 |

### 9.4.15 INT_EN_COMP2 Register (Offset = 23h) [reset = 0h]

INT_EN_COMP2 is shown in 図 9-17 and described in 表 9-18.

Return to Summary Table.

**図 9-17. INT_EN_COMP2 Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| INC_EN_23 | | INC_EN_22 | | INC_EN_21 | | INC_EN_20 | | INC_EN_19 | | INC_EN_18 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |
| 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| INC_EN_17 | | INC_EN_16 | | INC_EN_15 | | INC_EN_14 | | INC_EN_13 | | INC_EN_12 | |
| R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | | R/W-0h | |

LEGEND: R/W = Read/Write

**表 9-18. INT_EN_COMP2 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23-22 | INC_EN_23 | R/W | 0h | 0h = no interrupt generation for IN23<br>1h = interrupt generation on rising edge above THRES_COMP_IN20_IN23 for IN23<br>2h = interrupt generation on falling edge below THRES_COMP_IN20_IN23 for IN23<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN20_IN23 for IN23 |
| 21-20 | INC_EN_22 | R/W | 0h | 0h = no interrupt generation for IN22<br>1h = interrupt generation on rising edge above THRES_COMP_IN20_IN23 for IN22<br>2h = interrupt generation on falling edge below THRES_COMP_IN20_IN23 for IN22<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN20_IN23 for IN22 |
| 19-18 | INC_EN_21 | R/W | 0h | 0h = no interrupt generation for IN21<br>1h = interrupt generation on rising edge above THRES_COMP_IN20_IN23 for IN21<br>2h = interrupt generation on falling edge below THRES_COMP_IN20_IN23 for IN21<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN20_IN23 for IN21 |
| 17-16 | INC_EN_20 | R/W | 0h | 0h = no interrupt generation for IN20<br>1h = interrupt generation on rising edge above THRES_COMP_IN20_IN23 for IN20<br>2h = interrupt generation on falling edge below THRES_COMP_IN20_IN23 for IN20<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN20_IN23 for IN20 |
| 15-14 | INC_EN_19 | R/W | 0h | 0h = no interrupt generation for IN19<br>1h = interrupt generation on rising edge above THRES_COMP_IN16_IN19 for IN19<br>2h = interrupt generation on falling edge below THRES_COMP_IN16_IN19 for IN19<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN16_IN19 for IN19 |

**表 9-18. INT_EN_COMP2 Register Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 13-12 | INC_EN_18 | R/W | 0h | 0h = no interrupt generation for IN18<br>1h = interrupt generation on rising edge above THRES_COMP_IN16_IN19 for IN18<br>2h = interrupt generation on falling edge below THRES_COMP_IN16_IN19 for IN18<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN16_IN19 for IN18 |
| 11-10 | INC_EN_17 | R/W | 0h | 0h = no interrupt generation for IN17<br>1h = interrupt generation on rising edge above THRES_COMP_IN16_IN19 for IN17<br>2h = interrupt generation on falling edge below THRES_COMP_IN16_IN19 for IN17<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN16_IN19 for IN17 |
| 9-8 | INC_EN_16 | R/W | 0h | 0h = no interrupt generation for IN16<br>1h = interrupt generation on rising edge above THRES_COMP_IN16_IN19 for IN16<br>2h = interrupt generation on falling edge below THRES_COMP_IN16_IN19 for IN16<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN16_IN19 for IN16 |
| 7-6 | INC_EN_15 | R/W | 0h | 0h = no interrupt generation for IN15<br>1h = interrupt generation on rising edge above THRES_COMP_IN12_IN15 for IN15<br>2h = interrupt generation on falling edge below THRES_COMP_IN12_IN15 for IN15<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN12_IN15 for IN15 |
| 5-4 | INC_EN_14 | R/W | 0h | 0h = no interrupt generation for IN14<br>1h = interrupt generation on rising edge above THRES_COMP_IN12_IN15 for IN14<br>2h = interrupt generation on falling edge below THRES_COMP_IN12_IN15 for IN14<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN12_IN15 for IN14 |
| 3-2 | INC_EN_13 | R/W | 0h | 0h = no interrupt generation for IN13<br>1h = interrupt generation on rising edge above THRES_COMP_IN12_IN15 for IN13<br>2h = interrupt generation on falling edge below THRES_COMP_IN12_IN15 for IN13<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN12_IN15 for IN13 |
| 1-0 | INC_EN_12 | R/W | 0h | 0h = no interrupt generation for IN12<br>1h = interrupt generation on rising edge above THRES_COMP_IN12_IN15 for IN12<br>2h = interrupt generation on falling edge below THRES_COMP_IN12_IN15 for IN12<br>3h = interrupt generation on falling and rising edge of THRES_COMP_IN12_IN15 for IN12 |

### 9.4.16 INT_EN_CFG0 Register (Offset = 24h) [reset = 0h]

INT_EN_CFG0 is shown in 図 9-18 and described in 表 9-19.

Return to Summary Table.

**図 9-18. INT_EN_CFG0 Register**

| 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 |
|---|---|---|---|---|---|---|---|
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
| RESERVED | | | | | | | |
| R-0h | | | | | | | |
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CRC_CALC_EN | UV_EN | OV_EN | TW_EN | TSD_EN | SSC_EN | PRTY_FAIL_EN | SPI_FAIL_EN |
| R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h | R/W-0h |

LEGEND: R/W = Read/Write; R = Read only

**表 9-19. INT_EN_CFG0 Register Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 23-8 | RESERVED | R | 0h | Reserved |
| 7 | CRC_CALC_EN | R/W | 0h | 0h = $\overline{INT}$ pin assertion due to CRC calculation completion disabled.<br>1h = $\overline{INT}$ pin assertion due to CRC calculation completion enabled. |
| 6 | UV_EN | R/W | 0h | 0h = $\overline{INT}$ pin assertion due to UV event disabled.<br>1h = $\overline{INT}$ pin assertion due to UV event enabled. |
| 5 | OV_EN | R/W | 0h | 0h = $\overline{INT}$ pin assertion due to OV event disabled.<br>1h = $\overline{INT}$ pin assertion due to OV event enabled. |
| 4 | TW_EN | R/W | 0h | 0h = $\overline{INT}$ pin assertion due to TW event disabled.<br>1h = $\overline{INT}$ pin assertion due to TW event enabled. |
| 3 | TSD_EN | R/W | 0h | 0h = $\overline{INT}$ pin assertion due to TSD event disabled.<br>1h = $\overline{INT}$ pin assertion due to TSD event enabled. |
| 2 | SSC_EN | R/W | 0h | 0h = $\overline{INT}$ pin assertion due to SSC event disabled.<br>1h = $\overline{INT}$ pin assertion due to SSC event enabled. |
| 1 | PRTY_FAIL_EN | R/W | 0h | 0h = $\overline{INT}$ pin assertion due to parity fail event disabled.<br>1h = $\overline{INT}$ pin assertion due to parity fail event enabled. |
| 0 | SPI_FAIL_EN | R/W | 0h | 0h = $\overline{INT}$ pin assertion due to SPI fail event disabled.<br>1h = $\overline{INT}$ pin assertion due to SPI fail event enabled. |

# 10 Application and Implementation

**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The TIC10024-Q1 is an advanced 24-input Multiple Switch Detection Interface (MSDI) device designed to detect external mechanical switch status in a 12-V automotive system by acting as an interface between the switches and the low- voltage microcontroller. The device offers a number of unique features to replace systems implemented with discrete components, saving board space and reducing the bill of materials (BOM). The device can also be configured into low-power polling mode, which provides significant savings on system power consumption.

## 10.2 Digital Switch Detection in Automotive Body Control Module

The body control module (BCM) is an electronic control unit responsible for monitoring and controlling various electronic accessories in a vehicle body. Detection of various mechanical switches status in a vehicle is one important task handled by the BCM. Most switches inside the BCM are digital in nature, meaning they have either an ON or an OFF state. The TIC10024-Q1 can detect up to 24 digital switches. The following application diagram depicts how the TIC10024-Q1 is used in a BCM to detect an external digital switch and a detailed design example is shown in the following sections.

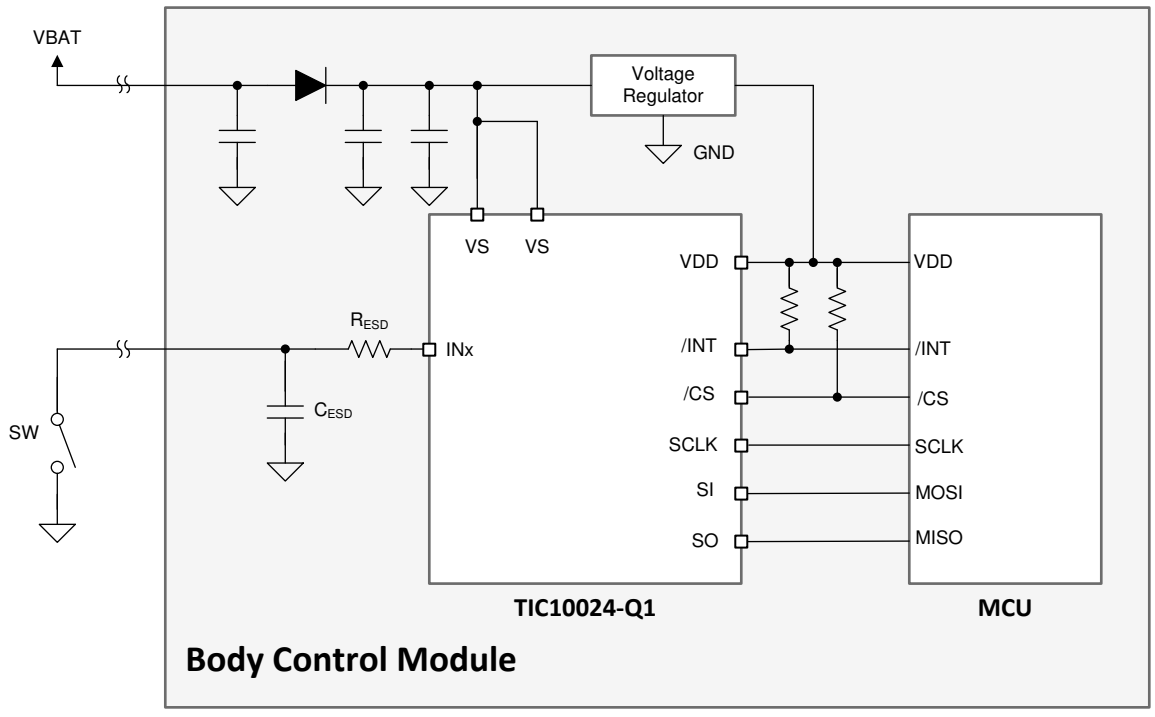





**図 10-1. Using TIC10024-Q1 to Monitor a Digital Switch in Body Control Module Application**

### 10.2.1 Design Requirements

**表 10-1. Example Digital Switch Specification**

| PARAMETER | SPECIFICATION | MIN | MAX |
|---|---|---|---|
| $V_{BAT}$ | 7 V ≤ $V_{BAT}$ ≤ 16 V | 7 V | 16 V |
| $V_{DIODE}$ (voltage drop across the reverse-blocking diode) | 0 V ≤ $V_{DIODE}$ ≤ 1 V | 0 V | 1 V |
| $R_{ESD}$ | 50 Ω ± 8% | 46 Ω | 54 Ω |
| $R_{SW}$ | 220 Ω Max when closed ± 8% | 0 Ω | 237.6 Ω |
| $R_{DIRT}$ | 5000 Ω Min | 5000 Ω | ∞ |
| Wetting current requirement | 10mA Typical | | |

An example of digital switch connected to ground shown in 図 10-1, with 表 10-1 summarizing its detailed requirements. The goal of this design is to utilize the TIC10024-Q1's integrated comparator to detect and differentiate between the 2 switch states:

1. State 1: SW open
2. State 2: SW closed

To mimic real automotive systems, the battery is assumed to be fluctuating between 7 V and 16 V. Taking into account the voltage drop across the reverse-blocking diode, the $V_S$ supply voltage to the TIC10024-Q1 device can fluctuate between 6 V and 16 V. $R_{DIRT}$ is introduced to model the small leakage flowing across the switch in open state. When the switch changes position and the switch state changes from one to another, the TIC10024-Q1 is required to correctly detect the state transition and issue an interrupt to alert the microcontroller. The switch information needs to be stored in the status registers for the microcontroller to retrieve.

### 10.2.2 Detailed Design Procedure

**表 10-2. Detailed Design Procedure**

| | STEP 1 | | STEP 2 | |
|---|---|---|---|---|
| | Equivalent Resistance Value (Ω) | | $V_{INX}$ (V) | |
| | MIN | MAX | MIN | MAX |
| State 1: SW open | 5000 | ∞ | >10 | - |
| State 2: SW closed | 0 | 291.6 | 0 | 3.32 |

Use the following procedures to calculate thresholds to program to the TIC10024-Q1 for proper switch detection:

1. Calculate the equivalent resistance values at the 2 switch states, taking into account $R_{DIRT}$ and the 8% resistance variation.
2. Estimate the voltage established when wetting current flows through the switch by utilizing the relationship $V_{INX} = R_{SW\_EQU} \times I_{WETT\_ACT}$, where $R_{SW\_EQU}$ is the equivalent switch resistance value and $I_{WETT\_ACT}$ is the actual wetting current flowing through the switch. The 10 mA wetting current setting is selected in this design as required by the specification. The wetting current variation, however, can occur depending on manufacturing process variation and operating temperature, and needs to be taken into account. Referring to the electrical table of the TIC10024-Q1 and assuming enough headroom for the current source (CSO) to operate, the 10mA wetting current setting produces current ranging between 8.4 mA and 11.4 mA (for 6 V ≤ $V_S$ ≤ 35 V condition). The voltage established on the TIC10024-Q1 input pin ($V_{INX}$) can be calculated accordingly.
3. After the $V_{INX}$ voltage is calculated for the 2 switch states, the proper threshold value needs to be chosen between minimum $V_{INX}$ voltage of state 1 (>10 V) and maximum $V_{INX}$ voltage of state 2 (3.32 V). The TIC10024-Q1 has 4 thresholds that can be configured for the comparator: 2 V, 2.7 V, 3 V, and 4 V. As a result, the proper threshold to be used in this design example is 4 V.
4. To properly program the device, follow the below recommend procedure:
   - Enable channel IN0 by setting IN_EN_0 bit to 1 in the IN_EN register
   - Program the wetting current to source by setting CS_IN0 bit to 0 in the CS SELECT register

- Program the wetting current to 10 mA by configuring WC_IN0_IN1 bits to 100 in the WC_CFG0 register
- Disable wetting current auto-scaling by setting AUTO_SCALE_DIS_CSO bit in WC_CFG1 register to 1
- Program the comparator threshold to 4 V by setting the THRES_COMP_IN0_IN3 bits to 11 in the THRES_COMP register
- Program interrupt generation to both rising and falling transitions by setting the INC_EN_0 bits to 11 in the INT_EN_COMP1 register
- Enable interrupt generation from switch state change by setting the SSC bit to 1 in the INT_EN_CFG0 register
- Program the CONFIG register: Keep the device in continuous mode by setting the POLL_EN bit to 0. Start device operation by setting the TRIGGER bit to 1.
- Read the INT_STAT register to clear the baseline SSC interrupt once the interrupt is observed.
- Toggle the external switch open and monitor the $\overline{INT}$ pin. Read the INT_STAT register and IN_STATE_COMP register to make sure the correct switch status is reported.

### 10.2.3 Application Curves

図 10-2 is the scope shot showing the switch getting toggled from close to open at time a). Before toggling, the voltage at $V_{IN0}$ stays low at roughly 2.7 V. Once the switch opens, the voltage at $V_{IN0}$ gets pulled high to the $V_S$ voltage. The $\overline{INT}$ pin is asserted shortly after the switch toggles at time b) to notify the microcontroller a switch state change event has occurred.

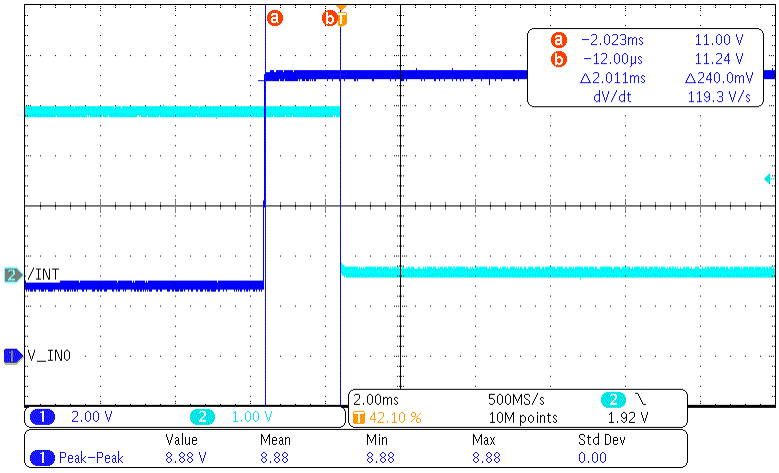



**図 10-2. Measured Waveform Showing $V_{IN0}$ Pin and $\overline{INT}$ Pin Voltages**

## 10.3 Systems Examples

### 10.3.1 Using TIC10024-Q1 in a 12 V Automotive System

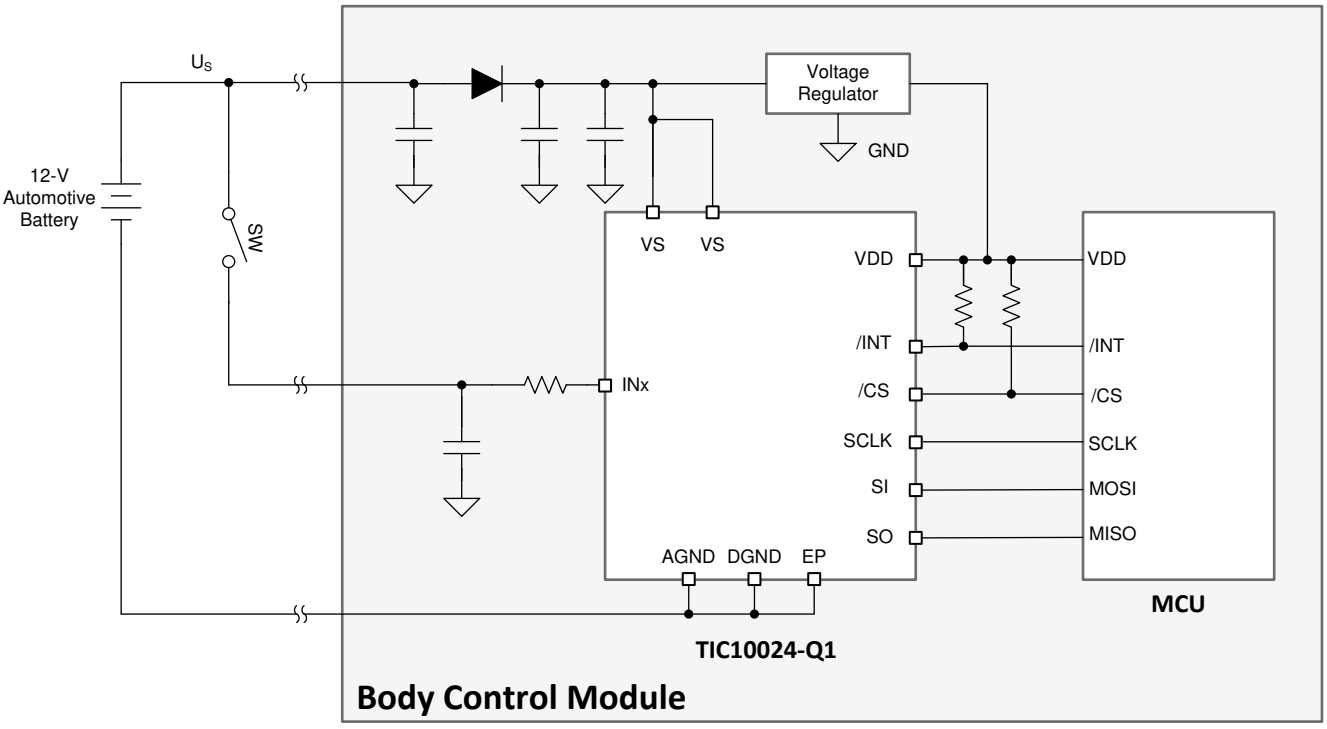





**図 10-3. Typical System Diagram of Battery Connections for TIC10024-Q1**

The TIC10024-Q1 is designed to operate with a 12 V automotive system. 図 10-3 depicts a typical system diagram to show how the device is connected to the battery. Please remember to be careful when connecting the battery directly to the device on the $V_S$ supply pin (through a reverse-blocking diode) or the input ($IN_X$) pins since an automotive battery can be subjected to various transient and over-voltage events. Manufacturers have independently created standards and test procedures in an effort to prevent sensitive electronics from failing due to these events. Recently, combined efforts are made with ISO to develop the ISO 16750-2 standard (Road vehicles -- Environmental conditions and testing for electrical and electronic equipment -- Part 2: Electrical loads), which describe the possible transients that could occur to an automotive battery and specify test methods to simulate them.

It shall be noted that the TIC10024-Q1 is designed and tested according to the ISO 16750-2 standard. A few voltage stress tests and their test conditions are listed below. Exposing the device to more severe transient events than described by the standard can potentially causes performance degradation and long-term damage to the device.

- Direct current supply voltage: $V_{BAT, min}$ = 6 V; $V_{BAT, max}$= 16 V
- To emulate a jump start event, voltage profile described in 図 10-4 is used.

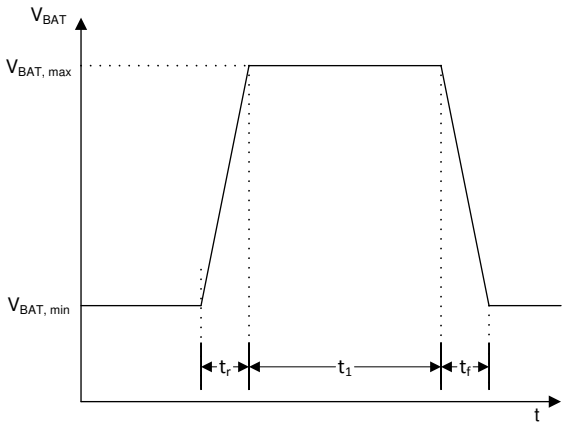



**図 10-4. Voltage Profile to Test a Jump Start Event**

**表 10-3. Voltage Profile Parameters to Test a Jump Start Event**

| Parameter | Value |
|---|---|
| $V_{BAT, min}$ | 10.8 V |
| $V_{BAT, max}$ | 24 V |
| $t_r$ | < 10 ms |
| $t_1$ | 60 s ± 6 s |
| $t_f$ | < 10 ms |
| Number of cycles | 1 |

To emulate a load dump event for an alternator with centralized load dump suppression, voltage profile described in 図 10-5 is used. $U_A$ and $U_S$* are applied directly to $V_{BAT}$.

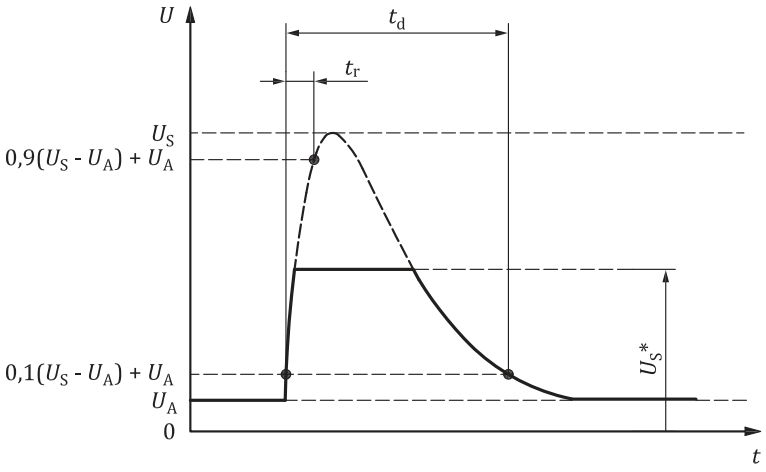



**図 10-5. Voltage Profile to Test a Load Dump Event With Centralized Load Dump Suppression**

**表 10-4. Voltage Profile to Test a Load Dump Event With Centralized Load Dump Suppression**

| Parameter | Value |
|---|---|
| $U_A$ | 13.5 V |
| $U_S$ | 79 V ≤ $U_S$ ≤ 101 |
| $U_S$* | 35 V |
| $t_d$ | 40 ms ≤ $t_d$ ≤ 400 ms |
| $t_r$ | < 10 ms |
| Number of cycles | 5 pulses at intervals of 1 min |

To emulate a cranking event, voltage profile describe in 図 10-6 is used. $U_S$, $U_{S6}$, and $U_A$ are applied directly to $V_{BAT}$.

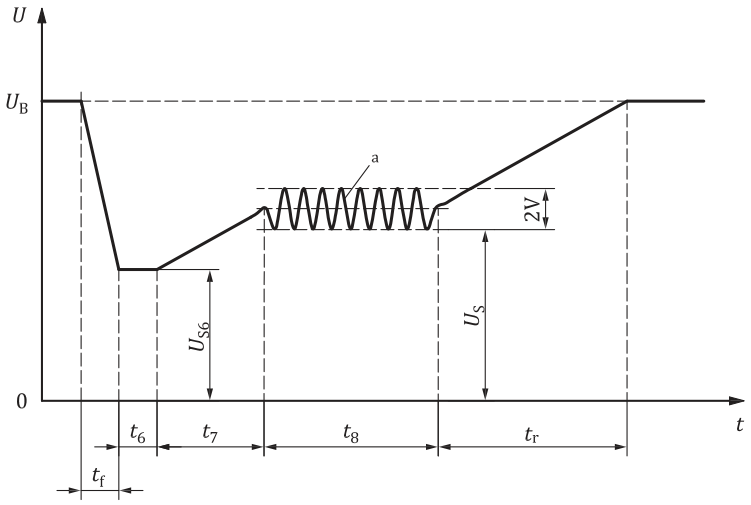



**図 10-6. Voltage Profile to Test a Cranking Event**

**表 10-5. Voltage Profile Used to Test a Cranking Event**

| Parameter | Value - Level I | Value - Level II | Value - Level IV |
|---|---|---|---|
| $U_{S6}$ | 8 V | 4.5 V | 6 V |
| $U_S$ | 9.5 V | 6.5 V | 6.5 V |
| $U_B$ | 14 V ± 0.2 V | 14 V ± 0.2 V | 14 V ± 0.2 V |
| $t_f$ | 5 ms ± 0.5 ms | 5 ms ± 0.5 ms | 5 ms ± 0.5 ms |
| $t_6$ | 15 ms ± 1.5 ms | 15 ms ± 1.5 ms | 15 ms ± 1.5 ms |
| $t_7$ | 50 ms ± 5 ms | 50 ms ± 5 ms | 50 ms ± 5 ms |
| $t_8$ | 1000 ms ± 100 ms | 10000 ms ± 1000 ms | 10000 ms ± 1000 ms |
| $t_r$ | 40 ms ± 4 ms | 100 ms ± 10 ms | 100 ms ± 10 ms |

## 11 Power Supply Recommendations

There are two supply input pins for the TIC10024-Q1: $V_S$ and $V_{DD}$. $V_S$ is the main power supply for the entire chip and is essential for all critical functions of the device. The $V_S$ supply is designed to be connected to a 12-V automotive battery (through a reverse blocking diode) with nominal operating voltage no greater than 16V. The $V_{DD}$ supply is used to determine the logic level on the SPI communication interface, source the current for the SO driver, and sets the pull-up voltage for the /CS pin. It can also be used as a possible external pull-up supply for the /INT pin as an alternative to the $V_S$ supply and it shall be connected to a 3 V to 5.5 V logic supply. Removing $V_{DD}$ from the device disables SPI communications, but does not impact normal operation of the device.

To improve stability of the supply inputs, some decoupling capacitors are recommended on the PCB. 図 11-1 shows an example on the on-board power supply decoupling scheme. The battery voltage ($V_{BAT}$) is decoupled on the Electronic Control Unit (ECU) board using a large decoupling capacitor ($C_{BUFF}$). The diode is installed to prevent damage to the internal system under reversed battery condition. $C_{VS}$ shall be installed close to the TIC10024-Q1 for best decoupling performance. The voltage regulator provides a regulated voltage for the digital portion of the device and for the local microcontroller and its output is decoupled with $C_{DECOUPLE}$. 表 11-1 lists recommended values for each individual decoupling capacitor shown in the system diagram.

**表 11-1. Decoupling Capacitor Recommendations**

| CRC RULE | VALUE |
|---|---|
| $C_{BUFF}$ | 100 µF, 50 V rated, ±20% |
| $C_{VBAT}$ | 100 nF, 50V rated, ±10%; X7R |
| $C_{VS}$ | 100 nF, 50 V rated |
| $C_{DECOUPLE}$ | 100 nF~1 µF |

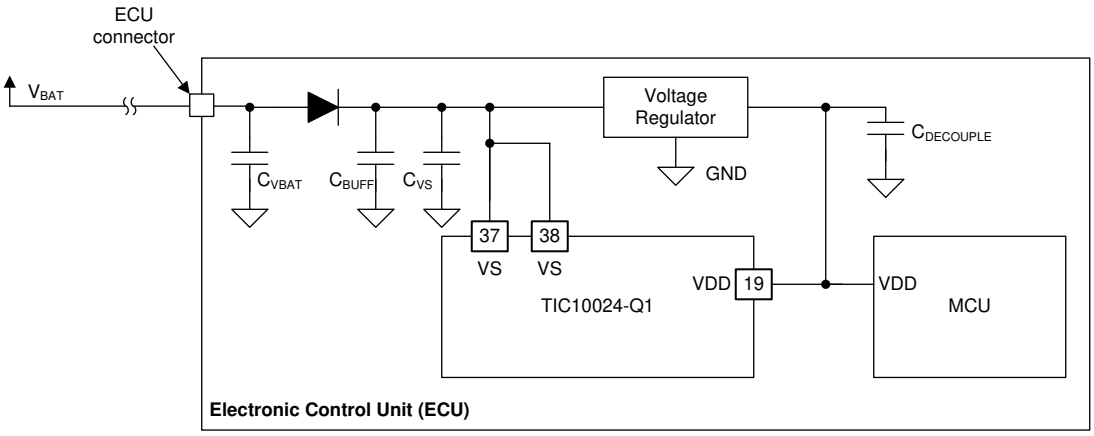





**図 11-1. Recommended Power Supply Decoupling**

# 12 Layout

## 12.1 Layout Guidelines

1. 図 12-1 illustrates an example of a PCB layout with the TIC10024-Q1. Some key considerations are:
2. Decouple the $V_S$ and $V_{DD}$ pins with capacitor using recommended values from section *Power Supply Recommendations* and place them as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the $V_S$ and $V_{DD}$ supplies.
3. Keep the input lines as short as possible.
4. Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
5. Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.
6. To achieve good thermal performance, the exposed thermal pad underneath the device must be soldered to the board and flooded with vias to ground planes. For simple double-sided PCBs where there are no internal layers, the surface layers can be used to remove heat. For multilayer PCBs, internal ground planes can be used for heat removal.
7. Minimize the inductive parasitic between the INx input capacitors and the thermal pad ground return.

## 12.2 Layout Example

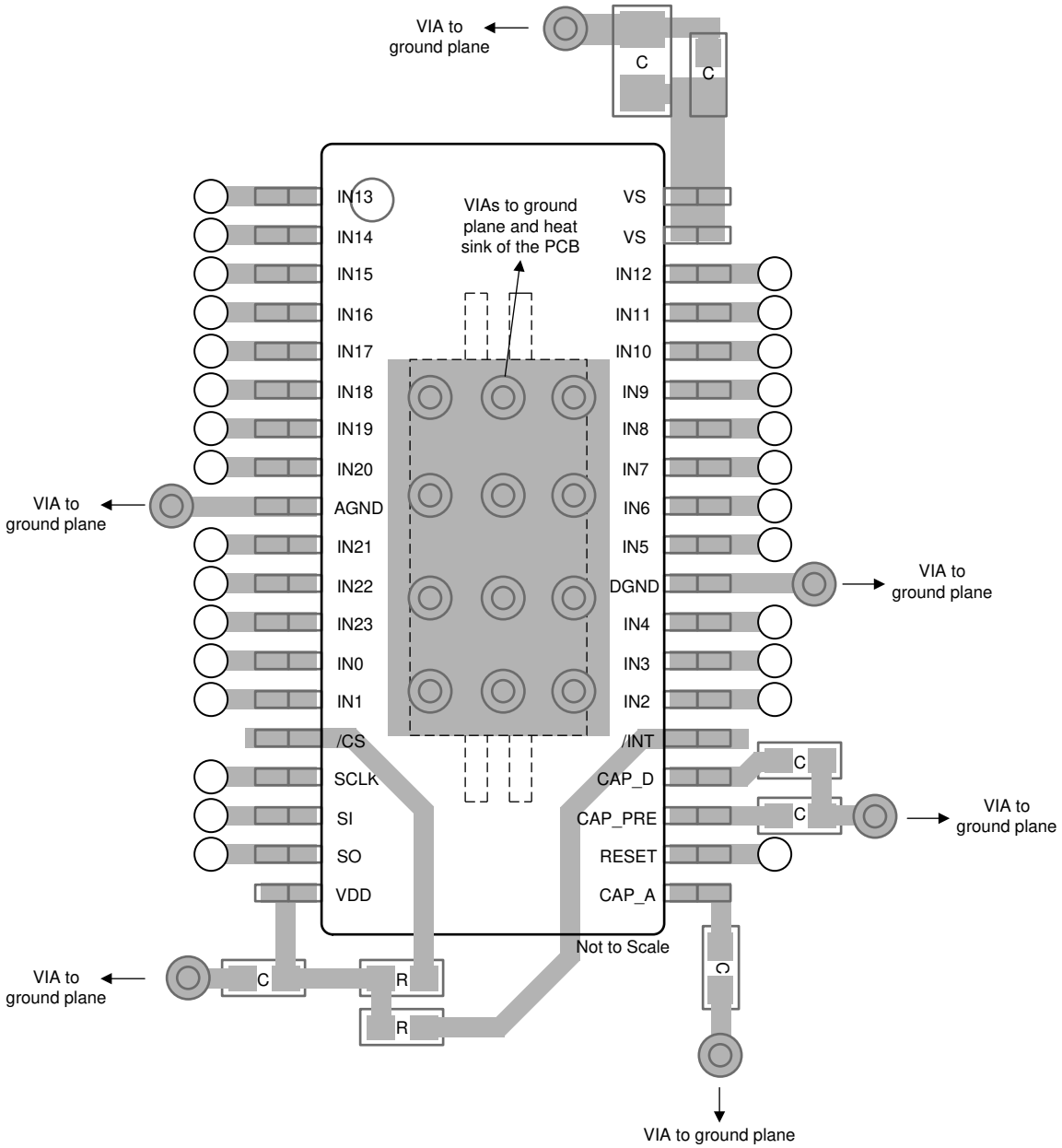



**図 12-1. Example Layout**

# 13 Device and Documentation Support

## 13.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 13.2 Community Resources

## 13.3 Trademarks

すべての商標は、それぞれの所有者に帰属します。

# 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| TIC10024QDCPRQ1 | Active | Production | HTSSOP (DCP) \| 38 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TIC10024Q |
| TIC10024QDCPRQ1.A | Active | Production | HTSSOP (DCP) \| 38 | 2000 \| LARGE T&R | Yes | NIPDAU | Level-3-260C-168 HR | -40 to 125 | TIC10024Q |

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

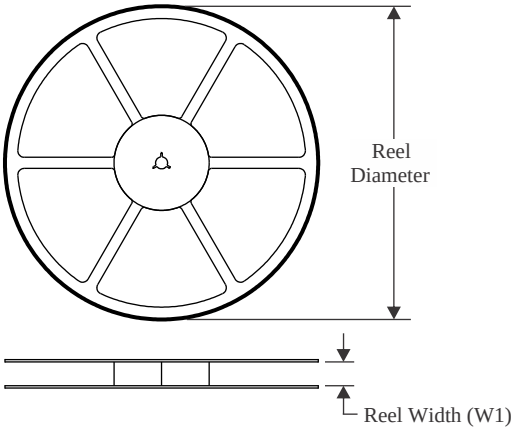
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

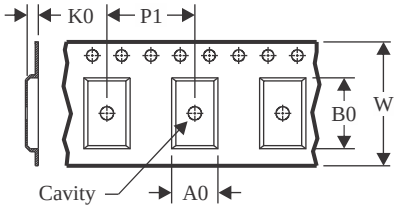
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

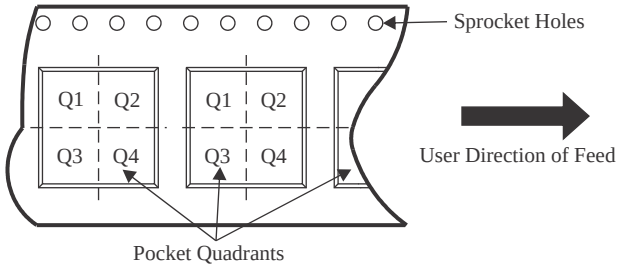



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

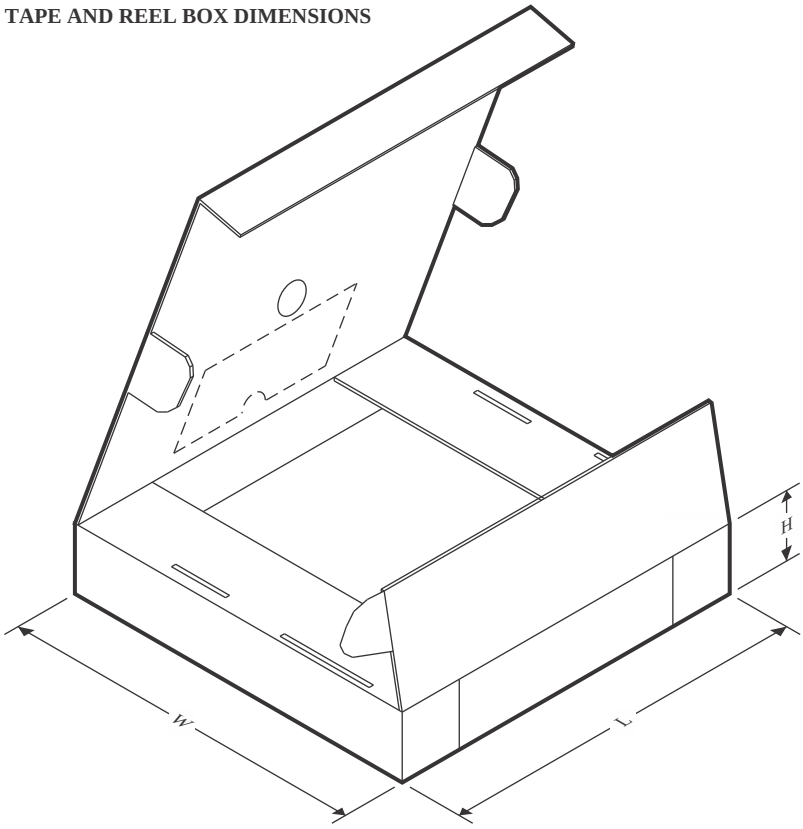
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| TIC10024QDCPRQ1 | HTSSOP | DCP | 38 | 2000 | 330.0 | 16.4 | 6.9 | 10.2 | 1.8 | 12.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| TIC10024QDCPRQ1 | HTSSOP | DCP | 38 | 2000 | 350.0 | 350.0 | 43.0 |

# GENERIC PACKAGE VIEW

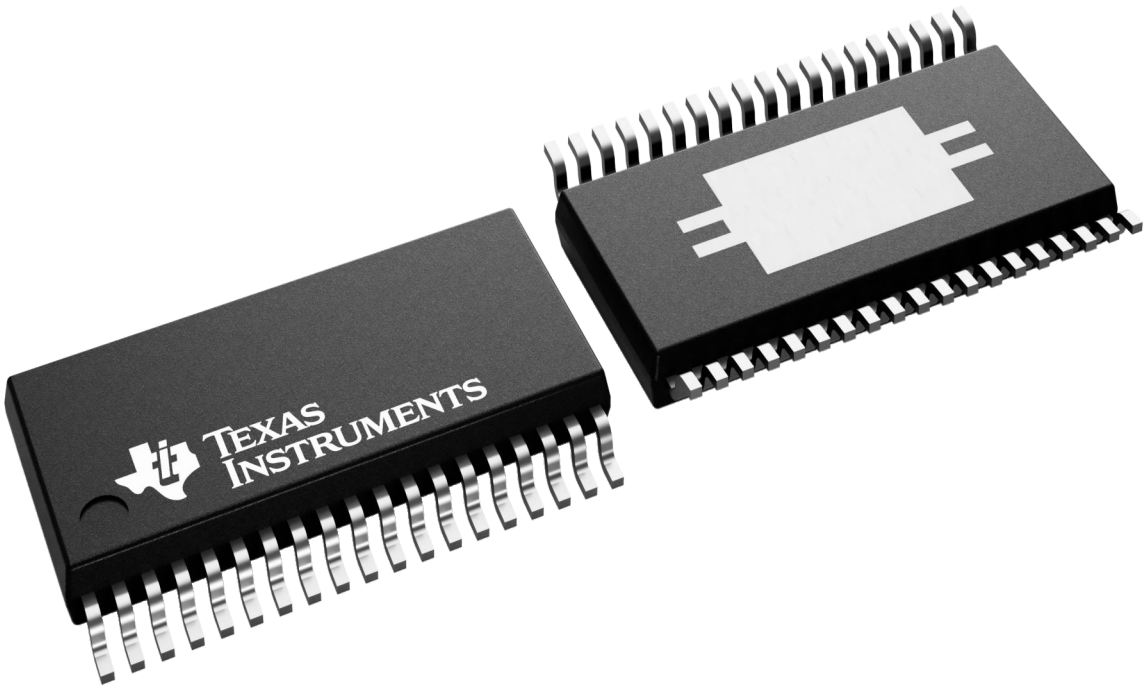
## DCP 38

## PowerPAD TSSOP - 1.2 mm max height

**4.4 x 9.7, 0.5 mm pitch**

SMALL OUTLINE PACKAGE

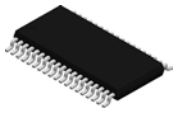
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4224560/B

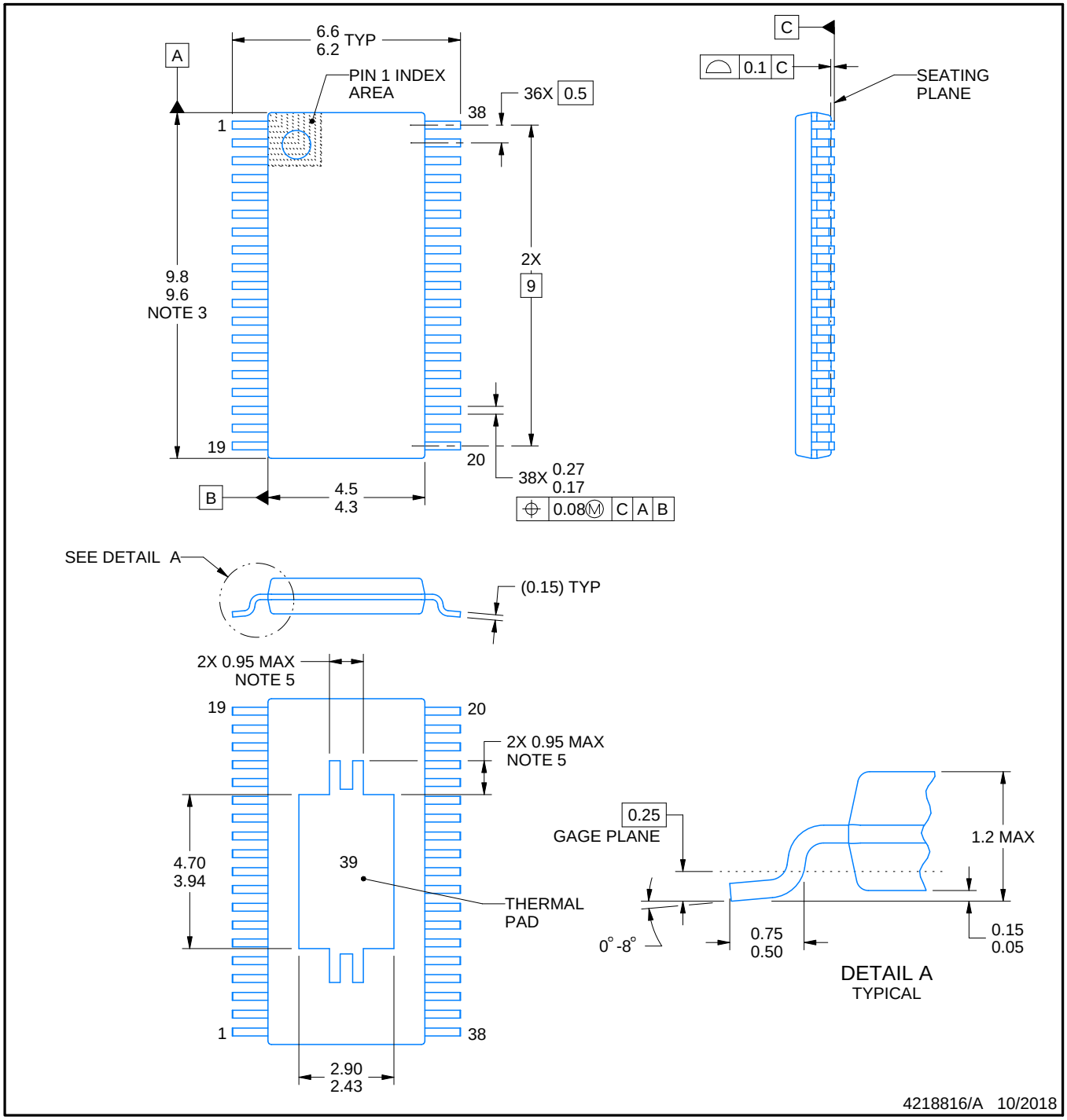
# PACKAGE OUTLINE

## DCP0038A



## PowerPAD™ TSSOP - 1.2 mm max height

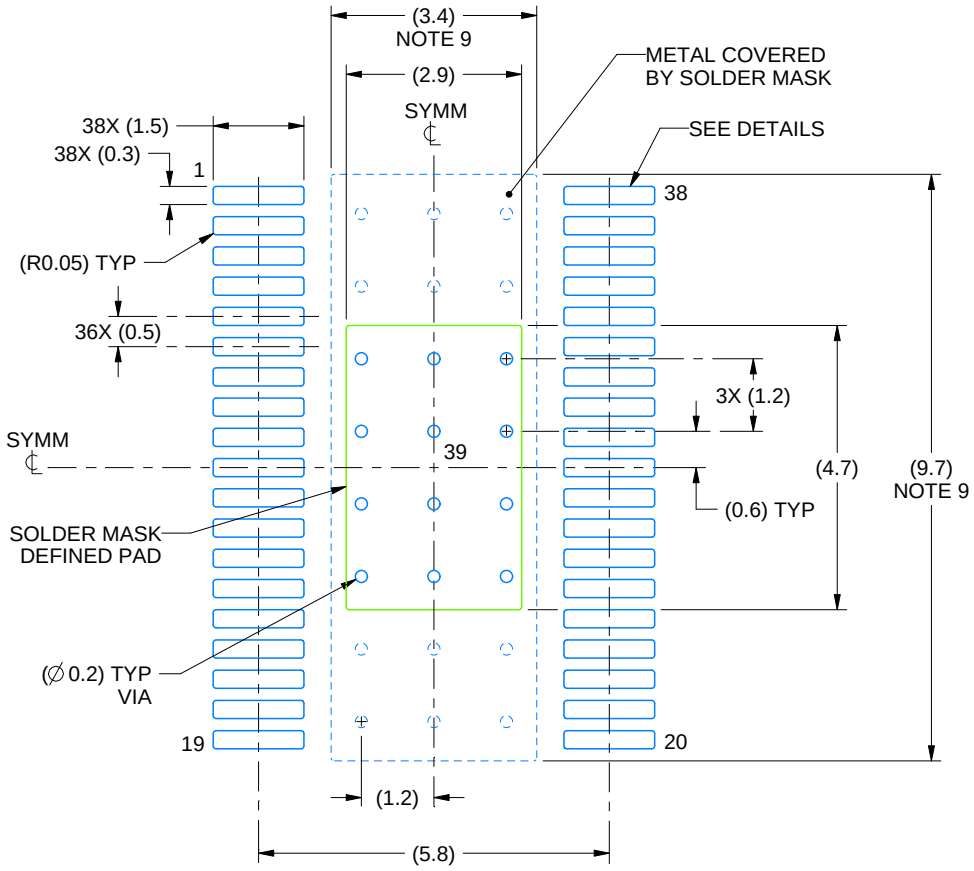
SMALL OUTLINE PACKAGE



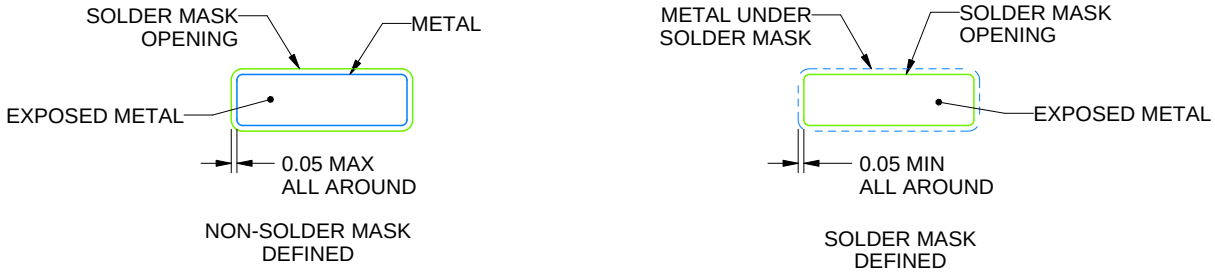

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X




SOLDER MASK DETAILS

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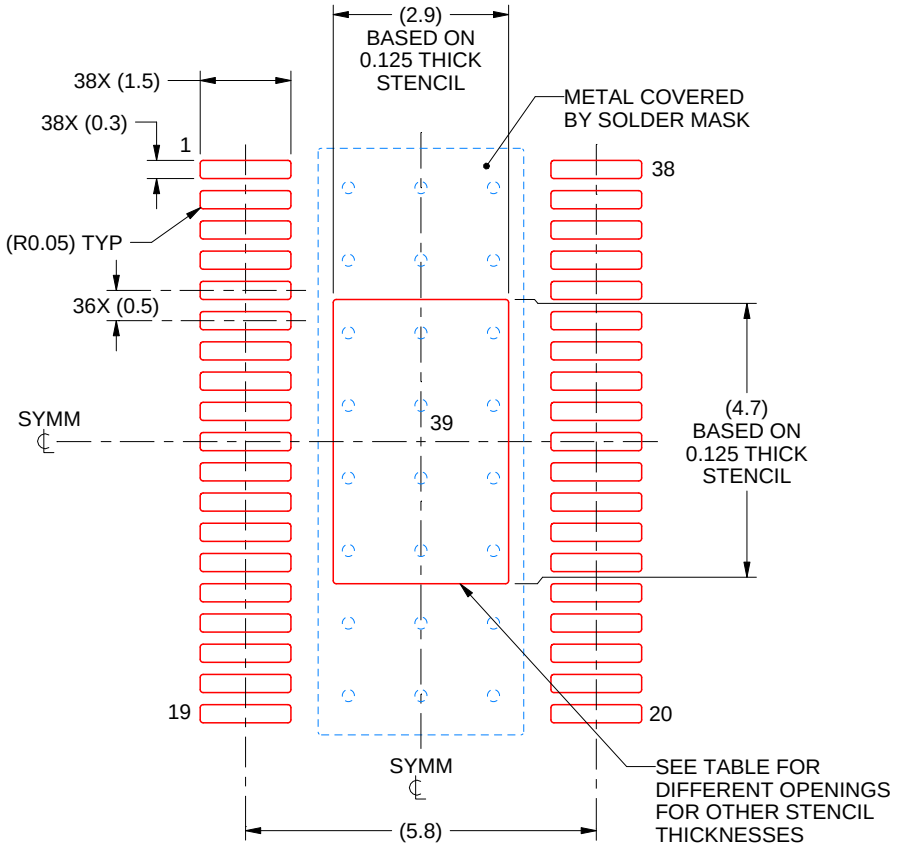
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|---|---|
| 0.1 | 3.24 X 5.25 |
| 0.125 | 2.90 X 4.70 (SHOWN) |
| 0.15 | 2.65 X 4.29 |
| 0.175 | 2.45 X 3.97 |

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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