TDA4VM プロセッサ

1 特長

プロセッサ コア:

- C7x 浮動小数点、ベクタ DSP、最高 1.0GHz、80GFLOPS、256GOPS
- ディープ ラーニング用マトリクス乗算アクセラレータ (MMA)、1.0GHz で最大 8TOPS (8b)
- 画像信号プロセッサ (ISP) 搭載ビジョン処理アクセラレータ (VPAC) と複数のビジョン支援アクセラレータ
- 深度およびモーション処理アクセラレータ (DMPAC)
- デュアル 64 ビット Arm® Cortex®-A72 マイクロプロセッサ サブシステム、最大 2.0GHz
  - デュアル コア Cortex®-A72 クラスタごとに 1MB の共有 L2 キャッシュ
  - Cortex®-A72 コアごとに 32KB L1 D キャッシュと 48KB L1 I キャッシュ
- 6 つの Arm® Cortex®-R5F MCU、最大 1.0GHz
  - 16K I キャッシュ、16K D キャッシュ、64K L2 TCM
  - 分離された MCU サブシステムに 2 つの Arm® Cortex®-R5F MCU
  - 汎用コンピューティング パーティションに 4 つの Arm® Cortex®-R5F MCU
- 2 つの C66x 浮動小数点 DSP、最高 1.35GHz、40GFLOPS、160GOPS
- 3D GPU PowerVR® Rogue 8XE GE8430、最高 750MHz、96GFLOPS、6Gpix/sec
- ほぼ最大限の処理権限をサポートするカスタム設計された相互接続構造

メモリ サブシステム:

- 最大 8MB のオンチップ L3 RAM、ECC およびコヒーレンシ機能付き
  - ECC エラー保護
  - 共有コヒーレント キャッシュ
  - 内部 DMA エンジンをサポート
- ECC 付きの外部メモリ インターフェイス (EMIF) モジュール
  - LPDDR4 メモリ タイプをサポート
  - 最大 4266MT/s の速度をサポート
  - インライン ECC 付きで の 32 ビット データ バス
- 汎用メモリ コントローラ (GPMC)
- メイン ドメインの 512KB のオンチップ SRAM、ECC 保護付き

機能安全:

- 機能安全準拠製品向け (一部の部品番号でのみ対応)
  - 機能安全アプリケーション向けに開発
  - ASIL-D/SIL-3 までを対象とした ISO 26262/IEC 61508 機能安全システム設計を支援するための資料を提供予定
  - ASIL-D/SC-3 までの決定論的能力に対応予定
  - ハードウェア整合性、MCU ドメイン向け ASIL-D/SIL-3 までを対象
  - ハードウェア整合性、MAIN ドメイン向け ASIL-B/SIL-2 までを対象
  - 安全関連認証
    - TÜV SÜD による ISO 26262 認証を計画中 (ASIL-D まで)
    - TÜV SÜD による IEC 61508 認証を計画中 (SIL-3 まで)
- 部品番号の末尾が Q1 のバリアントについては AEC-Q100 認定済み

デバイスのセキュリティ (一部の部品番号のみ):

- セキュアなランタイム サポートによるセキュア ブート
- お客様がプログラム可能なルート キー (RSA-4K または ECC-512 まで)
- 組み込みハードウェア セキュリティ モジュール
- 暗号化ハードウェア アクセラレータ – ECC 付き PKA、AES、SHA、RNG、DES、3DES

高速シリアル インターフェイス:

- 最大 8 つの外部ポートをサポートする統合型イーサネット スイッチ
  - すべてのポートが 2.5Gb SGMII をサポート
  - すべてのポートが 1Gb SGMII/RGMII をサポート
  - すべてのポートが 100Mb RMII をサポート
  - 任意の 2 つのポートが QSGMII をサポート (1 つの QSGMII ごとに 4 つの内部ポートを使用)
- 最大 4 つの PCI-Express® (PCIe) Gen3 コントローラ
  - コントローラごとに最大 2 つのレーン
  - Gen1 (2.5GT/s)、Gen2 (5.0GT/s)、Gen3 (8.0GT/s) で動作 (オート ネゴシエーション付き)
- 2 つの USB 3.0 デュアルロール デバイス (DRD) サブシステム
  - 2 つの Enhanced SuperSpeed Gen1 ポート
  - 各ポートは Type-C スイッチングをサポート
  - 各ポートを個別に USB ホスト、USB ペリフェラル、USB DRD として構成可能

車載インターフェイス:

- CAN-FD をフルサポートする 16 個のモジュラー コントローラ エリア ネットワーク (MCAN) モジュール
- 2 つの CSI2.0 4L RX と 1 つの CSI2.0 4L TX
  - レーンごとに 2.5Gbps の RX スループット (合計 20Gbps)

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

ディスプレイ サブシステム:

- 1 つの eDP/DP インターフェイス (マルチ ディスプレイ サポート (MST) 付き)
  - HDCP1.4/HDCP2.2 高帯域幅デジタル コンテンツ保護
- 1 つの DSI TX (最大 2.5K)
- 最大 2 つの DPI

オーディオ インターフェイス:

- 12 個のマルチチャネル オーディオ シリアル ポート (MCASP) モジュール

ビデオ アクセラレーション:

- Ultra-HD ビデオ、1 つ (3840 × 2160p、60fps) または 2 つ (3840 × 2160p、30fps) の H.264/H.265 デコード
- Full-HD ビデオ、4 つ (1920 × 1080p、60fps) または 8 つ (1920 × 1080p、30fps) の H.264/H.265 デコード
- Full-HD ビデオ、1 つ (1920 × 1080p、60fps) または最大 3 つ (1920 × 1080p、30fps) の H.264 エンコード

フラッシュ メモリ インターフェイス:

- 組み込み MultiMediaCard インターフェイス (eMMC™ 5.1)
- 2 つのレーンを持つユニバーサル フラッシュ ストレージ (UFS 2.1) インターフェイス
- 2 つの Secure Digital® 3.0/Secure Digital Input Output 3.0 インターフェイス (SD3.0/SDIO3.0)
- 2 つの同時フラッシュ インターフェイスを以下のように構成
  - 1 つの OSPI と 1 つの QSPI フラッシュ インターフェイス
  - または、1 つの HyperBus™ と 1 つの QSPI フラッシュ インターフェイス

システム オン チップ (SoC) アーキテクチャ:

- 16nm FinFET テクノロジ
- 24 mm × 24 mm、0.8mm ピッチ、827 ピンの FCBGA (ALF)、IPC クラス 3 PCB 配線に対応

TPS6594-Q1 コンパニオン パワー マネージメント IC (PMIC):

- ASIL-D までの機能安全対応
- 柔軟なマッピングにより各種の使用事例をサポート

2 アプリケーション

- 先進のサラウンド・ビューおよび駐車支援システム
- カメラ、レーダー、LIDAR センサを含む自律的センサ・フュージョン / 認識システム
- 単一センサおよびマルチセンサのフロント・カメラ・システム
- 次世代電子ミラー・システム
- 安全機能付きの産業用モバイル・ロボット (AGV/AMR)
- マシン・ビジョン
- スマート・リテール
- スマート・ショッピング・カート
- 建設、農業
- エッジ AI ボックス
- シングル・ボード・コンピュータ
- オフハイウェイ車両向け制御機能
- AI を搭載した産業用 PC

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3 概要

TDA4VM プロセッサ ファミリは、ADAS および自動運転車 (AV) アプリケーションを対象としており、ADAS プロセッサ市場においてテキサス・インスツルメンツがリーダーとして 10 年以上蓄積した膨大な市場知識の上に構築されています。機能安全準拠の対象アーキテクチャにおいて、高性能コンピューティング、ディープ ラーニング エンジン、信号処理および画像処理専用のアクセラレータの独自の組み合わせにより、TDA4VM デバイスは以下のさまざまな産業用アプリケーションに最適です。ロボティクス、マシン ビジョン、レーダーなど。TDA4VM は、高度なシステム統合によって、従来型とディープ ラーニングの両方のアルゴリズムを業界最高の電力 / 性能比で高精度計算し、集中 ECU またはスタンドアロン センサの複数センサ方式をサポートする先進車載用プラットフォームの拡張とコスト低減を実現できます。主要なコアとして、スカラーおよびベクター コアを持つ次世代 DSP、ディープ ラーニング専用および従来型アルゴリズム用アクセラレータ、汎用計算用の最新の Arm および GPU プロセッサ、統合型次世代イメージング サブシステム (ISP)、ビデオ コーデック、イーサネット ハブ、分離された MCU アイランドが含まれています。これらはすべて、車載グレードの安全性とセキュリティ ハードウェア アクセラレータにより保護されています。

主要な高性能コアの概要

「C7x」次世代 DSP は、テキサス・インスツルメンツの業界最先端の DSP と EVE コアを 1 つの高性能コアに統合し、浮動小数点ベクトル計算機能を追加することで、ソフトウェアのプログラミングを簡単にしながら従来のコードとの後方互換性を確保しています。新しい「MMA」ディープ ラーニング アクセラレータは、一般的な車載用の最も厳しい接合部温度である 125℃で動作する場合でも、業界最小の電力エンベロープ内で最大 8TOPS の性能を達成できます。専用 ADAS/AV ハードウェア アクセラレータは、システム性能に影響を及ぼさずに、ビジョン前処理と測距およびモーション処理を実行します。

汎用コンピューティング コアと統合の概要

Arm® Cortex®-A72 の独立デュアル コア クラスタ構成を使うと、ソフトウェア ハイパーバイザの必要性を最小限に抑えながらマルチ OS アプリケーションを簡単に実現できます。最大 6 つの Arm® Cortex®-R5F サブシステムが低レベルのタイム クリティカル処理タスクを実行し、Arm® Cortex®-A72 に負荷がかからないようにしてアプリケーションの実行に備えさせます。内蔵の「8XE GE8430」GPU は最高 100GFLOPS の性能を備えており、拡張表示アプリケーションの動的 3D レンダリングを可能にします。既存の世界最先端の ISP に基づいて構築された テキサス・インスツルメンツの第 7 世代 ISP は、より広範なセンサ スイートを処理する柔軟性、より深いビット深度のサポート、分析アプリケーションを対象とした機能を備えています。内蔵セキュリティ機能が現代の攻撃からデータを保護する一方で、内蔵の診断および安全機能は ASIL-D/SIL-3 レベルまでの動作をサポートしています。大きなデータ帯域幅を要求するシステムに対応するため、PCIe ハブとギガビット イーサネット スイッチが内蔵されており、多くのセンサ入力に必要なスループットをサポートするための CSI-2 ポートも内蔵されています。さらに高度な統合のため、TDA4VM ファミリには MCU アイランドも内蔵されているため、外部のシステム マイクロプロセッサは不要です。

パッケージ情報

部品番号 (1)	パッケージ	パッケージ サイズ(2)
TDA4VM…ALF	ALF (FCBGA、827)	24.0mm × 24.0mm
XJ721E…ALF	ALF (FCBGA、827)	24.0mm × 24.0mm

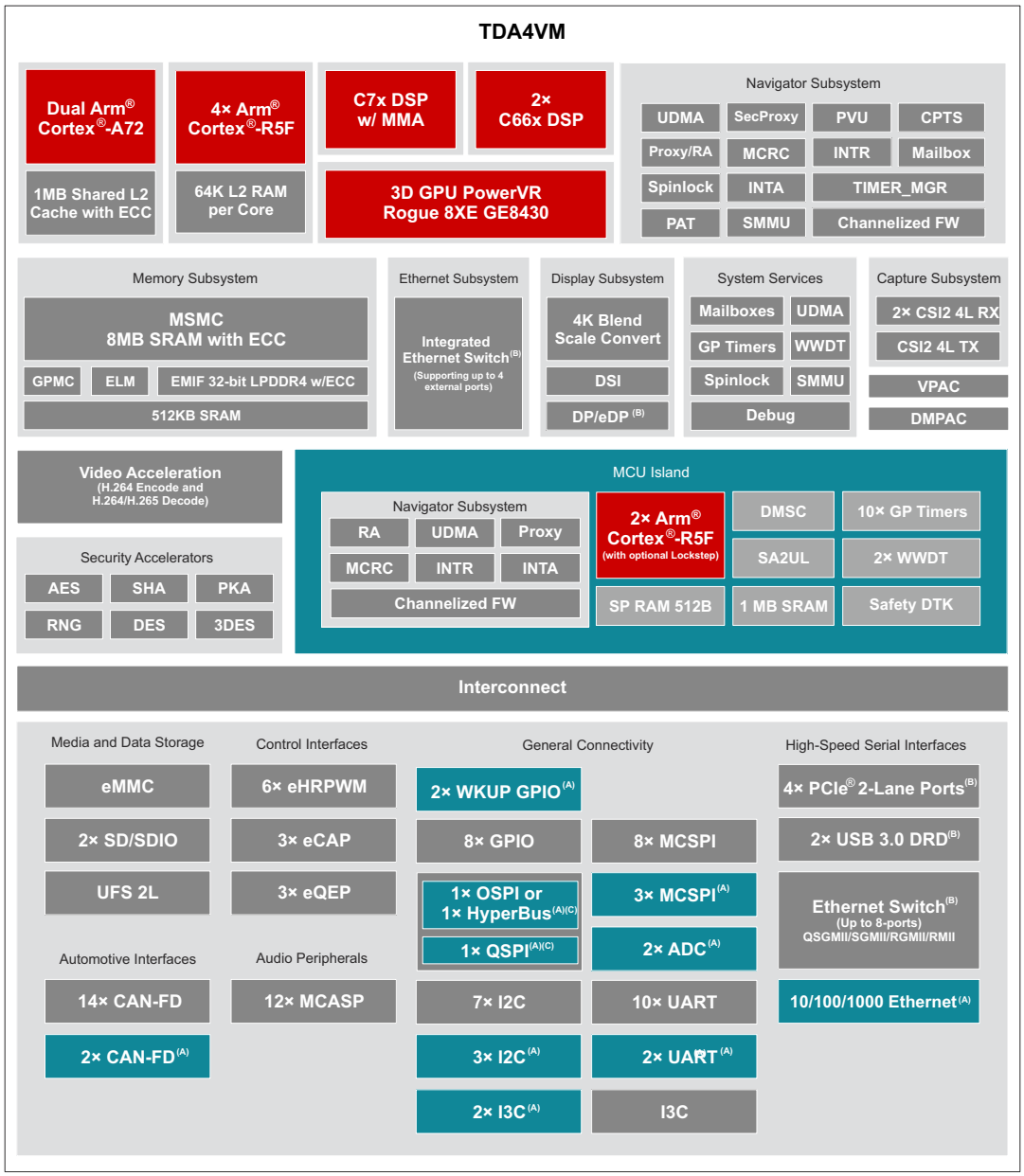
(1) 詳細については、「メカニカル、パッケージ、および注文情報」を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。

3.1 機能ブロック図

図 1-1 は、このデバイスの機能ブロック図です。

注

テキサス・インスツルメンツのソフトウェア開発キット (SDK) が現在サポートしているデバイス機能の詳細については、DRA829 および TDA4VM ソフトウェア ビルド シート (**PROCESSOR-SDK-J721E**) を参照してください。



A. このインターフェイスは MCU アイランドに位置しますが、システム全体からアクセス可能です。
B. DP、SGMII、USB3.0、PCIE[3:0] は合計 12 本の SerDes レーンを共有しています。
C. 2 つの同時フラッシュ インターフェイスは OSPI0 と OSPI1、または HyperBus™ と OSPI1 として構成されます。

図 3-1. 機能ブロック図

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4 Device Comparison

表 4-1 shows the features of the SoC.

注

To understand what device features are currently supported by TI Software Development Kits (SDKs), see the DRA829 and TDA4VM Software Build Sheet (**PROCESSOR-SDK-J721E**).

表 4-1. Device Comparison

FEATURES[7]	REFERENCE NAME	TDA4VM88	TDA4VM67	TDA4VM21
Features				
PROCESSORS AND ACCELERATORS				
Speed Grades		T	L	E
Arm Cortex-A72 Microprocessor Subsystem	Arm A72	Dual Core	Dual Core	Dual Core
Arm Cortex-R5F	Arm R5F	Hexa Core	Hexa Core	Quad Core[9]
	Lockstep	Optional[1]	Optional[1]	Optional[1]
Device Management Security Controller	DMSC	Yes	Yes	Yes
C7x Floating Point, Vector DSP	C7x DSP	Yes	Yes	Yes
Deep Learning Accelerator	MMA	Yes	Yes	Yes
Two C66x Floating Point DSP	C66x DSP	Dual Core	Dual Core	Single Core
Graphics Accelerator 3D GPU PowerVR Rogue 8XE GE8430	GPU	Yes	Yes	Yes
Depth and Motion Processing Accelerators	DMPAC	Yes	Yes	No
Vision Processing Accelerators	VPAC	Yes	Yes	Yes
Security Accelerators	SA	Yes	Yes	Yes
Video Encoder / Decoder	VENC/ VDEC	Yes	Yes	Yes
SAFETY AND SECURITY				
Safety Targeted	Safety	Optional[1]	Optional[1]	Optional[1]
Device Security	Security	Optional[2]	Optional[2]	Optional[2]
AEC-Q100 Qualified	Q1	Optional[3]	Optional[3]	Optional[3]
PROGRAM AND DATA STORAGE				
On-Chip Shared Memory (RAM) in MAIN Domain	OCSRAM	512KB SRAM	512KB SRAM	512KB SRAM
On-Chip Shared Memory (RAM) in MCU Domain	MCU_MSRAM	1MB SRAM	1MB SRAM	1MB SRAM
Multicore Shared Memory Controller	MSMC	8MB (On-Chip SRAM with ECC)	8MB (On-Chip SRAM with ECC)	8MB (On-Chip SRAM with ECC)
LPDDR4 DDR Subsystem	DDRSS	Up to 8GB (32-bit data) with inline ECC	Up to 8GB (32-bit data) with inline ECC	Up to 8GB (32-bit data) with inline ECC
	SECDED	7-Bit	7-Bit	7-Bit
General-Purpose Memory Controller	GPMC	Up to 1GB with ECC	Up to 1GB with ECC	Up to 1GB with ECC
PERIPHERALS				
Display Subsystem	DSS	Yes	Yes	Yes
Modular Controller Area Network Interface with Full CAN-FD Support	MCAN	16	16	16
General-Purpose I/O	GPIO	Up to 226	Up to 226	Up to 226
Inter-Integrated Circuit Interface	I2C	10	10	10
Improved Inter-Integrated Circuit Interface	I3C	3	3	3
Analog-to-Digital Converter	ADC	2	2	2

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表 4-1. Device Comparison (続き)

FEATURES[7]	REFERENCE NAME	TDA4VM88	TDA4VM67	TDA4VM21
Capture Subsystem with Camera Serial Interface (CSI2)	CSI2.0 4L RX	2	2	2
	CSI2.0 4L TX	1	1	1
Multichannel Serial Peripheral Interface	MCSPI	11	11	11
Multichannel Audio Serial Port	MCASP0	16 Serializers	16 Serializers	16 Serializers
	MCASP1	12 Serializers	12 Serializers	12 Serializers
	MCASP2	6 Serializers	6 Serializers	6 Serializers
	MCASP3	4 Serializers	4 Serializers	4 Serializers
	MCASP4	4 Serializers	4 Serializers	4 Serializers
	MCASP5	4 Serializers	4 Serializers	4 Serializers
	MCASP6	4 Serializers	4 Serializers	4 Serializers
	MCASP7	4 Serializers	4 Serializers	4 Serializers
	MCASP8	4 Serializers	4 Serializers	4 Serializers
	MCASP9	4 Serializers	4 Serializers	4 Serializers
	MCASP10	8 Serializers	8 Serializers	8 Serializers
	MCASP11	8 Serializers	8 Serializers	8 Serializers
MultiMedia Card/ Secure Digital Interface	MMCSD0	eMMC (8-bits)	eMMC (8-bits)	eMMC (8-bits)
	MMCSD1	SD/SDIO (4-bits)	SD/SDIO (4-bits)	SD/SDIO (4-bits)
	MMCSD2	SD/SDIO (4-bits)	SD/SDIO (4-bits)	SD/SDIO (4-bits)
Universal Flash Storage	UFS 2L	Yes (2 Lanes)	Yes (2 Lanes)	Yes (2 Lanes)
Flash Subsystem (FSS)	OSPI0	8-bits[6]	8-bits[6]	8-bits[6]
	OSPI1[8]	4-bits	4-bits	4-bits
	HyperBus	Yes[6]	Yes[6]	Yes[6]
4x PCI Express Port with Integrated PHY	PCIE0	Up to Two Lanes[4]	Up to Two Lanes[4]	Up to Two Lanes[4]
	PCIE1	Up to Two Lanes[4]	Up to Two Lanes[4]	Up to Two Lanes[4]
	PCIE2	Up to Two Lanes[4]	Up to Two Lanes[4]	Up to Two Lanes[4]
	PCIE3	Up to Two Lanes[4]	Up to Two Lanes[4]	Up to Two Lanes[4]
2x Programmable Real-Time Unit Subsystem and TSN Communication Subsystem (Ethernet Subsystem)	PRU_ICSSG0	No	No	No
	PRU_ICSSG1	No	No	No
Gigabit Ethernet Interface	CPSW2G	RMII or RGMII	RMII or RGMII	RMII or RGMII
	CPSW9G	8 × RMII 8 × RGMII 8 × SGMII[4]	4 × RMII 4 × RGMII 4 × SGMII[4] [5]	2 × RMII 2 × RGMII 2 × SGMII[4] [5]
General-Purpose Timers	TIMER	30	30	30
Enhanced High Resolution Pulse-Width Modulator Module	eHRPWM	6	6	6
Enhanced Capture Module	eCAP	3	3	3
Enhanced Quadrature Encoder Pulse Module	eQEP	3	3	3
Universal Asynchronous Receiver and Transmitter	UART	12	12	12
Universal Serial Bus (USB3.1) SuperSpeed Dual-Role-Device (DRD) Ports with SS PHY	USB0	Yes[4]	Yes[4]	Yes[4]
	USB1	Yes[4]	Yes[4]	Yes[4]

(1) Safety features including R5F Lockstep and SIL/ASIL ratings are only applicable to select part number variants as indicated by the Device Type (Y) identifier in the 表 9-1, *Nomenclature Description* table.
(2) Device security features including Secure Boot and Customer Programmable Keys are applicable to select part number variants as indicated by the Device Type (Y) identifier in the 表 9-1, *Nomenclature Description* table..
(3) AEC-Q100 qualification is applicable to select part number variants as indicated by the Automotive Designator (Q1) identifier in the 表 9-1, *Nomenclature Description* table.

(4) DP, SGMII, USB3.0, and PCIE[3:0] share total of twelve SerDes lanes.
(5) Devices that support 4x RMII, 4x RGMII, 4x SGMII
Allowed instances and pins:
   a. RMII1/RGMII1/SGMII1
   b. RMII2/RGMII2/SGMII2
   c. RMII3/RGMII3/SGMII3
   d. RMII4/RGMII4/SGMII4

   Devices that support 2x RMII, 2x RGMII, 2x SGMII
   Allowed instances and pins:
   a. RMII1/RGMII1/SGMII1
   b. RMII2/RGMII2/SGMII2
(6) Two simultaneous flash interfaces configured as OSPI0 and OSPI1, or HyperBus and OSPI1.
(7) Software should constrain the features used to match the intended production device.
(8) OSPI1 module only pins out 4 pins and is referred to as QSPI in some contexts.
(9) The Quad Core R5F device provides support for a dual core RF5 in the MCU domain (MCU_R5FSS) and a dual core R5F in the Main domain (R5FSS0).

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4.1 Related Products

Companion Products for TDA4VM Review products that are frequently purchased or used in conjunction with this product.

Software Development Kit for DRA8x & TDA4x Jacinto™ Processors Processor SDK RTOS (PSDK RTOS) can be used together with Processor SDK Linux (PSDK Linux) or Processor SDK QNX (PSDK QNX), to form a multi-processor software development platform for TDA4x and DRA8x SoCs within the TI's Jacinto™ Processors platform. The SDK provides a comprehensive set of software tools and components to help users develop and deploy their applications on supported J7 SoCs. PSDK RTOS and either PSDK Linux or PSDK QNX can be used together to implement various use-cases in robotics, vision, factory and building automation, and automotive ADAS and gateway systems.

TDA4VM Evaluation Module The TDA4VMXEVM is an evaluation platform designed to speed up development efforts and reduce time to market for ADAS applications.

The TDA4x EVM is based on a TDA4VMx System-on-Chip (SoC) that incorporates a powerful heterogeneous, scalable architecture that includes a mix of TI's fixed and floating-point TMS320C66x Digital Signal Processor (DSP) cores, the C71x DSP Core and Matrix Math Accelerator for AI, Arm® Cortex®-A72 cores, integrated ISP and vision processing acceleration, 2D and 3D GPU cores, H.264 encode/H.265 decode acceleration. An on-chip Safety island featuring dual-lockstep R5F cores helps the system achieve ASIL-D/SIL-3 level certification while reducing the need for an external safety microcontroller, further reducing system bill-of-materials. On-chip peripherals allow for multi-camera input via CSI-2 ports, vehicle connectivity based on PCI Express, CAN-FD and Gigabit Ethernet, and display connectivity via DSI interfaces.

The EVM is supported by the Processor SDK which includes foundational drivers, compute and vision kernels, and example application frameworks and demonstrations that show users how to take advantage of the powerful heterogeneous SoC architecture.

Application Notes and White Paper Next generation SoC family for L2/L3, near-field analytic systems using deep learning technologies

5 Terminal Configuration and Functions

5.1 Pin Diagram

注

The terms "ball", "pin", and "terminal" are used interchangeably throughout the document. An attempt is made to use "ball" only when referring to the physical package.

図 5-1 shows the ball locations for the 827-ball flip chip ball grid array (FCBGA) package that are used in conjunction with 表 5-1 図 5-1through 図 5-1 to locate signal names and ball grid numbers.

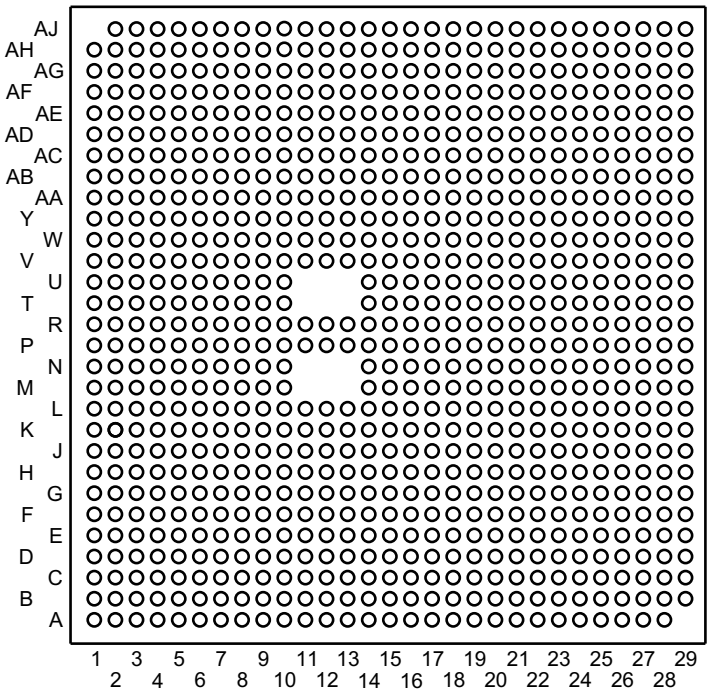

図 5-1. ALF FCBGA-N827 Pin Diagram (Bottom View)

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5.2 Pin Attributes

注

MCU_BOOTMODE pins are latched on the rising edge of MCU_PORz_OUT. BOOTMODE pins are latched on the rising edge of PORz_OUT.

注

Media Local Bus (MLB) is not available on this device.The following balls must be left unconnected if not used in GPIO mode: AE2, AD2, AD3, AC3, AC1, AD1

注

PRU_ICSSG0 and PRU_ICSSG1 are not available on this device. The prg* signals should not be used. Those pins can be used for other functions.

注

Devices that support CPSW9G Gigabit Ethernet Interface of 4x RMII, 4x RGMII, 4x SGMII
Allowed instances and pins:

1. RMII1/RGMII1/SGMII1
2. RMII2/RGMII2/SGMII2
3. RMII3/RGMII3/SGMII3
4. RMII4/RGMII4/SGMII4

Devices that support CPSW9G Gigabit Ethernet Interface of 2x RMII, 2x RGMII, 2x SGMII
Allowed instances and pins:

1. RMII1/RGMII1/SGMII1
2. RMII2/RGMII2/SGMII2

表 5-1. Pin Attributes

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
U7	CAP_VDDS0	CAP_VDDS0		CAP									
K23	CAP_VDDS0_MCU	CAP_VDDS0_MCU		CAP									
AB21	CAP_VDDS1	CAP_VDDS1		CAP									
J18	CAP_VDDS1_MCU	CAP_VDDS1_MCU		CAP									
Y18	CAP_VDDS2	CAP_VDDS2		CAP									
J19	CAP_VDDS2_MCU	CAP_VDDS2_MCU		CAP									

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
W21	CAP_VDDS3	CAP_VDDS3		CAP									
AA22	CAP_VDDS4	CAP_VDDS4		CAP									
R22	CAP_VDDS5	CAP_VDDS5		CAP									
V22	CAP_VDDS6	CAP_VDDS6		CAP									
B20	CSI0_RXCLKN	CSI0_RXCLKN		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
A21	CSI0_RXCLKP	CSI0_RXCLKP		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
F16	csi0_rxrcalib	CSI0_RXRCALIB		A	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
F15	csi1_rxrcalib	CSI1_RXRCALIB		A	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
B17	CSI1_RXCLKN	CSI1_RXCLKN		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
A18	CSI1_RXCLKP	CSI1_RXCLKP		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
B19	CSI0_RXN0	CSI0_RXN0		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
D18	CSI0_RXN1	CSI0_RXN1		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
D17	CSI0_RXN2	CSI0_RXN2		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
E16	CSI0_RXN3	CSI0_RXN3		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
A20	CSI0_RXP0	CSI0_RXP0		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
C19	CSI0_RXP1	CSI0_RXP1		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
C18	CSI0_RXP2	CSI0_RXP2		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
E17	CSI0_RXP3	CSI0_RXP3		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
B16	CSI1_RXN0	CSI1_RXN0		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
D15	CSI1_RXN1	CSI1_RXN1		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
D14	CSI1_RXN2	CSI1_RXN2		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
E13	CSI1_RXN3	CSI1_RXN3		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
A17	CSI1_RXP0	CSI1_RXP0		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
C16	CSI1_RXP1	CSI1_RXP1		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
C15	CSI1_RXP2	CSI1_RXP2		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
E14	CSI1_RXP3	CSI1_RXP3		I	OFF		1.8 V	VDDA_0P8_CSIRX / VDDA_1P8_CSIRX		D-PHY			
J1	ddr0_ckn	DDR0_CKN		IO	OFF		1.1 V	VDDS_DDR		DDR0			
H1	ddr0_ckp	DDR0_CKP		IO	OFF		1.1 V	VDDS_DDR		DDR0			
K6	ddr0_resetn	DDR0_RESETn		IO	OFF		1.1 V	VDDS_DDR		DDR0			
G4	ddr0_ca0	DDR0_CA0		IO	OFF		1.1 V	VDDS_DDR		DDR0			
H3	ddr0_ca1	DDR0_CA1		IO	OFF		1.1 V	VDDS_DDR		DDR0			

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
K5	ddr0_ca2	DDR0_CA2		IO	OFF		1.1 V	VDDS_DDR		DDR0			
J4	ddr0_ca3	DDR0_CA3		IO	OFF		1.1 V	VDDS_DDR		DDR0			
K2	ddr0_ca4	DDR0_CA4		IO	OFF		1.1 V	VDDS_DDR		DDR0			
H5	ddr0_ca5	DDR0_CA5		IO	OFF		1.1 V	VDDS_DDR		DDR0			
H2	ddr0_cal0	DDR0_CAL0		A	OFF		1.1 V	VDDS_DDR		DDR0			
G3	ddr0_cke0	DDR0_CKE0		IO	OFF		1.1 V	VDDS_DDR		DDR0			
J3	ddr0_cke1	DDR0_CKE1		IO	OFF		1.1 V	VDDS_DDR		DDR0			
J5	ddr0_csn0_0	DDR0_CSn0_0		IO	OFF		1.1 V	VDDS_DDR		DDR0			
K3	ddr0_csn0_1	DDR0_CSn0_1		IO	OFF		1.1 V	VDDS_DDR		DDR0			
G5	ddr0_csn1_0	DDR0_CSn1_0		IO	OFF		1.1 V	VDDS_DDR		DDR0			
J2	ddr0_csn1_1	DDR0_CSn1_1		IO	OFF		1.1 V	VDDS_DDR		DDR0			
A3	ddr0_dm0	DDR0_DM0		IO	OFF		1.1 V	VDDS_DDR		DDR0			
E4	ddr0_dm1	DDR0_DM1		IO	OFF		1.1 V	VDDS_DDR		DDR0			
N1	ddr0_dm2	DDR0_DM2		IO	OFF		1.1 V	VDDS_DDR		DDR0			
R5	ddr0_dm3	DDR0_DM3		IO	OFF		1.1 V	VDDS_DDR		DDR0			
A5	ddr0_dq0	DDR0_DQ0		IO	OFF		1.1 V	VDDS_DDR		DDR0			
A6	ddr0_dq1	DDR0_DQ1		IO	OFF		1.1 V	VDDS_DDR		DDR0			
B5	ddr0_dq2	DDR0_DQ2		IO	OFF		1.1 V	VDDS_DDR		DDR0			
C2	ddr0_dq3	DDR0_DQ3		IO	OFF		1.1 V	VDDS_DDR		DDR0			
B4	ddr0_dq4	DDR0_DQ4		IO	OFF		1.1 V	VDDS_DDR		DDR0			
C3	ddr0_dq5	DDR0_DQ5		IO	OFF		1.1 V	VDDS_DDR		DDR0			
A2	ddr0_dq6	DDR0_DQ6		IO	OFF		1.1 V	VDDS_DDR		DDR0			
A4	ddr0_dq7	DDR0_DQ7		IO	OFF		1.1 V	VDDS_DDR		DDR0			
D1	ddr0_dq8	DDR0_DQ8		IO	OFF		1.1 V	VDDS_DDR		DDR0			
C4	ddr0_dq9	DDR0_DQ9		IO	OFF		1.1 V	VDDS_DDR		DDR0			
F1	ddr0_dq10	DDR0_DQ10		IO	OFF		1.1 V	VDDS_DDR		DDR0			
G2	ddr0_dq11	DDR0_DQ11		IO	OFF		1.1 V	VDDS_DDR		DDR0			
F2	ddr0_dq12	DDR0_DQ12		IO	OFF		1.1 V	VDDS_DDR		DDR0			
F3	ddr0_dq13	DDR0_DQ13		IO	OFF		1.1 V	VDDS_DDR		DDR0			
D3	ddr0_dq14	DDR0_DQ14		IO	OFF		1.1 V	VDDS_DDR		DDR0			
F5	ddr0_dq15	DDR0_DQ15		IO	OFF		1.1 V	VDDS_DDR		DDR0			
L5	ddr0_dq16	DDR0_DQ16		IO	OFF		1.1 V	VDDS_DDR		DDR0			
M5	ddr0_dq17	DDR0_DQ17		IO	OFF		1.1 V	VDDS_DDR		DDR0			
N5	ddr0_dq18	DDR0_DQ18		IO	OFF		1.1 V	VDDS_DDR		DDR0			
L4	ddr0_dq19	DDR0_DQ19		IO	OFF		1.1 V	VDDS_DDR		DDR0			
L2	ddr0_dq20	DDR0_DQ20		IO	OFF		1.1 V	VDDS_DDR		DDR0			
L1	ddr0_dq21	DDR0_DQ21		IO	OFF		1.1 V	VDDS_DDR		DDR0			

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
N2	ddr0_dq22	DDR0_DQ22		IO	OFF		1.1 V	VDDS_DDR		DDR0			
N4	ddr0_dq23	DDR0_DQ23		IO	OFF		1.1 V	VDDS_DDR		DDR0			
T3	ddr0_dq24	DDR0_DQ24		IO	OFF		1.1 V	VDDS_DDR		DDR0			
T2	ddr0_dq25	DDR0_DQ25		IO	OFF		1.1 V	VDDS_DDR		DDR0			
P2	ddr0_dq26	DDR0_DQ26		IO	OFF		1.1 V	VDDS_DDR		DDR0			
P3	ddr0_dq27	DDR0_DQ27		IO	OFF		1.1 V	VDDS_DDR		DDR0			
P5	ddr0_dq28	DDR0_DQ28		IO	OFF		1.1 V	VDDS_DDR		DDR0			
R4	ddr0_dq29	DDR0_DQ29		IO	OFF		1.1 V	VDDS_DDR		DDR0			
T4	ddr0_dq30	DDR0_DQ30		IO	OFF		1.1 V	VDDS_DDR		DDR0			
T5	ddr0_dq31	DDR0_DQ31		IO	OFF		1.1 V	VDDS_DDR		DDR0			
B1	ddr0_dqs0n	DDR0_DQS0N		IO	OFF		1.1 V	VDDS_DDR		DDR0			
B2	ddr0_dqs0p	DDR0_DQS0P		IO	OFF		1.1 V	VDDS_DDR		DDR0			
E2	ddr0_dqs1n	DDR0_DQS1N		IO	OFF		1.1 V	VDDS_DDR		DDR0			
E3	ddr0_dqs1p	DDR0_DQS1P		IO	OFF		1.1 V	VDDS_DDR		DDR0			
M2	ddr0_dqs2n	DDR0_DQS2N		IO	OFF		1.1 V	VDDS_DDR		DDR0			
M3	ddr0_dqs2p	DDR0_DQS2P		IO	OFF		1.1 V	VDDS_DDR		DDR0			
R1	ddr0_dqs3n	DDR0_DQS3N		IO	OFF		1.1 V	VDDS_DDR		DDR0			
R2	ddr0_dqs3p	DDR0_DQS3P		IO	OFF		1.1 V	VDDS_DDR		DDR0			
P6	ddr_ret	DDR_RET		I	OFF		1.1 V	VDDS_DDR_BIAS		DDR0			
G6	dp0_auxn	DP0_AUXN		IO	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		AUX-PHY			
F7	dp0_auxp	DP0_AUXP		IO	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		AUX-PHY			
E10	DSI_TXCLKN	DSI_TXCLKN		O	OFF		1.8 V	VDDA_0P8_DSITX / VDDA_1P8_DSITX		D-PHY			
		CSI0_TXCLKN		O									
E11	DSI_TXCLKP	DSI_TXCLKP		O	OFF		1.8 V	VDDA_0P8_DSITX / VDDA_1P8_DSITX		D-PHY			
		CSI0_TXCLKP		O									
D11	DSI_TXN0	DSI_TXN0		IO	OFF		1.8 V	VDDA_0P8_DSITX / VDDA_1P8_DSITX		D-PHY			
		CSI0_TXN0		O									
D12	DSI_TXN1	DSI_TXN1		O	OFF		1.8 V	VDDA_0P8_DSITX / VDDA_1P8_DSITX		D-PHY			
		CSI0_TXN1		O									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
B13	DSI_TXN2	DSI_TXN2		O	OFF		1.8 V	VDDA_0P8_DSITX / VDDA_1P8_DSITX		D-PHY			
		CSI0_TXN2		O									
B14	DSI_TXN3	DSI_TXN3		O	OFF		1.8 V	VDDA_0P8_DSITX / VDDA_1P8_DSITX		D-PHY			
		CSI0_TXN3		O									
C12	DSI_TXP0	DSI_TXP0		IO	OFF		1.8 V	VDDA_0P8_DSITX / VDDA_1P8_DSITX		D-PHY			
		CSI0_TXP0		O									
C13	DSI_TXP1	DSI_TXP1		O	OFF		1.8 V	VDDA_0P8_DSITX / VDDA_1P8_DSITX		D-PHY			
		CSI0_TXP1		O									
A14	DSI_TXP2	DSI_TXP2		O	OFF		1.8 V	VDDA_0P8_DSITX / VDDA_1P8_DSITX		D-PHY			
		CSI0_TXP2		O									
A15	DSI_TXP3	DSI_TXP3		O	OFF		1.8 V	VDDA_0P8_DSITX / VDDA_1P8_DSITX		D-PHY			
		CSI0_TXP3		O									
F12	dsi_txrcalib	DSI_TXRCALIB		A	OFF		1.8 V	VDDA_0P8_DSITX / VDDA_1P8_DSITX		D-PHY			
U2	ecap0_in_apwm_out	ECAP0_IN_APWM_OUT	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	0/1
		SYNC0_OUT	1	O									
		CPTS0_RFT_CLK	2	I								0	
		SPI2_CS3	4	IO								1	
		I3C0_SDAPULLEN	5	O									
		SPI7_CS0	6	IO								1	
		GPIO1_11	7	IO								0	
C26	emu0	EMU0	0	IO	PU	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		1/1
B29	emu1	EMU1	0	IO	PU	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		1/1
AC18	extintn	EXTINTn	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	I2C OD FS		1	0/0
		GPIO0_0	7	IO								0	
U3	ext_refclk1	EXT_REFCLK1	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	0/1
		SYNC1_OUT	1	O									
		SPI7_CLK	6	IO								0	
		GPIO1_12	7	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AC5	i2c0_scl	I2C0_SCL	0	IOD	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OD FS		1	1/0
		GPIO1_7	7	IO								0	
AA5	i2c0_sda	I2C0_SDA	0	IOD	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OD FS		1	1/0
		GPIO1_8	7	IO								0	
Y6	i2c1_scl	I2C1_SCL	0	IOD	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OD FS		1	1/0
		CPTS0_HW1TSPUSH	1	I								0	
		GPIO1_9	7	IO								0	
AA6	i2c1_sda	I2C1_SDA	0	IOD	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	I2C OD FS		1	1/0
		CPTS0_HW2TSPUSH	1	I								0	
		GPIO1_10	7	IO								0	
W2	i3c0_scl	I3C0_SCL	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	1	0/1
		MMC2_SDCD	1	I								1	
		UART9_CTSn	2	I								1	
		MCAN2_RX	3	I								1	
		I2C6_SCL	4	IOD								1	
		DP0_HPD	5	I								0	
		PCIE0_CLKREQn	6	IO								0	
		GPIO1_5	7	IO								0	
		UART6_RXD	8	I								0	
W1	i3c0_sda	I3C0_SDA	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	1	0/1
		MMC2_SDWP	1	I								1	
		UART9_RTSn	2	O									
		MCAN2_TX	3	O									
		I2C6_SDA	4	IOD								1	
		PCIE1_CLKREQn	6	IO								0	
		GPIO1_6	7	IO								0	
		UART6_TXD	8	O								0	
W5	mcan0_rx	MCAN0_RX	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	1	0/1
		I2C2_SCL	4	IOD								1	
		GPIO1_1	7	IO								0	
W6	mcan0_tx	MCAN0_TX	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		0/1
		I2C2_SDA	4	IOD								1	
		GPIO1_2	7	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
W3	mcan1_rx	MCAN1_RX	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	1	0/1
		UART6_CTSn	1	I								1	
		UART9_RXD	2	I								1	
		USB0_DRVVBUS	3	O									
		USB1_DRVVBUS	4	O									
		GPIO1_3	7	IO								0	
V4	mcan1_tx	MCAN1_TX	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		0/1
		UART6_RTSn	1	O									
		UART9_TXD	2	O									
		USB0_DRVVBUS	3	O									
		USB1_DRVVBUS	4	O									
		GPIO1_4	7	IO								0	
K25	mcu_adc0_ain0	MCU_ADC0_AIN0	0	A	OFF	0	1.8 V	VDDA_ADC0		ADC12B			
		WKUP_GPIO0_68	-[1]	I									
K26	mcu_adc0_ain1	MCU_ADC0_AIN1	0	A	OFF	0	1.8 V	VDDA_ADC0		ADC12B			
		WKUP_GPIO0_69	-[1]	I									
K28	mcu_adc0_ain2	MCU_ADC0_AIN2	0	A	OFF	0	1.8 V	VDDA_ADC0		ADC12B			
		WKUP_GPIO0_70	-[1]	I									
L28	mcu_adc0_ain3	MCU_ADC0_AIN3	0	A	OFF	0	1.8 V	VDDA_ADC0		ADC12B			
		WKUP_GPIO0_71	-[1]	I									
K24	mcu_adc0_ain4	MCU_ADC0_AIN4	0	A	OFF	0	1.8 V	VDDA_ADC0		ADC12B			
		WKUP_GPIO0_72	-[1]	I									
K27	mcu_adc0_ain5	MCU_ADC0_AIN5	0	A	OFF	0	1.8 V	VDDA_ADC0		ADC12B			
		WKUP_GPIO0_73	-[1]	I									
K29	mcu_adc0_ain6	MCU_ADC0_AIN6	0	A	OFF	0	1.8 V	VDDA_ADC0		ADC12B			
		WKUP_GPIO0_74	-[1]	I									
L29	mcu_adc0_ain7	MCU_ADC0_AIN7	0	A	OFF	0	1.8 V	VDDA_ADC0		ADC12B			
		WKUP_GPIO0_75	-[1]	I									
N23	mcu_adc1_ain0	MCU_ADC1_AIN0	0	A	OFF	0	1.8 V	VDDA_ADC1		ADC12B			
		WKUP_GPIO0_76	-[1]	I									
M25	mcu_adc1_ain1	MCU_ADC1_AIN1	0	A	OFF	0	1.8 V	VDDA_ADC1		ADC12B			
		WKUP_GPIO0_77	-[1]	I									
L24	mcu_adc1_ain2	MCU_ADC1_AIN2	0	A	OFF	0	1.8 V	VDDA_ADC1		ADC12B			
		WKUP_GPIO0_78	-[1]	I									
L26	mcu_adc1_ain3	MCU_ADC1_AIN3	0	A	OFF	0	1.8 V	VDDA_ADC1		ADC12B			
		WKUP_GPIO0_79	-[1]	I									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
N24	mcu_adc1_ain4	MCU_ADC1_AIN4	0	A	OFF	0	1.8 V	VDDA_ADC1		ADC12B			
		WKUP_GPIO0_80	-[1]	I									
M24	mcu_adc1_ain5	MCU_ADC1_AIN5	0	A	OFF	0	1.8 V	VDDA_ADC1		ADC12B			
		WKUP_GPIO0_81	-[1]	I									
L25	mcu_adc1_ain6	MCU_ADC1_AIN6	0	A	OFF	0	1.8 V	VDDA_ADC1		ADC12B			
		WKUP_GPIO0_82	-[1]	I									
L27	mcu_adc1_ain7	MCU_ADC1_AIN7	0	A	OFF	0	1.8 V	VDDA_ADC1		ADC12B			
		WKUP_GPIO0_83	-[1]	I									
J26	mcu_i2c0_scl	MCU_I2C0_SCL	0	IOD	OFF	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	I2C OD FS		1	1/0
		WKUP_GPIO0_64	7	IO								0	
H25	mcu_i2c0_sda	MCU_I2C0_SDA	0	IOD	OFF	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	I2C OD FS		1	1/0
		WKUP_GPIO0_65	7	IO								0	
D26	mcu_i3c0_scl	MCU_I3C0_SCL	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	1	0/1
		MCU_UART0_CTSn	2	I								1	
		MCU_TIMER_IO8	4	IO								0	
		WKUP_GPIO0_60	7	IO								0	
D25	mcu_i3c0_sda	MCU_I3C0_SDA	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	1	0/1
		MCU_UART0_RTSn	2	O									
		MCU_TIMER_IO9	4	IO								0	
		WKUP_GPIO0_61	7	IO								0	
C29	mcu_mcan0_rx	MCU_MCAN0_RX	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	0	0/1
		WKUP_GPIO0_59	7	IO								0	
D29	mcu_mcan0_tx	MCU_MCAN0_TX	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		0/1
		WKUP_GPIO0_58	7	IO								0	
F23	mcu_mdio0_mdc	MCU_MDIO0_MDC	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD		0/1
		WKUP_GPIO0_51	7	IO								0	
E23	mcu_mdio0_mdio	MCU_MDIO0_MDIO	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD	0	0/1
		WKUP_GPIO0_50	7	IO								0	
E20	mcu_ospi0_clk	MCU_OSPI0_CLK	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD		0/1
		MCU_HYPERBUS0_CK	1	O									
		WKUP_GPIO0_16	7	IO								0	
D21	mcu_ospi0_dqs	MCU_OSPI0_DQS	0	I	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_HYPERBUS0_RWDS	1	IO								0	
		WKUP_GPIO0_18	7	IO								0	
C21	mcu_ospi0_lbclko	MCU_OSPI0_LBCLKO	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	1/1
		MCU_HYPERBUS0_CKn	1	O									
		WKUP_GPIO0_17	7	IO								0	

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
F22	mcu_ospi1_clk	MCU_OSPI1_CLK	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD		0/1
		WKUP_GPIO0_29	7	IO								0	
B23	mcu_ospi1_dqs	MCU_OSPI1_DQS	0	I	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_OSPI0_CSn3	1	O									
		MCU_HYPERBUS0_INTn	2	I								1	
		MCU_OSPI0_ECC_FAIL	6	I								1	
		WKUP_GPIO0_31	7	IO								0	
A23	mcu_ospi1_lbclko	MCU_OSPI1_LBCLKO	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	1/1
		MCU_OSPI0_CSn2	1	O									
		MCU_HYPERBUS0_RESETOn	2	I								1	
		MCU_OSPI0_RESET_OUT0	6	O									
		WKUP_GPIO0_30	7	IO								0	
F19	mcu_ospi0_csn0	MCU_OSPI0_CSn0	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD		0/1
		MCU_HYPERBUS0_CSn0	1	O									
		WKUP_GPIO0_27	7	IO								0	
E19	mcu_ospi0_csn1	MCU_OSPI0_CSn1	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD		0/1
		MCU_HYPERBUS0_RESETn	1	O									
		WKUP_GPIO0_28	7	IO								0	
D20	mcu_ospi0_d0	MCU_OSPI0_D0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_HYPERBUS0_DQ0	1	IO								0	
		WKUP_GPIO0_19	7	IO								0	
G19	mcu_ospi0_d1	MCU_OSPI0_D1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_HYPERBUS0_DQ1	1	IO								0	
		WKUP_GPIO0_20	7	IO								0	
G20	mcu_ospi0_d2	MCU_OSPI0_D2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_HYPERBUS0_DQ2	1	IO								0	
		WKUP_GPIO0_21	7	IO								0	
F20	mcu_ospi0_d3	MCU_OSPI0_D3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_HYPERBUS0_DQ3	1	IO								0	
		WKUP_GPIO0_22	7	IO								0	
F21	mcu_ospi0_d4	MCU_OSPI0_D4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_HYPERBUS0_DQ4	1	IO								0	
		WKUP_GPIO0_23	7	IO								0	
E21	mcu_ospi0_d5	MCU_OSPI0_D5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_HYPERBUS0_DQ5	1	IO								0	
		WKUP_GPIO0_24	7	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
B22	mcu_ospi0_d6	MCU_OSPI0_D6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_HYPERBUS0_DQ6	1	IO								0	
		WKUP_GPIO0_25	7	IO								0	
G21	mcu_ospi0_d7	MCU_OSPI0_D7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_HYPERBUS0_DQ7	1	IO								0	
		WKUP_GPIO0_26	7	IO								0	
C22	mcu_ospi1_csn0	MCU_OSPI1_CSn0	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD		0/1
		WKUP_GPIO0_36	7	IO								0	
E22	mcu_ospi1_csn1	MCU_OSPI1_CSn1	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD		0/1
		MCU_HYPERBUS0_WPn	1	O									
		MCU_TIMER_IO0	2	IO								0	
		MCU_HYPERBUS0_CSn1	3	O									
		MCU_UART0_RTSn	4	O									
		MCU_SPI0_CS2	5	IO								1	
		MCU_OSPI0_RESET_OUT1	6	O									
		WKUP_GPIO0_37	7	IO								0	
D22	mcu_ospi1_d0	MCU_OSPI1_D0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		WKUP_GPIO0_32	7	IO								0	
G22	mcu_ospi1_d1	MCU_OSPI1_D1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_UART0_RXD	4	I								1	
		MCU_SPI1_CS1	5	IO								1	
		WKUP_GPIO0_33	7	IO								0	
D23	mcu_ospi1_d2	MCU_OSPI1_D2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_UART0_TXD	4	O									
		MCU_SPI1_CS2	5	IO								1	
		WKUP_GPIO0_34	7	IO								0	
C23	mcu_ospi1_d3	MCU_OSPI1_D3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_UART0_CTSn	4	I								1	
		MCU_SPI0_CS1	5	IO								1	
		WKUP_GPIO0_35	7	IO								0	
H23	mcu_porz	MCU_PORz		I	OFF		1.8 V	VDDA_WKUP	Yes	FS Reset	PU/PD		
B28	mcu_porz_out	MCU_PORz_OUT	0	O	OFF	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		0/0
C27	mcu_resetstatz	MCU_RESETSTATz	0	O	OFF	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		0/0
D28	mcu_resetz	MCU_RESETz	0	I	PU	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		1/1

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
C24	mcu_rgmii1_rxc	MCU_RGMII1_RXC	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_RMII1_REF_CLK	1	I								0	
		WKUP_GPIO0_45	7	IO								0	
C25	mcu_rgmii1_rx_ctl	MCU_RGMII1_RX_CTL	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_RMII1_RX_ER	1	I								0	
		WKUP_GPIO0_39	7	IO								0	
B26	mcu_rgmii1_txc	MCU_RGMII1_TXC	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_RMII1_TX_EN	1	O									
		WKUP_GPIO0_44	7	IO								0	
B27	mcu_rgmii1_tx_ctl	MCU_RGMII1_TX_CTL	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD		0/1
		MCU_RMII1_CRS_DV	1	I								0	
		WKUP_GPIO0_38	7	IO								0	
B24	mcu_rgmii1_rd0	MCU_RGMII1_RD0	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_RMII1_RXD0	1	I								0	
		WKUP_GPIO0_49	7	IO								0	
A24	mcu_rgmii1_rd1	MCU_RGMII1_RD1	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_RMII1_RXD1	1	I								0	
		WKUP_GPIO0_48	7	IO								0	
D24	mcu_rgmii1_rd2	MCU_RGMII1_RD2	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_TIMER_IO5	1	IO								0	
		WKUP_GPIO0_47	7	IO								0	
A25	mcu_rgmii1_rd3	MCU_RGMII1_RD3	0	I	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_TIMER_IO4	1	IO								0	
		WKUP_GPIO0_46	7	IO								0	
B25	mcu_rgmii1_td0	MCU_RGMII1_TD0	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD		0/1
		MCU_RMII1_TXD0	1	O									
		WKUP_GPIO0_43	7	IO								0	
A26	mcu_rgmii1_td1	MCU_RGMII1_TD1	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD		0/1
		MCU_RMII1_TXD1	1	O									
		WKUP_GPIO0_42	7	IO								0	
A27	mcu_rgmii1_td2	MCU_RGMII1_TD2	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD		0/1
		MCU_TIMER_IO3	1	IO								0	
		MCU_ADC_EXT_TRIGGER1	3	I								0	
		WKUP_GPIO0_41	7	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
A28	mcu_rgmii1_td3	MCU_RGMII1_TD3	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2_MCU	Yes	LVCMOS	PU/PD		0/1
		MCU_TIMER_IO2	1	IO								0	
		MCU_ADC_EXT_TRIGGER0	3	I								0	
		WKUP_GPIO0_40	7	IO								0	
D27	mcu_safety_errorn	MCU_SAFETY_ERRORn	0	IO	PD	0	1.8 V	VDDA_WKUP	Yes	LVCMOS	PU/PD		1/0
E27	mcu_spi0_clk	MCU_SPI0_CLK	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	0	1/1
		WKUP_GPIO0_52	7	IO								0	
		MCU_BOOTMODE00	Bootstrap	I									
E25	mcu_spi0_cs0	MCU_SPI0_CS0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	1	0/1
		MCU_TIMER_IO1	4	IO								0	
		WKUP_GPIO0_55	7	IO								0	
E24	mcu_spi0_d0	MCU_SPI0_D0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	0	1/1
		WKUP_GPIO0_53	7	IO								0	
		MCU_BOOTMODE01	Bootstrap	I									
E28	mcu_spi0_d1	MCU_SPI0_D1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	0	1/1
		MCU_TIMER_IO0	4	IO								0	
		WKUP_GPIO0_54	7	IO								0	
		MCU_BOOTMODE02	Bootstrap	I									
V24	mdio0_mdc	MDIO0_MDC	0	O	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD		0/1
		TRC_DATA23	5	O									
		GPIO0_110	7	IO								0	
		GPMC0_WAIT2	8	I								0	
V26	mdio0_mdio	MDIO0_MDIO	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1
		TRC_DATA22	5	O									
		GPIO0_109	7	IO								0	
		GPMC0_WAIT3	8	I								0	
AE2	mlb0_mlbcn	MLB0_MLBCN	0	I	OFF	0	1.8 V	VDDA_1P8_MLB		MLB_LVDS			
		GPIO1_35	7	IO								0	
AD2	mlb0_mlbcp	MLB0_MLBCP	0	I	OFF	0	1.8 V	VDDA_1P8_MLB		MLB_LVDS			
		GPIO1_34	7	IO								0	
AD3	mlb0_mlbdn	MLB0_MLBDN	0	IO	OFF	0	1.8 V	VDDA_1P8_MLB		MLB_LVDS			
		GPIO1_33	7	IO								0	
AC3	mlb0_mlbdp	MLB0_MLBDP	0	IO	OFF	0	1.8 V	VDDA_1P8_MLB		MLB_LVDS			
		GPIO1_32	7	IO								0	
AC1	mlb0_mlbsn	MLB0_MLBSN	0	IO	OFF	0	1.8 V	VDDA_1P8_MLB		MLB_LVDS			
		GPIO1_31	7	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AD1	mlb0_mlbsp	MLB0_MLBSP	0	IO	OFF	0	1.8 V	VDDA_1P8_MLB		MLB_LVDS			
		GPIO1_30	7	IO								0	
AE1	mmc0_calpad	MMC0_CALPAD		A	OFF		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD		
AF1	mmc0_clk	MMC0_CLK		O	DRIVE 0 (OFF)		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD		
AE3	mmc0_cmd	MMC0_CMD		IO	DRIVE 1 (OFF)		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD	1	
AE4	mmc0_ds	MMC0_DS		IO	PD		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD	1	
P25	mmc1_clk	MMC1_CLK	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD	0	0/1
		UART8_RXD	1	I								1	
		I2C4_SCL	4	IOD								1	
		GPIO1_19	7	IO								0	
R29	mmc1_cmd	MMC1_CMD	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD	1	0/1
		UART8_TXD	1	O									
		I2C4_SDA	4	IOD								1	
		GPIO1_20	7	IO								0	
P23	mmc1_sdcd	MMC1_SDCD	0	I	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	1	0/1
		UART8_CTSn	1	I								1	
		UART0_DCDn	2	I								1	
		TIMER_IO2	3	IO								0	
		EQEP2_I	5	IO								0	
		PCIE2_CLKREQn	6	IO								0	
		GPIO1_21	7	IO								0	
		PRG0_IEP0_EDC_LATCH_IN1	8	I								0	
R28	mmc1_sdwp	MMC1_SDWP	0	I	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	1	0/1
		UART8_RTSn	1	O									
		UART0_DSRn	2	I								1	
		TIMER_IO3	3	IO								0	
		ECAP2_IN_APWM_OUT	4	IO								0	
		EQEP2_S	5	IO								0	
		PCIE3_CLKREQn	6	IO								0	
		GPIO1_22	7	IO								0	
		PRG0_IEP0_EDC_SYNC_OUT1	8	O								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
T26	mmc2_clk	MMC2_CLK	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD	0	0/1
		USB0_DRVVBUS	1	O									
		USB1_DRVVBUS	2	O									
		TIMER_IO6	3	IO								0	
		I2C3_SCL	4	IOD								1	
		UART3_RXD	5	I								1	
		GPIO1_27	7	IO								0	
T25	mmc2_cmd	MMC2_CMD	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD	1	0/1
		USB0_DRVVBUS	1	O									
		USB1_DRVVBUS	2	O									
		TIMER_IO7	3	IO								0	
		I2C3_SDA	4	IOD								1	
		UART3_TXD	5	O									
		GPIO1_28	7	IO								0	
AG2	mmc0_dat0	MMC0_DAT0		IO	PU		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD	1	
AH1	mmc0_dat1	MMC0_DAT1		IO	PU		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD	1	
AG3	mmc0_dat2	MMC0_DAT2		IO	PU		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD	1	
AF4	mmc0_dat3	MMC0_DAT3		IO	PU		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD	1	
AE5	mmc0_dat4	MMC0_DAT4		IO	PU		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD	1	
AF3	mmc0_dat5	MMC0_DAT5		IO	PU		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD	1	
AG1	mmc0_dat6	MMC0_DAT6		IO	PU		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD	1	
AF2	mmc0_dat7	MMC0_DAT7		IO	PU		1.8 V	VDDS_MMC0		eMMCPHY	PU/PD	1	
R24	mmc1_dat0	MMC1_DAT0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD	1	0/1
		UART7_RTSn	1	O									
		ECAP1_IN_APWM_OUT	2	IO								0	
		TIMER_IO1	3	IO								0	
		UART4_TXD	5	O									
		GPIO1_18	7	IO								0	
P24	mmc1_dat1	MMC1_DAT1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD	1	0/1
		UART7_CTSn	1	I								1	
		ECAP0_IN_APWM_OUT	2	IO								0	
		TIMER_IO0	3	IO								0	
		UART4_RXD	5	I								1	
		GPIO1_17	7	IO								0	
R25	mmc1_dat2	MMC1_DAT2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD	1	0/1
		UART7_TXD	1	O									
		GPIO1_16	7	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
R26	mmc1_dat3	MMC1_DAT3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV5	Yes	SDIO	PU/PD	1	0/1
		UART7_RXD	1	I								1	
		GPIO1_15	7	IO								0	
T24	mmc2_dat0	MMC2_DAT0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD	1	0/1
		UART9_RTSn	1	O									
		UART0_RIn	2	I								1	
		TIMER_IO5	3	IO								0	
		UART6_TXD	4	O									
		EQEP2_B	5	I								0	
		GPIO1_26	7	IO								0	
		PRG0_IEP1_EDC_SYNC_OUT1	8	O								0	
T27	mmc2_dat1	MMC2_DAT1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD	1	0/1
		UART9_CTSn	1	I								1	
		UART0_DTRn	2	O									
		TIMER_IO4	3	IO								0	
		UART6_RXD	4	I								1	
		EQEP2_A	5	I								0	
		GPIO1_25	7	IO								0	
		PRG0_IEP1_EDC_LATCH_IN1	8	I								0	
T29	mmc2_dat2	MMC2_DAT2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD	1	0/1
		UART9_TXD	1	O									
		CPTS0_HW2TSPUSH	2	I								0	
		I2C5_SDA	4	IOD								1	
		GPIO1_24	7	IO								0	
T28	mmc2_dat3	MMC2_DAT3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV6	Yes	SDIO	PU/PD	1	0/1
		UART9_RXD	1	I								1	
		CPTS0_HW1TSPUSH	2	I								0	
		I2C5_SCL	4	IOD								1	
		GPIO1_23	7	IO								0	
P29	osc1_xi	OSC1_XI		I	OFF		1.8 V	VDDS_OSC1		HFOSC			
P27	osc1_xo	OSC1_XO		O	OFF		1.8 V	VDDS_OSC1		HFOSC			
AE17	pcie_refclk0n	PCIE_REFCLK0N		IO	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
AD16	pcie_refclk0p	PCIE_REFCLK0P		IO	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AE14	pcie_refclk1n	PCIE_REFCLK1N		IO	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
AD15	pcie_refclk1p	PCIE_REFCLK1P		IO	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
AE11	pcie_refclk2n	PCIE_REFCLK2N		IO	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
AD12	pcie_refclk2p	PCIE_REFCLK2P		IO	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
AE9	pcie_refclk3n	PCIE_REFCLK3N		IO	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
AD10	pcie_refclk3p	PCIE_REFCLK3P		IO	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
E26	pmic_power_en0	MCU_I3C0_SDAPULLEN	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		0/0
		WKUP_GPIO0_66	7	IO								0	
G23	pmic_power_en1	PMIC_POWER_EN1	0	O	OFF	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		0/0
		MCU_I3C1_SDAPULLEN	5	O									
		WKUP_GPIO0_67	7	IO								0	
J24	porz	PORz	0	I	OFF	0	1.8 V	VDDA_WKUP	Yes	FS Reset	PU/PD		
U1	porz_out	PORz_OUT	0	O	OFF	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		0/0
AA27	prg0_mdio0_mdc	PRG0_MDIO0_MDC	0	O	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD		0/1
		I2C5_SDA	2	IOD								1	
		MCAN13_RX	6	I								1	
		GPIO0_84	7	IO								0	
		GPMC0_A0	8	OZ								0	
		DSS_FSYNC2	10	O									
		MCASP2_ACLKR	12	IO									
		MCASP2_AXR5	13	IO								0	

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
Y26	prg0_mdio0_mdio	PRG0_MDIO0_MDIO	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		I2C5_SCL	2	IOD								1	
		MCAN13_TX	6	O									
		GPIO0_83	7	IO								0	
		GPMC0_A27	8	OZ								0	
		DSS_FSYNC0	10	O									
		MCASP2_AFSR	12	IO									
		MCASP2_AXR4	13	IO								0	
AF28	prg0_pru0_gpo0	PRG0_PRU0_GPO0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI0	1	I								0	
		PRG0_RGMII1_RD0	2	I								0	
		PRG0_PWM3_A0	3	IO								0	
		RGMII3_RD0	4	I								0	
		RMII3_RXD1	5	I								0	
		GPIO0_43	7	IO								0	
		MCASP0_AXR0	12	IO									
AE28	prg0_pru0_gpo1	PRG0_PRU0_GPO1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI1	1	I								0	
		PRG0_RGMII1_RD1	2	I								0	
		PRG0_PWM3_B0	3	IO								1	
		RGMII3_RD1	4	I								0	
		RMII3_RXD0	5	I								0	
		GPIO0_44	7	IO								0	
		MCASP0_AXR1	12	IO									
AE27	prg0_pru0_gpo2	PRG0_PRU0_GPO2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI2	1	I								0	
		PRG0_RGMII1_RD2	2	I								0	
		PRG0_PWM2_A0	3	IO								0	
		RGMII3_RD2	4	I								0	
		RMII3_CRS_DV	5	I								0	
		GPIO0_45	7	IO								0	
		UART3_RXD	8	I								0	
		MCASP0_ACLKR	12	IO									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AD26	prg0_pru0_gpo3	PRG0_PRU0_GPO3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI3	1	I								0	
		PRG0_RGMII1_RD3	2	I								0	
		PRG0_PWM3_A2	3	IO								0	
		RGMII3_RD3	4	I								0	
		RMII3_RX_ER	5	I								0	
		GPIO0_46	7	IO								0	
		UART3_TXD	8	O								0	
		MCASP0_AFSR	12	IO									
AD25	prg0_pru0_gpo4	PRG0_PRU0_GPO4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI4	1	I								0	
		PRG0_RGMII1_RX_CTL	2	I								0	
		PRG0_PWM2_B0	3	IO								1	
		RGMII3_RX_CTL	4	I								0	
		RMII3_TXD1	5	O									
		GPIO0_47	7	IO								0	
		MCASP0_AXR2	12	IO									
AC29	prg0_pru0_gpo5	PRG0_PRU0_GPO5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	1/1
		PRG0_PRU0_GPI5	1	I								0	
		PRG0_PWM3_B2	3	IO								1	
		RMII3_TXD0	5	O									
		GPIO0_48	7	IO								0	
		GPMC0_AD0	8	IO								0	
		MCASP0_AXR3	12	IO									
		BOOTMODE2	Bootstrap	I									
AE26	prg0_pru0_gpo6	PRG0_PRU0_GPO6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI6	1	I								0	
		PRG0_RGMII1_RXC	2	I								0	
		PRG0_PWM3_A1	3	IO								0	
		RGMII3_RXC	4	I								0	
		RMII3_TX_EN	5	O									
		GPIO0_49	7	IO								0	
		MCASP0_AXR4	12	IO									

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AC28	prg0_pru0_gpo7	PRG0_PRU0_GPO7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI7	1	I								0	
		PRG0_IEP0_EDC_LATCH_IN1	2	I								0	
		PRG0_PWM3_B1	3	IO								1	
		PRG0_ECAP0_SYNC_IN	4	I								0	
		MCAN9_TX	6	O									
		GPIO0_50	7	IO								0	
		GPMC0_AD1	8	IO								0	
		MCASP0_AXR5	12	IO									
AC27	prg0_pru0_gpo8	PRG0_PRU0_GPO8	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI8	1	I								0	
		PRG0_PWM2_A1	3	IO								0	
		MCAN9_RX	6	I								1	
		GPIO0_51	7	IO								0	
		GPMC0_AD2	8	IO								0	
		MCASP0_AXR6	12	IO									
		UART6_RXD	14	I									
AB26	prg0_pru0_gpo9	PRG0_PRU0_GPO9	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI9	1	I								0	
		PRG0_UART0_CTSn	2	I								1	
		PRG0_PWM3_TZ_IN	3	I								0	
		SPI3_CS1	4	IO								1	
		PRG0_IEP0_EDIO_DATA_IN_OUT28	5	IO								0	
		MCAN10_TX	6	O									
		GPIO0_52	7	IO								0	
		GPMC0_AD3	8	IO								0	
		MCASP0_ACLKX	12	IO									
		UART6_TXD	14	O									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AB25	prg0_pru0_gpo10	PRG0_PRU0_GPO10	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI10	1	I								0	
		PRG0_UART0_RTSn	2	O									
		PRG0_PWM2_B1	3	IO								1	
		SPI3_CS2	4	IO								1	
		PRG0_IEP0_EDIO_DATA_IN_OUT29	5	IO								0	
		MCAN10_RX	6	I								1	
		GPIO0_53	7	IO								0	
		GPMC0_AD4	8	IO								0	
		MCASP0_AFSX	12	IO									
AJ28	prg0_pru0_gpo11	PRG0_PRU0_GPO11	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI11	1	I								0	
		PRG0_RGMII1_TD0	2	O									
		PRG0_PWM3_TZ_OUT	3	O									
		RGMII3_TD0	4	O									
		GPIO0_54	7	IO								0	
		CLKOUT	9	OZ									
		MCASP0_AXR7	12	IO									
AH27	prg0_pru0_gpo12	PRG0_PRU0_GPO12	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI12	1	I								0	
		PRG0_RGMII1_TD1	2	O									
		PRG0_PWM0_A0	3	IO								0	
		RGMII3_TD1	4	O									
		GPIO0_55	7	IO								0	
		DSS_FSYNC0	10	O									
		MCASP0_AXR8	12	IO									
AH29	prg0_pru0_gpo13	PRG0_PRU0_GPO13	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI13	1	I								0	
		PRG0_RGMII1_TD2	2	O									
		PRG0_PWM0_B0	3	IO								1	
		RGMII3_TD2	4	O									
		GPIO0_56	7	IO								0	
		DSS_FSYNC2	10	O									
		MCASP0_AXR9	12	IO									

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AG28	prg0_pru0_gpo14	PRG0_PRU0_GPO14	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI14	1	I								0	
		PRG0_RGMII1_TD3	2	O									
		PRG0_PWM0_A1	3	IO								0	
		RGMII3_TD3	4	O									
		GPIO0_57	7	IO								0	
		UART4_RXD	8	I								0	
		MCASP0_AXR10	12	IO									
AG27	prg0_pru0_gpo15	PRG0_PRU0_GPO15	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI15	1	I								0	
		PRG0_RGMII1_TX_CTL	2	O									
		PRG0_PWM0_B1	3	IO								1	
		RGMII3_TX_CTL	4	O									
		GPIO0_58	7	IO								0	
		UART4_TXD	8	O								0	
		DSS_FSYNC3	10	O									
		MCASP0_AXR11	12	IO									
AH28	prg0_pru0_gpo16	PRG0_PRU0_GPO16	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI16	1	I								0	
		PRG0_RGMII1_TXC	2	IO								0	
		PRG0_PWM0_A2	3	IO								0	
		RGMII3_TXC	4	O								0	
		GPIO0_59	7	IO								0	
		DSS_FSYNC1	10	O									
		MCASP0_AXR12	12	IO									
AB24	prg0_pru0_gpo17	PRG0_PRU0_GPO17	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	1/1
		PRG0_PRU0_GPI17	1	I								0	
		PRG0_IEP0_EDC_SYNC_OUT1	2	O									
		PRG0_PWM0_B2	3	IO								1	
		PRG0_ECAP0_SYNC_OUT	4	O									
		GPIO0_60	7	IO								0	
		GPMC0_AD5	8	IO								0	
		OBSCLK1	9	O								0	
		MCASP0_AXR13	12	IO									
		BOOTMODE7	Bootstrap	I									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AB29	prg0_pru0_gpo18	PRG0_PRU0_GPO18	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI18	1	I								0	
		PRG0_IEP0_EDC_LATCH_IN0	2	I								0	
		PRG0_PWM0_TZ_IN	3	I								0	
		PRG0_ECAP0_IN_APWM_OUT	4	IO								0	
		GPIO0_61	7	IO								0	
		GPMC0_AD6	8	IO								0	
		MCASP0_AXR14	12	IO									
AB28	prg0_pru0_gpo19	PRG0_PRU0_GPO19	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU0_GPI19	1	I								0	
		PRG0_IEP0_EDC_SYNC_OUT0	2	O									
		PRG0_PWM0_TZ_OUT	3	O									
		GPIO0_62	7	IO								0	
		GPMC0_AD7	8	IO								0	
		MCASP0_AXR15	12	IO									
AE29	prg0_pru1_gpo0	PRG0_PRU1_GPO0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI0	1	I								0	
		PRG0_RGMII2_RD0	2	I								0	
		RGMII4_RD0	4	I								0	
		RMII4_RXD0	5	I								0	
		GPIO0_63	7	IO								0	
		UART4_CTSn	8	I								0	
		MCASP1_AXR0	12	IO									
		UART5_RXD	14	I									
AD28	prg0_pru1_gpo1	PRG0_PRU1_GPO1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI1	1	I								0	
		PRG0_RGMII2_RD1	2	I								0	
		RGMII4_RD1	4	I								0	
		RMII4_RXD1	5	I								0	
		GPIO0_64	7	IO								0	
		UART4_RTSn	8	O								0	
		MCASP1_AXR1	12	IO									
		UART5_TXD	14	O									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AD27	prg0_pru1_gpo2	PRG0_PRU1_GPO2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI2	1	I								0	
		PRG0_RGMII2_RD2	2	I								0	
		PRG0_PWM2_A2	3	IO								0	
		RGMII4_RD2	4	I								0	
		RMII4_CRS_DV	5	I								0	
		GPIO0_65	7	IO								0	
		GPMC0_A23	8	OZ								0	
		MCASP1_ACLKR	12	IO									
		MCASP1_AXR10	13	IO								0	
AC25	prg0_pru1_gpo3	PRG0_PRU1_GPO3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI3	1	I								0	
		PRG0_RGMII2_RD3	2	I								0	
		RGMII4_RD3	4	I								0	
		RMII4_RX_ER	5	I								0	
		GPIO0_66	7	IO								0	
		MCASP1_AFSR	12	IO									
		MCASP1_AXR11	13	IO								0	
AD29	prg0_pru1_gpo4	PRG0_PRU1_GPO4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI4	1	I								0	
		PRG0_RGMII2_RX_CTL	2	I								0	
		PRG0_PWM2_B2	3	IO								1	
		RGMII4_RX_CTL	4	I								0	
		RMII4_TXD1	5	O									
		GPIO0_67	7	IO								0	
		GPMC0_A24	8	OZ								0	
		MCASP1_AXR2	12	IO									
AB27	prg0_pru1_gpo5	PRG0_PRU1_GPO5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	1/1
		PRG0_PRU1_GPI5	1	I								0	
		GPIO0_68	7	IO								0	
		GPMC0_AD8	8	IO								0	
		MCASP1_ACLKX	12	IO									
		BOOTMODE6	Bootstrap	I									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AC26	prg0_pru1_gpo6	PRG0_PRU1_GPO6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI6	1	I								0	
		PRG0_RGMII2_RXC	2	I								0	
		RGMII4_RXC	4	I								0	
		RMII4_TXD0	5	O									
		GPIO0_69	7	IO								0	
		GPMC0_A25	8	OZ								0	
		MCASP1_AXR3	12	IO									
AA24	prg0_pru1_gpo7	PRG0_PRU1_GPO7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI7	1	I								0	
		PRG0_IEP1_EDC_LATCH_IN1	2	I								0	
		SPI3_CS0	4	IO								1	
		MCAN11_TX	6	O									
		GPIO0_70	7	IO								0	
		GPMC0_AD9	8	IO								0	
		MCASP1_AXR4	12	IO									
		UART2_TXD	14	O									
AA28	prg0_pru1_gpo8	PRG0_PRU1_GPO8	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI8	1	I								0	
		PRG0_PWM2_TZ_OUT	3	O									
		MCAN11_RX	6	I								1	
		GPIO0_71	7	IO								0	
		GPMC0_AD10	8	IO								0	
		MCASP1_AFSX	12	IO									
Y24	prg0_pru1_gpo9	PRG0_PRU1_GPO9	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI9	1	I								0	
		PRG0_UART0_RXD	2	I								1	
		SPI3_CS3	4	IO								1	
		PRG0_IEP0_EDIO_DATA_IN_OUT30	6	IO								0	
		GPIO0_72	7	IO								0	
		GPMC0_AD11	8	IO								0	
		DSS_FSYNC3	10	O									
		MCASP1_AXR5	12	IO									
		UART8_RXD	14	I									

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AA25	prg0_pru1_gpo10	PRG0_PRU1_GPO10	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI10	1	I								0	
		PRG0_UART0_TXD	2	O									
		PRG0_PWM2_TZ_IN	3	I								0	
		PRG0_IEP0_EDIO_DATA_IN_OUT31	6	IO								0	
		GPIO0_73	7	IO								0	
		GPMC0_AD12	8	IO								0	
		CLKOUT	9	OZ								0	
		MCASP1_AXR6	12	IO									
		UART8_TXD	14	O									
AG26	prg0_pru1_gpo11	PRG0_PRU1_GPO11	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI11	1	I								0	
		PRG0_RGMII2_TD0	2	O									
		RGMII4_TD0	4	O									
		RMII4_TX_EN	5	O									
		GPIO0_74	7	IO								0	
		GPMC0_A26	8	OZ								0	
		MCASP1_AXR7	12	IO									
AF27	prg0_pru1_gpo12	PRG0_PRU1_GPO12	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI12	1	I								0	
		PRG0_RGMII2_TD1	2	O									
		PRG0_PWM1_A0	3	IO								0	
		RGMII4_TD1	4	O									
		GPIO0_75	7	IO								0	
		MCASP1_AXR8	12	IO									
		UART8_CTSn	14	I									
AF26	prg0_pru1_gpo13	PRG0_PRU1_GPO13	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI13	1	I								0	
		PRG0_RGMII2_TD2	2	O									
		PRG0_PWM1_B0	3	IO								1	
		RGMII4_TD2	4	O									
		GPIO0_76	7	IO								0	
		MCASP1_AXR9	12	IO									
		UART8_RTSn	14	O									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AE25	prg0_pru1_gpo14	PRG0_PRU1_GPO14	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI14	1	I								0	
		PRG0_RGMII2_TD3	2	O									
		PRG0_PWM1_A1	3	IO								0	
		RGMII4_TD3	4	O									
		GPIO0_77	7	IO								0	
		MCASP2_AXR0	12	IO									
		UART2_CTSn	14	I									
AF29	prg0_pru1_gpo15	PRG0_PRU1_GPO15	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI15	1	I								0	
		PRG0_RGMII2_TX_CTL	2	O									
		PRG0_PWM1_B1	3	IO								1	
		RGMII4_TX_CTL	4	O									
		GPIO0_78	7	IO								0	
		MCASP2_AXR1	12	IO									
		UART2_RTSn	14	O									
AG29	prg0_pru1_gpo16	PRG0_PRU1_GPO16	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI16	1	I								0	
		PRG0_RGMII2_TXC	2	IO								0	
		PRG0_PWM1_A2	3	IO								0	
		RGMII4_TXC	4	O								0	
		GPIO0_79	7	IO								0	
		MCASP2_AXR2	12	IO									
Y25	prg0_pru1_gpo17	PRG0_PRU1_GPO17	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	1/1
		PRG0_PRU1_GPI17	1	I								0	
		PRG0_IEP1_EDC_SYNC_OUT1	2	O									
		PRG0_PWM1_B2	3	IO								1	
		SPI3_CLK	4	IO								0	
		GPIO0_80	7	IO								0	
		GPMC0_AD13	8	IO								0	
		MCASP2_AXR3	12	IO									
		BOOTMODE3	Bootstrap	I									

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AA26	prg0_pru1_gpo18	PRG0_PRU1_GPO18	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI18	1	I								0	
		PRG0_IEP1_EDC_LATCH_IN0	2	I								0	
		PRG0_PWM1_TZ_IN	3	I								0	
		SPI3_D0	4	IO								0	
		MCAN12_TX	6	O									
		GPIO0_81	7	IO								0	
		GPMC0_AD14	8	IO								0	
		MCASP2_AFSX	12	IO									
		UART2_RXD	14	I									
AA29	prg0_pru1_gpo19	PRG0_PRU1_GPO19	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV1	Yes	LVCMOS	PU/PD	0	0/1
		PRG0_PRU1_GPI19	1	I								0	
		PRG0_IEP1_EDC_SYNC_OUT0	2	O									
		PRG0_PWM1_TZ_OUT	3	O									
		SPI3_D1	4	IO								0	
		MCAN12_RX	6	I								1	
		GPIO0_82	7	IO								0	
		GPMC0_AD15	8	IO								0	
		MCASP2_ACLKX	12	IO									
AD18	prg1_mdio0_mdc	PRG1_MDIO0_MDC	0	O	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD		0/1
		SPI1_CS3	1	IO								1	
		I2C4_SDA	2	IOD								1	
		RMII_REF_CLK	5	I								0	
		GPIO0_42	7	IO								0	
		VPFE0_DATA12	11	I									
		MCASP5_AXR3	12	IO								0	
		MCASP5_AFSR	13	IO								0	
		UART3_RTSn	14	O								0	
AD19	prg1_mdio0_mdio	PRG1_MDIO0_MDIO	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		SPI1_CS2	1	IO								1	
		I2C4_SCL	2	IOD								1	
		GPIO0_41	7	IO								0	
		DSS_FSYNC1	10	O									
		VPFE0_DATA11	11	I									
		MCASP5_AXR2	12	IO								0	
		MCASP5_ACLKR	13	IO								0	
		UART3_CTSn	14	I								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AC23	prg1_pru0_gpo0	PRG1_PRU0_GPO0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI0	1	I								0	
		PRG1_RGMII1_RD0	2	I								0	
		PRG1_PWM3_A0	3	IO								0	
		RGMII1_RD0	4	I								0	
		RMII1_RXD0	5	I								0	
		GPIO0_1	7	IO								0	
		GPMC0_BE1n	8	O								0	
		RGMII7_RD0	9	I									
		MCASP6_ACLKX	12	IO									
		UART0_RXD	14	I									
AG22	prg1_pru0_gpo1	PRG1_PRU0_GPO1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI1	1	I								0	
		PRG1_RGMII1_RD1	2	I								0	
		PRG1_PWM3_B0	3	IO								1	
		RGMII1_RD1	4	I								0	
		RMII1_RXD1	5	I								0	
		GPIO0_2	7	IO								0	
		GPMC0_WAIT0	8	I								0	
		RGMII7_RD1	9	I								0	
		MCASP6_AFSX	12	IO									
		UART0_TXD	14	O									
AF22	prg1_pru0_gpo2	PRG1_PRU0_GPO2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI2	1	I								0	
		PRG1_RGMII1_RD2	2	I								0	
		PRG1_PWM2_A0	3	IO								0	
		RGMII1_RD2	4	I								0	
		RMII1_CRS_DV	5	I								0	
		GPIO0_3	7	IO								0	
		GPMC0_WAIT1	8	I								0	
		RGMII7_RD2	9	I								0	
		MCASP6_AXR0	12	IO									
		UART1_RXD	14	I									

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AJ23	prg1_pru0_gpo3	PRG1_PRU0_GPO3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI3	1	I								0	
		PRG1_RGMII1_RD3	2	I								0	
		PRG1_PWM3_A2	3	IO								0	
		RGMII1_RD3	4	I								0	
		RMII1_RX_ER	5	I								0	
		GPIO0_4	7	IO								0	
		GPMC0_DIR	8	O								0	
		RGMII7_RD3	9	I									
		MCASP6_AXR1	12	IO									
		UART1_TXD	14	O									
AH23	prg1_pru0_gpo4	PRG1_PRU0_GPO4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI4	1	I								0	
		PRG1_RGMII1_RX_CTL	2	I								0	
		PRG1_PWM2_B0	3	IO								1	
		RGMII1_RX_CTL	4	I								0	
		RMII1_TXD0	5	O									
		GPIO0_5	7	IO								0	
		GPMC0_CSn2	8	O								0	
		RGMII7_RX_CTL	9	I									
		MCASP6_AXR2	12	IO									
		MCASP6_ACLKR	13	IO								0	
		UART2_RXD	14	I								0	
AD20	prg1_pru0_gpo5	PRG1_PRU0_GPO5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1
		PRG1_PRU0_GPI5	1	I								0	
		PRG1_PWM3_B2	3	IO								1	
		RMII1_TX_EN	5	O									
		GPIO0_6	7	IO								0	
		GPMC0_WEn	8	O								0	
		MCASP3_AXR0	12	IO									
		BOOTMODE0	Bootstrap	I									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AD22	prg1_pru0_gpo6	PRG1_PRU0_GPO6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI6	1	I								0	
		PRG1_RGMII1_RXC	2	I								0	
		PRG1_PWM3_A1	3	IO								0	
		RGMII1_RXC	4	I								0	
		RMII1_TXD1	5	O									
		AUDIO_EXT_REFCLK0	6	IO								0	
		GPIO0_7	7	IO								0	
		GPMC0_CSn3	8	O								0	
		RGMII7_RXC	9	I									
		MCASP6_AXR3	12	IO									
		MCASP6_AFSR	13	IO								0	
		UART2_TXD	14	O								0	
AE20	prg1_pru0_gpo7	PRG1_PRU0_GPO7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI7	1	I								0	
		PRG1_IEP0_EDC_LATCH_IN1	2	I								0	
		PRG1_PWM3_B1	3	IO								1	
		AUDIO_EXT_REFCLK1	5	IO								0	
		MCAN4_TX	6	O									
		GPIO0_8	7	IO								0	
		MCASP3_AXR1	12	IO									
AJ20	prg1_pru0_gpo8	PRG1_PRU0_GPO8	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI8	1	I								0	
		PRG1_PWM2_A1	3	IO								0	
		RMII5_RXD0	5	I								0	
		MCAN4_RX	6	I								1	
		GPIO0_9	7	IO								0	
		GPMC0_OEn_REn	8	O								0	
		VOUT0_DATA22	10	O									
		MCASP3_AXR2	12	IO									

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AG20	prg1_pru0_gpo9	PRG1_PRU0_GPO9	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI9	1	I								0	
		PRG1_UART0_CTSn	2	I								1	
		PRG1_PWM3_TZ_IN	3	I								0	
		SPI6_CS1	4	IO								1	
		RMII5_RXD1	5	I								0	
		GPIO0_10	7	IO								0	
		GPMC0_ADVn_ALE	8	O								0	
		PRG1_IEP0_EDIO_DATA_IN_OUT28	9	IO									
		VOUT0_DATA23	10	O								0	
		MCASP3_ACLKX	12	IO									
AD21	prg1_pru0_gpo10	PRG1_PRU0_GPO10	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI10	1	I								0	
		PRG1_UART0_RTSn	2	O									
		PRG1_PWM2_B1	3	IO								1	
		SPI6_CS2	4	IO								1	
		RMII5_CRS_DV	5	I								0	
		GPIO0_11	7	IO								0	
		GPMC0_BE0n_CLE	8	O								0	
		PRG1_IEP0_EDIO_DATA_IN_OUT29	9	IO									
		OBSCLK2	10	O								0	
		MCASP3_AFSX	12	IO									
AF24	prg1_pru0_gpo11	PRG1_PRU0_GPO11	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI11	1	I								0	
		PRG1_RGMII1_TD0	2	O									
		PRG1_PWM3_TZ_OUT	3	O									
		RGMII1_TD0	4	O									
		MCAN4_TX	6	O									
		GPIO0_12	7	IO								0	
		RGMII7_TD0	9	O									
		VOUT0_DATA16	10	O									
		VPFE0_DATA0	11	I									
		MCASP7_ACLKX	12	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AJ24	prg1_pru0_gpo12	PRG1_PRU0_GPO12	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI12	1	I								0	
		PRG1_RGMII1_TD1	2	O									
		PRG1_PWM0_A0	3	IO								0	
		RGMII1_TD1	4	O									
		MCAN4_RX	6	I								1	
		GPIO0_13	7	IO								0	
		RGMII7_TD1	9	O									
		VOUT0_DATA17	10	O									
		VPFE0_DATA1	11	I									
		MCASP7_AFSX	12	IO								0	
AG24	prg1_pru0_gpo13	PRG1_PRU0_GPO13	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI13	1	I								0	
		PRG1_RGMII1_TD2	2	O									
		PRG1_PWM0_B0	3	IO								1	
		RGMII1_TD2	4	O									
		MCAN5_TX	6	O									
		GPIO0_14	7	IO								0	
		RGMII7_TD2	9	O									
		VOUT0_DATA18	10	O									
		VPFE0_DATA2	11	I									
		MCASP7_AXR0	12	IO								0	
AD24	prg1_pru0_gpo14	PRG1_PRU0_GPO14	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI14	1	I								0	
		PRG1_RGMII1_TD3	2	O									
		PRG1_PWM0_A1	3	IO								0	
		RGMII1_TD3	4	O									
		MCAN5_RX	6	I								1	
		GPIO0_15	7	IO								0	
		RGMII7_TD3	9	O									
		VOUT0_DATA19	10	O									
		VPFE0_DATA3	11	I									
		MCASP7_AXR1	12	IO								0	

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AC24	prg1_pru0_gpo15	PRG1_PRU0_GPO15	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI15	1	I								0	
		PRG1_RGMII1_TX_CTL	2	O									
		PRG1_PWM0_B1	3	IO								1	
		RGMII1_TX_CTL	4	O									
		MCAN6_TX	6	O									
		GPIO0_16	7	IO								0	
		RGMII7_TX_CTL	9	O									
		VOUT0_DATA20	10	O									
		VPFE0_DATA4	11	I									
		MCASP7_AXR2	12	IO								0	
		MCASP7_ACLKR	13	IO								0	
AE24	prg1_pru0_gpo16	PRG1_PRU0_GPO16	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI16	1	I								0	
		PRG1_RGMII1_TXC	2	IO								0	
		PRG1_PWM0_A2	3	IO								0	
		RGMII1_TXC	4	O								0	
		MCAN6_RX	6	I								1	
		GPIO0_17	7	IO								0	
		RGMII7_TXC	9	O									
		VOUT0_DATA21	10	O								0	
		VPFE0_DATA5	11	I									
		MCASP7_AXR3	12	IO								0	
		MCASP7_AFSR	13	IO								0	
AJ21	prg1_pru0_gpo17	PRG1_PRU0_GPO17	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI17	1	I								0	
		PRG1_IEP0_EDC_SYNC_OUT1	2	O									
		PRG1_PWM0_B2	3	IO								1	
		RMII5_TXD1	5	O									
		MCAN5_TX	6	O									
		GPIO0_18	7	IO								0	
		VPFE0_DATA6	11	I									
		MCASP3_AXR3	12	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AE21	prg1_pru0_gpo18	PRG1_PRU0_GPO18	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI18	1	I								0	
		PRG1_IEP0_EDC_LATCH_IN0	2	I								0	
		PRG1_PWM0_TZ_IN	3	I								0	
		RMII5_RX_ER	5	I								0	
		MCAN5_RX	6	I								1	
		GPIO0_19	7	IO								0	
		VPFE0_DATA7	11	I									
		MCASP4_ACLKX	12	IO								0	
AH21	prg1_pru0_gpo19	PRG1_PRU0_GPO19	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU0_GPI19	1	I								0	
		PRG1_IEP0_EDC_SYNC_OUT0	2	O									
		PRG1_PWM0_TZ_OUT	3	O									
		RMII5_TXD0	5	O									
		MCAN6_TX	6	O									
		GPIO0_20	7	IO								0	
		VOUT0_EXTPCLKIN	10	I									
		VPFE0_PCLK	11	I								0	
		MCASP4_AFSX	12	IO								0	
AE22	prg1_pru1_gpo0	PRG1_PRU1_GPO0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI0	1	I								0	
		PRG1_RGMII2_RD0	2	I								0	
		RGMII2_RD0	4	I								0	
		RMII2_RXD0	5	I								0	
		GPIO0_21	7	IO								0	
		RGMII8_RD0	8	I								0	
		VOUT0_DATA0	10	O									
		VPFE0_HD	11	I									
		MCASP8_ACLKX	12	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AG23	prg1_pru1_gpo1	PRG1_PRU1_GPO1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI1	1	I								0	
		PRG1_RGMII2_RD1	2	I								0	
		RGMII2_RD1	4	I								0	
		RMII2_RXD1	5	I								0	
		GPIO0_22	7	IO								0	
		RGMII8_RD1	8	I								0	
		VOUT0_DATA1	10	O									
		VPFE0_FIELD	11	I									
		MCASP8_AFSX	12	IO								0	
AF23	prg1_pru1_gpo2	PRG1_PRU1_GPO2	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI2	1	I								0	
		PRG1_RGMII2_RD2	2	I								0	
		PRG1_PWM2_A2	3	IO								0	
		RGMII2_RD2	4	I								0	
		RMII2_CRS_DV	5	I								0	
		GPIO0_23	7	IO								0	
		RGMII8_RD2	8	I								0	
		VOUT0_DATA2	10	O									
		VPFE0_VD	11	I									
		MCASP8_AXR0	12	IO								0	
		MCASP3_ACLKR	13	IO								0	
AD23	prg1_pru1_gpo3	PRG1_PRU1_GPO3	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI3	1	I								0	
		PRG1_RGMII2_RD3	2	I								0	
		RGMII2_RD3	4	I								0	
		RMII2_RX_ER	5	I								0	
		GPIO0_24	7	IO								0	
		RGMII8_RD3	8	I								0	
		EQEP1_A	9	I								0	
		VOUT0_DATA3	10	O								0	
		VPFE0_WEN	11	I									
		MCASP8_AXR1	12	IO								0	
		MCASP3_AFSR	13	IO								0	
		TIMER_IO2	14	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AH24	prg1_pru1_gpo4	PRG1_PRU1_GPO4	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI4	1	I								0	
		PRG1_RGMII2_RX_CTL	2	I								0	
		PRG1_PWM2_B2	3	IO								1	
		RGMII2_RX_CTL	4	I								0	
		RMII2_TXD0	5	O									
		GPIO0_25	7	IO								0	
		RGMII8_RX_CTL	8	I								0	
		EQEP1_B	9	I								0	
		VOUT0_DATA4	10	O								0	
		VPFE0_DATA13	11	I									
		MCASP8_AXR2	12	IO								0	
		MCASP8_ACLKR	13	IO								0	
		TIMER_IO3	14	IO								0	
AG21	prg1_pru1_gpo5	PRG1_PRU1_GPO5	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI5	1	I								0	
		RMII5_TX_EN	5	O									
		MCAN6_RX	6	I								1	
		GPIO0_26	7	IO								0	
		GPMC0_WPn	8	O								0	
		EQEP1_S	9	IO									
		VOUT0_DATA5	10	O								0	
		MCASP4_AXR0	12	IO									
		TIMER_IO4	14	IO									
AE23	prg1_pru1_gpo6	PRG1_PRU1_GPO6	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI6	1	I								0	
		PRG1_RGMII2_RXC	2	I								0	
		RGMII2_RXC	4	I								0	
		RMII2_TXD1	5	O									
		GPIO0_27	7	IO								0	
		RGMII8_RXC	8	I								0	
		VOUT0_DATA6	10	O									
		VPFE0_DATA14	11	I									
		MCASP8_AXR3	12	IO								0	
		MCASP8_AFSR	13	IO								0	
		TIMER_IO5	14	IO								0	

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AC21	prg1_pru1_gpo7	PRG1_PRU1_GPO7	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI7	1	I								0	
		PRG1_IEP1_EDC_LATCH_IN1	2	I								0	
		SPI6_CS0	4	IO								1	
		RMII6_RX_ER	5	I								0	
		MCAN7_TX	6	O									
		GPIO0_28	7	IO								0	
		VOUT0_DATA7	10	O									
		VPFE0_DATA15	11	I									
		MCASP4_AXR1	12	IO								0	
		UART3_TXD	14	O									
Y23	prg1_pru1_gpo8	PRG1_PRU1_GPO8	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI8	1	I								0	
		PRG1_PWM2_TZ_OUT	3	O									
		RMII6_RXD0	5	I								0	
		MCAN7_RX	6	I								1	
		GPIO0_29	7	IO								0	
		GPMC0_CSn1	8	O								0	
		VOUT0_DATA8	10	O									
		MCASP4_AXR2	12	IO									
		UART3_RXD	14	I									
AF21	prg1_pru1_gpo9	PRG1_PRU1_GPO9	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI9	1	I								0	
		PRG1_UART0_RXD	2	I								1	
		SPI6_CS3	4	IO								1	
		RMII6_RXD1	5	I								0	
		MCAN8_TX	6	O									
		GPIO0_30	7	IO								0	
		GPMC0_CSn0	8	O								0	
		PRG1_IEP0_EDIO_DATA_IN_OUT30	9	IO									
		VOUT0_DATA9	10	O								0	
		MCASP4_AXR3	12	IO									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AB23	prg1_pru1_gpo10	PRG1_PRU1_GPO10	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI10	1	I								0	
		PRG1_UART0_TXD	2	O									
		PRG1_PWM2_TZ_IN	3	I								0	
		RMII6_CRS_DV	5	I								0	
		MCAN8_RX	6	I								1	
		GPIO0_31	7	IO								0	
		GPMC0_CLKOUT	8	O								0	
		PRG1_IEP0_EDIO_DATA_IN_OUT31	9	IO									
		VOUT0_DATA10	10	O								0	
		GPMC0_FCLK_MUX	11	O									
		MCASP5_ACLKX	12	IO									
AJ25	prg1_pru1_gpo11	PRG1_PRU1_GPO11	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI11	1	I								0	
		PRG1_RGMII2_TD0	2	O									
		RGMII2_TD0	4	O									
		RMII2_TX_EN	5	O									
		GPIO0_32	7	IO								0	
		RGMII8_TD0	8	O								0	
		EQEP1_I	9	IO									
		VOUT0_DATA11	10	O								0	
		MCASP9_ACLKX	12	IO									
AH25	prg1_pru1_gpo12	PRG1_PRU1_GPO12	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI12	1	I								0	
		PRG1_RGMII2_TD1	2	O									
		PRG1_PWM1_A0	3	IO								0	
		RGMII2_TD1	4	O									
		MCAN7_TX	6	O									
		GPIO0_33	7	IO								0	
		RGMII8_TD1	8	O								0	
		VOUT0_DATA12	10	O									
		MCASP9_AFSX	12	IO									

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AG25	prg1_pru1_gpo13	PRG1_PRU1_GPO13	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI13	1	I								0	
		PRG1_RGMII2_TD2	2	O									
		PRG1_PWM1_B0	3	IO								1	
		RGMII2_TD2	4	O									
		MCAN7_RX	6	I								1	
		GPIO0_34	7	IO								0	
		RGMII8_TD2	8	O								0	
		VOUT0_DATA13	10	O									
		VPFE0_DATA8	11	I									
		MCASP9_AXR0	12	IO								0	
		MCASP4_ACLKR	13	IO								0	
AH26	prg1_pru1_gpo14	PRG1_PRU1_GPO14	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI14	1	I								0	
		PRG1_RGMII2_TD3	2	O									
		PRG1_PWM1_A1	3	IO								0	
		RGMII2_TD3	4	O									
		MCAN8_TX	6	O									
		GPIO0_35	7	IO								0	
		RGMII8_TD3	8	O								0	
		VOUT0_DATA14	10	O									
		MCASP9_AXR1	12	IO									
		MCASP4_AFSR	13	IO								0	
AJ27	prg1_pru1_gpo15	PRG1_PRU1_GPO15	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI15	1	I								0	
		PRG1_RGMII2_TX_CTL	2	O									
		PRG1_PWM1_B1	3	IO								1	
		RGMII2_TX_CTL	4	O									
		MCAN8_RX	6	I								1	
		GPIO0_36	7	IO								0	
		RGMII8_TX_CTL	8	O								0	
		VOUT0_DATA15	10	O									
		VPFE0_DATA9	11	I									
		MCASP9_AXR2	12	IO								0	
		MCASP9_ACLKR	13	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AJ26	prg1_pru1_gpo16	PRG1_PRU1_GPO16	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI16	1	I								0	
		PRG1_RGMII2_TXC	2	IO								0	
		PRG1_PWM1_A2	3	IO								0	
		RGMII2_TXC	4	O								0	
		GPIO0_37	7	IO								0	
		RGMII8_TXC	8	O								0	
		VOUT0_VP2_HSYNC	9	O								0	
		VOUT0_HSYNC	10	O									
		MCASP9_AXR3	12	IO									
		MCASP9_AFSR	13	IO								0	
		VOUT0_VP0_HSYNC	14	O								0	
AC22	prg1_pru1_gpo17	PRG1_PRU1_GPO17	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	1/1
		PRG1_PRU1_GPI17	1	I								0	
		PRG1_IEP1_EDC_SYNC_OUT1	2	O									
		PRG1_PWM1_B2	3	IO								1	
		SPI6_CLK	4	IO								0	
		RMII6_TX_EN	5	O									
		PRG1_ECAP0_SYNC_OUT	6	O									
		GPIO0_38	7	IO								0	
		VOUT0_VP2_DE	9	O									
		VOUT0_DE	10	O									
		VPFE0_DATA10	11	I									
		MCASP5_AFSX	12	IO								0	
		VOUT0_VP0_DE	14	O									
		BOOTMODE1	Bootstrap	I									

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AJ22	prg1_pru1_gpo18	PRG1_PRU1_GPO18	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI18	1	I								0	
		PRG1_IEP1_EDC_LATCH_IN0	2	I								0	
		PRG1_PWM1_TZ_IN	3	I								0	
		SPI6_D0	4	IO								0	
		RMII6_TXD0	5	O									
		PRG1_ECAP0_SYNC_IN	6	I								0	
		GPIO0_39	7	IO								0	
		VOUT0_VP2_VSYNC	9	O									
		VOUT0_VSYNC	10	O									
		MCASP5_AXR0	12	IO									
		VOUT0_VP0_VSYNC	14	O									
AH22	prg1_pru1_gpo19	PRG1_PRU1_GPO19	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV2	Yes	LVCMOS	PU/PD	0	0/1
		PRG1_PRU1_GPI19	1	I								0	
		PRG1_IEP1_EDC_SYNC_OUT0	2	O									
		PRG1_PWM1_TZ_OUT	3	O									
		SPI6_D1	4	IO								0	
		RMII6_TXD1	5	O									
		PRG1_ECAP0_IN_APWM_OUT	6	IO								0	
		GPIO0_40	7	IO								0	
		VOUT0_PCLK	10	O									
		MCASP5_AXR1	12	IO									
T6	resetstatz	RESETSTATz	0	O	OFF	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		0/0
C28	RESET_REQZ	RESET_REQz	0	I	PU	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		1/1
U25	rgmii5_rxc	RGMII5_RXC	0	I	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1
		I2C6_SDA	2	IOD								1	
		VOUT1_DATA7	4	O									
		TRC_DATA5	5	O									
		EHRPWM_TZn_IN1	6	I								0	
		GPIO0_92	7	IO								0	
		GPMC0_A8	8	OZ								0	
		MCASP10_AXR3	12	IO									
		EHRPWM_SOCA	14	O									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
U26	rgmii5_rx_ctl	RGMII5_RX_CTL	0	I	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1
		RMII7_RX_ER	1	I								0	
		I2C2_SDA	2	IOD								1	
		VOUT1_DATA1	4	O									
		TRC_CTL	5	O									
		EHRPWM0_SYNCO	6	O									
		GPIO0_86	7	IO								0	
		GPMC0_A2	8	OZ								0	
		MCASP10_AFSX	12	IO									
U29	rgmii5_txc	RGMII5_TXC	0	O	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1
		RMII7_TX_EN	1	O									
		I2C6_SCL	2	IOD								1	
		VOUT1_DATA6	4	O									
		TRC_DATA4	5	O									
		EHRPWM1_B	6	IO								0	
		GPIO0_91	7	IO								0	
		GPMC0_A7	8	OZ								0	
		MCASP10_AXR2	12	IO									
U23	rgmii5_tx_ctl	RGMII5_TX_CTL	0	O	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD		0/1
		RMII7_CRS_DV	1	I								0	
		I2C2_SCL	2	IOD								1	
		VOUT1_DATA0	4	O									
		TRC_CLK	5	O									
		EHRPWM0_SYNCI	6	I								0	
		GPIO0_85	7	IO								0	
		GPMC0_A1	8	OZ								0	
		MCASP10_ACLKX	12	IO									
W26	rgmii6_rxc	RGMII6_RXC	0	I	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1
		AUDIO_EXT_REFCLK2	3	IO								0	
		VOUT1_DE	4	O									
		TRC_DATA17	5	O									
		EHRPWM4_B	6	IO								0	
		GPIO0_104	7	IO								0	
		GPMC0_A20	8	OZ								0	
		VOUT1_VP0_DE	9	O									
		MCASP10_AXR7	12	IO									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
V23	rgmii6_rx_ctl	RGMII6_RX_CTL	0	I	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1
		RMII8_RX_ER	1	I								0	
		VOUT1_DATA13	4	O									
		TRC_DATA11	5	O									
		EHRPWM3_A	6	IO								0	
		GPIO0_98	7	IO								0	
		GPMC0_A14	8	OZ								0	
		MCASP10_AFSR	12	IO									
W29	rgmii6_txc	RGMII6_TXC	0	O	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1
		RMII8_TX_EN	1	O									
		SPI5_CLK	3	IO								0	
		VOUT1_PCLK	4	O									
		TRC_DATA16	5	O									
		EHRPWM4_A	6	IO								0	
		GPIO0_103	7	IO								0	
		GPMC0_A19	8	OZ								0	
		MCASP10_AXR6	12	IO									
Y28	rgmii6_tx_ctl	RGMII6_TX_CTL	0	O	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD		0/1
		RMII8_CRS_DV	1	I								0	
		VOUT1_DATA12	4	O									
		TRC_DATA10	5	O									
		GPIO0_97	7	IO								0	
		GPMC0_A13	8	OZ								0	
		MCASP10_ACLKR	12	IO									
T23	rgmii5_rd0	RGMII5_RD0	0	I	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1
		RMII7_RXD0	1	I								0	
		UART6_RTSn	3	O									
		VOUT1_DATA11	4	O									
		TRC_DATA9	5	O									
		GPIO0_96	7	IO								0	
		GPMC0_A12	8	OZ								0	
		MCASP11_AXR3	12	IO									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
R23	rgmii5_rd1	RGMII5_RD1	0	I	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1
		RMII7_RXD1	1	I								0	
		UART6_CTSn	3	I								1	
		VOUT1_DATA10	4	O									
		TRC_DATA8	5	O									
		EHRPWM_TZn_IN2	6	I								0	
		GPIO0_95	7	IO								0	
		GPMC0_A11	8	OZ								0	
		MCASP11_AXR2	12	IO									
		EHRPWM_SOCB	14	O									
U24	rgmii5_rd2	RGMII5_RD2	0	I	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1
		UART3_RTSn	1	O									
		UART6_TXD	3	O									
		VOUT1_DATA9	4	O									
		TRC_DATA7	5	O									
		EHRPWM2_B	6	IO								0	
		GPIO0_94	7	IO								0	
		GPMC0_A10	8	OZ								0	
		MCASP11_AXR1	12	IO									
U27	rgmii5_rd3	RGMII5_RD3	0	I	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD	0	0/1
		UART3_CTSn	1	I								1	
		UART6_RXD	3	I								1	
		VOUT1_DATA8	4	O									
		TRC_DATA6	5	O									
		EHRPWM2_A	6	IO								0	
		GPIO0_93	7	IO								0	
		GPMC0_A9	8	OZ								0	
		MCASP11_AXR0	12	IO									
U28	rgmii5_td0	RGMII5_TD0	0	O	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD		0/1
		RMII7_TXD0	1	O									
		I2C3_SDA	2	IOD								1	
		VOUT1_DATA5	4	O									
		TRC_DATA3	5	O									
		EHRPWM1_A	6	IO								0	
		GPIO0_90	7	IO								0	
		GPMC0_A6	8	OZ								0	
		MCASP11_AFSX	12	IO									

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
V27	rgmii5_td1	RGMII5_TD1	0	O	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD		0/1
		RMII7_TXD1	1	O									
		I2C3_SCL	2	IOD								1	
		VOUT1_DATA4	4	O									
		TRC_DATA2	5	O									
		EHRPWM0_B	6	IO								0	
		GPIO0_89	7	IO								0	
		GPMC0_A5	8	OZ								0	
		MCASP11_ACLKX	12	IO									
V29	rgmii5_td2	RGMII5_TD2	0	O	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD		0/1
		UART3_TXD	1	O									
		SYNC3_OUT	3	O									
		VOUT1_DATA3	4	O									
		TRC_DATA1	5	O									
		EHRPWM0_A	6	IO								0	
		GPIO0_88	7	IO								0	
		GPMC0_A4	8	OZ								0	
		MCASP10_AXR1	12	IO									
V28	rgmii5_td3	RGMII5_TD3	0	O	OFF	7	1.8 V/3.3 V	VDDSHV3	Yes	LVCMOS	PU/PD		0/1
		UART3_RXD	1	I								1	
		SYNC2_OUT	3	O									
		VOUT1_DATA2	4	O									
		TRC_DATA0	5	O									
		EHRPWM_TZn_IN0	6	I								0	
		GPIO0_87	7	IO								0	
		GPMC0_A3	8	OZ								0	
		MCASP10_AXR0	12	IO									
W25	rgmii6_rd0	RGMII6_RD0	0	I	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1
		RMII8_RXD0	1	I								0	
		SPI5_CS1	3	IO								1	
		AUDIO_EXT_REFCLK3	4	IO								0	
		TRC_DATA21	5	O									
		EHRPWM_TZn_IN5	6	I								0	
		GPIO0_108	7	IO								0	
		GPMC0_DIR	8	O								0	
		MCASP11_AXR7	12	IO									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
W24	rgmii6_rd1	RGMII6_RD1	0	I	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1
		RMII8_RXD1	1	I								0	
		SPI5_D1	3	IO								0	
		VOUT1_EXTPCLKIN	4	I								0	
		TRC_DATA20	5	O									
		EHRPWM5_B	6	IO								0	
		GPIO0_107	7	IO								0	
		GPMC0_BE1n	8	O								0	
		MCASP11_AXR6	12	IO									
Y27	rgmii6_rd2	RGMII6_RD2	0	I	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1
		UART4_RTSn	1	O									
		UART5_TXD	3	O									
		TRC_DATA19	5	O									
		EHRPWM5_A	6	IO								0	
		GPIO0_106	7	IO								0	
		GPMC0_A22	8	OZ								0	
		MCASP11_AXR5	12	IO									
Y29	rgmii6_rd3	RGMII6_RD3	0	I	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD	0	0/1
		UART4_CTSn	1	I								1	
		UART5_RXD	3	I								1	
		CLKOUT	4	OZ									
		TRC_DATA18	5	O									
		EHRPWM_TZn_IN4	6	I								0	
		GPIO0_105	7	IO								0	
		GPMC0_A21	8	OZ								0	
		MCASP11_AXR4	12	IO									
W27	rgmii6_td0	RGMII6_TD0	0	O	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD		0/1
		RMII8_TXD0	1	O									
		SPI5_CS0	3	IO								1	
		VOUT1_HSYNC	4	O									
		TRC_DATA15	5	O									
		EHRPWM_TZn_IN3	6	I								0	
		GPIO0_102	7	IO								0	
		GPMC0_A18	8	OZ								0	
		VOUT1_VP0_HSYNC	9	O									
		MCASP10_AXR5	12	IO									

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
V25	rgmii6_td1	RGMII6_TD1	0	O	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD		0/1
		RMII8_TXD1	1	O									
		SPI5_D0	3	IO								0	
		VOUT1_VSYNC	4	O									
		TRC_DATA14	5	O									
		EHRPWM3_SYNCO	6	O									
		GPIO0_101	7	IO								0	
		GPMC0_A17	8	OZ								0	
		VOUT1_VP0_VSYNC	9	O									
		MCASP10_AXR4	12	IO									
W28	rgmii6_td2	RGMII6_TD2	0	O	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD		0/1
		UART4_TXD	1	O									
		SPI5_CS2	3	IO								1	
		VOUT1_DATA15	4	O									
		TRC_DATA13	5	O									
		EHRPWM3_SYNCI	6	I								0	
		GPIO0_100	7	IO								0	
		GPMC0_A16	8	OZ								0	
		MCASP11_AFSR	12	IO									
W23	rgmii6_td3	RGMII6_TD3	0	O	OFF	7	1.8 V/3.3 V	VDDSHV4	Yes	LVCMOS	PU/PD		0/1
		UART4_RXD	1	I								1	
		SPI5_CS3	3	IO								1	
		VOUT1_DATA14	4	O									
		TRC_DATA12	5	O									
		EHRPWM3_B	6	IO								0	
		GPIO0_99	7	IO								0	
		GPMC0_A15	8	OZ								0	
		MCASP11_ACLKR	12	IO									
E7	SERDES4_REFCLK_N	SERDES4_REFCLK_N		IO	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
AE18	serdes0_rext	SERDES0_REXT		A	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
AE13	serdes1_rext	SERDES1_REXT		A	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AD13	serdes2_rext	SERDES2_REXT		A	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
F9	serdes4_rext	SERDES4_REXT		I	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
E8	SERDES4_REFCLK_P	SERDES4_REFCLK_P		IO	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
AE8	serdes3_rext	SERDES3_REXT		A	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
AH19	SERDES0_RX0_N	SERDES0_RX0_N		I	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII1_RXN0											
		PCIE0_RXN0											
		USB0_SSRX2N											
AJ18	SERDES0_RX0_P	SERDES0_RX0_P		I	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII1_RXP0											
		PCIE0_RXP0											
		USB0_SSRX2P											
AH18	SERDES0_RX1_N	SERDES0_RX1_N		I	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII2_RXN0											
		PCIE0_RXN1											
		USB0_SSRX1N											
AJ17	SERDES0_RX1_P	SERDES0_RX1_P		I	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII2_RXP0											
		PCIE0_RXP1											
		USB0_SSRX1P											
AF19	SERDES0_TX0_N	SERDES0_TX0_N		O	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII1_TXN0											
		PCIE0_TXN0											
		USB0_SSTX2N											
AG18	SERDES0_TX0_P	SERDES0_TX0_P		O	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII1_TXP0											
		PCIE0_TXP0											
		USB0_SSTX2P											

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AF18	SERDES0_TX1_N	SERDES0_TX1_N		O	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII2_TXN0											
		PCIE0_TXN1											
		USB0_SSTX1N											
AG17	SERDES0_TX1_P	SERDES0_TX1_P		O	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII2_TXP0											
		PCIE0_TXP1											
		USB0_SSTX1P											
AH15	SERDES1_RX0_N	SERDES1_RX0_N		I	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII3_RXN0											
		PCIE1_RXN0											
		USB1_SSRX2N											
		PRG1_SGMII0_RXN0											
AJ14	SERDES1_RX0_P	SERDES1_RX0_P		I	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII3_RXP0											
		PCIE1_RXP0											
		USB1_SSRX2P											
		PRG1_SGMII0_RXP0											
AH16	SERDES1_RX1_N	SERDES1_RX1_N		I	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII4_RXN0											
		PCIE1_RXN1											
		USB1_SSRX1N											
		PRG1_SGMII1_RXN0											
AJ15	SERDES1_RX1_P	SERDES1_RX1_P		I	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII4_RXP0											
		PCIE1_RXP1											
		USB1_SSRX1P											
		PRG1_SGMII1_RXP0											
AF15	SERDES1_TX0_N	SERDES1_TX0_N		O	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII3_TXN0											
		PCIE1_TXN0											
		USB1_SSTX2N											
		PRG1_SGMII0_TXN0											

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AG14	SERDES1_TX0_P	SERDES1_TX0_P		O	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII3_TXP0											
		PCIE1_TXP0											
		USB1_SSTX2P											
		PRG1_SGMII0_TXP0											
AF16	SERDES1_TX1_N	SERDES1_TX1_N		O	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII4_TXN0											
		PCIE1_TXN1											
		USB1_SSTX1N											
		PRG1_SGMII1_TXN0											
AG15	SERDES1_TX1_P	SERDES1_TX1_P		O	OFF		0.8 V	VDDA_0P8_SERDES0_1 / VDDA_1P8_SERDES0_1		2-L-PHY			
		SGMII4_TXP0											
		PCIE1_TXP1											
		USB1_SSTX1P											
		PRG1_SGMII1_TXP0											
AH13	SERDES2_RX0_N	SERDES2_RX0_N		I	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE2_RXN0											
		USB1_SSRX2N											
		PRG1_SGMII0_RXN0											
AJ12	SERDES2_RX0_P	SERDES2_RX0_P		I	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE2_RXP0											
		USB1_SSRX2P											
		PRG1_SGMII0_RXP0											
AH12	SERDES2_RX1_N	SERDES2_RX1_N		I	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE2_RXN1											
		USB1_SSRX1N											
		PRG1_SGMII1_RXN0											
AJ11	SERDES2_RX1_P	SERDES2_RX1_P		I	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE2_RXP1											
		USB1_SSRX1P											
		PRG1_SGMII1_RXP0											
AF13	SERDES2_TX0_N	SERDES2_TX0_N		O	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE2_TXN0											
		USB1_SSTX2N											
		PRG1_SGMII0_TXN0											

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AG12	SERDES2_TX0_P	SERDES2_TX0_P		O	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE2_TXP0											
		USB1_SSTX2P											
		PRG1_SGMII0_TXP0											
AF12	SERDES2_TX1_N	SERDES2_TX1_N		O	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE2_TXN1											
		USB1_SSTX1N											
		PRG1_SGMII1_TXN0											
AG11	SERDES2_TX1_P	SERDES2_TX1_P		O	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE2_TXP1											
		USB1_SSTX1P											
		PRG1_SGMII1_TXP0											
AH9	SERDES3_RX0_N	SERDES3_RX0_N		I	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE3_RXN0											
		USB0_SSRX2N											
AJ8	SERDES3_RX0_P	SERDES3_RX0_P		I	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE3_RXP0											
		USB0_SSRX2P											
AH10	SERDES3_RX1_N	SERDES3_RX1_N		I	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE3_RXN1											
		USB0_SSRX1N											
AJ9	SERDES3_RX1_P	SERDES3_RX1_P		I	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE3_RXP1											
		USB0_SSRX1P											
AF9	SERDES3_TX0_N	SERDES3_TX0_N		O	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE3_TXN0											
		USB0_SSTX2N											
AG8	SERDES3_TX0_P	SERDES3_TX0_P		O	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE3_TXP0											
		USB0_SSTX2P											
AF10	SERDES3_TX1_N	SERDES3_TX1_N		O	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE3_TXN1											
		USB0_SSTX1N											
AG9	SERDES3_TX1_P	SERDES3_TX1_P		O	OFF		0.8 V	VDDA_0P8_SERDES2_3 / VDDA_1P8_SERDES2_3		2-L-PHY			
		PCIE3_TXP1											
		USB0_SSTX1P											

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
D9	SERDES4_RX0_N	SERDES4_RX0_N		I	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		SGMII5_RXN0											
C10	SERDES4_RX0_P	SERDES4_RX0_P		I	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		SGMII5_RXP0											
D8	SERDES4_RX1_N	SERDES4_RX1_N		I	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		SGMII6_RXN0											
C9	SERDES4_RX1_P	SERDES4_RX1_P		I	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		SGMII6_RXP0											
D6	SERDES4_RX2_N	SERDES4_RX2_N		I	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		SGMII7_RXN0											
C7	SERDES4_RX2_P	SERDES4_RX2_P		I	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		SGMII7_RXP0											
D5	SERDES4_RX3_N	SERDES4_RX3_N		I	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		SGMII8_RXN0											
C6	SERDES4_RX3_P	SERDES4_RX3_P		I	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		SGMII8_RXP0											
B11	SERDES4_TX0_N	SERDES4_TX0_N		O	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		DP0_TX0_N											
		SGMII5_TXN0											
A12	SERDES4_TX0_P	SERDES4_TX0_P		O	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		DP0_TX0_P											
		SGMII5_TXP0											
B10	SERDES4_TX1_N	SERDES4_TX1_N		O	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		DP0_TX1_N											
		SGMII6_TXN0											
A11	SERDES4_TX1_P	SERDES4_TX1_P		O	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		DP0_TX1_P											
		SGMII6_TXP0											
B8	SERDES4_TX2_N	SERDES4_TX2_N		O	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		DP0_TX2_N											
		SGMII7_TXN0											
A9	SERDES4_TX2_P	SERDES4_TX2_P		O	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		DP0_TX2_P											
		SGMII7_TXP0											

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
B7	SERDES4_TX3_N	SERDES4_TX3_N		O	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		DP0_TX3_N											
		SGMII8_TXN0											
A8	SERDES4_TX3_P	SERDES4_TX3_P		O	OFF		0.8 V	VDDA_0P8_DP / VDDA_1P8_DP		4-L-PHY			
		DP0_TX3_P											
		SGMII8_TXP0											
U4	soc_safety_errorn	SOC_SAFETY_ERRORn	0	IO	PD	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		1/0
AA1	spi0_clk	SPI0_CLK	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	0/1
		UART1_CTSn	1	I								1	
		I2C2_SCL	2	IOD								1	
		GPIO0_113	7	IO								0	
Y1	spi1_clk	SPI1_CLK	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	0/1
		UART5_CTSn	1	I								1	
		I2C4_SDA	2	IOD								1	
		UART2_RXD	3	I								1	
		GPIO0_118	7	IO								0	
		PRG0_IEP0_EDC_SYNC_OUT0	8	O								0	
AA2	spi0_cs0	SPI0_CS0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	1	0/1
		UART0_RTSn	1	O									
		GPIO0_111	7	IO								0	
Y4	spi0_cs1	SPI0_CS1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	1	0/1
		CPTS0_TS_COMP	1	O									
		I2C3_SCL	2	IOD								1	
		DP0_HPD	5	I								0	
		PRG1_IEP0_EDIO_OUTVALID	6	O									
		GPIO0_112	7	IO								0	
AB5	spi0_d0	SPI0_D0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	0/1
		UART1_RTSn	1	O									
		I2C2_SDA	2	IOD								1	
		GPIO0_114	7	IO								0	
AA3	spi0_d1	SPI0_D1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	0/1
		I2C6_SCL	2	IOD								1	
		GPIO0_115	7	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
Y3	spi1_cs0	SPI1_CS0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	1	0/1
		UART0_CTSn	1	I								1	
		UART5_RXD	3	I								1	
		PRG0_IEP0_EDIO_OUTVALID	6	O									
		GPIO0_116	7	IO								0	
		PRG0_IEP0_EDC_LATCH_IN0	8	I								0	
W4	spi1_cs1	SPI1_CS1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	1	0/1
		CPTS0_TS_SYNC	1	O									
		I2C3_SDA	2	IOD								1	
		UART5_TXD	3	O									
		GPIO0_117	7	IO								0	
Y5	spi1_d0	SPI1_D0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	0/1
		UART5_RTSn	1	O									
		I2C4_SCL	2	IOD								1	
		UART2_TXD	3	O									
		GPIO0_119	7	IO								0	
		PRG0_IEP1_EDC_LATCH_IN0	8	I								0	
Y2	spi1_d1	SPI1_D1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	0/1
		I2C6_SDA	2	IOD								1	
		GPIO0_120	7	IO								0	
		PRG0_IEP1_EDC_SYNC_OUT0	8	O								0	
E29	tck	TCK	0	I	PU	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		1/1
V1	tdi	TDI	0	I	PU	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		1/1
V3	tdo	TDO	0	OZ	PU	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		0/0
V6	timer_io0	TIMER_IO0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	1/1
		ECAP1_IN_APWM_OUT	1	IO								0	
		SYSCLKOUT0	2	O									
		SPI7_D0	6	IO								0	
		GPIO1_13	7	IO								0	
		BOOTMODE4	Bootstrap	I									
V5	timer_io1	TIMER_IO1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	0	1/1
		ECAP2_IN_APWM_OUT	1	IO								0	
		OBSCLK0	2	O									
		SPI7_D1	6	IO								0	
		GPIO1_14	7	IO								0	
		BOOTMODE5	Bootstrap	I									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
V2	tms	TMS	0	I	PU	0	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		1/1
F24	trstn	TRSTn	0	I	PD	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		1/1
AC2	uart0_ctsn	UART0_CTSn	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	1	0/1
		TIMER_IO6	1	IO								0	
		SPI0_CS2	2	IO								1	
		MCAN2_RX	3	I								1	
		SPI2_CS0	4	IO								1	
		EQEP0_A	5	I								0	
		GPIO0_123	7	IO								0	
AB1	uart0_rtsn	UART0_RTSn	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		0/1
		TIMER_IO7	1	IO								0	
		SPI0_CS3	2	IO								1	
		MCAN2_TX	3	O									
		SPI2_CLK	4	IO								0	
		EQEP0_B	5	I								0	
		GPIO0_124	7	IO								0	
AB2	uart0_rxd	UART0_RXD	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	1	0/1
		SPI2_CS1	4	IO								1	
		GPIO0_121	7	IO								0	
AB3	uart0_txd	UART0_TXD	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		0/1
		SPI2_CS2	4	IO								1	
		SPI7_CS1	6	IO								1	
		GPIO0_122	7	IO								0	
AC4	uart1_ctsn	UART1_CTSn	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	1	0/1
		MCAN3_RX	1	I								1	
		SPI2_D0	4	IO								0	
		EQEP0_S	5	IO								0	
		GPIO0_127	7	IO								0	
AD5	uart1_rtsn	UART1_RTSn	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		0/1
		MCAN3_TX	1	O									
		SPI2_D1	4	IO								0	
		EQEP0_I	5	IO								0	
		GPIO1_0	7	IO								0	
AA4	uart1_rxd	UART1_RXD	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD	1	0/1
		SPI7_CS2	6	IO								1	
		GPIO0_125	7	IO								0	

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AB4	uart1_txd	UART1_TXD	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		0/1
		I3C0_SDAPULLEN	5	O									
		SPI7_CS3	6	IO								1	
		GPIO0_126	7	IO								0	
AE6	ufs0_ref_clk	UFS0_REF_CLK		O	OFF		0.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY			
AD6	ufs0_rstn	UFS0_RSTn		O	OFF		0.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY			
AH3	ufs0_rx_dn0	UFS0_RX_DN0		I	OFF		0.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY			
AH4	ufs0_rx_dn1	UFS0_RX_DN1		I	OFF		0.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY			
AJ2	ufs0_rx_dp0	UFS0_RX_DP0		I	OFF		0.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY			
AJ3	ufs0_rx_dp1	UFS0_RX_DP1		I	OFF		0.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY			
AG6	ufs0_tx_dn0	UFS0_TX_DN0		O	OFF		0.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY			
AG5	ufs0_tx_dn1	UFS0_TX_DN1		O	OFF		0.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY			
AF7	ufs0_tx_dp0	UFS0_TX_DP0		O	OFF		0.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY			
AF6	ufs0_tx_dp1	UFS0_TX_DP1		O	OFF		0.8 V	VDDA_0P8_UFS / VDDA_1P8_UFS		M-PHY			
AJ5	usb0_dm	USB0_DM		IO	OFF		3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY			

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AH6	usb0_dp	USB0_DP		IO	OFF		3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY			
U6	usb0_drvvbus	USB0_DRVVBUS	0	O	PD	7	1.8 V/3.3 V	VDDSHV0	Yes	LVCMOS	PU/PD		0/1
		USB1_DRVVBUS	1	O									
		GPIO1_29	7	IO								0	
AC6	usb0_id	USB0_ID		A	OFF		3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY			
AB6	usb0_rcalib	USB0_RCALIB		IO	OFF		3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY			
AC7	usb0_vbus	USB0_VBUS		A	OFF		3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY			
AH7	usb1_dm	USB1_DM		IO	OFF		3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY			
AJ6	usb1_dp	USB1_DP		IO	OFF		3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY			
AD7	usb1_id	USB1_ID		A	OFF		3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY			
AD9	usb1_rcalib	USB1_RCALIB		IO	OFF		3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY			

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
AD8	usb1_vbus	USB1_VBUS		A	OFF		3.3 V	VDDA_0P8_USB / VDDA_1P8_USB / VDDA_3P3_USB		USB2PHY			
L14, V13, V16, W19	VDDAR_CORE	VDDAR_CORE		PWR									
L11, W12	VDDAR_CPU	VDDAR_CPU		PWR									
K19, T19	vddar_mcu	vddar_mcu		PWR									
H17	VDDA_0P8_CSIRX	VDDA_0P8_CSIRX		PWR									
G12, J12	VDDA_0P8_DP	VDDA_0P8_DP		PWR									
G14, H13	VDDA_0P8_DP_C	VDDA_0P8_DP_C		PWR									
H15	VDDA_0P8_DSITX	VDDA_0P8_DSITX		PWR									
J16	VDDA_0P8_DSITX_C	VDDA_0P8_DSITX_C		PWR									
AB9	VDDA_0P8_UFS	VDDA_0P8_UFS		PWR									
AA10	VDDA_0P8_USB	VDDA_0P8_USB		PWR									
AA15, Y14, Y16	VDDA_0P8_SERDES0_1	VDDA_0P8_SERDES0_1		PWR									
AA12, Y11, Y13	VDDA_0P8_SERDES2_3	VDDA_0P8_SERDES2_3		PWR									
AB14, AB15	VDDA_0P8_SERDES_C0_1	VDDA_0P8_SERDES_C0_1		PWR									
AB12, AB13	VDDA_0P8_SERDES_C2_3	VDDA_0P8_SERDES_C2_3		PWR									
G16	VDDA_1P8_CSIRX	VDDA_1P8_CSIRX		PWR									
H11	VDDA_1P8_DP	VDDA_1P8_DP		PWR									
J14	VDDA_1P8_DSITX	VDDA_1P8_DSITX		PWR									
AC8	VDDA_1P8_UFS	VDDA_1P8_UFS		PWR									
AC9	vdda_1p8_usb	vdda_1p8_usb		PWR									
AC14, AC15	VDDA_1P8_SERDES0_1	VDDA_1P8_SERDES0_1		PWR									
AC11, AC12	VDDA_1P8_SERDES2_3	VDDA_1P8_SERDES2_3		PWR									
AB10	vdda_3p3_usb	vdda_3p3_usb		PWR									
N22	VDDA_ADC0	VDDA_ADC0		PWR									
M23	VDDA_ADC1	VDDA_ADC1		PWR									
N9	VDDA_0P8_PLL_DDR	VDDA_0P8_PLL_DDR		PWR									
G18	VDDA_MCU_PLLGRP0	VDDA_MCU_PLLGRP0		PWR									
P21	VDDA_MCU_TEMP	VDDA_MCU_TEMP		PWR									
W7	VDDA_1P8_MLB	VDDA_1P8_MLB		PWR									
Y20	VDDA_PLLGRP0	VDDA_PLLGRP0		PWR									
W17	VDDA_PLLGRP1	VDDA_PLLGRP1		PWR									
M17	VDDA_PLLGRP2	VDDA_PLLGRP2		PWR									
L12	VDDA_PLLGRP3	VDDA_PLLGRP3		PWR									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
R11	VDDA_PLLGRP4	VDDA_PLLGRP4		PWR									
P9	VDDA_PLLGRP5	VDDA_PLLGRP5		PWR									
W18	VDDA_PLLGRP6	VDDA_PLLGRP6		PWR									
W8	VDDA_0P8_PLL_MLB	VDDA_0P8_PLL_MLB		PWR									
P22	vdda_por_wkup	vdda_por_wkup		PWR									
W15	VDDA_TEMP0_1	VDDA_TEMP0_1		PWR									
H9	VDDA_TEMP2_3	VDDA_TEMP2_3		PWR									
M26	VMON_ER_VSYS	VMON_ER_VSYS		A									
V19	VMON_IR_VEXT	VMON_IR_VEXT		A									
H22	VDDA_WKUP	VDDA_WKUP		PWR									
U8, V7	VDDSHV0	VDDSHV0		PWR									
L22, M22	VDDSHV0_MCU	VDDSHV0_MCU		PWR									
AA19, AA20, AC19, AC20	VDDSHV1	VDDSHV1		PWR									
H19, H21, J20	VDDSHV1_MCU	VDDSHV1_MCU		PWR									
AA17, AB16, AB18, AC17	VDDSHV2	VDDSHV2		PWR									
J22, K21	VDDSHV2_MCU	VDDSHV2_MCU		PWR									
V21, W22	VDDSHV3	VDDSHV3		PWR									
AA21, Y22	VDDSHV4	VDDSHV4		PWR									
T20, T22	VDDSHV5	VDDSHV5		PWR									
U20, U22	VDDSHV6	VDDSHV6		PWR									
A1, G8, J8, K7, L8, M7, N8, P7, R8, T1	vdds_ddr	vdds_ddr		PWR									
H7, J6, R6, T7	vdds_ddr_bias	vdds_ddr_bias		PWR									
M9	VDDS_DDR_C	VDDS_DDR_C		PWR									
AA8, AB7, Y7	vdds_mmc0	vdds_mmc0		PWR									
R21	VDDS_OSC1	VDDS_OSC1		PWR									
J10, K11, K13, K15, K17, K9, L10, L16, L18, M15, N14, N16, N18, P13, P15, P17, R14, R16, R18, R20, T15, T17, T9, U14, U16, U18, V15, V17, V20, W14	VDD_CORE	VDD_CORE		PWR									
N10, P11, R10, R12, U10, V11, V9, W10	VDD_CPU	VDD_CPU		PWR									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
Y9	VDDA_0P8_DLL_MMC0	VDDA_0P8_DLL_MMC0		PWR									
L20, M19, M21, N20, P19	vdd_mcu	vdd_mcu		PWR									
AB11	vpp_core	vpp_core		PWR									
F17	VPP_MCU	VPP_MCU		PWR									
AA13, AC10, AC13, AD11, AD14, AD17, AE10, AE12, AE15, AE16, AE19, AE7, AF20, AF25, AF5, AG4, AG7, AH2, AH20, AH5, AJ4, AJ7, B3, B6, C1, C5, D2, D4, E1, E5, F4, G1, G7, H4, H6, K1, K4, L3, M1, M28, M4, M6, N27, N29, N3, P1, P28, P4, R3, U5	vss	vss		GND									

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
A10, A13, A16, A19, A22, A7, AA11, AA14, AA16, AA18, AA7, AA9, AB17, AB19, AB20, AB22, AB8, AC16, AF11, AF14, AF17, AF8, AG10, AG13, AG16, AG19, AH11, AH14, AH17, AH8, AJ10, AJ13, AJ16, AJ19, B12, B15, B18, B21, B9, C11, C14, C17, C20, C8, D10, D13, D16, D19, D7, E12, E15, E9, F14, F8, G11, G13, G15, G17, H10, H12, H14, H16, H18, H20, H8, J11, J13, J15, J17, J21, J23, J7, J9, K10, K12, K14, K16, K18, K20, K22, K8, L13, L15, L17, L19, L21, L23, L7, L9, M10, M14, M16, M18, M20, M8, N15, N17, N19, N21, N7, P10, P12, P14, P16, P18, P20, P8, R13, R15, R17, R19, R7, R9, T10, T14, T16, T18, T21, T8, U15, U17, U19, U21, U9, V10, V12, V14, V18, V8, W11, W13, W16, W20, W9, Y10, Y12, Y15, Y17, Y19, Y21, Y8	VSS	VSS		GND									
F26	wkup_gpio0_0	MCU_SPI1_CLK	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	0	1/1
		MCU_SPI1_CLK	1	IO								0	
		WKUP_GPIO0_0	7	IO								0	
		MCU_BOOTMODE03	Bootstrap	I									
F25	wkup_gpio0_1	MCU_SPI1_D0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	0	1/1
		MCU_SPI1_D0	1	IO								0	
		WKUP_GPIO0_1	7	IO								0	
		MCU_BOOTMODE04	Bootstrap	I									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
F28	wkup_gpio0_2	MCU_SPI1_D1	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	0	1/1
		MCU_SPI1_D1	1	IO								0	
		WKUP_GPIO0_2	7	IO								0	
		MCU_BOOTMODE05	Bootstrap	I									
F27	wkup_gpio0_3	MCU_SPI1_CS0	0	IO	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	1	0/1
		MCU_SPI1_CS0	1	IO								1	
		WKUP_GPIO0_3	7	IO								0	
G25	wkup_gpio0_4	MCU_MCAN1_TX	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		0/1
		MCU_MCAN1_TX	1	O									
		MCU_SPI0_CS3	2	IO								1	
		MCU_ADC_EXT_TRIGGER0	3	I								pad	
		WKUP_GPIO0_4	7	IO								0	
G24	wkup_gpio0_5	MCU_MCAN1_RX	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	1	0/1
		MCU_MCAN1_RX	1	I								1	
		MCU_SPI1_CS3	2	IO								1	
		MCU_ADC_EXT_TRIGGER1	3	I								pad	
		WKUP_GPIO0_5	7	IO								0	
F29	wkup_gpio0_6	WKUP_UART0_CTSn	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	1	0/1
		WKUP_UART0_CTSn	1	I								1	
		MCU_CPTS0_HW1TSPUSH	2	I								0	
		MCU_I2C1_SCL	3	IOD								1	
		WKUP_GPIO0_6	7	IO								0	
G28	wkup_gpio0_7	WKUP_UART0_RTSn	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		0/1
		WKUP_UART0_RTSn	1	O									
		MCU_CPTS0_HW2TSPUSH	2	I								0	
		MCU_I2C1_SDA	3	IOD								1	
		WKUP_GPIO0_7	7	IO								0	
G27	wkup_gpio0_8	MCU_I2C1_SCL	0	IOD	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	1	0/1
		MCU_I2C1_SCL	1	IOD								1	
		MCU_CPTS0_TS_SYNC	2	O									
		MCU_I3C1_SCL	3	IO								1	
		MCU_TIMER_IO6	4	IO								0	
		WKUP_GPIO0_8	7	IO								0	

表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
G26	wkup_gpio0_9	MCU_I2C1_SDA	0	IOD	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	1	0/1
		MCU_I2C1_SDA	1	IOD								1	
		MCU_CPTS0_TS_COMP	2	O									
		MCU_I3C1_SDA	3	IO								1	
		MCU_TIMER_IO7	4	IO								0	
		WKUP_GPIO0_9	7	IO								0	
H26	wkup_gpio0_10	MCU_EXT_REFCLK0	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	0	0/1
		MCU_EXT_REFCLK0	1	I								0	
		MCU_UART0_TXD	2	O									
		MCU_ADC_EXT_TRIGGER0	3	I								0	
		MCU_CPTS0_RFT_CLK	4	I								0	
		MCU_SYSCLKOUT0	5	O									
		WKUP_GPIO0_10	7	IO								0	
H27	wkup_gpio0_11	MCU_OBSCLK0	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		0/1
		MCU_OBSCLK0	1	O									
		MCU_UART0_RXD	2	I								1	
		MCU_ADC_EXT_TRIGGER1	3	I								0	
		MCU_TIMER_IO1	4	IO								0	
		MCU_I3C1_SDAPULLEN	5	O									
		MCU_CLKOUT0	6	OZ									
		WKUP_GPIO0_11	7	IO								0	
G29	wkup_gpio0_12	MCU_UART0_TXD	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		1/1
		MCU_SPI0_CS1	1	O									
		WKUP_GPIO0_12	7	IO								0	
		MCU_BOOTMODE08	Bootstrap	I									
H28	wkup_gpio0_13	MCU_UART0_RXD	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	1	1/1
		MCU_SPI1_CS1	1	O									
		WKUP_GPIO0_13	7	IO								0	
		MCU_BOOTMODE09	Bootstrap	I									
H29	wkup_gpio0_14	MCU_UART0_CTSn	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	1	1/1
		MCU_SPI0_CS2	1	O									
		WKUP_GPIO0_14	7	IO								0	
		MCU_BOOTMODE06	Bootstrap	I									
J27	wkup_gpio0_15	MCU_UART0_RTSn	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		1/1
		MCU_SPI1_CS2	1	O									
		WKUP_GPIO0_15	7	IO								0	
		MCU_BOOTMODE07	Bootstrap	I									

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表 5-1. Pin Attributes (続き)

BALL NUMBER [1]	BALL NAME [2]	SIGNAL NAME [3]	MUXMODE [4]	TYPE [5]	BALL RESET STATE [6]	BALL RESET REL. MUXMODE	I/O VOLTAGE VALUE [8]	POWER [9]	HYS [10]	BUFFER TYPE [11]	PULL UP/ DOWN TYPE [12]	DSIS [13]	RXACTIVE/ TXDISABLE [14]
J25	wkup_i2c0_scl	WKUP_I2C0_SCL	0	IOD	OFF	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	I2C OD FS		1	1/0
		WKUP_GPIO0_62	7	IO								0	
H24	wkup_i2c0_sda	WKUP_I2C0_SDA	0	IOD	OFF	0	1.8 V/3.3 V	VDDSHV0_MCU	Yes	I2C OD FS		1	1/0
		WKUP_GPIO0_63	7	IO								0	
N28	wkup_lfosc0_xi	WKUP_LFOSC0_XI		I	OFF		1.8 V	VDDA_WKUP		LFOSC			
N26	wkup_lfosc0_xo	WKUP_LFOSC0_XO		O	OFF		1.8 V	VDDA_WKUP		LFOSC			
M29	wkup_osc0_xi	WKUP_OSC0_XI		I	OFF		1.8 V	VDDA_WKUP		HFOSC			
M27	wkup_osc0_xo	WKUP_OSC0_XO		O	OFF		1.8 V	VDDA_WKUP		HFOSC			
J29	wkup_uart0_rxd	WKUP_UART0_RXD	0	I	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD	1	0/1
		WKUP_GPIO0_56	7	IO								0	
J28	wkup_uart0_txd	WKUP_UART0_TXD	0	O	OFF	7	1.8 V/3.3 V	VDDSHV0_MCU	Yes	LVCMOS	PU/PD		0/1
		WKUP_GPIO0_57	7	IO								0	

1. The MUXMODE field is not used to select the multiplexed signal function for this pin. For more information, see *ADC Integration Details* section in *Device Configuration* chapter of the device TRM.

The following list describes the table column headers:

1. **BALL NUMBER:** Ball numbers on the bottom side associated with each signal on the bottom.
2. **BALL NAME:** Mechanical name from package device (name is taken from muxmode 0).
3. **SIGNAL NAME:** Names of signals multiplexed on each ball (also notice that the name of the ball is the signal name in muxmode 0).

注

表 5-1, *Pin Attributes*, does not take into account the subsystem multiplexing signals. Subsystem multiplexing signals are described in セクション 5.3, *Signal Descriptions*.

4. **MUXMODE:** Multiplexing mode number:
   a. MUXMODE 0 is the primary muxmode. The primary muxmode is not necessarily the default muxmode.

   注

   The default muxmode is the mode at the release of the reset; also see the BALL RESET REL. MUXMODE column.

   b. MUXMODE 1 through 7 are possible muxmodes for alternate functions. On each pin, some muxmodes are effectively used for alternate functions, while some muxmodes are not used. Only MUXMODE values which correspond to defined functions should be used.
   c. MCU_BOOTMODE pins are latched on the rising edge of MCU_PORz_OUT. BOOTMODE pins are latched on the rising edge of PORz_OUT.
   d. An empty box means Not Applicable.
5. **TYPE:** Signal type and direction:
   - I = Input

- O = Output
- IO = Input or Output
- IOD = Open drain terminal - Input or Output
- IOZ = Input, Output or Three-state terminal
- OZ = Output or Three-state terminal
- A = Analog
- PWR = Power
- GND = Ground
- CAP = LDO Capacitor.

6. **BALL RESET STATE:** The state of the terminal at power-on reset:
   - DRIVE 0 (OFF): The buffer drives V_{OL} (pulldown or pullup resistor not activated).
   - DRIVE 1 (OFF): The buffer drives V_{OH} (pulldown or pullup resistor not activated).
   - OFF: High-impedance
   - PD: High-impedance with an active pulldown resistor
   - PU: High-impedance with an active pullup resistor
   - An empty box means Not Applicable.
7. **BALL RESET REL. MUXMODE:** This muxmode is automatically configured at the release of the rstoutn signal.
   An empty box means Not Applicable.
8. **I/O VOLTAGE VALUE**: This column describes the IO voltage value (the corresponding power supply).
   An empty box means Not Applicable.
9. **POWER:** The voltage supply that powers the terminal IO buffers.
   An empty box means Not Applicable.
10. **HYS:** Indicates if the input buffer has hysteresis:
    - Yes: With hysteresis
    - No: Without hysteresis

    An empty box means No.

    For more information, see the hysteresis values in , *Electrical Characteristics* .
11. **BUFFER TYPE:** This column describes the associated output buffer type

    An empty box means Not Applicable.

    For drive strength of the associated output buffer, refer to, *Electrical Characteristics*.
12. **PULL UP/DOWN TYPE:** indicates the presence of an internal pullup or pulldown resistor. Pullup and pulldown resistors can be enabled or disabled via software.
    - PU: Internal pullup
    - PD: Internal pulldown
    - PU/PD: Internal pullup and pulldown
    - An empty box means No pull.

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13. **DSIS:** The deselected input state (DSIS) indicates the state driven on the peripheral input (logic "0", logic "1", or "PIN" level) when the peripheral pin function is not selected by any of the PINCNTLx registers.
    - 0: Logic 0 driven on the input signal port of the peripheral.
    - 1: Logic 1 driven on the input signal port of the peripheral.
    - An empty box means Not Applicable.
14. **RXACTIVE / TXDISABLE:**This column indicates the default value of the RXACTIVE / TXDISABLE bits in the PADCONFIG register.
    - RXACTIVE: 0 = receiver disabled, 1 = receiver enabled.
    - TXDISABLE: 0 = driver enabled, 1 = driver disabled.
    - An empty box means Not Applicable.

注

Configuring two pins to the same input signal is not supported as it can yield unexpected results. This can be easily prevented with the proper software configuration (HiZ mode is not an input signal).

注

When a pad is set into a multiplexing mode which is not defined by pin multiplexing, that pad's behavior is undefined. This should be avoided.

5.3 Signal Descriptions

Many signals are available on multiple pins, according to the software configuration of the pin multiplexing options.

The following list describes the column headers:

1. **SIGNAL NAME:** The name of the signal passing through the pin.

   注

   In *Pin Attributes* and *Pin Multiplexing* are not described the subsystem multiplexing signals.

2. **DESCRIPTION:** Description of the signal
3. **PIN TYPE:** Signal direction and type:
   - I = Input
   - O = Output
   - IO = Input or Output
   - IOD = Open drain terminal - Input or Output
   - IOZ = Input, Output or Three-state terminal
   - OZ = Output or Three-state terminal
   - A = Analog
   - PWR = Power
   - GND = Ground
   - CAP = LDO Capacitor
4. **BALL:** Associated balls bottom

   For more information on the I/O cell configurations, see *Pad Configuration Registers* section in *Device Configuration* chapter in the device TRM.

5.3.1 ADC

注

The ADC can be configured to be used as a GPI. For more information, see *Analog-to-Digital Converter (ADC)* section in *Peripherals* chapter in the device TRM.

5.3.1.1 MCU Domain

表 5-2. ADC Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_ADC_EXT_TRIGGER0	ADC Trigger Input	I	A28, G25, H26
MCU_ADC_EXT_TRIGGER1	ADC Trigger Input	I	A27, G24, H27

表 5-3. ADC0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_ADC0_AIN0	ADC Analog Input 0	A	K25
MCU_ADC0_AIN1	ADC Analog Input 1	A	K26
MCU_ADC0_AIN2	ADC Analog Input 2	A	K28
MCU_ADC0_AIN3	ADC Analog Input 3	A	L28
MCU_ADC0_AIN4	ADC Analog Input 4	A	K24
MCU_ADC0_AIN5	ADC Analog Input 5	A	K27
MCU_ADC0_AIN6	ADC Analog Input 6	A	K29
MCU_ADC0_AIN7	ADC Analog Input 7	A	L29

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表 5-4. ADC1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_ADC1_AIN0	ADC Analog Input 0	A	N23
MCU_ADC1_AIN1	ADC Analog Input 1	A	M25
MCU_ADC1_AIN2	ADC Analog Input 2	A	L24
MCU_ADC1_AIN3	ADC Analog Input 3	A	L26
MCU_ADC1_AIN4	ADC Analog Input 4	A	N24
MCU_ADC1_AIN5	ADC Analog Input 5	A	M24
MCU_ADC1_AIN6	ADC Analog Input 6	A	L25
MCU_ADC1_AIN7	ADC Analog Input 7	A	L27

5.3.2 DDRSS

5.3.2.1 MAIN Domain

表 5-5. DDRSS Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
DDR_RET	External IO Retention Enable	I	P6

表 5-6. DDRSS0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
DDR0_CKN	DDRSS Differential Clock (negative)	IO	J1
DDR0_CKP	DDRSS Differential Clock (positive)	IO	H1
DDR0_RESETn	DDRSS Reset	IO	K6
DDR0_CA0	DDRSS Command Address	IO	G4
DDR0_CA1	DDRSS Command Address	IO	H3
DDR0_CA2	DDRSS Command Address	IO	K5
DDR0_CA3	DDRSS Command Address	IO	J4
DDR0_CA4	DDRSS Command Address	IO	K2
DDR0_CA5	DDRSS Command Address	IO	H5
DDR0_CAL0[(1)]	IO Pad Calibration Resistor	A	H2
DDR0_CKE0	DDRSS Clock Enable	IO	G3
DDR0_CKE1	DDRSS Clock Enable	IO	J3
DDR0_CSn0_0	DDRSS Chip Select	IO	J5
DDR0_CSn0_1	DDRSS Chip Select	IO	K3
DDR0_CSn1_0	DDRSS Chip Select	IO	G5
DDR0_CSn1_1	DDRSS Chip Select	IO	J2
DDR0_DM0	DDRSS Data Mask	IO	A3
DDR0_DM1	DDRSS Data Mask	IO	E4
DDR0_DM2	DDRSS Data Mask	IO	N1
DDR0_DM3	DDRSS Data Mask	IO	R5
DDR0_DQ0	DDRSS Data	IO	A5
DDR0_DQ1	DDRSS Data	IO	A6
DDR0_DQ2	DDRSS Data	IO	B5
DDR0_DQ3	DDRSS Data	IO	C2
DDR0_DQ4	DDRSS Data	IO	B4
DDR0_DQ5	DDRSS Data	IO	C3

表 5-6. DDRSS0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
DDR0_DQ6	DDRSS Data	IO	A2
DDR0_DQ7	DDRSS Data	IO	A4
DDR0_DQ8	DDRSS Data	IO	D1
DDR0_DQ9	DDRSS Data	IO	C4
DDR0_DQ10	DDRSS Data	IO	F1
DDR0_DQ11	DDRSS Data	IO	G2
DDR0_DQ12	DDRSS Data	IO	F2
DDR0_DQ13	DDRSS Data	IO	F3
DDR0_DQ14	DDRSS Data	IO	D3
DDR0_DQ15	DDRSS Data	IO	F5
DDR0_DQ16	DDRSS Data	IO	L5
DDR0_DQ17	DDRSS Data	IO	M5
DDR0_DQ18	DDRSS Data	IO	N5
DDR0_DQ19	DDRSS Data	IO	L4
DDR0_DQ20	DDRSS Data	IO	L2
DDR0_DQ21	DDRSS Data	IO	L1
DDR0_DQ22	DDRSS Data	IO	N2
DDR0_DQ23	DDRSS Data	IO	N4
DDR0_DQ24	DDRSS Data	IO	T3
DDR0_DQ25	DDRSS Data	IO	T2
DDR0_DQ26	DDRSS Data	IO	P2
DDR0_DQ27	DDRSS Data	IO	P3
DDR0_DQ28	DDRSS Data	IO	P5
DDR0_DQ29	DDRSS Data	IO	R4
DDR0_DQ30	DDRSS Data	IO	T4
DDR0_DQ31	DDRSS Data	IO	T5
DDR0_DQS0N	DDRSS Complimentary Data Strobe	IO	B1
DDR0_DQS0P	DDRSS Data Strobe	IO	B2
DDR0_DQS1N	DDRSS Complimentary Data Strobe	IO	E2
DDR0_DQS1P	DDRSS Data Strobe	IO	E3
DDR0_DQS2N	DDRSS Complimentary Data Strobe	IO	M2
DDR0_DQS2P	DDRSS Data Strobe	IO	M3
DDR0_DQS3N	DDRSS Complimentary Data Strobe	IO	R1
DDR0_DQS3P	DDRSS Data Strobe	IO	R2

(1) An external 240 Ω ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.

5.3.3 GPIO

5.3.3.1 MAIN Domain

表 5-7. GPIO0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPIO0_0	General Purpose Input/Output	IO	AC18
GPIO0_1	General Purpose Input/Output	IO	AC23
GPIO0_2	General Purpose Input/Output	IO	AG22

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表 5-7. GPIO0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPIO0_3	General Purpose Input/Output	IO	AF22
GPIO0_4	General Purpose Input/Output	IO	AJ23
GPIO0_5	General Purpose Input/Output	IO	AH23
GPIO0_6	General Purpose Input/Output	IO	AD20
GPIO0_7	General Purpose Input/Output	IO	AD22
GPIO0_8	General Purpose Input/Output	IO	AE20
GPIO0_9	General Purpose Input/Output	IO	AJ20
GPIO0_10	General Purpose Input/Output	IO	AG20
GPIO0_11	General Purpose Input/Output	IO	AD21
GPIO0_12	General Purpose Input/Output	IO	AF24
GPIO0_13	General Purpose Input/Output	IO	AJ24
GPIO0_14	General Purpose Input/Output	IO	AG24
GPIO0_15	General Purpose Input/Output	IO	AD24
GPIO0_16	General Purpose Input/Output	IO	AC24
GPIO0_17	General Purpose Input/Output	IO	AE24
GPIO0_18	General Purpose Input/Output	IO	AJ21
GPIO0_19	General Purpose Input/Output	IO	AE21
GPIO0_100	General Purpose Input/Output	IO	W28
GPIO0_101	General Purpose Input/Output	IO	V25
GPIO0_102	General Purpose Input/Output	IO	W27
GPIO0_103	General Purpose Input/Output	IO	W29
GPIO0_104	General Purpose Input/Output	IO	W26
GPIO0_105	General Purpose Input/Output	IO	Y29
GPIO0_106	General Purpose Input/Output	IO	Y27
GPIO0_107	General Purpose Input/Output	IO	W24
GPIO0_108	General Purpose Input/Output	IO	W25
GPIO0_109	General Purpose Input/Output	IO	V26
GPIO0_110	General Purpose Input/Output	IO	V24
GPIO0_111	General Purpose Input/Output	IO	AA2
GPIO0_112	General Purpose Input/Output	IO	Y4
GPIO0_113	General Purpose Input/Output	IO	AA1
GPIO0_114	General Purpose Input/Output	IO	AB5
GPIO0_115	General Purpose Input/Output	IO	AA3
GPIO0_116	General Purpose Input/Output	IO	Y3
GPIO0_117	General Purpose Input/Output	IO	W4
GPIO0_118	General Purpose Input/Output	IO	Y1
GPIO0_119	General Purpose Input/Output	IO	Y5
GPIO0_120	General Purpose Input/Output	IO	Y2
GPIO0_121	General Purpose Input/Output	IO	AB2
GPIO0_122	General Purpose Input/Output	IO	AB3
GPIO0_123	General Purpose Input/Output	IO	AC2
GPIO0_124	General Purpose Input/Output	IO	AB1
GPIO0_125	General Purpose Input/Output	IO	AA4
GPIO0_126	General Purpose Input/Output	IO	AB4

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表 5-7. GPIO0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPIO0_127	General Purpose Input/Output	IO	AC4
GPIO0_20	General Purpose Input/Output	IO	AH21
GPIO0_21	General Purpose Input/Output	IO	AE22
GPIO0_22	General Purpose Input/Output	IO	AG23
GPIO0_23	General Purpose Input/Output	IO	AF23
GPIO0_24	General Purpose Input/Output	IO	AD23
GPIO0_25	General Purpose Input/Output	IO	AH24
GPIO0_26	General Purpose Input/Output	IO	AG21
GPIO0_27	General Purpose Input/Output	IO	AE23
GPIO0_28	General Purpose Input/Output	IO	AC21
GPIO0_29	General Purpose Input/Output	IO	Y23
GPIO0_30	General Purpose Input/Output	IO	AF21
GPIO0_31	General Purpose Input/Output	IO	AB23
GPIO0_32	General Purpose Input/Output	IO	AJ25
GPIO0_33	General Purpose Input/Output	IO	AH25
GPIO0_34	General Purpose Input/Output	IO	AG25
GPIO0_35	General Purpose Input/Output	IO	AH26
GPIO0_36	General Purpose Input/Output	IO	AJ27
GPIO0_37	General Purpose Input/Output	IO	AJ26
GPIO0_38	General Purpose Input/Output	IO	AC22
GPIO0_39	General Purpose Input/Output	IO	AJ22
GPIO0_40	General Purpose Input/Output	IO	AH22
GPIO0_41	General Purpose Input/Output	IO	AD19
GPIO0_42	General Purpose Input/Output	IO	AD18
GPIO0_43	General Purpose Input/Output	IO	AF28
GPIO0_44	General Purpose Input/Output	IO	AE28
GPIO0_45	General Purpose Input/Output	IO	AE27
GPIO0_46	General Purpose Input/Output	IO	AD26
GPIO0_47	General Purpose Input/Output	IO	AD25
GPIO0_48	General Purpose Input/Output	IO	AC29
GPIO0_49	General Purpose Input/Output	IO	AE26
GPIO0_50	General Purpose Input/Output	IO	AC28
GPIO0_51	General Purpose Input/Output	IO	AC27
GPIO0_52	General Purpose Input/Output	IO	AB26
GPIO0_53	General Purpose Input/Output	IO	AB25
GPIO0_54	General Purpose Input/Output	IO	AJ28
GPIO0_55	General Purpose Input/Output	IO	AH27
GPIO0_56	General Purpose Input/Output	IO	AH29
GPIO0_57	General Purpose Input/Output	IO	AG28
GPIO0_58	General Purpose Input/Output	IO	AG27
GPIO0_59	General Purpose Input/Output	IO	AH28
GPIO0_60	General Purpose Input/Output	IO	AB24
GPIO0_61	General Purpose Input/Output	IO	AB29
GPIO0_62	General Purpose Input/Output	IO	AB28

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表 5-7. GPIO0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPIO0_63	General Purpose Input/Output	IO	AE29
GPIO0_64	General Purpose Input/Output	IO	AD28
GPIO0_65	General Purpose Input/Output	IO	AD27
GPIO0_66	General Purpose Input/Output	IO	AC25
GPIO0_67	General Purpose Input/Output	IO	AD29
GPIO0_68	General Purpose Input/Output	IO	AB27
GPIO0_69	General Purpose Input/Output	IO	AC26
GPIO0_70	General Purpose Input/Output	IO	AA24
GPIO0_71	General Purpose Input/Output	IO	AA28
GPIO0_72	General Purpose Input/Output	IO	Y24
GPIO0_73	General Purpose Input/Output	IO	AA25
GPIO0_74	General Purpose Input/Output	IO	AG26
GPIO0_75	General Purpose Input/Output	IO	AF27
GPIO0_76	General Purpose Input/Output	IO	AF26
GPIO0_77	General Purpose Input/Output	IO	AE25
GPIO0_78	General Purpose Input/Output	IO	AF29
GPIO0_79	General Purpose Input/Output	IO	AG29
GPIO0_80	General Purpose Input/Output	IO	Y25
GPIO0_81	General Purpose Input/Output	IO	AA26
GPIO0_82	General Purpose Input/Output	IO	AA29
GPIO0_83	General Purpose Input/Output	IO	Y26
GPIO0_84	General Purpose Input/Output	IO	AA27
GPIO0_85	General Purpose Input/Output	IO	U23
GPIO0_86	General Purpose Input/Output	IO	U26
GPIO0_87	General Purpose Input/Output	IO	V28
GPIO0_88	General Purpose Input/Output	IO	V29
GPIO0_89	General Purpose Input/Output	IO	V27
GPIO0_90	General Purpose Input/Output	IO	U28
GPIO0_91	General Purpose Input/Output	IO	U29
GPIO0_92	General Purpose Input/Output	IO	U25
GPIO0_93	General Purpose Input/Output	IO	U27
GPIO0_94	General Purpose Input/Output	IO	U24
GPIO0_95	General Purpose Input/Output	IO	R23
GPIO0_96	General Purpose Input/Output	IO	T23
GPIO0_97	General Purpose Input/Output	IO	Y28
GPIO0_98	General Purpose Input/Output	IO	V23
GPIO0_99	General Purpose Input/Output	IO	W23

表 5-8. GPIO1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPIO1_0	General Purpose Input/Output	IO	AD5
GPIO1_1	General Purpose Input/Output	IO	W5
GPIO1_2	General Purpose Input/Output	IO	W6
GPIO1_3	General Purpose Input/Output	IO	W3

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表 5-8. GPIO1 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPIO1_4	General Purpose Input/Output	IO	V4
GPIO1_5	General Purpose Input/Output	IO	W2
GPIO1_6	General Purpose Input/Output	IO	W1
GPIO1_7	General Purpose Input/Output	IO	AC5
GPIO1_8	General Purpose Input/Output	IO	AA5
GPIO1_9	General Purpose Input/Output	IO	Y6
GPIO1_10	General Purpose Input/Output	IO	AA6
GPIO1_11	General Purpose Input/Output	IO	U2
GPIO1_12	General Purpose Input/Output	IO	U3
GPIO1_13	General Purpose Input/Output	IO	V6
GPIO1_14	General Purpose Input/Output	IO	V5
GPIO1_15	General Purpose Input/Output	IO	R26
GPIO1_16	General Purpose Input/Output	IO	R25
GPIO1_17	General Purpose Input/Output	IO	P24
GPIO1_18	General Purpose Input/Output	IO	R24
GPIO1_19	General Purpose Input/Output	IO	P25
GPIO1_20	General Purpose Input/Output	IO	R29
GPIO1_21	General Purpose Input/Output	IO	P23
GPIO1_22	General Purpose Input/Output	IO	R28
GPIO1_23	General Purpose Input/Output	IO	T28
GPIO1_24	General Purpose Input/Output	IO	T29
GPIO1_25	General Purpose Input/Output	IO	T27
GPIO1_26	General Purpose Input/Output	IO	T24
GPIO1_27	General Purpose Input/Output	IO	T26
GPIO1_28	General Purpose Input/Output	IO	T25
GPIO1_29	General Purpose Input/Output	IO	U6
GPIO1_30	General Purpose Input/Output	IO	AD1
GPIO1_31	General Purpose Input/Output	IO	AC1
GPIO1_32	General Purpose Input/Output	IO	AC3
GPIO1_33	General Purpose Input/Output	IO	AD3
GPIO1_34	General Purpose Input/Output	IO	AD2
GPIO1_35	General Purpose Input/Output	IO	AE2

5.3.3.2 WKUP Domain

表 5-9. GPIO0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
WKUP_GPIO0_0	General Purpose Input/Output	IO	F26
WKUP_GPIO0_1	General Purpose Input/Output	IO	F25
WKUP_GPIO0_2	General Purpose Input/Output	IO	F28
WKUP_GPIO0_3	General Purpose Input/Output	IO	F27
WKUP_GPIO0_4	General Purpose Input/Output	IO	G25
WKUP_GPIO0_5	General Purpose Input/Output	IO	G24
WKUP_GPIO0_6	General Purpose Input/Output	IO	F29

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表 5-9. GPIO0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
WKUP_GPIO0_7	General Purpose Input/Output	IO	G28
WKUP_GPIO0_8	General Purpose Input/Output	IO	G27
WKUP_GPIO0_9	General Purpose Input/Output	IO	G26
WKUP_GPIO0_10	General Purpose Input/Output	IO	H26
WKUP_GPIO0_11	General Purpose Input/Output	IO	H27
WKUP_GPIO0_12	General Purpose Input/Output	IO	G29
WKUP_GPIO0_13	General Purpose Input/Output	IO	H28
WKUP_GPIO0_14	General Purpose Input/Output	IO	H29
WKUP_GPIO0_15	General Purpose Input/Output	IO	J27
WKUP_GPIO0_16	General Purpose Input/Output	IO	E20
WKUP_GPIO0_17	General Purpose Input/Output	IO	C21
WKUP_GPIO0_18	General Purpose Input/Output	IO	D21
WKUP_GPIO0_19	General Purpose Input/Output	IO	D20
WKUP_GPIO0_20	General Purpose Input/Output	IO	G19
WKUP_GPIO0_21	General Purpose Input/Output	IO	G20
WKUP_GPIO0_22	General Purpose Input/Output	IO	F20
WKUP_GPIO0_23	General Purpose Input/Output	IO	F21
WKUP_GPIO0_24	General Purpose Input/Output	IO	E21
WKUP_GPIO0_25	General Purpose Input/Output	IO	B22
WKUP_GPIO0_26	General Purpose Input/Output	IO	G21
WKUP_GPIO0_27	General Purpose Input/Output	IO	F19
WKUP_GPIO0_28	General Purpose Input/Output	IO	E19
WKUP_GPIO0_29	General Purpose Input/Output	IO	F22
WKUP_GPIO0_30	General Purpose Input/Output	IO	A23
WKUP_GPIO0_31	General Purpose Input/Output	IO	B23
WKUP_GPIO0_32	General Purpose Input/Output	IO	D22
WKUP_GPIO0_33	General Purpose Input/Output	IO	G22
WKUP_GPIO0_34	General Purpose Input/Output	IO	D23
WKUP_GPIO0_35	General Purpose Input/Output	IO	C23
WKUP_GPIO0_36	General Purpose Input/Output	IO	C22
WKUP_GPIO0_37	General Purpose Input/Output	IO	E22
WKUP_GPIO0_38	General Purpose Input/Output	IO	B27
WKUP_GPIO0_39	General Purpose Input/Output	IO	C25
WKUP_GPIO0_40	General Purpose Input/Output	IO	A28
WKUP_GPIO0_41	General Purpose Input/Output	IO	A27
WKUP_GPIO0_42	General Purpose Input/Output	IO	A26
WKUP_GPIO0_43	General Purpose Input/Output	IO	B25
WKUP_GPIO0_44	General Purpose Input/Output	IO	B26
WKUP_GPIO0_45	General Purpose Input/Output	IO	C24
WKUP_GPIO0_46	General Purpose Input/Output	IO	A25
WKUP_GPIO0_47	General Purpose Input/Output	IO	D24
WKUP_GPIO0_48	General Purpose Input/Output	IO	A24
WKUP_GPIO0_49	General Purpose Input/Output	IO	B24
WKUP_GPIO0_50	General Purpose Input/Output	IO	E23

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表 5-9. GPIO0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
WKUP_GPIO0_51	General Purpose Input/Output	IO	F23
WKUP_GPIO0_52	General Purpose Input/Output	IO	E27
WKUP_GPIO0_53	General Purpose Input/Output	IO	E24
WKUP_GPIO0_54	General Purpose Input/Output	IO	E28
WKUP_GPIO0_55	General Purpose Input/Output	IO	E25
WKUP_GPIO0_56	General Purpose Input/Output	IO	J29
WKUP_GPIO0_57	General Purpose Input/Output	IO	J28
WKUP_GPIO0_58	General Purpose Input/Output	IO	D29
WKUP_GPIO0_59	General Purpose Input/Output	IO	C29
WKUP_GPIO0_60	General Purpose Input/Output	IO	D26
WKUP_GPIO0_61	General Purpose Input/Output	IO	D25
WKUP_GPIO0_62	General Purpose Input/Output	IO	J25
WKUP_GPIO0_63	General Purpose Input/Output	IO	H24
WKUP_GPIO0_64	General Purpose Input/Output	IO	J26
WKUP_GPIO0_65	General Purpose Input/Output	IO	H25
WKUP_GPIO0_66	General Purpose Input/Output	IO	E26
WKUP_GPIO0_67	General Purpose Input/Output	IO	G23
WKUP_GPIO0_68	General Purpose Input	I	K25
WKUP_GPIO0_69	General Purpose Input	I	K26
WKUP_GPIO0_70	General Purpose Input	I	K28
WKUP_GPIO0_71	General Purpose Input	I	L28
WKUP_GPIO0_72	General Purpose Input	I	K24
WKUP_GPIO0_73	General Purpose Input	I	K27
WKUP_GPIO0_74	General Purpose Input	I	K29
WKUP_GPIO0_75	General Purpose Input	I	L29
WKUP_GPIO0_76	General Purpose Input	I	N23
WKUP_GPIO0_77	General Purpose Input	I	M25
WKUP_GPIO0_78	General Purpose Input	I	L24
WKUP_GPIO0_79	General Purpose Input	I	L26
WKUP_GPIO0_80	General Purpose Input	I	N24
WKUP_GPIO0_81	General Purpose Input	I	M24
WKUP_GPIO0_82	General Purpose Input	I	L25
WKUP_GPIO0_83	General Purpose Input	I	L27

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5.3.4 I2C

5.3.4.1 MAIN Domain

表 5-10. I2C0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
I2C0_SCL	I2C Clock	IOD	AC5
I2C0_SDA	I2C Data	IOD	AA5

表 5-11. I2C1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
I2C1_SCL	I2C Clock	IOD	Y6
I2C1_SDA	I2C Data	IOD	AA6

表 5-12. I2C2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
I2C2_SCL	I2C Clock	IOD	AA1, U23, W5
I2C2_SDA	I2C Data	IOD	AB5, U26, W6

表 5-13. I2C3 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
I2C3_SCL	I2C Clock	IOD	T26, V27, Y4
I2C3_SDA	I2C Data	IOD	T25, U28, W4

表 5-14. I2C4 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
I2C4_SCL	I2C Clock	IOD	AD19, P25, Y5
I2C4_SDA	I2C Data	IOD	AD18, R29, Y1

表 5-15. I2C5 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
I2C5_SCL	I2C Clock	IOD	T28, Y26
I2C5_SDA	I2C Data	IOD	AA27, T29

表 5-16. I2C6 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
I2C6_SCL	I2C Clock	IOD	AA3, U29, W2
I2C6_SDA	I2C Data	IOD	U25, W1, Y2

5.3.4.2 MCU Domain

表 5-17. I2C0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_I2C0_SCL	I2C Clock	IOD	J26
MCU_I2C0_SDA	I2C Data	IOD	H25

表 5-18. I2C1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_I2C1_SCL	I2C Clock	IOD	F29, G27
MCU_I2C1_SDA	I2C Data	IOD	G26, G28

5.3.4.3 WKUP Domain

表 5-19. I2C0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
WKUP_I2C0_SCL	I2C Clock	IOD	J25
WKUP_I2C0_SDA	I2C Data	IOD	H24

5.3.5 I3C

5.3.5.1 MAIN Domain

表 5-20. I3C0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
I3C0_SCL	I3C Clock	IO	W2
I3C0_SDA	I3C Data	IO	W1
I3C0_SDAPULLEN	MAIN domain I3C Data Pull Enable	O	AB4, U2

5.3.5.2 MCU Domain

表 5-21. I3C0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_I3C0_SCL	I3C Clock	IO	D26
MCU_I3C0_SDA	I3C Data	IO	D25
MCU_I3C0_SDAPULLEN	MCU domain I3C Data Pull Enable	O	E26

表 5-22. I3C1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_I3C1_SCL	I3C Clock	IO	G27
MCU_I3C1_SDA	I3C Data	IO	G26
MCU_I3C1_SDAPULLEN	MCU domain I3C Data Pull Enable	O	G23, H27

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5.3.6 MCAN

5.3.6.1 MAIN Domain

表 5-23. MCAN0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN0_RX	MCAN Receive Data	I	W5
MCAN0_TX	MCAN Transmit Data	O	W6

表 5-24. MCAN1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN1_RX	MCAN Receive Data	I	W3
MCAN1_TX	MCAN Transmit Data	O	V4

表 5-25. MCAN2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN2_RX	MCAN Receive Data	I	AC2, W2
MCAN2_TX	MCAN Transmit Data	O	AB1, W1

表 5-26. MCAN3 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN3_RX	MCAN Receive Data	I	AC4
MCAN3_TX	MCAN Transmit Data	O	AD5

表 5-27. MCAN4 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN4_RX	MCAN Receive Data	I	AJ20, AJ24
MCAN4_TX	MCAN Transmit Data	O	AE20, AF24

表 5-28. MCAN5 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN5_RX	MCAN Receive Data	I	AD24, AE21
MCAN5_TX	MCAN Transmit Data	O	AG24, AJ21

表 5-29. MCAN6 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN6_RX	MCAN Receive Data	I	AE24, AG21
MCAN6_TX	MCAN Transmit Data	O	AC24, AH21

表 5-30. MCAN7 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN7_RX	MCAN Receive Data	I	AG25, Y23
MCAN7_TX	MCAN Transmit Data	O	AC21, AH25

表 5-31. MCAN8 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN8_RX	MCAN Receive Data	I	AB23, AJ27
MCAN8_TX	MCAN Transmit Data	O	AF21, AH26

表 5-32. MCAN9 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN9_RX	MCAN Receive Data	I	AC27
MCAN9_TX	MCAN Transmit Data	O	AC28

表 5-33. MCAN10 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN10_RX	MCAN Receive Data	I	AB25
MCAN10_TX	MCAN Transmit Data	O	AB26

表 5-34. MCAN11 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN11_RX	MCAN Receive Data	I	AA28
MCAN11_TX	MCAN Transmit Data	O	AA24

表 5-35. MCAN12 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN12_RX	MCAN Receive Data	I	AA29
MCAN12_TX	MCAN Transmit Data	O	AA26

表 5-36. MCAN13 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCAN13_RX	MCAN Receive Data	I	AA27
MCAN13_TX	MCAN Transmit Data	O	Y26

5.3.6.2 MCU Domain

表 5-37. MCAN0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_MCAN0_RX	MCAN Receive Data	I	C29
MCU_MCAN0_TX	MCAN Transmit Data	O	D29

表 5-38. MCAN1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_MCAN1_RX	MCAN Receive Data	I	G24
MCU_MCAN1_TX	MCAN Transmit Data	O	G25

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5.3.7 MCSPI

5.3.7.1 MAIN Domain

表 5-39. MCSPI0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SPI0_CLK	SPI Clock	IO	AA1
SPI0_CS0	SPI Chip Select 0	IO	AA2
SPI0_CS1	SPI Chip Select 1	IO	Y4
SPI0_CS2	SPI Chip Select 2	IO	AC2
SPI0_CS3	SPI Chip Select 3	IO	AB1
SPI0_D0	SPI Data 0	IO	AB5
SPI0_D1	SPI Data 1	IO	AA3

表 5-40. MCSPI1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SPI1_CLK	SPI Clock	IO	Y1
SPI1_CS0	SPI Chip Select 0	IO	Y3
SPI1_CS1	SPI Chip Select 1	IO	W4
SPI1_CS2	SPI Chip Select 2	IO	AD19
SPI1_CS3	SPI Chip Select 3	IO	AD18
SPI1_D0	SPI Data 0	IO	Y5
SPI1_D1	SPI Data 1	IO	Y2

表 5-41. MCSPI2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SPI2_CLK	SPI Clock	IO	AB1
SPI2_CS0	SPI Chip Select 0	IO	AC2
SPI2_CS1	SPI Chip Select 1	IO	AB2
SPI2_CS2	SPI Chip Select 2	IO	AB3
SPI2_CS3	SPI Chip Select 3	IO	U2
SPI2_D0	SPI Data 0	IO	AC4
SPI2_D1	SPI Data 1	IO	AD5

表 5-42. MCSPI3 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SPI3_CLK	SPI Clock	IO	Y25
SPI3_CS0	SPI Chip Select 0	IO	AA24
SPI3_CS1	SPI Chip Select 1	IO	AB26
SPI3_CS2	SPI Chip Select 2	IO	AB25
SPI3_CS3	SPI Chip Select 3	IO	Y24
SPI3_D0	SPI Data 0	IO	AA26
SPI3_D1	SPI Data 1	IO	AA29

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表 5-43. MCSPI5 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SPI5_CLK	SPI Clock	IO	W29
SPI5_CS0	SPI Chip Select 0	IO	W27
SPI5_CS1	SPI Chip Select 1	IO	W25
SPI5_CS2	SPI Chip Select 2	IO	W28
SPI5_CS3	SPI Chip Select 3	IO	W23
SPI5_D0	SPI Data 0	IO	V25
SPI5_D1	SPI Data 1	IO	W24

表 5-44. MCSPI6 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SPI6_CLK	SPI Clock	IO	AC22
SPI6_CS0	SPI Chip Select 0	IO	AC21
SPI6_CS1	SPI Chip Select 1	IO	AG20
SPI6_CS2	SPI Chip Select 2	IO	AD21
SPI6_CS3	SPI Chip Select 3	IO	AF21
SPI6_D0	SPI Data 0	IO	AJ22
SPI6_D1	SPI Data 1	IO	AH22

表 5-45. MCSPI7 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SPI7_CLK	SPI Clock	IO	U3
SPI7_CS0	SPI Chip Select 0	IO	U2
SPI7_CS1	SPI Chip Select 1	IO	AB3
SPI7_CS2	SPI Chip Select 2	IO	AA4
SPI7_CS3	SPI Chip Select 3	IO	AB4
SPI7_D0	SPI Data 0	IO	V6
SPI7_D1	SPI Data 1	IO	V5

5.3.7.2 MCU Domain

表 5-46. MCSPI0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_SPI0_CLK	SPI Clock	IO	E27
MCU_SPI0_CS0	SPI Chip Select 0	IO	E25
MCU_SPI0_CS1	SPI Chip Select 1	IO	C23, G29
MCU_SPI0_CS2	SPI Chip Select 2	IO	E22, H29
MCU_SPI0_CS3	SPI Chip Select 3	IO	G25
MCU_SPI0_D0	SPI Data 0	IO	E24
MCU_SPI0_D1	SPI Data 1	IO	E28

表 5-47. MCSPI1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_SPI1_CLK	SPI Clock	IO	F26

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表 5-47. MCSPI1 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_SPI1_CS0	SPI Chip Select 0	IO	F27
MCU_SPI1_CS1	SPI Chip Select 1	O	G22, H28
MCU_SPI1_CS2	SPI Chip Select 2	O	D23, J27
MCU_SPI1_CS3	SPI Chip Select 3	IO	G24
MCU_SPI1_D0	SPI Data 0	IO	F25
MCU_SPI1_D1	SPI Data 1	IO	F28

5.3.8 UART

5.3.8.1 MAIN Domain

表 5-48. UART0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART0_CTSn	UART Clear to Send (active low)	I	AC2, Y3
UART0_DCDn	UART Data Carrier Detect (active low)	I	P23
UART0_DSRn	UART Data Set Ready (active low)	I	R28
UART0_DTRn	UART Data Terminal Ready (active low)	O	T27
UART0_RIn	UART Ring Indicator	I	T24
UART0_RTSn	UART Request to Send (active low)	O	AA2, AB1
UART0_RXD	UART Receive Data	I	AB2, AC23
UART0_TXD	UART Transmit Data	O	AB3, AG22

表 5-49. UART1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART1_CTSn	UART Clear to Send (active low)	I	AA1, AC4
UART1_RTSn	UART Request to Send (active low)	O	AB5, AD5
UART1_RXD	UART Receive Data	I	AA4, AF22
UART1_TXD	UART Transmit Data	O	AB4, AJ23

表 5-50. UART2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART2_CTSn	UART Clear to Send (active low)	I	AE25
UART2_RTSn	UART Request to Send (active low)	O	AF29
UART2_RXD	UART Receive Data	I	AA26, AH23, Y1
UART2_TXD	UART Transmit Data	O	AA24, AD22, Y5

表 5-51. UART3 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART3_CTSn	UART Clear to Send (active low)	I	AD19, U27
UART3_RTSn	UART Request to Send (active low)	O	AD18, U24
UART3_RXD	UART Receive Data	I	AE27, T26, V28, Y23
UART3_TXD	UART Transmit Data	O	AC21, AD26, T25, V29

表 5-52. UART4 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART4_CTSn	UART Clear to Send (active low)	I	AE29, Y29
UART4_RTSn	UART Request to Send (active low)	O	AD28, Y27
UART4_RXD	UART Receive Data	I	AG28, P24, W23
UART4_TXD	UART Transmit Data	O	AG27, R24, W28

表 5-53. UART5 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART5_CTSn	UART Clear to Send (active low)	I	Y1
UART5_RTSn	UART Request to Send (active low)	O	Y5
UART5_RXD	UART Receive Data	I	AE29, Y29, Y3
UART5_TXD	UART Transmit Data	O	AD28, W4, Y27

表 5-54. UART6 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART6_CTSn	UART Clear to Send (active low)	I	R23, W3
UART6_RTSn	UART Request to Send (active low)	O	T23, V4
UART6_RXD	UART Receive Data	I	AC27, T27, U27, W2
UART6_TXD	UART Transmit Data	O	AB26, T24, U24, W1

表 5-55. UART7 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART7_CTSn	UART Clear to Send (active low)	I	P24
UART7_RTSn	UART Request to Send (active low)	O	R24
UART7_RXD	UART Receive Data	I	R26
UART7_TXD	UART Transmit Data	O	R25

表 5-56. UART8 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART8_CTSn	UART Clear to Send (active low)	I	AF27, P23
UART8_RTSn	UART Request to Send (active low)	O	AF26, R28
UART8_RXD	UART Receive Data	I	P25, Y24
UART8_TXD	UART Transmit Data	O	AA25, R29

表 5-57. UART9 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UART9_CTSn	UART Clear to Send (active low)	I	T27, W2
UART9_RTSn	UART Request to Send (active low)	O	T24, W1
UART9_RXD	UART Receive Data	I	T28, W3
UART9_TXD	UART Transmit Data	O	T29, V4

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5.3.8.2 MCU Domain

表 5-58. UART0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_UART0_CTSn	UART Clear to Send (active low)	I	C23, D26, H29
MCU_UART0_RTSn	UART Request to Send (active low)	O	D25, E22, J27
MCU_UART0_RXD	UART Receive Data	I	G22, H27, H28
MCU_UART0_TXD	UART Transmit Data	O	D23, G29, H26

5.3.8.3 WKUP Domain

表 5-59. UART0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
WKUP_UART0_CTSn	UART Clear to Send (active low)	I	F29
WKUP_UART0_RTSn	UART Request to Send (active low)	O	G28
WKUP_UART0_RXD	UART Receive Data	I	J29
WKUP_UART0_TXD	UART Transmit Data	O	J28

5.3.9 MDIO

5.3.9.1 MCU Domain

表 5-60. MDIO0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_MDIO0_MDC	MDIO Clock	O	F23
MCU_MDIO0_MDIO	MDIO Data	IO	E23

5.3.10 CPSW2G

注

The subsystem (SS) applies to both CPSW2G and the CPTS. For more details about CPTS signal characteristics, see the セクション 5.3.21, *CPTS signal descriptions*.

5.3.10.1 MCU Domain

表 5-61. CPSW2G0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_RGMII1_RXC	RGMII Receive Clock	I	C24
MCU_RGMII1_RX_CTL	RGMII Receive Control	I	C25
MCU_RGMII1_TXC	RGMII Transmit Clock	O	B26
MCU_RGMII1_TX_CTL	RGMII Transmit Control	O	B27
MCU_RGMII1_RD0	RGMII Receive Data 0	I	B24
MCU_RGMII1_RD1	RGMII Receive Data 1	I	A24
MCU_RGMII1_RD2	RGMII Receive Data 2	I	D24
MCU_RGMII1_RD3	RGMII Receive Data 3	I	A25
MCU_RGMII1_TD0	RGMII Transmit Data 0	O	B25
MCU_RGMII1_TD1	RGMII Transmit Data 1	O	A26
MCU_RGMII1_TD2	RGMII Transmit Data 2	O	A27
MCU_RGMII1_TD3	RGMII Transmit Data 3	O	A28

表 5-61. CPSW2G0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_RMII1_CRS_DV	RMII Carrier Sense / Data Valid	I	B27
MCU_RMII1_REF_CLK	RMII Reference Clock	I	C24
MCU_RMII1_RX_ER	RMII Receive Data Error	I	C25
MCU_RMII1_TX_EN	RMII Transmit Enable	O	B26
MCU_RMII1_RXD0	RMII Receive Data 0	I	B24
MCU_RMII1_RXD1	RMII Receive Data 1	I	A24
MCU_RMII1_TXD0	RMII Transmit Data 0	O	B25
MCU_RMII1_TXD1	RMII Transmit Data 1	O	A26

5.3.11 CPSW9G

5.3.11.1 MAIN Domain

表 5-62. CPSW9G0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
CLKOUT	RMII Clock Output (50 MHz). This pin is used for clock source to the external PHY and must be routed back to the RMII_REF_CLK pin for proper device operation.	OZ	AA25, AJ28, Y29
MDIO0_MDC	MDIO Clock	O	V24
MDIO0_MDIO	MDIO Data	IO	V26
RGMII1_RXC	RGMII Receive Clock	I	AD22
RGMII1_RX_CTL	RGMII Receive Control	I	AH23
RGMII1_TXC	RGMII Transmit Clock	O	AE24
RGMII1_TX_CTL	RGMII Transmit Control	O	AC24
RGMII2_RXC	RGMII Receive Clock	I	AE23
RGMII2_RX_CTL	RGMII Receive Control	I	AH24
RGMII2_TXC	RGMII Transmit Clock	O	AJ26
RGMII2_TX_CTL	RGMII Transmit Control	O	AJ27
RGMII3_RXC	RGMII Receive Clock	I	AE26
RGMII3_RX_CTL	RGMII Receive Control	I	AD25
RGMII3_TXC	RGMII Transmit Clock	O	AH28
RGMII3_TX_CTL	RGMII Transmit Control	O	AG27
RGMII4_RXC	RGMII Receive Clock	I	AC26
RGMII4_RX_CTL	RGMII Receive Control	I	AD29
RGMII4_TXC	RGMII Transmit Clock	O	AG29
RGMII4_TX_CTL	RGMII Transmit Control	O	AF29
RGMII5_RXC	RGMII Receive Clock	I	U25
RGMII5_RX_CTL	RGMII Receive Control	I	U26
RGMII5_TXC	RGMII Transmit Clock	O	U29
RGMII5_TX_CTL	RGMII Transmit Control	O	U23
RGMII6_RXC	RGMII Receive Clock	I	W26
RGMII6_RX_CTL	RGMII Receive Control	I	V23
RGMII6_TXC	RGMII Transmit Clock	O	W29
RGMII6_TX_CTL	RGMII Transmit Control	O	Y28
RGMII7_RXC	RGMII Receive Clock	I	AD22
RGMII7_RX_CTL	RGMII Receive Control	I	AH23

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表 5-62. CPSW9G0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
RGMII7_TXC	RGMII Transmit Clock	O	AE24
RGMII7_TX_CTL	RGMII Transmit Control	O	AC24
RGMII8_RXC	RGMII Receive Clock	I	AE23
RGMII8_RX_CTL	RGMII Receive Control	I	AH24
RGMII8_TXC	RGMII Transmit Clock	O	AJ26
RGMII8_TX_CTL	RGMII Transmit Control	O	AJ27
RGMII1_RD0	RGMII Receive Data 0	I	AC23
RGMII1_RD1	RGMII Receive Data 1	I	AG22
RGMII1_RD2	RGMII Receive Data 2	I	AF22
RGMII1_RD3	RGMII Receive Data 3	I	AJ23
RGMII1_TD0	RGMII Transmit Data 0	O	AF24
RGMII1_TD1	RGMII Transmit Data 1	O	AJ24
RGMII1_TD2	RGMII Transmit Data 2	O	AG24
RGMII1_TD3	RGMII Transmit Data 3	O	AD24
RGMII2_RD0	RGMII Receive Data 0	I	AE22
RGMII2_RD1	RGMII Receive Data 1	I	AG23
RGMII2_RD2	RGMII Receive Data 2	I	AF23
RGMII2_RD3	RGMII Receive Data 3	I	AD23
RGMII2_TD0	RGMII Transmit Data 0	O	AJ25
RGMII2_TD1	RGMII Transmit Data 1	O	AH25
RGMII2_TD2	RGMII Transmit Data 2	O	AG25
RGMII2_TD3	RGMII Transmit Data 3	O	AH26
RGMII3_RD0	RGMII Receive Data 0	I	AF28
RGMII3_RD1	RGMII Receive Data 1	I	AE28
RGMII3_RD2	RGMII Receive Data 2	I	AE27
RGMII3_RD3	RGMII Receive Data 3	I	AD26
RGMII3_TD0	RGMII Transmit Data 0	O	AJ28
RGMII3_TD1	RGMII Transmit Data 1	O	AH27
RGMII3_TD2	RGMII Transmit Data 2	O	AH29
RGMII3_TD3	RGMII Transmit Data 3	O	AG28
RGMII4_RD0	RGMII Receive Data 0	I	AE29
RGMII4_RD1	RGMII Receive Data 1	I	AD28
RGMII4_RD2	RGMII Receive Data 2	I	AD27
RGMII4_RD3	RGMII Receive Data 3	I	AC25
RGMII4_TD0	RGMII Transmit Data 0	O	AG26
RGMII4_TD1	RGMII Transmit Data 1	O	AF27
RGMII4_TD2	RGMII Transmit Data 2	O	AF26
RGMII4_TD3	RGMII Transmit Data 3	O	AE25
RGMII5_RD0	RGMII Receive Data 0	I	T23
RGMII5_RD1	RGMII Receive Data 1	I	R23
RGMII5_RD2	RGMII Receive Data 2	I	U24
RGMII5_RD3	RGMII Receive Data 3	I	U27
RGMII5_TD0	RGMII Transmit Data 0	O	U28
RGMII5_TD1	RGMII Transmit Data 1	O	V27

表 5-62. CPSW9G0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
RGMII5_TD2	RGMII Transmit Data 2	O	V29
RGMII5_TD3	RGMII Transmit Data 3	O	V28
RGMII6_RD0	RGMII Receive Data 0	I	W25
RGMII6_RD1	RGMII Receive Data 1	I	W24
RGMII6_RD2	RGMII Receive Data 2	I	Y27
RGMII6_RD3	RGMII Receive Data 3	I	Y29
RGMII6_TD0	RGMII Transmit Data 0	O	W27
RGMII6_TD1	RGMII Transmit Data 1	O	V25
RGMII6_TD2	RGMII Transmit Data 2	O	W28
RGMII6_TD3	RGMII Transmit Data 3	O	W23
RGMII7_RD0	RGMII Receive Data 0	I	AC23
RGMII7_RD1	RGMII Receive Data 1	I	AG22
RGMII7_RD2	RGMII Receive Data 2	I	AF22
RGMII7_RD3	RGMII Receive Data 3	I	AJ23
RGMII7_TD0	RGMII Transmit Data 0	O	AF24
RGMII7_TD1	RGMII Transmit Data 1	O	AJ24
RGMII7_TD2	RGMII Transmit Data 2	O	AG24
RGMII7_TD3	RGMII Transmit Data 3	O	AD24
RGMII8_RD0	RGMII Receive Data 0	I	AE22
RGMII8_RD1	RGMII Receive Data 1	I	AG23
RGMII8_RD2	RGMII Receive Data 2	I	AF23
RGMII8_RD3	RGMII Receive Data 3	I	AD23
RGMII8_TD0	RGMII Transmit Data 0	O	AJ25
RGMII8_TD1	RGMII Transmit Data 1	O	AH25
RGMII8_TD2	RGMII Transmit Data 2	O	AG25
RGMII8_TD3	RGMII Transmit Data 3	O	AH26
RMII1_CRS_DV	RMII Carrier Sense / Data Valid	I	AF22
RMII1_RX_ER	RMII Receive Data Error	I	AJ23
RMII1_TX_EN	RMII Transmit Enable	O	AD20
RMII2_CRS_DV	RMII Carrier Sense / Data Valid	I	AF23
RMII2_RX_ER	RMII Receive Data Error	I	AD23
RMII2_TX_EN	RMII Transmit Enable	O	AJ25
RMII3_CRS_DV	RMII Carrier Sense / Data Valid	I	AE27
RMII3_RX_ER	RMII Receive Data Error	I	AD26
RMII3_TX_EN	RMII Transmit Enable	O	AE26
RMII4_CRS_DV	RMII Carrier Sense / Data Valid	I	AD27
RMII4_RX_ER	RMII Receive Data Error	I	AC25
RMII4_TX_EN	RMII Transmit Enable	O	AG26
RMII5_CRS_DV	RMII Carrier Sense / Data Valid	I	AD21
RMII5_RX_ER	RMII Receive Data Error	I	AE21
RMII5_TX_EN	RMII Transmit Enable	O	AG21
RMII6_CRS_DV	RMII Carrier Sense / Data Valid	I	AB23
RMII6_RX_ER	RMII Receive Data Error	I	AC21
RMII6_TX_EN	RMII Transmit Enable	O	AC22

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表 5-62. CPSW9G0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
RMII7_CRS_DV	RMII Carrier Sense / Data Valid	I	U23
RMII7_RX_ER	RMII Receive Data Error	I	U26
RMII7_TX_EN	RMII Transmit Enable	O	U29
RMII8_CRS_DV	RMII Carrier Sense / Data Valid	I	Y28
RMII8_RX_ER	RMII Receive Data Error	I	V23
RMII8_TX_EN	RMII Transmit Enable	O	W29
RMII1_RXD0	RMII Receive Data 0	I	AC23
RMII1_RXD1	RMII Receive Data 1	I	AG22
RMII1_TXD0	RMII Transmit Data 0	O	AH23
RMII1_TXD1	RMII Transmit Data 1	O	AD22
RMII2_RXD0	RMII Receive Data 0	I	AE22
RMII2_RXD1	RMII Receive Data 1	I	AG23
RMII2_TXD0	RMII Transmit Data 0	O	AH24
RMII2_TXD1	RMII Transmit Data 1	O	AE23
RMII3_RXD0	RMII Receive Data 0	I	AE28
RMII3_RXD1	RMII Receive Data 1	I	AF28
RMII3_TXD0	RMII Transmit Data 0	O	AC29
RMII3_TXD1	RMII Transmit Data 1	O	AD25
RMII4_RXD0	RMII Receive Data 0	I	AE29
RMII4_RXD1	RMII Receive Data 1	I	AD28
RMII4_TXD0	RMII Transmit Data 0	O	AC26
RMII4_TXD1	RMII Transmit Data 1	O	AD29
RMII5_RXD0	RMII Receive Data 0	I	AJ20
RMII5_RXD1	RMII Receive Data 1	I	AG20
RMII5_TXD0	RMII Transmit Data 0	O	AH21
RMII5_TXD1	RMII Transmit Data 1	O	AJ21
RMII6_RXD0	RMII Receive Data 0	I	Y23
RMII6_RXD1	RMII Receive Data 1	I	AF21
RMII6_TXD0	RMII Transmit Data 0	O	AJ22
RMII6_TXD1	RMII Transmit Data 1	O	AH22
RMII7_RXD0	RMII Receive Data 0	I	T23
RMII7_RXD1	RMII Receive Data 1	I	R23
RMII7_TXD0	RMII Transmit Data 0	O	U28
RMII7_TXD1	RMII Transmit Data 1	O	V27
RMII8_RXD0	RMII Receive Data 0	I	W25
RMII8_RXD1	RMII Receive Data 1	I	W24
RMII8_TXD0	RMII Transmit Data 0	O	W27
RMII8_TXD1	RMII Transmit Data 1	O	V25
RMII_REF_CLK	RMII Reference Clock	I	AD18

5.3.12 ECAP

5.3.12.1 MAIN Domain

表 5-63. ECAP0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
ECAP0_IN_APWM_OUT	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	IO	P24, U2

表 5-64. ECAP1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
ECAP1_IN_APWM_OUT	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	IO	R24, V6

表 5-65. ECAP2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
ECAP2_IN_APWM_OUT	Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	IO	R28, V5

5.3.13 EQEP

5.3.13.1 MAIN Domain

表 5-66. EQEP0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EQEP0_A	EQEP Quadrature Input A	I	AC2
EQEP0_B	EQEP Quadrature Input B	I	AB1
EQEP0_I	EQEP Index	IO	AD5
EQEP0_S	EQEP Strobe	IO	AC4

表 5-67. EQEP1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EQEP1_A	EQEP Quadrature Input A	I	AD23
EQEP1_B	EQEP Quadrature Input B	I	AH24
EQEP1_I	EQEP Index	IO	AJ25
EQEP1_S	EQEP Strobe	IO	AG21

表 5-68. EQEP2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EQEP2_A	EQEP Quadrature Input A	I	T27
EQEP2_B	EQEP Quadrature Input B	I	T24
EQEP2_I	EQEP Index	IO	P23
EQEP2_S	EQEP Strobe	IO	R28

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5.3.14 EHRPWM

5.3.14.1 MAIN Domain

表 5-69. EHRPWM Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM_SOCA	EHRPWM Start of Conversion A	O	U25
EHRPWM_SOCB	EHRPWM Start of Conversion B	O	R23

表 5-70. EHRPWM0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM0_A	EHRPWM Output A	IO	V29
EHRPWM0_B	EHRPWM Output B	IO	V27
EHRPWM0_SYNCI	Sync Input to EHRPWM module from an external pin	I	U23
EHRPWM0_SYNCO	Sync Output to EHRPWM module to an external pin	O	U26
EHRPWM_TZn_IN0	EHRPWM Trip Zone Input 0 (active low)	I	V28

表 5-71. EHRPWM1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM1_A	EHRPWM Output A	IO	U28
EHRPWM1_B	EHRPWM Output B	IO	U29
EHRPWM_TZn_IN1	EHRPWM Trip Zone Input 1 (active low)	I	U25

表 5-72. EHRPWM2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM2_A	EHRPWM Output A	IO	U27
EHRPWM2_B	EHRPWM Output B	IO	U24
EHRPWM_TZn_IN2	EHRPWM Trip Zone Input 2 (active low)	I	R23

表 5-73. EHRPWM3 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM3_A	EHRPWM Output A	IO	V23
EHRPWM3_B	EHRPWM Output B	IO	W23
EHRPWM3_SYNCI	Sync Input to EHRPWM module from an external pin	I	W28
EHRPWM3_SYNCO	Sync Output to EHRPWM module to an external pin	O	V25
EHRPWM_TZn_IN3	EHRPWM Trip Zone Input 3 (active low)	I	W27

表 5-74. EHRPWM4 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM4_A	EHRPWM Output A	IO	W29
EHRPWM4_B	EHRPWM Output B	IO	W26
EHRPWM_TZn_IN4	EHRPWM Trip Zone Input 4 (active low)	I	Y29

表 5-75. EHRPWM5 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM5_A	EHRPWM Output A	IO	Y27

表 5-75. EHRPWM5 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EHRPWM5_B	EHRPWM Output B	IO	W24
EHRPWM_TZn_IN5	EHRPWM Trip Zone Input 5 (active low)	I	W25

5.3.15 USB

5.3.15.1 MAIN Domain

注

USB3 functionality is available on the SERDES pins. For more information, refer to セクション 5.3.16, *SERDES*.

表 5-76. USB0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
USB0_DM	USB 2.0 Differential Data (negative)	IO	AJ5
USB0_DP	USB 2.0 Differential Data (positive)	IO	AH6
USB0_DRVVBUS	USB VBUS control output (active high)	O	T25, T26, U6, V4, W3
USB0_ID	USB 2.0 Dual-Role Device Role Select	A	AC6
USB0_RCALIB(2)	Pin to connect to calibration resistor	A	AB6
USB0_VBUS(1)	USB Level-shifted VBUS Input	A	AC7

(1) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see セクション 8.3.4, *USB Design Guidelines*.
(2) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused.

表 5-77. USB1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
USB1_DM	USB 2.0 Differential Data (negative)	IO	AH7
USB1_DP	USB 2.0 Differential Data (positive)	IO	AJ6
USB1_DRVVBUS	USB VBUS control output (active high)	O	T25, T26, U6, V4, W3
USB1_ID	USB 2.0 Dual-Role Device Role Select	A	AD7
USB1_RCALIB(2)	Pin to connect to calibration resistor	A	AD9
USB1_VBUS(1)	USB Level-shifted VBUS Input	A	AD8

(1) An external resistor divider is required to limit the voltage applied to the device pin. For more information, see セクション 8.3.4, *USB Design Guidelines*.
(2) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused.

5.3.16 SERDES

5.3.16.1 MAIN Domain

表 5-78. SERDES0 Signal Descriptions

SIGNAL NAME [1] (2)	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PCIE0_CLKREQn	PCIE Clock Request Signal	IO	W2
PCIE_REFCLK0N	PCIE Reference Clock Input/Output (negative)	IO	AE17
PCIE_REFCLK0P	PCIE Reference Clock Input/Output (positive)	IO	AD16
SERDES0_REXT(1)	External Calibration Resistor	A	AE18
SERDES0_RX0_N	SERDES Differential Receive Data (negative)	I	AH19
SERDES0_RX0_P	SERDES Differential Receive Data (positive)	I	AJ18

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表 5-78. SERDES0 Signal Descriptions (続き)

SIGNAL NAME [1] (2)	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SERDES0_RX1_N	SERDES Differential Receive Data (negative)	I	AH18
SERDES0_RX1_P	SERDES Differential Receive Data (positive)	I	AJ17
SERDES0_TX0_N	SERDES Differential Transmit Data (negative)	O	AF19
SERDES0_TX0_P	SERDES Differential Transmit Data (positive)	O	AG18
SERDES0_TX1_N	SERDES Differential Transmit Data (negative)	O	AF18
SERDES0_TX1_P	SERDES Differential Transmit Data (positive)	O	AG17

(1) The external 3.01 kΩ ±1% resistor must be connected between this pin and VSS, even when the pin is unused.
(2) The functionality of these pins is controlled by SERDES0_LN[1:0]_CTRL LANE_FUNC_SEL.

表 5-79. SERDES1 Signal Descriptions

SIGNAL NAME [1] (2)	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PCIE1_CLKREQn	PCIE Clock Request Signal	IO	W1
PCIE_REFCLK1N	PCIE Reference Clock Input/Output (negative)	IO	AE14
PCIE_REFCLK1P	PCIE Reference Clock Input/Output (positive)	IO	AD15
SERDES1_REXT(1)	External Calibration Resistor	A	AE13
SERDES1_RX0_N	SERDES Differential Receive Data (negative)	I	AH15
SERDES1_RX0_P	SERDES Differential Receive Data (positive)	I	AJ14
SERDES1_RX1_N	SERDES Differential Receive Data (negative)	I	AH16
SERDES1_RX1_P	SERDES Differential Receive Data (positive)	I	AJ15
SERDES1_TX0_N	SERDES Differential Transmit Data (negative)	O	AF15
SERDES1_TX0_P	SERDES Differential Transmit Data (positive)	O	AG14
SERDES1_TX1_N	SERDES Differential Transmit Data (negative)	O	AF16
SERDES1_TX1_P	SERDES Differential Transmit Data (positive)	O	AG15

(1) The external 3.01 kΩ ±1% resistor must be connected between this pin and VSS, even when the pin is unused.
(2) The functionality of these pins is controlled by SERDES1_LN[1:0]_CTRL LANE_FUNC_SEL.

表 5-80. SERDES2 Signal Descriptions

SIGNAL NAME [1] (2)	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PCIE2_CLKREQn	PCIE Clock Request Signal	IO	P23
PCIE_REFCLK2N	PCIE Reference Clock Input/Output (negative)	IO	AE11
PCIE_REFCLK2P	PCIE Reference Clock Input/Output (positive)	IO	AD12
SERDES2_REXT(1)	External Calibration Resistor	A	AD13
SERDES2_RX0_N	SERDES Differential Receive Data (negative)	I	AH13
SERDES2_RX0_P	SERDES Differential Receive Data (positive)	I	AJ12
SERDES2_RX1_N	SERDES Differential Receive Data (negative)	I	AH12
SERDES2_RX1_P	SERDES Differential Receive Data (positive)	I	AJ11
SERDES2_TX0_N	SERDES Differential Transmit Data (negative)	O	AF13
SERDES2_TX0_P	SERDES Differential Transmit Data (positive)	O	AG12
SERDES2_TX1_N	SERDES Differential Transmit Data (negative)	O	AF12
SERDES2_TX1_P	SERDES Differential Transmit Data (positive)	O	AG11

(1) The external 3.01 kΩ ±1% resistor must be connected between this pin and VSS, even when the pin is unused.
(2) The functionality of these pins is controlled by SERDES2_LN[1:0]_CTRL LANE_FUNC_SEL.

表 5-81. SERDES3 Signal Descriptions

SIGNAL NAME [1] (2)	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PCIE3_CLKREQn	PCIE Clock Request Signal	IO	R28
PCIE_REFCLK3N	PCIE Reference Clock Input/Output (negative)	IO	AE9
PCIE_REFCLK3P	PCIE Reference Clock Input/Output (positive)	IO	AD10
SERDES3_REXT(1)	External Calibration Resistor	A	AE8
SERDES3_RX0_N	SERDES Differential Receive Data (negative)	I	AH9
SERDES3_RX0_P	SERDES Differential Receive Data (positive)	I	AJ8
SERDES3_RX1_N	SERDES Differential Receive Data (negative)	I	AH10
SERDES3_RX1_P	SERDES Differential Receive Data (positive)	I	AJ9
SERDES3_TX0_N	SERDES Differential Transmit Data (negative)	O	AF9
SERDES3_TX0_P	SERDES Differential Transmit Data (positive)	O	AG8
SERDES3_TX1_N	SERDES Differential Transmit Data (negative)	O	AF10
SERDES3_TX1_P	SERDES Differential Transmit Data (positive)	O	AG9

(1) The external 3.01 kΩ ±1% resistor must be connected between this pin and VSS, even when the pin is unused.
(2) The functionality of these pins is controlled by SERDES3_LN[1:0]_CTRL LANE_FUNC_SEL.

表 5-82. SERDES4 Signal Descriptions

SIGNAL NAME [1] (2)	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
SERDES4_REFCLK_N	SERDES Reference Differential Clock (negative)	IO	E7
SERDES4_REFCLK_P	SERDES Reference Differential Clock (positive)	IO	E8
SERDES4_REXT(1)	External Calibration Resistor	A	F9
SERDES4_RX0_N	SERDES Differential Receive Data (negative)	I	D9
SERDES4_RX0_P	SERDES Differential Receive Data (positive)	I	C10
SERDES4_RX1_N	SERDES Differential Receive Data (negative)	I	D8
SERDES4_RX1_P	SERDES Differential Receive Data (positive)	I	C9
SERDES4_RX2_N	SERDES Differential Receive Data (negative)	I	D6
SERDES4_RX2_P	SERDES Differential Receive Data (positive)	I	C7
SERDES4_RX3_N	SERDES Differential Receive Data (negative)	I	D5
SERDES4_RX3_P	SERDES Differential Receive Data (positive)	I	C6
SERDES4_TX0_N	SERDES Differential Transmit Data (negative)	O	B11
SERDES4_TX0_P	SERDES Differential Transmit Data (positive)	O	A12
SERDES4_TX1_N	SERDES Differential Transmit Data (negative)	O	B10
SERDES4_TX1_P	SERDES Differential Transmit Data (positive)	O	A11
SERDES4_TX2_N	SERDES Differential Transmit Data (negative)	O	B8
SERDES4_TX2_P	SERDES Differential Transmit Data (positive)	O	A9
SERDES4_TX3_N	SERDES Differential Transmit Data (negative)	O	B7
SERDES4_TX3_P	SERDES Differential Transmit Data (positive)	O	A8

(1) The external 3.01 kΩ ±1% resistor must be connected between this pin and VSS, even when the pin is unused.
(2) The functionality of these pins is controlled by SERDES4_LN[4:0]_CTRL LANE_FUNC_SEL.

5.3.17 OSPI

5.3.17.1 MCU Domain

表 5-83. OSPI0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_OSPI0_CLK	OSPI Clock	O	E20

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表 5-83. OSPI0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_OSPI0_DQS	OSPI Data Strobe (DQS) or Loopback Clock Input	I	D21
MCU_OSPI0_ECC_FAIL(1)	OSPI ECC Status	I	B23
MCU_OSPI0_LBCLKO	OSPI Loopback Clock Output	IO	C21
MCU_OSPI0_CSn0	OSPI Chip Select 0 (active low)	O	F19
MCU_OSPI0_CSn1	OSPI Chip Select 1 (active low)	O	E19
MCU_OSPI0_CSn2	OSPI Chip Select 2 (active low)	O	A23
MCU_OSPI0_CSn3	OSPI Chip Select 3 (active low)	O	B23
MCU_OSPI0_D0	OSPI Data 0	IO	D20
MCU_OSPI0_D1	OSPI Data 1	IO	G19
MCU_OSPI0_D2	OSPI Data 2	IO	G20
MCU_OSPI0_D3	OSPI Data 3	IO	F20
MCU_OSPI0_D4	OSPI Data 4	IO	F21
MCU_OSPI0_D5	OSPI Data 5	IO	E21
MCU_OSPI0_D6	OSPI Data 6	IO	B22
MCU_OSPI0_D7	OSPI Data 7	IO	G21
MCU_OSPI0_RESET_OUT0	OSPI Reset	O	A23
MCU_OSPI0_RESET_OUT1	OSPI Reset	O	E22

(1) An external pull-up resistor to corresponting power supply is recommended on this signal.

表 5-84. OSPI1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_OSPI1_CLK	OSPI Clock	O	F22
MCU_OSPI1_DQS	OSPI Data Strobe (DQS) or Loopback Clock Input	I	B23
MCU_OSPI1_LBCLKO	OSPI Loopback Clock Output	IO	A23
MCU_OSPI1_CSn0	OSPI Chip Select 0 (active low)	O	C22
MCU_OSPI1_CSn1	OSPI Chip Select 1 (active low)	O	E22
MCU_OSPI1_D0	OSPI Data 0	IO	D22
MCU_OSPI1_D1	OSPI Data 1	IO	G22
MCU_OSPI1_D2	OSPI Data 2	IO	D23
MCU_OSPI1_D3	OSPI Data 3	IO	C23

5.3.18 Hyperbus

5.3.18.1 MCU Domain

表 5-85. HYPERBUS0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_HYPERBUS0_CK	Hyperbus Differential Clock (positive)	O	E20
MCU_HYPERBUS0_CKn	Hyperbus Differential Clock (negative)	O	C21
MCU_HYPERBUS0_INTn	Hyperbus Interrupt (active low)	I	B23
MCU_HYPERBUS0_RESETn	Hyperbus Reset (active low) Output	O	E19
MCU_HYPERBUS0_RESETOn	Hyperbus Reset Status Indicator (active low) from Hyperbus Memory	I	A23
MCU_HYPERBUS0_RWDS	Hyperbus Read-Write Data Strobe	IO	D21
MCU_HYPERBUS0_WPn	Hyperbus Write Protect (not in use)	O	E22

表 5-85. HYPERBUS0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_HYPERBUS0_CSn0	Hyperbus Chip Select 0	O	F19
MCU_HYPERBUS0_CSn1	Hyperbus Chip Select 1	O	E22
MCU_HYPERBUS0_DQ0	Hyperbus Data 0	IO	D20
MCU_HYPERBUS0_DQ1	Hyperbus Data 1	IO	G19
MCU_HYPERBUS0_DQ2	Hyperbus Data 2	IO	G20
MCU_HYPERBUS0_DQ3	Hyperbus Data 3	IO	F20
MCU_HYPERBUS0_DQ4	Hyperbus Data 4	IO	F21
MCU_HYPERBUS0_DQ5	Hyperbus Data 5	IO	E21
MCU_HYPERBUS0_DQ6	Hyperbus Data 6	IO	B22
MCU_HYPERBUS0_DQ7	Hyperbus Data 7	IO	G21

5.3.19 GPMC

5.3.19.1 MAIN Domain

表 5-86. GPMC0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPMC0_FCLK_MUX	GPMC functional clock output selected through a mux logic	O	AB23
GPMC0_ADVn_ALE	GPMC Address Valid (active low) or Address Latch Enable	O	AG20
GPMC0_CLKOUT	GPMC clock generated for external synchronization	O	AB23
GPMC0_DIR	GPMC Data Bus Signal Direction Control	O	AJ23, W25
GPMC0_OEn_REn	GPMC Output Enable (active low) or Read Enable (active low)	O	AJ20
GPMC0_WEn	GPMC Write Enable (active low)	O	AD20
GPMC0_WPn	GPMC Flash Write Protect (active low)	O	AG21
GPMC0_A0	GPMC Address 0 Output. Only used to effectively address 8-bit data non-multiplexed memories	OZ	AA27
GPMC0_A1	GPMC address 1 Output in A/D non-multiplexed mode and Address 17 in A/D multiplexed mode	OZ	U23
GPMC0_A2	GPMC address 2 Output in A/D non-multiplexed mode and Address 18 in A/D multiplexed mode	OZ	U26
GPMC0_A3	GPMC address 3 Output in A/D non-multiplexed mode and Address 19 in A/D multiplexed mode	OZ	V28
GPMC0_A4	GPMC address 4 Output in A/D non-multiplexed mode and Address 20 in A/D multiplexed mode	OZ	V29
GPMC0_A5	GPMC address 5 Output in A/D non-multiplexed mode and Address 21 in A/D multiplexed mode	OZ	V27
GPMC0_A6	GPMC address 6 Output in A/D non-multiplexed mode and Address 22 in A/D multiplexed mode	OZ	U28
GPMC0_A7	GPMC address 7 Output in A/D non-multiplexed mode and Address 23 in A/D multiplexed mode	OZ	U29
GPMC0_A8	GPMC address 8 Output in A/D non-multiplexed mode and Address 24 in A/D multiplexed mode	OZ	U25
GPMC0_A9	GPMC address 9 Output in A/D non-multiplexed mode and Address 25 in A/D multiplexed mode	OZ	U27
GPMC0_A10	GPMC address 10 Output in A/D non-multiplexed mode and Address 26 in A/D multiplexed mode	OZ	U24

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表 5-86. GPMC0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPMC0_A11	GPMC address 11 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	R23
GPMC0_A12	GPMC address 12 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	T23
GPMC0_A13	GPMC address 13 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	Y28
GPMC0_A14	GPMC address 14 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	V23
GPMC0_A15	GPMC address 15 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	W23
GPMC0_A16	GPMC address 16 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	W28
GPMC0_A17	GPMC address 17 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	V25
GPMC0_A18	GPMC address 18 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	W27
GPMC0_A19	GPMC address 19 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	W29
GPMC0_A20	GPMC address 20 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	W26
GPMC0_A21	GPMC address 21 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	Y29
GPMC0_A22	GPMC address 22 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	Y27
GPMC0_A23	GPMC address 23 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AD27
GPMC0_A24	GPMC address 24 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AD29
GPMC0_A25	GPMC address 25 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AC26
GPMC0_A26	GPMC address 26 Output in A/D non-multiplexed mode and unused in A/D multiplexed mode	OZ	AG26
GPMC0_A27	GPMC address 27 in A/D non-multiplexed mode and Address 27 in A/D multiplexed mode	OZ	Y26
GPMC0_AD0	GPMC Data 0 Input/Output in A/D non-multiplexed mode and additionally Address 1 Output in A/D multiplexed mode	IO	AC29
GPMC0_AD1	GPMC Data 1 Input/Output in A/D non-multiplexed mode and additionally Address 2 Output in A/D multiplexed mode	IO	AC28
GPMC0_AD2	GPMC Data 2 Input/Output in A/D non-multiplexed mode and additionally Address 3 Output in A/D multiplexed mode	IO	AC27
GPMC0_AD3	GPMC Data 3 Input/Output in A/D non-multiplexed mode and additionally Address 4 Output in A/D multiplexed mode	IO	AB26
GPMC0_AD4	GPMC Data 4 Input/Output in A/D non-multiplexed mode and additionally Address 5 Output in A/D multiplexed mode	IO	AB25
GPMC0_AD5	GPMC Data 5 Input/Output in A/D non-multiplexed mode and additionally Address 6 Output in A/D multiplexed mode	IO	AB24

表 5-86. GPMC0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
GPMC0_AD6	GPMC Data 6 Input/Output in A/D non-multiplexed mode and additionally Address 7 Output in A/D multiplexed mode	IO	AB29
GPMC0_AD7	GPMC Data 7 Input/Output in A/D non-multiplexed mode and additionally Address 8 Output in A/D multiplexed mode	IO	AB28
GPMC0_AD8	GPMC Data 8 Input/Output in A/D non-multiplexed mode and additionally Address 9 Output in A/D multiplexed mode	IO	AB27
GPMC0_AD9	GPMC Data 9 Input/Output in A/D non-multiplexed mode and additionally Address 10 Output in A/D multiplexed mode	IO	AA24
GPMC0_AD10	GPMC Data 10 Input/Output in A/D non-multiplexed mode and additionally Address 11 Output in A/D multiplexed mode	IO	AA28
GPMC0_AD11	GPMC Data 11 Input/Output in A/D non-multiplexed mode and additionally Address 12 Output in A/D multiplexed mode	IO	Y24
GPMC0_AD12	GPMC Data 12 Input/Output in A/D non-multiplexed mode and additionally Address 13 Output in A/D multiplexed mode	IO	AA25
GPMC0_AD13	GPMC Data 13 Input/Output in A/D non-multiplexed mode and additionally Address 14 Output in A/D multiplexed mode	IO	Y25
GPMC0_AD14	GPMC Data 14 Input/Output in A/D non-multiplexed mode and additionally Address 15 Output in A/D multiplexed mode	IO	AA26
GPMC0_AD15	GPMC Data 15 Input/Output in A/D non-multiplexed mode and additionally Address 16 Output in A/D multiplexed mode	IO	AA29
GPMC0_BE0n_CLE	GPMC Lower-Byte Enable (active low) or Command Latch Enable	O	AD21
GPMC0_BE1n	GPMC Upper-Byte Enable (active low)	O	AC23, W24
GPMC0_CSn0	GPMC Chip Select 0 (active low)	O	AF21
GPMC0_CSn1	GPMC Chip Select 1 (active low)	O	Y23
GPMC0_CSn2	GPMC Chip Select 2 (active low)	O	AH23
GPMC0_CSn3	GPMC Chip Select 3 (active low)	O	AD22
GPMC0_WAIT0	GPMC External Indication of Wait	I	AG22
GPMC0_WAIT1	GPMC External Indication of Wait	I	AF22
GPMC0_WAIT2	GPMC External Indication of Wait	I	V24
GPMC0_WAIT3	GPMC External Indication of Wait	I	V26

5.3.20 MMC

5.3.20.1 MAIN Domain

表 5-87. MMC0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MMC0_CALPAD(1)	MMC/SD/SDIO Calibration Resistor	A	AE1
MMC0_CLK	MMC/SD/SDIO Clock	O	AF1
MMC0_CMD(2)	MMC/SD/SDIO Command	IO	AE3
MMC0_DS	MMC Data Strobe	IO	AE4

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表 5-87. MMC0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MMC0_DAT0[(2)]	MMC/SD/SDIO Data	IO	AG2
MMC0_DAT1[(2)]	MMC/SD/SDIO Data	IO	AH1
MMC0_DAT2[(2)]	MMC/SD/SDIO Data	IO	AG3
MMC0_DAT3[(2)]	MMC/SD/SDIO Data	IO	AF4
MMC0_DAT4[(2)]	MMC/SD/SDIO Data	IO	AE5
MMC0_DAT5[(2)]	MMC/SD/SDIO Data	IO	AF3
MMC0_DAT6[(2)]	MMC/SD/SDIO Data	IO	AG1
MMC0_DAT7[(2)]	MMC/SD/SDIO Data	IO	AF2

(1) An external 10 kΩ ±1% resistor must be connected between this pin and VSS. No external voltage should be applied to this pin.
(2) An external pull-up of 10 kΩ ~ 50 kΩ ±1% resistor, as specified in the specification, must be connected to this ball to ensure proper operation.

表 5-88. MMC1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MMC1_CLK[(1)]	MMC/SD/SDIO Clock	IO	P25
MMC1_CMD	MMC/SD/SDIO Command	IO	R29
MMC1_SDCD[(2)]	SD Card Detect	I	P23
MMC1_SDWP	SD Write Protect	I	R28
MMC1_DAT0	MMC/SD/SDIO Data	IO	R24
MMC1_DAT1	MMC/SD/SDIO Data	IO	P24
MMC1_DAT2	MMC/SD/SDIO Data	IO	R25
MMC1_DAT3	MMC/SD/SDIO Data	IO	R26

(1) For MMC1_CLK signal to work properly, the RXACTIVE bit of the CTRLMMR_PADCONFIG171 register should be set to 0x1 because of retiming purposes.
(2) For ROM boot from MMC1 interface to work properly, the MMC1_SDCD pin should be pulled low externally with a resistor to indicate an SD Card/Memory device is present.

表 5-89. MMC2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MMC2_CLK[(1)]	MMC/SD/SDIO Clock	IO	T26
MMC2_CMD	MMC/SD/SDIO Command	IO	T25
MMC2_SDCD[(2)]	SD Card Detect	I	W2
MMC2_SDWP	SD Write Protect	I	W1
MMC2_DAT0	MMC/SD/SDIO Data	IO	T24
MMC2_DAT1	MMC/SD/SDIO Data	IO	T27
MMC2_DAT2	MMC/SD/SDIO Data	IO	T29
MMC2_DAT3	MMC/SD/SDIO Data	IO	T28

(1) For MMC2_CLK signal to work properly, the RXACTIVE bit of the CTRLMMR_PADCONFIG172 register should be set to 0x1 because of retiming purposes.
(2) For MMC2 module to work properly, the MMC2_SDCD pin should be pulled low to indicate an SD Card/Memory device is present.

5.3.21 CPTS

注

Some CPTS signals are connected directly to CPTS modules within the device. Other CPTS signals are connected to the Time Sync Router and fanned out to peripherals linked to the router. Input signals are sent to the peripherals while output signals are sourced from the peripherals. For more information, see the Time Sync and Compare Events section in the Time Sync chapter in the device TRM.

5.3.21.1 MCU Domain

表 5-90. CPTS0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_CPTS0_RFT_CLK	CPTS Reference Clock	I	H26
MCU_CPTS0_TS_COMP	Time Stamp Counter Compare from MCU_CPSW0_CPTS0	O	G26
MCU_CPTS0_TS_SYNC	Time Stamp Counter Bit from MCU_CPSW0_CPTS0	O	G27
MCU_CPTS0_HW1TSPUSH	Hardware Time Stamp Push 1 input to Time Sync Router and MCU_CPSW0_CPTS0	I	F29
MCU_CPTS0_HW2TSPUSH	Hardware Time Stamp Push 2 input to Time Sync Router and MCU_CPSW0_CPTS0	I	G28

5.3.21.2 MAIN Domain

表 5-91. CPTS0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
CPTS0_RFT_CLK	CPTS Reference Clock	I	U2
CPTS0_TS_COMP	Time Stamp Counter Compare from NAVSS0_CPTS0	O	Y4
CPTS0_TS_SYNC	Time Stamp Counter Bit from NAVSS0_CPTS0	O	W4
CPTS0_HW1TSPUSH	Hardware Time Stamp Push input to Time Sync Router	I	T28, Y6
CPTS0_HW2TSPUSH	Hardware Time Stamp Push input to Time Sync Router	I	AA6, T29
SYNC0_OUT	Time Stamp Generator Bit 0 from Time Sync Router	O	U2
SYNC1_OUT	Time Stamp Generator Bit 1 from Time Sync Router	O	U3
SYNC2_OUT	Time Stamp Generator Bit 2 from Time Sync Router	O	V28
SYNC3_OUT	Time Stamp Generator Bit 3 from Time Sync Router	O	V29

5.3.22 UFS

5.3.22.1 MAIN Domain

表 5-92. UFS0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UFS0_REF_CLK	UFS Reference Clock	O	AE6
UFS0_RSTn	UFS Reset Out	O	AD6
UFS0_RX_DN0	UFS Lane 0 Differential Receive Data (negative)	I	AH3
UFS0_RX_DP0	UFS Lane 0 Differential Receive Data (positive)	I	AJ2
UFS0_RX_DN1	UFS Lane 1 Differential Receive Data (negative)	I	AH4
UFS0_RX_DP1	UFS Lane 1 Differential Receive Data (positive)	I	AJ3
UFS0_TX_DN0	UFS Lane 0 Differential Transmit Data (negative)	O	AG6
UFS0_TX_DP0	UFS Lane 0 Differential Transmit Data (positive)	O	AF7

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表 5-92. UFS0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
UFS0_TX_DN1	UFS Lane 1 Differential Transmit Data (negative)	O	AG5
UFS0_TX_DP1	UFS Lane 1 Differential Transmit Data (positive)	O	AF6

5.3.23 PRU_ICSSG [Currently Not Supported]

5.3.23.1 MAIN Domain

表 5-93. PRU_ICSSG0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG0_ECAP0_IN_APWM_OUT	PRU_ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	IO	AB29
PRG0_ECAP0_SYNC_IN	PRU_ICSSG ECAP Sync Input	I	AC28
PRG0_ECAP0_SYNC_OUT	PRU_ICSSG ECAP Sync Output	O	AB24
PRG0_IEP0_EDIO_OUTVALID	PRU_ICSSG Industrial Ethernet Digital I/O Outvalid	O	Y3
PRG0_IEP0_EDC_LATCH_IN0	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AB29, Y3
PRG0_IEP0_EDC_LATCH_IN1	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AC28, P23
PRG0_IEP0_EDC_SYNC_OUT0	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AB28, Y1
PRG0_IEP0_EDC_SYNC_OUT1	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AB24, R28
PRG0_IEP0_EDIO_DATA_IN_OUT28	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/ Output	IO	AB26
PRG0_IEP0_EDIO_DATA_IN_OUT29	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/ Output	IO	AB25
PRG0_IEP0_EDIO_DATA_IN_OUT30	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/ Output	IO	Y24
PRG0_IEP0_EDIO_DATA_IN_OUT31	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/ Output	IO	AA25
PRG0_IEP1_EDC_LATCH_IN0	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AA26, Y5
PRG0_IEP1_EDC_LATCH_IN1	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AA24, T27
PRG0_IEP1_EDC_SYNC_OUT0	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AA29, Y2
PRG0_IEP1_EDC_SYNC_OUT1	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	T24, Y25
PRG0_MDIO0_MDC	PRU_ICSSG MDIO Clock	O	AA27
PRG0_MDIO0_MDIO	PRU_ICSSG MDIO Data	IO	Y26
PRG0_PRU0_GPI0	PRU_ICSSG PRU Data Input	I	AF28
PRG0_PRU0_GPI1	PRU_ICSSG PRU Data Input	I	AE28
PRG0_PRU0_GPI2	PRU_ICSSG PRU Data Input	I	AE27
PRG0_PRU0_GPI3	PRU_ICSSG PRU Data Input	I	AD26
PRG0_PRU0_GPI4	PRU_ICSSG PRU Data Input	I	AD25
PRG0_PRU0_GPI5	PRU_ICSSG PRU Data Input	I	AC29
PRG0_PRU0_GPI6	PRU_ICSSG PRU Data Input	I	AE26
PRG0_PRU0_GPI7	PRU_ICSSG PRU Data Input	I	AC28
PRG0_PRU0_GPI8	PRU_ICSSG PRU Data Input	I	AC27

表 5-93. PRU_ICSSG0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG0_PRU0_GPI9	PRU_ICSSG PRU Data Input	I	AB26
PRG0_PRU0_GPI10	PRU_ICSSG PRU Data Input	I	AB25
PRG0_PRU0_GPI11	PRU_ICSSG PRU Data Input	I	AJ28
PRG0_PRU0_GPI12	PRU_ICSSG PRU Data Input	I	AH27
PRG0_PRU0_GPI13	PRU_ICSSG PRU Data Input	I	AH29
PRG0_PRU0_GPI14	PRU_ICSSG PRU Data Input	I	AG28
PRG0_PRU0_GPI15	PRU_ICSSG PRU Data Input	I	AG27
PRG0_PRU0_GPI16	PRU_ICSSG PRU Data Input	I	AH28
PRG0_PRU0_GPI17	PRU_ICSSG PRU Data Input	I	AB24
PRG0_PRU0_GPI18	PRU_ICSSG PRU Data Input	I	AB29
PRG0_PRU0_GPI19	PRU_ICSSG PRU Data Input	I	AB28
PRG0_PRU0_GPO0	PRU_ICSSG PRU Data Output	IO	AF28
PRG0_PRU0_GPO1	PRU_ICSSG PRU Data Output	IO	AE28
PRG0_PRU0_GPO2	PRU_ICSSG PRU Data Output	IO	AE27
PRG0_PRU0_GPO3	PRU_ICSSG PRU Data Output	IO	AD26
PRG0_PRU0_GPO4	PRU_ICSSG PRU Data Output	IO	AD25
PRG0_PRU0_GPO5	PRU_ICSSG PRU Data Output	IO	AC29
PRG0_PRU0_GPO6	PRU_ICSSG PRU Data Output	IO	AE26
PRG0_PRU0_GPO7	PRU_ICSSG PRU Data Output	IO	AC28
PRG0_PRU0_GPO8	PRU_ICSSG PRU Data Output	IO	AC27
PRG0_PRU0_GPO9	PRU_ICSSG PRU Data Output	IO	AB26
PRG0_PRU0_GPO10	PRU_ICSSG PRU Data Output	IO	AB25
PRG0_PRU0_GPO11	PRU_ICSSG PRU Data Output	IO	AJ28
PRG0_PRU0_GPO12	PRU_ICSSG PRU Data Output	IO	AH27
PRG0_PRU0_GPO13	PRU_ICSSG PRU Data Output	IO	AH29
PRG0_PRU0_GPO14	PRU_ICSSG PRU Data Output	IO	AG28
PRG0_PRU0_GPO15	PRU_ICSSG PRU Data Output	IO	AG27
PRG0_PRU0_GPO16	PRU_ICSSG PRU Data Output	IO	AH28
PRG0_PRU0_GPO17	PRU_ICSSG PRU Data Output	IO	AB24
PRG0_PRU0_GPO18	PRU_ICSSG PRU Data Output	IO	AB29
PRG0_PRU0_GPO19	PRU_ICSSG PRU Data Output	IO	AB28
PRG0_PRU1_GPI0	PRU_ICSSG PRU Data Input	I	AE29
PRG0_PRU1_GPI1	PRU_ICSSG PRU Data Input	I	AD28
PRG0_PRU1_GPI2	PRU_ICSSG PRU Data Input	I	AD27
PRG0_PRU1_GPI3	PRU_ICSSG PRU Data Input	I	AC25
PRG0_PRU1_GPI4	PRU_ICSSG PRU Data Input	I	AD29
PRG0_PRU1_GPI5	PRU_ICSSG PRU Data Input	I	AB27
PRG0_PRU1_GPI6	PRU_ICSSG PRU Data Input	I	AC26
PRG0_PRU1_GPI7	PRU_ICSSG PRU Data Input	I	AA24
PRG0_PRU1_GPI8	PRU_ICSSG PRU Data Input	I	AA28
PRG0_PRU1_GPI9	PRU_ICSSG PRU Data Input	I	Y24
PRG0_PRU1_GPI10	PRU_ICSSG PRU Data Input	I	AA25
PRG0_PRU1_GPI11	PRU_ICSSG PRU Data Input	I	AG26
PRG0_PRU1_GPI12	PRU_ICSSG PRU Data Input	I	AF27

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表 5-93. PRU_ICSSG0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG0_PRU1_GPI13	PRU_ICSSG PRU Data Input	I	AF26
PRG0_PRU1_GPI14	PRU_ICSSG PRU Data Input	I	AE25
PRG0_PRU1_GPI15	PRU_ICSSG PRU Data Input	I	AF29
PRG0_PRU1_GPI16	PRU_ICSSG PRU Data Input	I	AG29
PRG0_PRU1_GPI17	PRU_ICSSG PRU Data Input	I	Y25
PRG0_PRU1_GPI18	PRU_ICSSG PRU Data Input	I	AA26
PRG0_PRU1_GPI19	PRU_ICSSG PRU Data Input	I	AA29
PRG0_PRU1_GPO0	PRU_ICSSG PRU Data Output	IO	AE29
PRG0_PRU1_GPO1	PRU_ICSSG PRU Data Output	IO	AD28
PRG0_PRU1_GPO2	PRU_ICSSG PRU Data Output	IO	AD27
PRG0_PRU1_GPO3	PRU_ICSSG PRU Data Output	IO	AC25
PRG0_PRU1_GPO4	PRU_ICSSG PRU Data Output	IO	AD29
PRG0_PRU1_GPO5	PRU_ICSSG PRU Data Output	IO	AB27
PRG0_PRU1_GPO6	PRU_ICSSG PRU Data Output	IO	AC26
PRG0_PRU1_GPO7	PRU_ICSSG PRU Data Output	IO	AA24
PRG0_PRU1_GPO8	PRU_ICSSG PRU Data Output	IO	AA28
PRG0_PRU1_GPO9	PRU_ICSSG PRU Data Output	IO	Y24
PRG0_PRU1_GPO10	PRU_ICSSG PRU Data Output	IO	AA25
PRG0_PRU1_GPO11	PRU_ICSSG PRU Data Output	IO	AG26
PRG0_PRU1_GPO12	PRU_ICSSG PRU Data Output	IO	AF27
PRG0_PRU1_GPO13	PRU_ICSSG PRU Data Output	IO	AF26
PRG0_PRU1_GPO14	PRU_ICSSG PRU Data Output	IO	AE25
PRG0_PRU1_GPO15	PRU_ICSSG PRU Data Output	IO	AF29
PRG0_PRU1_GPO16	PRU_ICSSG PRU Data Output	IO	AG29
PRG0_PRU1_GPO17	PRU_ICSSG PRU Data Output	IO	Y25
PRG0_PRU1_GPO18	PRU_ICSSG PRU Data Output	IO	AA26
PRG0_PRU1_GPO19	PRU_ICSSG PRU Data Output	IO	AA29
PRG0_PWM0_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AB29
PRG0_PWM0_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AB28
PRG0_PWM1_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AA26
PRG0_PWM1_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AA29
PRG0_PWM2_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AA25
PRG0_PWM2_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AA28
PRG0_PWM3_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AB26
PRG0_PWM3_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AJ28
PRG0_PWM0_A0	PRU_ICSSG PWM Output A	IO	AH27
PRG0_PWM0_A1	PRU_ICSSG PWM Output A	IO	AG28
PRG0_PWM0_A2	PRU_ICSSG PWM Output A	IO	AH28
PRG0_PWM0_B0	PRU_ICSSG PWM Output B	IO	AH29
PRG0_PWM0_B1	PRU_ICSSG PWM Output B	IO	AG27
PRG0_PWM0_B2	PRU_ICSSG PWM Output B	IO	AB24
PRG0_PWM1_A0	PRU_ICSSG PWM Output A	IO	AF27
PRG0_PWM1_A1	PRU_ICSSG PWM Output A	IO	AE25
PRG0_PWM1_A2	PRU_ICSSG PWM Output A	IO	AG29

表 5-93. PRU_ICSSG0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG0_PWM1_B0	PRU_ICSSG PWM Output B	IO	AF26
PRG0_PWM1_B1	PRU_ICSSG PWM Output B	IO	AF29
PRG0_PWM1_B2	PRU_ICSSG PWM Output B	IO	Y25
PRG0_PWM2_A0	PRU_ICSSG PWM Output A	IO	AE27
PRG0_PWM2_A1	PRU_ICSSG PWM Output A	IO	AC27
PRG0_PWM2_A2	PRU_ICSSG PWM Output A	IO	AD27
PRG0_PWM2_B0	PRU_ICSSG PWM Output B	IO	AD25
PRG0_PWM2_B1	PRU_ICSSG PWM Output B	IO	AB25
PRG0_PWM2_B2	PRU_ICSSG PWM Output B	IO	AD29
PRG0_PWM3_A0	PRU_ICSSG PWM Output A	IO	AF28
PRG0_PWM3_A1	PRU_ICSSG PWM Output A	IO	AE26
PRG0_PWM3_A2	PRU_ICSSG PWM Output A	IO	AD26
PRG0_PWM3_B0	PRU_ICSSG PWM Output B	IO	AE28
PRG0_PWM3_B1	PRU_ICSSG PWM Output B	IO	AC28
PRG0_PWM3_B2	PRU_ICSSG PWM Output B	IO	AC29
PRG0_RGMII1_RXC	PRU_ICSSG RGMII Receive Clock	I	AE26
PRG0_RGMII1_RX_CTL	PRU_ICSSG RGMII Receive Control	I	AD25
PRG0_RGMII1_TXC	PRU_ICSSG RGMII Transmit Clock	IO	AH28
PRG0_RGMII1_TX_CTL	PRU_ICSSG RGMII Transmit Control	O	AG27
PRG0_RGMII2_RXC	PRU_ICSSG RGMII Receive Clock	I	AC26
PRG0_RGMII2_RX_CTL	PRU_ICSSG RGMII Receive Control	I	AD29
PRG0_RGMII2_TXC	PRU_ICSSG RGMII Transmit Clock	IO	AG29
PRG0_RGMII2_TX_CTL	PRU_ICSSG RGMII Transmit Control	O	AF29
PRG0_RGMII1_RD0	PRU_ICSSG RGMII Receive Data	I	AF28
PRG0_RGMII1_RD1	PRU_ICSSG RGMII Receive Data	I	AE28
PRG0_RGMII1_RD2	PRU_ICSSG RGMII Receive Data	I	AE27
PRG0_RGMII1_RD3	PRU_ICSSG RGMII Receive Data	I	AD26
PRG0_RGMII1_TD0	PRU_ICSSG RGMII Transmit Data	O	AJ28
PRG0_RGMII1_TD1	PRU_ICSSG RGMII Transmit Data	O	AH27
PRG0_RGMII1_TD2	PRU_ICSSG RGMII Transmit Data	O	AH29
PRG0_RGMII1_TD3	PRU_ICSSG RGMII Transmit Data	O	AG28
PRG0_RGMII2_RD0	PRU_ICSSG RGMII Receive Data	I	AE29
PRG0_RGMII2_RD1	PRU_ICSSG RGMII Receive Data	I	AD28
PRG0_RGMII2_RD2	PRU_ICSSG RGMII Receive Data	I	AD27
PRG0_RGMII2_RD3	PRU_ICSSG RGMII Receive Data	I	AC25
PRG0_RGMII2_TD0	PRU_ICSSG RGMII Transmit Data	O	AG26
PRG0_RGMII2_TD1	PRU_ICSSG RGMII Transmit Data	O	AF27
PRG0_RGMII2_TD2	PRU_ICSSG RGMII Transmit Data	O	AF26
PRG0_RGMII2_TD3	PRU_ICSSG RGMII Transmit Data	O	AE25
PRG0_UART0_CTSn	PRU_ICSSG UART Clear to Send (active low)	I	AB26
PRG0_UART0_RTSn	PRU_ICSSG UART Request to Send (active low)	O	AB25
PRG0_UART0_RXD	PRU_ICSSG UART Receive Data	I	Y24
PRG0_UART0_TXD	PRU_ICSSG UART Transmit Data	O	AA25

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表 5-94. PRU_ICSSG1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG1_ECAP0_IN_APWM_OUT	PRU_ICSSG Enhanced Capture (ECAP) Input or Auxiliary PWM (APWM) Ouput	IO	AH22
PRG1_ECAP0_SYNC_IN	PRU_ICSSG ECAP Sync Input	I	AJ22
PRG1_ECAP0_SYNC_OUT	PRU_ICSSG ECAP Sync Output	O	AC22
PRG1_IEP0_EDIO_OUTVALID	PRU_ICSSG Industrial Ethernet Digital I/O Outvalid	O	Y4
PRG1_IEP0_EDC_LATCH_IN0	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AE21
PRG1_IEP0_EDC_LATCH_IN1	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AE20
PRG1_IEP0_EDC_SYNC_OUT0	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AH21
PRG1_IEP0_EDC_SYNC_OUT1	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AJ21
PRG1_IEP0_EDIO_DATA_IN_OUT28	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/ Output	IO	AG20
PRG1_IEP0_EDIO_DATA_IN_OUT29	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/ Output	IO	AD21
PRG1_IEP0_EDIO_DATA_IN_OUT30	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/ Output	IO	AF21
PRG1_IEP0_EDIO_DATA_IN_OUT31	PRU_ICSSG Industrial Ethernet Digital I/O Data Input/ Output	IO	AB23
PRG1_IEP1_EDC_LATCH_IN0	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AJ22
PRG1_IEP1_EDC_LATCH_IN1	PRU_ICSSG Industrial Ethernet Distributed Clock Latch Input	I	AC21
PRG1_IEP1_EDC_SYNC_OUT0	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AH22
PRG1_IEP1_EDC_SYNC_OUT1	PRU_ICSSG Industrial Ethernet Distributed Clock Sync Output	O	AC22
PRG1_MDIO0_MDC	PRU_ICSSG MDIO Clock	O	AD18
PRG1_MDIO0_MDIO	PRU_ICSSG MDIO Data	IO	AD19
PRG1_PRU0_GPI0	PRU_ICSSG PRU Data Input	I	AC23
PRG1_PRU0_GPI1	PRU_ICSSG PRU Data Input	I	AG22
PRG1_PRU0_GPI2	PRU_ICSSG PRU Data Input	I	AF22
PRG1_PRU0_GPI3	PRU_ICSSG PRU Data Input	I	AJ23
PRG1_PRU0_GPI4	PRU_ICSSG PRU Data Input	I	AH23
PRG1_PRU0_GPI5	PRU_ICSSG PRU Data Input	I	AD20
PRG1_PRU0_GPI6	PRU_ICSSG PRU Data Input	I	AD22
PRG1_PRU0_GPI7	PRU_ICSSG PRU Data Input	I	AE20
PRG1_PRU0_GPI8	PRU_ICSSG PRU Data Input	I	AJ20
PRG1_PRU0_GPI9	PRU_ICSSG PRU Data Input	I	AG20
PRG1_PRU0_GPI10	PRU_ICSSG PRU Data Input	I	AD21
PRG1_PRU0_GPI11	PRU_ICSSG PRU Data Input	I	AF24
PRG1_PRU0_GPI12	PRU_ICSSG PRU Data Input	I	AJ24
PRG1_PRU0_GPI13	PRU_ICSSG PRU Data Input	I	AG24
PRG1_PRU0_GPI14	PRU_ICSSG PRU Data Input	I	AD24
PRG1_PRU0_GPI15	PRU_ICSSG PRU Data Input	I	AC24
PRG1_PRU0_GPI16	PRU_ICSSG PRU Data Input	I	AE24

表 5-94. PRU_ICSSG1 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG1_PRU0_GPI17	PRU_ICSSG PRU Data Input	I	AJ21
PRG1_PRU0_GPI18	PRU_ICSSG PRU Data Input	I	AE21
PRG1_PRU0_GPI19	PRU_ICSSG PRU Data Input	I	AH21
PRG1_PRU0_GPO0	PRU_ICSSG PRU Data Output	IO	AC23
PRG1_PRU0_GPO1	PRU_ICSSG PRU Data Output	IO	AG22
PRG1_PRU0_GPO2	PRU_ICSSG PRU Data Output	IO	AF22
PRG1_PRU0_GPO3	PRU_ICSSG PRU Data Output	IO	AJ23
PRG1_PRU0_GPO4	PRU_ICSSG PRU Data Output	IO	AH23
PRG1_PRU0_GPO5	PRU_ICSSG PRU Data Output	IO	AD20
PRG1_PRU0_GPO6	PRU_ICSSG PRU Data Output	IO	AD22
PRG1_PRU0_GPO7	PRU_ICSSG PRU Data Output	IO	AE20
PRG1_PRU0_GPO8	PRU_ICSSG PRU Data Output	IO	AJ20
PRG1_PRU0_GPO9	PRU_ICSSG PRU Data Output	IO	AG20
PRG1_PRU0_GPO10	PRU_ICSSG PRU Data Output	IO	AD21
PRG1_PRU0_GPO11	PRU_ICSSG PRU Data Output	IO	AF24
PRG1_PRU0_GPO12	PRU_ICSSG PRU Data Output	IO	AJ24
PRG1_PRU0_GPO13	PRU_ICSSG PRU Data Output	IO	AG24
PRG1_PRU0_GPO14	PRU_ICSSG PRU Data Output	IO	AD24
PRG1_PRU0_GPO15	PRU_ICSSG PRU Data Output	IO	AC24
PRG1_PRU0_GPO16	PRU_ICSSG PRU Data Output	IO	AE24
PRG1_PRU0_GPO17	PRU_ICSSG PRU Data Output	IO	AJ21
PRG1_PRU0_GPO18	PRU_ICSSG PRU Data Output	IO	AE21
PRG1_PRU0_GPO19	PRU_ICSSG PRU Data Output	IO	AH21
PRG1_PRU1_GPI0	PRU_ICSSG PRU Data Input	I	AE22
PRG1_PRU1_GPI1	PRU_ICSSG PRU Data Input	I	AG23
PRG1_PRU1_GPI2	PRU_ICSSG PRU Data Input	I	AF23
PRG1_PRU1_GPI3	PRU_ICSSG PRU Data Input	I	AD23
PRG1_PRU1_GPI4	PRU_ICSSG PRU Data Input	I	AH24
PRG1_PRU1_GPI5	PRU_ICSSG PRU Data Input	I	AG21
PRG1_PRU1_GPI6	PRU_ICSSG PRU Data Input	I	AE23
PRG1_PRU1_GPI7	PRU_ICSSG PRU Data Input	I	AC21
PRG1_PRU1_GPI8	PRU_ICSSG PRU Data Input	I	Y23
PRG1_PRU1_GPI9	PRU_ICSSG PRU Data Input	I	AF21
PRG1_PRU1_GPI10	PRU_ICSSG PRU Data Input	I	AB23
PRG1_PRU1_GPI11	PRU_ICSSG PRU Data Input	I	AJ25
PRG1_PRU1_GPI12	PRU_ICSSG PRU Data Input	I	AH25
PRG1_PRU1_GPI13	PRU_ICSSG PRU Data Input	I	AG25
PRG1_PRU1_GPI14	PRU_ICSSG PRU Data Input	I	AH26
PRG1_PRU1_GPI15	PRU_ICSSG PRU Data Input	I	AJ27
PRG1_PRU1_GPI16	PRU_ICSSG PRU Data Input	I	AJ26
PRG1_PRU1_GPI17	PRU_ICSSG PRU Data Input	I	AC22
PRG1_PRU1_GPI18	PRU_ICSSG PRU Data Input	I	AJ22
PRG1_PRU1_GPI19	PRU_ICSSG PRU Data Input	I	AH22
PRG1_PRU1_GPO0	PRU_ICSSG PRU Data Output	IO	AE22

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表 5-94. PRU_ICSSG1 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG1_PRU1_GPO1	PRU_ICSSG PRU Data Output	IO	AG23
PRG1_PRU1_GPO2	PRU_ICSSG PRU Data Output	IO	AF23
PRG1_PRU1_GPO3	PRU_ICSSG PRU Data Output	IO	AD23
PRG1_PRU1_GPO4	PRU_ICSSG PRU Data Output	IO	AH24
PRG1_PRU1_GPO5	PRU_ICSSG PRU Data Output	IO	AG21
PRG1_PRU1_GPO6	PRU_ICSSG PRU Data Output	IO	AE23
PRG1_PRU1_GPO7	PRU_ICSSG PRU Data Output	IO	AC21
PRG1_PRU1_GPO8	PRU_ICSSG PRU Data Output	IO	Y23
PRG1_PRU1_GPO9	PRU_ICSSG PRU Data Output	IO	AF21
PRG1_PRU1_GPO10	PRU_ICSSG PRU Data Output	IO	AB23
PRG1_PRU1_GPO11	PRU_ICSSG PRU Data Output	IO	AJ25
PRG1_PRU1_GPO12	PRU_ICSSG PRU Data Output	IO	AH25
PRG1_PRU1_GPO13	PRU_ICSSG PRU Data Output	IO	AG25
PRG1_PRU1_GPO14	PRU_ICSSG PRU Data Output	IO	AH26
PRG1_PRU1_GPO15	PRU_ICSSG PRU Data Output	IO	AJ27
PRG1_PRU1_GPO16	PRU_ICSSG PRU Data Output	IO	AJ26
PRG1_PRU1_GPO17	PRU_ICSSG PRU Data Output	IO	AC22
PRG1_PRU1_GPO18	PRU_ICSSG PRU Data Output	IO	AJ22
PRG1_PRU1_GPO19	PRU_ICSSG PRU Data Output	IO	AH22
PRG1_PWM0_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AE21
PRG1_PWM0_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AH21
PRG1_PWM1_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AJ22
PRG1_PWM1_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AH22
PRG1_PWM2_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AB23
PRG1_PWM2_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	Y23
PRG1_PWM3_TZ_IN	PRU_ICSSG PWM Trip Zone Input	I	AG20
PRG1_PWM3_TZ_OUT	PRU_ICSSG PWM Trip Zone Output	O	AF24
PRG1_PWM0_A0	PRU_ICSSG PWM Output A	IO	AJ24
PRG1_PWM0_A1	PRU_ICSSG PWM Output A	IO	AD24
PRG1_PWM0_A2	PRU_ICSSG PWM Output A	IO	AE24
PRG1_PWM0_B0	PRU_ICSSG PWM Output B	IO	AG24
PRG1_PWM0_B1	PRU_ICSSG PWM Output B	IO	AC24
PRG1_PWM0_B2	PRU_ICSSG PWM Output B	IO	AJ21
PRG1_PWM1_A0	PRU_ICSSG PWM Output A	IO	AH25
PRG1_PWM1_A1	PRU_ICSSG PWM Output A	IO	AH26
PRG1_PWM1_A2	PRU_ICSSG PWM Output A	IO	AJ26
PRG1_PWM1_B0	PRU_ICSSG PWM Output B	IO	AG25
PRG1_PWM1_B1	PRU_ICSSG PWM Output B	IO	AJ27
PRG1_PWM1_B2	PRU_ICSSG PWM Output B	IO	AC22
PRG1_PWM2_A0	PRU_ICSSG PWM Output A	IO	AF22
PRG1_PWM2_A1	PRU_ICSSG PWM Output A	IO	AJ20
PRG1_PWM2_A2	PRU_ICSSG PWM Output A	IO	AF23
PRG1_PWM2_B0	PRU_ICSSG PWM Output B	IO	AH23
PRG1_PWM2_B1	PRU_ICSSG PWM Output B	IO	AD21

表 5-94. PRU_ICSSG1 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
PRG1_PWM2_B2	PRU_ICSSG PWM Output B	IO	AH24
PRG1_PWM3_A0	PRU_ICSSG PWM Output A	IO	AC23
PRG1_PWM3_A1	PRU_ICSSG PWM Output A	IO	AD22
PRG1_PWM3_A2	PRU_ICSSG PWM Output A	IO	AJ23
PRG1_PWM3_B0	PRU_ICSSG PWM Output B	IO	AG22
PRG1_PWM3_B1	PRU_ICSSG PWM Output B	IO	AE20
PRG1_PWM3_B2	PRU_ICSSG PWM Output B	IO	AD20
PRG1_RGMII1_RXC	PRU_ICSSG RGMII Receive Clock	I	AD22
PRG1_RGMII1_RX_CTL	PRU_ICSSG RGMII Receive Control	I	AH23
PRG1_RGMII1_TXC	PRU_ICSSG RGMII Transmit Clock	IO	AE24
PRG1_RGMII1_TX_CTL	PRU_ICSSG RGMII Transmit Control	O	AC24
PRG1_RGMII2_RXC	PRU_ICSSG RGMII Receive Clock	I	AE23
PRG1_RGMII2_RX_CTL	PRU_ICSSG RGMII Receive Control	I	AH24
PRG1_RGMII2_TXC	PRU_ICSSG RGMII Transmit Clock	IO	AJ26
PRG1_RGMII2_TX_CTL	PRU_ICSSG RGMII Transmit Control	O	AJ27
PRG1_RGMII1_RD0	PRU_ICSSG RGMII Receive Data	I	AC23
PRG1_RGMII1_RD1	PRU_ICSSG RGMII Receive Data	I	AG22
PRG1_RGMII1_RD2	PRU_ICSSG RGMII Receive Data	I	AF22
PRG1_RGMII1_RD3	PRU_ICSSG RGMII Receive Data	I	AJ23
PRG1_RGMII1_TD0	PRU_ICSSG RGMII Transmit Data	O	AF24
PRG1_RGMII1_TD1	PRU_ICSSG RGMII Transmit Data	O	AJ24
PRG1_RGMII1_TD2	PRU_ICSSG RGMII Transmit Data	O	AG24
PRG1_RGMII1_TD3	PRU_ICSSG RGMII Transmit Data	O	AD24
PRG1_RGMII2_RD0	PRU_ICSSG RGMII Receive Data	I	AE22
PRG1_RGMII2_RD1	PRU_ICSSG RGMII Receive Data	I	AG23
PRG1_RGMII2_RD2	PRU_ICSSG RGMII Receive Data	I	AF23
PRG1_RGMII2_RD3	PRU_ICSSG RGMII Receive Data	I	AD23
PRG1_RGMII2_TD0	PRU_ICSSG RGMII Transmit Data	O	AJ25
PRG1_RGMII2_TD1	PRU_ICSSG RGMII Transmit Data	O	AH25
PRG1_RGMII2_TD2	PRU_ICSSG RGMII Transmit Data	O	AG25
PRG1_RGMII2_TD3	PRU_ICSSG RGMII Transmit Data	O	AH26
PRG1_UART0_CTSn	PRU_ICSSG UART Clear to Send (active low)	I	AG20
PRG1_UART0_RTSn	PRU_ICSSG UART Request to Send (active low)	O	AD21
PRG1_UART0_RXD	PRU_ICSSG UART Receive Data	I	AF21
PRG1_UART0_TXD	PRU_ICSSG UART Transmit Data	O	AB23

5.3.24 MCASP

5.3.24.1 MAIN Domain

表 5-95. MCASP0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP0_ACLKR	MCASP Receive Bit Clock	IO	AE27
MCASP0_ACLKX	MCASP Transmit Bit Clock	IO	AB26
MCASP0_AFSR	MCASP Receive Frame Sync	IO	AD26

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表 5-95. MCASP0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP0_AFSX	MCASP Transmit Frame Sync	IO	AB25
MCASP0_AXR0	MCASP Serial Data (Input/Output)	IO	AF28
MCASP0_AXR1	MCASP Serial Data (Input/Output)	IO	AE28
MCASP0_AXR2	MCASP Serial Data (Input/Output)	IO	AD25
MCASP0_AXR3	MCASP Serial Data (Input/Output)	IO	AC29
MCASP0_AXR4	MCASP Serial Data (Input/Output)	IO	AE26
MCASP0_AXR5	MCASP Serial Data (Input/Output)	IO	AC28
MCASP0_AXR6	MCASP Serial Data (Input/Output)	IO	AC27
MCASP0_AXR7	MCASP Serial Data (Input/Output)	IO	AJ28
MCASP0_AXR8	MCASP Serial Data (Input/Output)	IO	AH27
MCASP0_AXR9	MCASP Serial Data (Input/Output)	IO	AH29
MCASP0_AXR10	MCASP Serial Data (Input/Output)	IO	AG28
MCASP0_AXR11	MCASP Serial Data (Input/Output)	IO	AG27
MCASP0_AXR12	MCASP Serial Data (Input/Output)	IO	AH28
MCASP0_AXR13	MCASP Serial Data (Input/Output)	IO	AB24
MCASP0_AXR14	MCASP Serial Data (Input/Output)	IO	AB29
MCASP0_AXR15	MCASP Serial Data (Input/Output)	IO	AB28

表 5-96. MCASP1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP1_ACLKR	MCASP Receive Bit Clock	IO	AD27
MCASP1_ACLKX	MCASP Transmit Bit Clock	IO	AB27
MCASP1_AFSR	MCASP Receive Frame Sync	IO	AC25
MCASP1_AFSX	MCASP Transmit Frame Sync	IO	AA28
MCASP1_AXR0	MCASP Serial Data (Input/Output)	IO	AE29
MCASP1_AXR1	MCASP Serial Data (Input/Output)	IO	AD28
MCASP1_AXR2	MCASP Serial Data (Input/Output)	IO	AD29
MCASP1_AXR3	MCASP Serial Data (Input/Output)	IO	AC26
MCASP1_AXR4	MCASP Serial Data (Input/Output)	IO	AA24
MCASP1_AXR5	MCASP Serial Data (Input/Output)	IO	Y24
MCASP1_AXR6	MCASP Serial Data (Input/Output)	IO	AA25
MCASP1_AXR7	MCASP Serial Data (Input/Output)	IO	AG26
MCASP1_AXR8	MCASP Serial Data (Input/Output)	IO	AF27
MCASP1_AXR9	MCASP Serial Data (Input/Output)	IO	AF26
MCASP1_AXR10	MCASP Serial Data (Input/Output)	IO	AD27
MCASP1_AXR11	MCASP Serial Data (Input/Output)	IO	AC25

表 5-97. MCASP2 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP2_ACLKR	MCASP Receive Bit Clock	IO	AA27
MCASP2_ACLKX	MCASP Transmit Bit Clock	IO	AA29
MCASP2_AFSR	MCASP Receive Frame Sync	IO	Y26
MCASP2_AFSX	MCASP Transmit Frame Sync	IO	AA26

表 5-97. MCASP2 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP2_AXR0	MCASP Serial Data (Input/Output)	IO	AE25
MCASP2_AXR1	MCASP Serial Data (Input/Output)	IO	AF29
MCASP2_AXR2	MCASP Serial Data (Input/Output)	IO	AG29
MCASP2_AXR3	MCASP Serial Data (Input/Output)	IO	Y25
MCASP2_AXR4	MCASP Serial Data (Input/Output)	IO	Y26
MCASP2_AXR5	MCASP Serial Data (Input/Output)	IO	AA27

表 5-98. MCASP3 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP3_ACLKR	MCASP Receive Bit Clock	IO	AF23
MCASP3_ACLKX	MCASP Transmit Bit Clock	IO	AG20
MCASP3_AFSR	MCASP Receive Frame Sync	IO	AD23
MCASP3_AFSX	MCASP Transmit Frame Sync	IO	AD21
MCASP3_AXR0	MCASP Serial Data (Input/Output)	IO	AD20
MCASP3_AXR1	MCASP Serial Data (Input/Output)	IO	AE20
MCASP3_AXR2	MCASP Serial Data (Input/Output)	IO	AJ20
MCASP3_AXR3	MCASP Serial Data (Input/Output)	IO	AJ21

表 5-99. MCASP4 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP4_ACLKR	MCASP Receive Bit Clock	IO	AG25
MCASP4_ACLKX	MCASP Transmit Bit Clock	IO	AE21
MCASP4_AFSR	MCASP Receive Frame Sync	IO	AH26
MCASP4_AFSX	MCASP Transmit Frame Sync	IO	AH21
MCASP4_AXR0	MCASP Serial Data (Input/Output)	IO	AG21
MCASP4_AXR1	MCASP Serial Data (Input/Output)	IO	AC21
MCASP4_AXR2	MCASP Serial Data (Input/Output)	IO	Y23
MCASP4_AXR3	MCASP Serial Data (Input/Output)	IO	AF21

表 5-100. MCASP5 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP5_ACLKR	MCASP Receive Bit Clock	IO	AD19
MCASP5_ACLKX	MCASP Transmit Bit Clock	IO	AB23
MCASP5_AFSR	MCASP Receive Frame Sync	IO	AD18
MCASP5_AFSX	MCASP Transmit Frame Sync	IO	AC22
MCASP5_AXR0	MCASP Serial Data (Input/Output)	IO	AJ22
MCASP5_AXR1	MCASP Serial Data (Input/Output)	IO	AH22
MCASP5_AXR2	MCASP Serial Data (Input/Output)	IO	AD19
MCASP5_AXR3	MCASP Serial Data (Input/Output)	IO	AD18

表 5-101. MCASP6 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP6_ACLKR	MCASP Receive Bit Clock	IO	AH23

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表 5-101. MCASP6 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP6_ACLKX	MCASP Transmit Bit Clock	IO	AC23
MCASP6_AFSR	MCASP Receive Frame Sync	IO	AD22
MCASP6_AFSX	MCASP Transmit Frame Sync	IO	AG22
MCASP6_AXR0	MCASP Serial Data (Input/Output)	IO	AF22
MCASP6_AXR1	MCASP Serial Data (Input/Output)	IO	AJ23
MCASP6_AXR2	MCASP Serial Data (Input/Output)	IO	AH23
MCASP6_AXR3	MCASP Serial Data (Input/Output)	IO	AD22

表 5-102. MCASP7 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP7_ACLKR	MCASP Receive Bit Clock	IO	AC24
MCASP7_ACLKX	MCASP Transmit Bit Clock	IO	AF24
MCASP7_AFSR	MCASP Receive Frame Sync	IO	AE24
MCASP7_AFSX	MCASP Transmit Frame Sync	IO	AJ24
MCASP7_AXR0	MCASP Serial Data (Input/Output)	IO	AG24
MCASP7_AXR1	MCASP Serial Data (Input/Output)	IO	AD24
MCASP7_AXR2	MCASP Serial Data (Input/Output)	IO	AC24
MCASP7_AXR3	MCASP Serial Data (Input/Output)	IO	AE24

表 5-103. MCASP8 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP8_ACLKR	MCASP Receive Bit Clock	IO	AH24
MCASP8_ACLKX	MCASP Transmit Bit Clock	IO	AE22
MCASP8_AFSR	MCASP Receive Frame Sync	IO	AE23
MCASP8_AFSX	MCASP Transmit Frame Sync	IO	AG23
MCASP8_AXR0	MCASP Serial Data (Input/Output)	IO	AF23
MCASP8_AXR1	MCASP Serial Data (Input/Output)	IO	AD23
MCASP8_AXR2	MCASP Serial Data (Input/Output)	IO	AH24
MCASP8_AXR3	MCASP Serial Data (Input/Output)	IO	AE23

表 5-104. MCASP9 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP9_ACLKR	MCASP Receive Bit Clock	IO	AJ27
MCASP9_ACLKX	MCASP Transmit Bit Clock	IO	AJ25
MCASP9_AFSR	MCASP Receive Frame Sync	IO	AJ26
MCASP9_AFSX	MCASP Transmit Frame Sync	IO	AH25
MCASP9_AXR0	MCASP Serial Data (Input/Output)	IO	AG25
MCASP9_AXR1	MCASP Serial Data (Input/Output)	IO	AH26
MCASP9_AXR2	MCASP Serial Data (Input/Output)	IO	AJ27
MCASP9_AXR3	MCASP Serial Data (Input/Output)	IO	AJ26

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表 5-105. MCASP10 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP10_ACLKR	MCASP Receive Bit Clock	IO	Y28
MCASP10_ACLKX	MCASP Transmit Bit Clock	IO	U23
MCASP10_AFSR	MCASP Receive Frame Sync	IO	V23
MCASP10_AFSX	MCASP Transmit Frame Sync	IO	U26
MCASP10_AXR0	MCASP Serial Data (Input/Output)	IO	V28
MCASP10_AXR1	MCASP Serial Data (Input/Output)	IO	V29
MCASP10_AXR2	MCASP Serial Data (Input/Output)	IO	U29
MCASP10_AXR3	MCASP Serial Data (Input/Output)	IO	U25
MCASP10_AXR4	MCASP Serial Data (Input/Output)	IO	V25
MCASP10_AXR5	MCASP Serial Data (Input/Output)	IO	W27
MCASP10_AXR6	MCASP Serial Data (Input/Output)	IO	W29
MCASP10_AXR7	MCASP Serial Data (Input/Output)	IO	W26

表 5-106. MCASP11 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCASP11_ACLKR	MCASP Receive Bit Clock	IO	W23
MCASP11_ACLKX	MCASP Transmit Bit Clock	IO	V27
MCASP11_AFSR	MCASP Receive Frame Sync	IO	W28
MCASP11_AFSX	MCASP Transmit Frame Sync	IO	U28
MCASP11_AXR0	MCASP Serial Data (Input/Output)	IO	U27
MCASP11_AXR1	MCASP Serial Data (Input/Output)	IO	U24
MCASP11_AXR2	MCASP Serial Data (Input/Output)	IO	R23
MCASP11_AXR3	MCASP Serial Data (Input/Output)	IO	T23
MCASP11_AXR4	MCASP Serial Data (Input/Output)	IO	Y29
MCASP11_AXR5	MCASP Serial Data (Input/Output)	IO	Y27
MCASP11_AXR6	MCASP Serial Data (Input/Output)	IO	W24
MCASP11_AXR7	MCASP Serial Data (Input/Output)	IO	W25

5.3.25 DSS

5.3.25.1 MAIN Domain

表 5-107. DSS0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
DSS_FSYNC0	Video Output Frame Sync 0	O	AH27, Y26
DSS_FSYNC1	Video Output Frame Sync 1	O	AD19, AH28
DSS_FSYNC2	Video Output Frame Sync 2	O	AA27, AH29
DSS_FSYNC3	Video Output Frame Sync 3	O	AG27, Y24
VOUT0_DE	Video Output Data Enable	O	AC22
VOUT0_EXTPCLKIN	Video Output External Pixel Clock Input	I	AH21
VOUT0_HSYNC	Video Output Horizontal Sync	O	AJ26
VOUT0_PCLK	Video Output Pixel Clock Output	O	AH22
VOUT0_VSYNC	Video Output Vertical Sync	O	AJ22
VOUT0_DATA0	Video Output Data 0	O	AE22
VOUT0_DATA1	Video Output Data 1	O	AG23

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表 5-107. DSS0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VOUT0_DATA2	Video Output Data 2	O	AF23
VOUT0_DATA3	Video Output Data 3	O	AD23
VOUT0_DATA4	Video Output Data 4	O	AH24
VOUT0_DATA5	Video Output Data 5	O	AG21
VOUT0_DATA6	Video Output Data 6	O	AE23
VOUT0_DATA7	Video Output Data 7	O	AC21
VOUT0_DATA8	Video Output Data 8	O	Y23
VOUT0_DATA9	Video Output Data 9	O	AF21
VOUT0_DATA10	Video Output Data 10	O	AB23
VOUT0_DATA11	Video Output Data 11	O	AJ25
VOUT0_DATA12	Video Output Data 12	O	AH25
VOUT0_DATA13	Video Output Data 13	O	AG25
VOUT0_DATA14	Video Output Data 14	O	AH26
VOUT0_DATA15	Video Output Data 15	O	AJ27
VOUT0_DATA16	Video Output Data 16	O	AF24
VOUT0_DATA17	Video Output Data 17	O	AJ24
VOUT0_DATA18	Video Output Data 18	O	AG24
VOUT0_DATA19	Video Output Data 19	O	AD24
VOUT0_DATA20	Video Output Data 20	O	AC24
VOUT0_DATA21	Video Output Data 21	O	AE24
VOUT0_DATA22	Video Output Data 22	O	AJ20
VOUT0_DATA23	Video Output Data 23	O	AG20
VOUT0_VP0_DE	Video Output Data Enable	O	AC22
VOUT0_VP0_HSYNC	Video Output Horizontal Sync	O	AJ26
VOUT0_VP0_VSYNC	Video Output Vertical Sync	O	AJ22
VOUT0_VP2_DE	Video Output Data Enable	O	AC22
VOUT0_VP2_HSYNC	Video Output Horizontal Sync	O	AJ26
VOUT0_VP2_VSYNC	Video Output Vertical Sync	O	AJ22
VOUT1_DE	Video Output Data Enable	O	W26
VOUT1_EXTPCLKIN	Video Output External Pixel Clock Input	I	W24
VOUT1_HSYNC	Video Output Horizontal Sync	O	W27
VOUT1_PCLK	Video Output Pixel Clock Output	O	W29
VOUT1_VSYNC	Video Output Vertical Sync	O	V25
VOUT1_DATA0	Video Output Data 0	O	U23
VOUT1_DATA1	Video Output Data 1	O	U26
VOUT1_DATA2	Video Output Data 2	O	V28
VOUT1_DATA3	Video Output Data 3	O	V29
VOUT1_DATA4	Video Output Data 4	O	V27
VOUT1_DATA5	Video Output Data 5	O	U28
VOUT1_DATA6	Video Output Data 6	O	U29
VOUT1_DATA7	Video Output Data 7	O	U25
VOUT1_DATA8	Video Output Data 8	O	U27
VOUT1_DATA9	Video Output Data 9	O	U24
VOUT1_DATA10	Video Output Data 10	O	R23

表 5-107. DSS0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VOUT1_DATA11	Video Output Data 11	O	T23
VOUT1_DATA12	Video Output Data 12	O	Y28
VOUT1_DATA13	Video Output Data 13	O	V23
VOUT1_DATA14	Video Output Data 14	O	W23
VOUT1_DATA15	Video Output Data 15	O	W28
VOUT1_VP0_DE	Video Output Data Enable	O	W26
VOUT1_VP0_HSYNC	Video Output Horizontal Sync	O	W27
VOUT1_VP0_VSYNC	Video Output Vertical Sync	O	V25

5.3.26 DP

5.3.26.1 MAIN Domain

注

DP0_TX functionality is available on the SERDES pins. For more information, refer to セクション 5.3.16, *SERDES*.

表 5-108. DP0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
DP0_AUXN	Display port differential auxiliary data (negative)	IO	G6
DP0_AUXP	Display port differential auxiliary data (positive)	IO	F7
DP0_HPD	Display Port Hot Plugged Display Detect	I	W2, Y4

5.3.27 Camera Streaming Interface Receiver (CSI_RX_IF) Subsystem

5.3.27.1 MAIN Domain

表 5-109. CSI0 Signal Descriptions

SIGNAL NAME [1] (2)	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
CSI0_RXCLKN	CSI Differential Receive Clock Input (negative)	I	B20
CSI0_RXCLKP	CSI Differential Receive Clock Input (positive)	I	A21
CSI0_RXRCALIB(1)	CSI pin connected to external resistor for on-chip resistor calibration	A	F16
CSI0_RXN0	CSI Differential Receive Input (negative)	I	B19
CSI0_RXP0	CSI Differential Receive Input (positive)	I	A20
CSI0_RXN1	CSI Differential Receive Input (negative)	I	D18
CSI0_RXP1	CSI Differential Receive Input (positive)	I	C19
CSI0_RXN2	CSI Differential Receive Input (negative)	I	D17
CSI0_RXP2	CSI Differential Receive Input (positive)	I	C18
CSI0_RXN3	CSI Differential Receive Input (negative)	I	E16
CSI0_RXP3	CSI Differential Receive Input (positive)	I	E17

(1) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused.
(2) CSI TX functionally is available on the DSI pins. For more information, refer to セクション 5.3.28, *DSI_TX*.

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表 5-110. CSI1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
CSI1_RXCLKN	CSI Differential Receive Clock Input (negative)	I	B17
CSI1_RXCLKP	CSI Differential Receive Clock Input (positive)	I	A18
CSI1_RXRCALIB(1)	CSI pin connected to external resistor for on-chip resistor calibration	A	F15
CSI1_RXN0	CSI Differential Receive Input (negative)	I	B16
CSI1_RXP0	CSI Differential Receive Input (positive)	I	A17
CSI1_RXN1	CSI Differential Receive Input (negative)	I	D15
CSI1_RXP1	CSI Differential Receive Input (positive)	I	C16
CSI1_RXN2	CSI Differential Receive Input (negative)	I	D14
CSI1_RXP2	CSI Differential Receive Input (positive)	I	C15
CSI1_RXN3	CSI Differential Receive Input (negative)	I	E13
CSI1_RXP3	CSI Differential Receive Input (positive)	I	E14

(1) An external 500 Ω ±1% resistor must be connected between this pin and VSS, even when the pin is unused.

5.3.28 DSI_TX

5.3.28.1 MAIN Domain

表 5-111. DSI_TX0 Signal Descriptions

SIGNAL NAME [1] (1)	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
DSI_TXCLKN	DSI Differential Transmit Clock Output (positive)	O	E10
DSI_TXCLKP	DSI Differential Transmit Clock Output (negative)	O	E11
DSI_TXN0	DSI Differential Transmit Output (negative)	IO	D11
DSI_TXP0	DSI Differential Transmit Output (positive)	IO	C12
DSI_TXN1	DSI Differential Transmit Output (negative)	O	D12
DSI_TXP1	DSI Differential Transmit Output (positive)	O	C13
DSI_TXN2	DSI Differential Transmit Output (negative)	O	B13
DSI_TXP2	DSI Differential Transmit Output (positive)	O	A14
DSI_TXN3	DSI Differential Transmit Output (negative)	O	B14
DSI_TXP3	DSI Differential Transmit Output (positive)	O	A15
DSI_TXRCALIB(2)	DSI pin connected to external resistor for on-chip resistor calibration	A	F12

(1) The functionality of these pins is controlled by CTRLMMR_DPHY_TX0_CTRL[1:0] LANE_FUNC_SEL. 0x0 = DSI PPI, 0x1 = CSI0 TX.
(2) An external 500 Ω ±1%. resistor must be connected between this pin and VSS, even when the pin is unused.

5.3.29 VPFE

5.3.29.1 MAIN Domain

表 5-112. VPFE0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VPFE0_FIELD	Video Input Field Indicator	I	AG23
VPFE0_HD	Video Input Horizontal Sync	I	AE22
VPFE0_PCLK	Video Input Pixel Clock	I	AH21
VPFE0_VD	Video Input Vertical Sync	I	AF23
VPFE0_WEN	Video Input Write Enable	I	AD23
VPFE0_DATA0	Video Input Data	I	AF24
VPFE0_DATA1	Video Input Data	I	AJ24

表 5-112. VPFE0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VPFE0_DATA2	Video Input Data	I	AG24
VPFE0_DATA3	Video Input Data	I	AD24
VPFE0_DATA4	Video Input Data	I	AC24
VPFE0_DATA5	Video Input Data	I	AE24
VPFE0_DATA6	Video Input Data	I	AJ21
VPFE0_DATA7	Video Input Data	I	AE21
VPFE0_DATA8	Video Input Data	I	AG25
VPFE0_DATA9	Video Input Data	I	AJ27
VPFE0_DATA10	Video Input Data	I	AC22
VPFE0_DATA11	Video Input Data	I	AD19
VPFE0_DATA12	Video Input Data	I	AD18
VPFE0_DATA13	Video Input Data	I	AH24
VPFE0_DATA14	Video Input Data	I	AE23
VPFE0_DATA15	Video Input Data	I	AC21

5.3.30 DMTIMER

5.3.30.1 MAIN Domain

表 5-113. DMTIMER Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
TIMER_IO0	Timer Inputs and Outputs (not tied to single timer instance)	IO	P24, V6
TIMER_IO1	Timer Inputs and Outputs (not tied to single timer instance)	IO	R24, V5
TIMER_IO2	Timer Inputs and Outputs (not tied to single timer instance)	IO	AD23, P23
TIMER_IO3	Timer Inputs and Outputs (not tied to single timer instance)	IO	AH24, R28
TIMER_IO4	Timer Inputs and Outputs (not tied to single timer instance)	IO	AG21, T27
TIMER_IO5	Timer Inputs and Outputs (not tied to single timer instance)	IO	AE23, T24
TIMER_IO6	Timer Inputs and Outputs (not tied to single timer instance)	IO	AC2, T26
TIMER_IO7	Timer Inputs and Outputs (not tied to single timer instance)	IO	AB1, T25

5.3.30.2 MCU Domain

表 5-114. DMTIMER Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_TIMER_IO0	Timer Inputs and Outputs (not tied to single timer instance)	IO	E22, E28
MCU_TIMER_IO1	Timer Inputs and Outputs (not tied to single timer instance)	IO	E25, H27
MCU_TIMER_IO2	Timer Inputs and Outputs (not tied to single timer instance)	IO	A28

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表 5-114. DMTIMER Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_TIMER_IO3	Timer Inputs and Outputs (not tied to single timer instance)	IO	A27
MCU_TIMER_IO4	Timer Inputs and Outputs (not tied to single timer instance)	IO	A25
MCU_TIMER_IO5	Timer Inputs and Outputs (not tied to single timer instance)	IO	D24
MCU_TIMER_IO6	Timer Inputs and Outputs (not tied to single timer instance)	IO	G27
MCU_TIMER_IO7	Timer Inputs and Outputs (not tied to single timer instance)	IO	G26
MCU_TIMER_IO8	Timer Inputs and Outputs (not tied to single timer instance)	IO	D26
MCU_TIMER_IO9	Timer Inputs and Outputs (not tied to single timer instance)	IO	D25

5.3.31 Emulation and Debug

5.3.31.1 MAIN Domain

表 5-115. JTAG Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
EMU0	Emulation Control 0	IO	C26
EMU1	Emulation Control 1	IO	B29
TCK	JTAG Test Clock Input	I	E29
TDI	JTAG Test Data Input	I	V1
TDO	JTAG Test Data Output	OZ	V3
TMS	JTAG Test Mode Select Input	I	V2
TRSTn	JTAG Reset	I	F24

表 5-116. Trace Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
TRC_CLK	Trace Clock	O	U23
TRC_CTL	Trace Control	O	U26
TRC_DATA0	Trace Data 0	O	V28
TRC_DATA1	Trace Data 1	O	V29
TRC_DATA2	Trace Data 2	O	V27
TRC_DATA3	Trace Data 3	O	U28
TRC_DATA4	Trace Data 4	O	U29
TRC_DATA5	Trace Data 5	O	U25
TRC_DATA6	Trace Data 6	O	U27
TRC_DATA7	Trace Data 7	O	U24
TRC_DATA8	Trace Data 8	O	R23
TRC_DATA9	Trace Data 9	O	T23
TRC_DATA10	Trace Data 10	O	Y28
TRC_DATA11	Trace Data 11	O	V23
TRC_DATA12	Trace Data 12	O	W23
TRC_DATA13	Trace Data 13	O	W28
TRC_DATA14	Trace Data 14	O	V25
TRC_DATA15	Trace Data 15	O	W27
TRC_DATA16	Trace Data 16	O	W29
TRC_DATA17	Trace Data 17	O	W26
TRC_DATA18	Trace Data 18	O	Y29
TRC_DATA19	Trace Data 19	O	Y27
TRC_DATA20	Trace Data 20	O	W24
TRC_DATA21	Trace Data 21	O	W25
TRC_DATA22	Trace Data 22	O	V26
TRC_DATA23	Trace Data 23	O	V24

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5.3.32 System and Miscellaneous

5.3.32.1 Boot Mode Configuration

5.3.32.1.1 MAIN Domain

注

BOOTMODE pins are latched on the rising edge of PORz_OUT.

表 5-117. Sysboot Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
BOOTMODE0	Bootmode pin 0	I	AD20
BOOTMODE1	Bootmode pin 1	I	AC22
BOOTMODE2	Bootmode pin 2	I	AC29
BOOTMODE3	Bootmode pin 3	I	Y25
BOOTMODE4	Bootmode pin 4	I	V6
BOOTMODE5	Bootmode pin 5	I	V5
BOOTMODE6	Bootmode pin 6	I	AB27
BOOTMODE7[(1)]	Bootmode pin 7	I	AB24

(1) These signals must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level.

5.3.32.1.2 MCU Domain

注

MCU_BOOTMODE pins are latched on the rising edge of MCU_PORz_OUT.

表 5-118. Sysboot Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_BOOTMODE00	Bootmode pin 00	I	E27
MCU_BOOTMODE01	Bootmode pin 01	I	E24
MCU_BOOTMODE02	Bootmode pin 02	I	E28
MCU_BOOTMODE03	Bootmode pin 03	I	F26
MCU_BOOTMODE04	Bootmode pin 04	I	F25
MCU_BOOTMODE05	Bootmode pin 05	I	F28
MCU_BOOTMODE06	Bootmode pin 06	I	H29
MCU_BOOTMODE07	Bootmode pin 07	I	J27
MCU_BOOTMODE08	Bootmode pin 08	I	G29
MCU_BOOTMODE09	Bootmode pin 09	I	H28

5.3.32.2 Clock

5.3.32.2.1 MAIN Domain

表 5-119. Clock1 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
OSC1_XI	High frequency oscillator input	I	P29
OSC1_XO	High frequency oscillator output	O	P27

5.3.32.2.2 WKUP Domain

表 5-120. Clock0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
WKUP_LFOSC0_XI	Low frequency (32.768 KHz) oscillator input	I	N28
WKUP_LFOSC0_XO	Low frequency (32.768 KHz) oscillator output	O	N26
WKUP_OSC0_XI	High frequency oscillator input	I	M29
WKUP_OSC0_XO	High frequency oscillator output	O	M27

5.3.32.3 System

5.3.32.3.1 MAIN Domain

表 5-121. System0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
AUDIO_EXT_REFCLK0	External clock routed to ATL or MCASP as one of the selectable input clock sources, or as a output clock output for ATL or MCASP	IO	AD22
AUDIO_EXT_REFCLK1	External clock routed to ATL or MCASP as one of the selectable input clock sources, or as a output clock output for ATL or MCASP	IO	AE20
AUDIO_EXT_REFCLK2	External clock routed to ATL or MCASP as one of the selectable input clock sources, or as a output clock output for ATL or MCASP	IO	W26
AUDIO_EXT_REFCLK3	External clock routed to ATL or MCASP as one of the selectable input clock sources, or as a output clock output for ATL or MCASP	IO	W25
EXTINTn	External Interrupt	I	AC18
EXT_REFCLK1	External clock input to MAIN domain, routed to Timer clock muxes as one of the selectable input clock sources for Timer/WDT modules, or as reference clock to MAIN_PLL2 (PER1 PLL)	I	U3
OBSCLK0	Observation clock output for test and debug purposes only	O	V5
OBSCLK1	Observation clock output for test and debug purposes only	O	AB24
OBSCLK2	Observation clock output for test and debug purposes only	O	AD21
PORz_OUT	MAIN domain POR status output	O	U1
RESETSTATz	MAIN domain warm reset status output	O	T6
SOC_SAFETY_ERRORn	Error signal output from MAIN domain ESM	IO	U4
SYSCLKOUT0	SYSCLK0 output from MAIN PLL controller (divided by 6) for test and debug purposes only	O	V6
VMON_ER_VSYS	Voltage Monitor for System supply, requires External Resistor divider	A	M26
VMON_IR_VEXT	Voltage Monitor for External 1.8V supply, uses Internal Resistor divider	A	V19

5.3.32.3.2 WKUP Domain

表 5-122. System0 Signal Descriptions

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_CLKOUT0	Reference clock output for Ethernet PHYs (50MHz or 25MHz)	OZ	H27

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表 5-122. System0 Signal Descriptions (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
MCU_EXT_REFCLK0	External system clock input	I	H26
MCU_OBSCLK0	Observation clock output for test and debug purposes only	O	H27
MCU_PORz	MCU Domain cold reset	I	H23
MCU_PORz_OUT	MCU Domain POR status output	O	B28
MCU_RESETSTATz	MCU Domain warm reset status output	O	C27
MCU_RESETz	MCU Domain warm reset	I	D28
MCU_SAFETY_ERRORn	Error signal output from MCU Domain ESM	IO	D27
MCU_SYSCLKOUT0	MCU Domain system clock output for test and debug purposes only	O	H26
PORz	MAIN Domain cold reset	I	J24
RESET_REQz	MAIN Domain external warm reset request input	I	C28
PMIC_POWER_EN0	Pin name retained for legacy purposes, not used for power enable	NA	E26
PMIC_POWER_EN1	Power enable output for MAIN Domain supplies	O	G23

5.3.32.4 EFUSE

表 5-123. EFUSE Signal Description

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VPP_CORE(1)	Programming voltage for MAIN Domain efuses	PWR	AB11
VPP_MCU(1)	Programming voltage for MCU Domain efuses	PWR	F17

(1) This signal is valid only for High-Security devices. For more details, see セクション 6.7, *VPP Specification for One-Time Programmable (OTP) eFUSEs*. For General-Purpose devices do not connect any signal, test point, or board trace to this signal.

5.3.33 Power Supply

注

All power balls must be supplied with the voltages specified in セクション 6.4, *Recommended Operating Conditions,* unless otherwise specified in セクション 5.3, *Signal Descriptions*.

表 5-124. Power Supply Signal Description

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
CAP_VDDS0(1)	External capacitor connection for	CAP	U7
CAP_VDDS0_MCU(1)	External capacitor connection for	CAP	K23
CAP_VDDS1(1)	External capacitor connection for	CAP	AB21
CAP_VDDS1_MCU(1)	External capacitor connection for	CAP	J18
CAP_VDDS2(1)	External capacitor connection for	CAP	Y18
CAP_VDDS2_MCU(1)	External capacitor connection for	CAP	J19
CAP_VDDS3(1)	External capacitor connection for	CAP	W21
CAP_VDDS4(1)	External capacitor connection for	CAP	AA22
CAP_VDDS5(1)	External capacitor connection for	CAP	R22
CAP_VDDS6(1)	External capacitor connection for	CAP	V22
VDDAR_CORE	MAIN domain RAM supply	PWR	L14, V13, V16, W19
VDDAR_CPU	CPU RAM supply	PWR	L11, W12

表 5-124. Power Supply Signal Description (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VDDAR_MCU	MCUSS RAM supply	PWR	K19, T19
VDDA_0P8_CSIRX	CSIRX analog supply low	PWR	H17
VDDA_0P8_DP	Displayport SERDES analog supply low	PWR	G12, J12
VDDA_0P8_DP_C	Displayport SERDES clock supply	PWR	G14, H13
VDDA_0P8_DSITX	DSITX clock supply	PWR	H15
VDDA_0P8_DSITX_C	DSITX clock supply	PWR	J16
VDDA_0P8_UFS	UFS analog supply low	PWR	AB9
VDDA_0P8_USB	USB0-1 0.8 V analog supply	PWR	AA10
VDDA_0P8_SERDES0_1	SERDES0-1 analog supply low	PWR	AA15, Y14, Y16
VDDA_0P8_SERDES2_3	SERDES2-3 analog supply low	PWR	AA12, Y11, Y13
VDDA_0P8_SERDES_C0_1	SERDES0-1 clock supply	PWR	AB14, AB15
VDDA_0P8_SERDES_C2_3	SERDES2-3 clock supply	PWR	AB12, AB13
VDDA_1P8_CSIRX	CSIRX analog supply high	PWR	G16
VDDA_1P8_DP	Displayport SERDES analog supply high	PWR	H11
VDDA_1P8_DSITX	DSITX analog supply high	PWR	J14
VDDA_1P8_UFS	UFS analog supply high	PWR	AC8
VDDA_1P8_USB	USB0-1 1.8 V analog supply	PWR	AC9
VDDA_1P8_SERDES0_1	SERDES0-1 analog supply high	PWR	AC14, AC15
VDDA_1P8_SERDES2_3	SERDES2-3 analog supply high	PWR	AC11, AC12
VDDA_3P3_USB	USB0-1 3.3 V analog supply	PWR	AB10
VDDA_ADC0	ADC analog supply and high voltage reference (VREFP)	PWR	N22
VDDA_ADC1	ADC analog supply and high voltage reference (VREFP)	PWR	M23
VDDA_0P8_PLL_DDR	DDR PLL analog supply	PWR	N9
VDDA_MCU_PLLGRP0	Analog supply for MCU PLL Group 0	PWR	G18
VDDA_MCU_TEMP	Analog supply for temperature sensor 0 in MCU domain	PWR	P21
VDDA_1P8_MLB	MLB IO supply (6-pin interface)	PWR	W7
VDDA_PLLGRP0	Analog supply for MAIN PLL Group 0	PWR	Y20
VDDA_PLLGRP1	Analog supply for MAIN PLL Group 1	PWR	W17
VDDA_PLLGRP2	Analog supply for MAIN PLL Group 2	PWR	M17
VDDA_PLLGRP3	Analog supply for MAIN PLL Group 3	PWR	L12
VDDA_PLLGRP4	Analog supply for MAIN PLL Group 4	PWR	R11
VDDA_PLLGRP5	Analog supply for MAIN PLL Group 5 (DDR)	PWR	P9
VDDA_PLLGRP6	Analog supply for MAIN PLL Group 6	PWR	W18
VDDA_0P8_PLL_MLB	MLB PLL analog supply	PWR	W8
VDDA_POR_WKUP	WKUP domain analog supply	PWR	P22
VDDA_TEMP0_1	Analog supply for temperature sensor 0 and 1	PWR	W15
VDDA_TEMP2_3	Analog supply for temperature sensor 2 amd 3	PWR	H9
VDDA_WKUP	Oscillator supply for WKUP domain	PWR	H22
VDDSHV0	IO supply for MAIN domain general	PWR	U8, V7
VDDSHV0_MCU	IO supply MCUSS general IO group, and MCU and MAIN domain warm reset pins	PWR	L22, M22
VDDSHV1	IO supply for MAIN domain IO group 1	PWR	AA19, AA20, AC19, AC20
VDDSHV1_MCU	IO supply for MCUSS IO group 1	PWR	H19, H21, J20

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表 5-124. Power Supply Signal Description (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VDDSHV2	IO supply for MAIN domain IO group 2	PWR	AA17, AB16, AB18, AC17
VDDSHV2_MCU	IO supply for MCUSS IO group 2	PWR	J22, K21
VDDSHV3	IO supply for MAIN domain IO group 3	PWR	V21, W22
VDDSHV4	IO supply for MAIN domain IO group 4	PWR	AA21, Y22
VDDSHV5	IO supply for MAIN domain IO group 5	PWR	T20, T22
VDDSHV6	IO supply for MAIN domain IO group 6	PWR	U20, U22
VDDS_DDR	DDR inteface power supply	PWR	A1, G8, J8, K7, L8, M7, N8, P7, R8, T1
VDDS_DDR_BIAS	Bias supply for LPDDR4	PWR	H7, J6, R6, T7
VDDS_DDR_C	IO power for DDR Memory Clock Bit (MCB) macro	PWR	M9
VDDS_MMC0	MMC0 IO supply	PWR	AA8, AB7, Y7
VDDS_OSC1	HFOSC1 supply	PWR	R21
VDD_CORE	MAIN domain core supply	PWR	J10, K11, K13, K15, K17, K9, L10, L16, L18, M15, N14, N16, N18, P13, P15, P17, R14, R16, R18, R20, T15, T17, T9, U14, U16, U18, V15, V17, V20, W14
VDD_CPU	CPU core supply	PWR	N10, P11, R10, R12, U10, V11, V9, W10
VDDA_0P8_DLL_MMC0	MMC0 DLL analog supply	PWR	Y9
VDD_MCU	MCUSS core supply	PWR	L20, M19, M21, N20, P19

表 5-124. Power Supply Signal Description (続き)

SIGNAL NAME [1]	DESCRIPTION [2]	PIN TYPE [3]	BALL [4]
VSS	Ground	GND	AA13, AC10, AC13, AD11, AD14, AD17, AE10, AE12, AE15, AE16, AE19, AE7, AF20, AF25, AF5, AG4, AG7, AH2, AH20, AH5, AJ4, AJ7, B3, B6, C1, C5, D2, D4, E1, E5, F4, G1, G7, H4, H6, K1, K4, L3, M1, M28, M4, M6, N27, N29, N3, P1, P28, P4, R3, U5 A10, A13, A16, A19, A22, A7, AA11, AA14, AA16, AA18, AA7, AA9, AB17, AB19, AB20, AB22, AB8, AC16, AF11, AF14, AF17, AF8, AG10, AG13, AG16, AG19, AH11, AH14, AH17, AH8, AJ10, AJ13, AJ16, AJ19, B12, B15, B18, B21, B9, C11, C14, C17, C20, C8, D10, D13, D16, D19, D7, E12, E15, E9, F14, F8, G11, G13, G15, G17, H10, H12, H14, H16, H18, H20, H8, J11, J13, J15, J17, J21, J23, J7, J9, K10, K12, K14, K16, K18, K20, K22, K8, L13, L15, L17, L19, L21, L23, L7, L9, M10, M14, M16, M18, M20, M8, N15, N17, N19, N21, N7, P10, P12, P14, P16, P18, P20, P8, R13, R15, R17, R19, R7, R9, T10, T14, T16, T18, T21, T8, U15, U17, U19, U21, U9, V10, V12, V14, V18, V8, W11, W13, W16, W20, W9, Y10, Y12, Y15, Y17, Y19, Y21, Y8

(1) This pin must always be connected via a 1-μF ±10% capacitor to VSS.

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5.4 Pin Multiplexing

注

Many device pins support multiple signal functions. Some signal functions are selected via a single layer of multiplexers associated with pins. Other signal functions are selected via two or more layers of multiplexers, where one layer is associated with the pins and other layers are associated with peripheral logic functions.

表 5-125, *Pin Multiplexing* only describes signal multiplexing at the pins. For more information, related to signal multiplexing at the pins, see *Pad Configuration Registers* section in *Device Configuration* chapter in the device TRM. Refer to the respective peripheral chapter in the device TRM for information associated with peripheral signal multiplexing.

注

When a pad is set into a pin multiplexing mode which is not defined, that pad's behavior is undefined. This should be avoided.

注

表 5-125, *Pin Multiplexing* does not include SerDes signal functions. For more information, refer to the Serializer/Deserializer (SerDes) chapter in the device TRM.

注

表 5-125, *Pin Multiplexing* does not include DPHY_TX signal functions. For more information, refer to the Shared D-PHY Transmitter (DPHY_TX) chapter in the device TRM.

For more information on the I/O cell configurations, see *Pad Configuration Registers* section in *Device Configuration* chapter in the device TRM.

表 5-125. Pin Multiplexing

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x00011C294	PADCONFIG165	AD1	MLB0_MLBSP							GPIO1_30								
0x00011C29C	PADCONFIG167	AC3	MLB0_MLBDP							GPIO1_32								
0x00011C290	PADCONFIG164	U6	USB0_DRVVBUS	USB1_DRVVBUS						GPIO1_29								
0x00011C298	PADCONFIG166	AC1	MLB0_MLBSN							GPIO1_31								
0x00011C2A0	PADCONFIG168	AD3	MLB0_MLBDN							GPIO1_33								

表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x00011C2A4	PADCONFIG169	AD2	MLB0_MLBCP							GPIO1_34								
0x00011C2A8	PADCONFIG170	AE2	MLB0_MLBCN							GPIO1_35								
0x00011C000	PADCONFIG0	AC18	EXTINTn							GPIO0_0								
0x00011C004	PADCONFIG1	AC23	PRG1_PRU0_GPO0	PRG1_PRU0_GPI0	PRG1_RGMII1_RD0	PRG1_PWM3_A0	RGMII1_RD0	RMII1_RXD0		GPIO0_1	GPMC0_BE1n	RGMII7_RD0			MCASP6_ACLKX		UART0_RXD	
0x00011C008	PADCONFIG2	AG22	PRG1_PRU0_GPO1	PRG1_PRU0_GPI1	PRG1_RGMII1_RD1	PRG1_PWM3_B0	RGMII1_RD1	RMII1_RXD1		GPIO0_2	GPMC0_WAIT0	RGMII7_RD1			MCASP6_AFSX		UART0_TXD	
0x00011C00C	PADCONFIG3	AF22	PRG1_PRU0_GPO2	PRG1_PRU0_GPI2	PRG1_RGMII1_RD2	PRG1_PWM2_A0	RGMII1_RD2	RMII1_CRS_DV		GPIO0_3	GPMC0_WAIT1	RGMII7_RD2			MCASP6_AXR0		UART1_RXD	
0x00011C010	PADCONFIG4	AJ23	PRG1_PRU0_GPO3	PRG1_PRU0_GPI3	PRG1_RGMII1_RD3	PRG1_PWM3_A2	RGMII1_RD3	RMII1_RX_ER		GPIO0_4	GPMC0_DIR	RGMII7_RD3			MCASP6_AXR1		UART1_TXD	
0x00011C014	PADCONFIG5	AH23	PRG1_PRU0_GPO4	PRG1_PRU0_GPI4	PRG1_RGMII1_RX_CTL	PRG1_PWM2_B0	RGMII1_RX_CTL	RMII1_TXD0		GPIO0_5	GPMC0_CSn2	RGMII7_RX_CTL			MCASP6_AXR2	MCASP6_ACLKR	UART2_RXD	
0x00011C018	PADCONFIG6	AD20	PRG1_PRU0_GPO5	PRG1_PRU0_GPI5		PRG1_PWM3_B2		RMII1_TX_EN		GPIO0_6	GPMC0_WEn				MCASP3_AXR0			BOOTMODE0
0x00011C01C	PADCONFIG7	AD22	PRG1_PRU0_GPO6	PRG1_PRU0_GPI6	PRG1_RGMII1_RXC	PRG1_PWM3_A1	RGMII1_RXC	RMII1_TXD1	AUDIO_EXT_REFCLK0	GPIO0_7	GPMC0_CSn3	RGMII7_RXC			MCASP6_AXR3	MCASP6_AFSR	UART2_TXD	
0x00011C020	PADCONFIG8	AE20	PRG1_PRU0_GPO7	PRG1_PRU0_GPI7	PRG1_IEP0_EDC_LATCH_IN1	PRG1_PWM3_B1		AUDIO_EXT_REFCLK1	MCAN4_TX	GPIO0_8					MCASP3_AXR1			
0x00011C024	PADCONFIG9	AJ20	PRG1_PRU0_GPO8	PRG1_PRU0_GPI8		PRG1_PWM2_A1		RMII5_RXD0	MCAN4_RX	GPIO0_9	GPMC0_OEn_REn		VOUT0_DATA22		MCASP3_AXR2			
0x00011C028	PADCONFIG10	AG20	PRG1_PRU0_GPO9	PRG1_PRU0_GPI9	PRG1_UART0_CTSn	PRG1_PWM3_TZ_IN	SPI6_CS1	RMII5_RXD1		GPIO0_10	GPMC0_ADVn_ALE	PRG1_IEP0_EDIO_DATA_IN_OUT28	VOUT0_DATA23		MCASP3_ACLKX			
0x00011C02C	PADCONFIG11	AD21	PRG1_PRU0_GPO10	PRG1_PRU0_GPI10	PRG1_UART0_RTSn	PRG1_PWM2_B1	SPI6_CS2	RMII5_CRS_DV		GPIO0_11	GPMC0_BE0n_CLE	PRG1_IEP0_EDIO_DATA_IN_OUT29	OBSCLK2		MCASP3_AFSX			
0x00011C030	PADCONFIG12	AF24	PRG1_PRU0_GPO11	PRG1_PRU0_GPI11	PRG1_RGMII1_TD0	PRG1_PWM3_TZ_OUT	RGMII1_TD0		MCAN4_TX	GPIO0_12		RGMII7_TD0	VOUT0_DATA16	VPFE0_DATA0	MCASP7_ACLKX			
0x00011C034	PADCONFIG13	AJ24	PRG1_PRU0_GPO12	PRG1_PRU0_GPI12	PRG1_RGMII1_TD1	PRG1_PWM0_A0	RGMII1_TD1		MCAN4_RX	GPIO0_13		RGMII7_TD1	VOUT0_DATA17	VPFE0_DATA1	MCASP7_AFSX			
0x00011C038	PADCONFIG14	AG24	PRG1_PRU0_GPO13	PRG1_PRU0_GPI13	PRG1_RGMII1_TD2	PRG1_PWM0_B0	RGMII1_TD2		MCAN5_TX	GPIO0_14		RGMII7_TD2	VOUT0_DATA18	VPFE0_DATA2	MCASP7_AXR0			
0x00011C03C	PADCONFIG15	AD24	PRG1_PRU0_GPO14	PRG1_PRU0_GPI14	PRG1_RGMII1_TD3	PRG1_PWM0_A1	RGMII1_TD3		MCAN5_RX	GPIO0_15		RGMII7_TD3	VOUT0_DATA19	VPFE0_DATA3	MCASP7_AXR1			

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表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x00011C040	PADCONFIG16	AC24	PRG1_PRU0_GPO15	PRG1_PRU0_GPI15	PRG1_RGMII1_TX_CTL	PRG1_PWM0_B1	RGMII1_TX_CTL		MCAN6_TX	GPIO0_16		RGMII7_TX_CTL	VOUT0_DATA20	VPFE0_DATA4	MCASP7_AXR2	MCASP7_ACLKR		
0x00011C044	PADCONFIG17	AE24	PRG1_PRU0_GPO16	PRG1_PRU0_GPI16	PRG1_RGMII1_TXC	PRG1_PWM0_A2	RGMII1_TXC		MCAN6_RX	GPIO0_17		RGMII7_TXC	VOUT0_DATA21	VPFE0_DATA5	MCASP7_AXR3	MCASP7_AFSR		
0x00011C04C	PADCONFIG19	AJ21	PRG1_PRU0_GPO17	PRG1_PRU0_GPI17	PRG1_IEP0_EDC_SYNC_OUT1	PRG1_PWM0_B2		RMII5_TXD1	MCAN5_TX	GPIO0_18				VPFE0_DATA6	MCASP3_AXR3			
0x00011C050	PADCONFIG20	AE21	PRG1_PRU0_GPO18	PRG1_PRU0_GPI18	PRG1_IEP0_EDC_LATCH_IN0	PRG1_PWM0_TZ_IN		RMII5_RX_ER	MCAN5_RX	GPIO0_19				VPFE0_DATA7	MCASP4_ACLKX			
0x00011C054	PADCONFIG21	AH21	PRG1_PRU0_GPO19	PRG1_PRU0_GPI19	PRG1_IEP0_EDC_SYNC_OUT0	PRG1_PWM0_TZ_OUT		RMII5_TXD0	MCAN6_TX	GPIO0_20			VOUT0_EXTPCLKIN	VPFE0_PCLK	MCASP4_AFSX			
0x00011C058	PADCONFIG22	AE22	PRG1_PRU1_GPO0	PRG1_PRU1_GPI0	PRG1_RGMII2_RD0		RGMII2_RD0	RMII2_RXD0		GPIO0_21	RGMII8_RD0		VOUT0_DATA0	VPFE0_HD	MCASP8_ACLKX			
0x00011C05C	PADCONFIG23	AG23	PRG1_PRU1_GPO1	PRG1_PRU1_GPI1	PRG1_RGMII2_RD1		RGMII2_RD1	RMII2_RXD1		GPIO0_22	RGMII8_RD1		VOUT0_DATA1	VPFE0_FIELD	MCASP8_AFSX			
0x00011C060	PADCONFIG24	AF23	PRG1_PRU1_GPO2	PRG1_PRU1_GPI2	PRG1_RGMII2_RD2	PRG1_PWM2_A2	RGMII2_RD2	RMII2_CRS_DV		GPIO0_23	RGMII8_RD2		VOUT0_DATA2	VPFE0_VD	MCASP8_AXR0	MCASP3_ACLKR		
0x00011C064	PADCONFIG25	AD23	PRG1_PRU1_GPO3	PRG1_PRU1_GPI3	PRG1_RGMII2_RD3		RGMII2_RD3	RMII2_RX_ER		GPIO0_24	RGMII8_RD3	EQEP1_A	VOUT0_DATA3	VPFE0_WEN	MCASP8_AXR1	MCASP3_AFSR	TIMER_IO2	
0x00011C068	PADCONFIG26	AH24	PRG1_PRU1_GPO4	PRG1_PRU1_GPI4	PRG1_RGMII2_RX_CTL	PRG1_PWM2_B2	RGMII2_RX_CTL	RMII2_TXD0		GPIO0_25	RGMII8_RX_CTL	EQEP1_B	VOUT0_DATA4	VPFE0_DATA13	MCASP8_AXR2	MCASP8_ACLKR	TIMER_IO3	
0x00011C06C	PADCONFIG27	AG21	PRG1_PRU1_GPO5	PRG1_PRU1_GPI5				RMII5_TX_EN	MCAN6_RX	GPIO0_26	GPMC0_WPn	EQEP1_S	VOUT0_DATA5		MCASP4_AXR0		TIMER_IO4	
0x00011C070	PADCONFIG28	AE23	PRG1_PRU1_GPO6	PRG1_PRU1_GPI6	PRG1_RGMII2_RXC		RGMII2_RXC	RMII2_TXD1		GPIO0_27	RGMII8_RXC		VOUT0_DATA6	VPFE0_DATA14	MCASP8_AXR3	MCASP8_AFSR	TIMER_IO5	
0x00011C074	PADCONFIG29	AC21	PRG1_PRU1_GPO7	PRG1_PRU1_GPI7	PRG1_IEP1_EDC_LATCH_IN1		SPI6_CS0	RMII6_RX_ER	MCAN7_TX	GPIO0_28			VOUT0_DATA7	VPFE0_DATA15	MCASP4_AXR1		UART3_TXD	
0x00011C078	PADCONFIG30	Y23	PRG1_PRU1_GPO8	PRG1_PRU1_GPI8		PRG1_PWM2_TZ_OUT		RMII6_RXD0	MCAN7_RX	GPIO0_29	GPMC0_CSn1		VOUT0_DATA8		MCASP4_AXR2		UART3_RXD	
0x00011C07C	PADCONFIG31	AF21	PRG1_PRU1_GPO9	PRG1_PRU1_GPI9	PRG1_UART0_RXD		SPI6_CS3	RMII6_RXD1	MCAN8_TX	GPIO0_30	GPMC0_CSn0	PRG1_IEP0_EDIO_DATA_IN_OUT30	VOUT0_DATA9		MCASP4_AXR3			
0x00011C080	PADCONFIG32	AB23	PRG1_PRU1_GPO10	PRG1_PRU1_GPI10	PRG1_UART0_TXD	PRG1_PWM2_TZ_IN		RMII6_CRS_DV	MCAN8_RX	GPIO0_31	GPMC0_CLKOUT	PRG1_IEP0_EDIO_DATA_IN_OUT31	VOUT0_DATA10	GPMC0_FCLK_MUX	MCASP5_ACLKX			
0x00011C084	PADCONFIG33	AJ25	PRG1_PRU1_GPO11	PRG1_PRU1_GPI11	PRG1_RGMII2_TD0		RGMII2_TD0	RMII2_TX_EN		GPIO0_32	RGMII8_TD0	EQEP1_I	VOUT0_DATA11		MCASP9_ACLKX			
0x00011C088	PADCONFIG34	AH25	PRG1_PRU1_GPO12	PRG1_PRU1_GPI12	PRG1_RGMII2_TD1	PRG1_PWM1_A0	RGMII2_TD1		MCAN7_TX	GPIO0_33	RGMII8_TD1		VOUT0_DATA12		MCASP9_AFSX			

表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x00011C08C	PADCONFIG35	AG25	PRG1_PRU1_GPO13	PRG1_PRU1_GPI13	PRG1_RGMII2_TD2	PRG1_PWM1_B0	RGMII2_TD2		MCAN7_RX	GPIO0_34	RGMII8_TD2		VOUT0_DATA13	VPFE0_DATA8	MCASP9_AXR0	MCASP4_ACLKR		
0x00011C090	PADCONFIG36	AH26	PRG1_PRU1_GPO14	PRG1_PRU1_GPI14	PRG1_RGMII2_TD3	PRG1_PWM1_A1	RGMII2_TD3		MCAN8_TX	GPIO0_35	RGMII8_TD3		VOUT0_DATA14		MCASP9_AXR1	MCASP4_AFSR		
0x00011C094	PADCONFIG37	AJ27	PRG1_PRU1_GPO15	PRG1_PRU1_GPI15	PRG1_RGMII2_TX_CTL	PRG1_PWM1_B1	RGMII2_TX_CTL		MCAN8_RX	GPIO0_36	RGMII8_TX_CTL		VOUT0_DATA15	VPFE0_DATA9	MCASP9_AXR2	MCASP9_ACLKR		
0x00011C098	PADCONFIG38	AJ26	PRG1_PRU1_GPO16	PRG1_PRU1_GPI16	PRG1_RGMII2_TXC	PRG1_PWM1_A2	RGMII2_TXC			GPIO0_37	RGMII8_TXC	VOUT0_VP2_HSYNC	VOUT0_HSYNC		MCASP9_AXR3	MCASP9_AFSR	VOUT0_VP0_HSYNC	
0x00011C09C	PADCONFIG39	AC22	PRG1_PRU1_GPO17	PRG1_PRU1_GPI17	PRG1_IEP1_EDC_SYNC_OUT1	PRG1_PWM1_B2	SPI6_CLK	RMII6_TX_EN	PRG1_ECAP0_SYNC_OUT	GPIO0_38		VOUT0_VP2_DE	VOUT0_DE	VPFE0_DATA10	MCASP5_AFSX		VOUT0_VP0_DE	BOOTMODE1
0x00011C0A0	PADCONFIG40	AJ22	PRG1_PRU1_GPO18	PRG1_PRU1_GPI18	PRG1_IEP1_EDC_LATCH_IN0	PRG1_PWM1_TZ_IN	SPI6_D0	RMII6_TXD0	PRG1_ECAP0_SYNC_IN	GPIO0_39		VOUT0_VP2_VSYNC	VOUT0_VSYNC		MCASP5_AXR0		VOUT0_VP0_VSYNC	
0x00011C0A4	PADCONFIG41	AH22	PRG1_PRU1_GPO19	PRG1_PRU1_GPI19	PRG1_IEP1_EDC_SYNC_OUT0	PRG1_PWM1_TZ_OUT	SPI6_D1	RMII6_TXD1	PRG1_ECAP0_IN_APWM_OUT	GPIO0_40			VOUT0_PCLK		MCASP5_AXR1			
0x00011C0A8	PADCONFIG42	AD19	PRG1_MDIO0_MDIO	SPI1_CS2	I2C4_SCL					GPIO0_41			DSS_FSYNC1	VPFE0_DATA11	MCASP5_AXR2	MCASP5_ACLKR	UART3_CTSn	
0x00011C0AC	PADCONFIG43	AD18	PRG1_MDIO0_MDC	SPI1_CS3	I2C4_SDA			RMII_REF_CLK		GPIO0_42				VPFE0_DATA12	MCASP5_AXR3	MCASP5_AFSR	UART3_RTSn	
0x00011C0B0	PADCONFIG44	AF28	PRG0_PRU0_GPO0	PRG0_PRU0_GPI0	PRG0_RGMII1_RD0	PRG0_PWM3_A0	RGMII3_RD0	RMII3_RXD1		GPIO0_43					MCASP0_AXR0			
0x00011C0B4	PADCONFIG45	AE28	PRG0_PRU0_GPO1	PRG0_PRU0_GPI1	PRG0_RGMII1_RD1	PRG0_PWM3_B0	RGMII3_RD1	RMII3_RXD0		GPIO0_44					MCASP0_AXR1			
0x00011C0B8	PADCONFIG46	AE27	PRG0_PRU0_GPO2	PRG0_PRU0_GPI2	PRG0_RGMII1_RD2	PRG0_PWM2_A0	RGMII3_RD2	RMII3_CRS_DV		GPIO0_45	UART3_RXD				MCASP0_ACLKR			
0x00011C0BC	PADCONFIG47	AD26	PRG0_PRU0_GPO3	PRG0_PRU0_GPI3	PRG0_RGMII1_RD3	PRG0_PWM3_A2	RGMII3_RD3	RMII3_RX_ER		GPIO0_46	UART3_TXD				MCASP0_AFSR			
0x00011C0C0	PADCONFIG48	AD25	PRG0_PRU0_GPO4	PRG0_PRU0_GPI4	PRG0_RGMII1_RX_CTL	PRG0_PWM2_B0	RGMII3_RX_CTL	RMII3_TXD1		GPIO0_47					MCASP0_AXR2			
0x00011C0C4	PADCONFIG49	AC29	PRG0_PRU0_GPO5	PRG0_PRU0_GPI5		PRG0_PWM3_B2		RMII3_TXD0		GPIO0_48	GPMC0_AD0				MCASP0_AXR3			BOOTMODE2
0x00011C0C8	PADCONFIG50	AE26	PRG0_PRU0_GPO6	PRG0_PRU0_GPI6	PRG0_RGMII1_RXC	PRG0_PWM3_A1	RGMII3_RXC	RMII3_TX_EN		GPIO0_49					MCASP0_AXR4			
0x00011C0CC	PADCONFIG51	AC28	PRG0_PRU0_GPO7	PRG0_PRU0_GPI7	PRG0_IEP0_EDC_LATCH_IN1	PRG0_PWM3_B1	PRG0_ECAP0_SYNC_IN		MCAN9_TX	GPIO0_50	GPMC0_AD1				MCASP0_AXR5			
0x00011C0D0	PADCONFIG52	AC27	PRG0_PRU0_GPO8	PRG0_PRU0_GPI8		PRG0_PWM2_A1			MCAN9_RX	GPIO0_51	GPMC0_AD2				MCASP0_AXR6		UART6_RXD	
0x00011C0D4	PADCONFIG53	AB26	PRG0_PRU0_GPO9	PRG0_PRU0_GPI9	PRG0_UART0_CTSn	PRG0_PWM3_TZ_IN	SPI3_CS1	PRG0_IEP0_EDIO_DATA_IN_OUT28	MCAN10_TX	GPIO0_52	GPMC0_AD3				MCASP0_ACLKX		UART6_TXD	

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表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x00011C0D8	PADCONFIG54	AB25	PRG0_PRU0_GPO10	PRG0_PRU0_GPI10	PRG0_UART0_RTSn	PRG0_PWM2_B1	SPI3_CS2	PRG0_IEP0_EDIO_DATA_IN_OUT29	MCAN10_RX	GPIO0_53	GPMC0_AD4				MCASP0_AFSX			
0x00011C0DC	PADCONFIG55	AJ28	PRG0_PRU0_GPO11	PRG0_PRU0_GPI11	PRG0_RGMII1_TD0	PRG0_PWM3_TZ_OUT	RGMII3_TD0			GPIO0_54		CLKOUT			MCASP0_AXR7			
0x00011C0E0	PADCONFIG56	AH27	PRG0_PRU0_GPO12	PRG0_PRU0_GPI12	PRG0_RGMII1_TD1	PRG0_PWM0_A0	RGMII3_TD1			GPIO0_55			DSS_FSYNC0		MCASP0_AXR8			
0x00011C0E4	PADCONFIG57	AH29	PRG0_PRU0_GPO13	PRG0_PRU0_GPI13	PRG0_RGMII1_TD2	PRG0_PWM0_B0	RGMII3_TD2			GPIO0_56			DSS_FSYNC2		MCASP0_AXR9			
0x00011C0E8	PADCONFIG58	AG28	PRG0_PRU0_GPO14	PRG0_PRU0_GPI14	PRG0_RGMII1_TD3	PRG0_PWM0_A1	RGMII3_TD3			GPIO0_57	UART4_RXD				MCASP0_AXR10			
0x00011C0EC	PADCONFIG59	AG27	PRG0_PRU0_GPO15	PRG0_PRU0_GPI15	PRG0_RGMII1_TX_CTL	PRG0_PWM0_B1	RGMII3_TX_CTL			GPIO0_58	UART4_TXD		DSS_FSYNC3		MCASP0_AXR11			
0x00011C0F0	PADCONFIG60	AH28	PRG0_PRU0_GPO16	PRG0_PRU0_GPI16	PRG0_RGMII1_TXC	PRG0_PWM0_A2	RGMII3_TXC			GPIO0_59			DSS_FSYNC1		MCASP0_AXR12			
0x00011C0F4	PADCONFIG61	AB24	PRG0_PRU0_GPO17	PRG0_PRU0_GPI17	PRG0_IEP0_EDC_SYNC_OUT1	PRG0_PWM0_B2	PRG0_ECAP0_SYNC_OUT			GPIO0_60	GPMC0_AD5	OBSCLK1			MCASP0_AXR13			BOOTMODE7
0x00011C0F8	PADCONFIG62	AB29	PRG0_PRU0_GPO18	PRG0_PRU0_GPI18	PRG0_IEP0_EDC_LATCH_IN0	PRG0_PWM0_TZ_IN	PRG0_ECAP0_IN_APWM_OUT			GPIO0_61	GPMC0_AD6				MCASP0_AXR14			
0x00011C0FC	PADCONFIG63	AB28	PRG0_PRU0_GPO19	PRG0_PRU0_GPI19	PRG0_IEP0_EDC_SYNC_OUT0	PRG0_PWM0_TZ_OUT				GPIO0_62	GPMC0_AD7				MCASP0_AXR15			
0x00011C100	PADCONFIG64	AE29	PRG0_PRU1_GPO0	PRG0_PRU1_GPI0	PRG0_RGMII2_RD0		RGMII4_RD0	RMII4_RXD0		GPIO0_63	UART4_CTSn				MCASP1_AXR0		UART5_RXD	
0x00011C104	PADCONFIG65	AD28	PRG0_PRU1_GPO1	PRG0_PRU1_GPI1	PRG0_RGMII2_RD1		RGMII4_RD1	RMII4_RXD1		GPIO0_64	UART4_RTSn				MCASP1_AXR1		UART5_TXD	
0x00011C108	PADCONFIG66	AD27	PRG0_PRU1_GPO2	PRG0_PRU1_GPI2	PRG0_RGMII2_RD2	PRG0_PWM2_A2	RGMII4_RD2	RMII4_CRS_DV		GPIO0_65	GPMC0_A23				MCASP1_ACLKR	MCASP1_AXR10		
0x00011C10C	PADCONFIG67	AC25	PRG0_PRU1_GPO3	PRG0_PRU1_GPI3	PRG0_RGMII2_RD3		RGMII4_RD3	RMII4_RX_ER		GPIO0_66					MCASP1_AFSR	MCASP1_AXR11		
0x00011C110	PADCONFIG68	AD29	PRG0_PRU1_GPO4	PRG0_PRU1_GPI4	PRG0_RGMII2_RX_CTL	PRG0_PWM2_B2	RGMII4_RX_CTL	RMII4_TXD1		GPIO0_67	GPMC0_A24				MCASP1_AXR2			
0x00011C114	PADCONFIG69	AB27	PRG0_PRU1_GPO5	PRG0_PRU1_GPI5						GPIO0_68	GPMC0_AD8				MCASP1_ACLKX			BOOTMODE6
0x00011C118	PADCONFIG70	AC26	PRG0_PRU1_GPO6	PRG0_PRU1_GPI6	PRG0_RGMII2_RXC		RGMII4_RXC	RMII4_TXD0		GPIO0_69	GPMC0_A25				MCASP1_AXR3			
0x00011C11C	PADCONFIG71	AA24	PRG0_PRU1_GPO7	PRG0_PRU1_GPI7	PRG0_IEP1_EDC_LATCH_IN1		SPI3_CS0		MCAN11_TX	GPIO0_70	GPMC0_AD9				MCASP1_AXR4		UART2_TXD	

表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x00011C120	PADCONFIG72	AA28	PRG0_PRU1_GPO8	PRG0_PRU1_GPI8		PRG0_PWM2_TZ_OUT			MCAN11_RX	GPIO0_71	GPMC0_AD10				MCASP1_AFSX			
0x00011C124	PADCONFIG73	Y24	PRG0_PRU1_GPO9	PRG0_PRU1_GPI9	PRG0_UART0_RXD		SPI3_CS3		PRG0_IEP0_EDIO_DATA_IN_OUT30	GPIO0_72	GPMC0_AD11		DSS_FSYNC3		MCASP1_AXR5		UART8_RXD	
0x00011C128	PADCONFIG74	AA25	PRG0_PRU1_GPO10	PRG0_PRU1_GPI10	PRG0_UART0_TXD	PRG0_PWM2_TZ_IN			PRG0_IEP0_EDIO_DATA_IN_OUT31	GPIO0_73	GPMC0_AD12	CLKOUT			MCASP1_AXR6		UART8_TXD	
0x00011C12C	PADCONFIG75	AG26	PRG0_PRU1_GPO11	PRG0_PRU1_GPI11	PRG0_RGMII2_TD0		RGMII4_TD0	RMII4_TX_EN		GPIO0_74	GPMC0_A26				MCASP1_AXR7			
0x00011C130	PADCONFIG76	AF27	PRG0_PRU1_GPO12	PRG0_PRU1_GPI12	PRG0_RGMII2_TD1	PRG0_PWM1_A0	RGMII4_TD1			GPIO0_75					MCASP1_AXR8		UART8_CTSn	
0x00011C134	PADCONFIG77	AF26	PRG0_PRU1_GPO13	PRG0_PRU1_GPI13	PRG0_RGMII2_TD2	PRG0_PWM1_B0	RGMII4_TD2			GPIO0_76					MCASP1_AXR9		UART8_RTSn	
0x00011C138	PADCONFIG78	AE25	PRG0_PRU1_GPO14	PRG0_PRU1_GPI14	PRG0_RGMII2_TD3	PRG0_PWM1_A1	RGMII4_TD3			GPIO0_77					MCASP2_AXR0		UART2_CTSn	
0x00011C13C	PADCONFIG79	AF29	PRG0_PRU1_GPO15	PRG0_PRU1_GPI15	PRG0_RGMII2_TX_CTL	PRG0_PWM1_B1	RGMII4_TX_CTL			GPIO0_78					MCASP2_AXR1		UART2_RTSn	
0x00011C140	PADCONFIG80	AG29	PRG0_PRU1_GPO16	PRG0_PRU1_GPI16	PRG0_RGMII2_TXC	PRG0_PWM1_A2	RGMII4_TXC			GPIO0_79					MCASP2_AXR2			
0x00011C144	PADCONFIG81	Y25	PRG0_PRU1_GPO17	PRG0_PRU1_GPI17	PRG0_IEP1_EDC_SYNC_OUT1	PRG0_PWM1_B2	SPI3_CLK			GPIO0_80	GPMC0_AD13				MCASP2_AXR3			BOOTMODE3
0x00011C148	PADCONFIG82	AA26	PRG0_PRU1_GPO18	PRG0_PRU1_GPI18	PRG0_IEP1_EDC_LATCH_IN0	PRG0_PWM1_TZ_IN	SPI3_D0		MCAN12_TX	GPIO0_81	GPMC0_AD14				MCASP2_AFSX		UART2_RXD	
0x00011C14C	PADCONFIG83	AA29	PRG0_PRU1_GPO19	PRG0_PRU1_GPI19	PRG0_IEP1_EDC_SYNC_OUT0	PRG0_PWM1_TZ_OUT	SPI3_D1		MCAN12_RX	GPIO0_82	GPMC0_AD15				MCASP2_ACLKX			
0x00011C150	PADCONFIG84	Y26	PRG0_MDIO0_MDIO		I2C5_SCL				MCAN13_TX	GPIO0_83	GPMC0_A27		DSS_FSYNC0		MCASP2_AFSR	MCASP2_AXR4		
0x00011C154	PADCONFIG85	AA27	PRG0_MDIO0_MDC		I2C5_SDA				MCAN13_RX	GPIO0_84	GPMC0_A0		DSS_FSYNC2		MCASP2_ACLKR	MCASP2_AXR5		
0x00011C158	PADCONFIG86	U23	RGMII5_TX_CTL	RMII7_CRS_DV	I2C2_SCL		VOUT1_DATA0	TRC_CLK	EHRPWM0_SYNCI	GPIO0_85	GPMC0_A1				MCASP10_ACLKX			
0x00011C15C	PADCONFIG87	U26	RGMII5_RX_CTL	RMII7_RX_ER	I2C2_SDA		VOUT1_DATA1	TRC_CTL	EHRPWM0_SYNCO	GPIO0_86	GPMC0_A2				MCASP10_AFSX			
0x00011C160	PADCONFIG88	V28	RGMII5_TD3	UART3_RXD		SYNC2_OUT	VOUT1_DATA2	TRC_DATA0	EHRPWM_TZn_IN0	GPIO0_87	GPMC0_A3				MCASP10_AXR0			
0x00011C164	PADCONFIG89	V29	RGMII5_TD2	UART3_TXD		SYNC3_OUT	VOUT1_DATA3	TRC_DATA1	EHRPWM0_A	GPIO0_88	GPMC0_A4				MCASP10_AXR1			

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表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x00011C168	PADCONFIG90	V27	RGMII5_TD1	RMII7_TXD1	I2C3_SCL		VOUT1_DATA4	TRC_DATA2	EHRPWM0_B	GPIO0_89	GPMC0_A5				MCASP11_ACLKX			
0x00011C16C	PADCONFIG91	U28	RGMII5_TD0	RMII7_TXD0	I2C3_SDA		VOUT1_DATA5	TRC_DATA3	EHRPWM1_A	GPIO0_90	GPMC0_A6				MCASP11_AFSX			
0x00011C170	PADCONFIG92	U29	RGMII5_TXC	RMII7_TX_EN	I2C6_SCL		VOUT1_DATA6	TRC_DATA4	EHRPWM1_B	GPIO0_91	GPMC0_A7				MCASP10_AXR2			
0x00011C174	PADCONFIG93	U25	RGMII5_RXC		I2C6_SDA		VOUT1_DATA7	TRC_DATA5	EHRPWM_TZn_IN1	GPIO0_92	GPMC0_A8				MCASP10_AXR3		EHRPWM_SOCA	
0x00011C178	PADCONFIG94	U27	RGMII5_RD3	UART3_CTSn		UART6_RXD	VOUT1_DATA8	TRC_DATA6	EHRPWM2_A	GPIO0_93	GPMC0_A9				MCASP11_AXR0			
0x00011C17C	PADCONFIG95	U24	RGMII5_RD2	UART3_RTSn		UART6_TXD	VOUT1_DATA9	TRC_DATA7	EHRPWM2_B	GPIO0_94	GPMC0_A10				MCASP11_AXR1			
0x00011C180	PADCONFIG96	R23	RGMII5_RD1	RMII7_RXD1		UART6_CTSn	VOUT1_DATA10	TRC_DATA8	EHRPWM_TZn_IN2	GPIO0_95	GPMC0_A11				MCASP11_AXR2		EHRPWM_SOCB	
0x00011C184	PADCONFIG97	T23	RGMII5_RD0	RMII7_RXD0		UART6_RTSn	VOUT1_DATA11	TRC_DATA9		GPIO0_96	GPMC0_A12				MCASP11_AXR3			
0x00011C188	PADCONFIG98	Y28	RGMII6_TX_CTL	RMII8_CRS_DV			VOUT1_DATA12	TRC_DATA10		GPIO0_97	GPMC0_A13				MCASP10_ACLKR			
0x00011C18C	PADCONFIG99	V23	RGMII6_RX_CTL	RMII8_RX_ER			VOUT1_DATA13	TRC_DATA11	EHRPWM3_A	GPIO0_98	GPMC0_A14				MCASP10_AFSR			
0x00011C190	PADCONFIG100	W23	RGMII6_TD3	UART4_RXD		SPI5_CS3	VOUT1_DATA14	TRC_DATA12	EHRPWM3_B	GPIO0_99	GPMC0_A15				MCASP11_ACLKR			
0x00011C194	PADCONFIG101	W28	RGMII6_TD2	UART4_TXD		SPI5_CS2	VOUT1_DATA15	TRC_DATA13	EHRPWM3_SYNCI	GPIO0_100	GPMC0_A16				MCASP11_AFSR			
0x00011C198	PADCONFIG102	V25	RGMII6_TD1	RMII8_TXD1		SPI5_D0	VOUT1_VSYNC	TRC_DATA14	EHRPWM3_SYNCO	GPIO0_101	GPMC0_A17	VOUT1_VP0_VSYNC			MCASP10_AXR4			
0x00011C19C	PADCONFIG103	W27	RGMII6_TD0	RMII8_TXD0		SPI5_CS0	VOUT1_HSYNC	TRC_DATA15	EHRPWM_TZn_IN3	GPIO0_102	GPMC0_A18	VOUT1_VP0_HSYNC			MCASP10_AXR5			
0x00011C1A0	PADCONFIG104	W29	RGMII6_TXC	RMII8_TX_EN		SPI5_CLK	VOUT1_PCLK	TRC_DATA16	EHRPWM4_A	GPIO0_103	GPMC0_A19				MCASP10_AXR6			
0x00011C1A4	PADCONFIG105	W26	RGMII6_RXC			AUDIO_EXT_REFCLK2	VOUT1_DE	TRC_DATA17	EHRPWM4_B	GPIO0_104	GPMC0_A20	VOUT1_VP0_DE			MCASP10_AXR7			
0x00011C1A8	PADCONFIG106	Y29	RGMII6_RD3	UART4_CTSn		UART5_RXD	CLKOUT	TRC_DATA18	EHRPWM_TZn_IN4	GPIO0_105	GPMC0_A21				MCASP11_AXR4			
0x00011C1AC	PADCONFIG107	Y27	RGMII6_RD2	UART4_RTSn		UART5_TXD		TRC_DATA19	EHRPWM5_A	GPIO0_106	GPMC0_A22				MCASP11_AXR5			
0x00011C1B0	PADCONFIG108	W24	RGMII6_RD1	RMII8_RXD1		SPI5_D1	VOUT1_EXTPCLKIN	TRC_DATA20	EHRPWM5_B	GPIO0_107	GPMC0_BE1n				MCASP11_AXR6			
0x00011C1B4	PADCONFIG109	W25	RGMII6_RD0	RMII8_RXD0		SPI5_CS1	AUDIO_EXT_REFCLK3	TRC_DATA21	EHRPWM_TZn_IN5	GPIO0_108	GPMC0_DIR				MCASP11_AXR7			
0x00011C1B8	PADCONFIG110	V26	MDIO0_MDIO					TRC_DATA22		GPIO0_109	GPMC0_WAIT3							

表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x00011C1BC	PADCONFIG111	V24	MDIO0_MDC					TRC_DATA23		GPIO0_110	GPMC0_WAIT2							
0x00011C1C0	PADCONFIG112	AA2	SPI0_CS0	UART0_RTSn						GPIO0_111								
0x00011C1C4	PADCONFIG113	Y4	SPI0_CS1	CPTS0_TS_COMP	I2C3_SCL			DP0_HPD	PRG1_IEP0_EDIO_OUTVALID	GPIO0_112								
0x00011C1C8	PADCONFIG114	AA1	SPI0_CLK	UART1_CTSn	I2C2_SCL					GPIO0_113								
0x00011C1CC	PADCONFIG115	AB5	SPI0_D0	UART1_RTSn	I2C2_SDA					GPIO0_114								
0x00011C1D0	PADCONFIG116	AA3	SPI0_D1		I2C6_SCL					GPIO0_115								
0x00011C1D4	PADCONFIG117	Y3	SPI1_CS0	UART0_CTSn		UART5_RXD			PRG0_IEP0_EDIO_OUTVALID	GPIO0_116	PRG0_IEP0_EDC_LATCH_IN0							
0x00011C1D8	PADCONFIG118	W4	SPI1_CS1	CPTS0_TS_SYNC	I2C3_SDA	UART5_TXD				GPIO0_117								
0x00011C1DC	PADCONFIG119	Y1	SPI1_CLK	UART5_CTSn	I2C4_SDA	UART2_RXD				GPIO0_118	PRG0_IEP0_EDC_SYNC_OUT0							
0x00011C1E0	PADCONFIG120	Y5	SPI1_D0	UART5_RTSn	I2C4_SCL	UART2_TXD				GPIO0_119	PRG0_IEP1_EDC_LATCH_IN0							
0x00011C1E4	PADCONFIG121	Y2	SPI1_D1		I2C6_SDA					GPIO0_120	PRG0_IEP1_EDC_SYNC_OUT0							
0x00011C1E8	PADCONFIG122	AB2	UART0_RXD				SPI2_CS1			GPIO0_121								
0x00011C1EC	PADCONFIG123	AB3	UART0_TXD				SPI2_CS2		SPI7_CS1	GPIO0_122								
0x00011C1F0	PADCONFIG124	AC2	UART0_CTSn	TIMER_IO6	SPI0_CS2	MCAN2_RX	SPI2_CS0	EQEP0_A		GPIO0_123								
0x00011C1F4	PADCONFIG125	AB1	UART0_RTSn	TIMER_IO7	SPI0_CS3	MCAN2_TX	SPI2_CLK	EQEP0_B		GPIO0_124								
0x00011C1F8	PADCONFIG126	AA4	UART1_RXD						SPI7_CS2	GPIO0_125								
0x00011C1FC	PADCONFIG127	AB4	UART1_TXD					I3C0_SDAPULLEN	SPI7_CS3	GPIO0_126								
0x00011C200	PADCONFIG128	AC4	UART1_CTSn	MCAN3_RX			SPI2_D0	EQEP0_S		GPIO0_127								
0x00011C204	PADCONFIG129	AD5	UART1_RTSn	MCAN3_TX			SPI2_D1	EQEP0_I		GPIO1_0								
0x00011C208	PADCONFIG130	W5	MCAN0_RX				I2C2_SCL			GPIO1_1								
0x00011C20C	PADCONFIG131	W6	MCAN0_TX				I2C2_SDA			GPIO1_2								

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表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x00011C210	PADCONFIG132	W3	MCAN1_RX	UART6_CTSn	UART9_RXD	USB0_DRVVBUS	USB1_DRVVBUS			GPIO1_3								
0x00011C214	PADCONFIG133	V4	MCAN1_TX	UART6_RTSn	UART9_TXD	USB0_DRVVBUS	USB1_DRVVBUS			GPIO1_4								
0x00011C218	PADCONFIG134	W2	I3C0_SCL	MMC2_SDCD	UART9_CTSn	MCAN2_RX	I2C6_SCL	DP0_HPD	PCIE0_CLKREQn	GPIO1_5	UART6_RXD							
0x00011C21C	PADCONFIG135	W1	I3C0_SDA	MMC2_SDWP	UART9_RTSn	MCAN2_TX	I2C6_SDA		PCIE1_CLKREQn	GPIO1_6	UART6_TXD							
0x00011C220	PADCONFIG136	AC5	I2C0_SCL							GPIO1_7								
0x00011C224	PADCONFIG137	AA5	I2C0_SDA							GPIO1_8								
0x00011C228	PADCONFIG138	Y6	I2C1_SCL	CPTS0_HW1TSPUSH						GPIO1_9								
0x00011C22C	PADCONFIG139	AA6	I2C1_SDA	CPTS0_HW2TSPUSH						GPIO1_10								
0x00011C230	PADCONFIG140	U2	ECAP0_IN_APWM_OUT	SYNC0_OUT	CPTS0_RFT_CLK		SPI2_CS3	I3C0_SDAPULLEN	SPI7_CS0	GPIO1_11								
0x00011C234	PADCONFIG141	U3	EXT_REFCLK1	SYNC1_OUT					SPI7_CLK	GPIO1_12								
0x00011C238	PADCONFIG142	V6	TIMER_IO0	ECAP1_IN_APWM_OUT	SYSCLKOUT0				SPI7_D0	GPIO1_13								BOOTMODE4
0x00011C23C	PADCONFIG143	V5	TIMER_IO1	ECAP2_IN_APWM_OUT	OBSCLK0				SPI7_D1	GPIO1_14								BOOTMODE5
0x00011C240	PADCONFIG144	R26	MMC1_DAT3	UART7_RXD						GPIO1_15								
0x00011C244	PADCONFIG145	R25	MMC1_DAT2	UART7_TXD						GPIO1_16								
0x00011C248	PADCONFIG146	P24	MMC1_DAT1	UART7_CTSn	ECAP0_IN_APWM_OUT	TIMER_IO0		UART4_RXD		GPIO1_17								
0x00011C24C	PADCONFIG147	R24	MMC1_DAT0	UART7_RTSn	ECAP1_IN_APWM_OUT	TIMER_IO1		UART4_TXD		GPIO1_18								
0x00011C250	PADCONFIG148	P25	MMC1_CLK	UART8_RXD			I2C4_SCL			GPIO1_19								
0x00011C254	PADCONFIG149	R29	MMC1_CMD	UART8_TXD			I2C4_SDA			GPIO1_20								
0x00011C258	PADCONFIG150	P23	MMC1_SDCD	UART8_CTSn	UART0_DCDn	TIMER_IO2		EQEP2_I	PCIE2_CLKREQn	GPIO1_21	PRG0_IEP0_EDC_LATCH_IN1							

表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x00011C25C	PADCONFIG151	R28	MMC1_SDWP	UART8_RTSn	UART0_DSRn	TIMER_IO3	ECAP2_IN_APWM_OUT	EQEP2_S	PCIE3_CLKREQn	GPIO1_22	PRG0_IEP0_EDC_SYNC_OUT1							
0x00011C260	PADCONFIG152	T28	MMC2_DAT3	UART9_RXD	CPTS0_HW1TSPUSH		I2C5_SCL			GPIO1_23								
0x00011C264	PADCONFIG153	T29	MMC2_DAT2	UART9_TXD	CPTS0_HW2TSPUSH		I2C5_SDA			GPIO1_24								
0x00011C268	PADCONFIG154	T27	MMC2_DAT1	UART9_CTSn	UART0_DTRn	TIMER_IO4	UART6_RXD	EQEP2_A		GPIO1_25	PRG0_IEP1_EDC_LATCH_IN1							
0x00011C26C	PADCONFIG155	T24	MMC2_DAT0	UART9_RTSn	UART0_RIn	TIMER_IO5	UART6_TXD	EQEP2_B		GPIO1_26	PRG0_IEP1_EDC_SYNC_OUT1							
0x00011C270	PADCONFIG156	T26	MMC2_CLK	USB0_DRVVBUS	USB1_DRVVBUS	TIMER_IO6	I2C3_SCL	UART3_RXD		GPIO1_27								
0x00011C274	PADCONFIG157	T25	MMC2_CMD	USB0_DRVVBUS	USB1_DRVVBUS	TIMER_IO7	I2C3_SDA	UART3_TXD		GPIO1_28								
0x00011C278	PADCONFIG158	T6	RESETSTATz															
0x00011C27C	PADCONFIG159	U1	PORz_OUT															
0x00011C280	PADCONFIG160	U4	SOC_SAFETY_ERRORn															
0x00011C284	PADCONFIG161	V1	TDI															
0x00011C288	PADCONFIG162	V3	TDO															
0x00011C28C	PADCONFIG163	V2	TMS															
0x04301C000	WKUP_PADCONFIG0	E20	MCU_OSPI0_CLK	MCU_HYPERBUS0_CK						WKUP_GPIO0_16								
0x04301C004	WKUP_PADCONFIG1	C21	MCU_OSPI0_LBCLKO	MCU_HYPERBUS0_CKn						WKUP_GPIO0_17								
0x04301C008	WKUP_PADCONFIG2	D21	MCU_OSPI0_DQS	MCU_HYPERBUS0_RWDS						WKUP_GPIO0_18								
0x04301C00C	WKUP_PADCONFIG3	D20	MCU_OSPI0_D0	MCU_HYPERBUS0_DQ0						WKUP_GPIO0_19								
0x04301C010	WKUP_PADCONFIG4	G19	MCU_OSPI0_D1	MCU_HYPERBUS0_DQ1						WKUP_GPIO0_20								

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表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x04301C014	WKUP_PADCONFIG5	G20	MCU_OSPI0_D2	MCU_HYPERBUS0_DQ2						WKUP_GPIO0_21								
0x04301C018	WKUP_PADCONFIG6	F20	MCU_OSPI0_D3	MCU_HYPERBUS0_DQ3						WKUP_GPIO0_22								
0x04301C01C	WKUP_PADCONFIG7	F21	MCU_OSPI0_D4	MCU_HYPERBUS0_DQ4						WKUP_GPIO0_23								
0x04301C020	WKUP_PADCONFIG8	E21	MCU_OSPI0_D5	MCU_HYPERBUS0_DQ5						WKUP_GPIO0_24								
0x04301C024	WKUP_PADCONFIG9	B22	MCU_OSPI0_D6	MCU_HYPERBUS0_DQ6						WKUP_GPIO0_25								
0x04301C028	WKUP_PADCONFIG10	G21	MCU_OSPI0_D7	MCU_HYPERBUS0_DQ7						WKUP_GPIO0_26								
0x04301C02C	WKUP_PADCONFIG11	F19	MCU_OSPI0_CSn0	MCU_HYPERBUS0_CSn0						WKUP_GPIO0_27								
0x04301C030	WKUP_PADCONFIG12	E19	MCU_OSPI0_CSn1	MCU_HYPERBUS0_RESETn						WKUP_GPIO0_28								
0x04301C034	WKUP_PADCONFIG13	F22	MCU_OSPI1_CLK							WKUP_GPIO0_29								
0x04301C038	WKUP_PADCONFIG14	A23	MCU_OSPI1_LBCLKO	MCU_OSPI0_CSn2	MCU_HYPERBUS0_RESETOn				MCU_OSPI0_RESET_OUT0	WKUP_GPIO0_30								
0x04301C03C	WKUP_PADCONFIG15	B23	MCU_OSPI1_DQS	MCU_OSPI0_CSn3	MCU_HYPERBUS0_INTn				MCU_OSPI0_ECC_FAIL	WKUP_GPIO0_31								
0x04301C040	WKUP_PADCONFIG16	D22	MCU_OSPI1_D0							WKUP_GPIO0_32								
0x04301C044	WKUP_PADCONFIG17	G22	MCU_OSPI1_D1				MCU_UART0_RXD	MCU_SPI1_CS1		WKUP_GPIO0_33								
0x04301C048	WKUP_PADCONFIG18	D23	MCU_OSPI1_D2				MCU_UART0_TXD	MCU_SPI1_CS2		WKUP_GPIO0_34								
0x04301C04C	WKUP_PADCONFIG19	C23	MCU_OSPI1_D3				MCU_UART0_CTSn	MCU_SPI0_CS1		WKUP_GPIO0_35								
0x04301C050	WKUP_PADCONFIG20	C22	MCU_OSPI1_CSn0							WKUP_GPIO0_36								
0x04301C054	WKUP_PADCONFIG21	E22	MCU_OSPI1_CSn1	MCU_HYPERBUS0_WPn	MCU_TIMER_IO0	MCU_HYPERBUS0_CSn1	MCU_UART0_RTSn	MCU_SPI0_CS2	MCU_OSPI0_RESET_OUT1	WKUP_GPIO0_37								
0x04301C058	WKUP_PADCONFIG22	B27	MCU_RGMII1_TX_CTL	MCU_RMII1_CRS_DV						WKUP_GPIO0_38								

表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x04301C05C	WKUP_PADCONFIG23	C25	MCU_RGMII1_RX_CTL	MCU_RMII1_RX_ER						WKUP_GPIO0_39								
0x04301C060	WKUP_PADCONFIG24	A28	MCU_RGMII1_TD3	MCU_TIMER_IO2		MCU_ADC_EXT_TRIGGER0				WKUP_GPIO0_40								
0x04301C064	WKUP_PADCONFIG25	A27	MCU_RGMII1_TD2	MCU_TIMER_IO3		MCU_ADC_EXT_TRIGGER1				WKUP_GPIO0_41								
0x04301C068	WKUP_PADCONFIG26	A26	MCU_RGMII1_TD1	MCU_RMII1_TXD1						WKUP_GPIO0_42								
0x04301C06C	WKUP_PADCONFIG27	B25	MCU_RGMII1_TD0	MCU_RMII1_TXD0						WKUP_GPIO0_43								
0x04301C070	WKUP_PADCONFIG28	B26	MCU_RGMII1_TXC	MCU_RMII1_TX_EN						WKUP_GPIO0_44								
0x04301C074	WKUP_PADCONFIG29	C24	MCU_RGMII1_RXC	MCU_RMII1_REF_CLK						WKUP_GPIO0_45								
0x04301C078	WKUP_PADCONFIG30	A25	MCU_RGMII1_RD3	MCU_TIMER_IO4						WKUP_GPIO0_46								
0x04301C07C	WKUP_PADCONFIG31	D24	MCU_RGMII1_RD2	MCU_TIMER_IO5						WKUP_GPIO0_47								
0x04301C080	WKUP_PADCONFIG32	A24	MCU_RGMII1_RD1	MCU_RMII1_RXD1						WKUP_GPIO0_48								
0x04301C084	WKUP_PADCONFIG33	B24	MCU_RGMII1_RD0	MCU_RMII1_RXD0						WKUP_GPIO0_49								
0x04301C088	WKUP_PADCONFIG34	E23	MCU_MDIO0_MDIO							WKUP_GPIO0_50								
0x04301C08C	WKUP_PADCONFIG35	F23	MCU_MDIO0_MDC							WKUP_GPIO0_51								
0x04301C090	WKUP_PADCONFIG36	E27	MCU_SPI0_CLK							WKUP_GPIO0_52								MCU_BOOTMODE00
0x04301C094	WKUP_PADCONFIG37	E24	MCU_SPI0_D0							WKUP_GPIO0_53								MCU_BOOTMODE01
0x04301C098	WKUP_PADCONFIG38	E28	MCU_SPI0_D1				MCU_TIMER_IO0			WKUP_GPIO0_54								MCU_BOOTMODE02
0x04301C09C	WKUP_PADCONFIG39	E25	MCU_SPI0_CS0				MCU_TIMER_IO1			WKUP_GPIO0_55								
0x04301C0A0	WKUP_PADCONFIG40	J29	WKUP_UART0_RXD							WKUP_GPIO0_56								
0x04301C0A4	WKUP_PADCONFIG41	J28	WKUP_UART0_TXD							WKUP_GPIO0_57								
0x04301C0A8	WKUP_PADCONFIG42	D29	MCU_MCAN0_TX							WKUP_GPIO0_58								
0x04301C0AC	WKUP_PADCONFIG43	C29	MCU_MCAN0_RX							WKUP_GPIO0_59								

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表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x04301C0B0	WKUP_PADCONFIG44	F26	MCU_SPI1_CLK	MCU_SPI1_CLK						WKUP_GPIO0_0								MCU_BOOTMODE03
0x04301C0B4	WKUP_PADCONFIG45	F25	MCU_SPI1_D0	MCU_SPI1_D0						WKUP_GPIO0_1								MCU_BOOTMODE04
0x04301C0B8	WKUP_PADCONFIG46	F28	MCU_SPI1_D1	MCU_SPI1_D1						WKUP_GPIO0_2								MCU_BOOTMODE05
0x04301C0BC	WKUP_PADCONFIG47	F27	MCU_SPI1_CS0	MCU_SPI1_CS0						WKUP_GPIO0_3								
0x04301C0C0	WKUP_PADCONFIG48	G25	MCU_MCAN1_TX	MCU_MCAN1_TX	MCU_SPI0_CS3	MCU_ADC_EXT_TRIGGER0				WKUP_GPIO0_4								
0x04301C0C4	WKUP_PADCONFIG49	G24	MCU_MCAN1_RX	MCU_MCAN1_RX	MCU_SPI1_CS3	MCU_ADC_EXT_TRIGGER1				WKUP_GPIO0_5								
0x04301C0C8	WKUP_PADCONFIG50	F29	WKUP_UART0_CTSn	WKUP_UART0_CTSn	MCU_CPTS0_HW1TSPUSH	MCU_I2C1_SCL				WKUP_GPIO0_6								
0x04301C0CC	WKUP_PADCONFIG51	G28	WKUP_UART0_RTSn	WKUP_UART0_RTSn	MCU_CPTS0_HW2TSPUSH	MCU_I2C1_SDA				WKUP_GPIO0_7								
0x04301C0D0	WKUP_PADCONFIG52	G27	MCU_I2C1_SCL	MCU_I2C1_SCL	MCU_CPTS0_TS_SYNC	MCU_I3C1_SCL	MCU_TIMER_IO6			WKUP_GPIO0_8								
0x04301C0D4	WKUP_PADCONFIG53	G26	MCU_I2C1_SDA	MCU_I2C1_SDA	MCU_CPTS0_TS_COMP	MCU_I3C1_SDA	MCU_TIMER_IO7			WKUP_GPIO0_9								
0x04301C0D8	WKUP_PADCONFIG54	H26	MCU_EXT_REFCLK0	MCU_EXT_REFCLK0	MCU_UART0_TXD	MCU_ADC_EXT_TRIGGER0	MCU_CPTS0_RFT_CLK	MCU_SYSCLKOUT0		WKUP_GPIO0_10								
0x04301C0DC	WKUP_PADCONFIG55	H27	MCU_OBSCLK0	MCU_OBSCLK0	MCU_UART0_RXD	MCU_ADC_EXT_TRIGGER1	MCU_TIMER_IO1	MCU_I3C1_SDAPULLEN	MCU_CLKOUT0	WKUP_GPIO0_11								
0x04301C0E0	WKUP_PADCONFIG56	G29	MCU_UART0_TXD	MCU_SPI0_CS1						WKUP_GPIO0_12								MCU_BOOTMODE08
0x04301C0E4	WKUP_PADCONFIG57	H28	MCU_UART0_RXD	MCU_SPI1_CS1						WKUP_GPIO0_13								MCU_BOOTMODE09
0x04301C0E8	WKUP_PADCONFIG58	H29	MCU_UART0_CTSn	MCU_SPI0_CS2						WKUP_GPIO0_14								MCU_BOOTMODE06
0x04301C0EC	WKUP_PADCONFIG59	J27	MCU_UART0_RTSn	MCU_SPI1_CS2						WKUP_GPIO0_15								MCU_BOOTMODE07
0x04301C0F0	WKUP_PADCONFIG60	D26	MCU_I3C0_SCL		MCU_UART0_CTSn		MCU_TIMER_IO8			WKUP_GPIO0_60								
0x04301C0F4	WKUP_PADCONFIG61	D25	MCU_I3C0_SDA		MCU_UART0_RTSn		MCU_TIMER_IO9			WKUP_GPIO0_61								
0x04301C0F8	WKUP_PADCONFIG62	J25	WKUP_I2C0_SCL							WKUP_GPIO0_62								
0x04301C0FC	WKUP_PADCONFIG63	H24	WKUP_I2C0_SDA							WKUP_GPIO0_63								

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表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x04301C100	WKUP_PADCONFIG64	J26	MCU_I2C0_SCL							WKUP_GPIO0_64								
0x04301C104	WKUP_PADCONFIG65	H25	MCU_I2C0_SDA							WKUP_GPIO0_65								
0x04301C108	WKUP_PADCONFIG66	E26	MCU_I3C0_SDAPULLEN							WKUP_GPIO0_66								
0x04301C10C	WKUP_PADCONFIG67	G23	PMIC_POWER_EN1					MCU_I3C1_SDAPULLEN		WKUP_GPIO0_67								
0x04301C110	WKUP_PADCONFIG68	D27	MCU_SAFETY_ERRORn															
0x04301C114	WKUP_PADCONFIG69	D28	MCU_RESETz															
0x04301C118	WKUP_PADCONFIG70	C27	MCU_RESETSTATz															
0x04301C11C	WKUP_PADCONFIG71	B28	MCU_PORz_OUT															
0x04301C120	WKUP_PADCONFIG72	E29	TCK															
0x04301C124	WKUP_PADCONFIG73	F24	TRSTn															
0x04301C128	WKUP_PADCONFIG74	C26	EMU0															
0x04301C12C	WKUP_PADCONFIG75	B29	EMU1															
0x04301C130	WKUP_PADCONFIG76	K25	MCU_ADC0_AIN0															
0x04301C134	WKUP_PADCONFIG77	K26	MCU_ADC0_AIN1															
0x04301C138	WKUP_PADCONFIG78	K28	MCU_ADC0_AIN2															
0x04301C13C	WKUP_PADCONFIG79	L28	MCU_ADC0_AIN3															
0x04301C140	WKUP_PADCONFIG80	K24	MCU_ADC0_AIN4															
0x04301C144	WKUP_PADCONFIG81	K27	MCU_ADC0_AIN5															
0x04301C148	WKUP_PADCONFIG82	K29	MCU_ADC0_AIN6															
0x04301C14C	WKUP_PADCONFIG83	L29	MCU_ADC0_AIN7															
0x04301C150	WKUP_PADCONFIG84	N23	MCU_ADC1_AIN0															
0x04301C154	WKUP_PADCONFIG85	M25	MCU_ADC1_AIN1															

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表 5-125. Pin Multiplexing (続き)

ADDRESS	REGISTER NAME	BALL NUMBER	MUXMODE[14:0] SETTINGS															
			0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	Bootstrap
0x04301C158	WKUP_PADCONFIG86	L24	MCU_ADC1_AIN2															
0x04301C15C	WKUP_PADCONFIG87	L26	MCU_ADC1_AIN3															
0x04301C160	WKUP_PADCONFIG88	N24	MCU_ADC1_AIN4															
0x04301C164	WKUP_PADCONFIG89	M24	MCU_ADC1_AIN5															
0x04301C168	WKUP_PADCONFIG90	L25	MCU_ADC1_AIN6															
0x04301C16C	WKUP_PADCONFIG91	L27	MCU_ADC1_AIN7															
0x04301C170	WKUP_PADCONFIG92	C28	RESET_REQz															
0x04301C174	WKUP_PADCONFIG93	J24	PORz															

5.5 Pin Connectivity Requirements

This section describes the Unused/Reserved balls connection requirements.

注

All power balls must be supplied with the voltages specified in セクション 6.4, *Recommended Operating Conditions,* unless otherwise specified in セクション 5.3, *Signal Descriptions*.

注

MMC1_SDCD and MMC2_SDCD must be pulled down for respective MMC modules to work properly as a boot source.

表 5-126. Connectivity Requirements (ALF Package)

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
M29	WKUP_OSC0_XI	Each of these balls must be connected to VSS through a separate external pull resistor to ensure these balls are held to a valid logic low level if unused.
P29	OSC1_XI	
N28	WKUP_LFOSC0_XI	
F24	TRSTn	
K25	MCU_ADC0_AIN0	
K26	MCU_ADC0_AIN1	
K28	MCU_ADC0_AIN2	
L28	MCU_ADC0_AIN3	
K24	MCU_ADC0_AIN4	
K27	MCU_ADC0_AIN5	
K29	MCU_ADC0_AIN6	
L29	MCU_ADC0_AIN7	
N23	MCU_ADC1_AIN0	
M25	MCU_ADC1_AIN1	
L24	MCU_ADC1_AIN2	
L26	MCU_ADC1_AIN3	
N24	MCU_ADC1_AIN4	
M24	MCU_ADC1_AIN5	
L25	MCU_ADC1_AIN6	
L27	MCU_ADC1_AIN7	
B2	DDR0_DQS0P	
E3	DDR0_DQS1P	
M3	DDR0_DQS2P	
R2	DDR0_DQS3P	
M26	VMON_ER_VSYS	
V19	VMON_IR_VEXT	

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表 5-126. Connectivity Requirements (ALF Package) (続き)

BALL NUMBER	BALL NAME	CONNECTION REQUIREMENTS
AE18	SERDES0_REXT	Each of these balls must be connected to VSS through appropriate external pull resistor to ensure these balls are held to a valid logic low level if unused. The resistor value for the SERDES[4:0]_REXT pins is 3.01 kΩ ±1%, for the CSI[1:0]_RXRCALIB, USB[1:0]_RCALIB, and DSI_TXRCALIB pins is 500 Ω ±1%. This is the same connection as during functional mode.
AE13	SERDES1_REXT	
AD13	SERDES2_REXT	
AE8	SERDES3_REXT	
F9	SERDES4_REXT	
F16	CSI0_RXRCALIB	
F15	CSI1_RXRCALIB	
AB6	USB1_RCALIB	
AD9	USB1_RCALIB	
F12	DSI_TXRCALIB	
D28	MCU_RESETz	Each of these balls must be connected to the corresponding power supply through a separate external pull resistor to ensure these balls are held to a valid logic high level if unused. (1)
H23	MCU_PORz	
J24	PORz	
E29	TCK	
V2	TMS	
J25	WKUP_I2C0_SCL	
H24	WKUP_I2C0_SDA	
H25	MCU_I2C0_SDA	
J26	MCU_I2C0_SCL	
Y6	I2C1_SCL	
AA6	I2C1_SDA	
AA5	I2C0_SDA	
AC5	I2C0_SCL	
AC18	EXTINTn	
V1	TDI	
V3	TDO	
B29	EMU1	
C26	EMU0	
B1	DDR0_DQS0N	
E2	DDR0_DQS1N	
M2	DDR0_DQS2N	
R1	DDR0_DQS3N	
AB11	VPP_CORE	Each of these balls must be left unconnected if unused.
F17	VPP_MCU	
AE1	MMC0_CALPAD	
AE2	MLB0_MLBCN	
AD2	MLB0_MLBCP	
AD3	MLB0_MLBDN	
AC3	MLB0_MLBDP	
AC1	MLB0_MLBSN	
AD1	MLB0_MLBSP	

(1) To determine which power supply is associated with any IO refer to 表 5-1, *Pin Attributes*.

表 5-127. Reserved Balls Specific Connection Requirements

BALLS	CONNECTION REQUIREMENTS
A29 / AJ1 / U11 / U12 / U13 / T11 / T12 / T13 / M11 / M12 / M13 / N11 / N12 / N13	These balls do not exist on the package.
N25 / AJ29 / P26 / R27 / AD4 / E18 / F18 / G10 / F11 / N6 / L6 / F6 / E6 / G9 / F10 / AA23 / F13	These balls must be left unconnected.

注

All other unused signal balls **without** Pad Configuration Register can be left unconnected.

注

All other unused signal balls **with** a Pad Configuration Register can be left unconnected with their multiplexing mode set to GPIO input and internal pulldown resistor enabled.

Unused balls are defined as those which only connect to a PCB solder pad. This is the only use case where internal pull resistors are allowed as the only source/sink to hold a valid logic level.

Any balls connected to a via, test point, or PCB trace are considered used and must not depend on the internal pull resistor to hold a valid logic level.

Internal pull resistors are weak and may not source enough current to maintain a valid logic level for some operating conditions. This may be the case when connected to components with leakage to the opposite logic level, or when external noise sources couple to signal traces attached to balls which are only pulled to a valid logic level by the internal resistor. Therefore, external pull resistors may be required to hold a valid logic level on balls with external connections.

If balls are allowed to float between valid logic levels, the input buffer may enter a high-current state which could damage the IO cell.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1) (2)]

PARAMETER		MIN	MAX	UNIT
VDD_CORE	MAIN domain core supply	–0.3	1.05	V
VDD_MCU	MCUSS core supply	–0.3	1.05	V
VDD_CPU	CPU core supply	–0.3	1.05	V
VDDA_0P8_DLL_MMC0	MMC0 DLL analog supply	–0.3	1.05	V
VDDAR_CORE	MAIN domain RAM supply	–0.3	1.05	V
VDDAR_MCU	MCUSS RAM supply	–0.3	1.05	V
VDDAR_CPU	CPU RAM supply	–0.3	1.05	V
VDDA_0P8_DP	Displayport SERDES analog supply low	–0.3	1.05	V
VDDA_0P8_DP_C	Displayport SERDES clock supply	–0.3	1.05	V
VDDA_0P8_DSITX	DSITX clock supply	–0.3	1.05	V
VDDA_0P8_DSITX_C	DSITX clock supply	–0.3	1.05	V
VDDA_0P8_CSIRX	CSIRX analog supply low	–0.3	1.05	V
VDDA_0P8_SERDES0_1	SERDES0-1 analog supply low	–0.3	1.05	V
VDDA_0P8_SERDES2_3	SERDES2-3 analog supply low	–0.3	1.05	V
VDDA_0P8_SERDES_C0_1	SERDES0-1 clock supply	–0.3	1.05	V
VDDA_0P8_SERDES_C2_3	SERDES2-3 clock supply	–0.3	1.05	V
VDDA_0P8_USB	USB0-1 0.8 V analog supply	–0.3	1.05	V
VDDA_0P8_UFS	UFS analog supply low	–0.3	1.05	V
VDDA_0P8_PLL_MLB	MLB PLL analog supply	–0.3	1.05	V
VDDA_0P8_PLL_DDR	DDR PLL analog supply	–0.3	1.05	V
VDDA_1P8_USB	USB0-1 1.8 V analog supply	–0.3	2.2	V
VDDA_1P8_UFS	UFS analog supply high	–0.3	2.2	V
VDDA_1P8_DP	Displayport SERDES analog supply high	–0.3	2.2	V
VDDA_1P8_DSITX	DSITX analog supply high	–0.3	2.2	V
VDDA_1P8_CSIRX	CSIRX analog supply high	–0.3	2.2	V
VDDA_1P8_SERDES0_1	SERDES0-1 analog supply high	–0.3	2.2	V
VDDA_1P8_SERDES2_3	SERDES2-3 analog supply high	–0.3	2.2	V
VDDA_3P3_USB	USB0-1 3.3 V analog supply	–0.3	3.8	V
VDDA_MCU_PLLGRP0	Analog supply for MCU PLL Group 0	–0.3	2.2	V
VDDA_PLLGRP0	Analog supply for Main PLL Group 0	–0.3	2.2	V
VDDA_PLLGRP1	Analog supply for Main PLL Group 1	–0.3	2.2	V
VDDA_PLLGRP2	Analog supply for Main PLL Group 2	–0.3	2.2	V
VDDA_PLLGRP3	Analog supply for Main PLL Group 3	–0.3	2.2	V
VDDA_PLLGRP4	Analog supply for Main PLL Group 4	–0.3	2.2	V
VDDA_PLLGRP5	Analog supply for MAIN PLL Group 5 (DDR)	–0.3	2.2	V
VDDA_PLLGRP6	Analog supply for MAIN PLL Group 6	–0.3	2.2	V
VDDA_WKUP	Oscillator supply for WKUP domain	–0.3	2.2	V
VDDA_ADC0	ADC analog supply	–0.3	2.2	V
VDDA_ADC1	ADC analog supply	–0.3	2.2	V
VDDA_MCU_TEMP	Analog supply for temperature sensor 0 in MCU domain	–0.3	2.2	V
VDDA_POR_WKUP	WKUP domain analog supply	–0.3	2.2	V

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6.1 Absolute Maximum Ratings (続き)

over operating free-air temperature range (unless otherwise noted)[(1) (2)]

PARAMETER		MIN	MAX	UNIT
VDDA_1P8_MLB	MLB IO supply (6-pin interface)	–0.3	2.2	V
VDDA_TEMP_0_1	Analog supply for temperature sensor 0	–0.3	2.2	V
VDDA_TEMP_2_3	Analog supply for temperature sensor 2	–0.3	2.2	V
VDDS_DDR	DDR inteface power supply	–0.3	1.2	V
VDDS_DDR_BIAS	Bias supply for LPDDR4	–0.3	1.2	V

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6.1 Absolute Maximum Ratings (続き)

over operating free-air temperature range (unless otherwise noted)[1] [2]

PARAMETER			MIN	MAX	UNIT
VDDS_DDR_C	IO power for DDR Memory Clock Bit (MCB) macro		–0.3	1.2	V
VDDS_MMC0	MMC0 IO supply		–0.3	2.2	V
VDDS_OSC1	HFOSC1 supply		–0.3	2.2	V
VDDSHV0_MCU	IO supply MCUSS general IO group, and MCU and MAIN domain warm reset pins	1.8 V	–0.3	2.2	V
		3.3 V	–0.3	3.8	
VDDSHV0	IO supply for MAIN domain general	1.8 V	–0.3	2.2	V
		3.3 V	–0.3	3.8	
VDDSHV1_MCU	IO supply for MCUSS IO group 1	1.8 V	–0.3	2.2	V
		3.3 V	–0.3	3.8	
VDDSHV1	IO supply for MAIN domain IO group 1	1.8 V	–0.3	2.2	V
		3.3 V	–0.3	3.8	
VDDSHV2_MCU	IO supply for MCUSS IO group 2	1.8 V	–0.3	2.2	V
		3.3 V	–0.3	3.8	
VDDSHV2	IO supply for MAIN domain IO group 2	1.8 V	–0.3	2.2	V
		3.3 V	–0.3	3.8	
VDDSHV3	IO supply for MAIN domain IO group 3	1.8 V	–0.3	2.2	V
		3.3 V	–0.3	3.8	
VDDSHV4	IO supply for MAIN domain IO group 4	1.8 V	–0.3	2.2	V
		3.3 V	–0.3	3.8	
VDDSHV5	IO supply for MAIN domain IO group 5	1.8 V	–0.3	2.2	V
		3.3 V	–0.3	3.8	
VDDSHV6	IO supply for MAIN domain IO group 6	1.8 V	-0.3	2.2	V
		3.3 V	–0.3	3.8	
VPP_CORE	Supply voltage range for CORE EFUSE domain		–0.3	1.89	V
VPP_MCU	Supply voltage range for MCU EFUSE domain		–0.3	1.89	V
USB0_VBUS[9]	Voltage range for USB VBUS comparator input		–0.3	3.6	V
USB1_VBUS[9]	Voltage range for USB VBUS comparator input		–0.3	3.6	V
Steady State Max. Voltage at all fail-safe IO pins		I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, WKUP_I2C0_SCL, WKUP_I2C0_SDA, MCU_I2C0_SCL, MCU_I2C0_SDA, EXTINTn	–0.3	3.8	V
		MCU_PORz, PORz	–0.3	3.8	V
		VMON_IR_VEXT	–0.3	2.2	V
		VMON_ER_VSYS[7] [8]	–0.3	1.05	V
Steady State Max. Voltage at all other IO pins[3]		All other IO pins	–0.3	IO supply voltage + 0.3	V

6.1 Absolute Maximum Ratings (続き)

over operating free-air temperature range (unless otherwise noted)[(1) (2)]

PARAMETER		MIN	MAX	UNIT
Transient Overshoot and Undershoot specification at IO pin	20% of IO supply voltage for up to 20% of signal period 図 6-1(see *IO Transient Voltage Ranges*)		0.2 × VDD[(6)]	V
Latch-up Performance, Class II (125°C)[(4)]	I-Test	–100	100	mA
	Over-Voltage (OV) Test	NA	1.5 × VDD[(6)]	V
T_{STG} [(5)]	Storage temperature	–55	+150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under セクション 6.4, *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to their associated VSS or VSSA_x, unless otherwise noted.
(3) This parameter applies to all IO pins which are not fail-safe and the requirement applies to all values of IO supply voltage. For example, if the voltage applied to a specific IO supply is 0 volts the valid input voltage range for any IO powered by that supply will be –0.3 to +0.3 volts. Special attention should be applied anytime peripheral devices are not powered from the same power sources used to power the respective IO supply. It is important the attached peripheral never sources a voltage outside the valid input voltage range, including power supply ramp-up and ramp-down sequences.
(4) For current pulse injection:
Pins stressed per JEDEC JESD78E (Class II) and passed with specified I/O pin injection current and clamp voltage of 1.5 times maximum recommended I/O voltage and negative 0.5 times maximum recommended I/O voltage.
For overvoltage performance:
Supplies stressed per JEDEC JESD78E (Class II) and passed specified voltage injection.
(5) For tape and reel the storage temperature range is [–10°C; +50°C] with a maximum relative humidity of 70%. TI recommends returning to ambient room temperature before usage.
(6) VDD is the voltage on the corresponding power-supply pin(s) for the IO.
(7) An external resistor divider is required to create the VMON input value that triggers with V_{TH} = 0.45 when the V_{SYS} level reaches the minimum allowed threshold. A series resistor R2 (VMON_ER_VSYS = V_{SYS} × R1 / (R1 + R2)) of at least 10kΩ is recommended to limit current.
(8) The VMON_ER_VSYS pin provides a way to monitor the system power supply. For more information, see セクション 8.3.5 *System Power Supply Monitor Design Guidelines*.
(9) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see セクション 8.3.4, *USB VBUS Design Guidelines*.

Fail-safe IO terminals are designed such they do not have dependencies on the respective IO power supply voltage. This allows external voltage sources to be connected to these IO terminals when the respective IO power supplies are turned off. The I2C0_SCL, I2C0_SDA, I2C1_SCL, I2C1_SDA, DDR_FS_RESETn, NMIn, VMON_ER_VSYS, and VMON_IR_VEXT are the only fail-safe IO terminals. All other IO terminals are not fail-safe and the voltage applied to them should be limited to the value defined by the Steady State Max. Voltage at all IO pins parameter in セクション 6.1.

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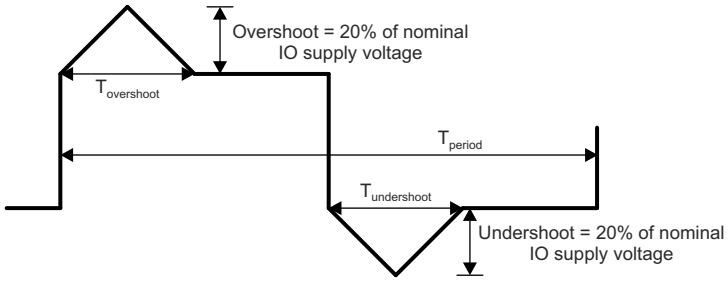

A. $T_{overshoot} + T_{undershoot} < 20\%$ of T_{period}

図 6-1. IO Transient Voltage Ranges

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002, Revision J[1]		±1000	V
		Charged-device model (CDM), per AEC Q100-011, Revision J	All pins	±250	
			Corner pins (A1, AJ29)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Power-On-Hour (POH) Limits

IP[1] [2] [3]	VOLTAGE DOMAIN	VOLTAGE (V) (MAX)	FREQUENCY (MHz) (MAX)	Tj(°C)	POH
All	100%	All	All Supported OPPs	Automotive -40°C to 125°C[4]	20000
All	100%	All	All Supported OPPs	Extended -40°C to 105°C	100000
All	100%	All	All Supported OPPs	Commercial 0°C to 90°C	100000

(1) This information is provided solely for your convenience and does not extend or modify the warranty provided under TI's standard terms and conditions for TI semiconductor products.
(2) Unless specified in the table above, all voltage domains and operating conditions are supported in the device at the noted temperatures
(3) POH is a function of voltage, temperature and time. Usage at higher voltages and temperatures will result in a reduction in POH.
(4) Automotive profile is defined as 20000 power on hours with junction temperature as follows: 5%@-40°C, 65%@70°C, 20%@110°C, and 10%@125°C.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION	MIN[1]	NOM	MAX[1]	UNIT
VDD_CORE	Boot/Active voltage for MAIN domain core supply	0.76	0.8	0.84	V
VDD_MCU	Boot/Active voltage for MCUSS core supply	0.76	0.8	0.89	V
VDD_CPU	Boot voltage for CPU core supply, applied at cold power up event	0.76	0.8	0.84	V
	Active voltage for CPU core supply, after AVS mode enabled in software	AVS[4]-5%	AVS[4]	AVS[4]+5%	V
VDD_CPU AVS Range	AVS valid voltage range for VDD_CPU	0.6		0.9	V
VDDA_0P8_DLL_MMC0	MMC PLL analog supply	0.76	0.8	0.84	V
VDDAR_CORE	Main domain RAM supply	0.81	0.85	0.89	V
VDDAR_MCU	MCUSS RAM supply	0.81	0.85	0.89	V
VDDAR_CPU	CPU RAM supply	0.81	0.85	0.89	V
VDDA_0P8_DP	Displayport SERDES clock supply	0.76	0.8	0.84	V
VDDA_0P8_DP_C	Displayport SERDES clock supply	0.76	0.8	0.84	V

6.4 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN[1]	NOM	MAX[1]	UNIT
VDDA_0P8_DSITX	DSITX clock supply		0.76	0.8	0.84	V
VDDA_0P8_DSITX_C	DSITX clock supply		0.76	0.8	0.84	V
VDDA_0P8_CSIRX	CSIRX analog supply low		0.76	0.8	0.84	V
VDDA_0P8_SERDES0_1	SERDES0-1 analog supply low		0.76	0.8	0.84	V
VDDA_0P8_SERDES2_3	SERDES2-3 analog supply low		0.76	0.8	0.84	V
VDDA_0P8_SERDES_C0_1	SERDES0-1 clock supply		0.76	0.8	0.84	V
VDDA_0P8_SERDES_C2_3	SERDES2-3 clock supply		0.76	0.8	0.84	V
VDDA_0P8_USB	USB0-1 0.8v analog supply		0.76	0.8	0.84	V
VDDA_0P8_UFS	UFS analog supply low		0.76	0.8	0.84	V
VDDA_1P8_USB	USB0-1 1.8v analog supply		1.71	1.8	1.89	V
VDDA_1P8_UFS	UFS analog supply high		1.71	1.8	1.89	V
VDDA_1P8_DP	Displayport SERDES analog supply high		1.71	1.8	1.89	V
VDDA_1P8_DSITX	DSITX analog supply high		1.71	1.8	1.89	V
VDDA_1P8_CSIRX	CSIRX analog supply high		1.71	1.8	1.89	V
VDDA_1P8_SERDES0_1	SERDES0-1 analog supply high		1.71	1.8	1.89	V
VDDA_1P8_SERDES2_3	SERDES2-3 analog supply high		1.71	1.8	1.89	V
VDDA_3P3_USB	USB0-1 3.3v analog supply		3.14	3.3	3.46	V
VDDA_MCU_PLLGRP0	Analog supply for MCU PLL Group 0		1.71	1.8	1.89	V
VDDA_PLLGRP0	Analog supply for Main PLL Group 0		1.71	1.8	1.89	V
VDDA_PLLGRP1	Analog supply for MAIN PLL Group 1		1.71	1.8	1.89	V
VDDA_PLLGRP2	Analog supply for MAIN PLL Group 2		1.71	1.8	1.89	V
VDDA_PLLGRP3	Analog supply for MAIN PLL Group 3		1.71	1.8	1.89	V
VDDA_PLLGRP4	Analog supply for MAIN PLL Group 4		1.71	1.8	1.89	V
VDDA_PLLGRP5	Analog supply for MAIN PLL Group 5 (DDR)		1.71	1.8	1.89	V
VDDA_PLLGRP6	Analog supply for MAIN PLL Group 6		1.71	1.8	1.89	V
VDDA_0P8_PLL_MLB	MLB PLL analog supply		0.76	0.8	0.84	V
VDDA_WKUP	Oscillator supply for wkup domain		1.71	1.8	1.89	V
VDDA_ADC0	ADC analog supply		1.71	1.8	1.89	V
VDDA_ADC1	ADC analog supply		1.71	1.8	1.89	V
VDDA_0P8_PLL_DDR	DDR PLL analog supply		0.76	0.8	0.84	V
VDDA_MCU_TEMP	Analog supply for temperature sensor 0 in MCU domain		1.71	1.8	1.89	V
VDDA_POR_WKUP	WKUP domain analog supply		1.71	1.8	1.89	V
VDDA_1P8_MLB	MLB IO supply (6-pin interface)		1.71	1.8	1.89	V
VDDA_TEMP0_1	Analog supply for temperature sensor 0 and 1		1.71	1.8	1.89	V
VDDA_TEMP2_3	Analog supply for temperature sensor 2 and 3		1.71	1.8	1.89	V
VDDS_DDR[2]	DDR inteface power supply		1.06	1.1	1.15	V
VDDS_DDR_BIAS	Bias supply for LPDDR4x		1.06	1.1	1.15	V
VDDS_DDR_C	IO power for DDR Memory Clock Bit (MCB) macro		1.06	1.1	1.15	V
VDDS_MMC0	MMC0 IO supply		1.71	1.8	1.89	V
VDDS_OSC1	HFOSC1 supply		1.71	1.8	1.89	V
VDDSHV0	IO supply for main domain general	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V

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6.4 Recommended Operating Conditions (続き)

over operating free-air temperature range (unless otherwise noted)

SUPPLY NAME	DESCRIPTION		MIN[1]	NOM	MAX[1]	UNIT
VDDSHV0_MCU	IO supply MCUSS general IO group, and MCU and Main domain warm reset pins	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV1	IO supply for main domain IO group 1	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV1_MCU	IO supply for MCUSS IO group 1	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV2	IO supply for main domain IO group 2	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV2_MCU	IO supply for MCUSS IO group 2	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV3	IO supply for main domain IO group 3	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV4	IO supply for main domain IO group 4	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV5	IO supply for main domain IO group 5	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
VDDSHV6	IO supply for main domain IO group 6	1.8-V operation	1.71	1.8	1.89	V
		3.3-V operation	3.14	3.3	3.46	V
USB0_VBUS	Voltage range for USB VBUS comparator input		0	See [5]	3.46	V
USB1_VBUS	Voltage range for USB VBUS comparator input			See [5]		V
USB0_ID	Voltage range for the USB ID input			See [3]		V
USB1_ID	Voltage range for the USB ID input			See [3]		V
VSS	Ground			0		V
T_J	Operating junction temperature range	Automotive	-40		125	°C
		Extended	-40		105	°C
		Commercial	0		90	°C

(1) The voltage at the device ball must never be below the MIN voltage or above the MAX voltage for any amount of time. This requirement includes dynamic voltage events such as AC ripple, voltage transients, voltage dips, and so forth.
(2) VDDS_DDR is required to still be powered with LPDDR4 voltage ranges, even If DDR interface is unused.
(3) This terminal is connected to analog circuits in the respective USB PHY. The circuit sources a known current while measuring the voltage to determine if the terminal is connected to VSS with a resistance less than 10 Ω or greater than 100 kΩ. The terminal should be connected to ground for USB host operation or open-circuit for USB peripheral operation, and should never be connected to any external voltage source.
(4) The AVS Voltages are device-dependent, voltage domain-dependent, and OPP-dependent. They must be read from the VTM_DEVINFO_VDn. For information about VTM_DEVINFO_VDn Registers address, please refer to Voltage and Thermal Manager section in the device TRM. The power supply should be adjustable over the ranges shown in the VDD_CPU AVS Range entry.
(5) An external resistor divider is required to limit the voltage applied to this device pin. For more information, see セクション 8.3.4, *USB VBUS Design Guidelines.*.

6.5 Operating Performance Points

This section describes the operating conditions of the device. This section also contains the description of each Operating Performance Point (OPP) for processor clocks and device core clocks.

表 6-1 describes the maximum supported frequency per speed grade for the device.

表 6-1. Speed Grade Maximum Frequency

DEVICE	MAXIMUM FREQUENCY (MHz)										
	A72SS0	C66SS0	C71SS0	R5FSS0/1	MCU_ R5SS0	GPU	CBASS0	VPAC	DMPAC	DMSC	LPDDR4
TDA4VMxT	2000	1350	1000	1000	1000	750	500	720(1)	520(1)	333	4266 MT/s(2)
TDA4VMxL	1500	1000	750	1000	1000	600	500	600(1)	433(1)	333	3733 MT/s(2)
TDA4VMxE	1000	1000	750	1000	1000	400	500	600(1)	N/A	333	3200 MT/s(2)

(1) Max VPAC and DMPAC speeds not available concurrently due to PLL sharing (max combinations are 720/480 and 650/520 for VPAC/DMPAC, respectively.

(2) Maximum DDR Frequency is limited based on the specific memory type (vendor) used in a system and by PCB implementation. TI strongly recommends that all designs follow the TI LPDDR4 EVM PCB layout exactly in every detail (*routing, spacing, vias/backdrill, PCB material, and so forth*) in order to achieve the full specified clock frequency. For details, see the Jacinto 7 LPDDR4 Board Design and Layout Guidelines.

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6.6 Electrical Characteristics

注

The interfaces or signals described in 表 6-2through 表 6-9 correspond to the interfaces or signals available in multiplexing mode 0 (Primary Function).

All interfaces or signals multiplexed on the balls described in these tables have the same DC electrical characteristics, unless multiplexing involves a PHY and GPIO combination, in which case different DC electrical characteristics are specified for the different multiplexing modes (Functions).

表 6-2. I2C, Open-Drain, Fail-Safe (I2C OD FS) Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BALL NAMES in Mode 0: WKUP_I2C0_SDA, WKUP_I2C0_SCL, MCU_I2C0_SDA, MCU_I2C0_SCL, I2C0_SDA, I2C0_SCL, I2C1_SDA, I2C1_SCL, EXTINTN						
BALL NUMBERS:H24 / J25 / H25 / J26 / AA5 / AC5 / AA6 / Y6 / AC18 H24/ J25 / H25 / J26 / AA5 / AC5 / AA6 / Y6 / AC18						
1.8-V MODE						
V_{IL}	Input low-level threshold				0.3 × VDDSHV[(1)]	V
V_{ILSS}	Input low-level threshold steady state				0.3 × VDDSHV[(1)]	V
V_{IH}	Input high-level threshold		0.7 × VDDSHV[(1)]			V
V_{IHSS}	Input high-level threshold steady state		0.7 × VDDSHV[(1)]			V
V_{HYS}	Input Hysteresis Voltage		0.1 × VDDSHV[(1)]			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			±10	µA
V_{OL}	Output low-level voltage				0.2 × VDDSHV[(1)]	V
I_{OL} [(2)]	Low Level Output Current	$V_{OL(MAX)}$	6			mA
SR_I [(4)]	Input Slew Rate		18f[(3)] or 1.8E+6			V/s
3.3-V MODE [(5)]						
V_{IL}	Input low-level threshold				0.3 × VDDSHV[(1)]	V
V_{ILSS}	Input low-level threshold steady state				0.25 × VDDSHV[(1)]	V
V_{IH}	Input high-level threshold		0.7 × VDDSHV[(1)]			V
V_{IHSS}	Input high-level threshold steady state		0.7 × VDDSHV[(1)]			V
V_{HYS}	Input Hysteresis Voltage		0.05 × VDDSHV[(1)]			mV
I_{IN}	Input Leakage Current	V_I = 3.3 V or 0 V			±10	µA
V_{OL}	Output low-level voltage				0.4[(1)]	V
I_{OL} [(2)]	Low Level Output Current	$V_{OL(MAX)}$	6			mA
SR_I [(4)]	Input Slew Rate		33f[(3)] or 3.3E+6		8E + 7	V/s

(1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see セクション 5.2, *Pin Attributes*, POWER column.

(2) The I_{OL} parameter defines the minimum Low Level Output Current for which the device is able to maintain the specified V_{OL} value. The value defined by this parameter should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} value for attached components.
(3) f = toggle frequency of the input signal in Hz.
(4) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.
(5) I2C Hs-mode is not supported, when operating the IO in 3.3-V mode.

表 6-3. Fail-Safe Reset (FS Reset) Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BALL NAMES in Mode 0: MCU_PORz, PORz						
BALL NUMBERS:H23 / J24						
V_{IL}	Input low-level threshold				0.3 × VDDSHV(1)	V
V_{ILSS}	Input low-level threshold steady state				0.3 × VDDSHV(1)	V
V_{IH}	Input high-level threshold		0.7 × VDDSHV(1)			V
V_{IHSS}	Input high-level threshold steady state		0.7 × VDDSHV(1)			V
V_{HYS}	Input Hysteresis Voltage		200			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			±10	µA

(1) VDDSHV stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see セクション 5.2, *Pin Attributes*, POWER column.

表 6-4. HFOSC/LFOSC Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
HIGH FREQUENCY OSCILLATOR						
BALL NAMES: WKUP_OSC0_XO, WKUP_OSC0_XI, OSC1_XO, OSC1_XI						
BALL NUMBERS:M27 / M29 / P27 / P29						
V_{IH}	Input high-level threshold		0.65 × VDDSHV(1)			V
V_{IL}	Input low-level threshold				0.35 × VDDSHV(1)	V
V_{HYS}	Input Hysteresis Voltage			49		mV
LOW FREQUENCY OSCILLATOR						
BALL NAMES: WKUP_LFOSC0_XO, WKUP_LFOSC0_XI						
BALL NUMBERS:N26 / N28						
V_{IH}	Input high-level threshold		0.65 × VDDA_WKUP (1)			V
V_{IL}	Input low-level threshold				0.35 × VDDA_WKUP (1)	V
V_{HYS}	Input Hysteresis Voltage	Active Mode		85		mV
		Bypass Mode		324		mV

(1) VDDSHV stands for corresponding power supply. For WKUP_OSC0, the corresponding power supply is VDDA_WKUP. For OSC1_XI, the corresponding power supply is VDDS_OSC1.

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表 6-5. eMMCPHY Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
BALL NAMES in Mode 0: MMC0_DAT[7:0], MMC0_CALPAD, MMC0_CMD, MMC0_DS, MMC0_CLK						
BALL NUMBERS:AG2 / AH1 / AG3 / AF4 / AE5 / AF3 / AG1 / AF2 / AE1 / AE3 / AE4 / AF1						
V_{IL}	Input low-level threshold				0.35 × VDDSHV(1)	V
V_{ILSS}	Input low-level threshold steady state				0.20	V
V_{IH}	Input high-level threshold		0.65 × VDDSHV(1)			V
V_{IHSS}	Input high-level threshold steady state		1.4			V
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			±10	µA
I_{OZ}	Tri-state Output Leakage Current	V_O = 1.8 V or 0 V			±10	µA
R_{PU}	Pull-up Resistor		15	20	25	kΩ
R_{PD}	Pull-down Resistor		15	20	25	kΩ
V_{OL}	Output low-level voltage				0.30	V
V_{OH}	Output high-level voltage		VDDSHV - 0.30(1)			V
I_{OL}	Low Level Output Current	$V_{OL(MAX)}$	2			mA
I_{OH}	High Level Output Current	$V_{OH(MAX)}$	2			mA
SR_I	Input Slew Rate		5E + 8			V/s

(1) VDDSHV stands for corresponding power supply (vddshv8). For more information on the power supply name and the corresponding ball, see セクション 5.2, *Pin Attributes*, POWER column.

表 6-6. SDIO Electrical Characteristics

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
BALL NAMES in Mode 0: MMC1_CLK, MMC1_CMD, MMC1_DAT[3:0], MMC2_CLK, MMC2_CMD, MMC2_DAT[3:0]						
BALL NUMBERS:P25 / R29 / R24 / P24 / R25 / R26 / T26 / T25 / T24 / T27 / T29 / T28						
1.8-V MODE						
V_{IL}	Input low-level threshold				0.58	V
V_{ILSS}	Input low-level threshold steady state				0.58	V
V_{IH}	Input high-level threshold		1.27			V
V_{IHSS}	Input high-level threshold steady state		1.7			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			±10	µA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output low-level voltage				0.45	V
V_{OH}	Output high-level voltage		VDDSHV-0.45(1)			V
I_{OL}	Low Level Output Current	$V_{OL(MAX)}$	4			mA
I_{OH}	High Level Output Current	$V_{OH(MAX)}$	4			mA
SR_I (3)	Input Slew Rate		18f(2) or 1.8E+6			V/s
3.3-V Mode						
V_{IL}	Input low-level threshold				0.25 × VDDSHV(1)	V

表 6-6. SDIO Electrical Characteristics (続き)

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
V_{ILSS}	Input low-level threshold steady state				0.15 × VDDSHV(1)	V
V_{IH}	Input high-level threshold		0.625 × VDDSHV(1)			V
V_{IHSS}	Input high-level threshold steady state		0.625 × VDDSHV(1)			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			±10	µA
R_{PU}	Pull-up Resistor		40	50	60	kΩ
R_{PD}	Pull-down Resistor		40	50	60	kΩ
V_{OL}	Output low-level voltage				0.125 × VDDSHV(1)	V
V_{OH}	Output high-level voltage		0.75 × VDDSHV(1)			V
I_{OL}	Low Level Output Current	$V_{OL(MAX)}$	6			mA
I_{OH}	High Level Output Current	$V_{OH(MAX)}$	10			mA
SR_I (3)	Input Slew Rate		33f(2) or 3.3E+6			V/s

(1) VDDSHV stands for corresponding power supply (vddshv8). For more information on the power supply name and the corresponding ball, see セクション 5.2, *Pin Attributes*, POWER column.
(2) f = toggle frequency of the input signal in Hz.
(3) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

CSI-2/DSI D-PHY Electrical Characteristics

注

CSI-2/DSI (D-PHY) interfaces are compliant with MIPI D-PHY specifications v1.2 dated August 1, 2014, including ECNs and Errata as applicable.

表 6-7. ADC12B Electrical Characteristics

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BALL NAMES in Mode 0: MCU_ADC0_AIN[7:0], MCU_ADC1_AIN[7:0]						
BALL NUMBERS:K24 / K25 / K26 / K27 / K28 / K29 / L24 / L25 / L26 / L27 / L28 / L29 / M24 / M25 / N23 / N24						
Analog Input						
$V_{MCU_ADC0/1_AIN[7:0]}$	Full-scale Input Range		VSS		VDDA_ADC0/1	V
DNL	Differential Non-Linearity		-1	0.5	4	LSB
INL	Integral Non-Linearity			±1	±4	LSB
$LSB_{GAIN-ERROR}$	Gain Error			±2		LSB
$LSB_{OFFSET-ERROR}$	Offset Error			±2		LSB
C_{IN}	Input Sampling Capacitance			5.5		pF
SNR	Signal-to-Noise Ratio	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		70		dB

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表 6-7. ADC12B Electrical Characteristics (続き)

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD	Total Harmonic Distortion	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		73		dB
SFDR	Spurious Free Dynamic Range	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		76		dB
$SNR_{(PLUS)}$	Signal-to-Noise Plus Distortion	Input Signal: 200 kHz sine wave at -0.5 dB Full Scale		69		dB
$R_{MCU_ADC0/1_AIN[0:7]}$	Input Impedance of MCU_ADC0/1_AIN[7:0]	f = input frequency		$[1/((65.97 \times 10^{-12}) \times f_{SMPL_CLK})]$		Ω
I_{IN}	Input Leakage	MCU_ADC0/1_AIN[7:0] = VSS			-10	µA
		MCU_ADC0/1_AIN[7:0] = VDDA_ADC0/1			24	µA
Sampling Dynamics						
F_{SMPL_CLK}	SMPL_CLK Frequency			60		MHz
t_C	Conversion Time			13		ADC0/1 SMPL_CLK Cycles
t_{ACQ}	Acquisition time		2		257	ADC0/1 SMPL_CLK Cycles
T_R	Sampling Rate	ADC0/1 SMPL_CLK = 60 MHz		4		MSPS
CCISO	Channel to Channel Isolation			100		dB
General Purpose Input Mode(1)						
V_{IL}	Input low-level threshold				0.35 × VDDA_ADC0/1	V
V_{ILSS}	Input high-level threshold steady state				0.35 × VDDA_ADC0/1	V
V_{IH}	Input high-level threshold		0.65 × VDDA_ADC0/1			V
V_{IHSS}	Input high-level threshold steady state		0.65 × VDDA_ADC0/1			V
V_{HYS}	Input Hysteresis Voltage		200			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			6	µA

(1) MCU_ADC0/1 can be configured to operate in General Purpose Input mode, where all MCU_ADC0/1_AIN[7:0] inputs are globally enabled to operate as digital inputs via the ADC0/1_CTRL register (gpi_mode_en = 1).

表 6-8. MLB LVCMOS Electrical Characteristics

Only GPIO mode supported. Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BALL NAMES in Mode 0: MLB0_MLBSN, MLB0_MLBDP, MLB0_MLBSP, MLB0_MLBCP, MLB0_MLBDN, MLB0_MLBCN						
BALL NUMBERS:AC1 / AC3 / AD1 / AD2 / AD3 / AE2						
V_{IL}	Input Low Voltage				0.3 × VDD(1)	V

表 6-8. MLB LVCMOS Electrical Characteristics (続き)

Only GPIO mode supported. Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD[(1)]	V
V_{IH}	Input High Voltage		0.7 × VDD[(1)]			V
V_{IHSS}	Input High Voltage Steady State		0.75 × VDD[(1)]			V
V_{HYS}	Input Hysteresis Voltage		80			mV
I_{IN}	Input Leakage Current	V_I = 1.8 V or 0 V			±10	µA
R_{PD}	Pull-down Resistor		20	53	130	kΩ
V_{OL}	Output Low Voltage				0.2	V
V_{OH}	Output High Voltage		VDD[(1)] - 0.2			V
I_{OL}	Low Level Output Current	$V_{OL(MAX)}$	6			mA
I_{OH}	High Level Output Current	$V_{OH(MIN)}$	6			mA
SR_I	Input Slew Rate[(2)]	f_{op} > 100 MHz	1			V/ns
		f_{op} < 1 MHz	10			V/ns

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see セクション 5.2, *Pin Attributes*, POWER column.
(2) Slew rate may be further limited, reference セクション 6.9 for actual slew rate during operation.

表 6-9. LVCMOS Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER[(1)]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BALL NAMES: ALL other IOs						
BALL NUMBERS: ALL other IOs						
1.8-V MODE						
V_{IL}	Input Low Voltage				0.35 × VDD[(1)]	V
V_{ILSS}	Input Low Voltage Steady State				0.3 × VDD[(1)]	V
V_{IH}	Input High Voltage		0.65 × VDD[(1)]			V
V_{IHSS}	Input High Voltage Steady State		0.85 × VDD[(1)]			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 1.8 V or 0 V			±10	µA
R_{PU}	Pull-up Resistor		15	22	30	kΩ
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.45	V
V_{OH}	Output High Voltage		VDD[(1)] - 0.45			V
I_{OL} [(2)]	Low Level Output Current	$V_{OL(MAX)}$	3			mA
I_{OH} [(2)]	High Level Output Current	$V_{OH(MIN)}$	3			mA
SR_I [(4)]	Input Slew Rate		18f[(3)] or 1.8E+6			V/s
3.3-V MODE						
V_{IL}	Input Low Voltage				0.8	V
V_{ILSS}	Input Low Voltage Steady State				0.6	V
V_{IH}	Input High Voltage		2.0			V
V_{IHSS}	Input High Voltage Steady State		2.0			V
V_{HYS}	Input Hysteresis Voltage		150			mV
I_{IN}	Input Leakage Current.	V_I = 3.3 V or 0 V			±10	µA

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表 6-9. LVCMOS Electrical Characteristics (続き)

over recommended operating conditions (unless otherwise noted)

PARAMETER[(1)]		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PD}	Pull-down Resistor		15	22	30	kΩ
V_{OL}	Output Low Voltage				0.4	V
V_{OH}	Output High Voltage		2.4			V
I_{OL} [(2)]	Low Level Output Current	$V_{OL(MAX)}$	5			mA
I_{OH} [(2)]	High Level Output Current	$V_{OH(MIN)}$	6			mA
SR_I [(4)]	Input Slew Rate		33f[(3)] or 3.3E+6			V/s

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball, see セクション 5.2, *Pin Attributes*, POWER column.
(2) The I_{OL} and I_{OH} parameters define the minimum Low Level Output Current and High Level Output Current for which the device is able to maintain the specified V_{OL} and V_{OH} values. Values defined by these parameters should be considered the maximum current available to a system implementation which needs to maintain the specified V_{OL} and V_{OH} values for attached components.
(3) f = toggle frequency of the input signal in Hz.
(4) This MIN parameter only applies to input signal functions which are not defined in their respective *Timing and Switching Characteristics* sections. Select the MIN parameter which results in the largest value.

USB2PHY Electrical Characteristics

注

USB0 and USB1 Electrical Characteristics are compliant with Universal Serial Bus Revision 2.0 Specification dated April 27, 2000 including ECNs and Errata as applicable.

SerDes 4-L-PHY/2-L-PHY Electrical Characteristics

注

The PCIe interfaces are compliant with the electrical parameters specified in PCI Express® Base Specification Revision 4.0, September 27, 2017.

This Device imposes an additional limit on SERDES REFCLK when used in Input mode with internal termination enabled, as described by parameter V_{REFCLK_TERM} in 表 6-10, *4-L-PHY SERDES REFCLK Electrical Characteristics*. Internal termination is enabled by default and must be disabled before applying a reference clock signal that exceeds the limits defined by V_{REFCLK_TERM}. External termination should always be enabled on the source side.

表 6-10. 4-L-PHY SERDES REFCLK Electrical Characteristics

Only applies when internal termination is enabled. Over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
BALL NAMES in Mode 0: SERDES4_REFCLK_P, SERDES4_REFCLK_N					
BALL NUMBERS:E8 / E7					
V_{REFCLK_TERM}	Single ended voltage threshold at the reference clock pin when internal termination is enabled			400	mV
R_{TERM}	Internal termination	40	50	62.5	Ω

注

The SerDes USB interfaces are compliant with the USB3.1 SuperSpeed Transmitter and Receiver Normative Electrical Parameters as defined in the Universal Serial Bus 3.1 Specification, Revision 1.0 , July 26, 2013.

注

The SGMII interfaces electrical characteristics are compliant with 1000BASE-KX per IEEE802.3 Clause 70.

注

The SGMII 2.5G / XAUI interfaces electrical characteristics are compliant with IEEE802.3 Clause 47.

注

The QSGMII interface electrical characteristics are compliant with QSGMII Specification revision 1.2.

This Device imposes an additional limit on the 2-L-PHY SERDES REFCLK, as described by parameters V_{IDTH} and V_{IDTL} in 表 6-11, *2-L-PHY SERDES REFCLK Electrical Characteristics*.

表 6-11. 2-L-PHY SERDES REFCLK Electrical Characteristics

Only applies when internal termination is enabled. Over recommended operating conditions (unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT
BALL NAMES in Mode 0: PCIE_REFCLK[3:0]P, PCIE_REFCLK[3:0]N					
BALL NUMBERS:AE9 / AD10 / AE11 / AD12 / AE14 / AD15 / AE17 / AD16					
V_{IDTH}	Input Differential high-level threshold			200	mV
V_{IDTL}	Input Differential low-level threshold	–200			mV

UFS M-PHY Electrical Characteristics

注

The UFS interface electrical characteristics are compliant with MIPI M-PHY Specification v3.1, February 17, 2014.

eDP/DP AUX-PHY Electrical Characteristics

注

The DP interface electrical characteristics are compliant with the VESA DisplayPort (DP) Standard v 1.4 February 23, 2016.

注

The eDP interface electrical characteristics are compliant with the VESA Embedded DisplayPort (eDP) Standard v1.4b October 23, 2015.

DDR0 Electrical Characteristics

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注

The DDR interface is compatible with JESD209-4B standard compliant LPDDR4 SDRAM devices.

6.7 VPP Specifications for One-Time Programmable (OTP) eFuses

This section specifies the operating conditions required for programming the OTP eFuses and is applicable only for High-Security Devices.

6.7.1 Recommended Operating Conditions for OTP eFuse Programming

over operating free-air temperature range (unless otherwise noted)

PARAMETER	DESCRIPTION	MIN	NOM	MAX	UNIT
VDD_CORE	Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)	See セクション 6.4			V
VDD_MCU	Supply voltage range for the core domain during OTP operation; OPP NOM (BOOT)	See セクション 6.4			V
VPP_CORE	Supply voltage range for the eFuse ROM domain during normal operation	N/A(2)			
	Supply voltage range for the eFuse ROM domain during OTP programming(1)	1.71	1.8	1.89	V
VPP_MCU	Supply voltage range for the eFuse ROM domain during normal operation	N/A(2)			
	Supply voltage range for the eFuse ROM domain during OTP programming(1)	1.71	1.8	1.89	V

(1) Supply voltage range includes DC errors and peak-to-peak noise. TI power management solutions TLV70718 from the TLV707x family meet the supply voltage range needed for VPP_CORE and VPP_MCU.
(2) N/A stands for Not Applicable.

6.7.2 Hardware Requirements

The following hardware requirements must be met when programming keys in the OTP eFuses:

- The VPP_CORE and VPP_MCU power supplies must be disabled when not programming OTP registers.
- The VPP_CORE and VPP_MCU power supplies must be ramped up after the proper device power-up sequence (for more details, see セクション 6.9.2).

6.7.3 Programming Sequence

Programming sequence for OTP eFuses:

- Power on the board per the power-up sequencing. No voltage should be applied on the VPP_CORE and VPP_MCU terminals during power up and normal operation.
- Load the OTP write software required to program the eFuse (contact your local TI representative for the OTP software package).
- Apply the voltage on the VPP_CORE and VPP_MCU terminals according to the specification in セクション 6.7.1.
- Run the software that programs the OTP registers.
- After validating the content of the OTP registers, remove the voltage from the VPP_CORE and VPP_MCU terminals.

6.7.4 Impact to Your Hardware Warranty

You recognize and accept at your own risk that your use of eFuse permanently alters the TI device. You acknowledge that eFuse can fail due to incorrect operating conditions or programming sequence. Such a failure may render the TI device inoperable and TI will be unable to confirm the TI device conformed to TI device specifications prior to the attempted eFuse. CONSEQUENTLY, TI WILL HAVE NO LIABILITY FOR ANY TI DEVICES THAT HAVE BEEN eFUSED.

6.8 Thermal Resistance Characteristics

This section provides the thermal resistance characteristics used on this device.

For reliability and operability concerns, the maximum junction temperature of the device has to be at or below the T_J value identified in セクション 6.4, *Recommended Operating Conditions*.

6.8.1 Thermal Resistance Characteristics for ALF Package

It is recommended to perform thermal simulations at the system level with the worst case device power consumption.

NO.	PARAMETER	DESCRIPTION	ALF PACKAGE	
			°C/W[(1)(3)]	AIR FLOW (m/s)[(2)]
T1	$R\Theta_{JC}$	Junction-to-case	0.25	N/A
T2	$R\Theta_{JB}$	Junction-to-board	2.1	N/A
T3	$R\Theta_{JA}$	Junction-to-free air	11.5	0
T4		Junction-to-moving air	7.4	1
T5			6.5	2
T6			6	3
T7	Ψ_{JT}	Junction-to-package top	0.1	0
T8			0.1	1
T9			0.1	2
T10			0.1	3
T11	Ψ_{JB}	Junction-to-board	1.6	0
T12			1.7	1
T13			1.6	2
T14			1.5	3

(1) These values are based on a JEDEC defined 2S2P system (with the exception of the Theta JC [RΘJC] value, which is based on a JEDEC defined 1S0P system) and will change based on environment as well as application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environment Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-6, *Integrated Circuit Thermal Test Method Environmental Conditions - Forced Convection (Moving Air)*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Packages*

(2) m/s = meters per second.
(3) °C/W = degrees Celsius per watt.

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6.9 Timing and Switching Characteristics

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The default SLEWRATE settings in each pad configuration register must be used to ensure timings, unless specific instructions are given otherwise.

6.9.1 Timing Parameters and Information

The timing parameter symbols used in セクション 6.9 are created in accordance with JEDEC Standard 100. To shorten the symbols, some pin names and other related terminologies have been abbreviated in 表 6-12:

表 6-12. Timing Parameters Subscripts

SYMBOL	PARAMETER
c	Cycle time (period)
d	Delay time
dis	Disable time
en	Enable time
h	Hold time
su	Setup time
START	Start bit
t	Transition time
v	Valid time
w	Pulse duration (width)
X	Unknown, changing, or don't care level
F	Fall time
H	High
L	Low
R	Rise time
V	Valid
IV	Invalid
AE	Active Edge
FE	First Edge
LE	Last Edge
Z	High impedance

6.9.2 Power Supply Sequencing

This section describes power supply sequencing required to ensure proper device operation. The device can be operated using either an isolated or combined MCU & Main power distribution network (PDN). Two different primary power sequences are recommended based upon isolated and combined MCU & Main PDNs. In addition, the device can be operated in either MCU Only or DDR Retention low power modes. Two different desired device power supply sequences for entry and exit of low power modes are shown.

The power supply names used in this section are specific to this device and align to names given in the Signal Descriptions section. Common power supply names may be used across different devices within the Jacinto 7™ processor family. These common supply names will have very similar if not identical functions across devices.

All power sequencing timing diagrams shown will use the following terminology:

- Primary = Essential power sequences of all voltage domains between off and full active states.
- $V_{OPR\ MIN}$ = Minimum operational voltage level that ensures functionality as specified in Recommended Operating Conditions
- Ramp-up = start of a voltage supply transition time from off condition to Vopr min.
- Ramp-down = start of a voltage supply transition time from Vopr to off condition
- Supply_“n” = multiple instances of similar power supplies (i.e. VDDSHVn = VDDSHV0, VDDSHV1, VDDSHV2 … VDDSHV6)
- Supply_“xxx” = multiple instances of similar power supplies used for different signal types (i.e. VDDA_1P8_xxx = VDDA_1P8_DSITX, VDDA_1P8_USB, VDDA_0P8_DSITX, VDDA_0P8_USB, etc.)
- Time stamps = “T#” markers with descriptions and approximate elapsed times for general reference. Specific timing transitions are dependent upon PDN design (see PDN User Guide for details).

6.9.2.1 Power Supply Slew Rate Requirement

To maintain the safe operating range of the internal ESD protection devices, TI recommends limiting the maximum slew rate of supplies to be less than 100 mV/us, as shown in 図 6-2. For instance, a 1.8V supply should have a ramp time > 18 µs to ensure the slew rate < 100mV/us.

図 6-2 describes the Power Supply Slew Rate Requirement in the device.

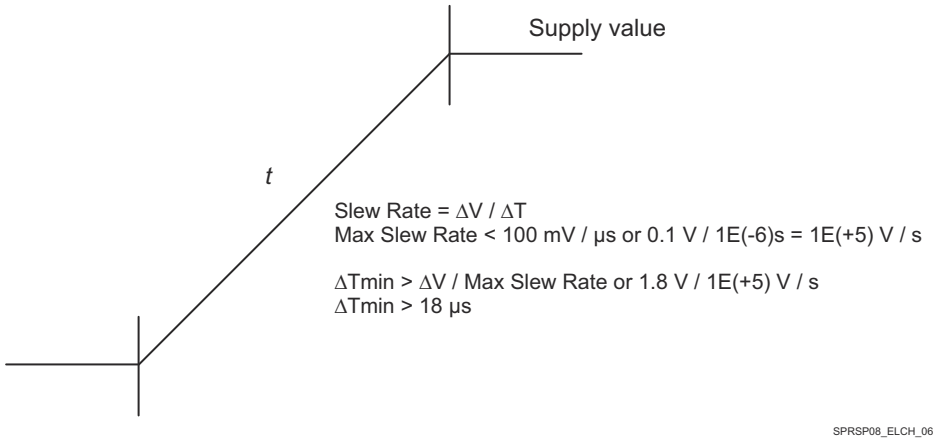

図 6-2. Power Supply Slew and Slew Rate

6.9.2.2 Combined MCU and Main Domains Power-Up Sequencing

図 6-3 describes the primary power-up sequencing when similar MCU and Main voltage domains are combined into common power rails. Combining MCU and Main voltage domains simplifies PDN design by reducing total number of power rails and sources while making MCU and Main processor sub-systems operational dependent on common power rails. 表 8-1 in セクション 8.1, *Power Supply Mapping* captures recommended device power supply groups to power rail mapping summary.

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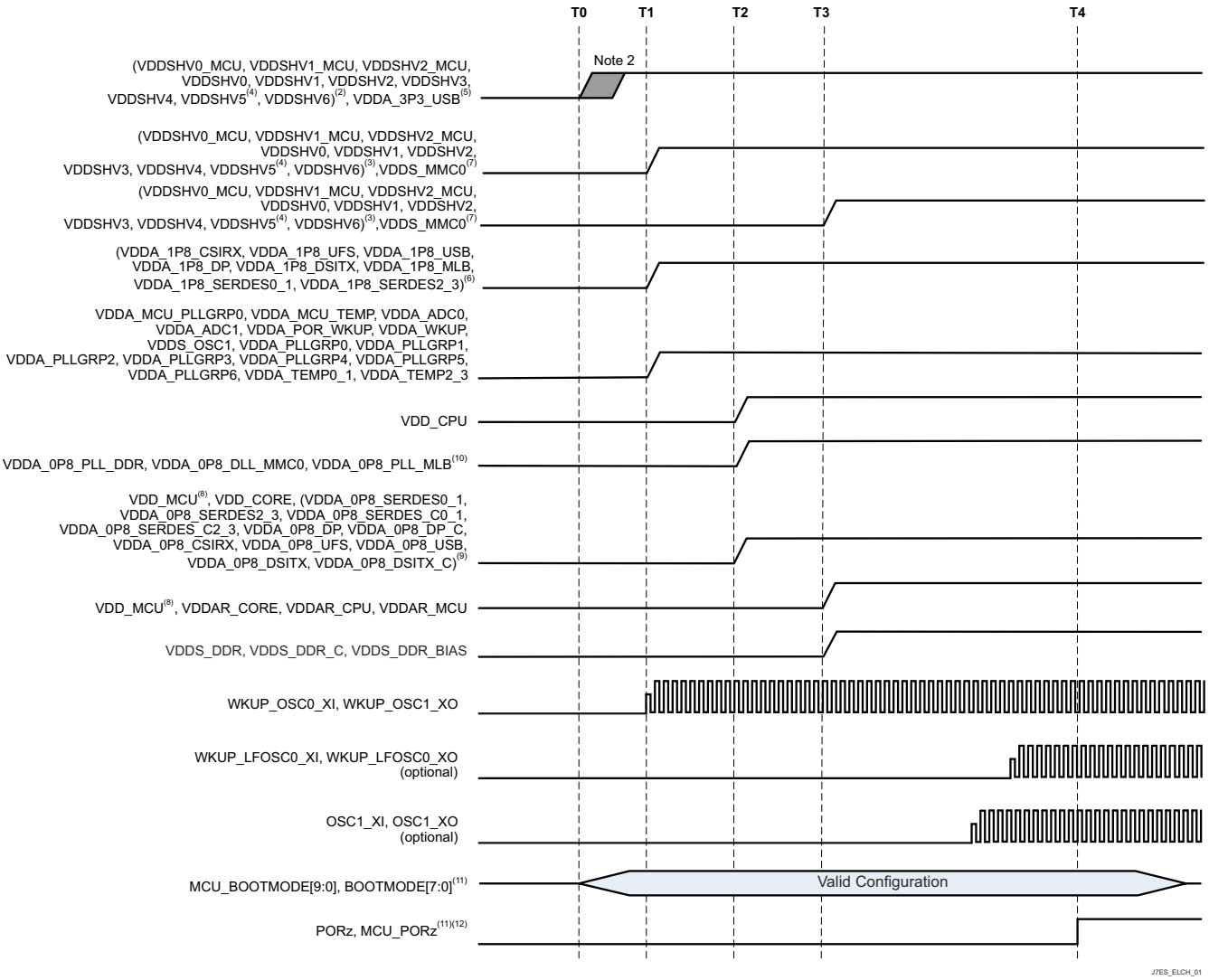

図 6-3. Combined MCU and Main Domains, Primary Power-Up Sequence

1. Time Stamp Markers

   T0 – 3.3V voltages start ramp-up to $V_{OPR\ MIN}$. (0ms)

   T1 – 1.8V voltages start ramp-up to $V_{OPR\ MIN}$. (2ms)

   T2 – Low voltage core supplies start ramp-up to $V_{OPR\ MIN}$. (3ms)

   T3 – Low voltage RAM array voltages start ramp-up to $V_{OPR\ MIN}$. (4ms)

   T4 – OSC1 is stable and PORz/MCU_PORz are de-asserted to release processor from reset. (13ms)
2. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces. A few supplies could have varying start times between T0 to T1 due to PDN designs using different power resources with varying turn-on & ramp-up time delays.
3. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 1.8V to support 1.8V digital interfaces. When eMMC memories are used, Main 1.8V supplies could have a ramp-up aligned to T3 due to PDN designs grouping supplies with VDD_MMC0.
4. VDDSHV5 supports MMC1 signaling for SD memory cards. If compliant high-speed SD card operation is needed, then an independent, dual voltage (3.3V/1.8V) power source and rail are required. The start of ramp-up to 3.3V will be same as other 3.3V domains as shown. If SD card is not needed or standard data

rates with fixed 3.3V operation is acceptable, then domain can be grouped with digital IO 3.3V power rail. If a SD card is capable of operating with fixed 1.8V, then domain can be grouped with digital IO 1.8V power rail.

5. VDDA_3P3_USB is 3.3V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-up to 3.3V will be same as other 3.3V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3V digital IO power rail either directly or through a supply filter.
6. VDDA_1P8_<phy> are 1.8V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8V power rail either directly or through an in-line supply filter is allowed.
7. VDD_MMC0 is 1.8V digital supply supporting MMC0 signaling for eMMC interface. If MMC0 or eMMC0 interface is not needed, then domain can be grouped with digital IO 1.8V power rail with power up time stamp at T1. However, if MMC0 interface is needed, then VDD_MMC0 must not start ramp-up until time stamp T3 after VDD_CORE has reached $V_{OPR\ MIN}$. Any MCU or Main dual voltage IO operating at 1.8V can be grouped with VDD_MMC0 into a common power rail with power up time stamp T3.
8. VDD_MCU is a digital voltage supply with a wide operational voltage range and power sequencing flexibility, enabling it to be grouped and ramped-up with either 0.8V VDD_CORE at time stamp T2 or 0.85V RAM array domains (VDDAR_xxx) at time stamp T3.
9. VDDA_1P8_<clk/pll/ana> are 1.8V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine analog VDDA_1P8_<phy> domains or digital VDDSHVn_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals.
10. VDDA_0P8_<dll/pll> are 0.8V analog domains supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
11. Minimum set-up and hold times shown with respect to MCU_PORz and PORz asserting high to latch MCU_BOOTMODEn (referenced to MCU_VDDSHV0) and BOOTMODEn (reference to VDDSHV2) settings into registers during power up sequence.
12. Minimum elapsed time from crystal oscillator circuitry being energized (VDDS_OSC1 at T1) until stable clock frequency is reached depends upon on crystal oscillator, capacitor parameters and PCB parasitic values. A conservative 10ms elapsed time defined by (T4 – T1) time stamps is shown. This could be reduced depending upon customer's clock circuit (that is, crystal oscillator or clock generator) and PCB designs.

6.9.2.3 Combined MCU and Main Domains Power- Down Sequencing

図 6-4 describes the device power-down sequencing.

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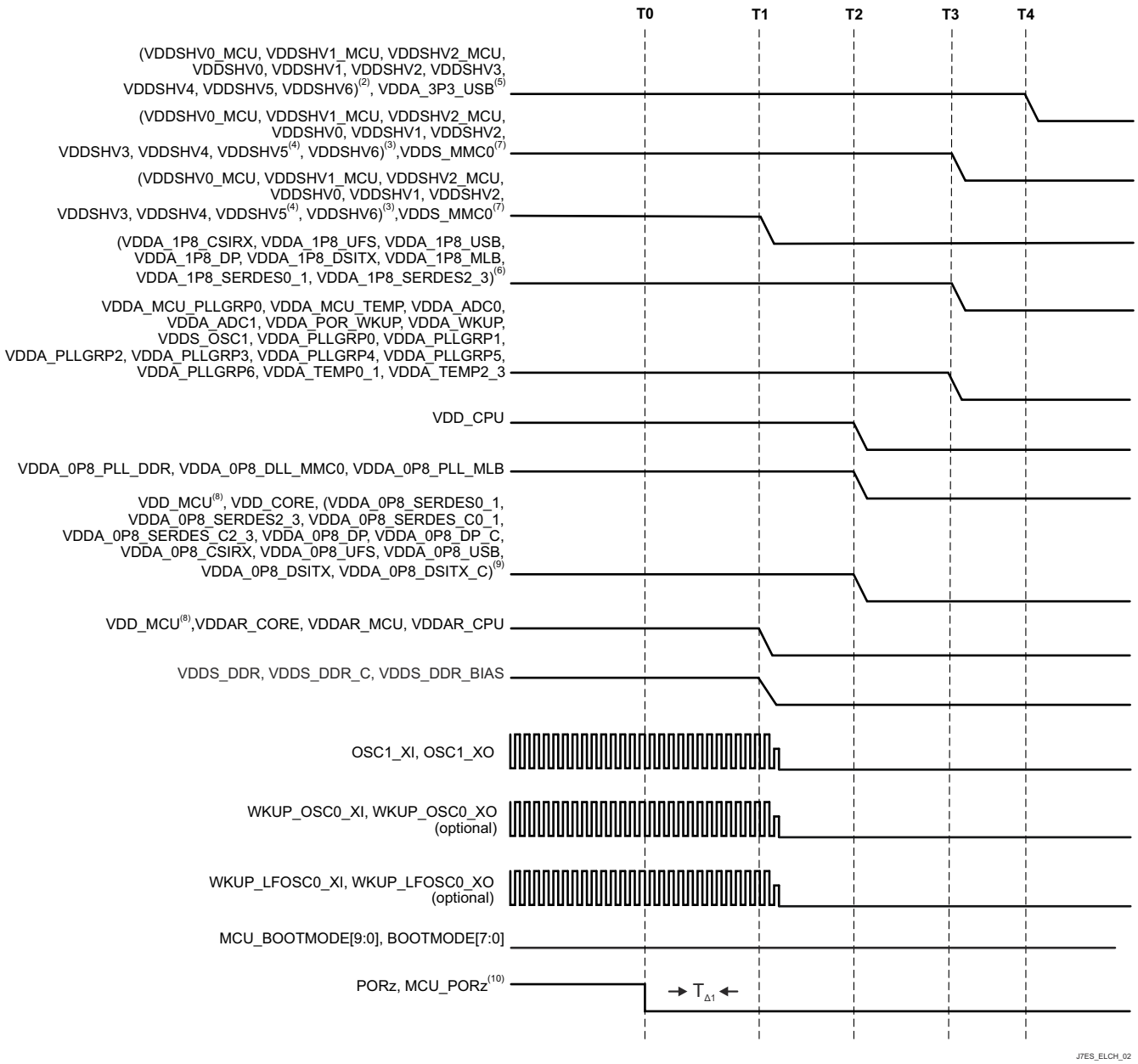

図 6-4. Combined MCU and Main Domains, Primary Power-Down Sequence

1. Time Stamp Markers

   T0 – MCU_PORz & PORz assert low to put all processor resources in safe state. (0ms)

   T1 – Main DDR, SRAM Core & SRAM CPU power supplies start ramp-down. (0.5ms)

   T2 – Low voltage core supplies start supply ramp-down. (2.5ms)

   T3 - 1.8V voltages start supply ramp-down. (3.0ms)

   T4 – 3.3V voltages start supply ramp-down. (3.5ms)
2. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces

3. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 1.8V to support 1.8V digital interfaces. When eMMC memories are used, Main 1.8V supplies could have a ramp-down aligned to T1 due to PDN designs grouping supplies with VDD_MMC0.
4. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3V/1.8V) power rail is required for compliant, high-speed SD card operations. If compliant highspeed SD card operation is needed, then an independent, dual voltage (3.3V/1.8V) power source and rail are required. The start of ramp-down from 3.3V/1.8V will be same as other 3.3V domains as shown. If SD card is not needed or standard data rates with fixed 3.3V operation is acceptable, then domain can be grouped with digital IO 3.3V power rail. If a SD card is capable of operating with fixed 1.8V, then domain can be grouped with digital IO 1.8V power rail.
5. VDDA_3P3_USB is 3.3V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-down from 3.3V will be same as other 3.3V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3V digital IO power rail either directly or through a supply filter.
6. VDDA_1P8_<phy> are 1.8V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8V power rail either directly or through an in-line supply filter is allowed.
7. VDD_MMC0 is 1.8V digital supply supporting MMC0 signaling for eMMC interface and must ramp-down at time stamp T1 before VDD_CORE starts ramp-down. Any MCU or Main dual voltage IO operating at 1.8V can be grouped with VDD_MMC0 into a common power rail with power down time stamp T1. If MMC0 or eMMC0 interface is not needed, then domain can be grouped with digital IO 1.8V power rail and ramp-down at time stamp T3.
8. VDD_MCU is a digital voltage supply with a wide operational voltage range and power sequencing flexibility, enabling it to be grouped and ramped-down with either 0.8V VDD_CORE at time stamp T2 or 0.85V RAM array domains (VDDAR_xxx) at time stamp T1.
9. VDDA_1P8_<clk/pll/ana> are 1.8V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine analog VDDA_1P8_<phy> domains or digital VDDSHVn_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals.
10. MCU_PORz and PORz must be asserted low for TΔ1 = 200us min to ensure SoC resources enter into safe state before any voltage begins to ramp down.

6.9.2.4 Isolated MCU and Main Domains Power- Up Sequencing

Isolated MCU and Main voltage domains enable an SoC's MCU and Main processor sub-systems to operate independently. There are 2 reasons an SoC's PDN design may need to support independent MCU and Main processor functionality. First is to provide flexibility to enable SoC low power modes that can significant reduce SoC power dissipation when processor operations are not needed. Second is to enable robustness to gain freedom from interference (FFI) of a single fault impacting both MCU and Main processor sub-systems which is especially beneficial if using the SoC's MCU as the system safety monitoring processor. The number of additional PDN power rails needed is dependent upon number of different MCU IO signaling voltage levels. If only 1.8V IO signaling is used, the only 2 additional power rails could be required. If both 1.8 and 3.3V IO signaling is desired, then 4 additional power rails could be needed. 表 8-2 in セクション 8.1, *Power Supply Mapping* captures recommended device power supplies to power rail mapping summary.

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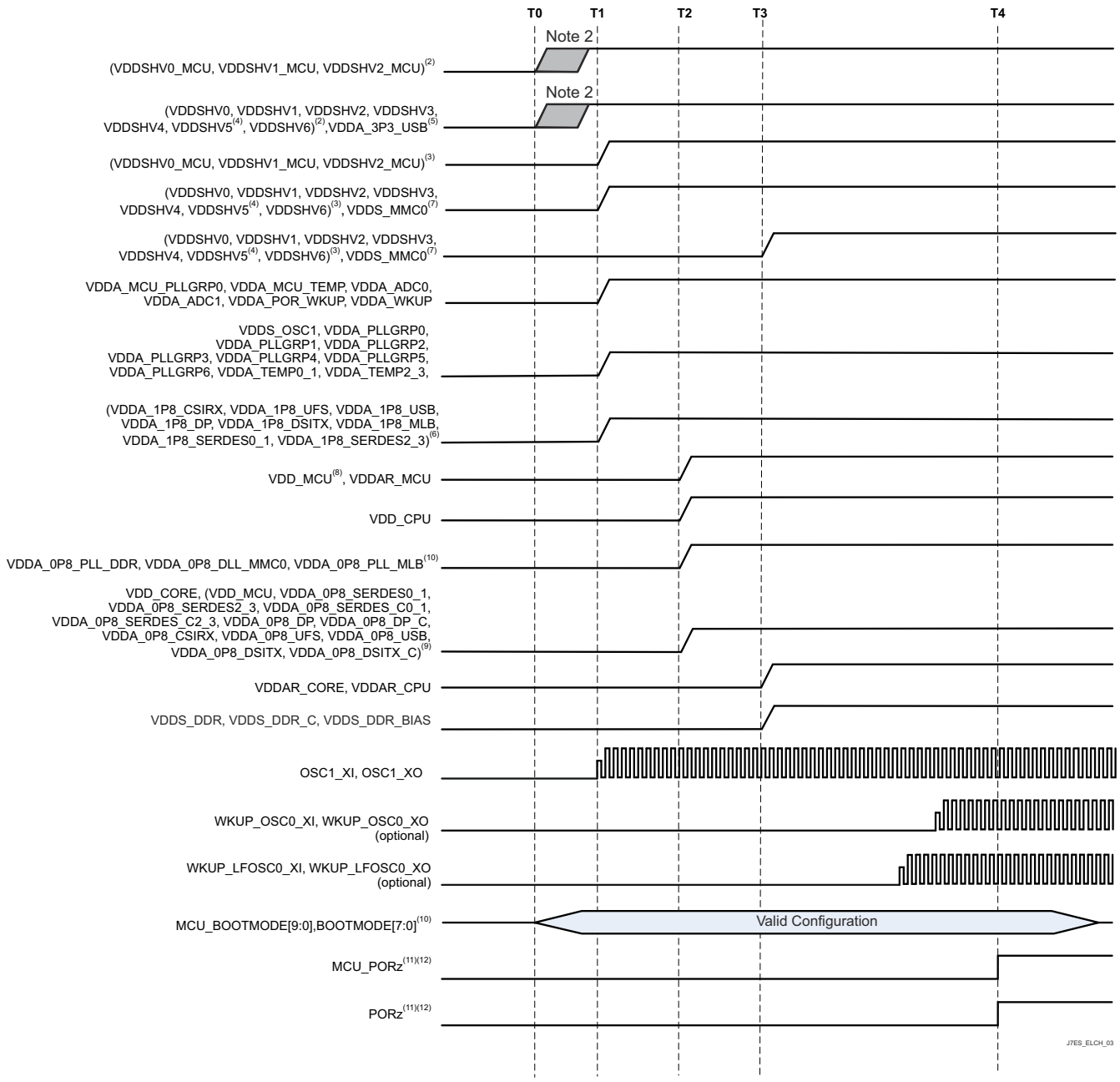

図 6-5. Isolated MCU and Main Domains, Primary Power-Up Sequence

1. Time Stamp Markers

   T0 – 3.3V voltages start ramp-up to $V_{OPR\ MIN}$. (0ms)

   T1 – 1.8V voltages startramp-up to $V_{OPR\ MIN}$. (2ms)

   T2 – Low voltage core supplies start ramp-up to $V_{OPR\ MIN}$. (3ms)

   T3 – Low voltage RAM array voltages start ramp-up to $V_{OPR\ MIN}$. (4ms)

   T4 – OSC1 is stable and PORz/MCU_PORz are de-asserted to release processor from reset. (13ms)
2. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces. A few supplies could have varying start times between T0 to T1 due to PDN designs using different power resources with varying turn-on & ramp-up time delays.

3. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 1.8V to support 1.8V digital interfaces. When eMMC memories are used, Main 1.8V supplies could have delayed start times that aligns to T3 due to PDN designs grouping supplies with VDD_MMC0.
4. VDDSHV5 supports MMC1 signaling for SD memory cards. If compliant UHS-I SD card operation is needed, then an independent, dual voltage (3.3V/1.8V) power source and rail are required. The start of ramp-up to 3.3V will be same as other 3.3V domains as shown. If SD card is not needed or standard data rates with fixed 3.3V operation is acceptable, then supply can be grouped with digital IO 3.3V power rail. If a SD card is capable of operating with fixed 1.8V, then supply can be grouped with digital IO 1.8V power rail.
5. VDDA_3P3_USB is 3.3V analog supply used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-up to 3.3V will be same as other 3.3V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then supply can be grouped with 3.3V digital IO power rail either directly or through a supply filter.
6. VDDA_1P8_<phy> are 1.8V analog supplies supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then supplies can be grouped with digital IO 1.8V power rail either directly or through an in-line supply filter is allowed.
7. VDD_MMC0 is 1.8V digital supply supporting MMC0 signaling for eMMC interface and must ramp up at time stamp T3. Any MCU or Main dual voltage IO operating at 1.8V can be grouped with VDD_MMC0 into a common power rail with a ramp-up at time stamp T3. If MMC0 or eMMC0 interface is not needed, then domain can be grouped with digital IO 1.8V power rail with ramp-up at time stamp T1.
8. VDD_MCU is a digital voltage supply with a wide operational voltage range and power sequencing flexibility, enabling it to be grouped and ramped-up with either 0.8V VDD_CORE at time stamp T2 or 0.85V RAM array domains (VDDAR_xxx) at time stamp T3.
9. VDDA_1P8_<clk/pll/ana> are 1.8V analog supplies supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine analog VDDA_1P8_<phy> domains or digital VDDSHVn_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals.
10. VDDA_0P8_<dll/pll> are 0.8V analog supplies supporting PLL and DLL circuitry needing a low noise supply for optimal performance. It is not recommended to combine these domains with any other 0.8V domains since high frequency switching noise could negatively impact jitter performance of PLL and DLL signals.
11. Minimum set-up and hold times shown with respect to MCU_PORz and PORz asserting high to latch MCU_BOOTMODEn (referenced to MCU_VDDSHV0) and BOOTMODEn (reference to VDDSHV2) settings into registers during power up sequence.
12. Minimum elapsed time from crystal oscillator circuitry being energized (VDDS_OSC1 at T1) until stable clock frequency is reached depends upon on crystal oscillator, capacitor parameters and PCB parasitic values. A conservative 10ms elapsed time defined by (T4 – T1) time stamps is shown. This could be reduced depending upon customer's clock circuit (that is, crystal oscillator or clock generator) and PCB designs.

6.9.2.5 Isolated MCU and Main Domains, Primary Power- Down Sequencing

図 6-6 describes the device power-down sequencing.

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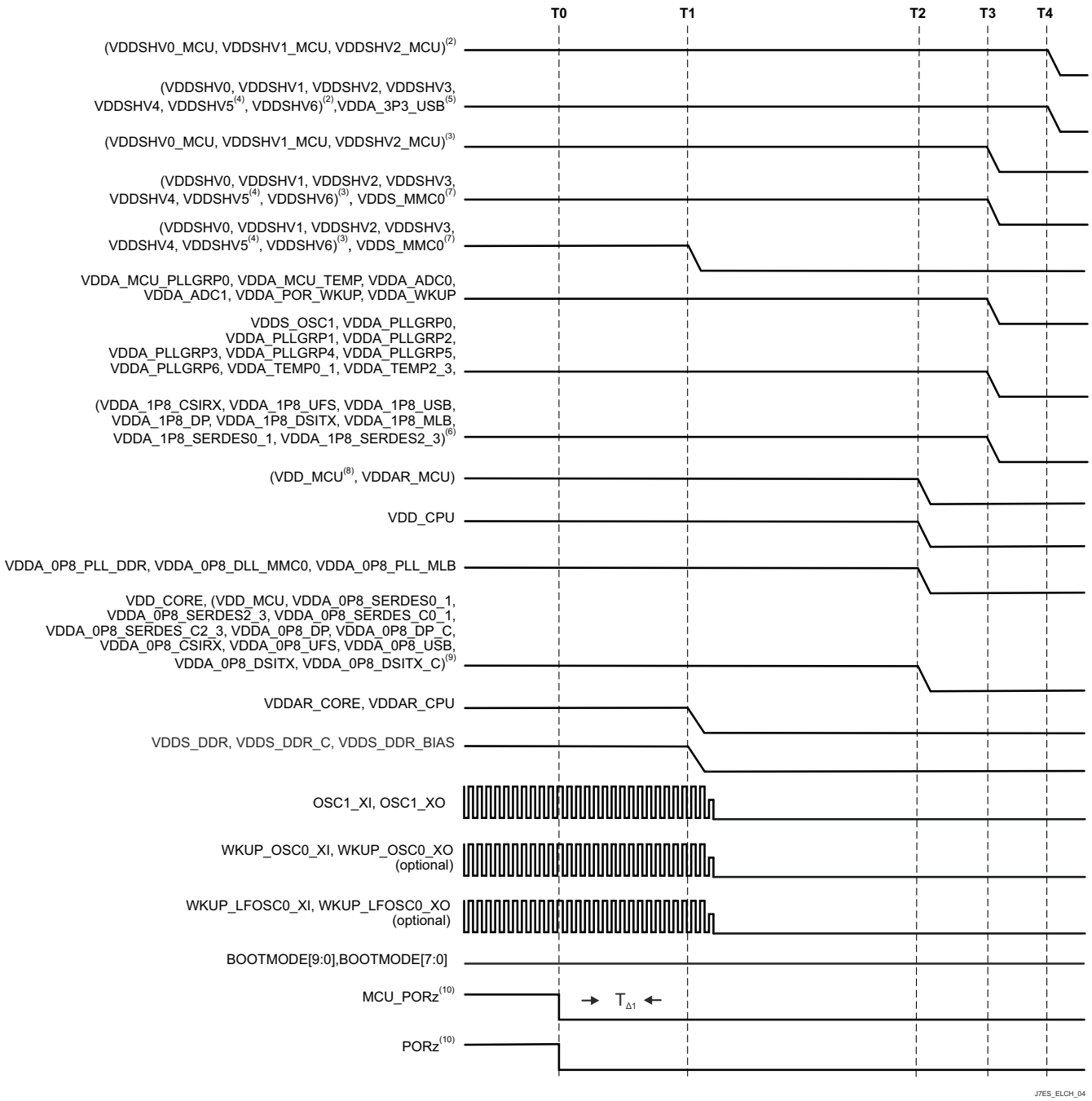

図 6-6. Isolated MCU and Main Domains, Primary Power- Down Sequencing

1. Time Stamp Markers

   T0 – MCU_PORz & PORz assert low to put all processor resources in safe state. (0ms)

   T1 – Main DDR, SRAM Core & SRAM CPU power supplies start ramp-down. (0.5ms)

   T2 – Low voltage core supplies start supply ramp-down. (2.5ms)

   T3 - 1.8V voltages start supply ramp-down. (3.0ms)

   T4 – 3.3V voltages start supply ramp-down. (3.5ms)

2. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces
3. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 1.8V to support 1.8V digital interfaces. When eMMC memories are used, Main 1.8V supplies could have a ramp-down aligned to T1 due to PDN designs grouping supplies with VDD_MMC0.
4. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3V/1.8V) power rail is required for compliant, high-speed SD card operations. If compliant highspeed SD card operation is needed, then an independent, dual voltage (3.3V/1.8V) power source and rail are required. The start of ramp-down from 3.3V/1.8V will be same as other 3.3V domains as shown. If SD card is not needed or standard data rates with fixed 3.3V operation is acceptable, then domain can be grouped with digital IO 3.3V power rail. If a SD card is capable of operating with fixed 1.8V, then domain can be grouped with digital IO 1.8V power rail.
5. VDDA_3P3_USB is 3.3V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. The start of ramp-down from 3.3V will be same as other 3.3V domains as shown. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3V digital IO power rail either directly or through a supply filter.
6. VDDA_1P8_<phy> are 1.8V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8V power rail either directly or through an in-line supply filter is allowed.
7. VDD_MMC0 is 1.8V digital supply supporting MMC0 signaling for eMMC interface and must ramp-down at time stamp T1 before VDD_CORE starts ramp-down. Any MCU or Main dual voltage IO operating at 1.8V can be grouped with VDD_MMC0 into a common power rail with power down time stamp T1. If MMC0 or eMMC0 interface is not needed, then domain can be grouped with digital IO 1.8V power rail and ramp-down at time stamp T3.
8. VDD_MCU is a digital voltage supply with a wide operating voltage range and power sequencing flexibility, enabling it to be grouped and ramped-down with either 0.8V VDD_CORE at time stamp T2 or 0.85V RAM array domains (VDDAR_xxx) at time stamp T1.
9. VDDA_1P8_<clk/pll/ana> are 1.8V analog domains supporting clock oscillator, PLL & analog circuitry needing a low noise supply for optimal performance. It is not recommended to combine analog VDDA_1P8_<phy> domains or digital VDDSHVn_MCU and VDDSHVn IO domains since high frequency switching noise could negatively impact jitter performance of clock, PLL and DLL signals.
10. MCU_PORz and PORz must be asserted low for TΔ1 = 200us min to ensure SoC resources enter into safe state before any voltage begins to ramp down.

6.9.2.6 Entry and Exit of MCU Only State

Entry into MCU Only lower power state is accomplished by executing a power down sequence except for the 4 MCU supply groups (VDDSHVx_MCU at 3.3V, VDDSHVx_MCU at 1.8V, VDDA_MCU_PLLGRP0/VDDA_MCU_TEMP analog supplies at 1.8V, VDD_MCU/VDDAR_MCU at 0.85V) that remain energized. Exit from MCU Only state is accomplished by executing a power up sequence with the 4 MCU supply groups remaining energized throughout the sequence. The example diagram shown is for an Isolated MCU & Main PDN type with eMMC support.

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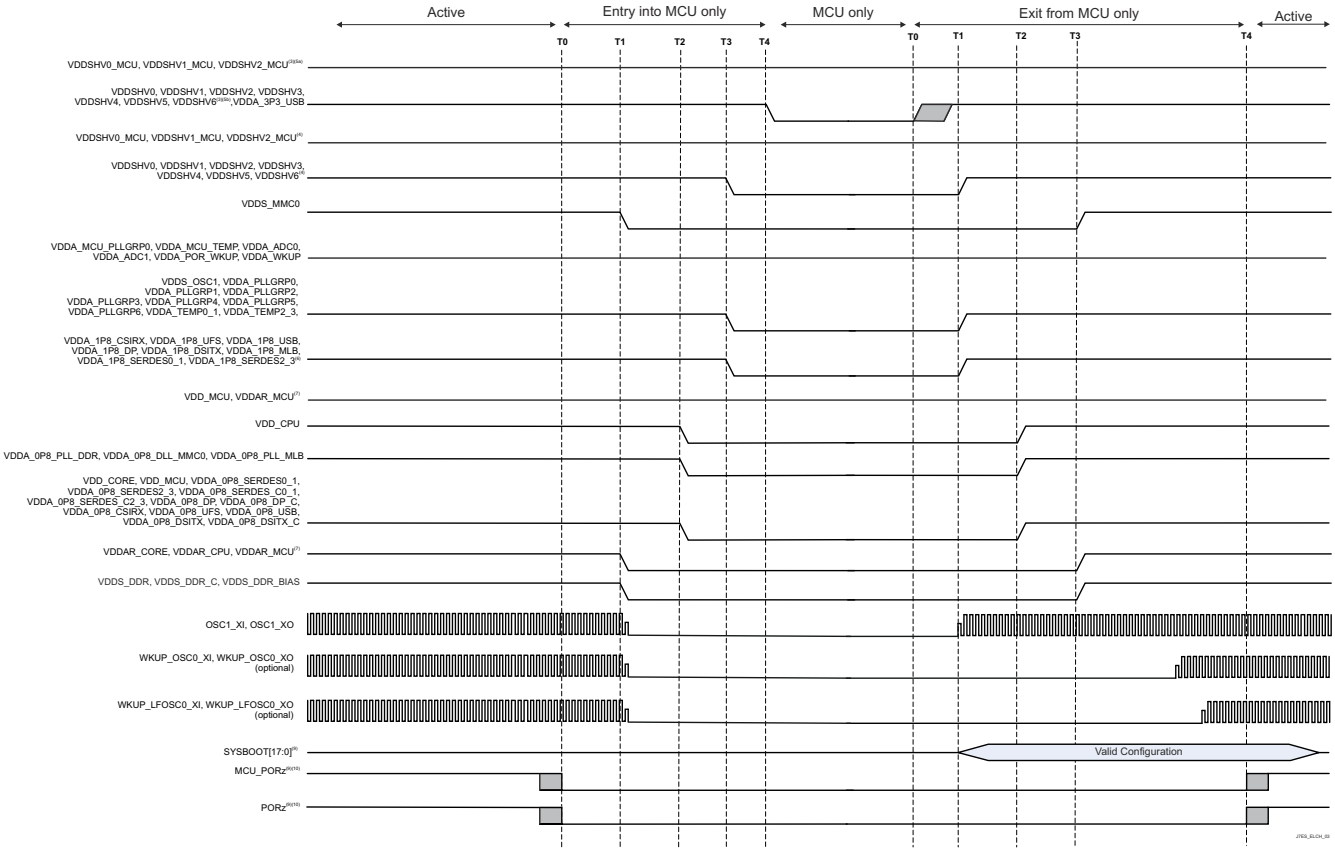

図 6-7. Entry and Exit of MCU Only Sequencing

6.9.2.7 Entry and Exit of DDR Retention State

Entry into DDR Retention (Suspend-to-RAM or S2R) state is accomplished by executing a power down sequence except for the 1 device DDR supply group (VDDS_DDR_BIAS, VDDS_DDR, and VDDS_DDR_C at 1.1V), and 1 additional discrete SDRAM supply (VDD_LPDDR4_1V8 at 1.8V; not shown in diagram below) that remain energized. Exit from DDR Retention state is accomplished by executing a power up sequence with these 2 DDR supply groups remaining energized throughout the sequence. The example diagram shown is for an Isolated MCU & Main PDN type with eMMC support.

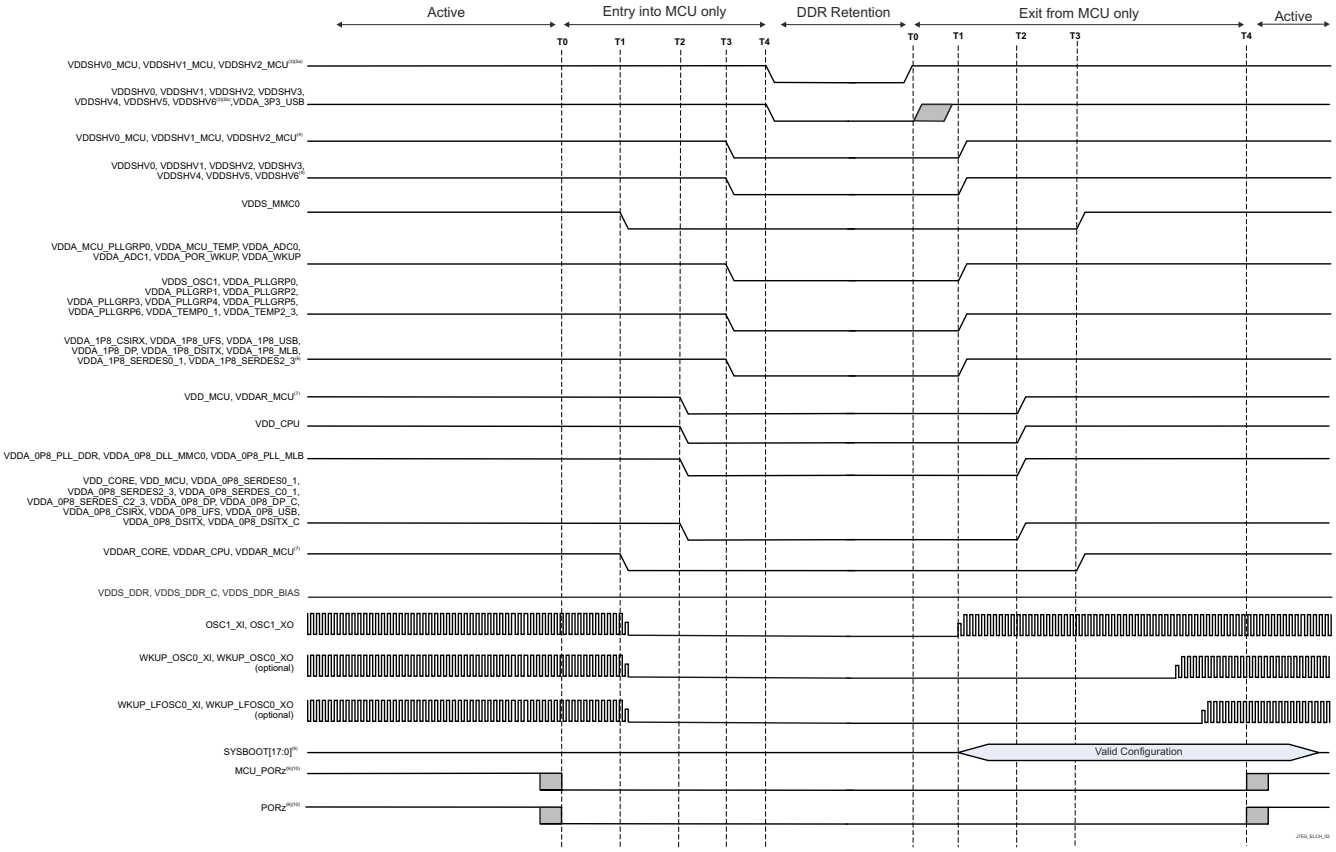

図 6-8. Entry and Exit of DDR Retention Sequencing

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6.9.3 System Timing

For more details about features and additional description information on the subsystem multiplexing signals, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

表 6-13. System Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	2	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	3	30	pF

6.9.3.1 Reset Timing

Tables and figures provided in this section define timing requirements and switching characteristics for reset related signals.

表 6-14. MCU_PORz Timing Requirements

see 図 6-9

NO.			MIN	TYP	MAX	UNIT
RST1	$t_{h(MCUD_SUPPLIES_VALID - MCU_PORz)}$	Hold time, MCU_PORz active (low) at Power-up after all MCU DOMAIN supplies valid (using external crystal)	N + 1200[(2)]	9500000		ns
RST2		Hold time, MCU_PORz active (low) at Power-up after all MCU DOMAIN supplies[(1)] valid and external clock stable (using external LVCMOS oscillator)	1200			ns
RST3	$t_{w(MCU_PORzL)}$	Pulse Width minimum, MCU_PORz low after Power-up (without removal of Power or system reference clock MCU_OSC0_XI/XO)	1200			ns

(1) For definition of the MCU DOMAIN supplies, see the Combined MCU and Main Domains Power-Up sequence.
(2) N = oscillator start-up time

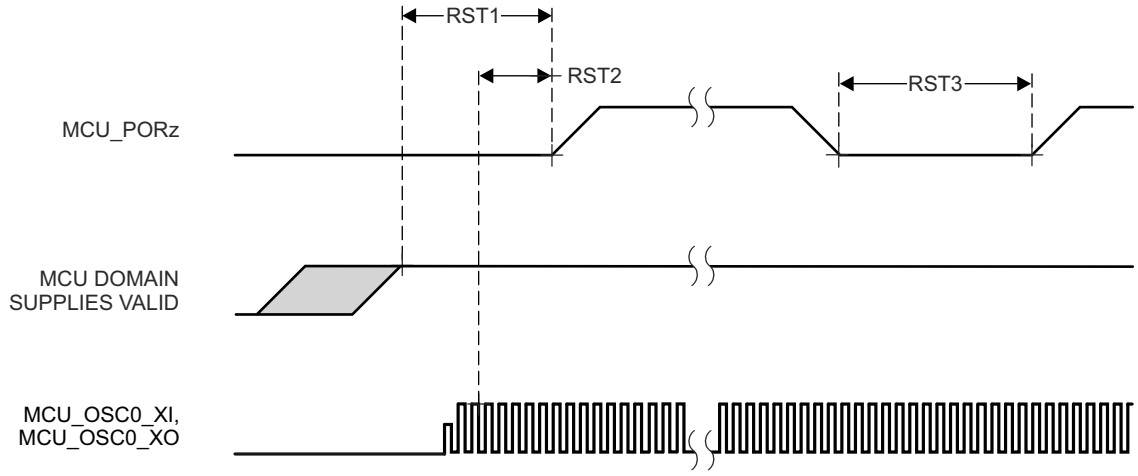

図 6-9. MCU_PORz Timing Requirements

表 6-15. PORz Timing Requirements

see 図 6-10

NO.			MIN	MAX	UNIT
RST4	$t_{h(MAIND_SUPPLIES_VALID - PORz)}$	Hold time, PORz active (low) at Power-up after all MAIN DOMAIN supplies1 valid	1200		ns
RST5	$t_{w(PORzL)}$	Pulse Width minimum, PORz low after Power-up	1200		ns

1. For definition of the MAIN DOMAIN supplies, see the Combined MCU and Main Domains Power-Up sequence.

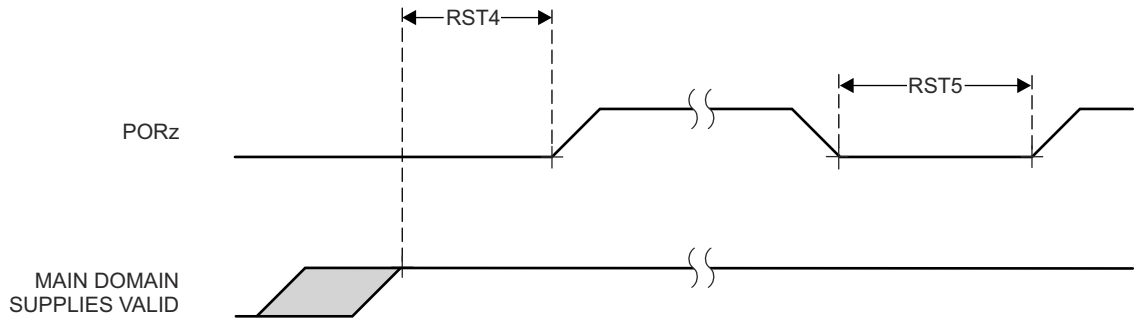

図 6-10. PORz Timing Requirements

表 6-16. MCU_PORz initiates; MCU_PORz_OUT, PORz_OUT, MCU_RESETSTATz, and RESETSTATz Switching Characteristics

see 図 6-11

NO.	PARAMETER		MODE	MIN	MAX	UNIT
RST6	$t_{d(MCU_PORzL-MCU_PORz_OUTL)}$	Delay time, MCU_PORz active (low) to MCU_PORz_OUT active (low)		0		ns
RST7	$t_{d(MCU_PORzH-MCU_PORz_OUTH)}$	Delay time, MCU_PORz inactive (high) to MCU_PORz_OUT inactive (high)		0		ns
RST8	$t_{d(MCU_PORzL-PORz_OUTL)}$	Delay time, MCU_PORz active (low) to PORz_OUT active (low)		0		ns
RST9	$t_{d(MCU_PORzH-PORz_OUTH)}$	Delay time, MCU_PORz inactive (high) to PORz_OUT inactive (high)		1500		ns
RST10	$t_{d(MCU_PORzL-MCU_RESETSTATzL)}$	Delay time, MCU_PORz active (low) to MCU_RESETSTATz active (low)		0		ns
RST11	$t_{d(MCU_PORzH-MCU_RESETSTATzH)}$	Delay time, MCU_PORz inactive (high) to MCU_RESETSTATz inactive (high)	POST bypass	12000*S(1)		ns
RST12	$t_{d(MCU_PORzL-RESETSTATzL)}$	Delay time, MCU_PORz active (low) to RESETSTATz active (low)		0		ns
RST13	$t_{d(MCU_PORzH-RESETSTATzH)}$	Delay time, MCU_PORz inactive (high) to RESETSTATz inactive (high)		14500*S(1)		ns
RST14	$t_{w(MCU_PORz_OUTL)}$	Pulse width minimum, MCU_PORz_OUT active (low)		1200		ns
RST15	$t_{w(PORz_OUTL)}$	Pulse Width Minimum PORz_OUT low		2550		ns
RST16	$t_{w(MCU_RESETSTATzL)}$	Pulse Width Minimum MCU_RESETSTATz low		3900*S(1)		ns
RST17	$t_{w(RESETSTATzL)}$	Pulse Width Minimum RESETSTATz low		2650*S(1)		ns

(1) S = MCU_OSC0_XI/XO clock period.

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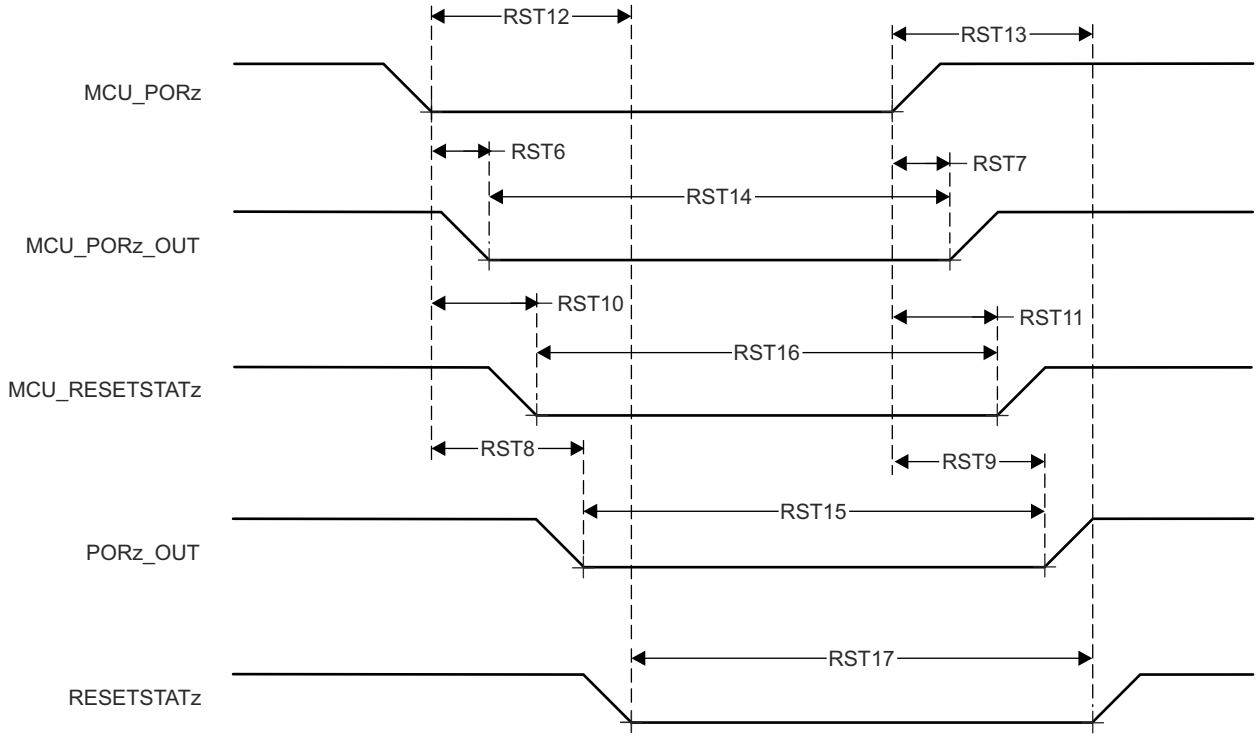

図 6-11. MCU_PORz initiates; MCU_PORz_OUT, PORz_OUT, MCU_RESETSTATz, and RESETSTATz Switching Characteristics

表 6-17. PORz Initiates; PORz_OUT and RESETSTATz Switching Characteristics

see 図 6-12

NO.	PARAMETER		MODE	MIN	MAX	UNIT
RST18	$t_{d(PORzL-PORz_OUTL)}$	Delay time, PORz active (low) toPORz_OUT active (low)	software control of POR_RST_ISO_DONE_Z	T(1)		
			CTRLMMR_WKUP_POR_RST_CTRL[0].POR_RST_ISO_DONE_Z = 0	0		ns
RST19	$t_{d(PORzH-PORz_OUTH)}$	Delay time, PORz active (high) toPORz_OUT active (high)		1300		ns
RST20	$t_{d(PORzL-RESETSTATzL)}$	Delay time, PORz active (low) to RESETSTATz active (low)		T(1)		
			CTRLMMR_WKUP_POR_RST_CTRL[0].POR_RST_ISO_DONE_Z = 0	0		ns
RST21	$t_{d(PORzH-RESETSTATzH)}$	Delay time, PORz active (high) to RESETSTATz active (high)		14500*S (2)		ns

(1) T = Reset Isolation Time (Software Dependent).
(2) S = MCU_OSC0_XI/XO clock period.

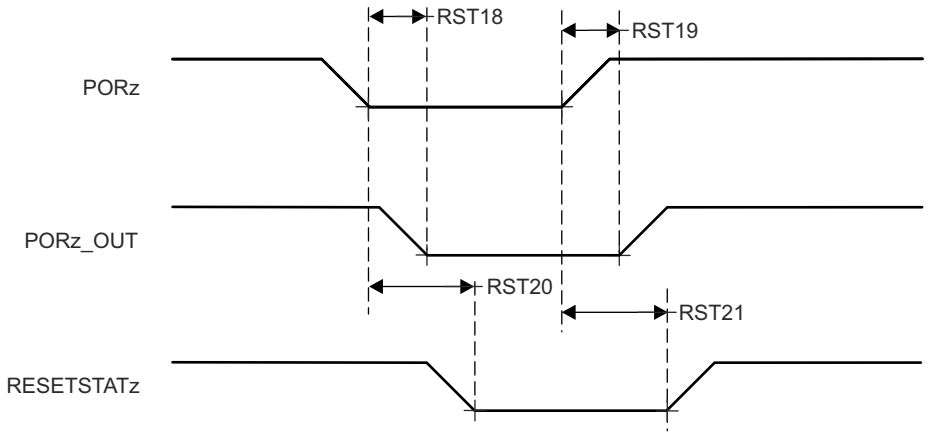

図 6-12. PORz initiates; PORz_OUT and RESETSTATz Switching Characteristics

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表 6-18. MCU_RESETz Timing Requirements

see 図 6-13

NO.			MIN	MAX	UNIT
RST22	$t_{w(MCU_RESETzL)}$ (1)	Pulse Width minimum, MCU_RESETz active (low)	1200		ns

(1) Timing for MCU_RESETz is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

表 6-19. MCU_RESETz initiates; MCU_RESETSTATz, and RESETSTATz Switching Characteristics

see 図 6-13

NO.	PARAMETER		MIN	MAX	UNIT
RST23	$t_{d(MCU_RESETzL-MCU_RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to MCU_RESETSTATz active (low)	800		ns
RST24	$t_{d(MCU_RESETzH-MCU_RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to MCU_RESETSTATz inactive (high)	3900*S(1)		ns
RST25	$t_{d(MCU_RESETzL-RESETSTATzL)}$	Delay time, MCU_RESETz active (low) to RESETSTATz active (low)	800		ns
RST26	$t_{d(MCU_RESETzH-RESETSTATzH)}$	Delay time, MCU_RESETz inactive (high) to RESETSTATz inactive (high)	3900*S(1)		ns

(1) S = MCU_OSC0_XI/XO clock period.

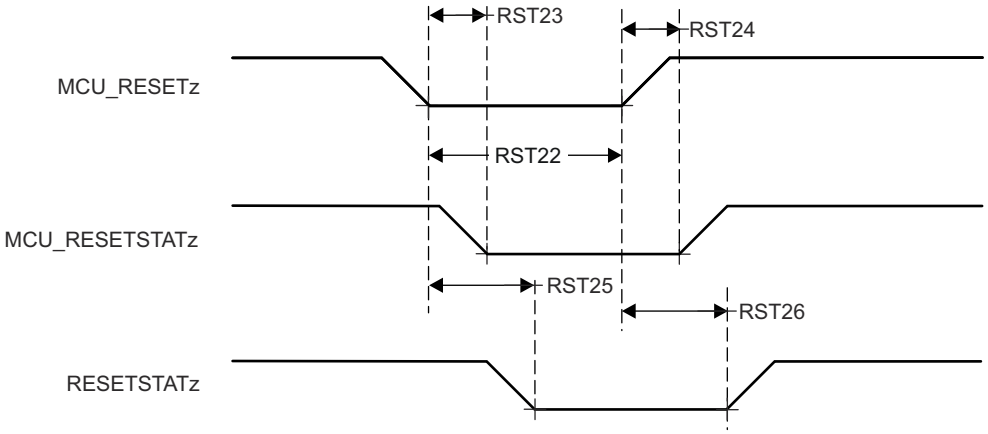

図 6-13. MCU_RESETz initiates; MCU_RESETSTATz, and RESETSTATz Timing Requirements and Switching Characteristics

表 6-20. RESET_REQz Timing Requirements

see 図 6-14

NO.			MIN	MAX	UNIT
RST27	$t_{w(RESET_REQzL)}$ (1)	Pulse Width minimum, RESET_REQz active (low)	1200		ns

(1) Timing for RESET_REQz is valid only after all supplies are valid and MCU_PORz has been asserted for the specified time.

表 6-21. RESET_REQz initiates; RESETSTATz Switching Characteristics

see 図 6-14

NO.	PARAMETER		MODE	MIN	MAX	UNIT
RST28	$t_{d(RESET_REQzL-RESETSTATzL)}$	Delay time, RESET_REQz active (low) to RESETSTATz active (low)	software control of SOC_WARMRST_ISO_DONE_Z	T(1)		
			CTRLMMR_WKUP_MAIN_WARM_RST_CTRL[0].SOC_WARMRST_ISO_DONE_Z = 0	740		ns
RST29	$t_{d(RESET_REQzH-RESETSTATzH)}$	Delay time, RESET_REQz inactive (high) to RESETSTATz inactive (high)		2650*S (2)		ns

(1) T = Reset Isolation Time (Software Dependent).
(2) S = MCU_OSC0_XI/XO clock period.

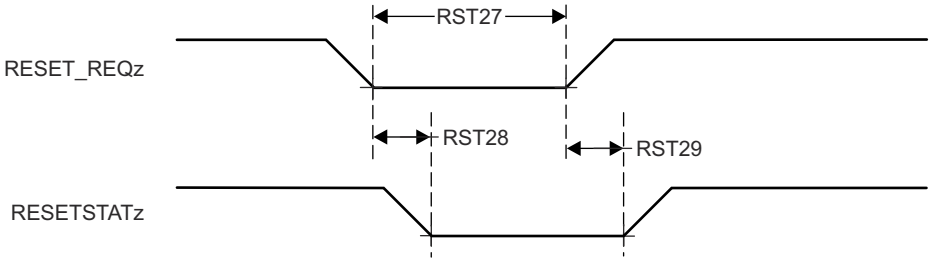

図 6-14. RESET_REQz initiates; RESETSTATz Timing Requirements and Switching Characteristics

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表 6-22. EMUx Timing Requirements

see 図 6-15

NO.			MIN	MAX	UNIT
RST30	$t_{su(EMUx-MCU_PORz)}$	Setup time, EMU[1:0] before MCU_PORz inactive (high)	3*S(1)		ns
RST31	$t_{h(MCU_PORz - EMUx)}$	Hold time, EMU[1:0] after MCU_PORz inactive (high)	10		ns

(1) S = MCU_OSC0_XI/XO clock period.

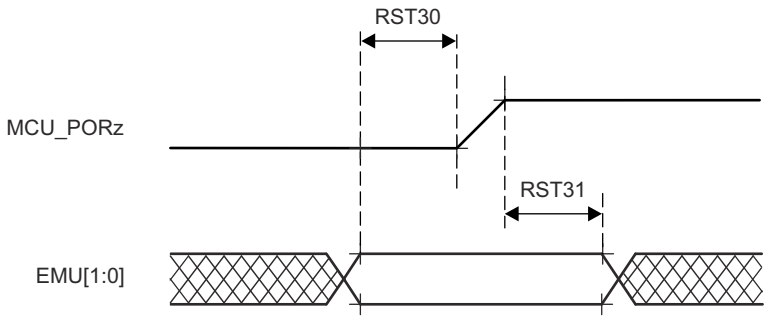

図 6-15. EMUx Timing Requirements

表 6-23. MCU_BOOTMODE Timing Requirements

see 図 6-16

NO.			MIN	MAX	UNIT
RST32	$t_{su(MCU_BOOTMODE-MCU_PORz_OUT)}$	Setup time, MCU_BOOTMODE[09:00] before MCU_PORz_OUT high	3*S(1)		ns
RST33	$t_{h(MCU_PORz_OUT - MCU_BOOTMODE)}$	Hold time, MCU_BOOTMODE[09:00] after MCU_PORz_OUT high	0		ns

(1) S = MCU_OSC0_XI/XO clock period.

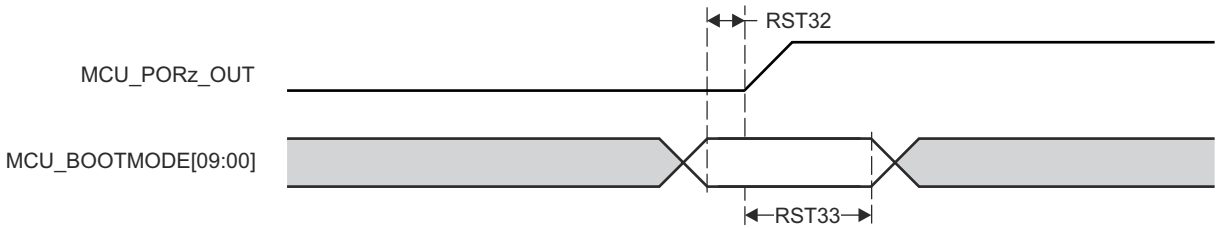

図 6-16. MCU_BOOTMODE Timing Requirements

表 6-24. BOOTMODE Timing Requirements

see 図 6-17

NO.			MIN	MAX	UNIT
RST34	$t_{su(BOOTMODE-PORz_OUT)}$	Setup time, BOOTMODE[7:0] before PORz_OUT high	3*S[(1)]		ns
RST35	$t_{h(PORz_OUT - BOOTMODE)}$	Hold time, BOOTMODE[7:0] after PORz_OUT high	0		ns

(1) S = MCU_OSC0_XI/XO clock period.

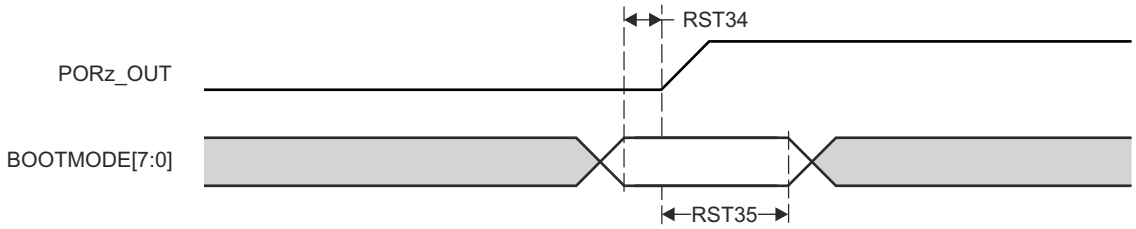

図 6-17. BOOTMODE Timing Requirements

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6.9.3.2 Safety Signal Timing

Tables and figures provided in this section define switching characteristics for MCU_SAFETY_ERRORn and SOC_SAFETY_ERRORn.

表 6-25. MCU_SAFETY_ERRORn Switching Characteristics

see 図 6-18

NO.	PARAMETER		MIN	MAX	UNIT
SFTY1	$t_{w(MCU_SAFETY_ERRORn)}$	Pulse width minimum, MCU_SAFETY_ERRORn active (PWM mode disabled)	P*R(1) (2)		ns
SFTY2	$t_{d\ (ERROR_CONDITION\text{-}MCU_SAFETY_ERRORnL)}$	Delay time, ERROR CONDITION to MCU_SAFETY_ERRORn active	50*P(1)		ns

(1) P = ESM functional clock (MCU_SYSCLK0 /6).
(2) R = Error Pin Counter Pre-Load Register count value.

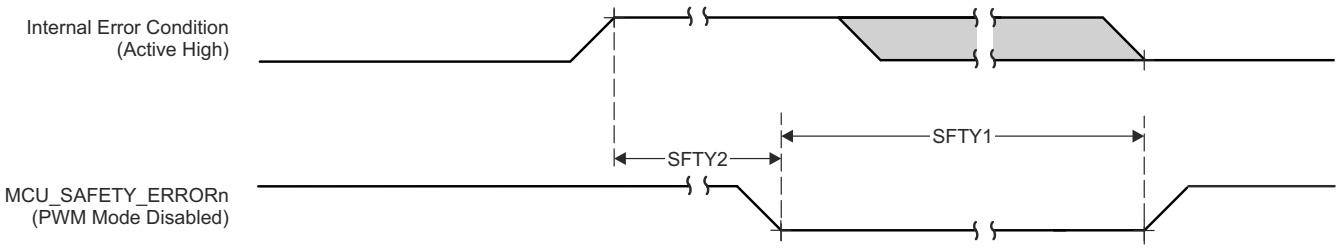

図 6-18. MCU_SAFETY_ERRORn Switching Characteristics

表 6-26. SOC_SAFETY_ERRORn Switching Characteristics

see 図 6-19

NO.	PARAMETER		MIN	MAX	UNIT
SFTY3	$t_{w(SOC_SAFETY_ERRORn)}$	Pulse width minimum,SOC_SAFETY_ERRORn active (PWM mode disabled)	P*R(1) (2)		ns
SFTY4	$t_{d\ (ERROR_CONDITION\text{-}SOC_SAFETY_ERRORnL)}$	Delay time, ERROR CONDITION to SOC_SAFETY_ERRORn active	50*P(1)		ns

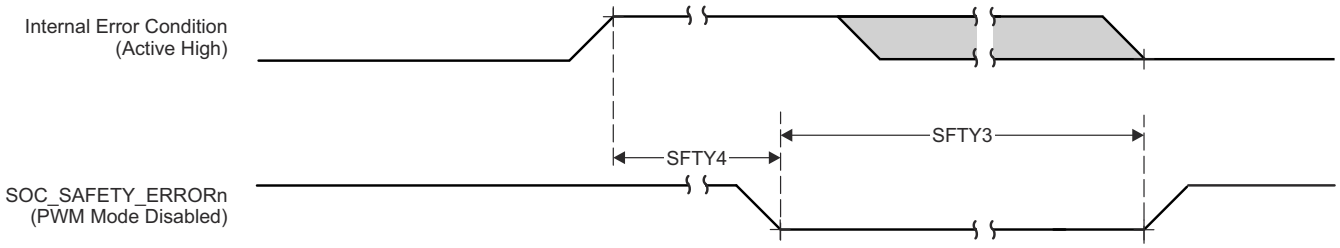

図 6-19. SOC_SAFETY_ERRORn Switching Characteristics

6.9.3.3 Clock Timing

Tables and figures provided in this section define timing requirements and switching characteristics for clock signals.

表 6-27. Clock Timng Requiements

see 図 6-20

NO.			MIN	MAX	UNIT
CLK1	$t_{c(EXT_REFCLK1)}$	Cycle time minimum, EXT_REFCLK1	10		ns
CLK2	$t_{w(EXT_REFCLK1H)}$	Pulse Duration minimum, EXT_REFCLK1 high	E*0.45(1)	E*0.55(1)	ns
CLK3	$t_{w(EXT_REFCLK1L)}$	Pulse Duration minimum, EXT_REFCLK1 low	E*0.45(1)	E*0.55(1)	ns

(1) E = EXT_REFCLK1 cycle time.

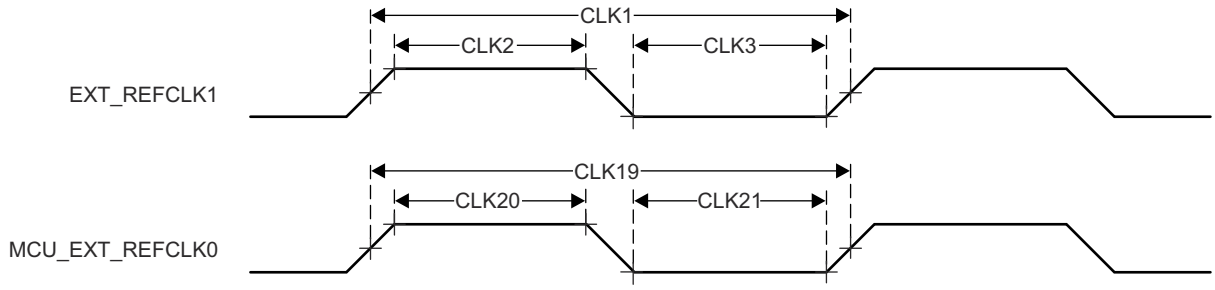

図 6-20. Clock Timing Requirements

表 6-28. Clock Switching Characteristics

see 図 6-21

NO.	PARAMETER		MIN	MAX	UNIT
CLK4	$t_{c(SYSCLKOUT0)}$	Cycle time minimum,SYSCLKOUT0	8		ns
CLK5	$t_{w(SYSCLKOUT0H)}$	Pulse Duration minimum, SYSCLKOUT0 high	A*0.4(1)	A*0.6(1)	ns
CLK6	$t_{w(SYSCLKOUT0L)}$	Pulse Duration minimum, SYSCLKOUT0 low	A*0.4(1)	A*0.6(1)	ns
CLK7	$t_{c(OBSCLK0)}$	Cycle time minimum, OBSCLK0	5		ns
CLK8	$t_{w(OBSCLK0H)}$	Pulse Duration minimum, OBSCLK0 high	B*0.4(2)	B*0.6(2)	ns
CLK9	$t_{w(OBSCLK0L)}$	Pulse Duration minimum,OBSCLK0 low	B*0.4(2)	B*0.6(2)	ns
CLK10	$t_{c(CLKOUT0)}$	Cycle time minimum, CLKOUT0	20		ns
CLK11	$t_{w(CLKOUT0H)}$	Pulse Duration minimum, CLKOUT0 high	C*0.4(3)	C*0.6(3)	ns
CLK12	$t_{w(CLKOUT0L)}$	Pulse Duration minimum,CLKOUT0 low	C*0.4(3)	C*0.6(3)	ns

(1) A = SYSCLKOUT0 cycle time.
(2) B = OBSCLK0 cycle time.
(3) C = CLKOUT0 cycle time.

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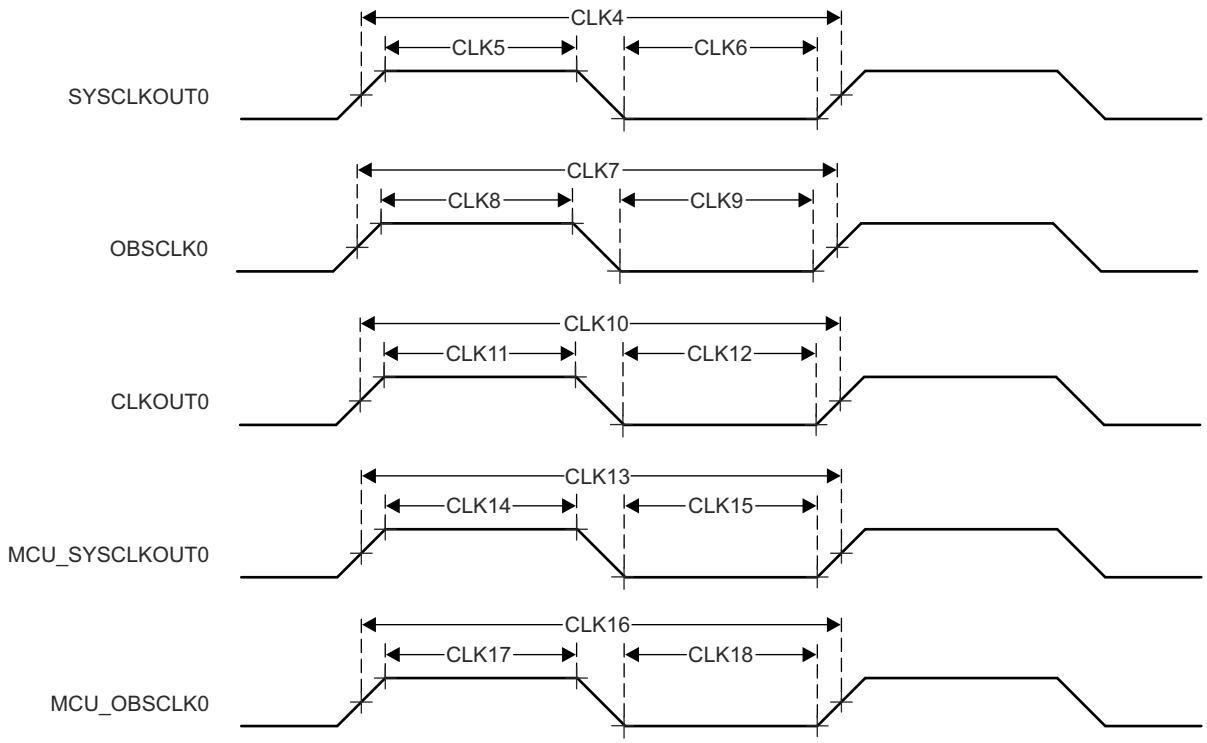

図 6-21. Clock Switching Characteristics

6.9.4 Clock Specifications

6.9.4.1 Input and Output Clocks / Oscillators

Various external clock inputs/outputs are needed to drive the device. Summary of these input clock signals is as follows:

- OSC1_XO/OSC1_XI — External main crystal interface pins connected to internal oscillator which sources reference clock and provides reference clock to PLLs within MAIN domain. Also, for audio applications, high-frequency oscillator 0 is used to provide audio clock frequencies to MCASPs.
- High frequency oscillators inputs
  - OSC1_XO/OSC1_XI — external main crystal interface pins connected to internal oscillator which sources reference clock. Provides reference clock to PLLs within MCU domain and MAIN domain. This high-frequency oscillator is used to provide audio clock frequencies to MCASPs.
  - WKUP_OSC0_XO/WKUP_OSC0_XI — external main crystal interface pins connected to internal oscillator which sources reference clock. Provides reference clock to PLLs within WKUP and MAIN domain.
- Low frequency oscillator input
  - WKUP_LFOSC_XO/WKUP_LFOSC_XI — external main crystal interface pins connected to internal oscillator which sources reference clock provides a clock for low power operation in deeper sleep modes.
- General purpose clock inputs
  - MCU_EXT_REFCLK0 — optional external. Provides system clock input (MCU domain).
  - EXT_REFCLK1 — optional external System clock input (MAIN domain). Optionally PLL2 (PER1) and MCASP can be sourced by EXT_REFCLK1 (sourced externally).
  - SERDES4_REFCLK_P/N — SerDes reference clock input for PCIe or Optional USB3 and SGMII interfaces.
  - PCIE_REFCLK[3:0]N/P — There are 4 differential clock input/output pins to support PCIe devices.
- External video pixel clock inputs
  - VOUT0_EXTPCLKIN — optional for the DPI0 port of DSS.
  - VOUT1_EXTPCLKIN — optional for the DPI1 port of DSS.

- External CPTS reference clock inputs
  - MCU_CPTS_RFT_CLK — CPTS reference clock inputs for MCU_CPTS_RFT_CLK.
  - CPTS_RFT_CLK — CPTS reference clock inputs for CPTS_RFT_CLK.
- External audio reference clock input/output pins
  - AUDIO_EXT_REFCLK0
  - AUDIO_EXT_REFCLK1
  - AUDIO_EXT_REFCLK2
  - AUDIO_EXT_REFCLK3

図 6-22 shows the external input clock sources and the output clocks to peripherals.

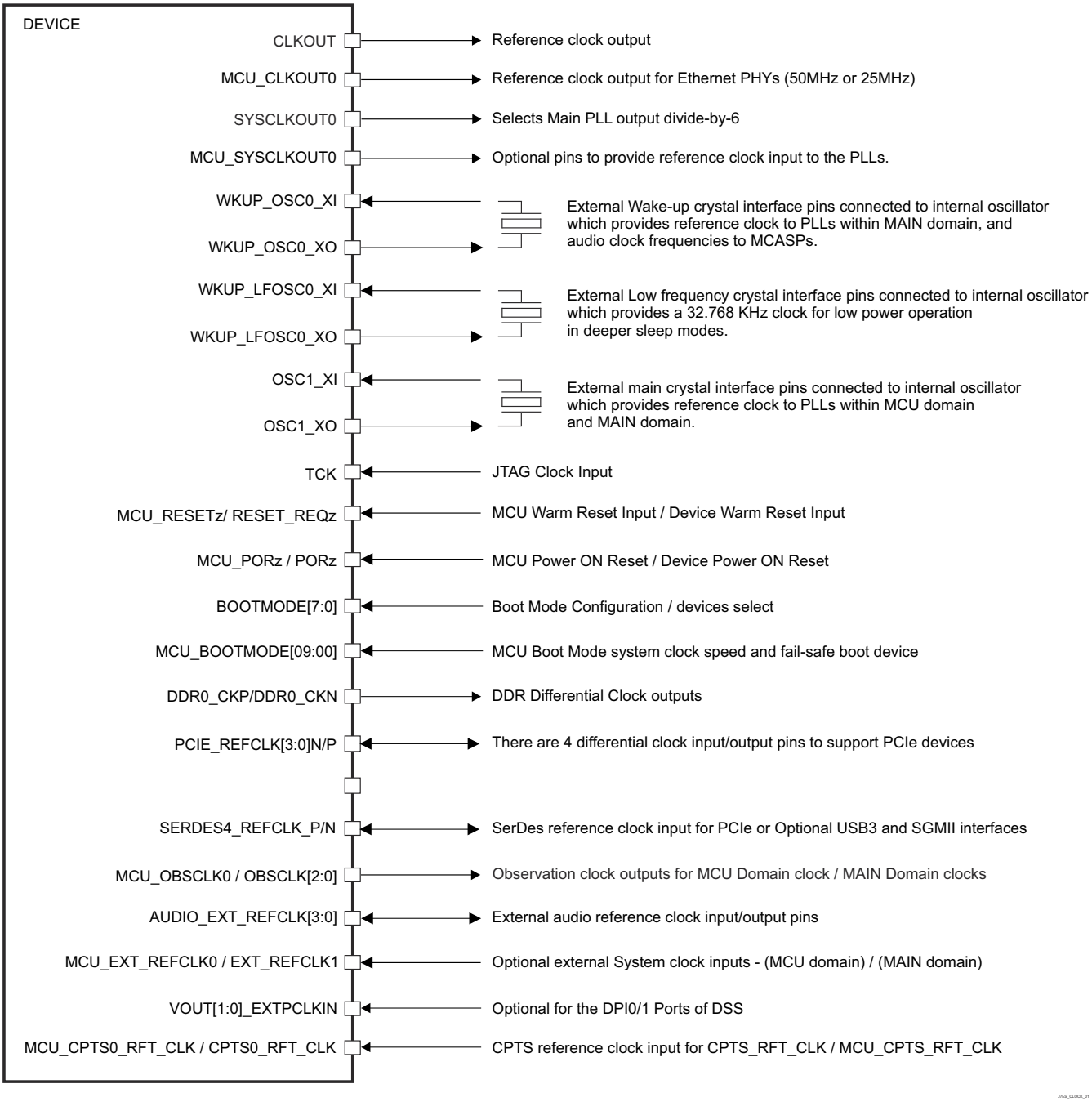

図 6-22. Input Clocks Interface

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For more information about Input clock interfaces, see *Clocking* section in *Device Configuration* chapter in the device TRM.

6.9.4.1.1 WKUP_OSC0 Internal Oscillator Clock Source

図 6-23 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit should be placed as close as possible to the WKUP_OSC0_XI and WKUP_OSC0_XO pins.

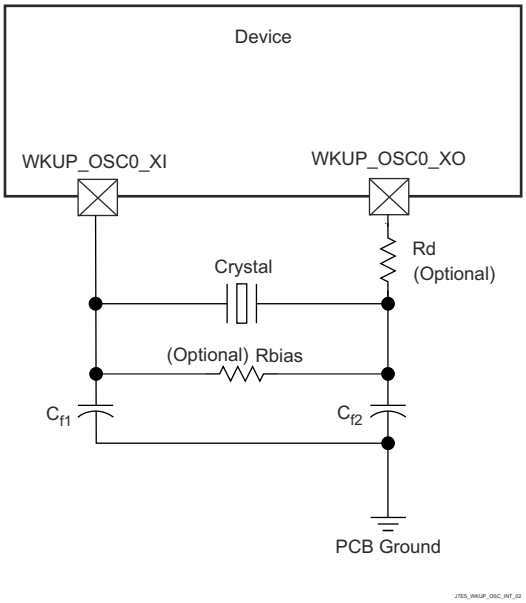

図 6-23. WKUP_OSC0 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. 表 6-29 summarizes the required electrical constraints.

表 6-29. WKUP_OSC0 Crystal Electrical Characteristics

PARAMETER				MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency				19.2, 20, 24, 25, 26, 27		MHz
F_{xtal}	Crystal Frequency Stability and Tolerance		Ethernet RGMII and RMII not used			±100	ppm
			Ethernet RGMII and RMII using derived clock			±50	
$C_{L1+PCBXI}$	Capacitance of C_{L1} + C_{PCBXI}			12		24	pF
$C_{L2+PCBXO}$	Capacitance of C_{L2} + C_{PCBXO}			12		24	pF
C_L	Crystal Load Capacitance			6		12	pF
C_{shunt}	Crystal Circuit Shunt Capacitance	ESR_{xtal} = 30 Ω	19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz			7	pF
		ESR_{xtal} = 40 Ω	19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz			5	pF
		ESR_{xtal} = 50 Ω	19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz			5	pF
		ESR_{xtal} = 60 Ω	19.2 MHz, 20 MHz, 24 MHz			5	pF
		ESR_{xtal} = 80 Ω	19.2 MHz, 20 MHz			5	pF
			25 MHz			3	pF
		ESR_{xtal} = 100 Ω	19.2 MHz, 20 MHz			3	pF

表 6-29. WKUP_OSC0 Crystal Electrical Characteristics (続き)

PARAMETER		MIN	TYP	MAX	UNIT
ESR_{xtal}	Crystal Effective Series Resistance			100	Ω

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

表 6-30 details the switching characteristics of the oscillator and the requirements of the input clock.

表 6-30. WKUP_OSC0 Switching Characteristics – Crystal Mode

PARAMETER		MIN	TYP	MAX	UNIT
C_{XI}	XI Capacitance			1.55	pF
C_{XO}	XO Capacitance			1.35	pF
C_{XIXO}	XI to XO Mutual Capacitance			0.1	pF
t_s	Maximum Start-up Time		9.5(1)		ms

(1) **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum startup and operation over temperature/voltage extremes.**

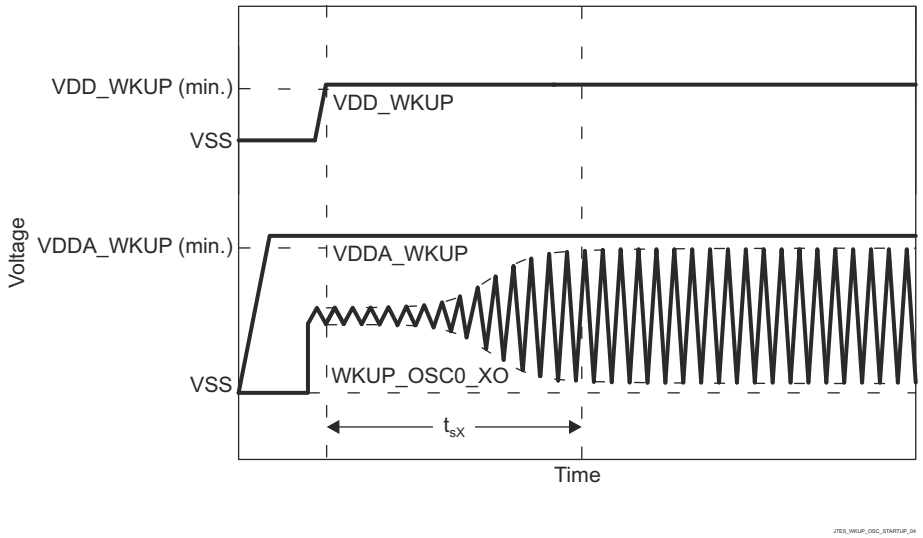

図 6-24. WKUP_OSC0 Start-up Time

6.9.4.1.1.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load, C_L, of this circuit is a combination of discrete capacitors C_{L1}, C_{L2}, and several parasitic contributions. PCB signal traces which connect crystal circuit components to WKUP_OSC0_XI and WKUP_OSC0_XO have parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where the PCB designer should be able to extract parasitic capacitance for each signal trace. The WKUP_OSC0 circuits and device package have combined parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where these parasitic capacitance values are defined in 表 6-30.

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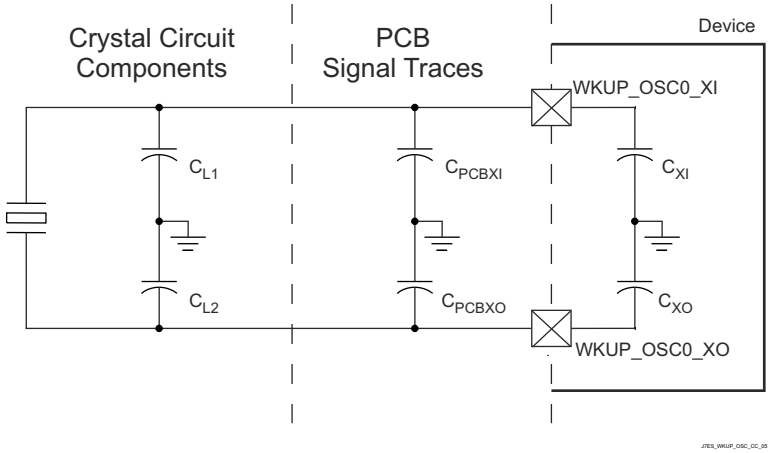

図 6-25. Load Capacitance

Load capacitors, C_{L1} and C_{L2} in 図 6-23, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer.

$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$

To determine the value of C_{L1} and C_{L2}, multiply the capacitive load value C_L by 2. Using this result, subtract the combined values of $C_{PCBXI} + C_{XI}$ to determine the value of C_{L1} and the combined values of $C_{PCBXO} + C_{XO}$ to determine the value of C_{L2}. For example, if C_L = 10 pF, C_{PCBXI} = 2.9 pF, C_{XI} = 0.5 pF, C_{PCBXO} = 3.7 pF, C_{XO} = 0.5 pF, the value of $C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 \times 10\text{ pF}) - 2.9\text{ pF} - 0.5\text{ pF})] = 16.6$ pF and $C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 \times 10\text{ pF}) - 3.7\text{ pF} - 0.5\text{ pF})] = 15.8$ pF

6.9.4.1.1.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for WKUP_OSC0 operating conditions defined in 表 6-29. Shunt capacitance, C_{shunt}, of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to WKUP_OSC0 have mutual parasitic capacitance to each other, $C_{PCBXIXO}$, where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance, C_{XIXO}, where this mutual parasitic capacitance value is defined in 表 6-30.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

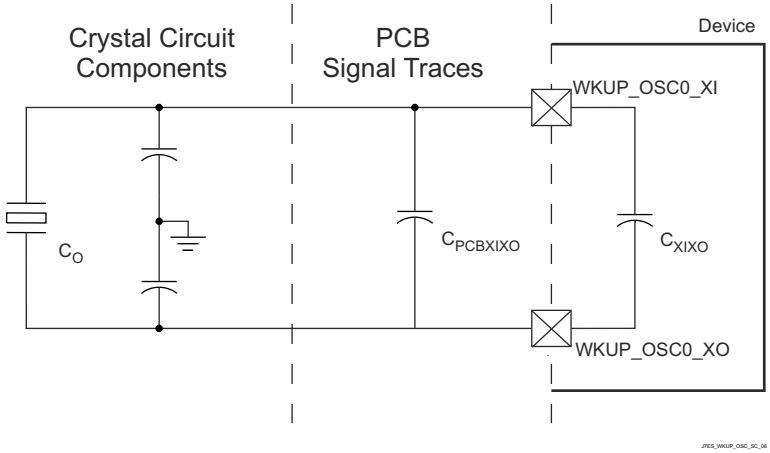

図 6-26. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied. C_O in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30 Ω, $C_{PCBXIXO}$ = 0.04 pF, C_{XIXO} = 0.01 pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

6.9.4.1.2 WKUP_OSC0 LVCMOS Digital Clock Source

図 6-27 shows the recommended oscillator connections when WKUP_OSC0_XI is connected to a 1.8-V LVCMOS square-wave digital clock source.

注

A DC steady-state condition is not allowed on WKUP_OSC0_XI when the oscillator is powered up. This is not allowed because WKUP_OSC0_XI is internally AC coupled to a comparator that may enter a unknown state when DC is applied to the input. Therefore, application software should power down WKUP_OSC0 any time WKUP_OSC0_XI is not toggling between logic states.

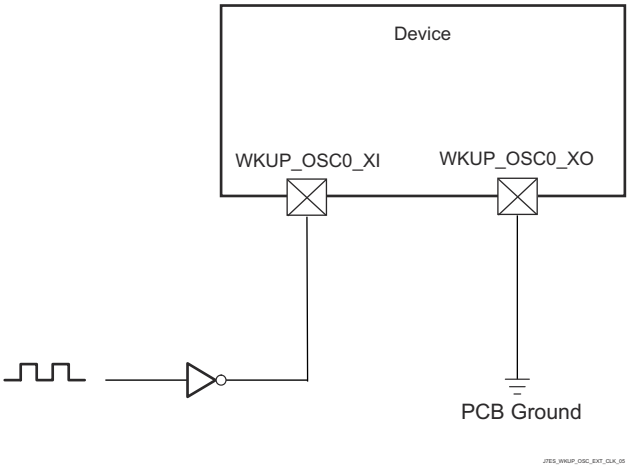

図 6-27. 1.8-V LVCMOS-Compatible Clock Input

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6.9.4.1.3 Auxiliary OSC1 Internal Oscillator Clock Source

図 6-28 shows the recommended crystal circuit. All discrete components used to implement the oscillator circuit should be placed as close as possible to the OSC1_XI and OSC1_XO pins.

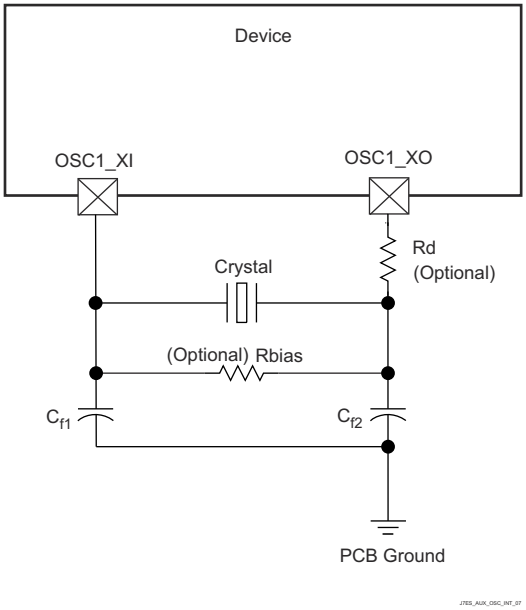

図 6-28. OSC1 Crystal Implementation

The crystal must be in the fundamental mode of operation and parallel resonant. 表 6-31 summarizes the required electrical constraints.

表 6-31. OSC1 Crystal Electrical Characteristics

PARAMETER				MIN	TYP	MAX	UNIT
F_{xtal}	Crystal Parallel Resonance Frequency			19.2		27	MHz
F_{xtal}	Crystal Frequency Stability and Tolerance		Ethernet RGMII and RMII not used			±100	ppm
			Ethernet RGMII and RMII using derived clock			±50	
$C_{L1+PCBXI}$	Capacitance of C_{L1} + C_{PCBXI}			12		24	pF
$C_{L2+PCBXO}$	Capacitance of C_{L2} + C_{PCBXO}			12		24	pF
C_L	Crystal Load Capacitance			6		12	pF
C_{shunt}	Crystal Circuit Shunt Capacitance	ESR_{xtal} = 30 Ω	19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz			7	pF
		ESR_{xtal} = 40 Ω	19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz			5	pF
		ESR_{xtal} = 50 Ω	19.2 MHz, 20 MHz, 24 MHz, 25 MHz, 26 MHz, 27 MHz			5	pF
		ESR_{xtal} = 60 Ω	19.2 MHz, 20 MHz, 24 MHz			5	pF
		ESR_{xtal} = 80 Ω	19.2 MHz, 20 MHz			5	pF
			25 MHz			3	pF
		ESR_{xtal} = 100 Ω	19.2 MHz, 20 MHz			3	pF
ESR_{xtal}	Crystal Effective Series Resistance					100	Ω

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

表 6-32 details the switching characteristics of the oscillator and the requirements of the input clock.

表 6-32. OSC1 Switching Characteristics – Crystal Mode

PARAMETER		MIN	TYP	MAX	UNIT
C_{XI}	XI Capacitance			1.55	pF
C_{XO}	XO Capacitance			1.35	pF
C_{XIXO}	XI to XO Mutual Capacitance			0.9	fF
t_s	Maximum Start-up Time		9.5[(1)]		ms

(1) **TI strongly encourages each customer to submit samples of the device to the resonator/crystal vendors for validation. The vendors are equipped to determine what load capacitors will best tune their resonator/crystal to the microcontroller device for optimum startup and operation over temperature/voltage extremes.**

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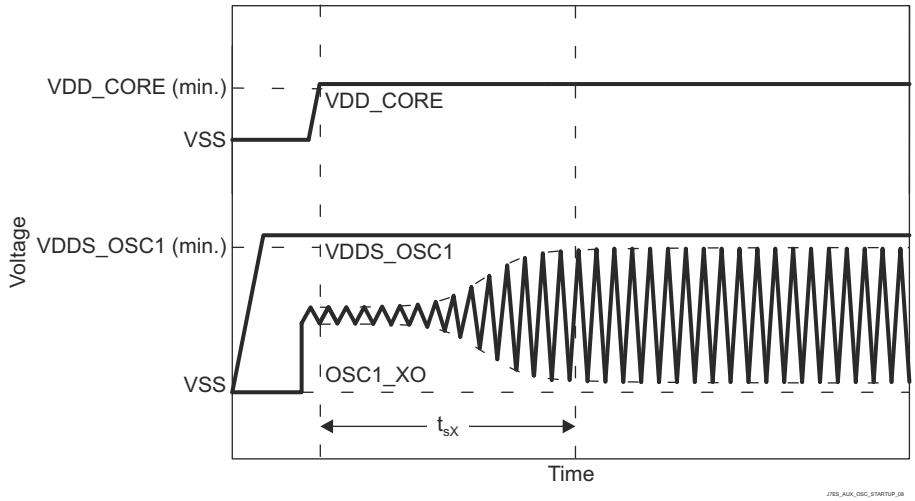

図 6-29. OSC1 Start-up Time

6.9.4.1.3.1 Load Capacitance

The crystal circuit must be designed such that it applies the appropriate capacitive load to the crystal, as defined by the crystal manufacturer. The capacitive load, C_L, of this circuit is a combination of discrete capacitors C_{L1}, C_{L2}, and several parasitic contributions. PCB signal traces which connect crystal circuit components to OSC1_XI and OSC1_XO have parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where the PCB designer should be able to extract parasitic capacitance for each signal trace. The OSC1 circuits and device package have combined parasitic capacitance to ground, C_{PCBXI} and C_{PCBXO}, where these parasitic capacitance values are defined in 表 6-32.

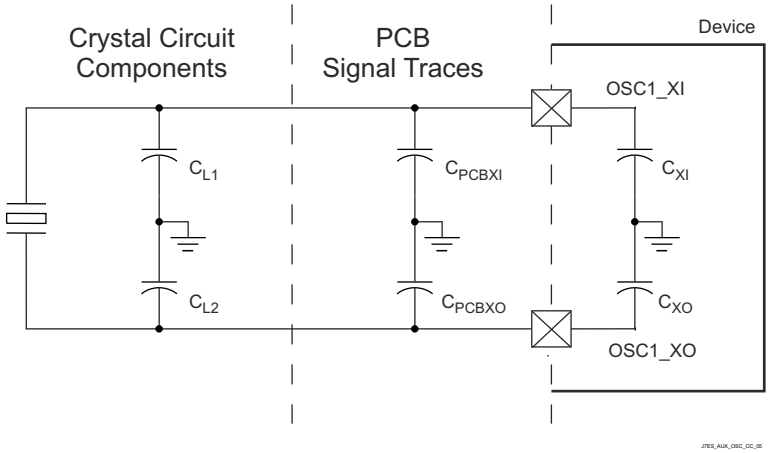

図 6-30. Load Capacitance

Load capacitors, C_{L1} and C_{L2} in 図 6-28, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer.

$$C_L = [(C_{L1} + C_{PCBXI} + C_{XI}) \times (C_{L2} + C_{PCBXO} + C_{XO})] / [(C_{L1} + C_{PCBXI} + C_{XI}) + (C_{L2} + C_{PCBXO} + C_{XO})]$$

To determine the value of C_{L1} and C_{L2}, multiply the capacitive load value C_L by 2. Using this result, subtract the combined values of C_{PCBXI} + C_{XI} to determine the value of C_{L1} and the combined values of C_{PCBXO} + C_{XO} to determine the value of C_{L2}. For example, if C_L = 10 pF, C_{PCBXI} = 2.9 pF, C_{XI} = 0.5 pF, C_{PCBXO} = 3.7 pF, C_{XO} = 0.5 pF, the value of C_{L1} = [(2C_L) - (C_{PCBXI} + C_{XI})] = [(2 × 10 pF) - 2.9 pF - 0.5 pF)] = 16.6 pF and C_{L2} = [(2C_L) - (C_{PCBXO} + C_{XO})] = [(2 × 10 pF) - 3.7 pF - 0.5 pF)] = 15.8 pF

6.9.4.1.3.2 Shunt Capacitance

The crystal circuit must also be designed such that it does not exceed the maximum shunt capacitance for OSC1 operating conditions defined in 表 6-31. Shunt capacitance, C_{shunt}, of the crystal circuit is a combination of crystal shunt capacitance and parasitic contributions. PCB signal traces which connect crystal circuit components to OSC1 have mutual parasitic capacitance to each other, $C_{PCBXIXO}$, where the PCB designer should be able to extract mutual parasitic capacitance between these signal traces. The device package also has mutual parasitic capacitance, C_{XIXO}, where this mutual parasitic capacitance value is defined in 表 6-32.

PCB routing should be designed to minimize mutual capacitance between XI and XO signal traces. This is typically done by keeping signal traces short and not routing them in close proximity. Mutual capacitance can also be minimized by placing a ground trace between these signals when the layout requires them to be routed in close proximity. It is important to minimize the mutual capacitance on the PCB to provide as much margin as possible when selecting a crystal.

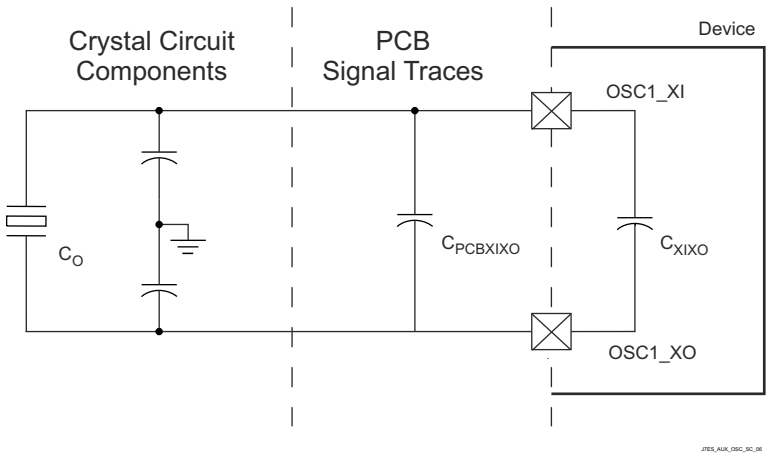

図 6-31. Shunt Capacitance

A crystal should be chosen such that the below equation is satisfied. C_O in the equation is the maximum shunt capacitance specified by the crystal manufacturer.

$C_{shunt} \geq C_O + C_{PCBXIXO} + C_{XIXO}$

For example, the equation would be satisfied when the crystal being used is 25 MHz with an ESR = 30 Ω, $C_{PCBXIXO}$ = 0.04 pF, C_{XIXO} = 0.01 pF, and shunt capacitance of the crystal is less than or equal to 6.95 pF.

6.9.4.1.4 Auxiliary OSC1 LVCMOS Digital Clock Source

図 6-32 shows the recommended oscillator connections when OSC1 is connected to a 1.8-V LVCMOS square-wave digital clock source.

注

A DC steady-state condition is not allowed on OSC1_XI when the oscillator is powered up. This is not allowed because OSC1_XI is internally AC coupled to a comparator that may enter a unknown state when DC is applied to the input. Therefore, application software should power down OSC1 any time OSC1_XI is not toggling between logic states.

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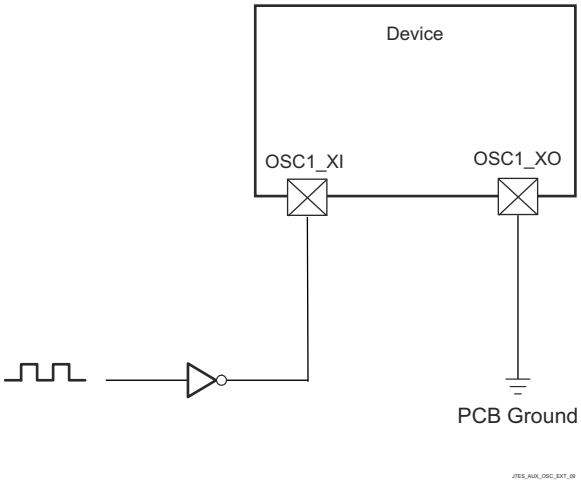

図 6-32. 1.8-V LVCMOS-Compatible Clock Input

6.9.4.1.5 Auxiliary OSC1 Not Used

図 6-33 shows the recommended oscillator connections when OSC1 is not used. OSC1_XI must be connected to VSS through an external pull resistor (R_{pd}) to ensure this input is held to a valid low level when unused since the internal pull-down resistor is disabled by default.

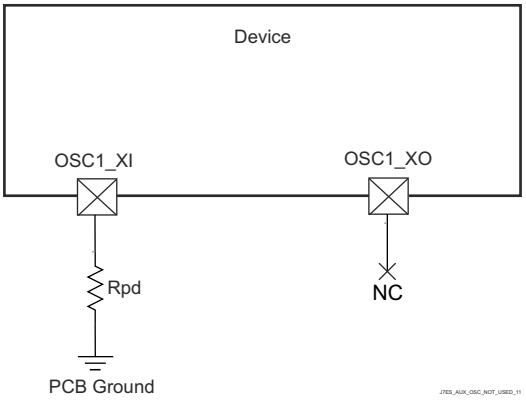

図 6-33. OSC1 Not Used

6.9.4.1.6 WKUP_LFOSC0 Internal Oscillator Clock Source

図 6-34 shows the recommended crystal circuit. It is recommended that preproduction printed-circuit board (PCB) designs include the two optional resistors R_{bias} and R_d in case they are required for proper oscillator operation when combined with production crystal circuit components. In most cases, R_{bias} is not required and R_d is a 0-Ω resistor. These resistors may be removed from production PCB designs after evaluating oscillator performance with production crystal circuit components installed on preproduction PCBs.

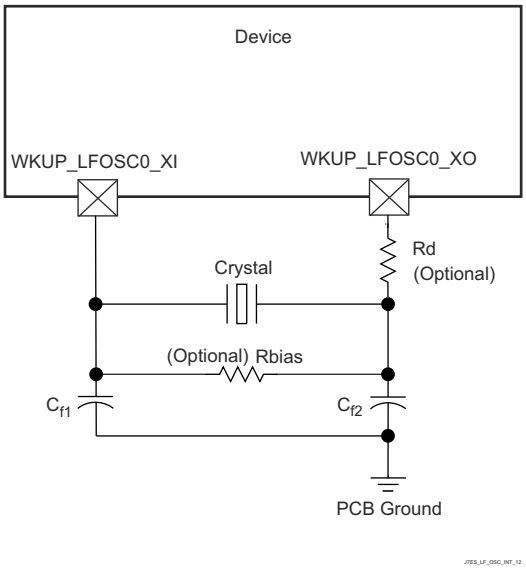

図 6-34. WKUP_LFOSC0 Crystal Implementation

表 6-33 presents LFXOSC modes of operation.

表 6-33. LFXOSC Modes of Operation

MODE	BP_C	PD_C	XI	XO	CLK_OUT	DESCRIPTION
ACTIVE	0	0	XTAL	XTAL	CLK_OUT	Active oscillator mode providing 32kHz
PWRDN	0	1	X	PD	LOW	Output will be pulled down to LOW. PAD to be tri-stated. Active mode disabled
BYPASS	1	0	CLK	PD	CLK	XI is driven by external clock source. XO is pulled down to LOW. Due to ESD diode to supply, XI should not be driven unless oscillator supply is present.

注

User should set CTRLMMR_WKUP_LFXOSC_TRIM[18:16] i_mult = 3b’001 for CL in the range 6pf to 9.5pf. CTRLMMR_WKUP_LFXOSC_TRIM [18:16] i_mult = 3b’010 for CL in the range 8.5pf to 12pf. Default setting is 3b’010.

注

The load capacitors, C_{f1} and C_{f2} in 図 6-35, should be chosen such that the below equation is satisfied. C_L in the equation is the load specified by the crystal manufacturer. All discrete components used to implement the oscillator circuit should be placed as close as possible to the associated oscillator WKUP_LFOSC0_XI, WKUP_LFOSC0_XO, and VSS pins.

$$C_L = \frac{C_{f1} C_{f2}}{(C_{f1} + C_{f2})}$$

図 6-35. Load Capacitance Equation

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The crystal must be in the fundamental mode of operation and parallel resonant. 表 6-34 summarizes the required electrical constraints.

表 6-34. WKUP_LFOSC0 Crystal Electrical Characteristics

NAME	DESCRIPTION		MIN	TYP	MAX	UNIT
f_p	Parallel resonance crystal frequency			32768		Hz
C_{f1}	C_{f1} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12		24	pF
C_{f2}	C_{f2} load capacitance for crystal parallel resonance with $C_{f1} = C_{f2}$		12		24	pF
C_{shunt}	Shunt capacitance	ESRxtal – 40 Ω			4	pF
		ESRxtal – 60 Ω			3	pF
		ESRxtal – 80 Ω			2	pF
		ESRxtal – 100 Ω			1	pF
ESR	Crystal effective series resistance				100	kΩ

When selecting a crystal, the system design must consider the temperature and aging characteristics of a based on the worst case environment and expected life expectancy of the system.

表 6-35 details the switching characteristics of the oscillator and the requirements of the input clock.

表 6-35. WKUP_LFOSC0 Switching Characteristics – Crystal Mode

NAME	DESCRIPTION	MIN	TYP	MAX	UNIT
f_{xtal}	Oscillation frequency		32768		Hz
t_{sX}	Start-up time			96.5	ms

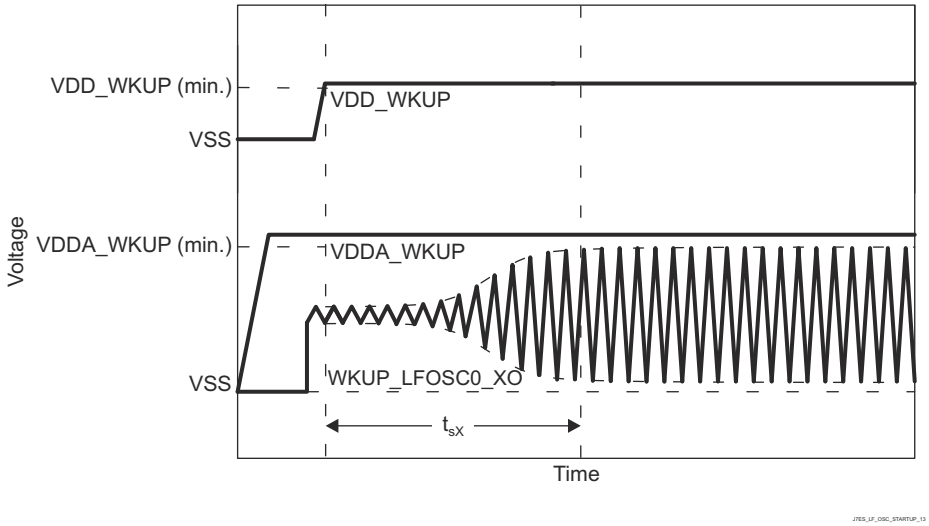

図 6-36. WKUP_LFOSC0 Start-up Time

6.9.4.1.7 WKUP_LFOSC0 Not Used

図 6-37 shows the recommended oscillator connections when WKUP_LFOSC0 is not used. WKUP_LFOSC0 may be a no-connect while the oscillator remains disabled since the internal pull-down resistor is enabled by default.

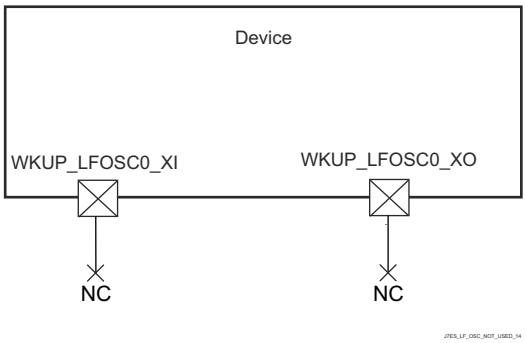

図 6-37. WKUP_LFOSC0 Not Used

6.9.4.2 Output Clocks

The device provides several system clock outputs. Summary of these output clocks are as follows:

- **MCU_CLKOUT0**
  - Reference clock output for Ethernet PHYs (50 MHz or 25 MHz)
- **MCU_SYSCLKOUT0**
  - SYSCLK0 of WKUP_PLLCTRL0 is divided by 6 and then sent out of the device as a LVCMOS clock signal (MCU_SYSCLKOUT0). This signal can be used to test if the main chip clock is functioning or not.
- **MCU_OBSCLK0**
  - On the clock output MCU_OBSCLK0, oscillators and PLLs clocks can be observed for tests and debug.
- **SYSCLKOUT0**
  - SYSCLK0 from the MAIN_PLL controller is divided by 6 and then sent out of the device as a LVCMOS clock signal (SYSCLKOUT0). This signal can be used to test if the main chip clock is functioning or not.
- **CLKOUT**
  - Reference clock output
- **OBSCLK[2:0]**
  - On the clock output OBSCLK0, oscillators and PLLs clocks can be observed for tests and debug.

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6.9.4.3 PLLs

Power is supplied to the Phase-Locked Loop circuitries (PLLs) by internal regulators that derive power from the off-chip power-supply.

There are total of three PLLs in the device in WKUP and MCU domains:

- MCU_PLL0 (MCU R5FSS PLL) with WKUP_PLLCTRL0
- MCU_PLL1 (MCU PERIPHERAL PLL)
- MCU_PLL2 (MCU CPSW PLL)

There are total of twenty PLLs in the device in MAIN domain:

- PLL0 (MAIN PLL) with PLLCTRL0
- PLL1 (PER0 PLL)
- PLL2 (PER1 PLL)
- PLL3 (CPSW9G PLL)
- PLL4 (AUDIO0 PLL)
- PLL5 (VIDEO PLL)
- PLL6 (GPU PLL)
- PLL7 (C7x PLL)
- PLL8 (ARM0 PLL)
- PLL12 (DDR PLL)
- PLL13 (C66 PLL)
- PLL14 (R5F PLL)
- PLL15 (AUDIO1 PLL)
- PLL16 (DSS PLL0)
- PLL17 (DSS PLL1)
- PLL18 (DSS PLL2)
- PLL19 (DSS PLL3)
- PLL23 (DSS PLL7)
- PLL24 (MLB PLL)
- PLL25 (VISION PLL)

注

For more information, see:

- *Device Configuration* / *Clocking* / *PLLs* section in the device TRM.
- *Peripherals* / *Display Subsystem* Overview section in the device TRM.

注

The input reference clock (OSC1_XI/OSC1_XO) is specified and the lock time is ensured by the PLL controller, as documented in the *Device Configuration* chapter in the device TRM.

6.9.4.4 Module and Peripheral Clocks Frequencies

セクション 6.9.5, *Peripherals* section documents the maximum frequency associated with the peripheral clocks of the device.

For more details on the clocking structure of each module, reference *Device Configurations* chapter in the device TRM.

6.9.5 Peripherals

6.9.5.1 ATL

The device contains ATL module that can be used for asynchronous sample rate conversion of audio. The ATL calculates the error between two time bases, such as audio syncs, and optionally generates an averaged clock using cycle stealing via software.

注

For more information about ATL, see *Audio Tracking Logic (ATL)* section in *Peripherals* chapter in the device TRM.

表 6-36 represents ATL timing conditions.

表 6-36. ATL Timing Conditions

PARAMETER		MODE	MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	External reference CLK	0.5	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	Internal reference CLK	1	10	pF

セクション 6.9.5.1.1, セクション 6.9.5.1.2, セクション 6.9.5.1.3, and セクション 6.9.5.1.4 present timing requirements and switching characteristics for ATL.

6.9.5.1.1 ATL_PCLK Timing Requirements

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D1	$t_{c(pclk)}$	Cycle time, ATL_PCLK	External reference CLK	5		ns
D2	$t_{w(pclkL)}$	Pulse Duration, ATL_PCLK low	External reference CLK	0.45 × M[(1)] + 2.5		ns
D3	$t_{w(pclkH)}$	Pulse Duration, ATL_PCLK high	External reference CLK	0.45 × M[(1)] + 2.5		ns

(1) M = ATL_CLK[x] period

6.9.5.1.2 ATL_AWS[x] Timing Requirements

NO.			MODE	MIN	MAX	UNIT
D4	$t_{c(aws)}$	Cycle Time, ATL_AWS[x][(3)]	External reference CLK	2 × M[(1)]		ns
D5	$t_{w(awsL)}$	Pulse Duration, ATL_AWS[x][(3)] low	External reference CLK	0.45 × A[(2)] + 2.5		ns
D6	$t_{w(awsH)}$	Pulse Duration, ATL_AWS[x][(3)] high	External reference CLK	0.45 × A[(2)] + 2.5		ns

(1) M = ATL_CLK[x] period
(2) A = ATL_AWS[x] period
(3) x = 0 to 3

6.9.5.1.3 ATL_BWS[x] Timing Requirements

NO.			MODE	MIN	MAX	UNIT
D7	$t_{c(bws)}$	Cycle Time, ATL_BWS[x][(3)]	External reference clock	2 × M[(1)]		ns
D8	$t_{w(bwsL)}$	Pulse Duration, ATL_BWS[x] low[(3)]	External reference clock	0.45 × B[(2)] + 2.5		ns

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NO.			MODE	MIN	MAX	UNIT
D9	$t_{w(bwsH)}$	Pulse Duration, ATL_BWS[x] high[3]	External reference clock	0.45 × B[2] + 2.5		ns

(1) M = ATL_CLK[x] period
(2) B = ATL_BWS[x] period
(3) x = 0 to 3

6.9.5.1.4 ATCLK[x] Switching Characteristics

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D10	$t_{c(atclk)}$	Cycle time, ATCLK[x][3]	Internal reference CLK	20		ns
D11	$t_{w(atclkL)}$	Pulse Duration, ATCLK[x] low[3]	Internal reference CLK	0.45 × P[2] - M[1] - 0.3		ns
D12	$t_{w(atclkH)}$	Pulse Duration, ATCLK[x] high[3]	Internal reference CLK	0.45 × P[2] - M[1] - 0.3		ns

(1) M = ATL_CLK[x] period
(2) P = ATCLK[x] period
(3) x = 0 to 3

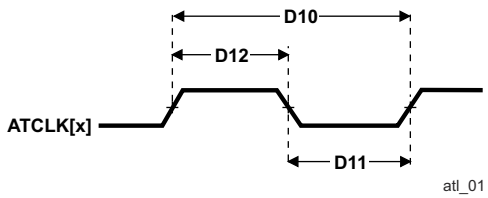

図 6-38. ATCLK[x] Timing

6.9.5.2 VPFE

表 6-37 represents VPFE timnig conditions.

表 6-37. VPFE Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1.3	2.64	V/ns
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		50	ps

表 6-38, 図 6-39, and 図 6-40 represent timing requirements for VPFE0.

表 6-38. Timing Requirements for VPFE0

NO.(1)			MIN	MAX	UNIT
V1	$t_{c(pclk)}$	Cycle time, VPFE0_PCLK	6.06(1)		ns
V2	$t_{w(pclkH)}$	Pulse duration, VPFE0_PCLK high	0.45 × P(2)		ns
V3	$t_{w(pclkL)}$	Pulse duration, VPFE0_PCLK low	0.45 × P(2)		ns
V4	$t_{su(ctrlV\text{-}pclkV)}$	Setup time, control signals (VPFE0_HD, VPFE0_VD, VPFE0_WEN, VPFE0_FIELD) valid before VPFE0_PCLK transition	2.12		ns
V5	$t_{su(dataV\text{-}pclkV)}$	Setup time, VPFE0_DATA[15:0] valid before VPFE0_PCLK transition	2.38		ns
V6	$t_{h(pclkV\text{-}ctrlV/dataV)}$	Hold time, control signals (VPFE0_HD, VPFE0_VD, VPFE0_WEN, VPFE0_FIELD) and VPFE0_DATA[15:0] valid after VPFE0_PCLK transition	-0.05		ns

(1) For maximum frequency of 165 MHz.
(2) P = VPFE0_PCLK period.

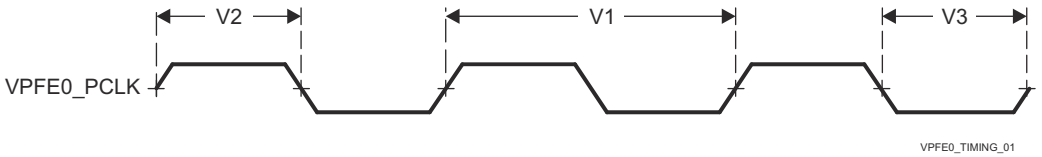

図 6-39. VPFE0 Clock Signal Requirement

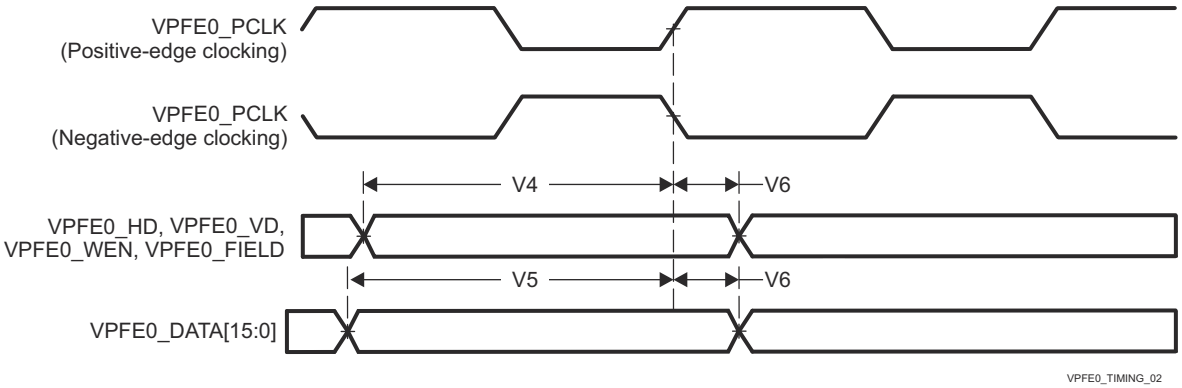

図 6-40. VPFE0 Timing Requirements

For more information, see *Video Processing Front End (VPFE)* section in *Peripherals* chapter in the device TRM.

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6.9.5.3 CPSW2G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding sections within , セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

6.9.5.3.1 CPSW2G MDIO Interface Timings

表 6-39 represents CPSW2G timing conditions.

表 6-39. CPSW2G MDIO Timing Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input signal slew rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	10	470	pF

表 6-40, 表 6-41, and 図 6-41 present timing requirements for MDIO.

表 6-40. CPSW2G MDIO Timing Requirements

NO.			MIN	MAX	UNIT
MDIO1	$t_{su(mdioV-mdcH)}$	Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high	90		ns
MDIO2	$t_{h(mdcH-mdioV)}$	Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high	0		ns

表 6-41. CPSW2G MDIO Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
MDIO3	$t_{c(mdc)}$	Cycle time, MDIO[x]_MDC	400		ns
MDIO4	$t_{w(mdcH)}$	Pulse Duration, MDIO[x]_MDC high	160		ns
MDIO5	$t_{w(mdcL)}$	Pulse Duration, MDIO[x]_MDC low	160		ns
MDIO7	$t_{d(mdcL-mdioV)}$	Delay time, MDIO[x]_MDC low to MDIO[x]_MDIO valid	-150	150	ns

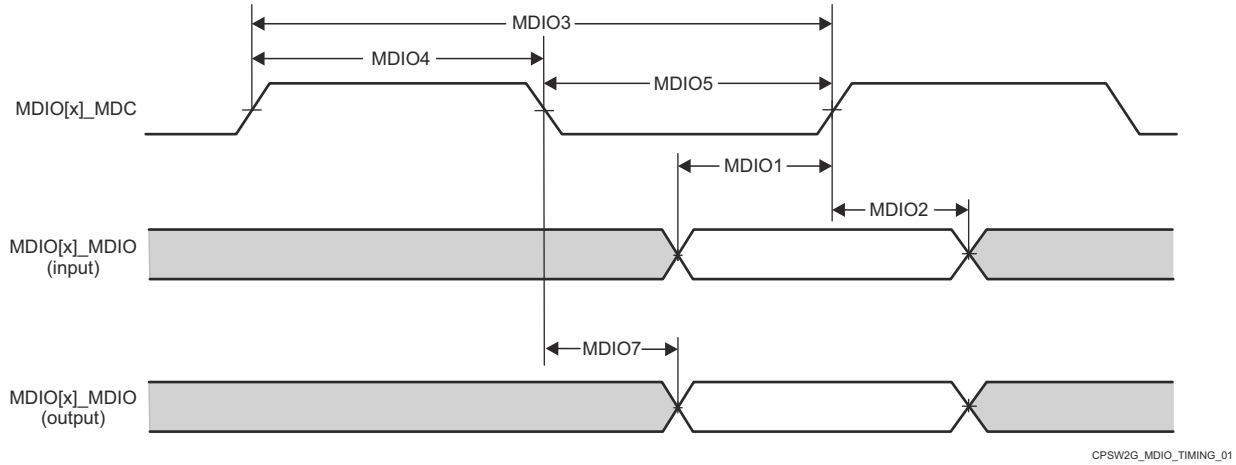


図 6-41. CPSW2G MDIO Timing Requirements and Switching Characteristics

注

x = 0 in MCU domain

6.9.5.3.2 CPSW2G RMII Timings

表 6-42, セクション 6.9.5.3.2.1, セクション 6.9.5.3.2.2, and セクション 6.9.5.3.2.3 present timing conditions, requirements, and switching characteristics for CPSW2G RMII.

表 6-42. CPSW2G RMII Timing Conditions

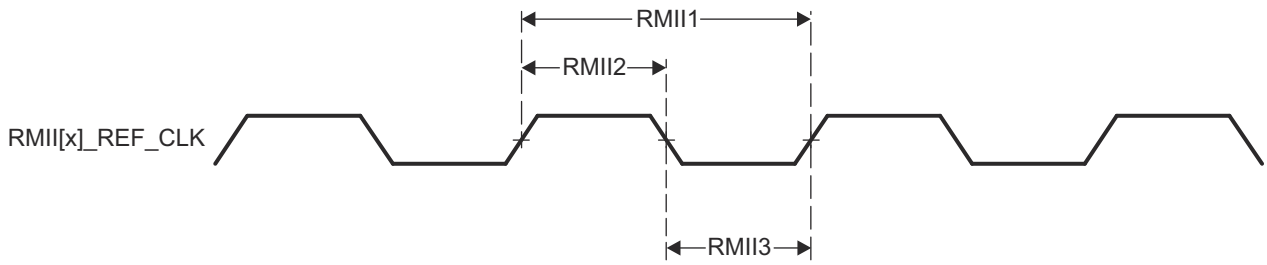
PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input signal slew rate	VDDSHVx(1) = 1.8V	0.2	0.54	V/ns
		VDDSHVx(1) = 3.3V	0.8	1.2	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		3	25	pF

(1) x = 0 - 5, where x indicates the respective IO power rail. Refer to *Pin Attributes* for more information on IO power rail assinments.

6.9.5.3.2.1 CPSW2G RMII[x]_REF_CLK Timing Requirements – RMII Mode

see 図 6-42

NO.			MIN	MAX	UNIT
RMII1	$t_{c(ref_clk)}$	Cycle time, RMII[x]_REF_CLK	19.999	20.001	ns
RMII2	$t_{w(ref_clkH)}$	Pulse Duration, RMII[x]_REF_CLK high	7	13	ns
RMII3	$t_{w(ref_clkL)}$	Pulse Duration, RMII[x]_REF_CLK low	7	13	ns



A. x = 1 in MCU domain.

図 6-42. CPSW2G RMII[x]_REFCLK Timing Requirements – RMII Mode

6.9.5.3.2.2 CPSW2G RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RX_ER Timing Requirements – RMII Mode

NO.			MIN	MAX	UNIT
RMII4	$t_{su(rxdV\text{-}ref_clkH)}$	Setup time, RMII[x]_RXD[1:0] valid before RMII[x]_REF_CLK rising edge	4		ns
	$t_{su(crs_dvV\text{-}ref_clkH)}$	Setup time, RMII[x]_CRS_DV valid before RMII[x]_REF_CLK rising edge	4		ns
	$t_{su(rx_erV\text{-}ref_clkH)}$	Setup time, RMII[x]_RX_ER valid before RMII[x]_REF_CLK rising edge	4		ns
RMII5	$t_{h(ref_clkH\text{-}rxdV)}$	Hold time, RMII[x]_RXD[1:0] valid after RMII[x]_REF_CLK rising edge	2		ns
	$t_{h(ref_clkH\text{-}crs_dvV)}$	Hold time, RMII[x]_CRS_DV valid after RMII[x]_REF_CLK rising edge	2		ns
	$t_{h(ref_clkH\text{-}rx_erV)}$	Hold time, RMII[x]_RX_ER valid after RMII[x]_REF_CLK rising edge	2		ns

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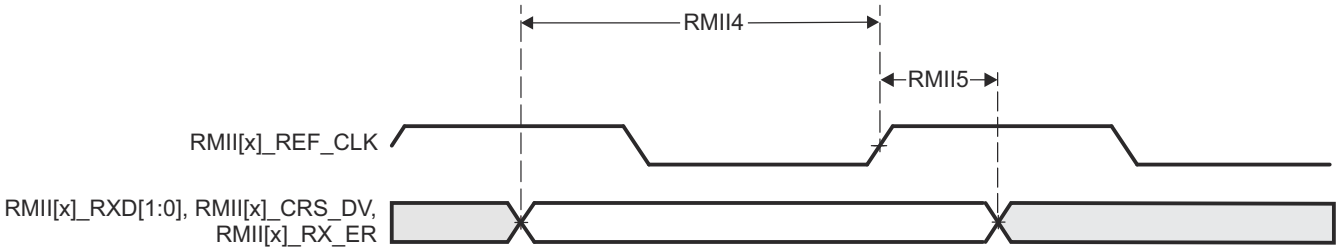


図 6-43. CPSW2G RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RX_ER Timing Requirements – RMII Mode

セクション 6.9.5.3.2.3, and 図 6-44 present switching characteristics for CPSW2G RMII Transmit.

6.9.5.3.2.3 CPSW2G RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

see 図 6-44

NO.	PARAMETER		MIN	MAX	UNIT
RMII6	$t_{d(ref_clkH-txdV)}$	Delay time, RMII[x]_REF_CLK rising edge to RMII[x]_TXD[1:0] valid	2	13	ns
	$t_{d(ref_clkH-tx_enV)}$	Delay time, RMII[x]_REF_CLK rising edge to RMII[x]_TX_EN valid	2	13	ns

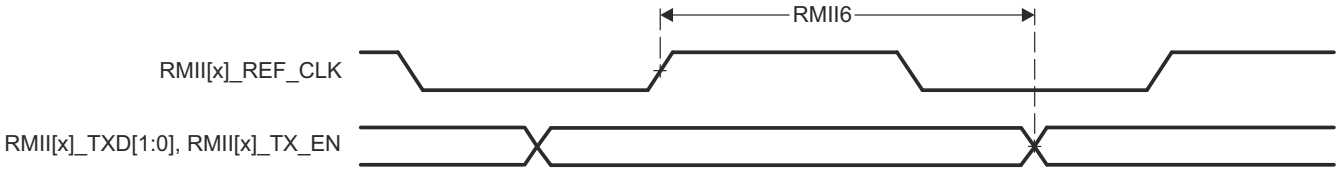


図 6-44. RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

6.9.5.3.3 CPSW2G RGMII Timings

セクション 6.9.5.3.3.1, セクション 6.9.5.3.3.2, and 図 6-46 present timing requirements for receive RGMII operation.

For more information, see *Gigabit Ethernet MAC (MCU_CPSW0)* section in *Peripherals* chapter in the device TRM.

表 6-43. CPSW2G RGMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		2.64	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC, RGMII[x]_TD[3:0], RGMII[x]_TX_CTL		50	ps

6.9.5.3.3.1 RGMII[x]_RXC Timing Requirements – RGMII Mode

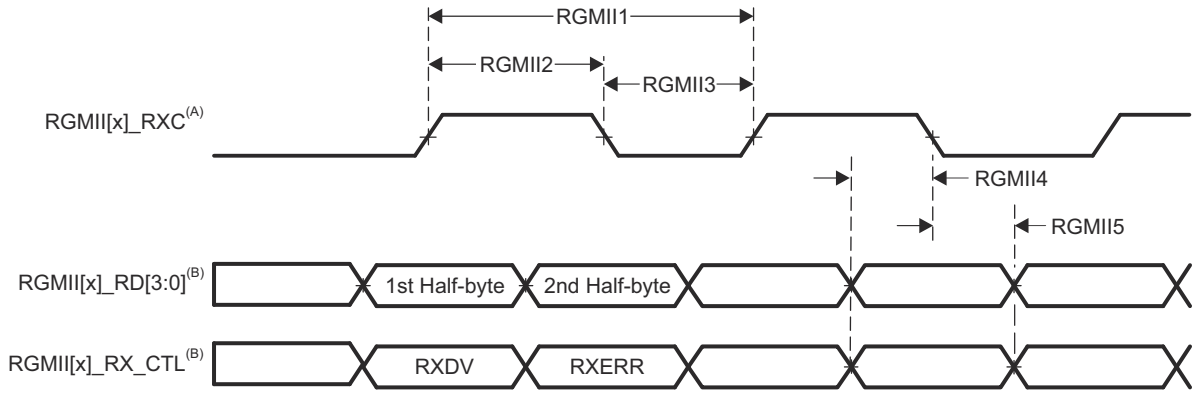
see 図 6-45

NO.			MODE	MIN	MAX	UNIT
RGMII1	$t_{c(rxc)}$	Cycle time, RGMII[x]_RXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII2	$t_{w(rxcH)}$	Pulse duration, RGMII[x]_RXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII3	$t_{w(rxcL)}$	Pulse duration, RGMII[x]_RXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

6.9.5.3.3.2 CPSW2G Timing Requirements for RGMII[x]_RD[3:0], and RGMII[x]_RCTL – RGMII Mode

see 図 6-45

NO.			MODE	MIN	MAX	UNIT
RGMII4	$t_{su(rdV-rxcV)}$	Setup time, RGMII[x]_RD[3:0] valid before RGMII[x]_RXC transition	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{su(rx_ctlV-rxcV)}$	Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC transition	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
RGMII5	$t_{h(rxcV-rdV)}$	Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC transition	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{h(rxcV-rx_ctlV)}$	Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC transition	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns



A. RGMII_RXC must be externally delayed relative to the data and control pins.
B. Data and control information is received using both edges of the clocks. RGMII_RXD[3:0] carries data bits 3-0 on the rising edge of RGMII_RXC and data bits 7-4 on the falling edge of RGMII_RXC. Similarly, RGMII_RXCTL carries RXDV on rising edge of RGMII_RXC and RXERR on falling edge of RGMII_RXC.

図 6-45. CPSW2G Receive Interface Timing, RGMII Operation

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セクション 6.9.5.3.3.3, セクション 6.9.5.3.3.4 present switching characteristics for transmit - RGMII for 10 Mbps, 100 Mbps, and 1000 Mbps.

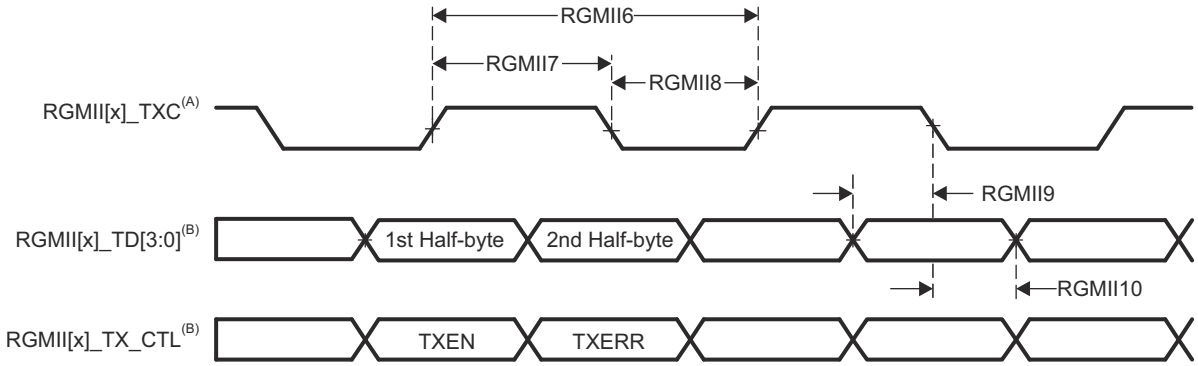
6.9.5.3.3.3 CPSW2G RGMII[x]_TXC Switching Characteristics – RGMII Mode

NO.	PARAMETER		MODE	MIN	MAX	UNIT
RGMII6	$t_{c(txc)}$	Cycle time, RGMII[x]_TXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII7	$t_{w(txcH)}$	Pulse duration, RGMII[x]_TXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII8	$t_{w(txcL)}$	Pulse duration, RGMII[x]_TXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

6.9.5.3.3.4 RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics – RGMII Mode

see 図 6-46

NO.	PARAMETER		MODE	MIN	MAX	UNIT
RGMII9	$t_{osu(tdV-txcV)}$	Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC transition	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.05		ns
	$t_{osu(tx_ctlV-txcV)}$	Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC transition	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.05		ns
RGMII10	$t_{oh(tdV-txcV)}$	Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC transition	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.05		ns
	$t_{oh(tx_ctlV-txcV)}$	Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC transition	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.05		ns



A. TXC is delayed internally before being driven to the RGMII[x]_TXC pin. This internal delay is always enabled.
B. Data and control information is received using both edges of the clocks. RGMII_TD[3:0] carries data bits 3-0 on the rising edge of RGMII_TXC and data bits 7-4 on the falling edge of RGMII_TXC. Similarly, RGMII_TX_CTL carries TXDV on rising edge of RGMII_TXC and RTXERR on falling edge of RGMII_TXC.

図 6-46. CPSW2G Transmit Interface Timing RGMII Mode

6.9.5.4 CPSW9G

For more details about features and additional description information on the device Gigabit Ethernet MAC, see the corresponding sections within , セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

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表 6-44 represents CPSW9G timing conditions.

表 6-44. CPSW9G Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input signal slew rate	0.9	3.6	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	10	470	pF

6.9.5.4.1 CPSW9G MDIO Interface Timings

表 6-45, 表 6-46, and 図 6-47 present timing requirements and switching characteristics for MDIO.

表 6-45. CPSW9G MDIO Timing Requirements

NO.	PARAMETER(1)		MIN	MAX	UNIT
MDIO1	$t_{su(mdioV-mdcH)}$	Setup time, MDIO[x]_MDIO valid before MDIO[x]_MDC high	90		ns
MDIO2	$t_{h(mdcH-mdioV)}$	Hold time, MDIO[x]_MDIO valid after MDIO[x]_MDC high	0		ns

表 6-46. CPSW9G MDIO Switching Characteristics

NO.	PARAMETER(1)		MIN	MAX	UNIT
MDIO3	$t_{c(mdc)}$	Cycle time, MDIO[x]_MDC	400		ns
MDIO4	$t_{w(mdcH)}$	Pulse Duration, MDIO[x]_MDC high	160		ns
MDIO5	$t_{w(mdcL)}$	Pulse Duration, MDIO[x]_MDC low	160		ns
MDIO7	$t_{d(mdcL-mdioV)}$	Delay time, MDIO[x]_MDC falling edge to MDIO[x]_MDIO valid	-150	150	ns

(1) x = 0

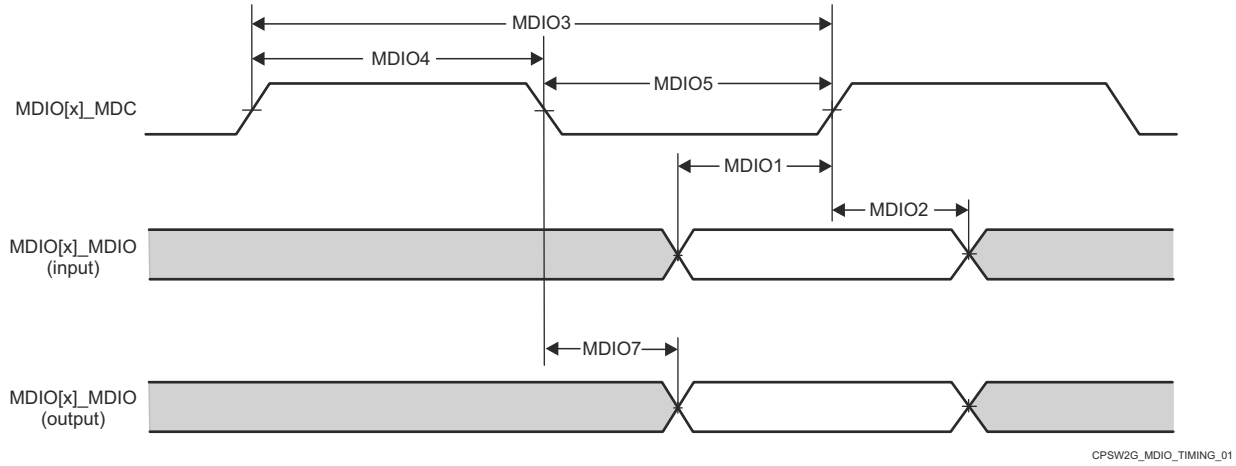

図 6-47. CPSW9G MDIO Diagrams Receive and Transmit

6.9.5.4.2 CPSW9G RMII Timings

表 6-47, セクション 6.9.5.4.2.1, セクション 6.9.5.4.2.2, and 図 6-48 present timing requirements for CPSW9G RMII receive.

表 6-47. CPSW9G RMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	VDDSHVx(1) = 1.8V	0.108	0.54	V/ns
		VDDSHVx(1) = 3.3V	0.4	1.2	V/ns

表 6-47. CPSW9G RMII Timing Conditions (続き)

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output load capacitance	3	25	pF

(1) x = 0 - 5, where x indicates the respective IO power rail. Refer to *Pin Attributes* for more information on IO power rail assinments.

6.9.5.4.2.1 RMII[x]_REF_CLK Timing Requirements – RMII Mode

see 図 6-48

NO.			MIN	TYP	MAX	UNIT
RMII1	$t_{c(ref_clk)}$	Cycle time, RMII[x]_REF_CLK	19.999		20.001	ns
RMII2	$t_{w(ref_clkH)}$	Pulse Duration, RMII[x]_REF_CLK high	7		13	ns
RMII3	$t_{w(ref_clkL)}$	Pulse Duration, RMII[x]_REF_CLK low	7		13	ns

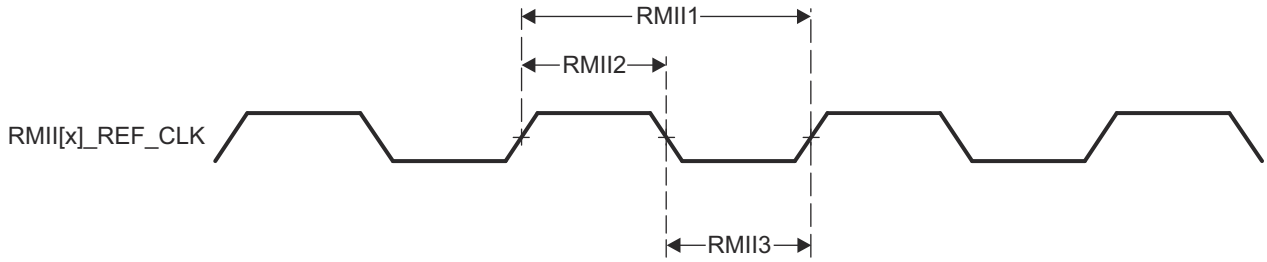

図 6-48. RMII[x]_REF_CLK Timing Requirements – RMII Mode

6.9.5.4.2.2 RMII[x]_RXD[1:0], RMII[x]_CRS_DV, and RMII[x]_RX_ER Timing Requirements – RMII Mode

NO.	PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
RMII4	$t_{su(rxdV\text{-}ref_clkH)}$	Setup time, RMII[x]_RXD[1:0] valid before RMII[x]_REF_CLK rising edge	4			ns
	$t_{su(crs_dvV\text{-}ref_clkH)}$	Setup time, RMII[x]_CRS_DV valid before RMII[x]_REF_CLK rising edge	4			ns
	$t_{su(rx_erV\text{-}ref_clkH)}$	Setup time, RMII[x]_RX_ER valid before RMII[x]_REF_CLK rising edge	4			ns
RMII5	$t_{h(ref_clkH\text{-}rxdV)}$	Hold time, RMII[x]_RXD[1:0] valid after RMII[x]_REF_CLK rising edge	2			ns
	$t_{h(ref_clkH\text{-}crs_dvV)}$	Hold time, RMII[x]_CRS_DV valid after RMII[x]_REF_CLK rising edge	2			ns
	$t_{h(ref_clkH\text{-}rx_erV)}$	Hold time, RMII[x]_RX_ER valid after RMII[x]_REF_CLK rising edge	2			ns

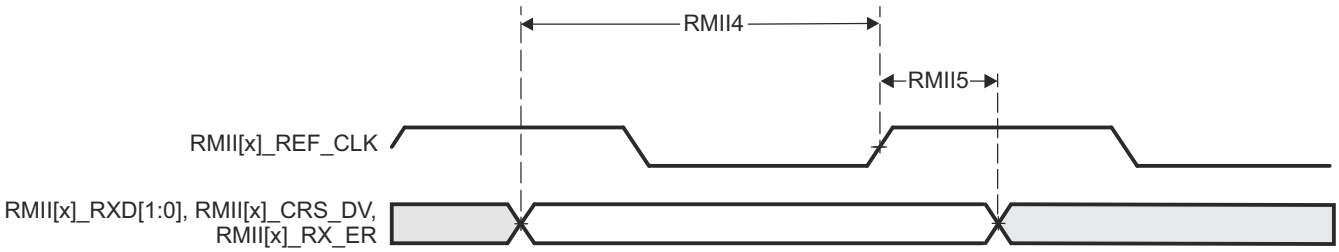

図 6-49. CPSW9G RMII[x]_RXD[1:0], RMII[x]_CRS_DV, RMII[x]_RXER Timing Requirements – RMII Mode

セクション 6.9.5.4.2.3 and present switching characteristics for CPSW9G RMII transmit.

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6.9.5.4.2.3 RMII[x]_TXD[1:0], and RMII[x]_TXEN Switching Characteristics – RMII Mode

NO.	PARAMETER		MIN	TYP	MAX	UNIT
RMII6	$t_{d(ref_clkH\text{-}txdV)}$	Delay time, RMII[x]_REF_CLK rising edge to RMII[x]_TXD[1:0] valid	2		13	ns
	$t_{d(ref_clkH\text{-}tx_enV)}$	Delay time, RMII[x]_REF_CLK rising edge to RMII[x]_TX_EN valid	2		13	ns

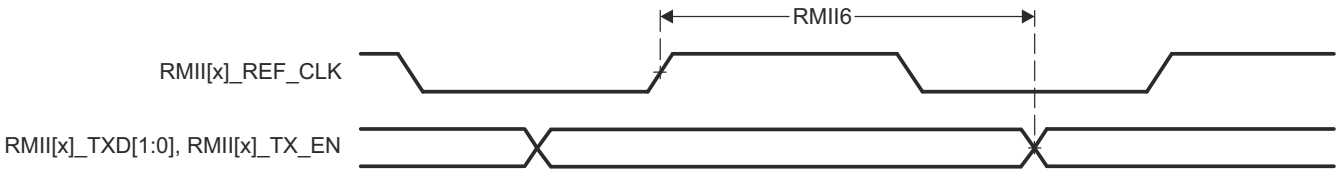


図 6-50. RMII[x]_TXD[1:0], and RMII[x]_TX_EN Switching Characteristics – RMII Mode

6.9.5.4.3 CPSW9G RGMII Timings

表 6-48, セクション 6.9.5.4.3.1, セクション 6.9.5.4.3.2, and 図 6-51 present timing requirements for receive RGMII operation.

For more information, see *Gigabit Ethernet Switch (CPSW0)* section in *Peripherals* chapter in the device TRM.

表 6-48. CPSW9G RGMII Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		2.64	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		2	20	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	RGMII[x]_RXC, RGMII[x]_RD[3:0], RGMII[x]_RX_CTL		50	ps
		RGMII[x]_TXC, RGMII[x]_TD[3:0], RGMII[x]_TX_CTL		50	ps

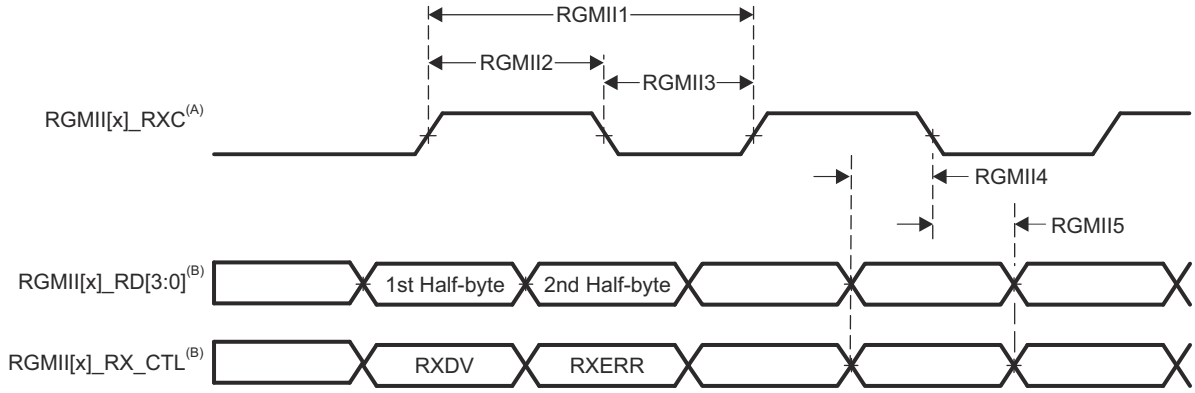
6.9.5.4.3.1 RGMII[x]_RXC Timing Requirements – RGMII Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
RGMII1	$t_{c(rxc)}$	Cycle time, RGMII[x]_RXC	10Mbps	360	440	ns
			100Mbps	36	44	ns
			1000Mbps	7.2	8.8	ns
RGMII2	$t_{w(rxcH)}$	Pulse duration, RGMII[x]_RXC high	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns
RGMII3	$t_{w(rxcL)}$	Pulse duration, RGMII[x]_RXC low	10Mbps	160	240	ns
			100Mbps	16	24	ns
			1000Mbps	3.6	4.4	ns

6.9.5.4.3.2 RGMII[x]_RD[3:0] and RGMII[x]_RCTL Timing Requirements – RGMII Mode

see 図 6-51

NO.			MODE	MIN	MAX	UNIT
RGMII4	$t_{su(rdV-rxcV)}$	Setup time, RGMII[x]_RD[3:0] valid before RGMII[x]_RXC transition	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{su(rx_ctlV-rxcV)}$	Setup time, RGMII[x]_RX_CTL valid before RGMII[x]_RXC transition	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
RGMII5	$t_{h(rxcV-rdV)}$	Hold time, RGMII[x]_RD[3:0] valid after RGMII[x]_RXC transition	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns
	$t_{h(rxcV-rx_ctlV)}$	Hold time, RGMII[x]_RX_CTL valid after RGMII[x]_RXC transition	10Mbps	1		ns
			100Mbps	1		ns
			1000Mbps	1		ns



A. RGMII_RXC must be externally delayed relative to the data and control pins.
B. Data and control information is received using both edges of the clocks. RGMII_RXD[3:0] carries data bits 3-0 on the rising edge of RGMII_RXC and data bits 7-4 on the falling edge of RGMII_RXC. Similarly, RGMII_RXCTL carries RXDV on rising edge of RGMII_RXC and RXERR on falling edge of RGMII_RXC.

図 6-51. CPSW9G RGMII[x]_RXC, RGMII[x]_RD[3:0] and RGMII[x]_RCTL Timing Requirements – RGMII Mode

セクション 6.9.5.4.3.3, セクション 6.9.5.4.3.4, and 図 6-52 present switching characteristics for transmit - RGMII for 10 Mbps, 100 Mbps, and 1000 Mbps.

6.9.5.4.3.3 RGMII[x]_TXC Switching Characteristics – RGMII Mode

see 図 6-52

NO.	PARAMETER		MODE	MIN	TYP	MAX	UNIT
RGMII6	$t_{c(txc)}$	Cycle time, RGMII[x]_TXC	10Mbps	360		440	ns
			100Mbps	36		44	ns
			1000Mbps	7.2		8.8	ns
RGMII7	$t_{w(txcH)}$	Pulse duration, RGMII[x]_TXC high	10Mbps	160		240	ns
			100Mbps	16		24	ns
			1000Mbps	3.6		4.4	ns

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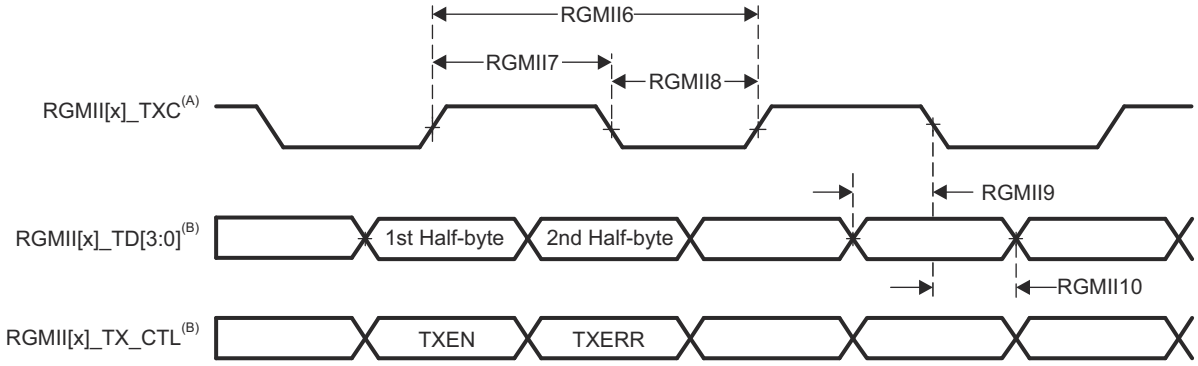
see 図 6-52

NO.	PARAMETER		MODE	MIN	TYP	MAX	UNIT
RGMII8	$t_{w(txcL)}$	Pulse duration, RGMII[x]_TXC low	10Mbps	160		240	ns
			100Mbps	16		24	ns
			1000Mbps	3.6		4.4	ns

6.9.5.4.3.4 RGMII[x]_TD[3:0] and RGMII[x]_TX_CTL Switching Characteristics – RGMII Mode

see 図 6-52

NO.	PARAMETER		MODE	MIN	MAX	UNIT
RGMII9	$t_{osu(tdV-txcV)}$	Output setup time, RGMII[x]_TD[3:0] valid to RGMII[x]_TXC transition	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.05		ns
	$t_{osu(tx_ctlV-txcV)}$	Output setup time, RGMII[x]_TX_CTL valid to RGMII[x]_TXC transition	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.05		ns
RGMII10	$t_{oh(tdV-txcV)}$	Output hold time, RGMII[x]_TD[3:0] valid after RGMII[x]_TXC transition	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.05		ns
	$t_{oh(tx_ctlV-txcV)}$	Output hold time, RGMII[x]_TX_CTL valid after RGMII[x]_TXC transition	10Mbps	1.2		ns
			100Mbps	1.2		ns
			1000Mbps	1.05		ns



A. TXC is delayed internally before being driven to the RGMII[x]_TXC pin. This internal delay is always enabled.
B. Data and control information is received using both edges of the clocks. RGMII_TD[3:0] carries data bits 3-0 on the rising edge of RGMII_TXC and data bits 7-4 on the falling edge of RGMII_TXC. Similarly, RGMII_TX_CTL carries TXDV on rising edge of RGMII_TXC and RTXERR on falling edge of RGMII_TXC.

図 6-52. CPSW9G RGMII[x]_TXC, RGMII[x]_TD[3:0], and RGMII[x]_TX_CTL Switching Characteristics - RGMII Mode

6.9.5.5 CSI-2

注

For more information, see the Camera Streaming Interface Receiver (CSI_RX_IF) chapter in the device TRM.

The CSI_RX_IF deals with the processing of the pixel data coming from an external image sensor and data from memory. It is a key component for the following multimedia applications: camera viewfinder, video record, and still image capture.

The CSI_RX_IF has a primary serial interface (CSI-2 port) compliant with the MIPI D-PHY RX specification v1.2 and the MIPI CSI-2 specification v1.3, with 4 differential data lanes plus 1 differential clock lane in synchronous mode, double data rate. Refer to the specification for timing details.

- 2.5 Gbps (1.25 GHz) for each lane.

6.9.5.6 DDRSS

For more details about features and additional description information on the device LPDDR4 Memory Interfaces, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

The device has dedicated interface to LPDDR4. It supports JEDEC JESD209-4B standard compliant LPDDR4 SDRAM devices with the following features:

- 32-bit data path to external SDRAM memory
- Memory device capacity: Up to 8GB address space available over two chip selects (4GB per rank)
- No support for byte mode, or memories with more than 17 row address bits

表 6-49 and 図 6-53 present switching characteristics for DDRSS.

表 6-49. Switching Characteristics for DDRSS

NO.	PARAMETER		DDR TYPE	MIN	MAX	UNIT
1	$t_{c(DDR_CKP/DDR_CKN)}$	Cycle time, DDR0_CKP and DDR0_CKN	LPDDR4	0.536	3.003	ns

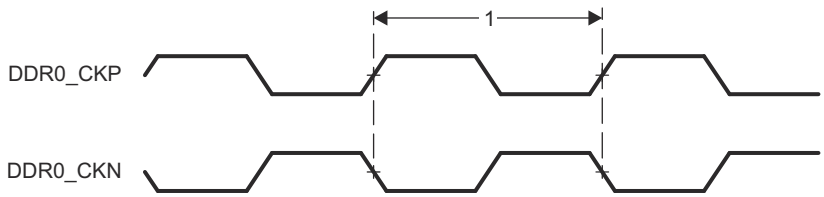


図 6-53. DDRSS Memory Interface Clock Timing

For more information, see *DDR Subsystem (DDRSS)* section in *Memory Controllers* chapter in the device TRM.

6.9.5.7 DSS

For more details about features and additional description information on the device Display Subsystem – Video Output Ports, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

表 6-50 represents DPI timing conditions.

表 6-50. DPI Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1.44	26.4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1.5	5	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

表 6-51, 表 6-52, 図 6-54 and 図 6-55 assume testing over the recommended operating conditions and electrical characteristic conditions.

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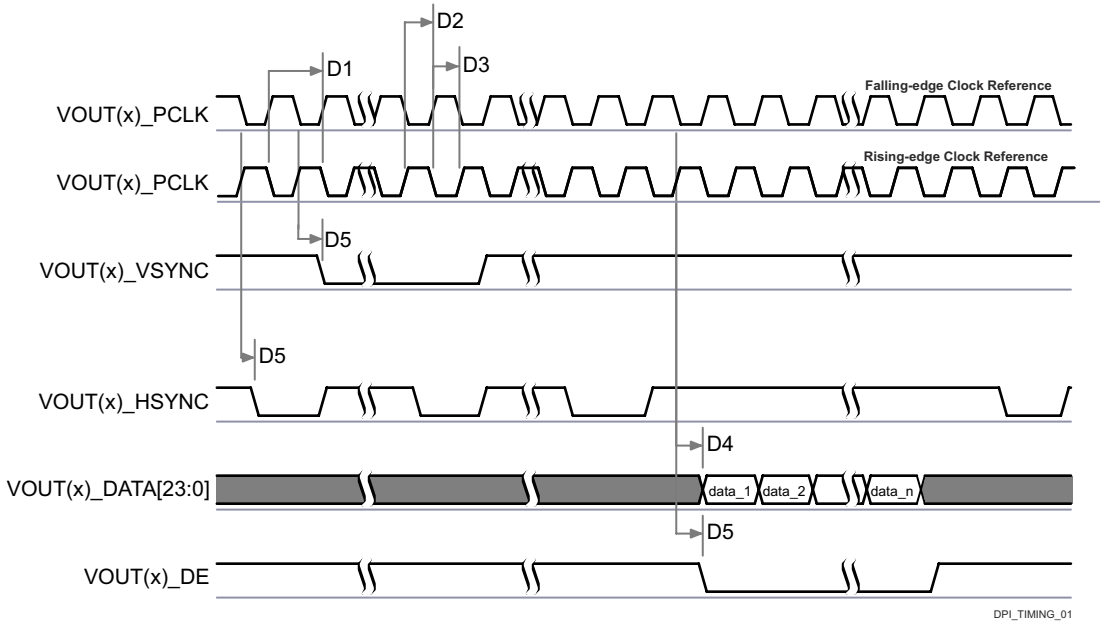
表 6-51. DPI Video Output Switching Characteristics

NO.(2)	PARAMETER		MIN	MAX	UNIT
D1	$t_{c(pclk)}$	Cycle time, VOUT(x)_PCLK	6.06		ns
D2	$t_{w(pclkL)}$	Pulse duration, VOUT(x)_PCLK low	0.475×P(1)		ns
D3	$t_{w(pclkH)}$	Pulse duration, VOUT(x)_PCLK high	0.475×P(1)		ns
D4	$t_{d(pclkV\text{-}dataV)}$	Delay time, VOUT(x)_PCLK transition to VOUT(x)_DATA[23:0] transition	-0.68	1.78	ns
D5	$t_{d(pclkV\text{-}ctrlL)}$	Delay time, VOUT(x)_PCLK transition to control signals VOUT(x)_VSYNC, VOUT(x)_HSYNC, VOUT(x)_DE falling edge	-0.68	1.78	ns

(1) P = output VOUT(x)_PCLK period in ns.
(2) x in VOUT(x) = 1 or 2



A. The configuration of assertion of the data can be programmed on the falling or rising edge of the pixel clock.
B. The polarity and the pulse width of VOUT(x)_HSYNC and VOUT(x)_VSYNC are programmable, refer to *Display Subsystem (DSS)* section in *Peripherals* chapter in the device TRM.
C. The VOUT(x)_PCLK frequency can be configured, refer to *Display Subsystem* section in *Peripherals* chapter in the device TRM.
D. x in VOUT(x) = 1 or 2.

図 6-54. DPI Video Output

表 6-52. DPI External Pixel Clock Timing Requirements

NO.(2)			MIN	MAX	UNIT
D6	$t_{c(extpclkin)}$	Cycle time, VOUT(x)_EXTPCLKIN	6.06		ns
D7	$t_{w(extpclkinL)}$	Pulse duration, VOUT(x)_EXTPCLKIN low	0.45×P(1)		ns
D8	$t_{w(extpclkinH)}$	Pulse duration, VOUT(x)_EXTPCLKIN high	0.45×P(1)		ns

(1) P = output VOUT(x)_PCLK period in ns.
(2) x in VOUT(x) = 1 or 2

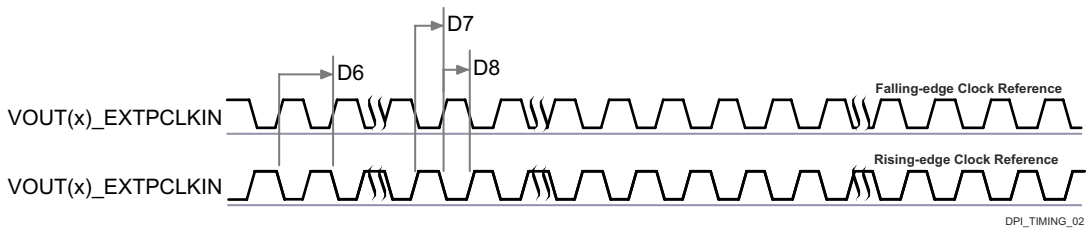


図 6-55. DPI External Pixel Clock Input

For more information, see *Display Subsystem (DSS) and Peripherals* section in *Peripherals* chapter in the device TRM.

6.9.5.8 eCAP

The supported features by the device ECAP are:

- 32-bit time base counter
- 4-event time-stamp registers (each 32 bits)
- Independent edge polarity selection for up to four sequenced time-stamp capture events
- Interrupt capabilities on any of the four capture events
- Input capture signal pre-scaling (from 1 to 16)
- Support of different capture modes (single shot capture, continuous mode capture, absolute timestamp capture or difference mode time-stamp capture)

表 6-53 represents ECAP timing conditions.

表 6-53. ECAP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

セクション 6.9.5.8.1 and セクション 6.9.5.8.2 present timing and switching characteristics for eCAP (see 図 6-56 and 図 6-57).

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6.9.5.8.1 Timing Requirements for eCAP

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP1	$t_{w(cap)}$	Pulse duration, CAP (asynchronous)	2 + 2P[(1)]		ns

(1) P = sysclk

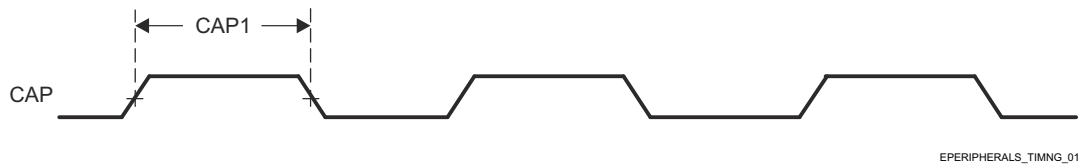

図 6-56. eCAP Input Timings

6.9.5.8.2 Switching Characteristics for eCAP

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
CAP2	$t_{w(apwm)}$	Pulse duration, APWM	-2 + 2P[(1)]		ns

(1) P = sysclk

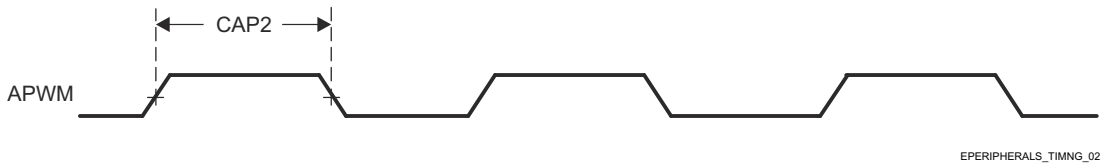

図 6-57. eCAP Output Timings

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

6.9.5.9 EPWM

The supported features by the device EPWM are:

- Dedicated 16-bit time-base counter with period and frequency control
- Two independent PWM outputs which can be used in different configurations (with single-edge operation, with dual-edge symmetric operation or one independent PWM output with dual-edge asymmetric operation)
- Asynchronous override control of PWM signals during fault conditions
- Programmable phase-control support for lag or lead operation relative to other EPWM modules
- Dead-band generation with independent rising and falling edge delay control
- Programmable trip zone allocation of both latched and un-latched fault conditions
- Events enabling to trigger both CPU interrupts and start of ADC conversions

表 6-54 represents EPWM timing conditions.

表 6-54. EPWM Timing Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

セクション 6.9.5.9.1, セクション 6.9.5.9.2 and present timing and switching characteristics for eHRPWM (see 図 6-58, 図 6-59, 図 6-60, and 図 6-61).

6.9.5.9.1 Switching Characteristics for eHRPWM

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM1	$t_{w(pwm)}$	Pulse duration, EHRPWM_A/B, high or low	P-3[(1)]		ns
PWM2	$t_{w(syncout)}$	Pulse duration, EHRPWM_SYNCO	P-3[(1)]		ns
PWM3	$t_{d(tzL-pwmV)}$	Delay time, EHRPWM_TZn_IN falling edge to EHRPWM_A/B valid		11	ns
PWM4	$t_{d(tzL-pwmZ)}$	Delay time, EHRPWM_TZn_IN falling edge to EHRPWM_A/B Hi-Z		11	ns
PWM5	$t_{w(soc)}$	Pulse duration, EHRPWM_SOCA/B	P-3[(1)]		ns

(1) P = sysclk

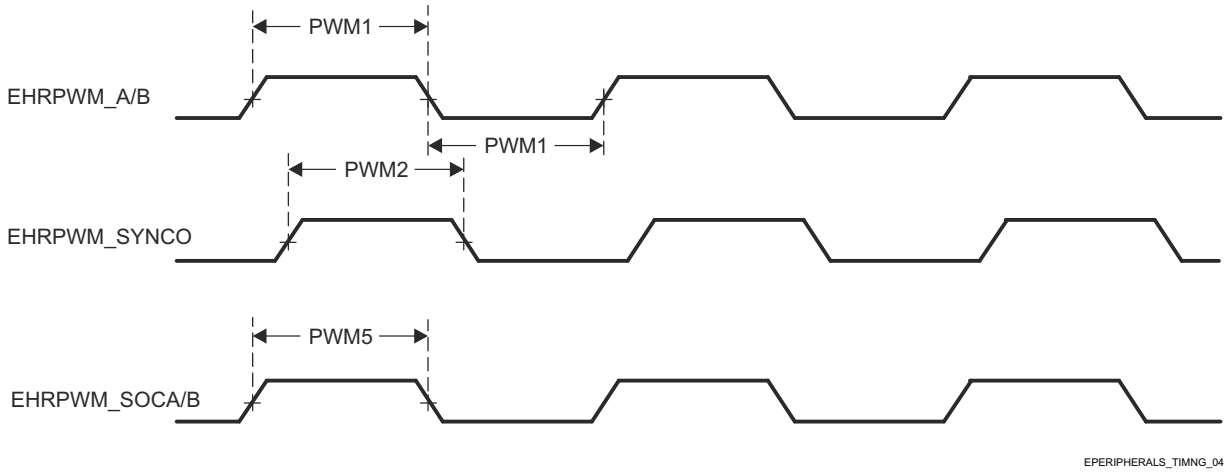

図 6-58. EPWM_A/B_out, ePWM_SYNCO, and ePWM_SOCA/B Input Timings

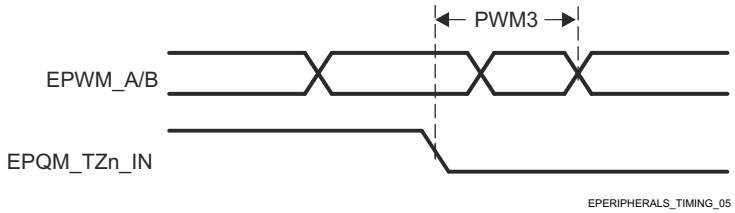

図 6-59. EPWM_A/B and ePWM_TZn_IN Forced High/Low Input Timings

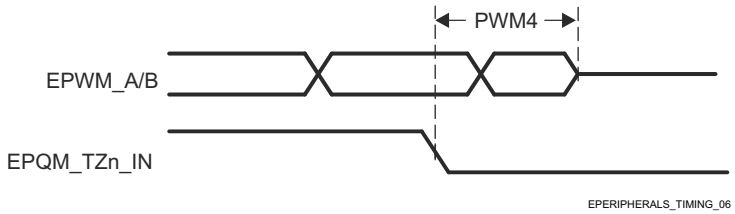

図 6-60. EPWM_A/B and ePWM_TZn_IN Hi–Z Input Timings

6.9.5.9.2 Timing Requirements for eHRPWM

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM6	$t_{w(synci)}$	Pulse duration, EHRPWM_SYNCI	2 + 2P[(1)]		ns

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NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
PWM7	$t_{w(tz)}$	Pulse duration, EHRPWM_TZn_IN low	2 + 3P[(1)]		ns

(1) P = sysclk

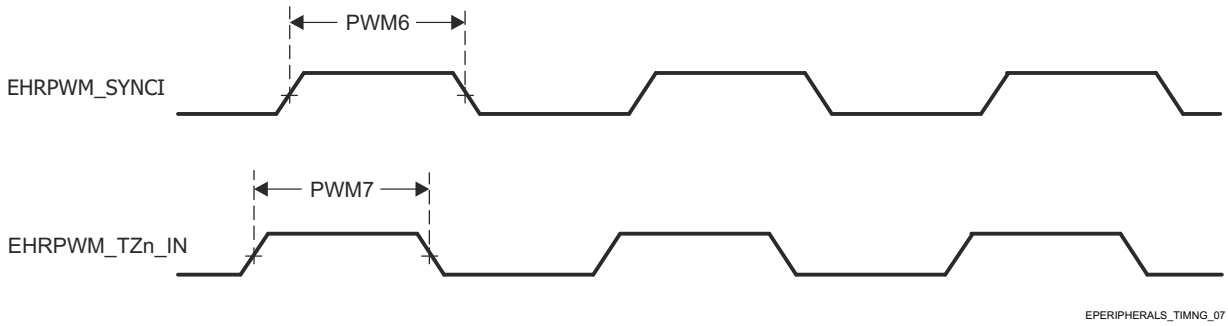

図 6-61. ePWM_SYNCI and ePWM_TZn_IN Output Timings

For more information, see *Camera Subsystem* section in *Peripherals* chapter in the device TRM.

6.9.5.10 eQEP

The supported features by the device eQEP are:

- Input Synchronization
- Three Stage/Six Stage Digital Noise Filter
- Quadrature Decoder Unit
- Position Counter and Control unit for position measurement
- Quadrature Edge Capture unit for low speed measurement
- Unit Time base for speed/frequency measurement
- Watchdog Timer for detecting stalls

表 6-55 represents EQEP timing conditions.

表 6-55. EQEP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	1	4	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	7	pF

セクション 6.9.5.10.1 and セクション 6.9.5.10.2 present timing requirements and switching characteristics for eQEP (see 図 6-62).

6.9.5.10.1 Timing Requirements for eQEP

NO.			MIN	MAX	UNIT
QEP1	$t_{w(qep)}$	Pulse duration, QEP_A/B	2 + 2P[(1)]		ns
QEP2	$t_{w(qepiH)}$	Pulse duration, QEP_I high	2 + 2P[(1)]		ns
QEP3	$t_{w(qepiL)}$	Pulse duration, QEP_I low	2 + 2P[(1)]		ns
QEP4	$t_{w(qepsH)}$	Pulse duration, QEP_S high	2 + 2P[(1)]		ns

NO.			MIN	MAX	UNIT
QEP5	$t_{w(qepsL)}$	Pulse duration, QEP_S low	2 + 2P(1)		ns

(1) P = sysclk

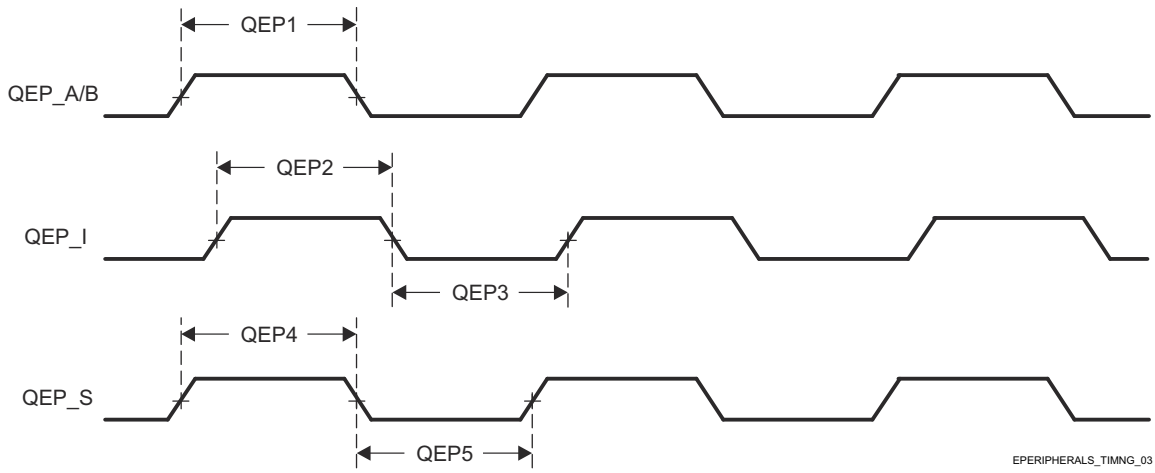

図 6-62. eQEP Input Timings

6.9.5.10.2 Switching Characteristics for eQEP

NO.	PARAMETER		MIN	MAX	UNIT
QEP6	$t_{d(QEP\text{-}CNTR)}$	Delay time, external clock to counter increment		24	ns

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

6.9.5.11 GPIO

The device has ten instances of GPIO modules. The GPIO modules are integrated in three groups.

- Group one: WKUP_GPIO0 and WKUP_GPIO1
- Group two: GPIO0, GPIO2, GPIO4, and GPIO6
- Group three: GPIO1, GPIO3, GPIO5, and GPIO7

Within each group, exactly one module is selected to control the corresponding I/O pins and pin interrupts.

The GPIO pins are grouped into banks (16 pins per bank), which means that each GPIO module provides up to 144 dedicated general-purpose pins with input and output capabilities; thus, the general-purpose interface supports up to 432 (3 instances × (9 banks × 16 pins)) pins. Since WKUP_GPIOu_[84:143] (u = 0, 1), GPIOn_[128:143] (n = 0, 2, 4, 6), and GPIOm_[36:143] (m = 1, 3, 5 ,7) are reserved in this device, general purpose interface supports up to 248 I/O pins.

For more details about features and additional description information on the device General-Purpose Interface, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

注

The general-purpose input/output i (i = 0 to 1) is also referred to as GPIOi.

表 6-56 represents GPIO timing conditions.

表 6-56. GPIO Timing Conditions

PARAMETER	BUFFER TYPE	MIN	MAX	UNIT
INPUT CONDITIONS				

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表 6-56. GPIO Timing Conditions (続き)

PARAMETER		BUFFER TYPE	MIN	MAX	UNIT
SR_I	Input slew rate	LVCMOS (VDD[1] = 1.8 V)	0.0018	6.6	V/ns
		LVCMOS (VDD[1] = 3.3V)	0.0033	6.6	V/ns
		I2C OD FS (VDD[1] = 1.8 V)	0.0018	6.6	V/ns
		I2C OD FS (VDD[1] = 3.3V)	0.0033	0.08	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	LVCMOS	3	10	pF
		I2C OD FS	3	100	pF

(1) VDD stands for corresponding power supply. For more information on the power supply name and the corresponding ball(s), see POWER column of the *Pin Attributes* table.

セクション 6.9.5.11.1 and セクション 6.9.5.11.2 present timings and switching characteristics of the GPIO Interface.

6.9.5.11.1 GPIO Timing Requirements

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
GPIO1	$t_{w(GPIO_IN)}$	Pulse width, GPIOn_x	2P + 30[1]		ns

(1) P = functional clock period in ns.

6.9.5.11.2 GPIO Switching Characteristics

NO.	PARAMETER	DESCRIPTION	BUFFER TYPE	MIN	MAX	UNIT
GPIO2	$t_{w(GPIO_OUT)}$	Pulse width, GPIOn_x	LVCMOS	0.975P[1] - 3.6		ns
			I2C OD FS	160		ns

(1) P = functional clock period in ns.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

6.9.5.12 GPMC

For more details about features and additional description information on the device General-Purpose Memory Controller, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

表 6-57 represents GPMC timing conditions.

注

The IO timings provided in this section are applicable for all combinations of signals for GPMC0. However, the timings are only valid for GPMC0 if signals within a single IOSET are used. The IOSETs are defined in the セクション 6.9.5.12.4 , *GPMC0_IOSET*,table.

表 6-57. GPMC Timing Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
Input Conditions				
t_{SR}	Input slew rate	1.65	4	V/ns
Output Conditions				
C_{LOAD}	Output load capacitance	5	20	pF

6.9.5.12.1 GPMC and NOR Flash — Synchronous Mode

セクション 6.9.5.12.1.1 and セクション 6.9.5.12.1.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 図 6-63 through 図 6-67).

6.9.5.12.1.1 GPMC and NOR Flash Timing Requirements — Synchronous Mode

NO.	PARAMETER	DESCRIPTION[2]	MODE[3]	MIN	MAX	MIN	MAX	UNIT
				100 MHz[4]		133 MHz[4]		
F12	$t_{su(dV-clkH)}$	Setup time, input data GPMC_AD[15:0] valid before output clock GPMC_CLK high	div_by_1_mode;	1.81		1.11		ns
			not_div_by_1_mode;	1.06				ns
F13	$t_{h(clkH-dV)}$	Hold time, input data GPMC_AD[15:0] valid after output clock GPMC_CLK high	div_by_1_mode;	1.78		2.28		ns
			not_div_by_1_mode;	1.78				ns
F21	$t_{su(waitV-clkH)}$	Setup time, input wait GPMC_WAIT[j] valid before output clock GPMC_CLK high[1]	div_by_1_mode;	1.81		1.11		ns
			not_div_by_1_mode;	1.06				ns
F22	$t_{h(clkH-waitV)}$	Hold time, input wait GPMC_WAIT[j] valid after output clock GPMC_CLK high[1]	div_by_1_mode;	1.78		2.28		ns
			not_div_by_1_mode;	1.78				ns

(1) In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.
(2) Wait monitoring support is limited to a WaitMonitoringTime value > 0. For a full description of wait monitoring feature, see *General-Purpose Memory Controller (GPMC)* section in the device TRM.
(3) For div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 1h to 3h:
  - GPMC_CLK frequency = GPMC_FCLK frequency / (2 to 4)
-

(4) For 100 MHz:
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = MAIN_PLL2_HSDIV1_CLKOUT / 3

For 133 MHz:
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = MAIN_PLL0_HSDIV3_CLKOUT

6.9.5.12.1.2 GPMC and NOR Flash Switching Characteristics – Synchronous Mode

NO.[2]	PARAMETER	DESCRIPTION	MODE[19]	MIN	MAX	MIN	MAX	UNIT
				100 MHz[20]		133 MHz[20]		
F0	tc(clk)	Period, output clock GPMC_CLK[18]	div_by_1_mode;	10		7.52		ns
F1	$t_{w(clkH)}$	Typical pulse duration, output clock GPMC_CLK high	div_by_1_mode	0.475*P[15]- 0.3		0.475*P[15]- 0.3		ns
F1	$t_{w(clkL)}$	Typical pulse duration, output clock GPMC_CLK low	div_by_1_mode	0.475*P[15]- 0.3		0.475*P[15]- 0.3		ns
F2	$t_{d(clkH-csnV)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] transition[14]	div_by_1_mode no extra_delay	F[6]-2.2	F+3.75	F[6]-2.2	F[6]+3.75	ns
F3	$t_{d(clkH-CSn[i]V)}$	Delay time, output clock GPMC_CLK rising edge to output chip select GPMC_CSn[i] invalid[14]	div_by_1_mode no extra_delay	E[5]-2.2	E[5]+3.75	E[5]-2.2	E[5]+3.75	ns
F4	$t_{d(aV-clk)}$	Delay time, output address GPMC_A[27:1] valid to output clock GPMC_CLK first edge	div_by_1_mode	B[2]-2.3	B[2]+4.5	B[2]-2.3	B[2]+4.5	ns
F5	$t_{d(clkH-aIV)}$	Delay time, output clock GPMC_CLK rising edge to output address GPMC_A[27:1] invalid	div_by_1_mode;	-2.3	4.5	-2.3	4.5	ns

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NO.[2]	PARAMETER	DESCRIPTION	MODE[19]	MIN	MAX	MIN	MAX	UNIT
				100 MHz[20]		133 MHz[20]		
F6	$t_{d(be[x]nV-clk)}$	Delay time, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n valid to output clock GPMC_CLK first edge	div_by_1_mode	B[2]-2.3	B[2]+1.9	B[2]-2.3	B[2]+1.9	ns
F7	$t_{d(clkH-be[x]nIV)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n invalid[11]	div_by_1_mode	D[4]-2.3	D[4]+1.9	D[4]-2.3	D[4]+1.9	ns
F7	$t_{d(clkL-be[x]nIV)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid[12]	div_by_1_mode	D[4]-2.3	D[4]+1.9	D[4]-2.3	D[4]+1.9	ns
F7	$t_{d(clkL-be[x]nIV)}$.	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n invalid[13]	div_by_1_mode	D[4]-2.3	D[4]+1.9	D[4]-2.3	D[4]+1.9	ns
F8	$t_{d(clkH-advn)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE transition	div_by_1_mode no extra_delay	G[7]-2.3	G[7]+4.5	G[7]-2.3	G[7]+4.5	ns
F9	$t_{d(clkH-advnIV)}$	Delay time, output clock GPMC_CLK rising edge to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode; no extra_delay	D[4]-2.3	D[4]+4.5	D[4]-2.3	D[4]+4.5	ns
F10	$t_{d(clkH-oen)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn transition	div_by_1_mode no extra_delay	H[8]-2.3	H[8]+3.5	H[8]-2.3	H[8]+3.5	ns
F11	$t_{d(clkH-oenIV)}$	Delay time, output clock GPMC_CLK rising edge to output enable GPMC_OEn_REn invalid	div_by_1_mode no extra_delay	E[8]-2.3	E[8]+3.5	E[8]-2.3	E[8]+ 3.5	ns
F14	$t_{d(clkH-wen)}$	Delay time, output clock GPMC_CLK rising edge to output write enable GPMC_WEn transition	div_by_1_mode no extra_delay	I[9]- 2.3	I[9]+4.5	I[9]- 2.3	I[9]+4.5	ns
F15	$t_{d(clkH-do)}$	Delay time, output clock GPMC_CLK rising edge to output data GPMC_AD[15:0] transition[11]	div_by_1_mode	J[10]-2.3	J[10]+2.7	J[10]-2.3	J[10]+2.7	ns
F15	$t_{d(clkL-do)}$	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition[12]	div_by_1_mode	J[10]-2.3	J[10]+2.7	J[10]-2.3	J[10]+2.7	ns
F15	$t_{d(clkL-do)}$.	Delay time, GPMC_CLK falling edge to GPMC_AD[15:0] data bus transition[13]	div_by_1_mode	J[10]-2.3	J[10]+2.7	J[10]-2.3	J[10]+2.7	ns
F17	$t_{d(clkH-be[x]n)}$	Delay time, output clock GPMC_CLK rising edge to output lower byte enable and command latch enable GPMC_BE0n_CLE transition[11]	div_by_1_mode	J[10]-2.3	J[10]+1.9	J[10]-2.3	J[10]+1.9	ns
F17	$t_{d(clkL-be[x]n)}$	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition[12]	div_by_1_mode	J[10]-2.3	J[10]+1.9	J[10]-2.3	J[10]+1.9	ns
F17	$t_{d(clkL-be[x]n)}$.	Delay time, GPMC_CLK falling edge to GPMC_BE0n_CLE, GPMC_BE1n transition[13]	div_by_1_mode	J[10]-2.3	J[10]+1.9	J[10]-2.3	J[10]+1.9	ns
F18	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[i] low[14]	Read	A[1]		A[1]		ns
			Write	A[1]		A[1]		ns
F19	$t_{w(be[x]nV)}$	Pulse duration, output lower byte enable and command latch enable GPMC_BE0n_CLE, output upper byte enable GPMC_BE1n low	Read	C[3]		C[3]		ns
			Write	C[3]		C[3]		ns

NO.[2]	PARAMETER	DESCRIPTION	MODE[19]	MIN	MAX	MIN	MAX	UNIT
				100 MHz[20]		133 MHz[20]		
F20	$t_{w(advnV)}$	Pulse duration, output address valid and address latch enable GPMC_ADVn_ALE low	Read	K[16]		K[16]		ns
			Write	K[16]		K[16]		ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
With n being the page burst access number.

(2) B = ClkActivationTime × GPMC_FCLK[17]

(3) For single read: C = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst read: C = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst write: C = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
With n being the page burst access number.

(4) For single read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst read: D = (RdCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst write: D = (WrCycleTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]

(5) For single read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst read: E = (CSRdOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For burst write: E = (CSWrOffTime - AccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]

(6) For csn falling edge (CS activated):
- Case GPMCFCLKDIVIDER = 0:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK[17]
- Case GPMCFCLKDIVIDER = 1:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK[17] if (ClkActivationTime and CSOnTime are odd) or (ClkActivationTime and CSOnTime are even)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK[17] otherwise
- Case GPMCFCLKDIVIDER = 2:
  - F = 0.5 × CSExtraDelay × GPMC_FCLK[17] if ((CSOnTime - ClkActivationTime) is a multiple of 3)
  - F = (1 + 0.5 × CSExtraDelay) × GPMC_FCLK[17] if ((CSOnTime - ClkActivationTime - 1) is a multiple of 3)
  - F = (2 + 0.5 × CSExtraDelay) × GPMC_FCLK[17] if ((CSOnTime - ClkActivationTime - 2) is a multiple of 3)

(7) For ADV falling edge (ADV activated):
- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK[17]
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK[17] if (ClkActivationTime and ADVOnTime are odd) or (ClkActivationTime and ADVOnTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK[17] otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK[17] if ((ADVOnTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK[17] if ((ADVOnTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK[17] if ((ADVOnTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Reading mode:
- Case GPMCFCLKDIVIDER = 0:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK[17]
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK[17] if (ClkActivationTime and ADVRdOffTime are odd) or (ClkActivationTime and ADVRdOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK[17] otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK[17] if ((ADVRdOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK[17] if ((ADVRdOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK[17] if ((ADVRdOffTime - ClkActivationTime - 2) is a multiple of 3)

For ADV rising edge (ADV deactivated) in Writing mode:
- Case GPMCFCLKDIVIDER = 0:

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  - G = 0.5 × ADVExtraDelay × GPMC_FCLK[17]
- Case GPMCFCLKDIVIDER = 1:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK[17] if (ClkActivationTime and ADVWrOffTime are odd) or (ClkActivationTime and ADVWrOffTime are even)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK[17] otherwise
- Case GPMCFCLKDIVIDER = 2:
  - G = 0.5 × ADVExtraDelay × GPMC_FCLK[17] if ((ADVWrOffTime - ClkActivationTime) is a multiple of 3)
  - G = (1 + 0.5 × ADVExtraDelay) × GPMC_FCLK[17] if ((ADVWrOffTime - ClkActivationTime - 1) is a multiple of 3)
  - G = (2 + 0.5 × ADVExtraDelay) × GPMC_FCLK[17] if ((ADVWrOffTime - ClkActivationTime - 2) is a multiple of 3)

(8) For OE falling edge (OE activated) and IO DIR rising edge (Data Bus input direction):
- Case GPMCFCLKDIVIDER = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK[17]
- Case GPMCFCLKDIVIDER = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK[17] if (ClkActivationTime and OEOnTime are odd) or (ClkActivationTime and OEOnTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK[17] otherwise
- Case GPMCFCLKDIVIDER = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK[17] if ((OEOnTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK[17] if ((OEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK[17] if ((OEOnTime - ClkActivationTime - 2) is a multiple of 3)

For OE rising edge (OE deactivated):
- Case GPMCFCLKDIVIDER = 0:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK[17]
- Case GPMCFCLKDIVIDER = 1:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK[17] if (ClkActivationTime and OEOffTime are odd) or (ClkActivationTime and OEOffTime are even)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK[17] otherwise
- Case GPMCFCLKDIVIDER = 2:
  - H = 0.5 × OEExtraDelay × GPMC_FCLK[17] if ((OEOffTime - ClkActivationTime) is a multiple of 3)
  - H = (1 + 0.5 × OEExtraDelay) × GPMC_FCLK[17] if ((OEOffTime - ClkActivationTime - 1) is a multiple of 3)
  - H = (2 + 0.5 × OEExtraDelay) × GPMC_FCLK[17] if ((OEOffTime - ClkActivationTime - 2) is a multiple of 3)

(9) For WE falling edge (WE activated):
- Case GPMCFCLKDIVIDER = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[17]
- Case GPMCFCLKDIVIDER = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[17] if (ClkActivationTime and WEOnTime are odd) or (ClkActivationTime and WEOnTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK[17] otherwise
- Case GPMCFCLKDIVIDER = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[17] if ((WEOnTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK[17] if ((WEOnTime - ClkActivationTime - 1) is a multiple of 3)
  - I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK[17] if ((WEOnTime - ClkActivationTime - 2) is a multiple of 3)

For WE rising edge (WE deactivated):
- Case GPMCFCLKDIVIDER = 0:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK [17]
- Case GPMCFCLKDIVIDER = 1:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[17] if (ClkActivationTime and WEOffTime are odd) or (ClkActivationTime and WEOffTime are even)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK[17] otherwise
- Case GPMCFCLKDIVIDER = 2:
  - I = 0.5 × WEExtraDelay × GPMC_FCLK[17] if ((WEOffTime - ClkActivationTime) is a multiple of 3)
  - I = (1 + 0.5 × WEExtraDelay) × GPMC_FCLK[17] if ((WEOffTime - ClkActivationTime - 1) is a multiple of 3)

– I = (2 + 0.5 × WEExtraDelay) × GPMC_FCLK[17] if ((WEOffTime - ClkActivationTime - 2) is a multiple of 3)

(10) J = GPMC_FCLK[17]
(11) First transfer only for CLK DIV 1 mode.
(12) Half cycle; for all data after initial transfer for CLK DIV 1 mode.
(13) Half cycle of GPMC_CLKOUT; for all data for modes other than CLK DIV 1 mode. GPMC_CLKOUT divide down from GPMC_FCLK.
(14) In GPMC_CSn[i], i is equal to 0, 1, 2, or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.
(15) P = GPMC_CLK period in ns
(16) For read: K = (ADVRdOffTime - ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
For write: K = (ADVWrOffTime - ADVOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[17]
(17) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(18) Related to the GPMC_CLK output clock maximum and minimum frequencies programmable in the GPMC module by setting the GPMC_CONFIG1_i configuration register bit field GPMCFCLKDIVIDER.
(19) For div_by_1_mode:

- GPMC_CONFIG1_i register: GPMCFCLKDIVIDER = 0h:
  – GPMC_CLK frequency = GPMC_FCLK frequency

For no extra_delay:

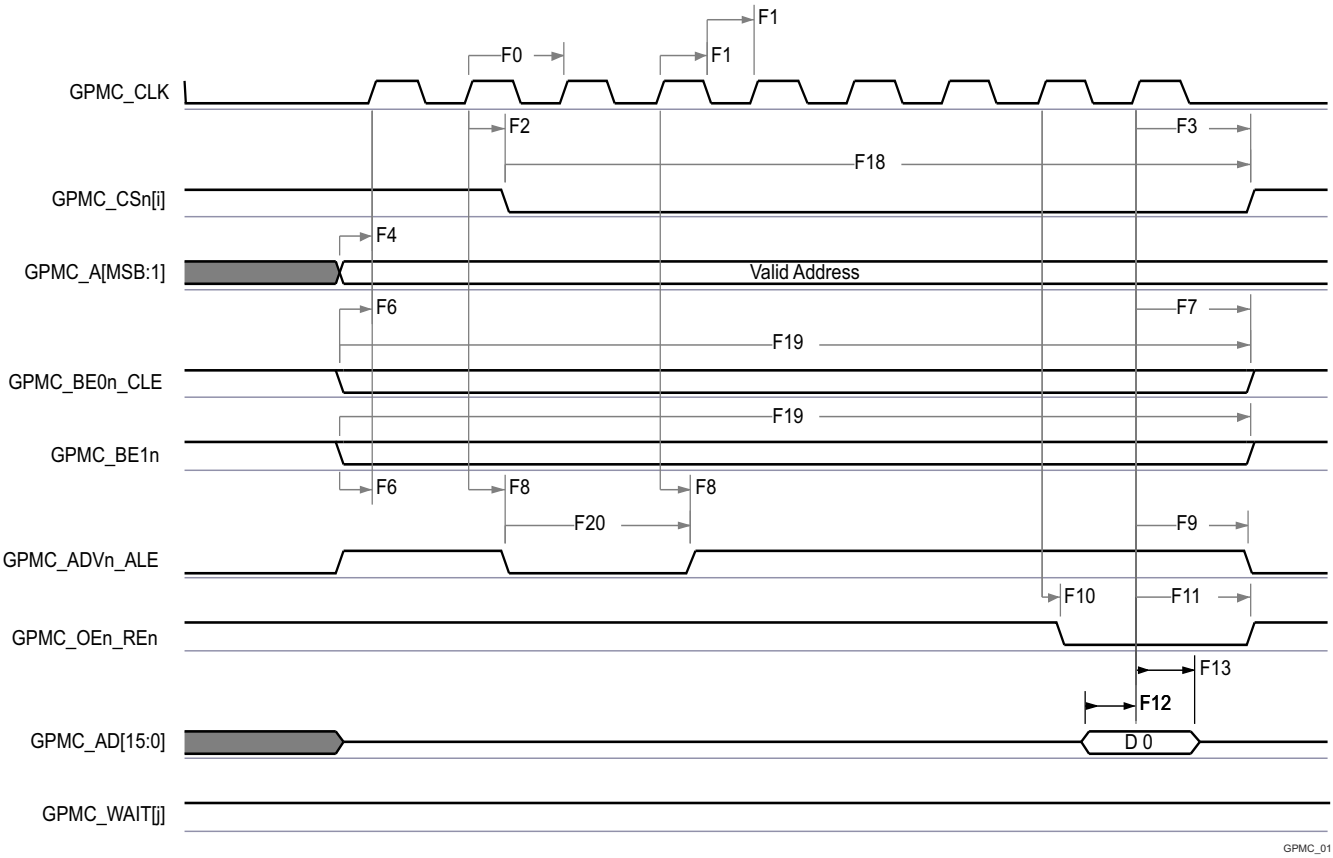
- GPMC_CONFIG2_i Register: CSEXTRADELAY = 0h = CSn Timing control signal is not delayed
- GPMC_CONFIG4_i Register: WEEXTRADELAY = 0h = nWE timing control signal is not delayed
- GPMC_CONFIG4_i Register: OEEXTRADELAY = 0h = nOE timing control signal is not delayed
- GPMC_CONFIG3_i Register: ADVEXTRADELAY = 0h = nADV timing control signal is not delayed

(20) For 100 MHz:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 01 = MAIN_PLL2_HSDIV1_CLKOUT / 3

For 133 MHz:

- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = MAIN_PLL0_HSDIV3_CLKOUT



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

図 6-63. GPMC and NOR Flash — Synchronous Single Read (GPMCFCLKDIVIDER = 0)

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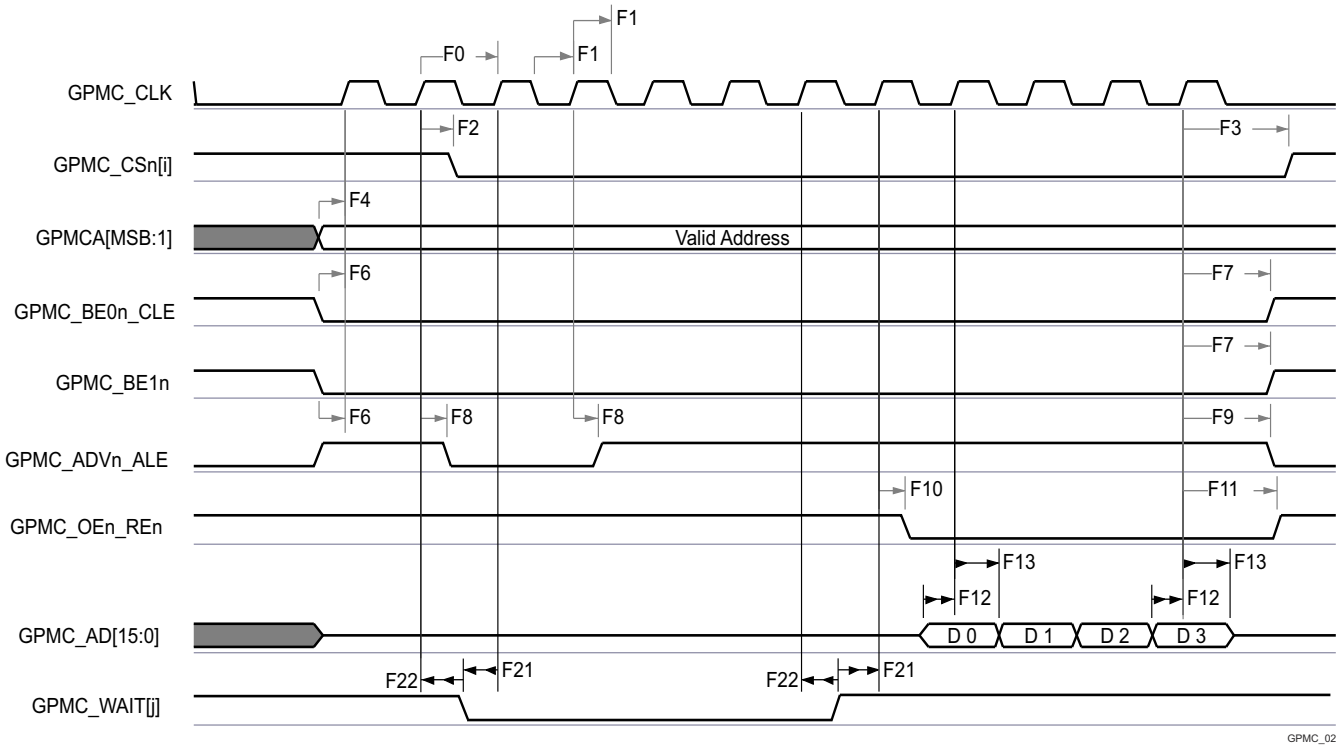
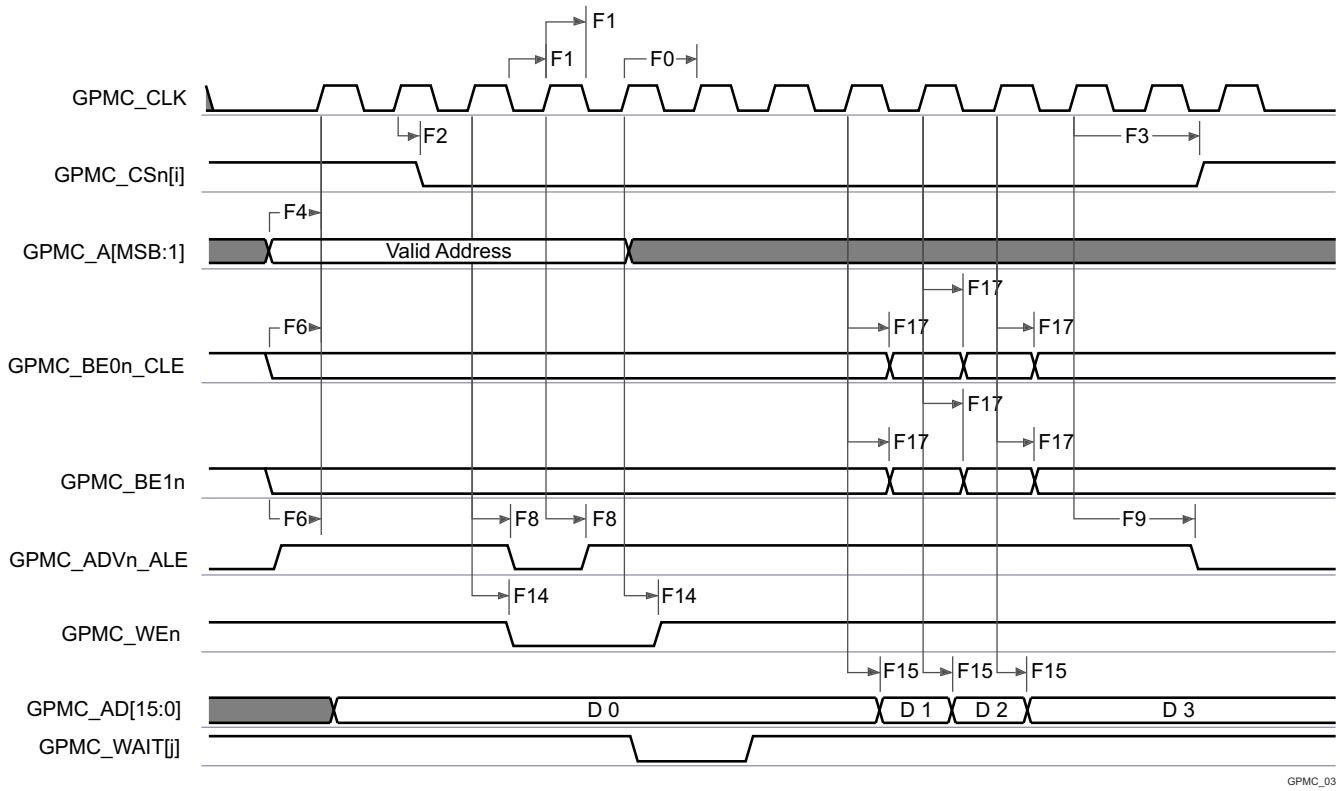


A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

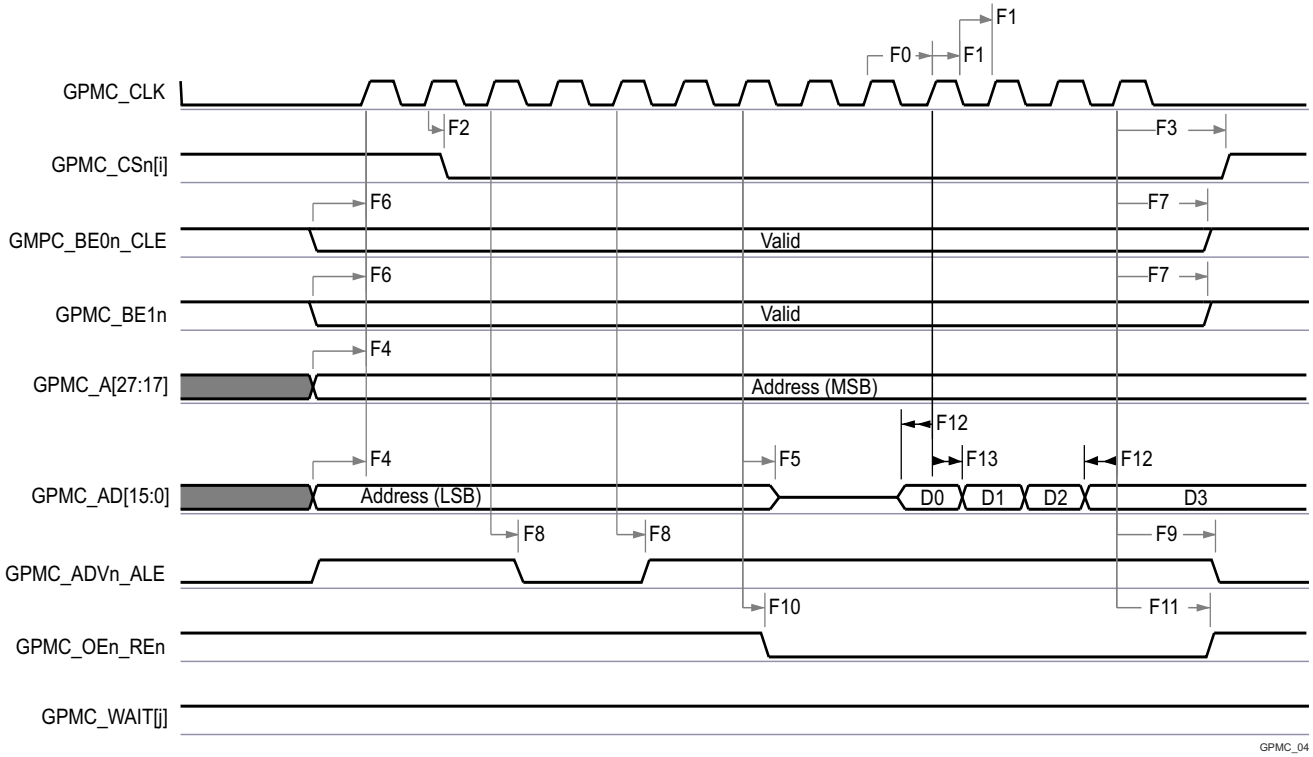
図 6-64. GPMC and NOR Flash — Synchronous Burst Read — 4x16–bit (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

B. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

図 6-65. GPMC and NOR Flash—Synchronous Burst Write (GPMCFCLKDIVIDER = 0)



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

図 6-66. GPMC and Multiplexed NOR Flash — Synchronous Burst Read

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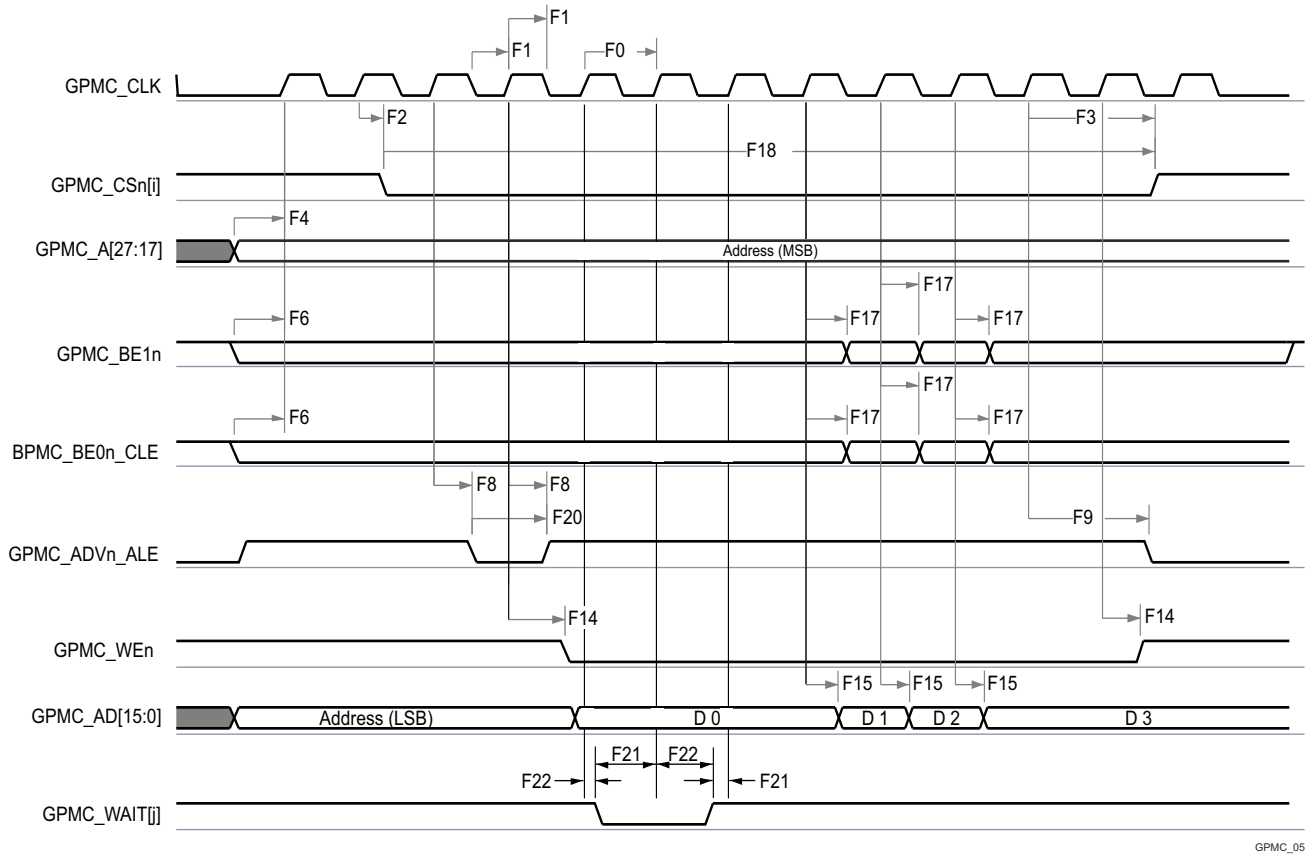

A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
B. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

図 6-67. GPMC and Multiplexed NOR Flash — Synchronous Burst Write

6.9.5.12.2 GPMC and NOR Flash — Asynchronous Mode

セクション 6.9.5.12.2.1 and セクション 6.9.5.12.2.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 図 6-68 through 図 6-73).

6.9.5.12.2.1 GPMC and NOR Flash Timing Requirements – Asynchronous Mode

NO.			MODE[7]	MIN	MAX	UNIT
FA5[1]	$t_{acc(d)}$	Data access time	div_by_1_mode		H[5]	ns
FA20[2]	$t_{acc1\text{-}pgmode(d)}$	Page mode successive data access time	div_by_1_mode		P[4]	ns
FA21[3]	$t_{acc2\text{-}pgmode(d)}$	Page mode first data access time	div_by_1_mode		H[5]	ns

(1) The FA5 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data is internally sampled by active functional clock edge. FA5 value must be stored inside the AccessTime register bit field.
(2) The FA20 prameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data is internally sampled by active functional clock edge after FA20 functional clock cycles. The FA20 value must be stored in the PageBurstAccessTime register bit field.
(3) The FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data is internally sampled by active functional clock edge. FA21 value must be stored inside the AccessTime register bit field.
(4) P = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[6]
(5) H = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[6]
(6) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(7) For div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:

– GPMC_CLK frequency = GPMC_FCLK frequency

6.9.5.12.2.2 GPMC and NOR Flash Switching Characteristics – Asynchronous Mode

NO.	PARAMETER	DESCRIPTION	MODE[15]	MIN MAX 133 MHz[16]	UNIT
FA0	$t_{w(be[x]nV)}$	Pulse duration, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid time	Read	N[12]	ns
			Write	N[12]	
FA1	$t_{w(csnV)}$	Pulse duration, output chip select GPMC_CSn[i][13] low	Read	A[1]	ns
			Write	A[1]	
FA3	$t_{d(csnV-advnIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output address valid and address latch enable GPMC_ADVn_ALE invalid	Read	B[2]-2.55 B[2]+2.65	ns
			Write	B[2]-2.55 B[2]+2.65	
FA4	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output enable GPMC_OEn_REn invalid (Single read)	div_by_1_mode;	C[3]-2.55 C[3]+2.65	ns
FA9	$t_{d(aV-csnV)}$	Delay time, output address GPMC_A[27:1] valid to output chip select GPMC_CSn[i][13] valid	div_by_1_mode;	J[9]-2.55 J[9]+2.65	ns
FA10	$t_{d(be[x]nV-csnV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE, output upper-byte enable GPMC_BE1n valid to output chip select GPMC_CSn[i][13] valid	div_by_1_mode;	J[9]-2.55 J[9]+2.65	ns
FA12	$t_{d(csnV-advnV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output address valid and address latch enable GPMC_ADVn_ALE valid	div_by_1_mode;	K[10]-2.55 K[10]+2.65	ns
FA13	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output enable GPMC_OEn_REn valid	div_by_1_mode;	L[11]-2.55 L[11]+2.65	ns
FA16	$t_{w(aIV)}$	Pulse duration output address GPMC_A[26:1] invalid between 2 successive read and write accesses	div_by_1_mode;	G[7]	ns
FA18	$t_{d(csnV-oenIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output enable GPMC_OEn_REn invalid (Burst read)	div_by_1_mode;	I[8]-2.55 I[8]+2.65	ns
FA20	$t_{w(aV)}$	Pulse duration, output address GPMC_A[27:1] valid - 2nd, 3rd, and 4th accesses	div_by_1_mode;	D[4]	ns
FA25	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output write enable GPMC_WEn valid	div_by_1_mode;	E[5]-2.55 E[5]+2.65	ns
FA27	$t_{d(csnV-wenIV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output write enable GPMC_WEn invalid	div_by_1_mode;	F[6]-2.55 F[6]+2.65	ns
FA28	$t_{d(wenV-dV)}$	Delay time, output write enable GPMC_WEn valid to output data GPMC_AD[15:0] valid	div_by_1_mode;	2.65	ns
FA29	$t_{d(dV-csnV)}$	Delay time, output data GPMC_AD[15:0] valid to output chip select GPMC_CSn[i][13] valid	div_by_1_mode;	J[9]-2.55 J[9]+2.65	ns
FA37	$t_{d(oenV-aIV)}$	Delay time, output enable GPMC_OEn_REn valid to output address GPMC_AD[15:0] phase end	div_by_1_mode;	2.65	ns

(1) For single read: A = (CSRdOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For single write: A = (CSWrOffTime - CSOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst read: A = (CSRdOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
For burst write: A = (CSWrOffTime - CSOnTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
with n being the page burst access number
(2) For reading: B = ((ADVRdOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
For writing: B = ((ADVWrOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(3) C = ((OEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(4) D = PageBurstAccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[14]
(5) E = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(6) F = ((WEOffTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]

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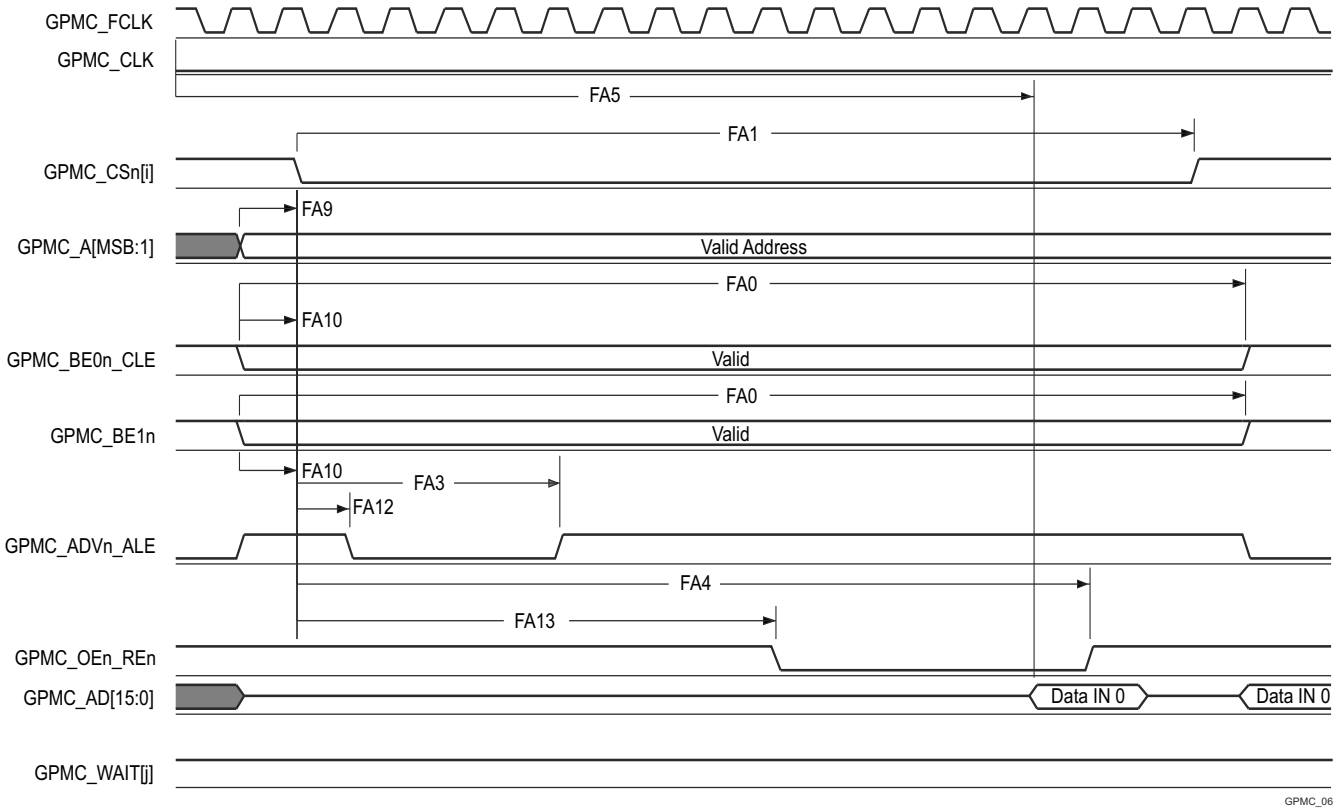
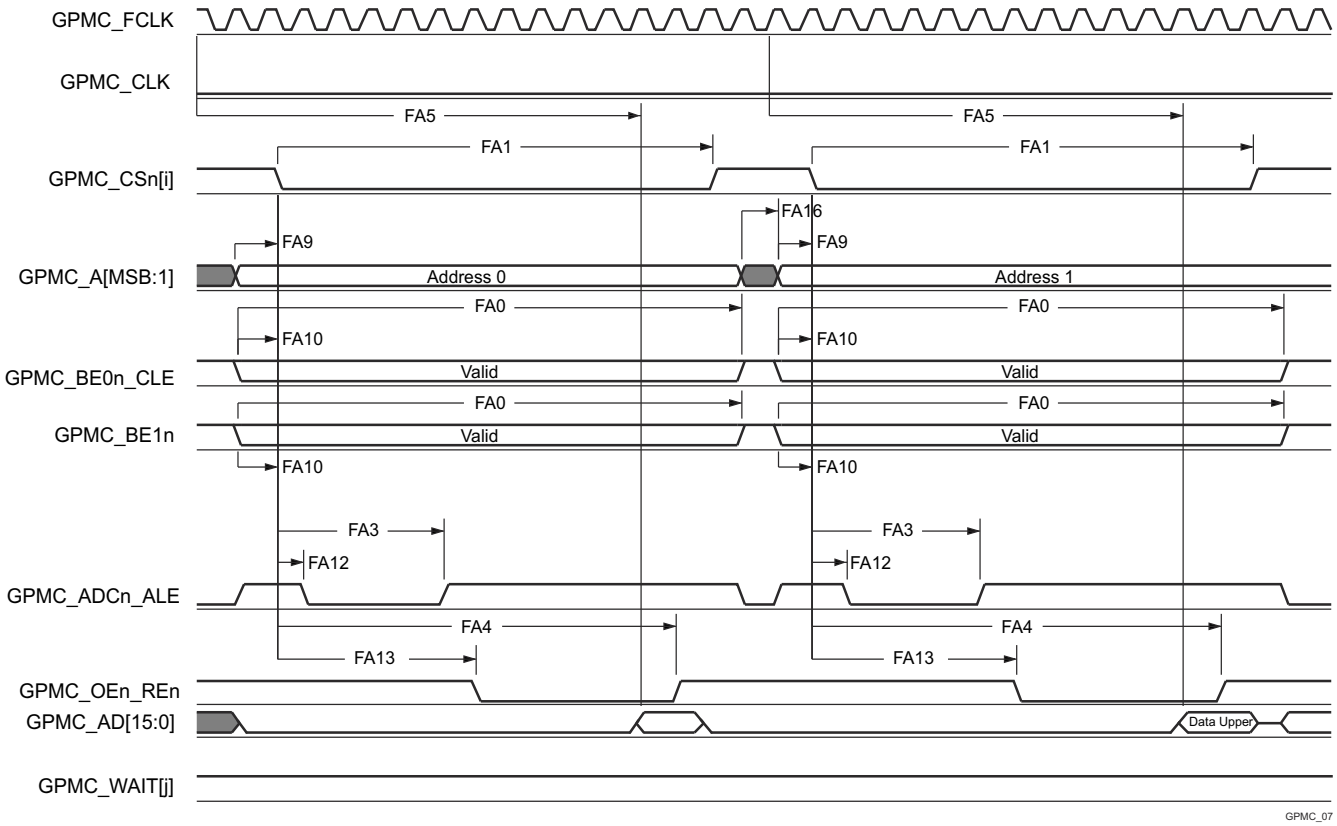
(7) G = Cycle2CycleDelay × GPMC_FCLK(14)
(8) I = ((OEOffTime + (n - 1) × PageBurstAccessTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
(9) J = (CSOnTime × (TimeParaGranularity + 1) + 0.5 × CSExtraDelay) × GPMC_FCLK(14)
(10) K = ((ADVOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
(11) L = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK(14)
(12) For single read: N = RdCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For single write: N = WrCycleTime × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst read: N = (RdCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
For burst write: N = (WrCycleTime + (n - 1) × PageBurstAccessTime) × (TimeParaGranularity + 1) × GPMC_FCLK(14)
(13) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(15) For div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

(16) For 133 MHz:
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = MAIN_PLL0_HSDIV3_CLKOUT



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

図 6-68. GPMC and NOR Flash — Asynchronous Read — Single Word



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.

C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

図 6-69. GPMC and NOR Flash — Asynchronous Read — 32–Bit

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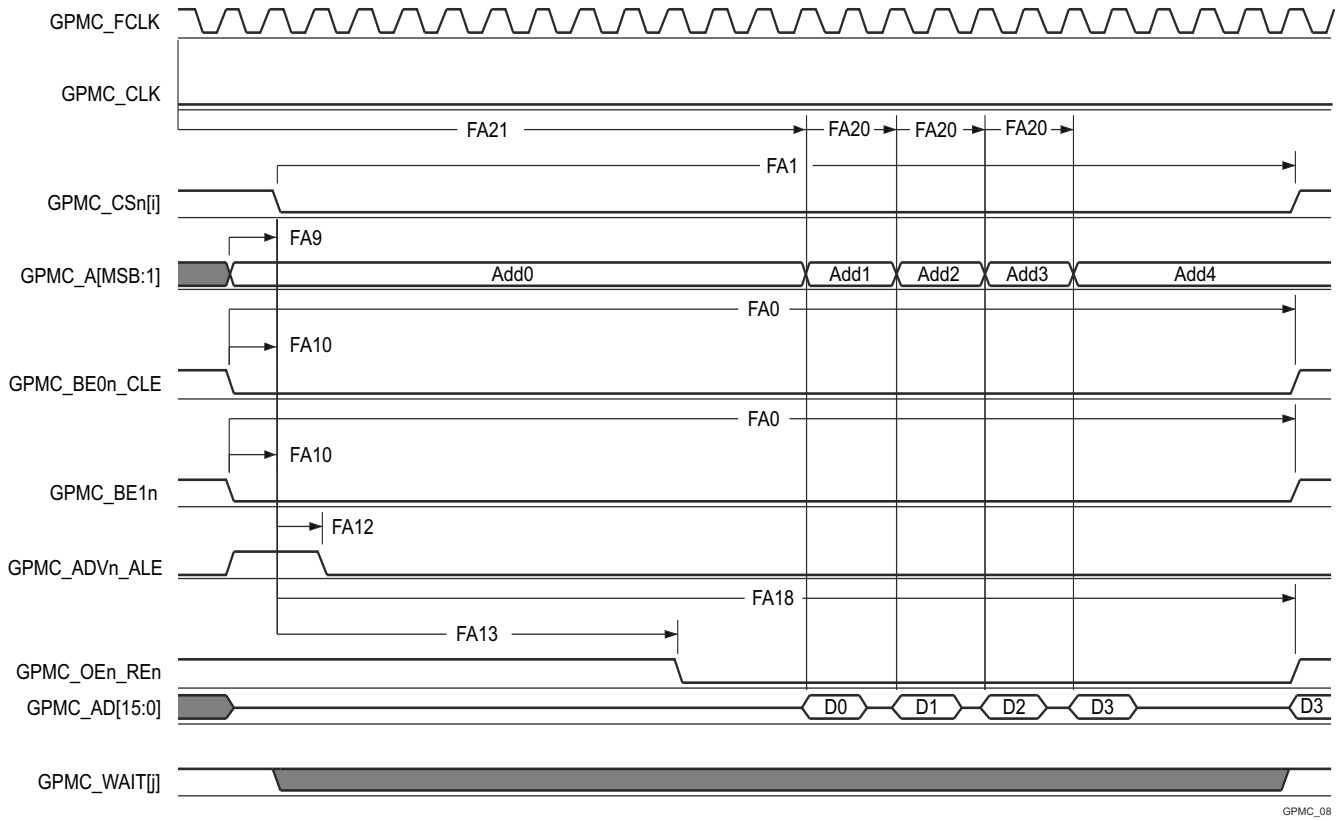


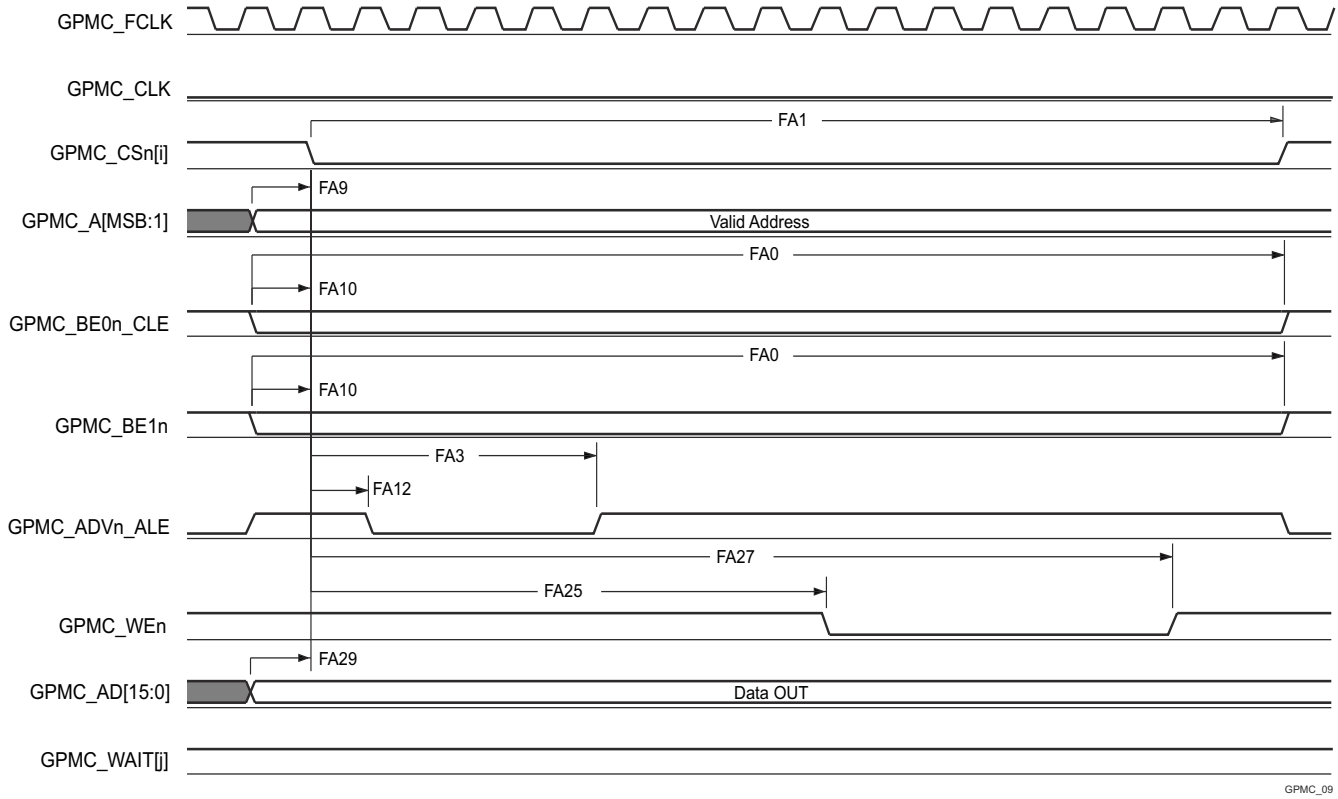
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

B. FA21 parameter illustrates amount of time required to internally sample first input page data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA21 functional clock cycles, first input page data will be internally sampled by active functional clock edge. FA21 calculation must be stored inside AccessTime register bits field.

C. FA20 parameter illustrates amount of time required to internally sample successive input page data. It is expressed in number of GPMC functional clock cycles. After each access to input page data, next input page data will be internally sampled by active functional clock edge after FA20 functional clock cycles. FA20 is also the duration of address phases for successive input page data (excluding first input page data). FA20 value must be stored in PageBurstAccessTime register bits field.

D. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

図 6-70. GPMC and NOR Flash — Asynchronous Read — Page Mode 4x16–Bit



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

図 6-71. GPMC and NOR Flash — Asynchronous Write — Single Word

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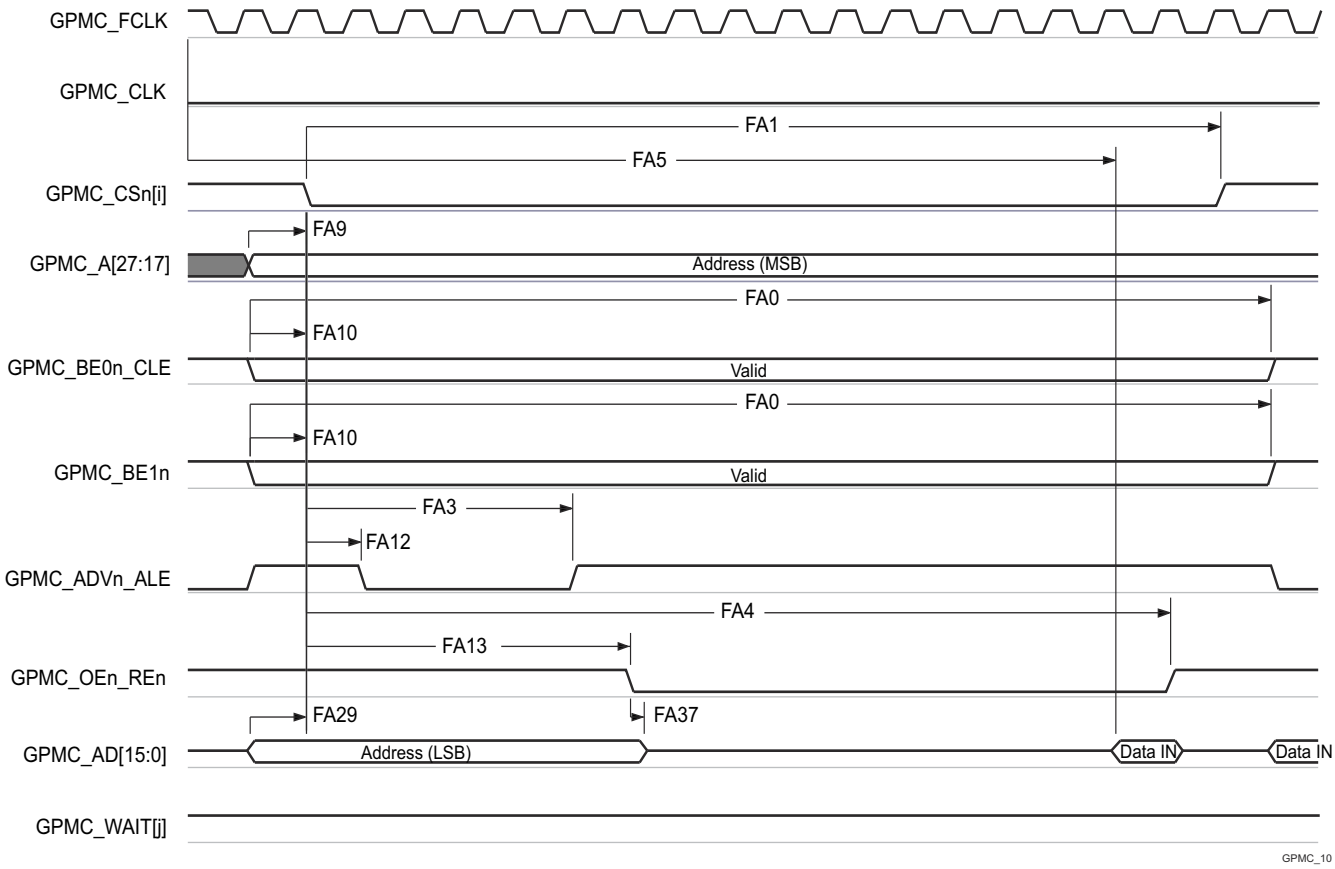
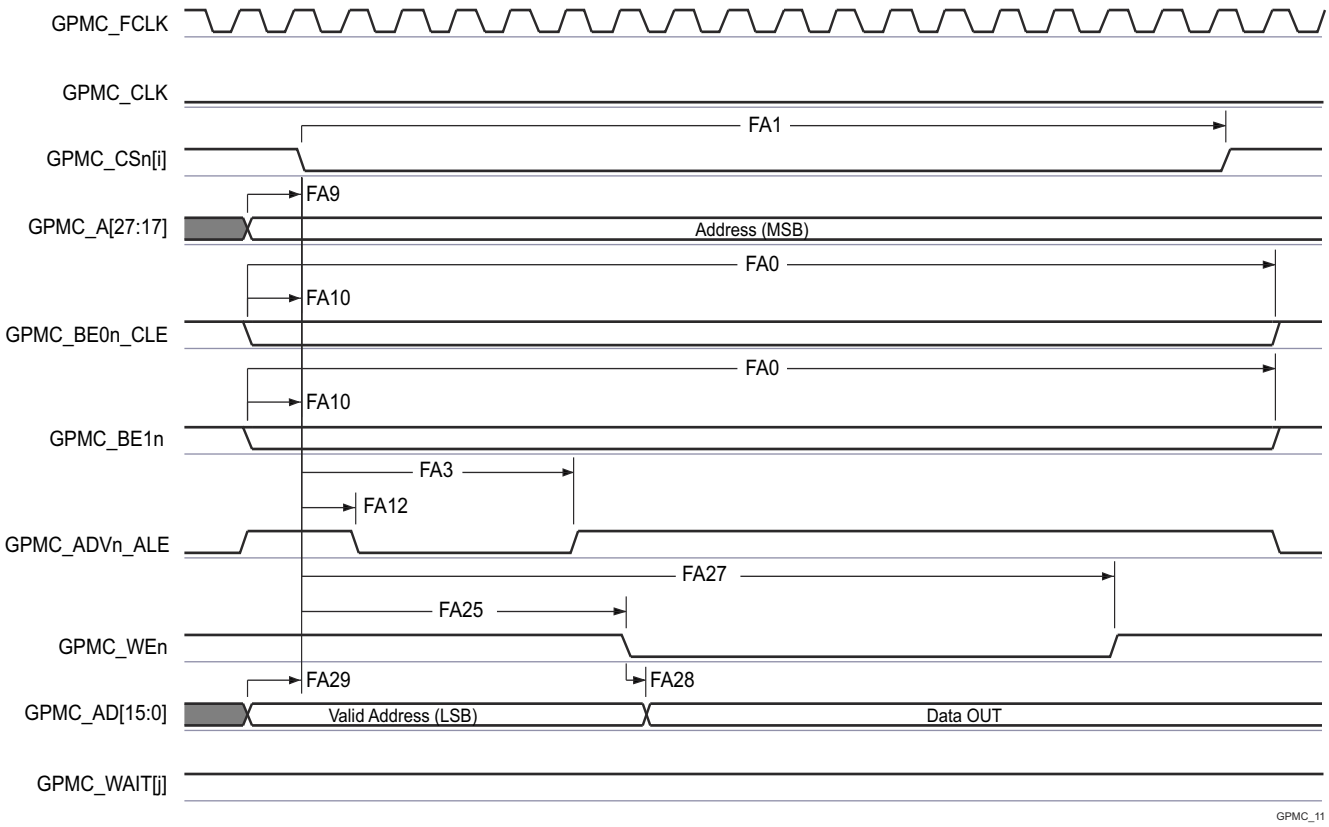


A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.
B. FA5 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after FA5 functional clock cycles, input data will be internally sampled by active functional clock edge. FA5 value must be stored inside AccessTime register bits field.
C. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.

図 6-72. GPMC and Multiplexed NOR Flash — Asynchronous Read — Single Word



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

図 6-73. GPMC and Multiplexed NOR Flash — Asynchronous Write — Single Word

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6.9.5.12.3 GPMC and NAND Flash — Asynchronous Mode

セクション 6.9.5.12.3.1 and セクション 6.9.5.12.3.2 assume testing over the recommended operating conditions and electrical characteristic conditions below (see 図 6-74 through 図 6-77).

6.9.5.12.3.1 GPMC and NAND Flash Timing Requirements – Asynchronous Mode

NO.			MODE[4]	MIN	MAX	UNIT
				133 MHz[5]		
GNF12[1]	$t_{acc(d)}$	Access time, input data GPMC_AD[15:0][3]	div_by_1_mode;		J[2]	ns

(1) The GNF12 parameter illustrates the amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of the read cycle and after GNF12 functional clock cycles, input data is internally sampled by the active functional clock edge. The GNF12 value must be stored inside AccessTime register bit field.
(2) J = AccessTime × (TimeParaGranularity + 1) × GPMC_FCLK[3]
(3) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(4) For div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

(5) For 133 MHz:
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = MAIN_PLL0_HSDIV3_CLKOUT

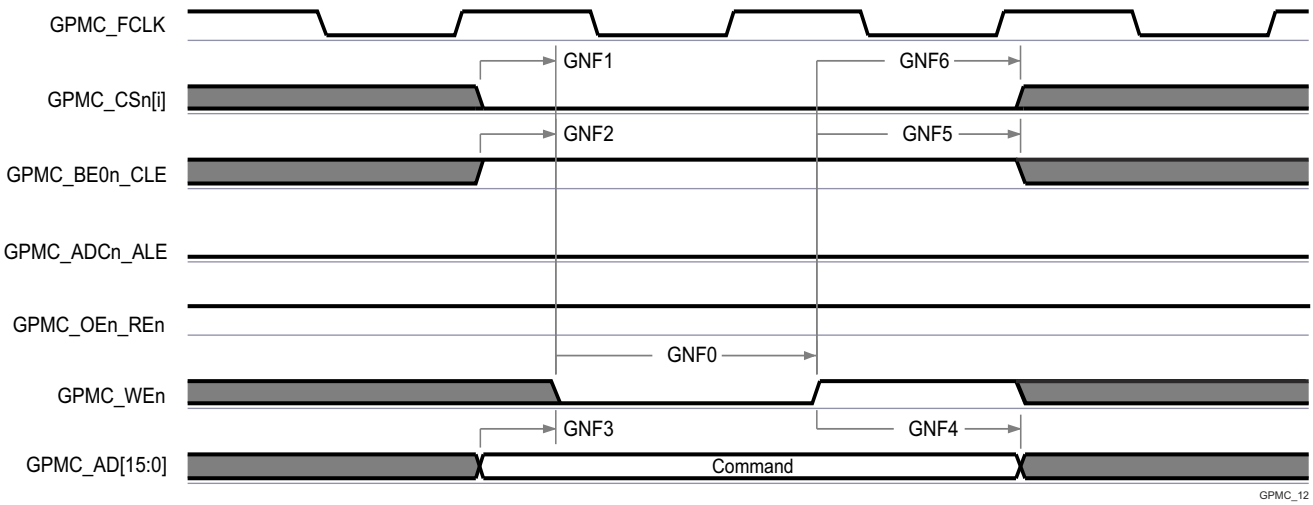
6.9.5.12.3.2 GPMC and NAND Flash Switching Characteristics – Asynchronous Mode

NO.	PARAMETER		MODE[15]	MIN	MAX	UNIT
				133 MHz[16]		
GNF0	$t_{w(wenV)}$	Pulse duration, output write enable GPMC_WEn valid	div_by_1_mode;	A[1]		ns
GNF1	$t_{d(csnV-wenV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output write enable GPMC_WEn valid	div_by_1_mode;	B[2]-2.55	B[2]+2.65	ns
GNF2	$t_{w(cleH-wenV)}$	Delay time, output lower-byte enable and command latch enable GPMC_BE0n_CLE high to output write enable GPMC_WEn valid	div_by_1_mode;	C[3]-2.55	C[3]+2.65	ns
GNF3	$t_{w(wenV-dV)}$	Delay time, output data GPMC_AD[15:0] valid to output write enable GPMC_WEn valid	div_by_1_mode;	D[4]-2.55	D[4]+2.65	ns
GNF4	$t_{w(wenIV-dIV)}$	Delay time, output write enable GPMC_WEn invalid to output data GPMC_AD[15:0] invalid	div_by_1_mode;	E[5]-2.55	E[5]+2.65	ns
GNF5	$t_{w(wenIV-cleIV)}$	Delay time, output write enable GPMC_WEn invalid to output lower-byte enable and command latch enable GPMC_BE0n_CLE invalid	div_by_1_mode;	F[6]-2.55	F[6]+2.65	ns
GNF6	$t_{w(wenIV-CSn[i]V)}$	Delay time, output write enable GPMC_WEn invalid to output chip select GPMC_CSn[i][13] invalid	div_by_1_mode;	G[7]-2.55	G[7]+2.65	ns
GNF7	$t_{w(aleH-wenV)}$	Delay time, output address valid and address latch enable GPMC_ADVn_ALE high to output write enable GPMC_WEn valid	div_by_1_mode;	C[3]-2.55	C[3]+2.65	ns
GNF8	$t_{w(wenIV-aleIV)}$	Delay time, output write enable GPMC_WEn invalid to output address valid and address latch enable GPMC_ADVn_ALE invalid	div_by_1_mode;	F[6]-2.55	F[6]+2.65	ns
GNF9	$t_{c(wen)}$	Cycle time, write	div_by_1_mode;		H[8]	ns
GNF10	$t_{d(csnV-oenV)}$	Delay time, output chip select GPMC_CSn[i][13] valid to output enable GPMC_OEn_REn valid	div_by_1_mode;	I[9]-2.55	I[9]+2.65	ns
GNF13	$t_{w(oenV)}$	Pulse duration, output enable GPMC_OEn_REn valid	div_by_1_mode;		K[10]	ns
GNF14	$t_{c(oen)}$	Cycle time, read	div_by_1_mode;	L[11]		ns

NO.	PARAMETER		MODE[15]	MIN	MAX	UNIT
				133 MHz[16]		
GNF15	$t_{w(oenIV-CSn[i]V)}$	Delay time, output enable GPMC_OEn_REn invalid to output chip select GPMC_CSn[i][13] invalid	div_by_1_mode;	M[12]-2.55	M[12]+2.65	ns

(1) A = (WEOffTime - WEOnTime) × (TimeParaGranularity + 1) × GPMC_FCLK[14]
(2) B = ((WEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(3) C = ((WEOnTime - ADVOnTime) × (TimeParaGranularity + 1) + 0.5 × (WEExtraDelay - ADVExtraDelay)) × GPMC_FCLK[14]
(4) D = (WEOnTime × (TimeParaGranularity + 1) + 0.5 × WEExtraDelay) × GPMC_FCLK[14]
(5) E = ((WrCycleTime - WEOffTime) × (TimeParaGranularity + 1) - 0.5 × WEExtraDelay) × GPMC_FCLK[14]
(6) F = ((ADVWrOffTime - WEOffTime) × (TimeParaGranularity + 1) + 0.5 × (ADVExtraDelay - WEExtraDelay)) × GPMC_FCLK[14]
(7) G = ((CSWrOffTime - WEOffTime) × (TimeParaGranularity + 1) + 0.5 × (CSExtraDelay - WEExtraDelay)) × GPMC_FCLK[14]
(8) H = WrCycleTime × (1 + TimeParaGranularity) × GPMC_FCLK[14]
(9) I = ((OEOnTime - CSOnTime) × (TimeParaGranularity + 1) + 0.5 × (OEExtraDelay - CSExtraDelay)) × GPMC_FCLK[14]
(10) K = (OEOffTime - OEOnTime) × (1 + TimeParaGranularity) × GPMC_FCLK[14]
(11) L = RdCycleTime × (1 + TimeParaGranularity) × GPMC_FCLK[14]
(12) M = ((CSRdOffTime - OEOffTime) × (TimeParaGranularity + 1) + 0.5 × (CSExtraDelay - OEExtraDelay)) × GPMC_FCLK[14]
(13) In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.
(14) GPMC_FCLK is general-purpose memory controller internal functional clock period in ns.
(15) For div_by_1_mode:
- GPMC_CONFIG1_i Register: GPMCFCLKDIVIDER = 0h:
  - GPMC_CLK frequency = GPMC_FCLK frequency

(16) For 133 MHz:
- CTRLMMR_GPMC_CLKSEL[1-0] CLK_SEL = 00 = MAIN_PLL0_HSDIV3_CLKOUT



A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

図 6-74. GPMC and NAND Flash — Command Latch Cycle

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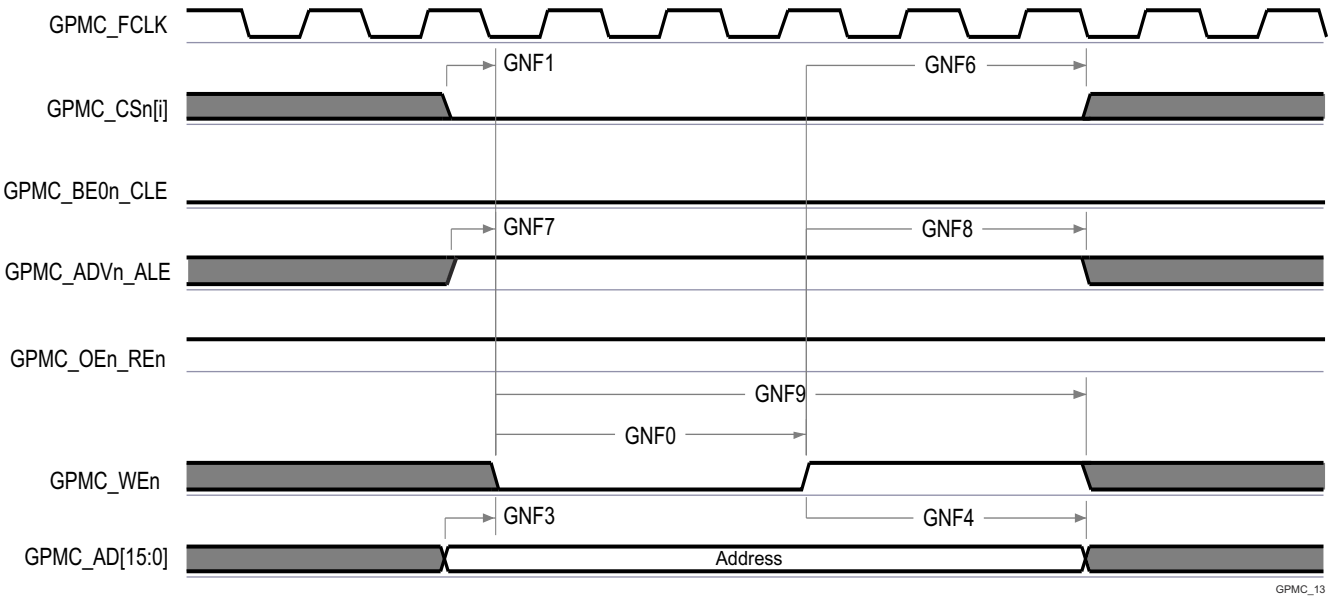
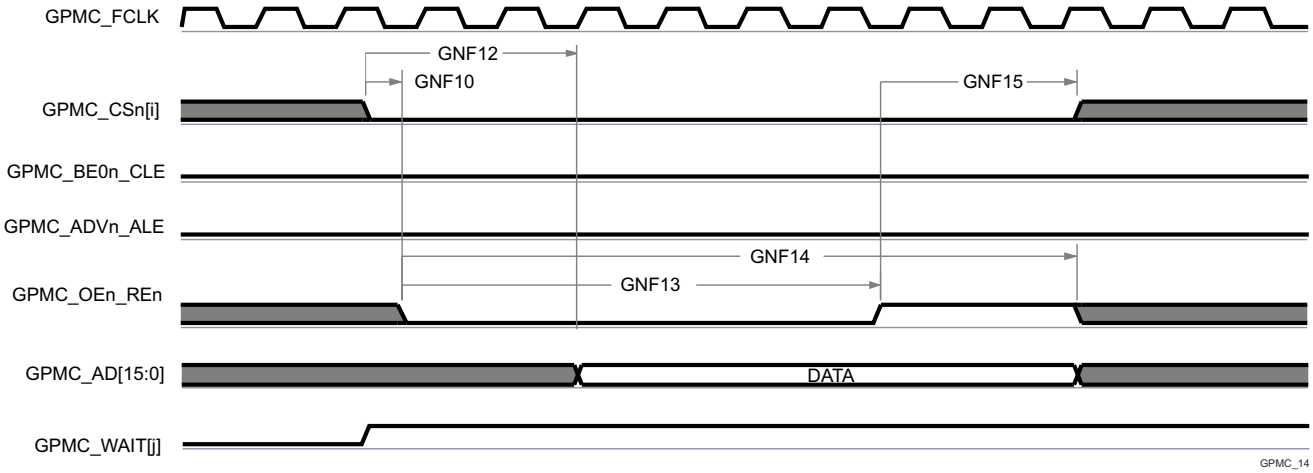


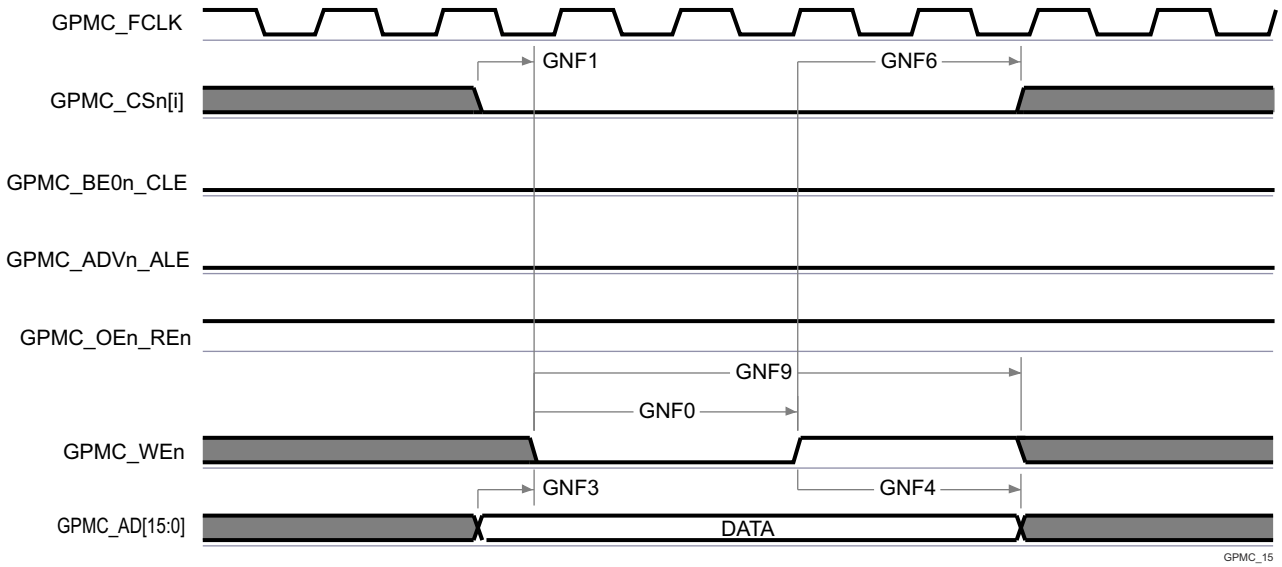
A. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

図 6-75. GPMC and NAND Flash — Address Latch Cycle



A. GNF12 parameter illustrates amount of time required to internally sample input data. It is expressed in number of GPMC functional clock cycles. From start of read cycle and after GNF12 functional clock cycles, input data will be internally sampled by active functional clock edge. GNF12 value must be stored inside AccessTime register bits field.
B. GPMC_FCLK is an internal clock (GPMC functional clock) not provided externally.
C. In GPMC_CSn[i], i is equal to 0, 1, 2 or 3. In GPMC_WAIT[j], j is equal to 0, 1, 2, or 3.

図 6-76. GPMC and NAND Flash — Data Read Cycle



A. `In GPMC_CSn[i], i is equal to 0, 1, 2 or 3.

図 6-77. GPMC and NAND Flash — Data Write Cycle

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

6.9.5.12.4 GPMC0 IOSET

表 6-58 present the specific groupings of signals (IOSET) for use with GPMC0.

表 6-58. GPMC0 IOSET

Signals	IOSET1		IOSET2	
	BALL NAME	MUX	BALL NAME	MUX
GPMC0_WAIT2	MDIO0_MDC	8	MDIO0_MDC	8
GPMC0_BE1n	PRG1_PRU0_GPO0	8	RGMII6_RD1	8
GPMC0_WAIT0	PRG1_PRU0_GPO1	8	PRG1_PRU0_GPO1	8
GPMC0_WAIT1	PRG1_PRU0_GPO2	8	PRG1_PRU0_GPO2	8
GPMC0_DIR	PRG1_PRU0_GPO3	8	PRG1_PRU0_GPO3	8
GPMC0_CSn2	PRG1_PRU0_GPO4	8	PRG1_PRU0_GPO4	8
GPMC0_WEn	PRG1_PRU0_GPO5	8	PRG1_PRU0_GPO5	8
GPMC0_CSn3	PRG1_PRU0_GPO6	8	PRG1_PRU0_GPO6	8
GPMC0_OEn_REn	PRG1_PRU0_GPO8	8	PRG1_PRU0_GPO8	8
GPMC0_ADVn_ALE	PRG1_PRU0_GPO9	8	PRG1_PRU0_GPO9	8
GPMC0_BE0n_CLE	PRG1_PRU0_GPO10	8	PRG1_PRU0_GPO10	8
GPMC0_WPn	PRG1_PRU1_GPO5	8	PRG1_PRU1_GPO5	8
GPMC0_CSn1	PRG1_PRU1_GPO8	8	PRG1_PRU1_GPO8	8
GPMC0_CSn0	PRG1_PRU1_GPO9	8	PRG1_PRU1_GPO9	8
GPMC0_CLKOUT	PRG1_PRU1_GPO10	8	PRG1_PRU1_GPO10	8
GPMC0_AD0	PRG0_PRU0_GPO5	8	PRG0_PRU0_GPO5	8
GPMC0_AD1	PRG0_PRU0_GPO7	8	PRG0_PRU0_GPO7	8
GPMC0_AD2	PRG0_PRU0_GPO8	8	PRG0_PRU0_GPO8	8
GPMC0_AD3	PRG0_PRU0_GPO9	8	PRG0_PRU0_GPO9	8
GPMC0_AD4	PRG0_PRU0_GPO10	8	PRG0_PRU0_GPO10	8
GPMC0_AD5	PRG0_PRU0_GPO17	8	PRG0_PRU0_GPO17	8

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表 6-58. GPMC0 IOSET (続き)

Signals	IOSET1		IOSET2	
	BALL NAME	MUX	BALL NAME	MUX
GPMC0_AD6	PRG0_PRU0_GPO18	8	PRG0_PRU0_GPO18	8
GPMC0_AD7	PRG0_PRU0_GPO19	8	PRG0_PRU0_GPO19	8
GPMC0_AD8	PRG0_PRU1_GPO5	8	PRG0_PRU1_GPO5	8
GPMC0_AD9	PRG0_PRU1_GPO7	8	PRG0_PRU1_GPO7	8
GPMC0_AD10	PRG0_PRU1_GPO8	8	PRG0_PRU1_GPO8	8
GPMC0_AD11	PRG0_PRU1_GPO9	8	PRG0_PRU1_GPO9	8
GPMC0_AD12	PRG0_PRU1_GPO10	8	PRG0_PRU1_GPO10	8
GPMC0_AD13	PRG0_PRU1_GPO17	8	PRG0_PRU1_GPO17	8
GPMC0_AD14	PRG0_PRU1_GPO18	8	PRG0_PRU1_GPO18	8
GPMC0_AD15	PRG0_PRU1_GPO19	8	PRG0_PRU1_GPO19	8
GPMC0_A0	PRG0_MDIO0_MDC	8	PRG0_MDIO0_MDC	8
GPMC0_A1	RGMII5_TX_CTL	8	RGMII5_TX_CTL	8
GPMC0_A2	RGMII5_RX_CTL	8	RGMII5_RX_CTL	8
GPMC0_A3	RGMII5_TD3	8	RGMII5_TD3	8
GPMC0_A4	RGMII5_TD2	8	RGMII5_TD2	8
GPMC0_A5	RGMII5_TD1	8	RGMII5_TD1	8
GPMC0_A6	RGMII5_TD0	8	RGMII5_TD0	8
GPMC0_A7	RGMII5_TXC	8	RGMII5_TXC	8
GPMC0_A8	RGMII5_RXC	8	RGMII5_RXC	8
GPMC0_A9	RGMII5_RD3	8	RGMII5_RD3	8
GPMC0_A10	RGMII5_RD2	8	RGMII5_RD2	8
GPMC0_A11	RGMII5_RD1	8	RGMII5_RD1	8
GPMC0_A12	RGMII5_RD0	8	RGMII5_RD0	8
GPMC0_A13	RGMII6_TX_CTL	8	RGMII6_TX_CTL	8
GPMC0_A14	RGMII6_RX_CTL	8	RGMII6_RX_CTL	8
GPMC0_A15	RGMII6_TD3	8	RGMII6_TD3	8
GPMC0_A16	RGMII6_TD2	8	RGMII6_TD2	8
GPMC0_A17	RGMII6_TD1	8	RGMII6_TD1	8
GPMC0_A18	RGMII6_TD0	8	RGMII6_TD0	8
GPMC0_A19	RGMII6_TXC	8	RGMII6_TXC	8
GPMC0_A20	RGMII6_RXC	8	RGMII6_RXC	8
GPMC0_A21	RGMII6_RD3	8	RGMII6_RD3	8
GPMC0_A22	RGMII6_RD2	8	RGMII6_RD2	8
GPMC0_A23	PRG0_PRU1_GPO2	8	PRG0_PRU1_GPO2	8
GPMC0_A24	PRG0_PRU1_GPO4	8	PRG0_PRU1_GPO4	8
GPMC0_A25	PRG0_PRU1_GPO6	8	PRG0_PRU1_GPO6	8
GPMC0_A26	PRG0_PRU1_GPO11	8	PRG0_PRU1_GPO11	8
GPMC0_A27	PRG0_MDIO0_MDIO	8	PRG0_MDIO0_MDIO	8
GPMC0_WAIT3	MDIO0_MDIO	8	MDIO0_MDIO	8

6.9.5.13 HyperBus

For more details about features and additional description information on the device HyperBus, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

セクション 6.9.5.13.1, セクション 6.9.5.13.2, and セクション 6.9.5.13.3 assume testing over the recommended operating conditions and electrical characteristic conditions (see 図 6-78, 図 6-79, and 図 6-80).

表 6-59 represents HyperBus timing conditions.

表 6-59. HyperBus Timing Conditions

PARAMETER	DESCRIPTION		MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		2	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance		1.5	10	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch between traces	CK and CKn; RWDS and DQ[7:0]		10	ps
		CK/CKn and RWDS; CK/CKn and CSn		200	ps
		CK/CKn and DQ[7:0]		35	ps
		RESETn and CSn[1:0]		340	ps

6.9.5.13.1 Timing Requirements for HyperBus

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
D1	$t_{w(resetnL)}$	Pulse duration, HYPERBUS0_RESETn low		200		ns
D2	$t_{w(csnL)}$	Pulse duration, HYPERBUS0_CSn[1:0] low			1000	ns
D3	$t_{d(resetnH-csnL)}$	Delay time, HYPERBUS0_RESETn rising edge to HYPERBUS0_CSn[1:0] falling edge		200.34		ns
D4	$t_{d(csnL-rwdsL)}$	Delay time, HYPERBUS0_CSn[1:0] falling edge to HYPERBUS0_RWDS falling edge	166 MHz		186	ns
			100 MHz		182	ns
D5	$t_{skn(rwdsV-dV)}$	Input skew, HYPERBUS0_RWDS transition to HYPERBUS0_DQ[7:0] valid	166 MHz	-0.46	0.46	ns
LFD5			100 MHz	-0.81	0.81	ns

6.9.5.13.2 HyperBus 166 MHz Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
D6	$t_{c(ck/ckn)}$	Cycle time, HYPERBUS0_CK/CKn	6		ns
D7	$t_{w(ck/ckn)}$	Pulse duration, HYPERBUS0_CK/CKn high or low	2.85		ns
D8	$t_{w(csnH)}$	Pulse duration, HYPERBUS0_CSn[1:0] invalid between operations	6		ns
D9	$t_{d(csnL-ckH/cknL)}$	Delay time, HYPERBUS0_CSn[1:0] falling edge to first HYPERBUS0_CK rising (HYPERBUS0_CKn falling) edge		-3.28	ns
D10	$t_{d(ckL/cknH-csnH)}$	Delay time, last falling HYPERBUS0_CK (rising HYPERBUS0_Ckn) edge to HYPERBUS0_CSn[1:0] rising	0.28		ns
D11	$t_{d(ckV/cknV-rwdsV)}$	Delay time, HYPERBUS0_CK/CKn transition to HYPERBUS0_RWDS valid	0.68	2.14	ns
D12	$t_{d(ckV-dV)}$	Delay time, HYPERBUS0_CK/CKn transition to HYPERBUS0_DQ[7:0] valid	0.71	2.3	ns

6.9.5.13.3 HyperBus 100 MHz Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
LFD6	$t_{c(ck/ckn)}$	Cycle time, HYPERBUS0_CK/CKn	10		ns
LFD7	$t_{w(ck/ckn)}$	Pulse duration, HYPERBUS0_CK/CKn high or low	4.88		ns
LFD8	$t_{w(csnH)}$	Pulse duration, HYPERBUS0_CSn[1:0] invalid between operations	10		ns

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NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
LFD9	$t_{d(csnL-ckH/cknL)}$	Delay time, HYPERBUS0_CSn[1:0] falling edge to first HYPERBUS0_CK rising (HYPERBUS0_CKn falling) edge		-3.33	ns
LFD10	$t_{d(ckL/cknH-csnH)}$	Delay time, last falling HYPERBUS0_CK (rising HYPERBUS0_Ckn) edge to HYPERBUS0_CSn[1:0] rising	0.33		ns
LFD11	$t_{d(ckV/cknV-rwdsV)}$	Delay time, HYPERBUS0_CK/CKn transition to HYPERBUS0_RWDS valid	1.13	3.68	ns
LFD12	$t_{d(ckV/cknV-dV)}$	Delay time, HYPERBUS0_CK/CKn transition to HYPERBUS0_DQ[7:0] valid	1.16	3.84	ns

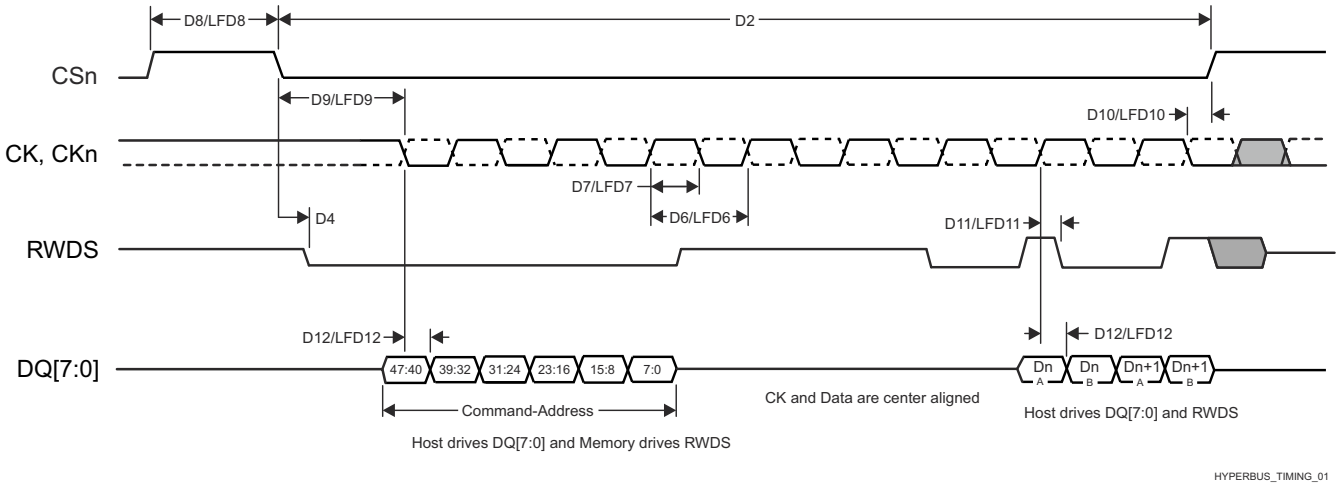

図 6-78. HyperBus Timing Diagrams – Transmitter Mode

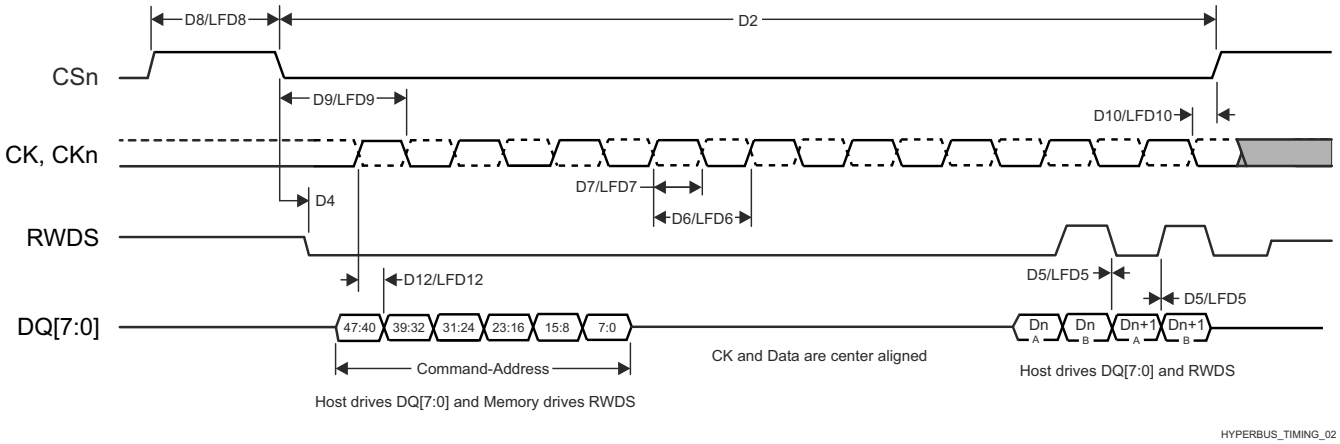

図 6-79. HyperBus Timing Diagrams – Receiver Mode

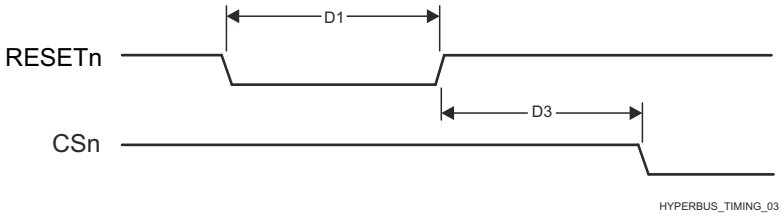

図 6-80. HyperBus Timing Diagrams – Reset

For more information, see *HyperBus Interface* section in *Peripherals* chapter in the device TRM.

6.9.5.14 I2C

The Inter-IC module is compliant with the Philips I2C Bus Specification, revision 2.1. Refer to the specification for timing details for all but rise/fall time parameters.

Philips I2C specification rise/fall timings apply only to MCU_I2C0, WKUP_I2C0, and I2C[0-1]. All other instances of I2C use standard LVCMOS buffers to emulate open-drain buffers, and their rise/fall times should be referenced using the device IBIS model.

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

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6.9.5.15 I3C

For more details about features and additional description information on the device Inter-Integrated Circuit, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

表 6-60, 表 6-61 , 表 6-62, 図 6-81, 表 6-64, 図 6-82, and 図 6-83 assume testing over the recommended operating conditions and electrical characteristic conditions.

表 6-60. I3C Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.2276	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance		50	pF

表 6-61. I3C Open Drain Timing Requirements

see 図 6-81

NO.			MODE	MIN	MAX	UNIT
OD4	$t_{su(sdaV-sclH)}$	Setup time, SDA valid before SCL rising edge	Master	3		ns

表 6-62. I3C Open Drain Switching Characteristics

see 図 6-81

NO.	PARAMETER		MODE	MIN	MAX	UNIT
OD1	$t_{w(sclL_od)}$	Pulse duration, SCL low	Master	200		ns
	$t_{w(sclL_od_dig)}$			$t_{w(sclL_od)}$ + $t_{f(sda_od), min}$		ns
OD2	$t_{w(sclH_od)}$	Pulse duration, SCL high	Master		41	ns
	$t_{w(sclH_od_dig)}$				$t_{w(sclH_od)}$ + $t_{f(scl)}$	ns
OD3	$t_{f(sda_od)}$	Fall time, SDA	Master	$t_{f(scl)}$	12	ns
OD5	$t_{d(sclL-START)}$	Delay time, SCL low after START (S) condition	Master, ENTAS0	38.4	1000	ns
			Master, ENTAS1	38.4	100000	ns
			Master, ENTAS2	38.4	2000000	ns
			Master, ENTAS3	38.4	50000000	ns
OD6	$t_{d(sclH-STOP)}$	Delay time, SCL high before STOP (P) condition	Master	$t_{d(sclV), min}$ / 2		ns
OD7	$t_{w(mmoverlap)}$	Pulse duration, current master to secondary master overlap time during handoff	Master	$t_{w(sclL_od_dig)}$		ns
OD8	$t_{w(aval)}$	Pulse duration, Bus Available condition	Master	1000		ns
OD9	$t_{w(idle)}$	Pulse duration, Bus Idle condition	Master	1000000		ns
OD10	$t_{w(mmlock)}$	Pulse duration, new master not driving SDA low	Master	$t_{w(aval)}$		ns

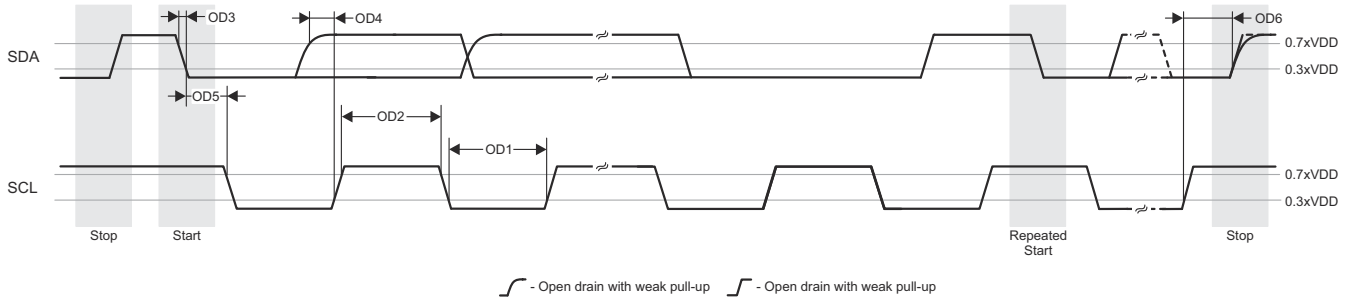

図 6-81. I3C Open Drain Timing Requirements

表 6-63. I3C Push-Pull Timing Requirements - SDR and HDR-DDR Modes

図 6-82 and 図 6-83

NO.			MODE	MIN	MAX	UNIT
D8	$t_{h(sclV-sdaV)}$	Hold time, SDA valid after SCL transition	Master	$t_{r(scl)}$ + 3 and $t_{f(scl)}$ + 3		ns
D9	$t_{su(sdaV-sclV)}$	Seutp time, SDA valid before SCL transition	Master	3		ns

表 6-64. I3C Push-Pull Switching Characteristics - SDR and HDR-DDR Modes

see 図 6-83, 図 6-82

NO.	PARAMETER		MODE	MIN	MAX	UNIT
D1	$t_{c(scl)}$	Cycle time, SCL	Master	80	100000	ns
D2	$t_{w(sclL)}$	Pulse duration, SCL low	Master	24		ns
	$t_{w(sclL_dig)}$			32		ns
D4	$t_{w(sclH)}$	Pulse duration, SCL high	Master	24		ns
	$t_{w(sclH_dig)}$			32		ns
D6	$t_{r(scl)}$	Rise time, SCL	Master	150 × 1 / $t_{c(scl)}$	60	ns
D7	$t_{f(scl)}$	Fall time, SCL	Master	150 × 1 / $t_{c(scl)}$	60	ns
D10	$t_{d(Sr-sclV)}$	Delay time, SCL valid after Repeated START (Sr)	Master	$t_{d(sclV-START),\ min}$		ns
D11	$t_{d(sclV-Sr)}$	Delay time, Repeated START (Sr) after SCL valid	Master	$t_{d(sclV-START),\ min}$ / 2		ns

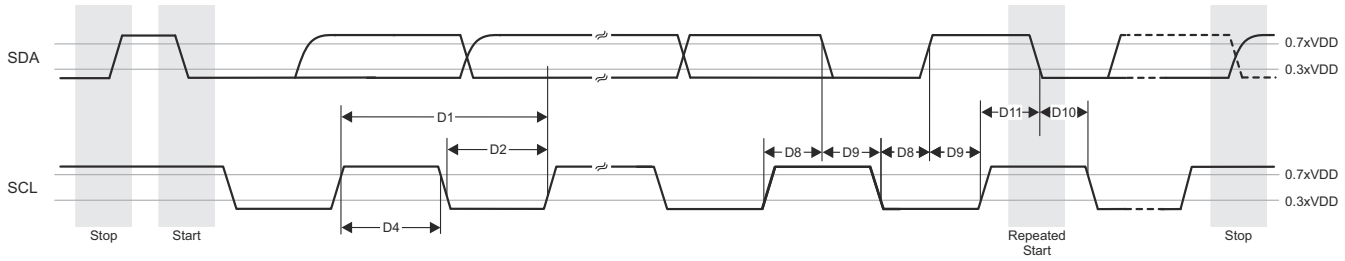

図 6-82. I3C Push-Pull Timing Requirements - HDR-DDR Mode

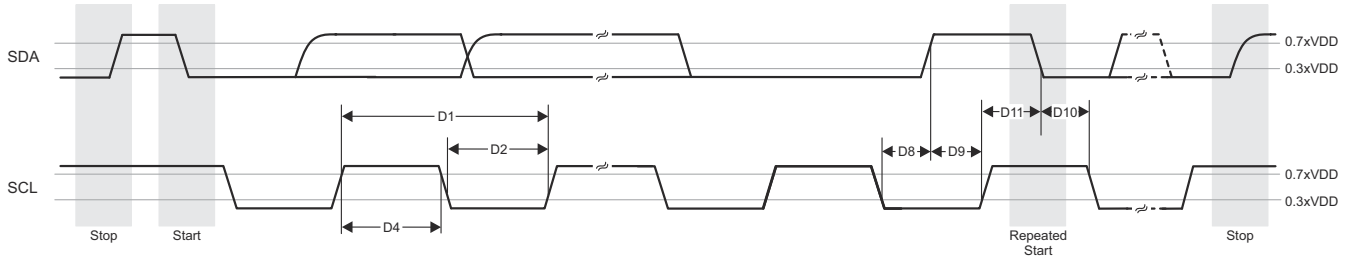

図 6-83. I3C Push-Pull Timing Requirements - SDR Mode

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6.9.5.16 MCAN

For more details about features and additional description information on the device Controller Area Network Interface, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

注

The device has multiple MCAN modules. MCANn is a generic prefix applied to MCAN signal names, where n represents the specific MCAN module.

表 6-65. MCAN Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	2	15	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	5	20	pF

表 6-66. MCAN Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
M1	$t_{d(MCAN_TX)}$	Delay time, transmit shift register to MCANn_TX pin(1)		10	ns
M2	$t_{d(MCAN_RX)}$	Delay time, MCANn_RX pin to receive shift register(1)		10	ns

(1) n is [0:13] in MCANn_* or [0:1] in MCU_MCANn_*

For more information, see *Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

6.9.5.17 MCASP

For more details about features and additional description information on the device Multichannel Audio Serial Port, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

表 6-68 and 図 6-84 present timing requirements for MCASP0 to MCASP11.

表 6-67 represents MCASP timing conditions.

表 6-67. MCASP Timing Conditions

PARAMETER		MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.7	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	10	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	100	1100	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

表 6-68. MCASP Timing Requirements

NO.			MODE(1)	MIN	MAX	UNIT
ASP1	$t_{c(AHCLKRX)}$	Cycle time, MCASP[x]_AHCLKR/X		15.26		ns
ASP2	$t_{w(AHCLKRX)}$	Pulse duration, MCASP[x]_AHCLKR/X high or low		0.5P(2) - 1.53		ns
ASP3	$t_{c(ACLKRX)}$	Cycle time, MCASP[x]_ACLKR/X		15.26		ns
ASP4	$t_{w(ACLKRX)}$	Pulse duration, MCASP[x]_ACLKR/X high or low		0.5R(3) - 1.53		ns
ASP5	$t_{su(AFSRX-ACLKRX)}$	Setup time, MCASP[x]_AFSR/X input valid before MCASP[x]_ACLKR/X	ACLKR/X int	12.3		ns
			ACLKR/X ext in/out	4		
ASP6	$t_{h(ACLKRX-AFSRX)}$	Hold time, MCASP[x]_AFSR/X input valid after MCASP[x]_ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in/out	1.6		
ASP7	$t_{su(AXR-ACLKRX)}$	Setup time, MCASP[x]_AXR input valid before MCASP[x]_ACLKR/X	ACLKR/X int	12.3		ns
			ACLKR/X ext in/out	4		
ASP8	$t_{h(ACLKRX-AXR)}$	Hold time, MCASP[x]_AXR input valid after MCASP[x]_ACLKR/X	ACLKR/X int	-1		ns
			ACLKR/X ext in/out	1.6		

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = AHCLKR/X period in ns.
(3) R = ACLKR/X period in ns.

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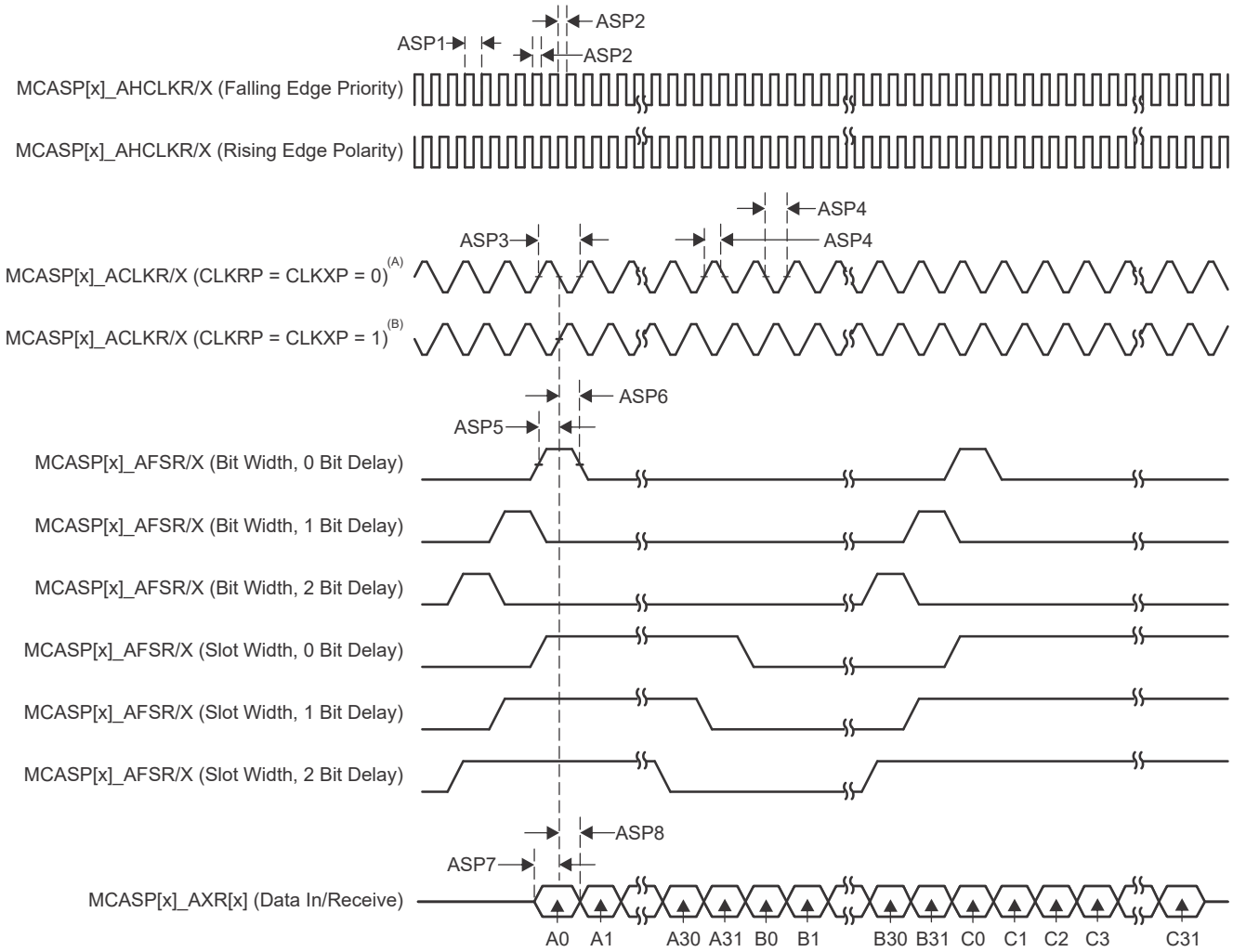

A. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

B. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

図 6-84. MCASP Input Timing

表 6-69 and 図 6-85 present switching characteristics over recommended operating conditions for MCASP0 to MCASP11.

表 6-69. MCASP Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE(1)	MIN	MAX	UNIT
ASP9	$t_{c(AHCLKRX)}$	Cycle time, MCASP[x]_AHCLKR/X		20		ns
ASP10	$t_{w(AHCLKRX)}$	Pulse duration, MCASP[x]_AHCLKR/X high or low		0.5P(2) - 2		ns
ASP11	$t_{c(ACLKRX)}$	Cycle time, MCASP[x]_ACLKR/X		20		ns
ASP12	$t_{w(ACLKRX)}$	Pulse duration, MCASP[x]_ACLKR/X high or low		0.5R(3) - 2		ns
ASP13	$t_{d(ACLKRX-AFSRX)}$	Delay time, MCASP[x]_ACLKR/X transmit edge to MCASP[x]_AFSR/X output valid	ACLKR/X int	0	7.25	ns
			ACLKR/X ext in/out	-15.28	12.84	
ASP14	$t_{d(ACLKX-AXR)}$	Delay time, MCASP[x]_ACLKX transmit edge to MCASP[x]_AXR output valid	ACLKR/X int	0	7.25	ns
			ACLKR/X ext in/out	-15.28	12.84	
ASP15	$t_{dis(ACLKX-AXR)}$	Disable time, MCASP[x]_ACLKX transmit edge to MCASP[x]_AXR output high impedance	ACLKR/X int	0	7.25	ns
			ACLKR/X ext in/out	-14.9	14	

(1) ACLKR internal: ACLKRCTL.CLKRM=1, PDIR.ACLKR = 1
ACLKR external input: ACLKRCTL.CLKRM=0, PDIR.ACLKR=0
ACLKR external output: ACLKRCTL.CLKRM=0, PDIR.ACLKR=1
ACLKX internal: ACLKXCTL.CLKXM=1, PDIR.ACLKX = 1
ACLKX external input: ACLKXCTL.CLKXM=0, PDIR.ACLKX=0
ACLKX external output: ACLKXCTL.CLKXM=0, PDIR.ACLKX=1
(2) P = AHCLKR/X period in ns.
(3) R = ACLKR/X period in ns.

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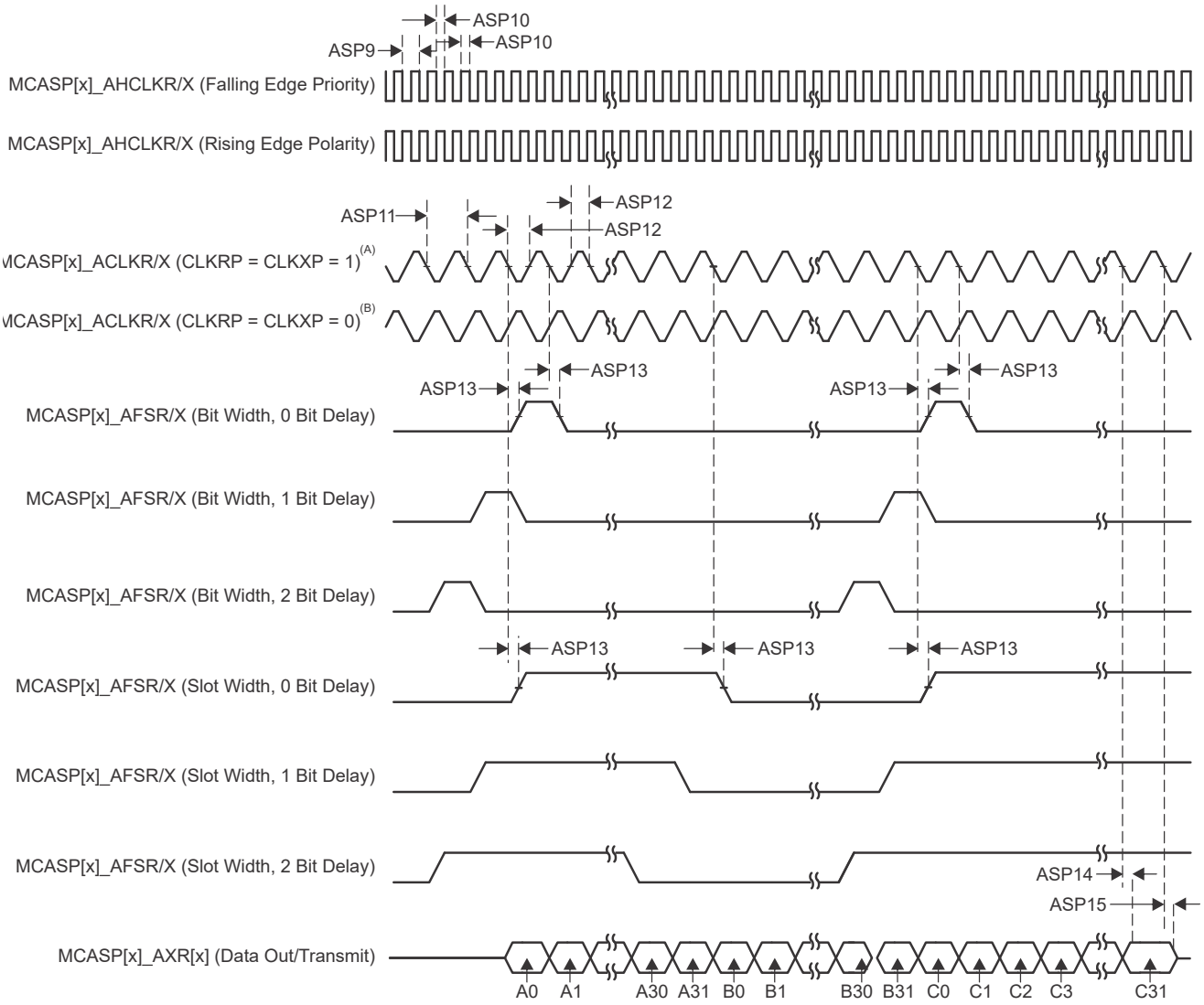

A. For CLKRP = CLKXP = 1, the MCASP transmitter is configured for falling edge (to shift data out) and the MCASP receiver is configured for rising edge (to shift data in).

B. For CLKRP = CLKXP = 0, the MCASP transmitter is configured for rising edge (to shift data out) and the MCASP receiver is configured for falling edge (to shift data in).

図 6-85. MCASP Output Timing

For more information, see *Multichannel Audio Serial Port (MCASP)* section in *Peripherals* chapter in the device TRM.

6.9.5.18 MCSPI

For more details about features and additional description information on the device Serial Port Interface, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

表 6-70 represents MCSPI timing conditions.

注

The IO timings provided in this section are applicable for all combinations of signals for MCU_SPI0 and MCU_SPI1. However, the timings are only valid for MCU_SPI0 and MCU_SPI1 if signals within a single IOSET are used. The IOSETs are defined in the 表 6-75 and 表 6-76 tables.

表 6-70. MCSPI Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate		2	8.5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	CLK	6	24	pF
		D[x], CSi	6	12	pF

6.9.5.18.1 MCSPI — Master Mode

表 6-71, 図 6-86, 表 6-72, and 図 6-87 present timing requirements and switching characteristics for MCSPI – Master Mode.

表 6-71. MCSPI Timing Requirements - Master Mode

see 図 6-86

NO.			MIN	MAX	UNIT
SM4	$t_{su(misoV-spiclkV)}$	Setup time, SPI_D[x] valid before SPI_CLK active edge	2.8		ns
SM5	$t_{h(spiclkV-misoV)}$	Hold time, SPI_D[x] valid after SPI_CLK active edge	3		ns

表 6-72. MCSPI Switching Characteristics - Master Mode

see 図 6-87

NO.	PARAMETER		MODE	MIN	MAX	UNIT
SM1	$t_{c(spiclk)}$	Cycle time, SPI_CLK		20.8		ns
SM2	$t_{w(spiclkL)}$	Pulse duration, SPI_CLK low		0.5P - 1(1)		ns
SM3	$t_{w(spiclkH)}$	Pulse duration, SPI_CLK high		0.5P - 1(1)		ns
SM6	$t_{d(spiclkV-simoV)}$	Delay time, SPI_CLK active edge to SPI_D[x] transition		-3	2.5	ns
SM7	$t_{d(csV-simoV)}$	Delay time, SPI_CSi active edge to SPI_D[x] transition		5		ns
SM8	$t_{d(csV-spiclk)}$	Delay time, SPI_CSi active to SPI_CLK first edge	PHA = 0(2)	B - 4(3)		ns
			PHA = 1 (2)	A - 4(4)		ns
SM9	$t_{d(spiclkV-csV)}$	Delay time, SPI_CLK last edge to SPI_CSi inactive	PHA = 0(2)	A - 4(4)		ns
			PHA = 1(2)	B - 4(3)		ns

(1) P = SPI_CLK period in ns
(2) SPI_CLK phase is programmable with the PHA bit of the MCSPI_CHCONF_0/1/2/3 register

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(3) B = (TCS + .5) * TSPICLKREF, where TCSns a bit field of the MCSPI_CHCONF_0/1/2/3 register and Fratio = Even >= 2.
(4) When P = 20.8 ns, A = (TCS + 1) * TSPICLKREF, where TCSns a bit field of the MCSPI_CHCONF_0/1/2/3 register.
When P > 20.8 ns, A = (TCS + 0.5) * Fratio * TSPICLKREF, where TCSns a bit field of the MCSPI_CHCONF_0/1/2/3 register.

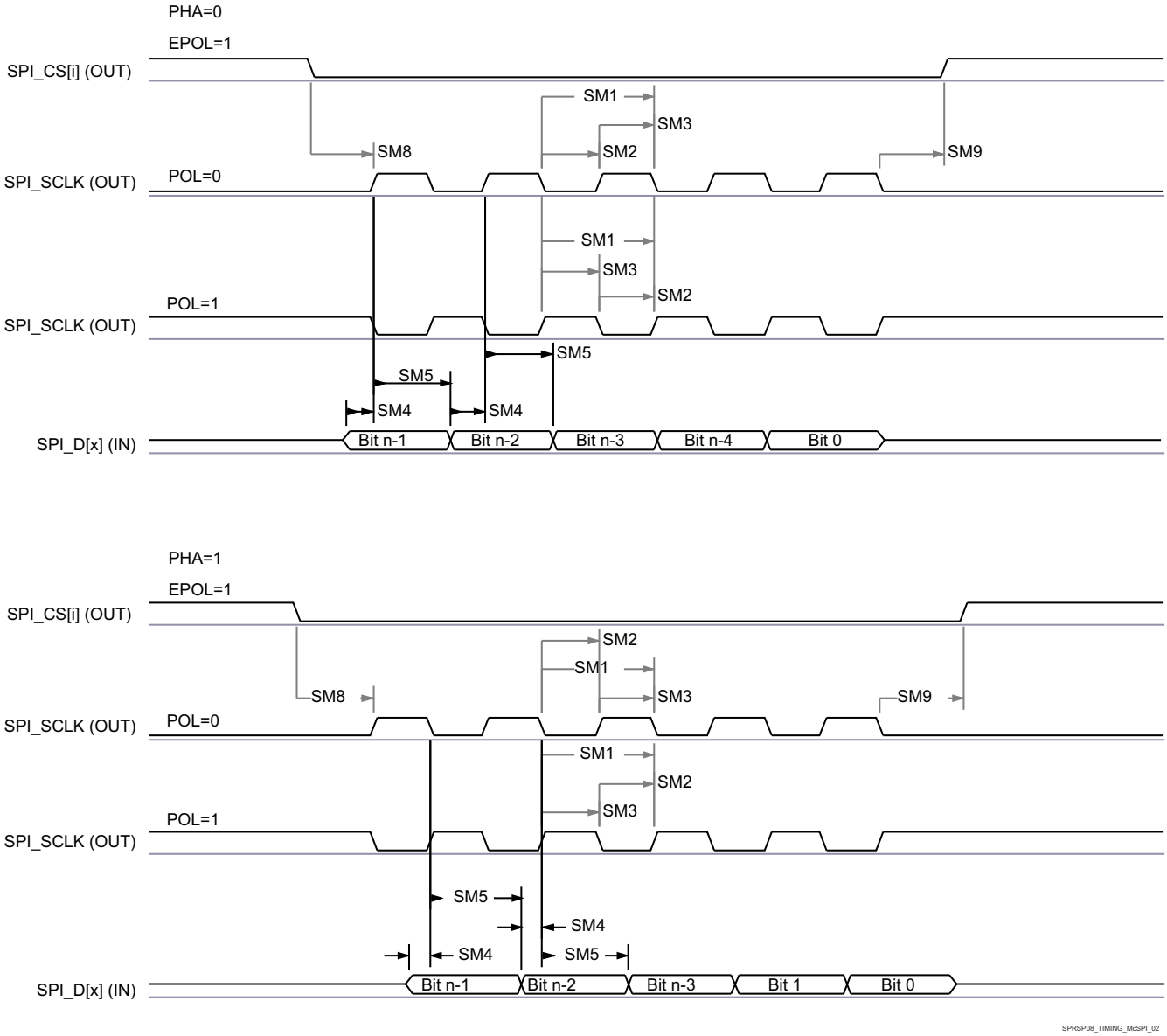

図 6-86. SPI Master Mode Receive Timing

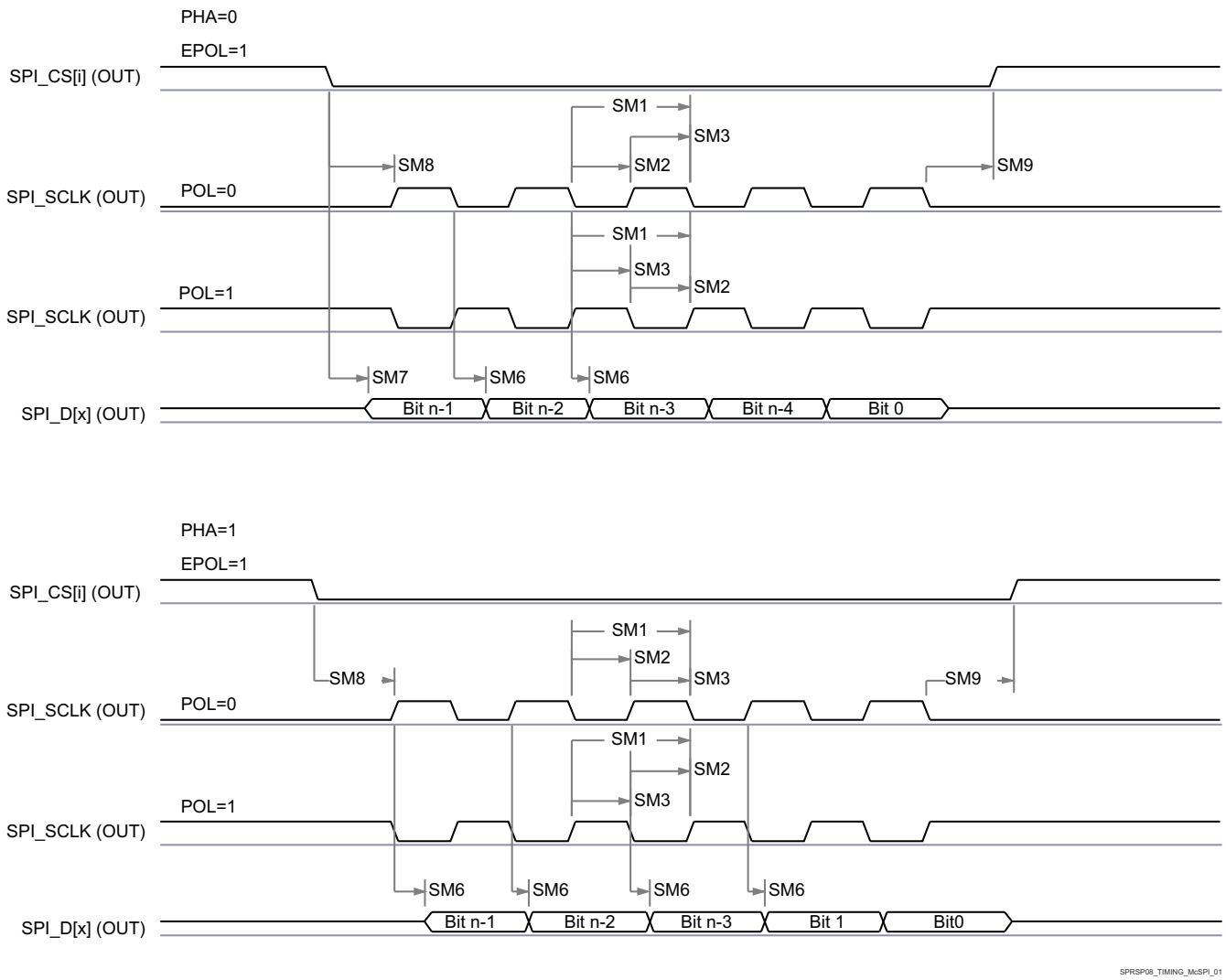

図 6-87. MCSPI Master Mode Transmit Timing

6.9.5.18.2 MCSPI — Slave Mode

表 6-73, 表 6-74, 図 6-88, and 図 6-89 present timing requirements and switching characteristics for MCSPI – Slave Mode.

表 6-73. MCSPI Timing Requirements - Slave Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SS1	$t_{c(spiclk)}$	Cycle time, SPI_CLK		20.8		ns
SS2	$t_{w(spiclkL)}$	Pulse duration, SPI_CLK low		0.45P[(1)]		ns
SS3	$t_{w(spiclkH)}$	Pulse duration, SPI_CLK high		0.45P[(1)]		ns
SS4	$t_{su(simoV-spiclkV)}$	Setup time, SPI_D[x] valid before SPI_CLK active edge		5		ns
SS5	$t_{h(spiclkV-simoV)}$	Hold time, SPI_D[x] valid after SPI_CLK active edge		5		ns
SS8	$t_{su(csV-spiclkV)}$	Setup time, SPI_CSi valid before SPI_CLK first edge		5		ns
SS9	$t_{h(spiclkV-csV)}$	Hold time, SPI_CSi valid after SPI_CLK last edge		5		ns

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表 6-74. MCSPI Switching Characteristics - Slave Mode

NO.	PARAMETER	DESCRIPTION	MIN	MAX	UNIT
SS6	$t_{d(spiclkV-somiV)}$	Delay time, SPI_CLK active edge to SPI_D[x] transition	2	17.12	ns
SS7	$t_{sk(csV-somiV)}$	Delay time, SPI_CSi active edge to SPI_D[x] transition	20.95		ns

(1) P = SPI_CLK period in ns.

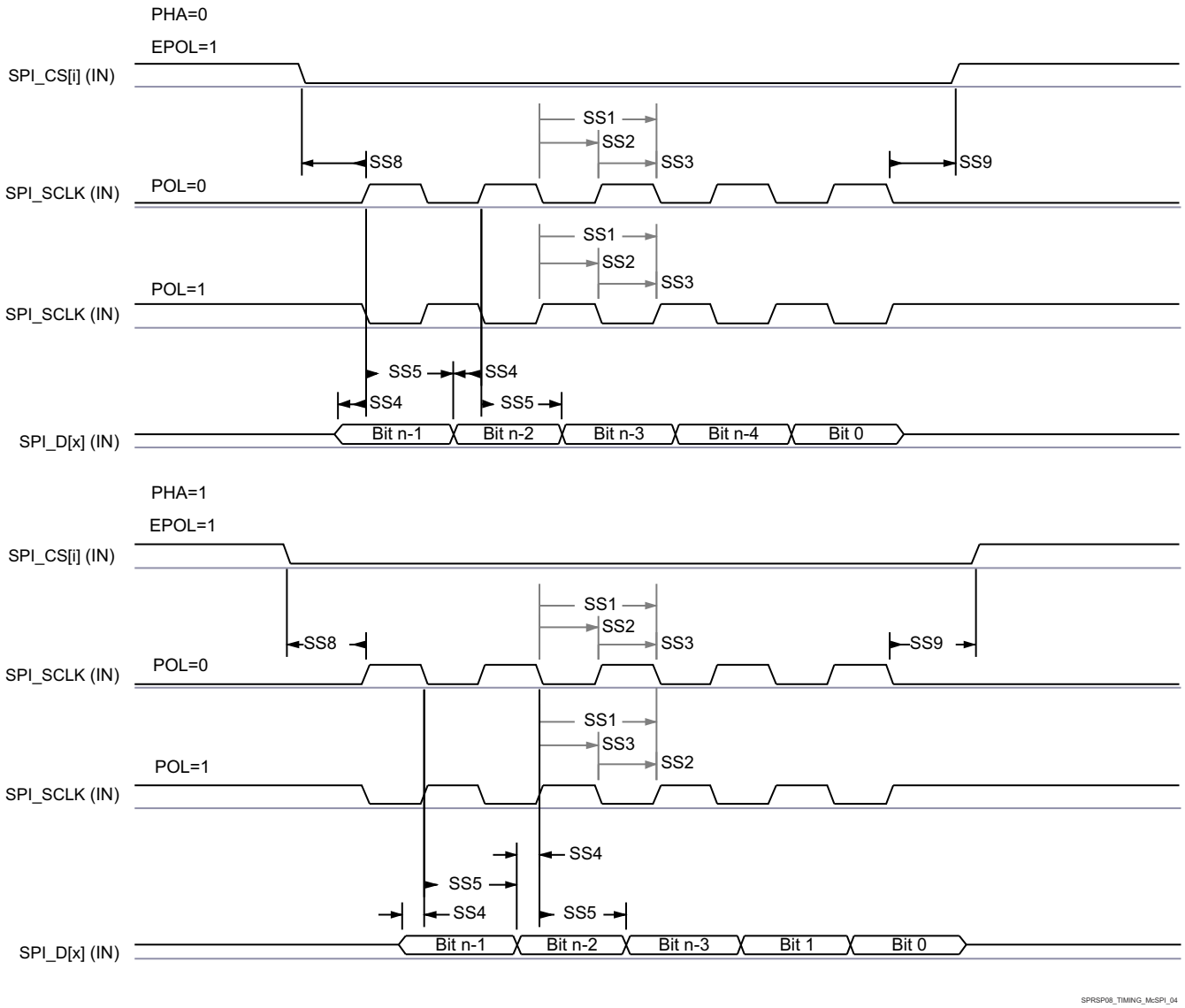

図 6-88. SPI Slave Mode Receive Timing

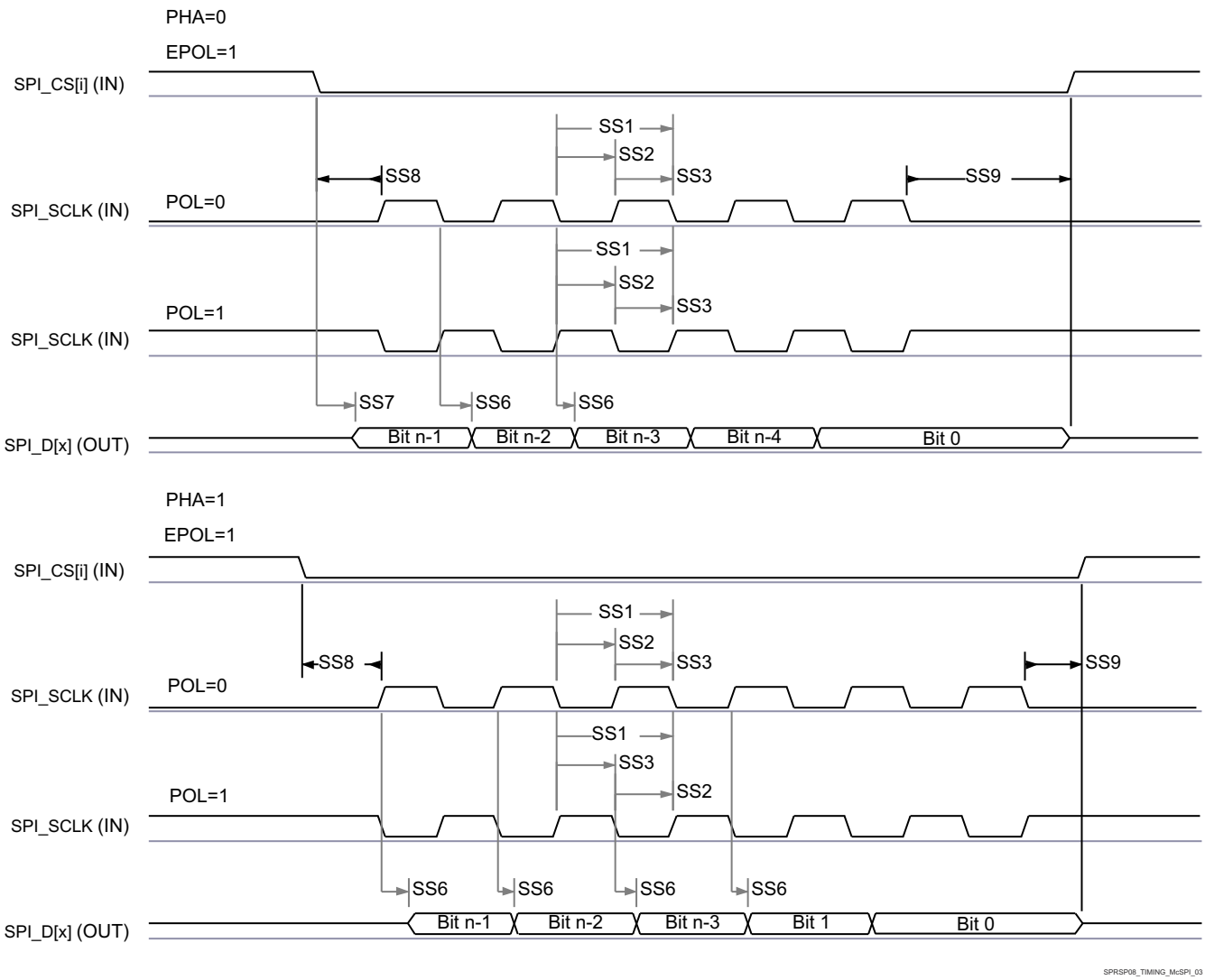

図 6-89. MCSPI Slave Mode Transmit Timing

表 6-75 and 表 6-76 present the specific groupings of signals (IOSET) for use with MCU_SPI0 and MCU_SPI1.

表 6-75. MCU_SPI0 IOSETs

Signals	IOSET1		IOSET2	
	BALL NAME	MUX	BALL NAME	MUX
MCU_SPI0_CLK	MCU_SPI0_CLK	0	MCU_SPI0_CLK	0
MCU_SPI0_D0	MCU_SPI0_D0	0	MCU_SPI0_D0	0
MCU_SPI0_D1	MCU_SPI0_D1	0	MCU_SPI0_D1	0
MCU_SPI0_CS0	MCU_SPI0_CS0	0	MCU_SPI0_CS0	0
MCU_SPI0_CS1	MCU_OSPI1_D3	5	WKUP_GPIO0_12	1
MCU_SPI0_CS2	MCU_OSPI1_CSn1	5	WKUP_GPIO0_14	1

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表 6-76. MCU_SPI1 IOSET

Signals	IOSET1		IOSET2	
	BALL NAME	MUX	BALL NAME	MUX
MCU_SPI1_CLK	MCU_SPI1_CLK	0	MCU_SPI1_CLK	0
MCU_SPI1_D0	MCU_SPI1_D0	0	MCU_SPI1_D0	0
MCU_SPI1_D1	MCU_SPI1_D1	0	MCU_SPI1_D1	0
MCU_SPI1_CS0	MCU_SPI1_CS0	0	MCU_SPI1_CS0	0
MCU_SPI1_CS1	MCU_OSPI1_D1	5	WKUP_GPIO0_13	1
MCU_SPI1_CS2	MCU_OSPI1_D2	5	WKUP_GPIO0_15	1

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

6.9.5.19 MMCSD

The MMCSD Host Controller provides an interface to embedded Multi-Media Card (MMC), Secure Digital (SD), and Secure Digital IO (SDIO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more details about MMCSD interfaces, see the corresponding MMC0, MMC1, and MMC2 sections within

, *Signal Descriptions* and , *Detailed Description*.

注

Some operating modes require software configuration of the MMC DLL delay settings, as shown in 表 6-77 and 表 6-86.

For more information, see *Multi-Media Card/Secure Digital (MMCSD) Interface* section in *Peripherals* chapter in the device TRM.

6.9.5.19.1 MMC0 - eMMC Interface

MMC0 interface is compliant with the JEDEC eMMC electrical standard v5.1 (JESD84-B51) and it supports the following eMMC applications:

- Legacy speed
- High speed SDR
- High speed DDR
- HS200

表 6-77 presents the required DLL software configuration settings for MMC0 timing modes.

表 6-77. MMC0 DLL Delay Mapping for All Timing Modes

REGISTER NAME		MMCSD0_SS_PHY_CTRL_4_REG					MMCSD0_SS_PHY_CTRL_5_REG		
BIT FIELD		[31:24]	[20]	[15:12]	[8]	[4:0]	[17:16]	[10:8]	[2:0]
BIT FIELD NAME		STRBSEL	OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	SELDLYTXCLK SELDLYRXCLK	FRQSEL	CLKBUFSEL
MODE	DESCRIPTION	STROBE DELAY	OUTPUT DELAY ENABLE	OUTPUT DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DLL/ DELAY CHAIN SELECT	DLL REF FREQUENCY	DELAY BUFFER DURATION
Legacy SDR	8-bit PHY operating 1.8 V, 25 MHz	0x0	0x0	NA	0x1	0x10	0x1	0x0	0x7
High Speed SDR	8-bit PHY operating 1.8 V, 50 MHz	0x0	0x0	NA	0x1	0xA	0x1	0x0	0x7

表 6-77. MMC0 DLL Delay Mapping for All Timing Modes (続き)

REGISTER NAME		MMCSD0_SS_PHY_CTRL_4_REG					MMCSD0_SS_PHY_CTRL_5_REG		
BIT FIELD		[31:24]	[20]	[15:12]	[8]	[4:0]	[17:16]	[10:8]	[2:0]
BIT FIELD NAME		STRBSEL	OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	SELDLYTXCLK SELDLYRXCLK	FRQSEL	CLKBUFSEL
MODE	DESCRIPTION	STROBE DELAY	OUTPUT DELAY ENABLE	OUTPUT DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DLL/ DELAY CHAIN SELECT	DLL REF FREQUENCY	DELAY BUFFER DURATION
High Speed DDR	8-bit PHY operating 1.8 V, 50 MHz	0x0	0x1	0x5	0x1	0x3	0x0	0x4	0x7
HS200	8-bit PHY operating 1.8 V, 200 MHz	0x0	0x1	0x6	0x1	Tuning	0x0	0x0	0x7

表 6-78 presents timing conditions for MMC0.

表 6-78. MMC0 Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	Legacy SDR	0.14	1.44	V/ns
		High Speed SDR	0.3	0.9	V/ns
		High Speed DDR (CMD)	0.3	0.9	V/ns
		High Speed DDR (DAT[7:0])	0.45	0.9	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	HS200	1	6	pF
		All other modes	1	12	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	All modes	126	756	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	Legacy SDR, High Speed SDR, High Speed DDR		100	ps
		HS200		8	ps

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6.9.5.19.1.1 Legacy SDR Mode

表 6-79, 図 6-90, 表 6-80, and 図 6-91 present timing requirements and switching characteristics for MMC0 – Legacy SDR Mode.

表 6-79. MMC0 Timing Requirements – Legacy SDR Mode

see 図 6-90

NO.			MIN	MAX	UNIT
LSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	9.69		ns
LSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	9.65		ns
LSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	9.69		ns
LSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	9.65		ns

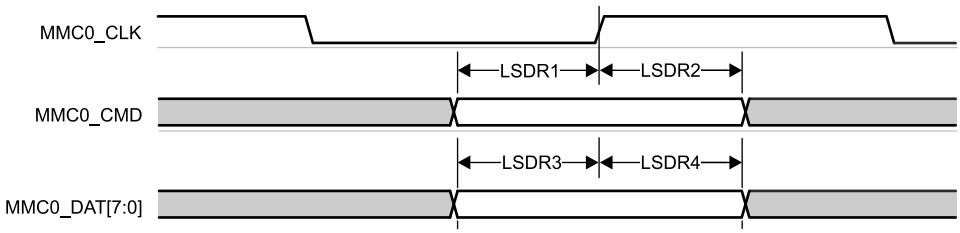

図 6-90. MMC0 – Legacy SDR – Receive Mode

表 6-80. MMC0 Switching Characteristics – Legacy SDR Mode

see 図 6-91

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		25	MHz
LSDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	40		ns
LSDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	18.7		ns
LSDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	18.7		ns
LSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	-2.74	5.07	ns
LSDR9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition	-2.74	5.07	ns

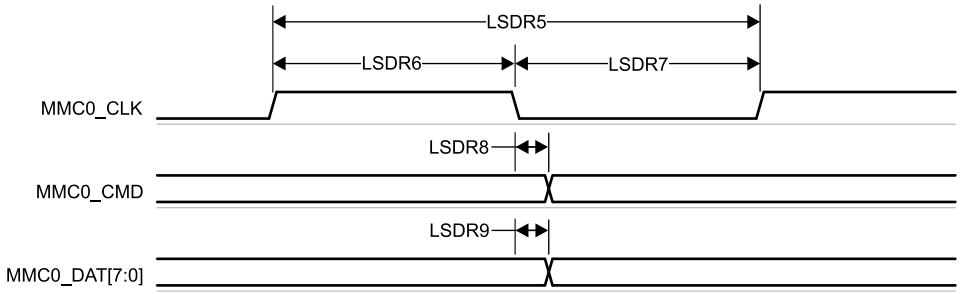

図 6-91. MMC0 – Legacy SDR – Transmit Mode

6.9.5.19.1.2 High Speed SDR Mode

表 6-81, 図 6-92, 表 6-82, and 図 6-93 present timing requirements and switching characteristics for MMC0 – High Speed SDR Mode.

表 6-81. MMC0 Timing Requirements – High Speed SDR Mode

see 図 6-92

NO.			MIN	MAX	UNIT
HSSDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	2.99		ns
HSSDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	2.67		ns
HSSDR3	$t_{su(dV-clkH)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK rising edge	2.99		ns
HSSDR4	$t_{h(clkH-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK rising edge	2.67		ns

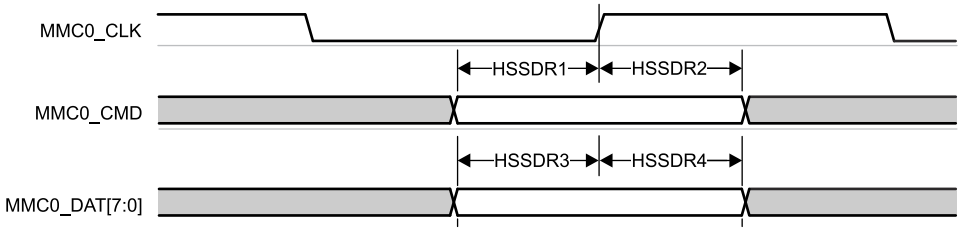

図 6-92. MMC0 – High Speed SDR Mode – Receive Mode

表 6-82. MMC0 Switching Characteristics – High Speed SDR Mode

see 図 6-93

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
HSSDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
HSSDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
HSSDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
HSSDR8	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK falling edge to MMC0_CMD transition	-0.84	3.65	ns
HSSDR9	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK falling edge to MMC0_DAT[7:0] transition	-0.84	3.65	ns

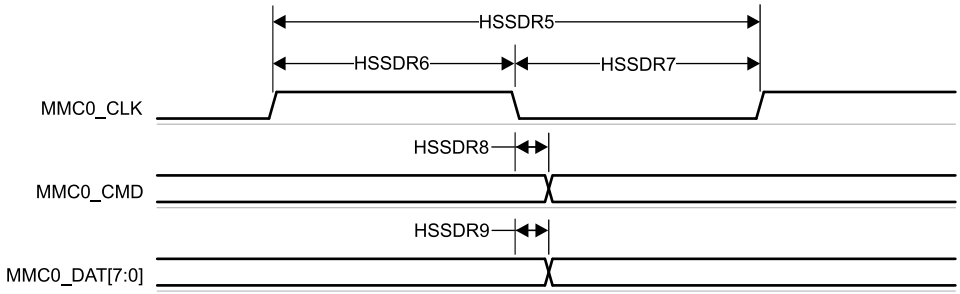

図 6-93. MMC0 – High Speed SDR Mode – Transmit Mode

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6.9.5.19.1.3 High Speed DDR Mode

表 6-83, 図 6-94, 表 6-84, and 図 6-95 present timing requirements and switching characteristics for MMC0 – High Speed DDR Mode.

表 6-83. MMC0 Timing Requirements – High Speed DDR Mode

see 図 6-94

NO.			MIN	MAX	UNIT
HSDDR1	$t_{su(cmdV-clkH)}$	Setup time, MMC0_CMD valid before MMC0_CLK rising edge	2		ns
HSDDR2	$t_{h(clkH-cmdV)}$	Hold time, MMC0_CMD valid after MMC0_CLK rising edge	2.5		ns
HSDDR3	$t_{su(dV-clkV)}$	Setup time, MMC0_DAT[7:0] valid before MMC0_CLK transition	0.74		ns
HSDDR4	$t_{h(clkV-dV)}$	Hold time, MMC0_DAT[7:0] valid after MMC0_CLK transition	1.67		ns

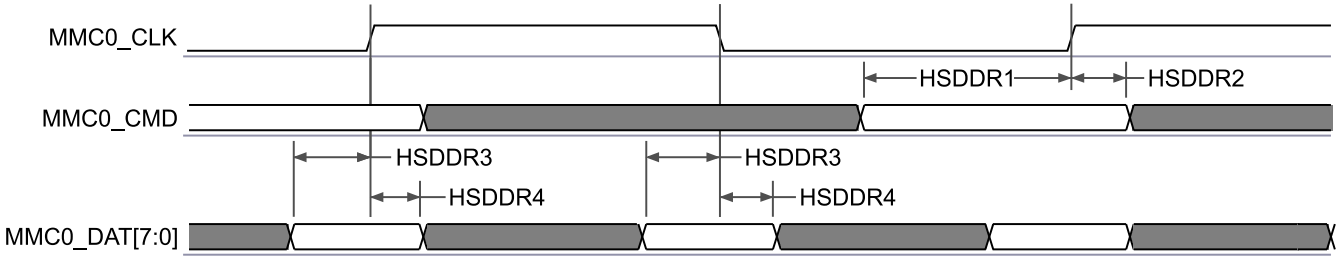

図 6-94. MMC0 – High Speed DDR Mode – Receive Mode

表 6-84. MMC0 Switching Characteristics – High Speed DDR Mode

see 図 6-95

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		50	MHz
HSDDR5	$t_{c(clk)}$	Cycle time, MMC0_CLK	20		ns
HSDDR6	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	9.2		ns
HSDDR7	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	9.2		ns
HSDDR8	$t_{d(clkH-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	3.4	9.72	ns
HSDDR9	$t_{d(clkV-dV)}$	Delay time, MMC0_CLK transition to MMC0_DAT[7:0] transition	2.9	6.6	ns

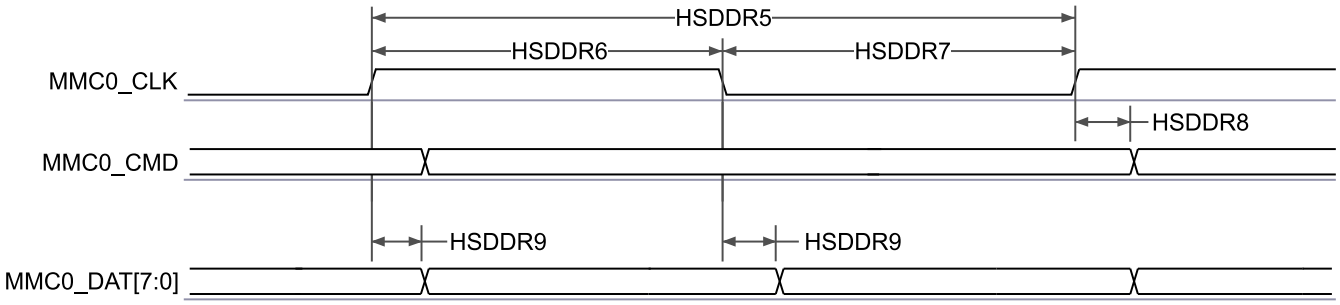

図 6-95. MMC0 – High Speed DDR Mode – Transmit Mode

6.9.5.19.1.4 HS200 Mode

表 6-85 and 図 6-96 present switching characteristics for MMC0 – HS200 Mode.

表 6-85. MMC0 Switching Characteristics – HS200 Mode

see 図 6-96

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC0_CLK		200	MHz
HS2005	$t_{c(clk)}$	Cycle time, MMC0_CLK	5		ns
HS2006	$t_{w(clkH)}$	Pulse duration, MMC0_CLK high	2.08		ns
HS2007	$t_{w(clkL)}$	Pulse duration, MMC0_CLK low	2.08		ns
HS2008	$t_{d(clkL-cmdV)}$	Delay time, MMC0_CLK rising edge to MMC0_CMD transition	1.12	3.16	ns
HS2009	$t_{d(clkL-dV)}$	Delay time, MMC0_CLK rising edge to MMC0_DAT[7:0] transition	1.12	3.16	ns

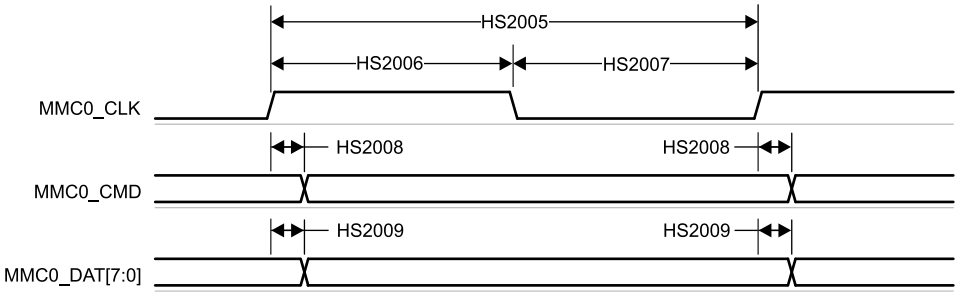

図 6-96. MMC0 – HS200 Mode – Transmit Mode

6.9.5.19.2 MMC1/2 - SD/SDIO Interface

MMC1 and MMC2 interfaces are compliant with the SD Host Controller Standard Specification 4.10 and SD Physical Layer Specification v3.01 as well as SDIO Specification v3.00 and they support the following SD Card applications:

- Default speed
- High speed
- UHS–I SDR12
- UHS–I SDR25
- UHS–I SDR50
- UHS–I SDR104
- UHS–I DDR50

表 6-86 presents the required DLL software configuration settings for MMC1 timing modes.

表 6-86. MMC1/2 DLL Delay Mapping for All Timing Modes

REGISTER NAME		MMCSD12_SS_PHY_CTRL_4_REG				MMCSD12_SS_PHY_CTRL_5_REG
BIT FIELD		[20]	[15:12]	[8]	[4:0]	[2:0]
BIT FIELD NAME		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	CLKBUFSEL
MODE	DESCRIPTION	DELAY ENABLE	DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DELAY BUFFER DURATION
Default Speed	4-bit PHY operating 3.3 V, 25 MHz	0x1	0x1	0x0	0x0	0x7
High Speed	4-bit PHY operating 3.3 V, 50 MHz	0x1	0x1	0x0	0x0	0x7
UHS-I SDR12	4-bit PHY operating 1.8 V, 25 MHz	0x1	0xF	0x0	0x0	0x7

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表 6-86. MMC1/2 DLL Delay Mapping for All Timing Modes (続き)

REGISTER NAME		MMCSD12_SS_PHY_CTRL_4_REG				MMCSD12_SS_PHY_CTRL_5_REG
BIT FIELD		[20]	[15:12]	[8]	[4:0]	[2:0]
BIT FIELD NAME		OTAPDLYENA	OTAPDLYSEL	ITAPDLYENA	ITAPDLYSEL	CLKBUFSEL
MODE	DESCRIPTION	DELAY ENABLE	DELAY VALUE	INPUT DELAY ENABLE	INPUT DELAY VALUE	DELAY BUFFER DURATION
UHS-I SDR25	4-bit PHY operating 1.8 V, 50 MHz	0x1	0xF	0x0	0x0	0x7
UHS-I SDR50	4-bit PHY operating 1.8 V, 100 MHz	0x1	0xC	0x1	Tuning	0x7
UHS-I DR50	4-bit PHY operating 1.8 V, 50 MHz	0x1	0xC	0x1	0x2	0x7
UHS-I SDR104	4-bit PHY operating 1.8, V 200 MHz	0x1	0x5	0x1	Tuning	0x7

表 6-87 presents timing conditions for MMC1.

表 6-87. MMC1/2 Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	Default Speed, High Speed	0.69	2.06	V/ns
		UHS–I SDR12, UHS–I SDR25	0.34	1.34	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	All modes	1	10	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay of each trace	UHS–I DDR50	240	1134	ps
		All other modes	126	1386	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces	UHS–I DDR50, UHS–I SDR104		20	ps
		All other modes		100	ps

6.9.5.19.2.1 Default Speed Mode

表 6-88, 図 6-97, 表 6-89, and 図 6-98 present timing requirements and switching characteristics for MMC1/2 – Default Speed Mode.

表 6-88. MMC1/2 Timing Requirements – Default Speed Mode

see 図 6-97

NO.			MIN	MAX	UNIT
DS1	$t_{su(cmdV-clkH)}$	Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge	2.55		ns
DS2	$t_{h(clkH-cmdV)}$	Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge	4.65		ns
DS3	$t_{su(dV-clkH)}$	Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge	2.55		ns
DS4	$t_{h(clkH-dV)}$	Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge	4.65		ns

A. x = 1, 2 for MMC1 and MMC2
B. x = 1, 2 for MMC1 and MMC2

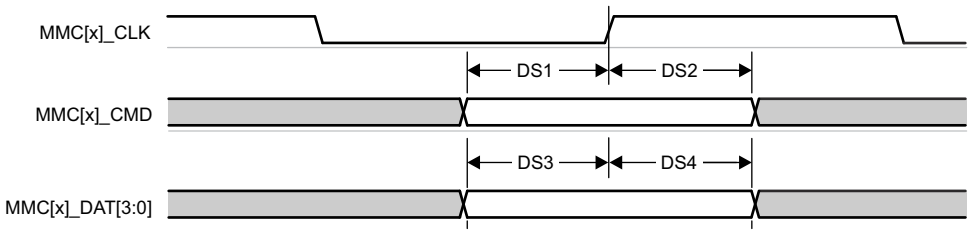

図 6-97. MMC1/2 – Default Speed – Receive Mode

表 6-89. MMC1/2 Switching Characteristics – Default Speed Mode

see 図 6-98

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		25	MHz
DS5	$t_{c(clk)}$	Cycle time, MMC[x]_CLK	40		ns
DS6	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	18.7		ns
DS7	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	18.7		ns
DS8	$t_{d(clkL-cmdV)}$	Delay time, MMC[x]_CLK falling edge to MMC[x]_CMD transition	-2.93	3.63	ns
DS9	$t_{d(clkL-dV)}$	Delay time, MMC[x]_CLK falling edge to MMC[x]_DAT[3:0] transition	-2.93	3.63	ns

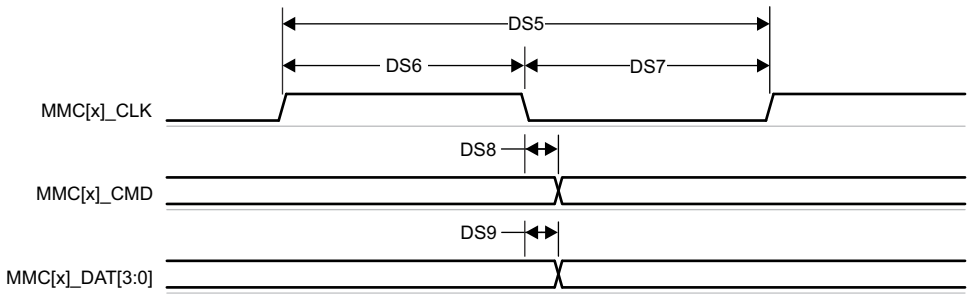

図 6-98. MMC1/2 – Default Speed – Transmit Mode

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6.9.5.19.2.2 High Speed Mode

表 6-90, 図 6-99, 表 6-91, and 図 6-100 present timing requirements and switching characteristics for MMC1/2 – High Speed Mode.

表 6-90. MMC1/2 Timing Requirements – High Speed Mode

see 図 6-99

NO.			MIN	MAX	UNIT
HS1	$t_{su(cmdV-clkH)}$	Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge	2.55		ns
HS2	$t_{h(clkH-cmdV)}$	Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge	2.67		ns
HS3	$t_{su(dV-clkH)}$	Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge	2.55		ns
HS4	$t_{h(clkH-dV)}$	Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge	2.67		ns

A. x = 1, 2 for MMC1 and MMC2
B. x = 1, 2 for MMC1 and MMC2

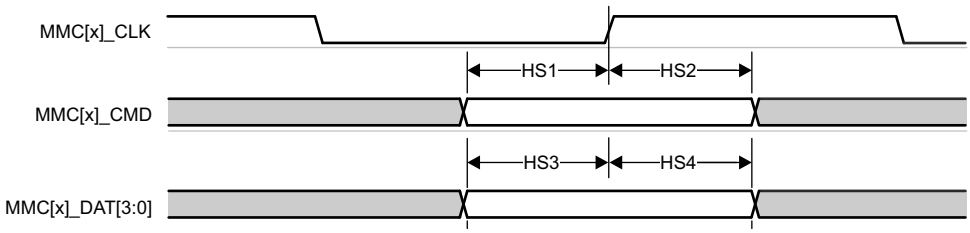

図 6-99. MMC1 /2– High Speed – Receive Mode

表 6-91. MMC1/2 Switching Characteristics – High Speed Mode

see 図 6-100

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		50	MHz
HS5	$t_{c(clk)}$	Cycle time. MMC[x]_CLK	20		ns
HS6	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	9.2		ns
HS7	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	9.2		ns
HS8	$t_{d(clkL-cmdV)}$	Delay time, MMC[x]_CLK falling edge to MMC[x]_CMD transition	-1.77	2.35	ns
HS9	$t_{d(clkL-dV)}$	Delay time, MMC[x]_CLK falling edge to MMC[x]_DAT[3:0] transition	-1.77	2.35	ns

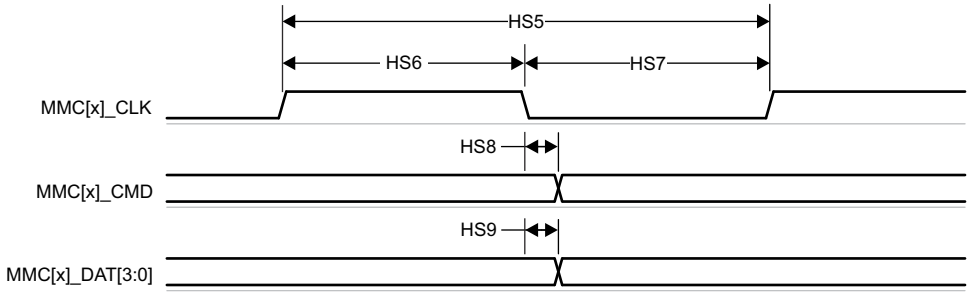

図 6-100. MMC1/2 – High Speed – Transmit Mode

6.9.5.19.2.3 UHS–I SDR12 Mode

表 6-92, 図 6-101, 表 6-93, and 図 6-102 present timing requirements and switching characteristics for MMC1/2 – UHS-I SDR12 Mode.

表 6-92. MMC1/2 Timing Requirements – UHS-I SDR12 Mode

see 図 6-101

NO.			MIN	MAX	UNIT
SDR121	$t_{su(cmdV-clkH)}$	Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge	21.65		ns
SDR122	$t_{h(clkH-cmdV)}$	Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge	1.67		ns
SDR123	$t_{su(dV-clkH)}$	Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge	21.65		ns
SDR124	$t_{h(clkH-dV)}$	Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge	1.67		ns

A. x = 1, 2 for MMC1 and MMC2
B. x = 1, 2 for MMC1 and MMC2

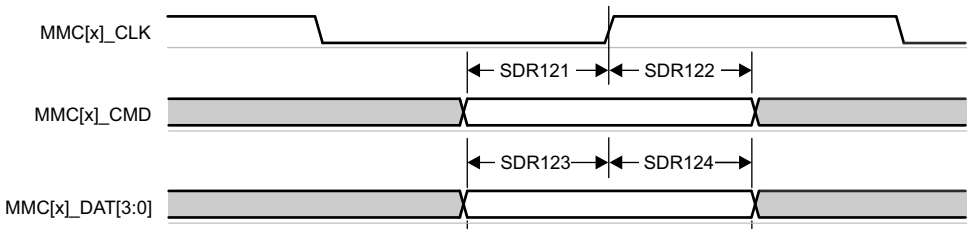

図 6-101. MMC1/2 – UHS-I SDR12 – Receive Mode

表 6-93. MMC1/2 Switching Characteristics – UHS-I SDR12 Mode

see 図 6-102

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		25	MHz
SDR125	$t_{c(clk)}$	Cycle time, MMC[x]_CLK	40		ns
SDR126	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	18.7		ns
SDR127	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	18.7		ns
SDR128	$t_{d(clkH-cmdV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition	1.2	13.69	ns
SDR129	$t_{d(clkH-dV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition	1.2	13.69	ns

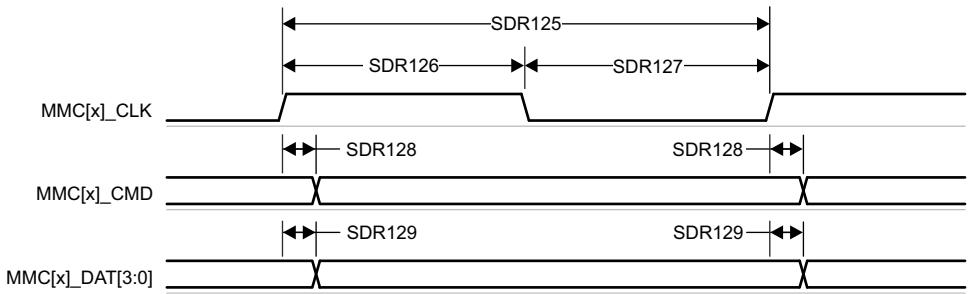

図 6-102. MMC1/2 – UHS-I SDR12 – Transmit Mode

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6.9.5.19.2.4 UHS–I SDR25 Mode

表 6-94, 図 6-103, 表 6-95, and 図 6-104 present timing requirements and switching characteristics for MMC1/2 – UHS-I SDR25 Mode.

表 6-94. MMC1/2 Timing Requirements – UHS-I SDR25 Mode

see 図 6-103

NO.			MIN	MAX	UNIT
SDR251	$t_{su(cmdV-clkH)}$	Setup time, MMC[x]_CMD valid before MMC[x]_CLK rising edge	2.15		ns
SDR252	$t_{h(clkH-cmdV)}$	Hold time, MMC[x]_CMD valid after MMC[x]_CLK rising edge	1.67		ns
SDR253	$t_{su(dV-clkH)}$	Setup time, MMC[x]_DAT[3:0] valid before MMC[x]_CLK rising edge	2.15		ns
SDR254	$t_{h(clkH-dV)}$	Hold time, MMC[x]_DAT[3:0] valid after MMC[x]_CLK rising edge	1.67		ns

A. x = 1, 2 for MMC1 and MMC2
B. x = 1, 2 for MMC1 and MMC2

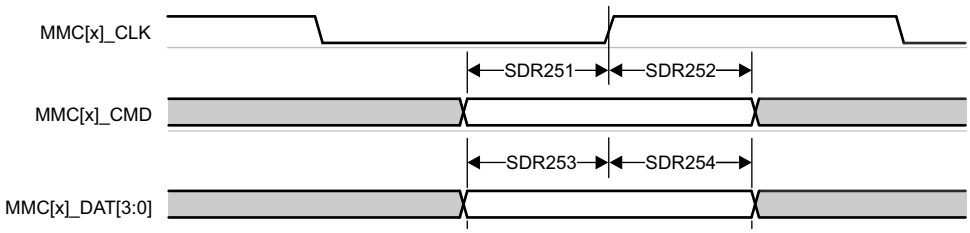

図 6-103. MMC1/2 – UHS-I SDR25 – Receive Mode

表 6-95. MMC1/2 Switching Characteristics – UHS-I SDR25 Mode

see 図 6-104

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		50	MHz
SDR255	$t_{c(clk)}$	Cycle time, MMC[x]_CLK	20		ns
SDR256	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	9.2		ns
SDR257	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	9.2		ns
SDR258	$t_{d(clkH-cmdV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition	2.4	9.8	ns
SDR259	$t_{d(clkH-dV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition	2.4	9.8	ns

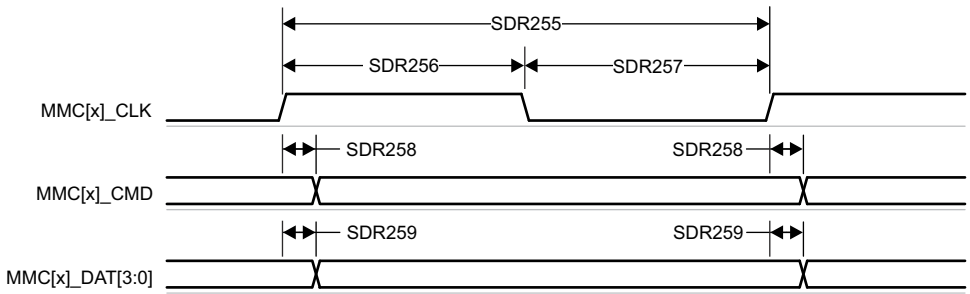

図 6-104. MMC1/2 – UHS-I SDR25 – Transmit Mode

6.9.5.19.2.5 UHS–I SDR50 Mode

表 6-96, and 図 6-105 presents switching characteristics for MMC1/2 – UHS-I SDR50 Mode.

表 6-96. MMC1/2 Switching Characteristics – UHS-I SDR50 Mode

see 図 6-105

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		100	MHz
SDR505	$t_{c(clk)}$	Cycle time, MMC[x]_CLK	10		ns
SDR506	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	4.45		ns
SDR507	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	4.45		ns
SDR508	$t_{d(clkH-cmdV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition	1.2	6.35	ns
SDR509	$t_{d(clkH-dV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition	1.2	6.35	ns

A. x = 1, 2 for MMC1 and MMC2

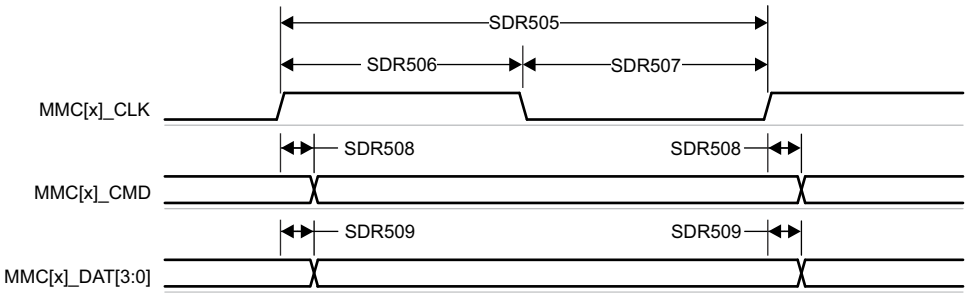

図 6-105. MMC1/2 – UHS-I SDR50 – Transmit Mode

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6.9.5.19.2.6 UHS–I DDR50 Mode

表 6-97 and 図 6-106 present switching characteristics for MMC1/2 – UHS-I DDR50 Mode.

表 6-97. MMC1/2 Switching Characteristics – UHS-I DDR50 Mode

see 図 6-106

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		50	MHz
DDR505	$t_{c(clk)}$	Cycle time, MMC[x]_CLK	20		ns
DDR506	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	9.2		ns
DDR507	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	9.2		ns
DDR508	$t_{d(clkH-cmdV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition	1.2	9.8	ns
DDR509	$t_{d(clk-dV)}$	Delay time, MMC[x]_CLK transition to MMC[x]_DAT[3:0] transition	1.2	6.35	ns

A. x = 1, 2 for MMC1 and MMC2

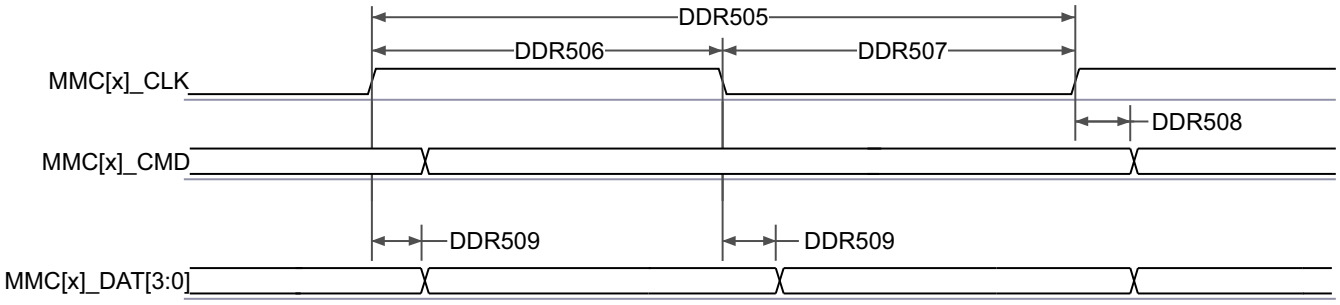

図 6-106. MMC1/2 – UHS-I DDR50 – Transmit Mode

6.9.5.19.2.7 UHS–I SDR104 Mode

表 6-98, and 図 6-107 present switching characteristics for MMC1/2 – UHS-I SDR104 Mode.

表 6-98. MMC1/2 Switching Characteristics – UHS-I SDR104 Mode

see 図 6-107

NO.	PARAMETER		MIN	MAX	UNIT
	$f_{op(clk)}$	Operating frequency, MMC[x]_CLK		200	MHz
SDR1045	$t_{c(clk)}$	Cycle time, MMC[x]_CLK	5		ns
SDR1046	$t_{w(clkH)}$	Pulse duration, MMC[x]_CLK high	2.08		ns
SDR1047	$t_{w(clkL)}$	Pulse duration, MMC[x]_CLK low	2.08		ns
SDR1048	$t_{d(clkH-cmdV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_CMD transition	1.12	3.16	ns
SDR1049	$t_{d(clkH-dV)}$	Delay time, MMC[x]_CLK rising edge to MMC[x]_DAT[3:0] transition	1.12	3.16	ns

A. x = 1, 2 for MMC1 and MMC2

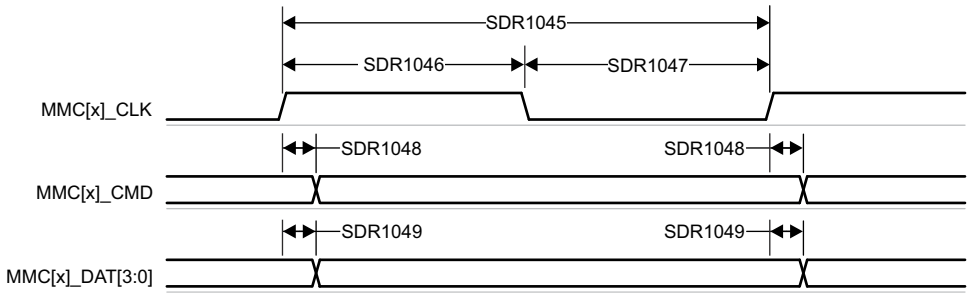

図 6-107. MMC1/2 – UHS-I SDR104 – Transmit Mode

6.9.5.20 CPTS

表 6-99 represents CPTS timing conditions.

表 6-99. CPTS Timing Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	10	pF

セクション 6.9.5.20.1, セクション 6.9.5.20.2, 図 6-108, and 図 6-109 present timing requirements and switching characteristics of the CPTS interface.

6.9.5.20.1 CPTS Timing Requirements

see 図 6-108

NO.			MIN	MAX	UNIT
T1	$t_{w(HWnTSPUSHH)}$	Pulse duration, HWnTSPUSH(2) high	12P + 2(1)		ns
T2	$t_{w(HWnTSPUSHL)}$	Pulse duration, HWnTSPUSH(2) low	12P + 2(1)		ns
T3	$t_{c(RFT_CLK)}$	Cycle time, RFT_CLK	5	8	ns
T4	$t_{w(RFT_CLKH)}$	Pulse duration, RFT_CLK high	0.45 * T(3)		ns
T5	$t_{w(RFT_CLKL)}$	Pulse duration, RFT_CLK low	0.45 * T(3)		ns

(1) P = functional clock period in ns.
(2) In HWnTSPUSH, n = 1 to 2.
(3) T = RFT_CLK period in ns.

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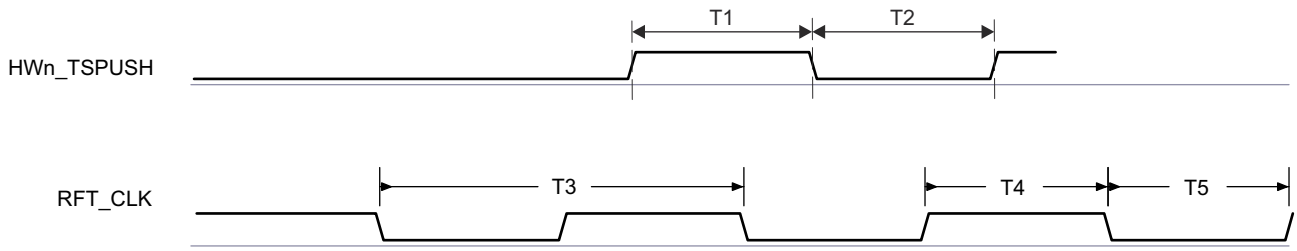

図 6-108. CPTS Timing Requirements

6.9.5.20.2 CPTS Switching Characteristics

see 図 6-109

NO.	PARAMETER		SOURCE	MIN	MAX	UNIT
T6	$t_{w(TS_COMPH)}$	Pulse duration, TS_COMP high		36P - 2[(1)]		ns
T7	$t_{w(TS_COMPL)}$	Pulse duration, TS_COMP low		36P - 2[(1)]		ns
T8	$t_{w(TS_SYNCH)}$	Pulse duration, TS_SYNC high		36P - 2[(1)]		ns
T9	$t_{w(TS_SYNCL)}$	Pulse duration, TS_SYNC low		36P - 2[(1)]		ns
T10	$t_{w(SYNC_OUTH)}$	Pulse duration, SYNCn_OUT[(2)] high	TS_SYNC	36P - 2[(1)]		ns
			TS_GENF	5P - 2[(1)]		ns
T11	$t_{w(SYNC_OUTL)}$	Pulse duration, SYNCn_OUT[(2)] low	TS_SYNC	36P - 2[(1)]		ns
			TS_GENF	5P - 2[(1)]		ns

(1) P = functional clock period in ns.
(2) n = 0 to 3 in SYNCn_OUT

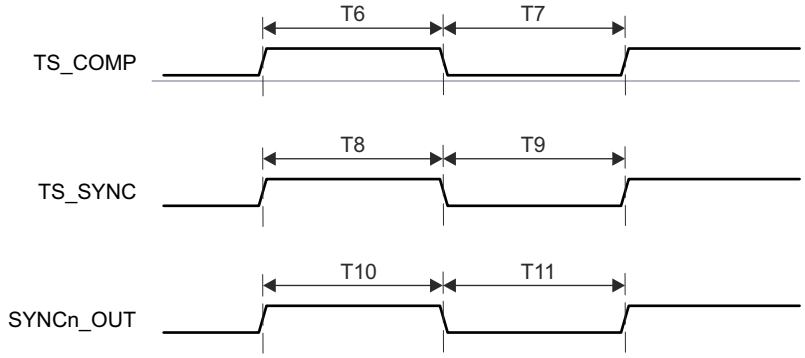

図 6-109. CPTS Switching Characteristics

For more information, see *Navigator Subsystem (NAVSS)* section in *Data Movement Architecture (DMA)* chapter in the device TRM.

6.9.5.21 OSPI

For more details about features and additional description information on the device Octal Serial Peripheral Interface, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

表 6-100 represents OSPI timing conditions.

表 6-100. OSPI Timing Conditions

PARAMETER			MIN	MAX	UNIT
INPUT CONDITIONS					
SR_I	Input slew rate	3.3 V	2	6	V/ns
		All other modes	1	6	V/ns

表 6-100. OSPI Timing Conditions (続き)

PARAMETER			MIN	MAX	UNIT
OUTPUT CONDITIONS					
C_L	Output load capacitance	All modes	3	10	pF
PCB CONNECTIVITY REQUIREMENTS					
$t_{d(Trace\ Delay)}$	Propagation delay OSPI_CLK trace	No Loopback; Internal Pad Loopback		450	ps
	Propagation delay OSPI_LBCLKO trace	External Board Loopback	2*L-30[(2)]	2*L+30[(2)]	ps
	Propagation delay OSPI_DQS trace	DQS	L-30[(2)]	L+30[(2)]	ps
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch OSPI_D[i:0][(1)], OSPI_CSn relative to OSPI_CLK	All modes		60	ps

(1) i in D[i:0] = 0 to 7 for OSPI0; i in [i:0] = 3 for OSPI1
(2) L = Propagation delay of OSPI_CLK trace

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6.9.5.21.1 OSPI PHY Mode

6.9.5.21.1.1 OSPI With Data Training

注

I/O timing requirements and switching characteristics are not applicable when OSPI is used with data training. Follow the セクション 8.3.2, *OSPI and QSPI Board Design and Layout Guidelines* section to ensure proper operation.

6.9.5.21.1.1.1 OSPI Switching Characteristics – Data Training

PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
$t_{c(CLK)}$	Cycle time, CLK	DDR, 1.8V	6		ns
		DDR, 3.3V	7.5		ns
$t_{c(CLK)}$	Cycle time, CLK	SDR, 1.8V	6		ns
		SDR, 3.3V	7.5		ns

6.9.5.21.1.2 OSPI Without Data Training

注

The I/O Timings provided in this section are only applicable when data training is not implemented. Additionally, the I/O Timings are valid only for some OSPI usage modes when the corresponding DLL Delays are configured as described in 表 6-101 found in this section.

セクション 6.9.5.21.1.2.4, セクション 6.9.5.21.1.2.2, セクション 6.9.5.21.1.2, and セクション 6.9.5.21.1.2 present switching characteristics for OSPI DDR and SDR Mode.

6.9.5.21.1.2.1 OSPI Timing Requirements – SDR Mode

表 6-101. OSPI DLL Delay Mapping - SDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE
All modes	PHY_CONFIG_TX_DLL_DELAY_FLD	0x0
	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, D[i:0] valid before active CLK edge(1)	1.8V, Internal Loopback	-2.19		ns
			3.3V, Internal Loopback	-1.71		ns
O20	$t_{h(CLK-D)}$	Hold time, D[i:0] valid after active CLK edge(1)	1.8V, Internal Loopback	7.62		ns
			3.3V, Internal Loopbacl	8.1		ns
O21	$t_{su(D-LBCLK)}$	Setup time, D[i:0] valid before active LBCLK input (DQS) edge(1)	1.8V, External Board Loopback	-3.1		ns
			3.3V, External Board Loopback	-2.72		ns
O22	$t_{h(LBCLK-D)}$	Hold time, D[i:0] valid after active LBCLK input (DQS) edge(1)	1.8V, External Board Loopback	3.81		ns
			3.3V, External Board Loopback	4.33		ns

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1

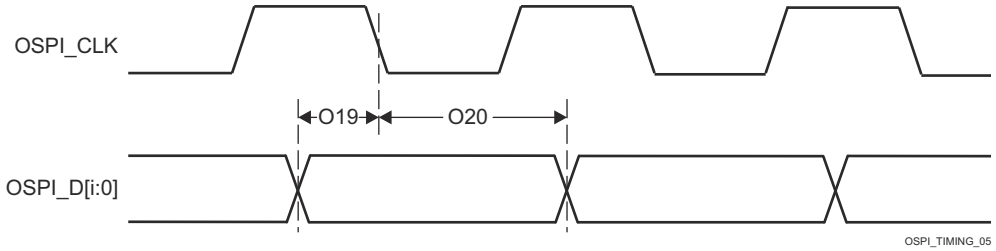

図 6-110. OSPI Timing Requirements – SDR, Internal Clock and Internal Pad Loopback Clock

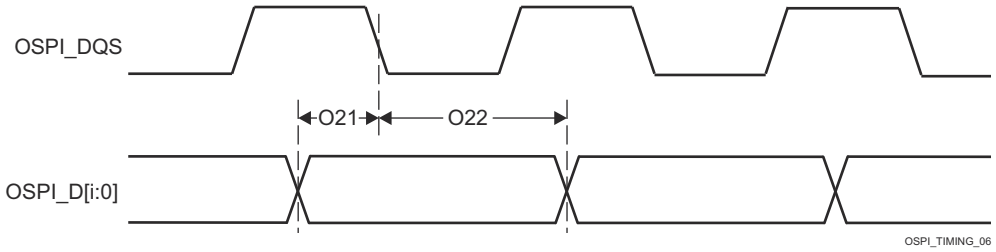

図 6-111. OSPI Timing Requirements – SDR, External Loopback Clock

6.9.5.21.1.2.2 OSPI Switching Characteristics – SDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, CLK	1.8V	7		ns
			3.3V	7.5		ns
O8	$t_{w(CLKL)}$	Pulse duration, CLK low		-0.3+0.475*P (2)		ns
O9	$t_{w(CLKH)}$	Pulse duration, CLK high		-0.3+0.475*P (2)		ns
O10	$t_{d(CLK-CSn)}$	Delay time, CLK rising edge to CSn active edge	1.8V	0.475 * P + 0.975 * N * R (2) (3) (5)	0.475 * P + 0.975 * N * R + 1 (3) (3) (5)	ns
			3.3V	0.475 * P + 0.975 * N * R (2) (3) (5)	0.475 * P + 0.975 * N * R + 1 (2) (3) (5)	ns
O11	$t_{d(CLK-CSn)}$	Delay time, CLK rising edge to CSn inactive edge	1.8V	0.475 * P + 0.975 * N * R - 1 (2) (4) (5)	0.475 * P + 0.975 * N * R + 1 (2) (4) (5)	ns
			3.3V	-1+0.475 * P + 0.975 * N * R (2) (4) (5)	1+0.475 * P + 0.975 * N * R (2) (4) (5)	ns
O12	$t_{d(CLK-D)}$	Delay time, CLK active edge to D[i:0] transition(1)	1.8V	-1.16	1.25	ns
			3.3V	-1.33	1.51	ns

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1
(2) P = CLK cycle time = SCLK period
(3) N = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(4) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(5) R = refclk

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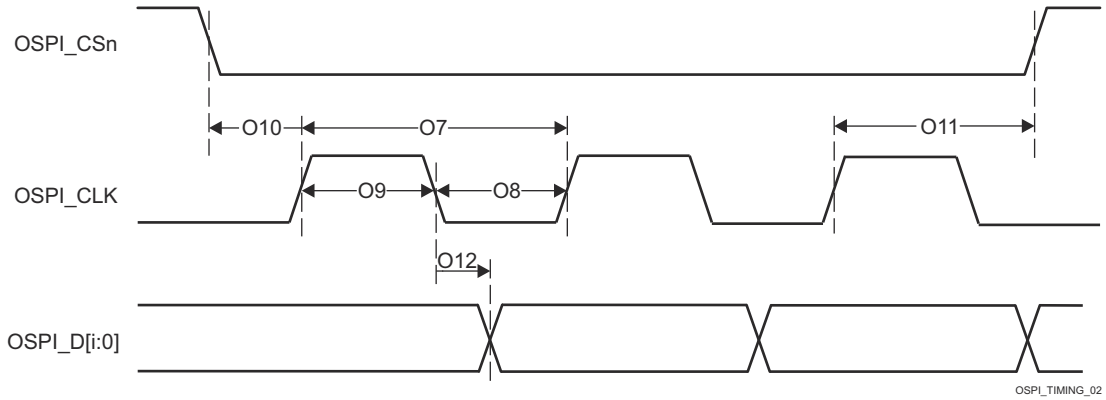

図 6-112. OSPI Switching Characteristics – SDR

セクション 6.9.5.21.1.2.3, セクション 6.9.5.21.1.2.1, セクション 6.9.5.21.1.2.2, セクション 6.9.5.21.1.2.2, and 図 6-111 presents timing requirements for OSPI DDR and SDR Mode.

6.9.5.21.1.2.3 OSPI Timing Requirements – DDR Mode

表 6-102. OSPI DLL Delay Mapping - DDR Timing Modes

MODE	OSPI_PHY_CONFIGURATION_REG BIT FIELD	DELAY VALUE	
		OSPI0	OSPI1
Transmit			
1.8V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x40	0x41
3.3V	PHY_CONFIG_TX_DLL_DELAY_FLD	0x3C	0x3E
Receive			
1.8V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x13	0x15
3.3V, DQS	PHY_CONFIG_RX_DLL_DELAY_FLD	0x1E	0x1E
All other modes	PHY_CONFIG_RX_DLL_DELAY_FLD	0x0	0x0

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O15	$t_{su(D-LBCLK)}$	Setup time, D[i:0] valid before active LBCLK (DQS) edge(1)	1.8V, External Board Loopback	0.52		ns
			3.3V, External Board Loopback	1.97		ns
O16	$t_{h(LBCLK-D)}$	Hold time, D[i:0] valid after active LBCLK (DQS) edge(1)	1.8V, External Board Loopback	1.24 (2)		ns
			3.3V, External Board Loopback	1.44 (2)		ns
O17	$t_{su(D-DQS)}$	Setup time, DQS edge to D[i:0] transition(1)	1.8V, DQS	-0.46		ns
			3.3V, DQS	-0.66		ns
O18	$t_{h(DQS-D)}$	Hold time, DQS edge to D[i:0] transition(1)	1.8V, DQS	3.59		ns
			3.3V, DQS	8.89		ns

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1
(2) This Hold time requirement is larger than the Hold time provided by a typical flash device. Therefore, the trace length between the SoC and flash device must be sufficiently long enough to ensure that the Hold time is met at the SoC. Refer to セクション 8.3.2 for more details.

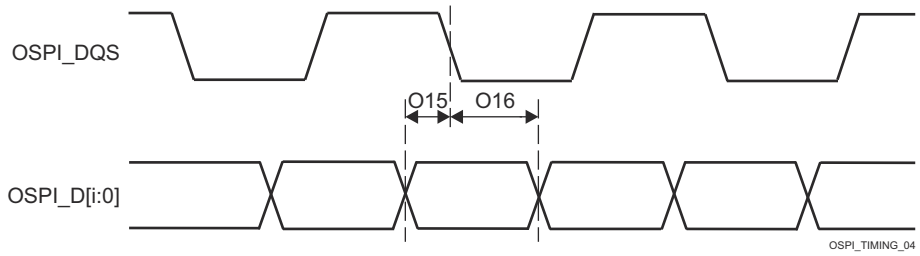

図 6-113. OSPI Timing Requirements – DDR, External Loopback Clock and DQS

6.9.5.21.1.2.4 OSPI Switching Characteristics – DDR Mode

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, CLK	1.8V	19		ns
			3.3V	19		ns
O2	$t_{w(CLKL)}$	Pulse duration, CLK low		0.475*P - 0.3 (2)		ns
O3	$t_{w(CLKH)}$	Pulse duration, CLK high		0.475*P - 0.3 (2)		ns
O4	$t_{d(CLK-CSn)}$	Delay time, CSn active edge to CLK rising edge	1.8V	0.475 * P + 0.975 * N * R (2) (3) (5)	0.475 * P + 0.975 * N * R + 1 (2) (3) (5)	ns
			3.3V	0.475 * P + 0.975 * N * R (2) (3) (5)	0.475 * P + 0.975 * N * R + 1 (2) (3) (5)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, CLK rising edge to CSn inactive edge	1.8V	0.475 * P + 0.975 * N * R - 7 (2) (4) (5)	0.475 * P + 0.975 * N * R (2) (4) (5)	ns
			3.3V, OSPI0 DDR TX; 3.3V, OSPI1 DDR TX	0.475 * P + 0.975 * N * R - 7 (2) (4) (5)	0.475 * P + 0.975 * N * R (2) (4) (5)	ns
O6	$t_{d(CLK-D)}$	Delay time, CLK active edge to D[i:0] transition (1)	1.8V, OSPI0 DDR TX; 1.8V, OSPI1 DDR TX	-7.71	-1.56	ns
			3.3V, OSPI0 DDR TX; 3.3V, OSPI1 DDR TX	-7.71	-1.56	ns

(1) i in [i:0] = 7 for OSPI0, i in [i:0] = 3 for OSPI1
(2) P = CLK cycle time = SCLK period
(3) N = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(4) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(5) R = refclk

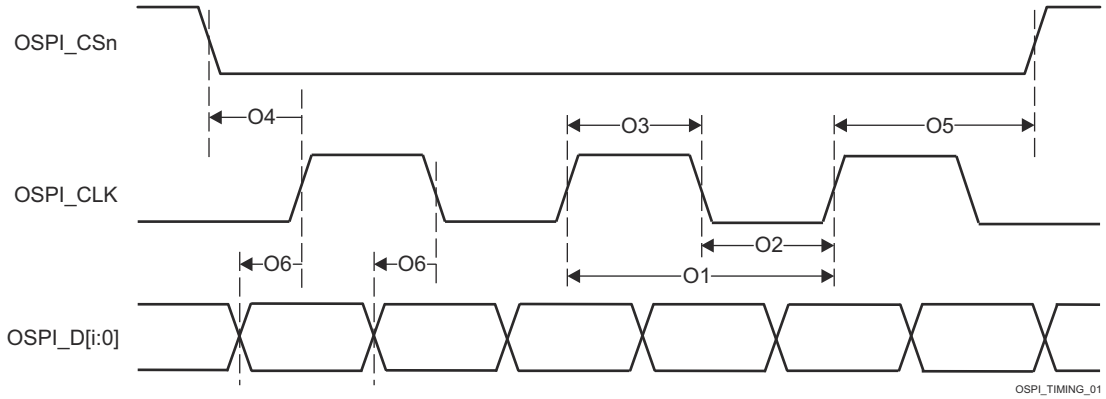

図 6-114. OSPI Switching Characteristics – DDR

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6.9.5.21.2 OSPI Tap Mode

6.9.5.21.2.1 OSPI Tap SDR Timing

表 6-103, 図 6-115, 表 6-104, and 図 6-116 present timing requirements and switching characteristics for OSPI0 Tap SDR Mode.

表 6-103. OSPI Timing Requirements – Tap SDR Mode

see 図 6-115

NO.			MODE	MIN	MAX	UNIT
O19	$t_{su(D-CLK)}$	Setup time, OSPI_D[7:0] valid before active OSPI_CLK edge	No Loopback	(10.4 - (0.975T(1)R(2)))		ns
O20	$t_{h(CLK-D)}$	Hold time, OSPI_D[7:0] valid after active OSPI_CLK edge	No Loopback	(–0.2 + (0.975T(1)R(2)))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = reference clock cycle time in ns

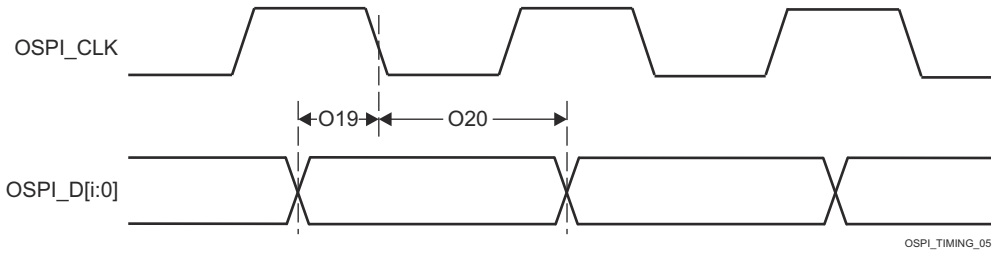

図 6-115. OSPI Timing Requirements – Tap SDR, No Loopback

表 6-104. OSPI0/1 Switching Characteristics – Tap SDR Mode

see 図 6-116

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O7	$t_{c(CLK)}$	Cycle time, OSPI0/1_CLK		20		ns
O8	$t_{w(CLKL)}$	Pulse duration, OSPI0/1_CLK low		((0.475P(1)) - 0.3)		ns
O9	$t_{w(CLKH)}$	Pulse duration, OSPI0/1_CLK high		((0.475P(1)) - 0.3)		ns
O10	$t_{d(CSn-CLK)}$	Delay time, OSPI0/1_CSn[3:0] active edge to OSPI0/1_CLK rising edge		((0.475P(1)) + (0.975M(2)R(4)) - 1.5)	((0.525P(1)) + (1.025M(2)R(4)) + 1.5)	ns
O11	$t_{d(CLK-CSn)}$	Delay time, OSPI0/1_CLK rising edge to OSPI0/1_CSn[3:0] inactive edge		((0.475P(1)) + (0.975N(3)R(4)) - 1.5)	((0.525P(1)) + (1.025N(3)R(4)) + 1.5)	ns
O12	$t_{d(CLK-D)}$	Delay time, OSPI0/1_CLK active edge to OSPI0/1_D[7:0] transition		–2	2	ns

(1) P = SCLK cycle time in ns = OSPI0/1_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) R = reference clock cycle time in ns

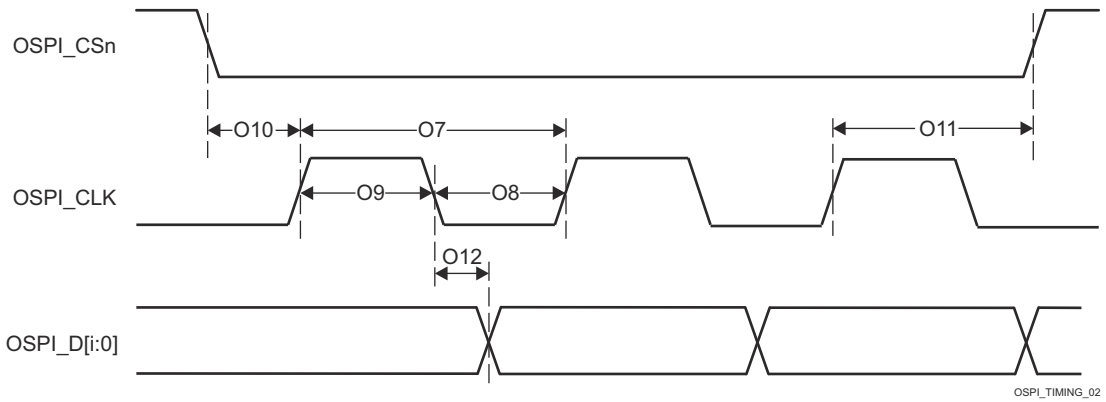

図 6-116. OSPI Switching Characteristics – Tap SDR, No Loopback

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6.9.5.21.2.2 OSPI Tap DDR Timing

表 6-105, 図 6-117, 表 6-106, and 図 6-118 present timing requirements and switching characteristics for OSPI0 Tap DDR Mode.

表 6-105. OSPI Timing Requirements – Tap DDR Mode

see 図 6-117

NO.			MODE	MIN	MAX	UNIT
O13	$t_{su(D-CLK)}$	Setup time, OSPI0/1_D[7:0] valid before active OSPI0/1_CLK edge	No Loopback	(12.04 - (0.975T(1)R(2)))		ns
O14	$t_{h(CLK-D)}$	Hold time, OSPI0/1_D[7:0] valid after active OSPI0/1_CLK edge	No Loopback	(1.84 + (0.975T(1)R(2)))		ns

(1) T = OSPI_RD_DATA_CAPTURE_REG[DELAY_FLD]
(2) R = reference clock cycle time in ns

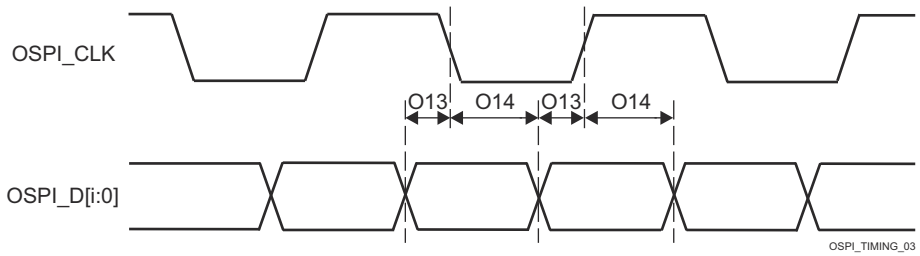

図 6-117. OSPI Timing Requirements – Tap DDR, No Loopback

表 6-106. OSPI0/1 Switching Characteristics – Tap DDR Mode

see 図 6-118

NO.	PARAMETER		MODE	MIN	MAX	UNIT
O1	$t_{c(CLK)}$	Cycle time, OSPI0/1_CLK		40		ns
O2	$t_{w(CLKL)}$	Pulse duration, OSPI0/1_CLK low		((0.475P[1]) - 0.3)		ns
O3	$t_{w(CLKH)}$	Pulse duration, OSPI0/1_CLK high		((0.475P[1]) - 0.3)		ns
O4	$t_{d(CSn-CLK)}$	Delay time, OSPI0/1_CSn[3:0] active edge to OSPI0/1_CLK rising edge		((0.475P[1]) + ((0.975M[2]R[5]) - 1.5)	((0.525P[1]) + (1.025M[2]R[5]) + 1.5)	ns
O5	$t_{d(CLK-CSn)}$	Delay time, OSPI0/1_CLK rising edge to OSPI0/1_CSn[3:0] inactive edge		((0.475P[1]) + (0.975N[3]R[5]) - 1.5)	((0.525P[1]) + (1.025N[3]R[5]) + 1.5)	ns
O6	$t_{d(CLK-D)}$	Delay time, OSPI0/1_CLK active edge to OSPI0/1_D[7:0] transition		(–17.94 + (0.975(T[4] + 1)R[5]))	(–1.56 + (1.025(T[4] + 1)R[5]))	ns

(1) P = SCLK cycle time in ns = OSPI0_CLK cycle time in ns
(2) M = OSPI_DEV_DELAY_REG[D_INIT_FLD]
(3) N = OSPI_DEV_DELAY_REG[D_AFTER_FLD]
(4) T = OSPI_RD_DATA_CAPTURE_REG[DDR_READ_DELAY_FLD]
(5) R = reference clock cycle time in ns

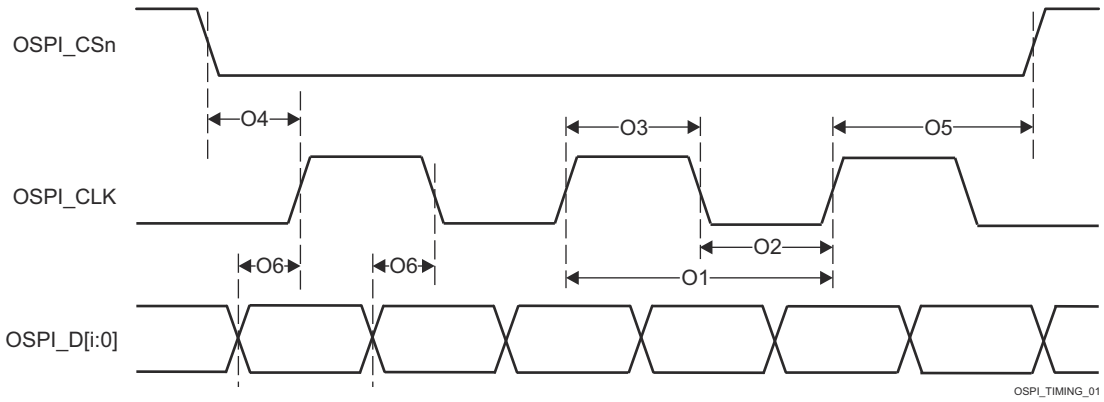

図 6-118. OSPI Switching Characteristics – Tap DDR, No Loopback

6.9.5.22 PCIE

The PCI-Express Subsystem is compliant with the PCIe® Base Specification, Revision 4.0. Refer to the specification for timing details.

For more details about features and additional description information on the device Peripheral Component Interconnect Express, see the corresponding sections within , セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter in the device TRM.

6.9.5.23 Timers

For more details about features and additional description information on the device Timers, see the corresponding sections within , セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

表 6-107 represents Timers timing conditions.

表 6-107. Timers Timing Conditions

PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
INPUT CONDITIONS					

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表 6-107. Timers Timing Conditions (続き)

PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
SR_I	Input slew rate	CAPTURE	0.5	5	V/ns
OUTPUT CONDITIONS					
C_L	Output load capacitance	PWM	2	10	pF

セクション 6.9.5.23.1, セクション 6.9.5.23.2 and 図 6-119 present timings and switching characteristics of the Timers.

6.9.5.23.1 Timing Requirements for Timers

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T1	$t_{w(TINPH)}$	Pulse duration, high	CAPTURE	2.5 + 4P[(1)]		ns
T2	$t_{w(TINPL)}$	Pulse duration, low	CAPTURE	2.5 + 4P[(1)]		ns

(1) P = functional clock period in ns.

6.9.5.23.2 Switching Characteristics for Timers

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
T3	$t_{w(TOUTH)}$	Pulse duration, high	PWM	-2.5 + 4P[(1)]		ns
T4	$t_{w(TOUTL)}$	Pulse duration, low	PWM	-2.5 + 4P[(1)]		ns

(1) P = functional clock period in ns.

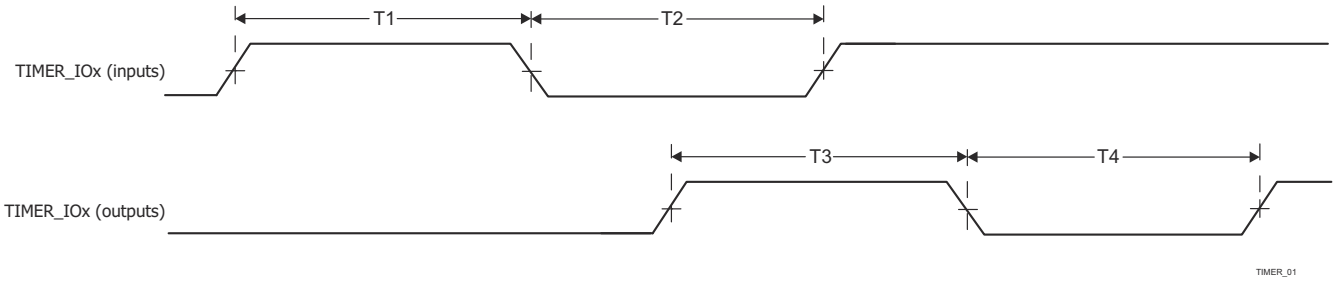

図 6-119. Timer Timing

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

6.9.5.24 UART

For more details about features and additional description information on the device Universal Asynchronous Receiver Transmitter, see the corresponding sections within , セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

表 6-108 represents UART timing conditions.

表 6-108. UART Timing Conditions

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
INPUT CONDITIONS				
SR_I	Input slew rate	0.5	5	V/ns
OUTPUT CONDITIONS				
C_L	Output load capacitance	1	30	pF
PCB CONNECTIVITY REQUIREMENTS				

表 6-108. UART Timing Conditions (続き)

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
$t_{d(Trace\ Mismatch\ Delay)}$	Propagation delay mismatch across all traces		100	ps

セクション 6.9.5.24.1, セクション 6.9.5.24.2, and 図 6-120 present timing requirements and switching characteristics for UART interface.

6.9.5.24.1 Timing Requirements for UART

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
4	$t_{w(rxd)}$	Pulse width, receive data bit, high or low		0.95U[(1)]	1.05U[(1)]	ns
5	$t_{w(rxdS)}$	Pulse width, receive start bit, low		0.95U[(1)]		ns

(1) U = UART baud time = 1/Programmed baud rate

6.9.5.24.2 UART Switching Characteristics

NO.	PARAMETER	DESCRIPTION	MODE	MIN	MAX	UNIT
	$f_{op(baud)}$	Maximum programmable baud rate	15 pF		12	MHz
			30 pF		0.115	
1	$t_{d(ctsnL\text{-}txdV)}$	Delay time, receive CTSn bit to transmit data		30		ns
2	$t_{w(txd)}$	Pulse width, transmit data bit, high or low		U - 2[(1)]	U + 2[(1)]	ns
3	$t_{w(txdS)}$	Pulse width, transmit start bit, low		U - 2[(1)]		ns

(1) U = UART baud time = 1/Programmed baud rate

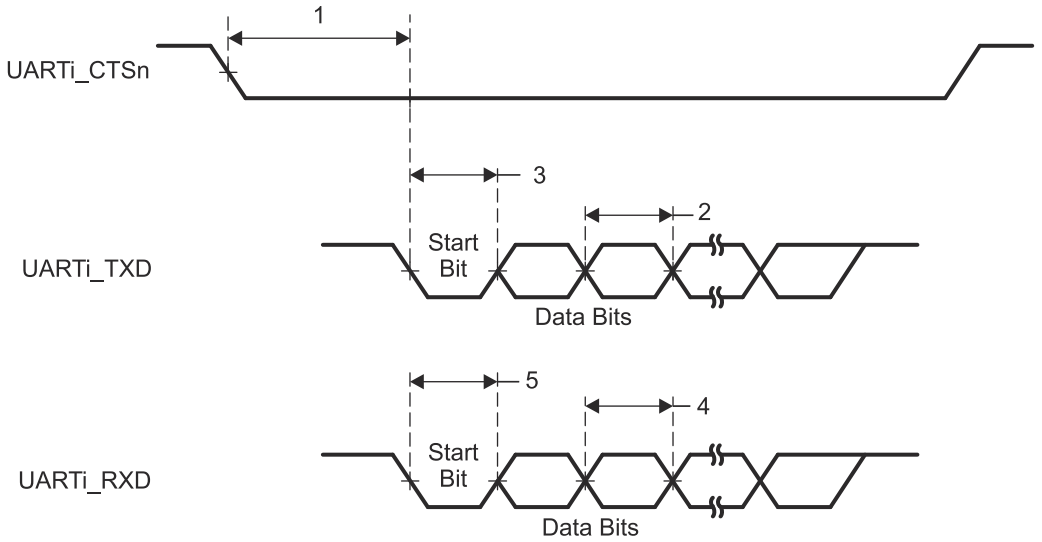

図 6-120. UART Timing

For more information, see *Universal Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

6.9.5.25 USB

The USB 2.0 subsystem is compliant with the Universal Serial Bus (USB) Specification, revision 2.0. Refer to the specification for timing details.

The USB 3.1 GEN1 Dual-Role Device Subsystem is compliant with the Universal Serial Bus (USB) 3.1 Specification, revision 1.0. Refer to the specification for timing details.

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For more details about features and additional description information on the device Universal Serial Bus Subsystem (USB), see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

6.9.6 Emulation and Debug

6.9.6.1 Trace

表 6-109. Trace Timing Conditions

PARAMETER		MIN	MAX	UNIT
OUTPUT CONDITIONS				
C_L	Output load capacitance	2	5	pF
PCB CONNECTIVITY REQUIREMENTS				
$t_{d(Trace\ Mismatch)}$	Propagation delay mismatch across all traces		200	ps

表 6-110 and 図 6-121 assume testing over the recommended operating conditions and electrical characteristic conditions.

表 6-110. Trace Switching Characteristics

NO.	PARAMETER		MIN	MAX	UNIT
1.8 V Mode					
DBTR1	$t_{c(TRC_CLK)}$	Cycle time, TRC_CLK	6.50		ns
DBTR2	$t_{w(TRC_CLKH)}$	Pulse width, TRC_CLK high	2.50		ns
DBTR3	$t_{w(TRC_CLKL)}$	Pulse width, TRC_CLK low	2.50		ns
DBTR4	$t_{osu(TRC_DATAV-TRC_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	0.81		ns
DBTR5	$t_{oh(TRC_CLK-TRC_DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	0.81		ns
DBTR6	$t_{osu(TRC_CTLV-TRC_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	0.81		ns
DBTR7	$t_{oh(TRC_CLK-TRC_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	0.81		ns
3.3 V Mode					
DBTR1	$t_{c(TRC_CLK)}$	Cycle time, TRC_CLK	9.75		ns
DBTR2	$t_{w(TRC_CLKH)}$	Pulse width, TRC_CLK high	4.13		ns
DBTR3	$t_{w(TRC_CLKL)}$	Pulse width, TRC_CLK low	4.13		ns
DBTR4	$t_{osu(TRC_DATAV-TRC_CLK)}$	Output setup time, TRC_DATA valid to TRC_CLK edge	1.22		ns
DBTR5	$t_{oh(TRC_CLK-TRC_DATAI)}$	Output hold time, TRC_CLK edge to TRC_DATA invalid	1.22		ns
DBTR6	$t_{osu(TRC_CTLV-TRC_CLK)}$	Output setup time, TRC_CTL valid to TRC_CLK edge	1.22		ns
DBTR7	$t_{oh(TRC_CLK-TRC_CTLI)}$	Output hold time, TRC_CLK edge to TRC_CTL invalid	1.22		ns

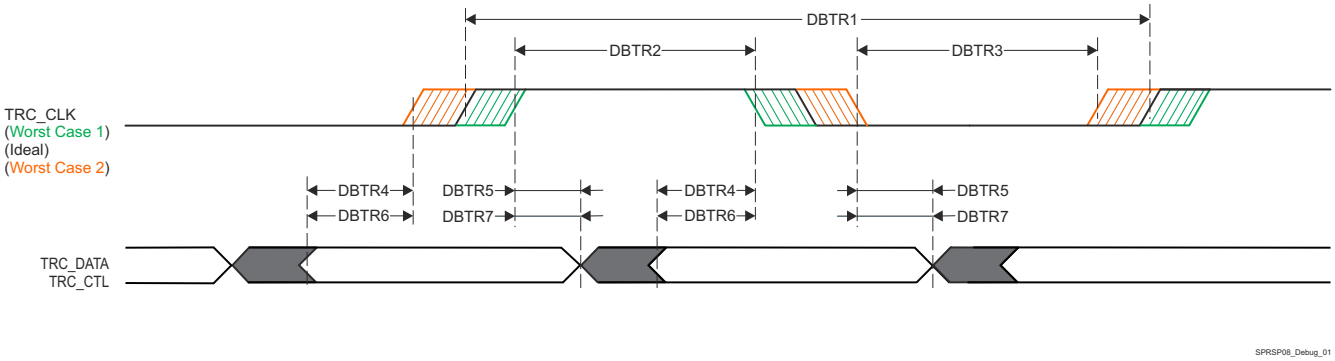

図 6-121. Trace Switching Characteristics

6.9.6.2 JTAG

For more details about features and additional description information on the device IEEE 1149.1 Standard–Test–Access Port, see the corresponding sections within セクション 5.3, *Signal Descriptions* and セクション 7, *Detailed Description*.

表 6-111. JTAG Timing Conditions

PARAMETER		MIN	MAX	UNIT
Input Conditions				
SR_I	Input slew rate	0.25	2.00	V/ns
Output Conditions				
C_L	Output load capacitance	5	15	pF

6.9.6.2.1 JTAG Electrical Data and Timing

セクション 6.9.6.2.1.1, セクション 6.9.6.2.1.2, and 図 6-122 assume testing over the recommended operating conditions and electrical characteristic conditions.

6.9.6.2.1.1 JTAG Timing Requirements

See 図 6-122

NO.			MIN	MAX	UNIT
J1	$t_{c(TCK)}$	Cycle time minimum, TCK	100		ns
J2	$t_{w(TCKH)}$	Pulse width minimum, TCK high	40		ns
J3	$t_{w(TCKL)}$	Pulse width minimum, TCK low	40		ns
J4	$t_{su(TDI-TCK)}$	Input setup time minimum, TDI valid to TCK high	13		ns
	$t_{su(TMS-TCK)}$	Input setup time minimum, TMS valid to TCK high	13		ns
J5	$t_{h(TCK-TDI)}$	Input hold time minimum, TDI valid from TCK high	7.7		ns
	$t_{h(TCK-TMS)}$	Input hold time minimum, TMS valid from TCK high	7.7		ns

1. The JTAG signals are split across two IO power domains on the device. Timings parameters defined in this table only apply when the two IO power domains are operating at the same voltage. Values for these timing parameters are not defined when operating the two IO power domains at different voltages since propagation delay through the device IO buffers differ when some are operating at 1.8V while others are operating at 3.3V. This effectively reduces timing margin beyond the values defined in this table. The JTAG interface is still expected to function when the two IO power domains are operated at different voltages, assuming the system designer has implemented appropriate level shifters and the operating frequency is reduced to accommodate additional delay inserted by the level-shifters and IO buffers operating at different voltages.

6.9.6.2.1.2 JTAG Switching Characteristics

See 図 6-122

NO.	PARAMETER		MIN	MAX	UNIT
J6	$t_{d(TCKL-TDOI)}$	Delay time minimum, TCK low to TDO invalid	0		ns
J7	$t_{d(TCKL-TDOV)}$	Delay time maximum, TCK low to TDO valid		37.75	ns

1. The JTAG signals are split across two IO power domains on the device. Timings parameters defined in this table only apply when the two IO power domains are operating at the same voltage. Values for these timing parameters are not defined when operating the two IO power domains at different voltages since propagation delay through the device IO buffers differ when some are operating at 1.8V while others are operating at 3.3V. This effectively reduces timing margin beyond the values defined in this table. The JTAG interface is still expected to function when the two IO power domains are operated at different voltages, assuming the system designer has implemented appropriate level shifters and the operating frequency is

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reduced to accommodate additional delay inserted by the level-shifters and IO buffers operating at different voltages.

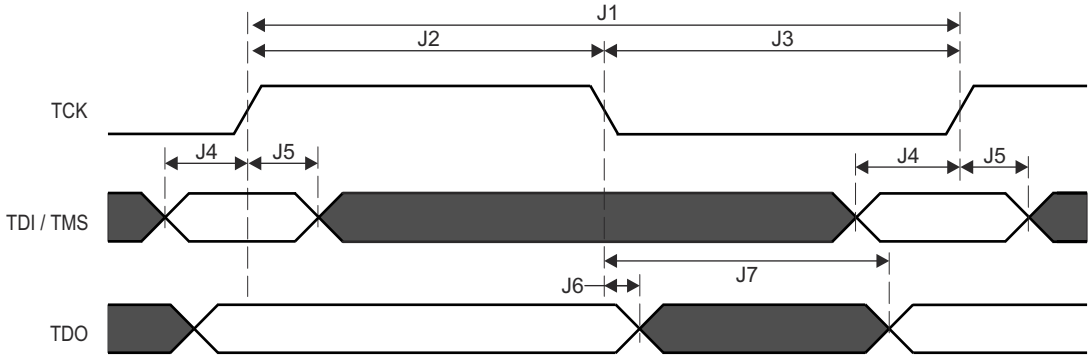

図 6-122. JTAG Timing Requirements and Switching Characteristics

7 Detailed Description

7.1 Overview

The TDA4VM processor family is based on the evolutionary Jacinto 7 architecture, targeted at ADAS and Autonomous Vehicle (AV) applications and built on extensive market knowledge accumulated over a decade of TI's leadership in the ADAS processor market. The TDA4VM provides high performance compute for both traditional and deep learning algorithms at industry leading power/performance ratios with a high level of system integration to enable scalability and lower costs for advanced automotive platforms supporting multiple sensor modalities in centralized ECUs or stand-alone sensors. Key cores include next generation DSP with scalar and vector cores, dedicated deep learning and traditional algorithm accelerators, latest Arm and GPU processors for general compute, an integrated next generation imaging subsystem (ISP), video codec, Ethernet hub and isolated MCU island. All protected by automotive grade safety and security hardware accelerators.

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For more information on features, subsystems, and architecture of superset device System on Chip (SoC), see the device TRM.

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7.2 Processor Subsystems

7.2.1 Arm Cortex-A72

The device implements one dual-core Arm® Cortex®-A72 MPU, which is integrated inside the Compute Cluster, along with other modules. The Cortex-A72 cores are general-purpose processors that can be used for running customer applications.

The A72SS is built around the Arm Cortex-A72 MPCore (A72 cluster), which is provided by Arm and configured by TI. It is based on the symmetric multiprocessor (SMP) architecture, and thus it delivers high performance and optimal power management and debug capabilities.

The A72 processor is a multi-issue out-of-order superscalar execution engine with integrated L1 instruction and data caches, compatible with Armv8-A architecture. The Armv8-A architecture brings a number of new features. These include 64-bit data processing, extended virtual addressing and 64-bit general purpose registers.

For more information, see *Dual-A72 MPU Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

7.2.2 Arm Cortex-R5F

The MCU_ARMSS is a dual-core implementation of the Arm® Cortex®-R5F processor configured for split/lock operation. It also includes accompanying memories (L1 caches and tightly-coupled memories), standard Arm® CoreSight™ debug and trace architecture, integrated Vectored Interrupt Manager (VIM), ECC Aggregators, and various wrappers for protocol conversion and address translation for easy integration into the SoC.

For more information, see *Dual-R5F MCU Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

7.2.3 DSP C71x

The TMS320C71x is the next-generation fixed and floating-point DSP platform. The C71x DSP is a new core in the Texas Instruments' DSP family. The C71x DSP supports vector signal processing, providing significant lift in DSP processing power over a broad range of general signal processing tasks in comparison to the C6x DSP family. In addition, the C71x provides several specialized functions which accelerate targeted functions by more than 30 times. Besides expanding vector processing capabilities, the new C71x core also incorporates advanced techniques to improve control code efficiency and ease of programming such as branch prediction, protected pipeline, precise exception and virtual memory management.

For more information, see *C71x DSP Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

7.2.4 DSP C66x

The C66x subsystem is based on the TI's standard TMS320C66x DSP CorePac module. It includes subsystem logic to ease the C66x CorePac integration into the SoC, while maximizing software reuse from previous devices.

The C66x DSP extends the performance of the C64x+ and C674x DSPs through enhancements and new features. Many of the new features target increased performance for vector processing. The C64x+ and C674x DSPs support 2-way SIMD operations for 16-bit data and 4-way SIMD operations for 8-bit data. On C66x DSP, the vector processing capability is improved by extending the width of the SIMD instructions.

The C66x DSP can execute instructions that operate on 128-bit vectors. For example, the QMPY32 instruction is able to perform the element-to-element multiplication between two vectors of four 32-bit data each. The C66x DSP also supports SIMD for floating-point operations. Improved vector processing capability (each instruction can process multiple data in parallel) combined with the natural instruction level parallelism of C6000 architecture (for example, execution of up to eight instructions per cycle) results in a very high level of parallelism that can be exploited by DSP programmers through the use of TI's optimized C/C++ compiler.

For more information, see *C66x DSP Subsystem* section in *Processors and Accelerators* chapter in the device TRM.

7.3 Accelerators and Coprocessors

7.3.1 GPU

The Graphics Processing Unit (GPU) accelerates 3-dimensional (3D) and 2-dimensional (2D) graphics and compute applications.

The GPU module is a scalable architecture which efficiently processes a number of different workload concurrently:

- 3D Graphic Workload, which involves vertex data and pixel data processing for rendering of 3D scenes.
- 2D Graphic Workload, which involves pixel data processing for rendering 2D objects.
- Compute Applications Workload, which involves general purpose data processing.

For more information, see *Graphics Accelerator (GPU)* section in *Processors and Accelerators* chapter in the device TRM.

7.3.2 VPAC

The Vision Pre-processing Accelerator (VPAC) is a set of common vision primitive functions, performing memory-to-memory (M2M) pixel data processing tasks, such as: color processing and enhancement, noise filtering, wide dynamic range (WDR) processing, lens distortion correction, pixel remap for dewarping, on-the-fly scale generation, on-the-fly pyramid generation. The VPAC offloads these common tasks from the main SoC processors (ARM, DSP, etc.), so these CPUs can be utilized for differentiated high-level algorithms. The VPAC is designed to support multiple cameras by working in time-multiplexing mode. The VPAC works as front end to vision processing and prepares frame/scales for further processing by other vision accelerators or processor cores in the SoC.

For more information, see *Vision Pre-processing Accelerator (VPAC)* section in *Processors and Accelerators* chapter in the device TRM.

7.3.3 DMPAC

The Depth and Motion Perception Accelerator (DMPAC) is a power efficient hardware accelerator that computes dense stereo depth maps (*depth*) and dense optical flow vectors (*motion*) from camera inputs.

The image/video sensor-based environmental perception (also known as scene understanding) is at the core of many emerging applications in automotive, industrial and consumer electronics. Typically, this involves detection of all objects in the scene along with their 3D position and motion with regards to the observer or the car by analyzing one or many related input video streams. Various computer vision algorithms are used to achieve these tasks.

A very robust method of obtaining the 3D depth from images is to use two cameras in a stereo setup - two cameras with known relative positions and camera parameters. The two images of the same scene, captured from two different camera poses/perspectives, are analyzed to find disparities among every pixel positions in the images. This is known as the Stereo Disparity map. The disparity values of every pixel can be used to obtain the 3D positions of the object/space they belong to via triangulation.

On the other hand, by analyzing two images from a single camera, captured at two different time instances (that is, two temporal frames in a video), one can determine where each pixel in a past frame moved to in the future frame. This is known as the Optical Flow vector. The flow vectors for each pixel position can be used to obtain 3D structure of the scene, identify moving objects and determine their relative speed and direction of motion.

The DMPAC is dedicated to the aforesaid image processing tasks. The stereo and optical flow processing is partitioned into two top level sub-blocks: the Dense Optical Flow (DOF) engine and the Stereo Disparity Engine (SDE). The DOF and SDE blocks share a common shared local memory, DMA, external messaging and control infrastructure.

For more information, see *Depth and Motion Perception Accelerator (DMPAC)* section in *Processors and Accelerators* chapter in the device TRM.

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7.3.4 D5520MP2

The DECODER module is a D5520MP2 dual-core PowerVR® VPU (video processor unit).

The D5520MP2 is capable of supporting:

- 1x 4kp60 decode or
- 2x 4kp30 decodes or
- 4x 1080p60 decodes or
- 8x 1080p30 decodes

For more information, see *Multi-Standard HD Video Decoder (D5520MP2)* section in *Processors and Accelerators* chapter in the device TRM.

7.3.5 VXE384MP2

The ENCODER module is a VXE384MP2 core PowerVR® VPU (video processor unit).

The VXE384MP2 is capable of supporting:

- 1x 1080p60 video stream encoding or
- 2x or 3x 1080p30 video stream encodings

For more information, see *Multi-Standard HD Video Encoder (VXE384MP2)* section in *Processors and Accelerators* chapter in the device TRM.

7.4 Other Subsystems

7.4.1 MSMC

The Multicore Shared Memory Controller (MSMC) forms the heart of the compute cluster (COMPUTE_CLUSTER0) providing high-bandwidth resource access both to and from all of the connected processing elements and the rest of the system. MSMC serves as the data-movement backbone of the compute cluster.

For more information, see *Multicore Shared Memory Controller (MSMC)* section in *Device Configuration* chapter in the device TRM.

7.4.2 NAVSS

7.4.2.1 NAVSS0

Main SoC Navigator Subsystem (NAVSS0) consists of DMA/Queue Management components – UDMA and Ring Accelerator (UDMASS), Peripherals (Module subsystem [MODSS]), Virtualization translation (VirtSS), and a North Bridge (NBSS).

7.4.2.2 MCU_NAVSS

MCU Navigator Subsystem (MCU NAVSS) has a subset of the modules of the main NAVSS and is instantiated in the MCU domain.

MCU Navigator Subsystem consists of DMA/Queue Management components – UDMA and Ring Accelerator (UDMASS), and Peripherals (Module subsystem [MODSS]).

For more information, see *Main Navigator Subsystem (NAVSS)* and *MCU Navigator Subsystem (MCU NAVSS)* sections in the device TRM.

7.4.3 PDMA Controller

The Peripheral DMA is a simple DMA which has been architected to specifically meet the data transfer needs of peripherals, which perform data transfers using memory mapped registers accessed via a standard non-coherent bus fabric. The PDMA module is intended to be located close to one or more peripherals which require an external DMA for data movement and is architected to reduce cost by using VBUSP interfaces and supporting only statically configured Transfer Request (TR) operations.

The PDMA is only responsible for performing the data movement transactions which interact with the peripherals themselves. Data which is read from a given peripheral is packed by a PDMA source channel into a PSI-L data stream which is then sent to a remote peer UDMA-P destination channel which then performs the movement of the data into memory. Likewise, a remote UDMA-P source channel fetches data from memory and transfers it to a peer PDMA destination channel over PSI-L which then performs the writes to the peripheral.

The PDMA architecture is intentionally heterogeneous (UDMA-P + PDMA) to right size the data transfer complexity at each point in the system to match the requirements of whatever is being transferred to or from. Peripherals are typically FIFO based and do not require multi-dimensional transfers beyond their FIFO dimensioning requirements, so the PDMA transfer engines are kept simple with only a few dimensions (typically for sample size and FIFO depth), hardcoded address maps, and simple triggering capabilities.

Multiple source and destination channels are provided within the PDMA which allow multiple simultaneous transfer operations to be ongoing. The DMA controller maintains state information for each of the channels and employs round-robin scheduling between channels in order to share the underlying DMA hardware.

For more information, see *PDMA Controller* section in *DMA Controllers* chapter in the device TRM.

7.4.4 Power Supply

The device requires 6 power supply types and 1 internal LDO connection type, see *Power Supply Signal Descriptions*:

- Digital IO Voltages
- Digital Low Voltages

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- Digital AVS Voltage
- Analog PHY & CLK Voltages
- Analog Low Voltages
- Efuse Programming Voltages
- LDO Bulk Filter Capacitors

Common device power supply input types can be grouped together into power rails. All power rails must be supplied by power resources designed to support the most strigent power supply voltage specification and total load current demands. Two recommended Power Distribution Networks (PDNs) have been defined that either combine or isolate MCU and Main domains, (refer to セクション 8.1, *Power Supply Mapping*).

It is possible that a few power supply inputs may not be needed in some systems. In such cases, all unused supply inputs, other than VPP_CORE & VPP_MCU, must be connected to a valid power rail with a proper voltage level in order to ensure device reliability (refer to セクション 6.4, *Recommended Operating Conditions*). The following examples are given for reference:

1. If MCU Island safety monitor or MCU Only low power processing are not used, then VDD_MCU supply can be combined with the VDD_CORE supply with compatible operating voltage specification.
2. If UHS-I SD Card or USB2.0 interface is not needed, then VDDSHV5 (MMC1 interface) and VDDA_USB_3P3 (USB PHY interface) can be combined with VDD_IO_3V3 digital IO power rail.
3. If General Purpose device type is used, then Efuse programming voltages VPP_CORE & VPP_MCU are not needed and should be left unconnected.

7.4.5 Peripherals

7.4.5.1 ADC

The Analog-to-Digital Converter (ADC) module contains a single 12-bit ADC which can be multiplexed to any 1 of 8 analog inputs (channels).

For more information, see *Analog-to-Digital Converter (ADC)* section in *Peripherals* chapter in the device TRM.

7.4.5.2 ATL

The Audio Tracking Logic (ATL) is used by HD Radio™ applications to synchronize the digital audio output to the baseband clock. This same IP can also be used generically to track errors between two reference signals (such as frame syncs) and generate a modulated clock output (using software-controlled cycle stealing) which averages to some desired frequency. This process can be used as a hardware assist for asynchronous sample rate conversion algorithms.

For more information, see *Audio Tracking Logic (ATL)* section in *Peripherals* chapter in the device TRM.

7.4.5.3 CSI

7.4.5.3.1 Camera Streaming Interface Receiver (CSI_RX_IF) and MIPI DPHY Receiver (DPHY_RX)

The integration of the CSI_RX_IF module allows the device to stream video inputs from multiple cameras to the image processing accelerator (VPAC) or to internal memory. The video input may also be retransmitted via the transmitter CSI (CSI_TX_IF) for debug and test purposes.

For more information, see *Camera Streaming Interface (CSI)* section in *Peripherals* chapter in the device TRM.

7.4.5.3.2 Camera Streaming Interface Transmitter (CSI_TX_IF)

The integration of the CSI_TX_IF module allows the device to stream out video data from memory, or retransmit from the CSI receivers as an optional loopback output for diagnostics, debug, and test purposes.

For more information, see *Camera Streaming Interface (CSI)* section in *Peripherals* chapter in the device TRM.

7.4.5.4 CPSW2G

The two-port Gigabit Ethernet MAC (MCU_CPSW0) subsystem provides Ethernet packet communication for the device and is configured in a similar manner as an Ethernet switch. MCU_CPSW0 features the Reduced Gigabit

Media Independent Interface (RGMII), Reduced Media Independent Interface (RMII), and the Management Data Input/Output (MDIO) interface for physical layer device (PHY) management.

For more information, see *Gigabit Ethernet Switch (CPSW0)* section in *Peripherals* chapter in the device TRM.

7.4.5.5 CPSW9G

The 9-port Gigabit Ethernet Switch (CPSW0) subsystem provides Ethernet packet communication for the device and can be configured as an Ethernet switch. CPSW0 features the Serial Gigabit Media Independent Interface (SGMII), Reduced Gigabit Media Independent Interface (RGMII), Reduced Media Independent Interface (RMII) and the Management Data Input/Output (MDIO) interface for physical layer device (PHY) management.

For more information, see *Gigabit Ethernet Switch (MCU_CPSW0)* section in *Peripherals* chapter in the device TRM.

7.4.5.6 DCC

The Dual Clock Comparator (DCC) is used to determine the accuracy of a clock signal during the time execution of an application. Specifically, the DCC is designed to detect drifts from the expected clock frequency. The desired accuracy can be programed based on calculation for each application. The DCC measures the frequency of a selectable clock source using another input clock as a reference.

For more information, see *Dual Clock Comparator (DCC)* section in *Peripherals* chapter in the device TRM.

7.4.5.7 DDRSS

The DDR subsystem in this device comprises DDR controller, DDR PHY and wrapper logic to integrate these blocks in the device. The DDR subsystem is referred to as DDRSS0 and is used to provide an interface to external SDRAM devices which can be utilized for storing program or data. DDRSS0 is accessed via MSMC, and not directly through the system interconnect.

For more information, see *DDR Subsystem (DDRSS)* section in *Peripherals* chapter in the device TRM.

7.4.5.8 DSS

The DSS is a flexible composition-enabled display subsystem, that supports multiple high resolution display outputs. It consists of one Display Controller (DISPC) and one Frame Buffer Decompression Core (FBDC). The DISPC supports a multi-layer blending and transparency for each of its display outputs. The DISPC also supports a write-back pipeline with scaling to enable memory-to-memory composition and/or to capture a display output for Ethernet video encoding.

For more information, see *Display Subsystem (DSS)* section in *Peripherals* chapter in the device TRM.

7.4.5.8.1 DSI

The MIPI DSI v1.3.1 Controller (DSITX) implements the stream arbitration and low-level protocol layer functionalities required by MIPI DSI 1.3 standard. It supports up to 4 x 2.5 Gbps D-PHY data lanes in a single-link configuration and handles the byte lane mapping per use case (1, 2, 3, or 4-lanes). The accompaning DSI (Physical Layer) D-PHY module (DPHYTX) provides the video output interfacing by implementing a four-lane MIPI D-PHY transmitter.

For more information, see *Display Subsystem (DSS) and Display Peripherals* section in *Peripherals* chapter in the device TRM.

7.4.5.8.2 eDP

The VESA DP1.4/eDP1.4 Compliant Transmitter Host Controller (EDP) can output up to 4 video streams (through Multiple Stream Transport / MST) and one audio stream through the 4-lane accompaning SerDes module. It provides up to 25.92 Gbps of application bandwidth. An additional eDP (Physical Layer) auxiliary PHY (AUXPHY) module implements a doubly-terminated differential pair required for 1 Mbps data rates over a long (15m) cable.

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For more information, see *Display Subsystem (DSS) and Display Peripherals* section in *Peripherals* chapter in the device TRM.

7.4.5.9 VPFE

The Video Processing Front End (VPFE) is an input interface module that receives raw (unprocessed) image/video data or YUV digital video data from external imaging peripherals (such as image sensors, video decoders, etc) and performs DMA transfers to store the captured data in the system DDR memory.

For more information, see *Video Processing Front End (VPFE)* section in *Peripherals* chapter in the device TRM.

7.4.5.10 eCAP

The enhanced Capture (ECAP) module can be used for:

- Sample rate measurements of audio inputs
- Speed measurements of rotating machinery (for example, toothed sprockets sensed via Hall sensors)
- Elapsed time measurements between position sensor pulses
- Period and duty cycle measurements of pulse train signals
- Decoding current or voltage amplitude derived from duty cycle encoded current/voltage sensors.

For more information, see *Enhanced Capture (ECAP) Module* section in *Peripherals* chapter in the device TRM.

7.4.5.11 EPWM

An effective PWM peripheral must be able to generate complex pulse width waveforms with minimal CPU overhead or intervention. It needs to be highly programmable and very flexible while being easy to understand and use. The EPWM unit described here addresses these requirements by allocating all needed timing and control resources on a per PWM channel basis. Cross coupling or sharing of resources has been avoided; instead, the EPWM is built up from smaller single channel modules with separate resources and that can operate together as required to form a system. This modular approach results in an orthogonal architecture and provides a more transparent view of the peripheral structure, helping users to understand its operation quickly.

In the further description the letter x within a signal or module name is used to indicate a generic EPWM instance on a device. For example, output signals EPWMxA and EPWMxB refer to the output signals from the EPWM_x instance. Thus, EPWM1A and EPWM1B belong to EPWM1, EPWM2A and EPWM2B belong to EPWM2, and so forth.

Additionally, the EPWM integration allows this synchronization scheme to be extended to the capture peripheral modules (ECAP). The number of modules is device-dependent and based on target application needs. Modules can also operate stand-alone.

For more information, see *Enhanced Pulse Width Modulation (EPWM) Module* section in *Peripherals* chapter in the device TRM.

7.4.5.12 ELM

The Error Location Module (ELM) is used with the GPMC. Syndrome polynomials generated on-the-fly when reading a NAND flash page and stored in GPMC registers are passed to the ELM. A host processor can then correct the data block by flipping the bits to which the ELM error-location outputs point.

When reading from NAND flash memories, some level of error-correction is required. In the case of NAND modules with no internal correction capability, sometimes referred to as *bare NANDs*, the correction process is delegated to the memory controller. ELM can be also used to support parallel NOR flash or NAND flash.

For more information, see *Error Location Module (ELM)* section in *Peripherals* chapter in the device TRM.

7.4.5.13 ESM

The Error Signaling Module (ESM) aggregates safety-related events and/or errors from throughout the device into one location. It can signal both low and high priority interrupts to a processor to deal with a safety event and/or manipulate an I/O error pin to signal an external hardware that an error has occurred. Therefore an external controller is able to reset the device or keep the system in safe, known state.

For more information, see *Error Signaling Module (ESM)* section in *Peripherals* chapter in the device TRM.

7.4.5.14 eQEP

The Enhnanced Quadrature Encoder Pulse (EQEP) peripheral is used for direct interface with a linear or rotary incremental encoder to get position, direction and speed information from a rotating machine for use in high performance motion and position control system. The disk of an incremental encoder is patterned with a single track of slots patterns. These slots create an alternating pattern of dark and light lines. The disk count is defined as the number of dark/light line pairs that occur per revolution (lines per revolution). As a rule, a second track is added to generate a signal that occurs once per revolution (index signal: QEPI), which can be used to indicate an absolute position. Encoder manufacturers identify the index pulse using different terms such as index, marker, home position and zero reference.

For more information, see *Enhanced Quadrature Encoder Pulse (EQEP) Module* section in *Peripherals* chapter in the device TRM.

7.4.5.15 GPIO

The General-Purpose Input/Output (GPIO) peripheral provides dedicated general-purpose pins that can be configured as either inputs or outputs. When configured as an output, the user can write to an internal register to control the state driven on the output pin. When configured as an input, user can obtain the state of the input by reading the state of an internal register.

In addition, the GPIO peripheral can produce host CPU interrupts and DMA synchronization events in different interrupt/event generation modes.

For more information, see *General-Purpose Interface (GPIO)* section in *Peripherals* chapter in the device TRM.

7.4.5.16 GPMC

The General-Purpose Memory Controller is a unified memory controller dedicated for interfacing with external memory devices like:

- Asynchronous SRAM-like memories and application-specific integrated circuit (ASIC) devices
- Asynchronous, synchronous, and page mode (available only in non-multiplexed mode) burst NOR flash devices
- NAND flash
- Pseudo-SRAM devices

For more information, see *General-Purpose Memory Controller (GPMC)* section in *Peripherals* chapter in the device TRM.

7.4.5.17 Hyperbus

The Hyperbus module is a part of the device Flash Subsystem (FSS).

The Hyperbus module is low pin count memory interface that provides high read/write performance. The Hyperbus module connects to hyperbus memory (HyperFlash or HyperRAM) and uses simple hyperbus protocol for read and write transactions.

There is one Hyperbus™ module inside the device. The Hyperbus module includes one Hyperbus Memory Controller (HBMC).

For more information, see *Hyperbus Interface* section in *Peripherals* chapter in the device TRM.

7.4.5.18 I2C

The device contains ten multimaster Inter-Integrated Circuit (I2C) controllers each of which provides an interface between a local host (LH), such as an Arm or a Digital Signal Processor (DSP), and any I^2C-bus-compatible device that connects via the I^2C serial bus. External components attached to the I^2C bus can serially transmit and receive up to 8 bits of data to and from the LH device through the 2-wire I^2C interface.

Each multimaster I2C module can be configured to act like a slave or master I^2C-compatible device.

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The WKUP_I2C0, MCU_I2C0, I2C0, and I2C1 controllers have dedicated I^2C compliant open drain buffers, and support high speed mode (up to 3.4 Mbps in 1.8 V mode and up to 400 kbps in 3.3 V mode). The MCU_I2C1, I2C2, I2C3, I2C4, I2C5, and I2C6 controllers are multiplexed with standard LVCMOS I/O, connected to emulate open drain, and support fast mode (up to 400 kbps in 1.8 V/3.3 V mode). The I2C emulation is achieved by configuring the LVCMOS buffers to output Hi-Z instead of driving high when transmitting logic 1.

For more information, see *Inter-Integrated Circuit (I2C) Interface* section in *Peripherals* chapter in the device TRM.

7.4.5.19 I3C

The device contains three Improved Inter-Integrated Circuit (I3C) controllers each of which provides an interface between a local host (LH), such as an Arm, and any I3C-bus-compatible device that connects via the I3C serial bus.

For more information, see *Improved Inter-Integrated Circuit (I3C) Interface* section in *Peripherals* chapter in the device TRM.

7.4.5.20 MCAN

The Controller Area Network (CAN) is a serial communications protocol which efficiently supports distributed real-time control. CAN has high immunity to electrical interference. In a CAN network, many short messages are broadcast to the entire network, which provides for data consistency in every node of the system.

The MCAN module supports both classic CAN and CAN FD (CAN with Flexible Data-Rate) specifications. CAN FD feature allows high throughput and increased payload per data frame. The classic CAN and CAN FD devices can coexist on the same network without any conflict.

For more information, see *Modular Controller Area Network (MCAN)* section in *Peripherals* chapter in the device TRM.

7.4.5.21 MCASP

The MCASP functions as a general-purpose audio serial port are optimized to the requirements of various audio applications. The MCASP module can operate in both transmit and receive modes. The MCASP is useful for time-division multiplexed (TDM) stream, Inter-IC Sound (I2S) protocols reception and transmission as well as for an inter-component digital audio interface transmission (DIT). The MCASP has the flexibility to gluelessly connect to a Sony/Philips digital interface (S/PDIF) transmit physical layer component.

Although inter-component digital audio interface reception (DIR) mode (this is, S/PDIF stream receiving) is not natively supported by the MCASP module, a specific TDM mode implementation for the MCASP receivers allows an easy connection to external DIR components (for example, S/PDIF to I2S format converters).

For more information, see *Multichannel Audio Serial Port (MCASP)* section in *Peripherals* chapter in the device TRM.

7.4.5.22 MCRC Controller

VBUSM CRC controller is a module which is used to perform CRC (Cyclic Redundancy Check) to verify the integrity of a memory system. A signature representing the contents of the memory is obtained when the contents of the memory are read into MCRC Controller. The responsibility of MCRC controller is to calculate the signature for a set of data and then compare the calculated signature value against a predetermined good signature value. MCRC controller provides four channels to perform CRC calculation on multiple memories in parallel and can be used on any memory system. Channel 1 can also be put into data trace mode, where MCRC controller compresses each data being read through CPU read data bus.

For more information, see *MCRC Controller* section in *Interprocessor Communication* chapter in the device TRM.

7.4.5.23 MCSPI

The MCSPI module is a multichannel transmit/receive, master/slave synchronous serial bus.

There are total of eleven MCSPI modules in the device.

For more information, see *Multichannel Serial Peripheral Interface (MCSPI)* section in *Peripherals* chapter in the device TRM.

7.4.5.24 MMC/SD

The MMCSD Host Controller provides an interface to eMMC 5.1 (embedded MultiMedia Card), SD 4.10 (Secure Digital), and SDIO 4.0 (Secure Digital IO) devices. The MMCSD Host Controller deals with MMC/SD/SDIO protocol at transmission level, data packing, adding cyclic redundancy checks (CRCs), start/end bit insertion, and checking for syntactical correctness.

For more information, see *Multimedia Card/Secure Digital (MMC/SD) Interface* section in *Peripherals* chapter in the device TRM.

7.4.5.25 OSPI

The Octal Serial Peripheral Interface (OSPI) module is a kind of Serial Peripheral Interface (SPI) module which allows single, dual, quad or octal read and write access to external flash devices. This module has a memory mapped register interface, which provides a direct memory interface for accessing data from external flash devices, simplifying software requirements.

The OSPI module is used to transfer data, either in a memory mapped direct mode (for example a processor wishing to execute code directly from external flash memory), or in an indirect mode where the module is set-up to silently perform some requested operation, signalling its completion via interrupts or status registers. For indirect operations, data is transferred between system memory and external flash memory via an internal SRAM which is loaded for writes and unloaded for reads by a device master at low latency system speeds. Interrupts or status registers are used to identify the specific times at which this SRAM should be accessed using user programmable configuration registers.

For more information, see *Octal Serial Peripheral Interface (OSPI)* section in *Peripherals* chapter in the device TRM.

7.4.5.26 PCIE

The Peripheral Component Interconnect Express (PCIe) subsystem is built around a multi-lane dual-mode PCIe controller that provides low pin-count, high reliability, and high-speed data transfers at rates of up to 8.0 Gbps per lane for serial links on backplanes and printed wiring boards.

For more information, see *Peripheral Component Interconnect Express (PCIe) Subsystem* section in *Peripherals* chapter in the device TRM.

7.4.5.27 SerDes

SerDes'es goal is to convert device (SoC) parallel data into serialized data that can be output over a highspeed electrical interface. In the opposite direction, SerDes converts high-speed serial data into parallel data that can be processed by the device. To this end, the SerDes contains a variety of functional blocks to handle both the external analog interface as well as the internal digital logic.

For more information, see *Serializer/Deserializer (SerDes)* section in *Peripherals* chapter in the device TRM.

7.4.5.28 WWDT

The Windowed Watchdog Timer provides timer functionality for operating systems and for benchmarking code. The module incorporates several counters, which define the timebases needed for scheduling in the operating system. The module is implemented with an RTI module, but only WWDT is supported.

This module is specifically designed to fulfill the requirements for OSEK (“Offene Systeme und deren Schnittstellen für die Elektronik im Kraftfahrzeug”; “Open Systems and the Corresponding Interfaces for Automotive Electronics”) as well as OSEK/Time compliant operating systems.

For more information, see *Real Time Interrupt (RTI) Module* section in *Peripherals* chapter in the device TRM.

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7.4.5.29 Timers

All timers include specific functions to generate accurate tick interrupts to the operating system.

Each timer can be clocked from several different independent clocks. The selection of clock source is made from registers in the MCU_CTRL_MMR0/CTRL_MMR0.

In the MCU domain the device provides 10 timer pins to be used as MCU Timer Capture inputs or as MCU Timer PWM outputs. In order to provide maximum flexibility, these 10 pins may be used with any of MCU_TIMER0 through MCU_TIMER9 instances. System level muxes are used to control the capture source pin for each MCU_TIMER[9-0] and the MCU_TIMER[9-0] source for each MCU_TIMER_IO[1-0] PWM output.

In the MAIN domain the device provides 8 timer pins to be used as Timer Capture inputs or as Timer PWM outputs. For maximum flexibility, these 8 pins may be used with any of TIMER0 through TIMER19 instances. System level muxes are used to control the capture source pin for each TIMER[19-0] and the TIMER[19-0] source for each TIMER_IO[7-0] PWM output.

Each odd numbered timer instance from each of the domains may be optionally cascaded with the previous even numbered timer instance from the same domain to form up to a 64-bit timer. For example, TIMER1 may be cascaded to TIMER0, MCU_TIMER1 may be cascaded to MCU_TIMER0, etc.

When cascaded, TIMERi acts as a 32-bit prescaler to TIMERi+1, as well as MCU_TIMERn acts as a 32-bit prescaler to MCU_TIMERn+1. TIMERi / MCU_TIMERn must be configured to generate a PWM output edge at the desired rate to increment the TIMERi+1/ MCU_TIMERn+1 counter.

For more information, see *Timers* section in *Peripherals* chapter in the device TRM.

7.4.5.30 UART

The UART is a slave peripheral that utilizes the DMA for data transfer or interrupt polling via host CPU. There are twelve UART modules in the device. All UART modules support IrDA and CIR modes when 48 MHz function clock is used. Each UART can be used for configuration and data exchange with a number of external peripheral devices or interprocessor communication between devices.

For more information, see *Universal Synchronous/Asynchronous Receiver/Transmitter (UART)* section in *Peripherals* chapter in the device TRM.

7.4.5.31 USB

Similar to earlier versions of USB bus, USB 3.0 is a general-purpose cable bus, supporting data exchange between a host device and a wide range of simultaneously accessible peripherals.

The device supports two identical USB subsystems:

- USB3SS0 is SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with on-chip SS (USB3.0) PHY and HS/FS/LS (1) (USB2.0) PHY
- USB3SS1 is SuperSpeed (SS) USB 3.0 Dual-Role-Device (DRD) subsystem with on-chip SS (USB3.0) PHY and HS/FS/LS (USB2.0) PHY

For more information, see *Universal Serial Bus (USB) Subsystem* section in *Peripherals* chapter in the device TRM.

7.4.5.32 UFS

The Universal Flash Storage (UFS) interface is a standard-based serial interface engine.

There is one UFS module inside the device - UFS0. The UFS module includes one UFS 2.1 host controller (HC) with an integrated M-PHY.

The UFS module complies with the standards as listed in 表 7-1.

表 7-1. UFS Standards

DOCUMENT	VERSION	DESCRIPTION
JESD220-1A	v1.1	Universal Flash Storage (UFS) Unified Memory Extension

表 7-1. UFS Standards (続き)

DOCUMENT	VERSION	DESCRIPTION
JESD220-2	v1.0	Universal Flash Storage (UFS) Card Extension
JESD220C	v2.1, March 2016	Universal Flash Storage (UFS)
JESD223-1B	v1.1A	Universal Flash Storage Host Controller Interface (UFSHCI) Unified Memory Extension
JESD223C	v2.1, March 2016	Universal Flash Storage Host Controller Interface (UFSHCI)
JESD224	March 2013	Universal Flash Storage (UFS) Test
	November, 2001	Federal Information Processing Standards (FIPS) 197 Advanced Encryption Standard (AES)
	v3.1, 2014	MIPI® Alliance Specification for M-PHY
	v1.60, 2013	MIPI Alliance Specification for Unified Protocol (UniProSM)
	Revision 24, August 2010	Small Computer System Interface (SCSI) Block Commands - 3
	Revision 27, October 2010	SCSI Primary Commands - 4

For more information, see *Universal Flash Storage (UFS) Interface* section in *Peripherals* chapter in the device TRM.

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8 Applications and Implementation

注

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8.1 Power Supply Mapping

This Jacinto 7™ processor device can be operated in several different modes of operation depending upon the number of power resources, power supply groups (i.e. power rails) and control signals available:

- Full Active
- MCU Only low power mode
- DDR Retention (Suspend-to-RAM or S2R) low power mode
- MCU Island safety monitor
- Extended MCU safety monitor

Two power distribution networks (PDNs) that support these different operational modes are recommended and provide optional end product features. To name a few:

- Dual Voltage (1.8V & 3.3V) IO Interfaces
- Compliant UHS-I SD Card
- Compliant USB2.0
- High Security device type Efuse programming on-board for in-field updates

An Isolated PDN provides independent MCU & Main power resources & rails (see 表 8-2) to support power rail Freedom From Interference (FFI) as desired to reach end product system functional safety targets. An isolated PDN is needed to support MCU Only lower power mode or MCU Island safety monitoring. MCU ONLY can significantly reduce device power by disabling all Main processing while only keeping MCU processor resources active. A Combined PDN reduces total number of power resources & rails by grouping MCU & Main supplies into common power rails (see 表 8-1). This PDN can be used for Extended MCU safety processing but does not allow for MCU Island safety monitor or MCU Only low power modes. The DDR Retention low power mode can be supported with either an Isolated or Combined PDN scheme.

The TPS6594x & LP8764x Power Management ICs (PMICs) are key power components in the two recommended PDNs. Additional discrete power components may be added as desired to support optional system features. TI has optimized recommended PDNs using these PMICs for the following reasons:

- Full device performance entitlement as validated on TI Evalution boards
- Enable all system functional safety features and analysis captured in device safety manual
- Support power rail load steps, supply voltage accuracies and maximum load currents with margins
- Meet device primary & low power mode supply sequencing requirements (refer to セクション 6.9.2, *Power Supply Sequencing*)
- Provide Adaptive Voltage Scaling (AVS) Class 0 device requirements with TI validated software

For full PDN design and operational details, refer to either

1. "Dual TPS6594-Q1 PMIC User Guide for Jacinto 7™ DRA829 and TDA4VM Automotived PDN-0B (SLVUC32)" for legacy designs aligned to original EVM PDN-0A wishing to minimize SCH & PCB updates
2. "Dual TPS6594-Q1 PMIC User Guide for Jacinto 7™ DRA829 and TDA4VM Automotived PDN-0C (SLVUC99)" for all new designs

表 8-1. Combined MCU and Main Voltage Domain Power Rail Mapping

TYPES	VOLTAGE [V]	DOMAIN NAMES	DOMAIN GROUPS	POWER RAILS	#
Digital IO	3.3	(VDDSHV0_MCU, VDDSHV1_MCU, VDDSHV2_MCU, VDDSHV0,VDDSHV1, VDDSHV2, VDDSHV3, VDDSHV4, VDDSHV5[3], VDDSHV6)[1], VDDA_3P3_USB[4]	VDDSHVn_MCU,VDDSHVn, VDDA_3P3_USB[4]	VDD_IO_3V3	1
Digital IO	1.8	(VDDSHV0_MCU, VDDSHV1_MCU, VDDSHV2_MCU, VDDSHV0, VDDSHV1, VDDSHV2, VDDSHV, VDDSHV4, VDDSHV5[3], VDDSHV6)[2]	VDDSHVn_MCU[2] VDDSHVn[3 2]	VDD_IO_1V8	2
Digital IO	1.8	VDDS_MMC0[6]	VDDS_MMC0[6]	VDDS_MMC0_1V8[6]	3
Analog PHY	1.8	(VDDA_1P8_CSIRX, VDDA_1P8_USB, VDDA_1P8_UFS, VDDA_1P8_DP, VDDA_1P8_DSITX, VDDA_1P8_MLB, VDDA_1P8_SERDES)	VDDA_1P8_<phy>[5]	VDD_PHY_1V8[5]	4
Analog Clk, Meas	1.8	VDDA_MCU_PLLGRP0, VDDA_MCU_TEMP, VDDA_ADC_MCU, VDDA_POR_WKUP, VDDA_WKUP VDDS_OSC1, VDDA_PLLGRP6:0, VDDA_TEMP3:0	VDDA_1P8_<clk/meas>	VDA_LN_1V8	5
Analog, low voltage	0.80	VDDA_0P8_PLL_MLB, VDDA_0P8_PLL_DDR, VDDA_0P8_DLL_MMC0	VDDA_0P8_DPLL	VDA_DPLL_0V8	6
Digital, AVS low voltage	0.77 – 0.84	VDD_CPU	VDD_CPU	VDD_CPU_AVS	7
Digital, low voltage	0.80	VDD_MCU[7], VDD_CORE, (VDDA_0P8_SERDES, VDDA_0P8_SERDES_C, VDDA_0P8_DP, VDDA_0P8_DP_C, VDDA_0P8_DSITX, VDDA_0P8_DSITX_C, VDDA_0P8_CSIRX, VDDA_0P8_UFS, VDDA_0P8_USB) [8]	VDD_MCU VDD_CORE VDDA_0P8_<phy>[8]	VDD_PROC_0V8	8
Digital, low voltage	0.85	VDDAR_MCU, VDDAR_CORE, VDDAR_CPU	VDDAR	VDD_RAM_0V85	9
Digital, low voltage	1.1	VDDS_DDR_BIAS, VDDS_DDR, VDDS_DDR_C	VDDS_DDR	VDD_DDR_1V1	10

1. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces
2. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 1.8V to support 1.8V digital interfaces
3. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3/1.8V) power rail is required for compliant, high-speed SD card operations. If SD card is not needed or standard data rates with fixed

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3.3V operation is acceptable, then domain can be grouped with digital IO 3.3V power rail. If a SD card is capable of operating with fixed 1.8V, then domain can be grouped with digital IO 1.8V power rail.

4. VDDA_3P3_USB is 3.3V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3V digital IO power rail either directly or through a supply filter.
5. VDDA_1P8_<phy> are 1.8V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8V power rail either directly or through an in-line supply filter is allowed.
6. VDD_MMC0 is 1.8V digital supply supporting MMC0 signaling for eMMC interface. If MMC0 or eMMC0 interface is not needed, then domain can be grouped with digital IO 1.8V power rail. However, if MMC0 interface is needed, then VDD_MMC0 must not start ramp-up until VDD_CORE has reached Vopr min.
7. VDD_MCU is a digital voltage supply with a wide operational voltage range and power sequencing flexibility, enabling it to be grouped and ramped-up with either 0.8V VDD_CORE or 0.85V RAM array domains (VDDAR_xxx).
8. VDDA_1P8_<clk/pll/ana> are 1.8V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance.

表 8-2. Isolated MCU and Main Voltage Domain Power Rail Mapping

TYPES	VOLTAGE [V]	DOMAIN NAMES	DOMAIN GROUPS	POWER RAILS	#
Digital IO	3.3	(VDDSHV0_MCU, VDDSHV1_MCU, VDDSHV2_MCU)[1]	VDDSHVn_MCU	VDD_MCUIO_3V3	1
Digital IO	3.3	(VDDSHV0, VDDSHV1, VDDSHV2, VDDSHV3, VDDSHV4, VDDSHV5[3], VDDSHV6)[1], VDDA_3P3_USB[4]	VDDSHVn, VDDA_3P3_USB[4]	VDD_IO_3V3	2
Digital IO	1.8	(VDDSHV0_MCU, VDDSHV1_MCU, VDDSHV2_MCU)[2]	VDDSHVn_MCU[2]	VDD_MCUIO_1V8	3
Digital IO	1.8	(VDDSHV0, VDDSHV1, VDDSHV2, VDDSHV3, VDDSHV4, VDDSHV5[3], VDDSHV6)[2]	VDDSHVn2 [3]	VDD_IO_1V8	4
Digital IO	1.8	VDDS_MMC0[6]	VDDS_MMC0[6]	VDDS_MMC0_1V8[6]	5
Analog Clk, Meas	1.8	VDDA_MCU_PLLGRP0, VDDA_MCU_TEMP, VDDA_ADC_MCU, VDDA_POR_WKUP, VDDA_WKUP	VDDA_MCU1P8_<clk/meas>	VDA_MCU_1V8	6
Analog Clk, Meas	1.8	VDDS_OSC1, VDDA_PLLGRP6:0, VDDA_TEMP3:0	VDDA_1P8_<clk/meas>	VDA_DPLL_1V8	7
Analog PHY	1.8	(VDDA_1P8_CSIRX, VDDA_1P8_USB, VDDA_1P8_UFS, VDDA_1P8_DP, VDDA_1P8_DSITX, VDDA_1P8_MLB, VDDA_1P8_SERDES)[5]	VDDA_1P8_<phy>[5]	VDA_PHY_1V8[5]	8
Analog, low voltage	0.80	VDDA_0P8_PLL_MLB, VDDA_0P8_PLL_DDR, VDDA_0P8_DLL_MMC0	VDDA_0P8_DPLL	VDA_DPLL_0V8	9
Digital, low voltage	0.80	VDD_MCU, VDDAR_MCU	VDD_MCU, VDDAR_MCU	VDD_MCU_0V85	10

表 8-2. Isolated MCU and Main Voltage Domain Power Rail Mapping (続き)

TYPES	VOLTAGE [V]	DOMAIN NAMES	DOMAIN GROUPS	POWER RAILS	#
Digital, AVS low voltage	0.77 – 0.84	vdd_cpu	VDD_CPU	VDD_CPU_AVS	11
Digital, low voltage	0.80	VDD_CORE, (VDDA_0P8_SERDES, VDDA_0P8_SERDES_C, VDDA_0P8_DP, VDDA_0P8_DP_C, VDDA_0P8_DSITX, VDDA_0P8_DSITX_C, VDDA_0P8_CSIRX, VDDA_0P8_UFS, VDDA_0P8_USB)[8]	VDD_CORE, VDDA_0P8_<phy>[8]	VDD_CORE_0V8	12
Digital, low voltage	0.85	VDDAR_CORE, VDDAR_CPU	VDDAR	VDD_RAM_0V85	13
Digital, low voltage	1.1	VDDS_DDR_BIAS,VDDS_DDR, VDDS_DDR_C	VDDS_DDR	VDD_DDR_1V1	14

1. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 3.3V to support 3.3V digital interfaces
2. Any MCU or Main dual voltage IO supplies (VDDSHVn_MCU or VDDSHVn) being supplied by 1.8V to support 1.8V digital interfaces
3. VDDSHV5 supports MMC1 signaling for SD memory cards. A dual voltage (3.3/1.8V) power rail is required for compliant, high-speed SD card operations. If SD card is not needed or standard data rates with fixed 3.3V operation is acceptable, then domain can be grouped with digital IO 3.3V power rail. If a SD card is capable of operating with fixed 1.8V, then domain can be grouped with digital IO 1.8V power rail.
4. VDDA_3P3_USB is 3.3V analog domain used for USB 2.0 differential interface signaling. A low noise, analog supply is recommended to provide best signal integrity for USB data eye mask compliance. If USB interface is not needed or data bit errors can be tolerated, then domain can be grouped with 3.3V digital IO power rail either directly or through a supply filter.
5. VDDA_1P8_<phy> are 1.8V analog domains supporting multiple serial PHY interfaces. A low noise, analog supply is recommended to provide best signal integrity, interface performance and spec compliance. If any of these interfaces are not needed, data bit errors or non-compliant operation can be tolerated, then domains can be grouped with digital IO 1.8V power rail either directly or through an in-line supply filter is allowed.
6. VDD_MMC0 is 1.8V digital supply supporting MMC0 signaling for eMMC interface. If MMC0 or eMMC0 interface is not needed, then domain can be grouped with digital IO 1.8V power rail. However, if MMC0 interface is needed, then VDD_MMC0 must not start ramp-up until VDD_CORE has reached $V_{OPR\ MIN}$.
7. VDD_MCU is a digital voltage supply with a wide operational voltage range and power sequencing flexibility, enabling it to be grouped and ramped-up with either 0.8V VDD_CORE or 0.85V RAM array domains (VDDAR_xxx).
8. VDDA_1P8_<clk/pll/ana> are 1.8V analog domains supporting clock oscillator, PLL and analog circuitry needing a low noise supply for optimal performance.

8.2 Device Connection and Layout Fundamentals

8.2.1 Power Supply Decoupling and Bulk Capacitors

8.2.1.1 Power Distribution Network Implementation Guidance

The *Jacinto 7 Processor Power Distribution Networks: Implementation and Analysis (SPRACN5)* provides guidance for successful implementation of the power distribution network. This includes PCB stackup guidance as well as guidance for optimizing the selection and placement of the decoupling capacitors. TI supports *only* designs that follow the board design guidelines contained in the application report.

8.2.2 External Oscillator

For more information, see セクション 6.9.4.1, Input and output Clocks/Oscillators.

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8.2.3 JTAG and EMU

Texas Instruments supports a variety of eXtended Development System (XDS) JTAG controllers with various debug capabilities beyond only JTAG support. A summary of this information is available in the XDS Target Connection Guide.

For more recommendations on EMU routing, see Emulation and Trace Headers Technical Reference Manual

8.2.4 Reset

The device incorporates four external reset pins (MCU_PORz, MCU_RESETz, PORz, and RESET_REQz) and four reset status pins (MCU_PORz_OUT, MCU_RESETSTATz, PORz_OUT, and RESETSTATz). These pins can be driven by an external power good circuitry or Power Management IC (PMIC). MCU_PORz and Main PORz pins should be held active low during the entire power-up phase, and until all power supplies as well as the HFOSC0 clock are stable.

All MCU domain resets act as master resets to the whole device, whereas Main domain resets only reset Main domain (MCU domain is reset isolated from all Main domain resets).

8.2.5 Unused Pins

For more information about Unused Pins, see *Connections for Unused Pins*

8.2.6 Hardware Design Guide for Jacinto™ 7 Devices

The Hardware Design Guide for Jacinto™ 7 Devices document describes hardware system design considerations for the Jacinto™ 7 family of processors.This design guide is intended to be used as an aid during the development of application hardware.

8.3 Peripheral- and Interface-Specific Design Information

8.3.1 LPDDR4 Board Design and Layout Guidelines

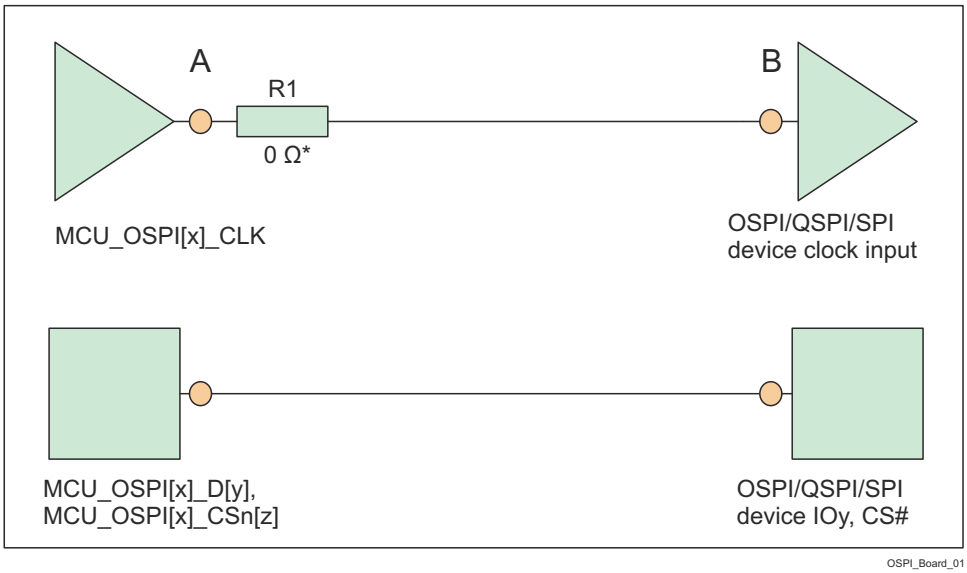
The goal of the Jacinto 7 LPDDR4 Board Design and Layout Guidelines is to make the LPDDR4 system implementation straightforward for all designers. Requirements have been distilled down to a set of layout and routing rules that allow designers to successfully implement a robust design for the topologies that TI supports. TI only supports board designs using LPDDR4 memories that follow the guidelines in this document.

8.3.2 OSPI and QSPI Board Design and Layout Guidelines

The following section details the routing guidelines that must be observed when routing the OSPI and QSPI interfaces.

8.3.2.1 No Loopback and Internal Pad Loopback

- The MCU_OSPI[x]_CLK output signal must be connected to the CLK pin of the flash device
- The signal propagation delay from the MCU_OSPI[x]_CLK signal to the flash device must be < 450 ps (~7cm as stripline or ~8cm as microstrip)
- 50 Ω PCB routing is recommended along with series terminations, as shown in 図 8-1
- Propagation delays and matching:
  - A to B < 450 ps
  - Matching skew: < 60 ps



* 0 Ω resistor (R1), located as close as possible to the MCU_OSPI[x]_CLK pin, is placeholder for fine tuning, if needed.

図 8-1. OSPI Interface High Level Schematic

8.3.2.2 External Board Loopback

- The MCU_OSPI[x]_CLK output signal must be connected to the CLK pin of the flash device
- The MCU_OSPI[x]_LBCLKO output signal must be looped back into the MCU_OSPI[x]_DQS input
- The signal propagation delay from the MCU_OSPI[x]_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to half of the signal propagation delay from the MCU_OPSI[x]_LBCLKO pin to the MCU_OSPI[x]_DQS pin ((C to D)/2). See the note below.
- The signal propagation delay from the MCU_OSPI[x]_CLK pin to the flash device CLK input pin (A to B) must be approximately equal to the signal propagation delay of the control and data signals between the flash device and the SoC device (E to F, or F to E)
- 50 Ω PCB routing is recommended along with series terminations, as shown in 図 8-2
- Propagation delays and matching:

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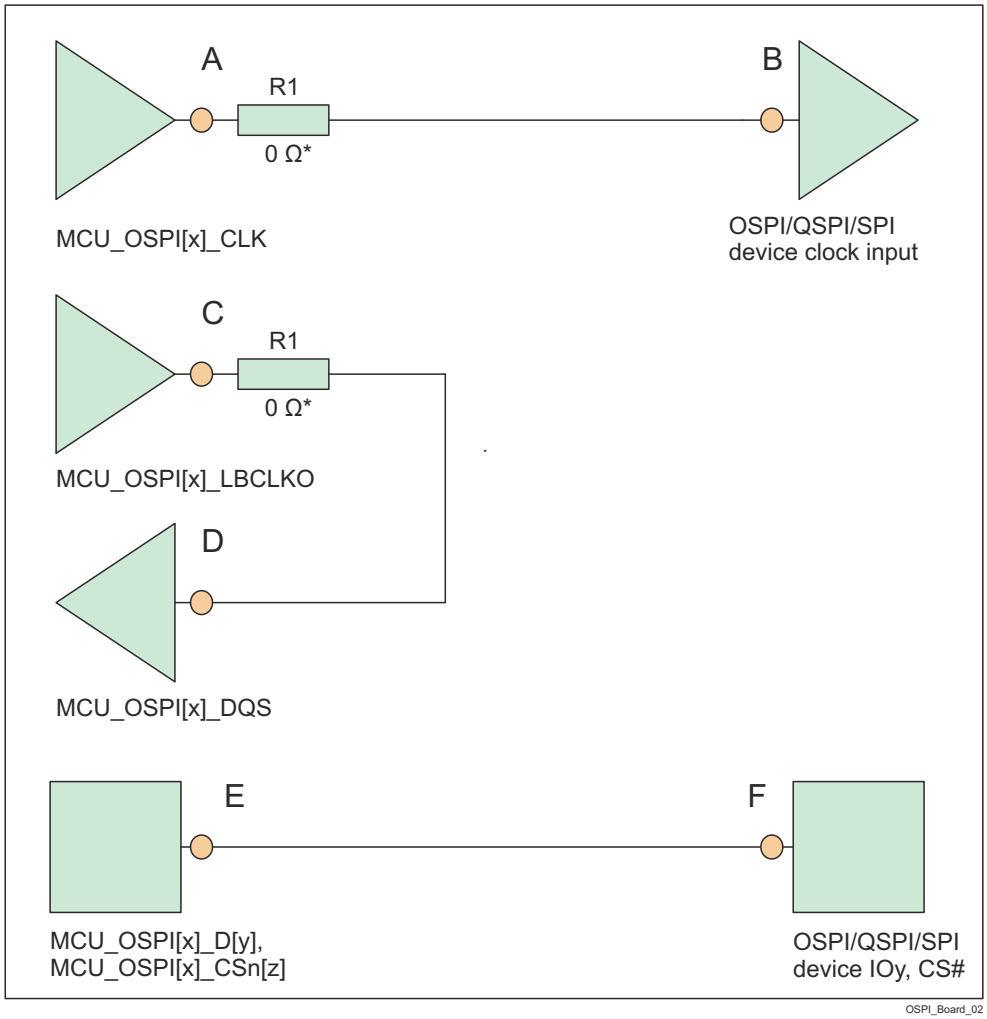
– A to B = E to F = (C to D) / 2
– Matching skew: < 60 ps

注

The OSPI Board Loopback Hold time requirement (described in セクション 6.9.5.21, *OSPI*) is larger than the Hold time provided by a typical flash device. Therefore, the length of MCU_OPSI[x]_LBCLKO pin to the MCU_OSPI[x]_DQS pin (C to D) can be shortened to compensate.



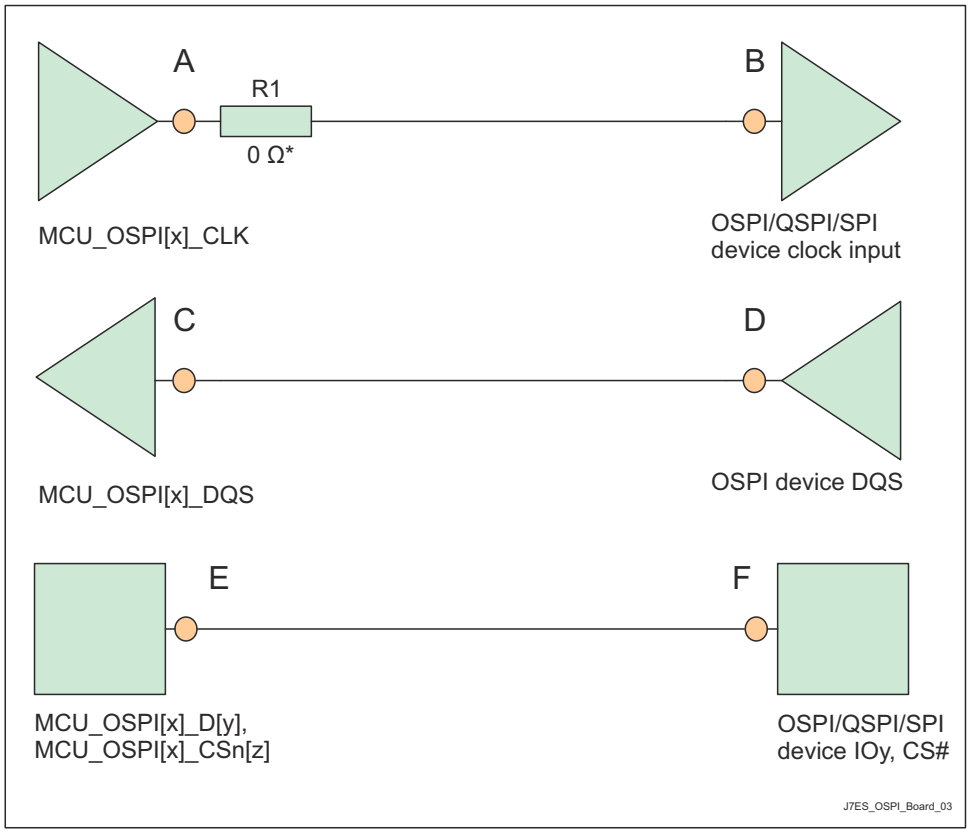
* 0 Ω resistor (R1), located as close as possible to the MCU_OSPI[x]_CLK and MCU_OSPI[x]_LBCLKO pins, is a placeholder for fine tuning, if needed.

図 8-2. OSPI Interface High Level Schematic

8.3.2.3 DQS (only available in Octal Flash devices)

- The MCU_OSPI[x]_CLK output signal must be connected to the CLK pin of the flash device
- The DQS pin of the flash devices must be connected to MCU_OSPI[x]_DQS signal
- The signal propagation delay from the MCU_OSPI[x]_CLK pin to the flash device CLK input pin (A to B) should be approximately equal to the signal propagation delay from the MCU_OSPI[x]_DQS pin to the DQS output pin (C to D)
- 50 Ω PCB routing is recommended along with series terminations, as shown in 図 8-3
- Propagation delays and matching:

– A to B = C to D
– Matching skew: < 60 ps



* 0 Ω resistor (R1), located as close as possible to the MCU_OSPI[x]_CLK pin, is a placeholder for fine tuning, if needed.

図 8-3. OSPI Interface High Level Schematic

8.3.3 SERDES REFCLK Design Guidelines

The following section details the routing guidelines that must be observed when terminating the SERDES REFCLK and is applicable only when SERDES REFCLK is configured to input mode.

1. 50 Ω to GND is recommended on each leg.
2. Internal AC coupling is always enabled, so external biasing is not needed.

8.3.4 USB VBUS Design Guidelines

The USB 3.1 specification allows the VBUS voltage to be as high as 5.5 V for normal operation, and as high as 20 V when the Power Delivery addendum is supported. Some applications require a max voltage to be 30 V.

The device requires the VBUS signal voltage be scaled down using an external resistor divider (as shown in the 図 8-4), which limits the voltage applied to the actual device pin (USB0_VBUS, USB1_VBUS). The tolerance of these external resistors should be equal to or less than 1%, and the leakage current of zener diode at 5 V should be less than 100 nA.

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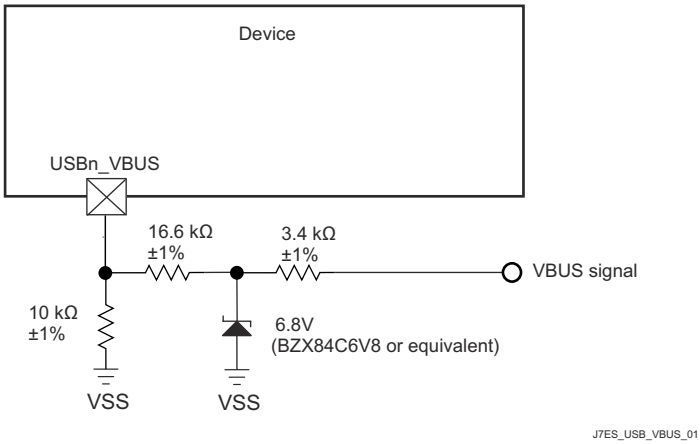

A. USBn_VBUS, where n = 0 or 1.

図 8-4. USB VBUS Detect Voltage Divider / Clamp Circuit

The USB0_VBUS and USB1_VBUS pins can be considered to be fail-safe because the external circuit in 図 8-4 limits the input current to the actual device pin in a case where VBUS is applied while the device is powered off.

8.3.5 System Power Supply Monitor Design Guidelines

The VMON_ER_VSYS pin provides a way to monitor a system power supply. This system power supply is typically a single pre-regulated power source for the entire system. This supply is monitored by comparing the output of an external voltage divider circuit sourced by this supply with an internal voltage reference, with a power fail event being triggered when the voltage applied to VMON_ER_VSYS drops below the internal reference voltage. The actual system power supply voltage trip point is determined by the system designer when selecting component values used to implement the external resistor voltage divider circuit. When designing the resistor divider circuit it is important to understand various factors which contribute to variability in the system power supply monitor trip point. The first thing to consider is the initial accuracy of the VMON_ER_VSYS input threshold which has a nominal value of 0.45 V, with a variation of ±3%. Precision 1% resistors with similar thermal coefficient are recommended for implementing the resistor voltage divider. This minimizes variability contributed by resistor value tolerances. Input leakage current associated with VMON_ER_VSYS must also be considered since any current flowing into the pin creates a loading error on the voltage divider output. The VMON_ER_VSYS input leakage current may be in the range of 10 nA to 2.5 µA when applying 0.45 V.

注

The resistor voltage divider shall be designed such that its output voltage never exceeds themaximum value defined in セクション 6.4, *Recommended Operating Conditions* during normal operating conditions.

図 8-5 presents an example, where the system power supply is nominally 5 V and the maximum trigger threshold is 5 V - 10%, or 4.5 V.

For this example, it is important to understand which variables effect the maximum trigger threshold when selecting resistor values. It is obvious a device which has a VMON_ER_VSYS input threshold of 0.45 V + 3% needs to be considered when trying to design a voltage divider that doesn’t trip until the system supply drops 10%. The effect of resistor tolerance and input leakage also needs to be considered, but how these contributions effect the maximum trigger point may not be obvious. When selecting component values which produce a maximum trigger voltage, the system designer must consider a condition where the value of R1 is 1% low and the value of R2 is 1% high combined with a condition where input leakage current for the VMON_ER_VSYS pin is 2.5 µA. When implementing a resistor divider where R1 = 4.81 KΩ and R2 = 40.2 KΩ, the result is a maximum trigger threshold of 4.523 V.

Once component values have been selected to satisfy the maximum trigger voltage as described above, the system designer can determine the minimum trigger voltage by calculating the applied voltage that produces an output voltage of 0.45 V - 3% when the value of R1 is 1% high and the value of R2 is 1% low, and the input leakage current is 10 nA, or zero. Using an input leakage of zero with the resistor values given above, the result is a minimum trigger threshold of 4.008 V.

This example demonstrates a system power supply voltage trip point that ranges from 4.008 V to 4.523 V. Approximately 250 mV of this range is introduced by VMON_ER_VSYS input threshold accuracy of ±3%, approximately 150 mV of this range is introduced by resistor tolerance of ±1%, and approximately 100 mV of this range is introduced by loading error when VMON_ER_VSYS input leakage current is 2.5 µA.

The resistor values selected in this example produces approximately 100 µA of bias current through the resistor divider when the system supply is 4.5 V. The 100 mV of loading error mentioned above could be reduced to about 10 mV by increasing the bias current through the resistor divider to approximately 1 mA. So resistor divider bias current vs loading error is something the system designer needs to consider when selecting component values.

The system designer should also consider implementing a noise filter on the voltage divider output since VMON_ER_VSYS has minimum hysteresis and a high-bandwidth response to transients. This could be done by installing a capacitor across R1 as shown in 図 8-5. However, the system designer must determine the response time of this filter based on system supply noise and expected response to transient events.

図 8-5 presents an example, when the system power supply voltage is nominally 5 V and the desired trigger threshold is -10% or 4.5 V.

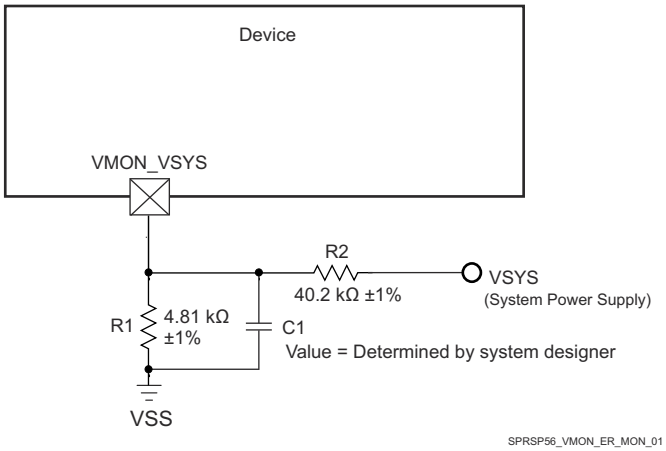

図 8-5. System Supply Monitor Voltage Divider Circuit

8.3.6 High Speed Differential Signal Routing Guidance

The High Speed Interface Layout Guidelines provides guidance for successful routing of the high speed differential signals. This includes PCB stackup and materials guidance as well as routing skew, length and spacing limits. TI supports *only* designs that follow the board design guidelines contained in the application report.

8.3.7 Thermal Solution Guidance

The Thermal Design Guide for DSP and ARM Application Processors provides guidance for successful implementation of a thermal solution for system designs containing this device. This document provides background information on common terms and methods related to thermal solutions. TI only supports designs that follow system design guidelines contained in the application report.

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all microprocessors (MPUs) and support tools. Each device has one of three prefixes: X, P, or null (no prefix) (for example, TDA4VM). Texas Instruments recommends two of three possible prefix designators for its support tools: TMDX and TMDS. These prefixes represent evolutionary stages of product development from engineering prototypes (TMDX) through fully qualified production devices and tools (TMDS).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

Support tool development evolutionary flow:

TMDX Development-support product that has not yet completed Texas Instruments internal qualification testing.

TMDS Fully-qualified development-support product.

X and P devices and TMDX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

Production devices and TMDS development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

For orderable part numbers of TDA4VM devices in the ALF package type, see the Package Option Addendum of this document, the TI website (ti.com), or contact your TI sales representative.

9.1.1 Standard Package Symbolization

注

Some devices may have a cosmetic circular marking visible on the top of the device package which results from the production test process. In addition, some devices may also show a color variation in the package substrate which results from the substrate manufacturer. These differences are cosmetic only with no reliability impact.

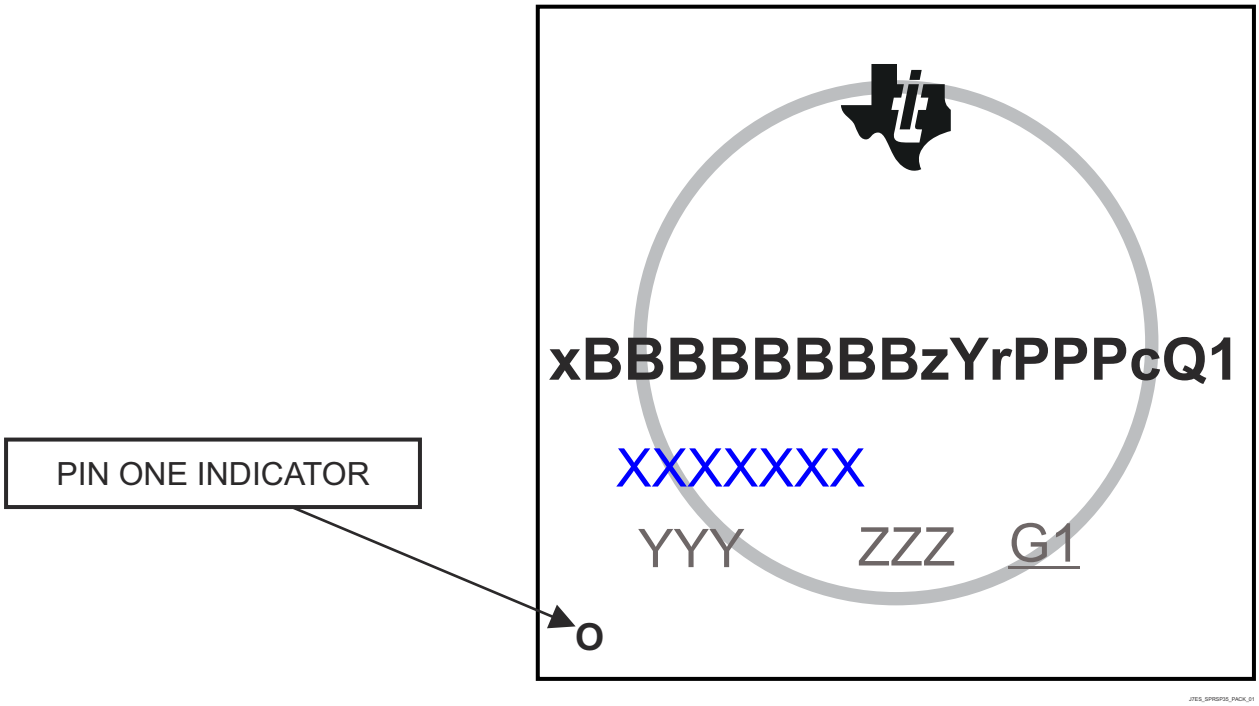

図 9-1. Printed Device Reference

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9.1.2 Device Naming Convention

表 9-1. Nomenclature Description

FIELD PARAMETER	FIELD DESCRIPTION	VALUES		DESCRIPTION
		MARKING	ORDERABLE	
x	Device evolution stage[1]	X		Prototype
		P		Preproduction (production test flow, no reliability data)
		BLANK		Production
BBBBBBB[2]	Base production part number	J721E[2]		Preproduction superset device
		TDA4VM88		See 表 4-1, *Device Comparison*
		TDA4VM67		See 表 4-1, *Device Comparison*
		TDA4VM21		See 表 4-1, *Device Comparison*
z	Device Speed	T		See 表 6-1, *Speed Grade Maximum Frequency*.
		L		
		E		
		OTHER		Alternate speed grade
Y	Device type	G		General purpose (Prototype and Production)
		C		General purpose, R5F Lockstep capable
		0		High Security[3] capable
		5		High Security[3] capable, R5F Lockstep capable
		R		High Security Prime[3] capable, R5F Lockstep capable
		D		High Security[3] capable, R5F Lockstep capable, Customer Dev Keys. Only available on preproduction J721E devices.
		P		High Security Prime[3] capable, R5F Lockstep capable, Customer Dev Keys. Only available on preproduction J721E devices.
r	Device revision	A or BLANK		SR 1.0
		B		SR 1.1
		C		SR 2.0
PPP	Package designator	ALF		ALF FCBGA-N827 (24 mm x 24 mm) Package
c	Carrier designator	N/A	BLANK	Tray
		N/A	R	Tape and Reel
Q1	Automotive Designator	BLANK		Not automotive qualified. Supports T_J = –40°C to 105°C
		Q1		Meet AEC-Q100 qualification requirements, with exceptions as specified in this document (data sheet). Supports T_J = –40°C to 125°C
XXXXXXX	Lot Trace Code	As Marked	N/A	Lot Trace Code (LTC)
YYY	Production Code	As Marked	N/A	Production Code, for TI use only
ZZZ	Production Code	As Marked	N/A	Production Code, for TI use only
O	Pin One	As Marked	N/A	Pin one designator
G1	ECAT	As Marked	N/A	ECAT—Green package designator

(1) To designate the stages in the product development cycle, TI assigns prefixes to the part numbers. These prefixes represent evolutionary stages of product development from engineering prototypes through fully qualified production devices. Prototype devices are shipped against the following disclaimer:
"This product is still in development and is intended for internal evaluation purposes."
Notwithstanding any provision to the contrary, TI makes no warranty expressed, implied, or statutory, including any implied warranty of merchantability of fitness for a specific purpose, of this device.

(2) J721E is the base part number for the superset device. Software should constrain the features used to match the intended production device.

(3) For HS device support, TI recommends the 0, 5, or D device types. The R and P (HS "prime") device types are not recommended for most applications, as they require extra steps in the manufacturing process and have a higher cost.

注

BLANK in the symbol or part number is collapsed so there are no gaps between characters.

9.2 Tools and Software

The following products support development for TDA4VM platforms:

Development Tools

Code Composer Studio™ Integrated Development Environment Code Composer Studio (CCS) Integrated Development Environment (IDE) is a development environment that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers.

Pin mux tool The Pin MUX Utility is a software tool which provides a Graphical User Interface for configuring pin multiplexing settings, resolving conflicts and specifying I/O cell characteristics for TI MPUs. Results are output as C header/code files that can be imported into software development kits (SDKs) or used to configure customer's custom software. Version 4 of the Pin Mux utility adds the capability of automatically selecting a mux configuration that satisfies the entered requirements.

For a complete listing of development-support tools for the processor platform, visit the Texas Instruments website at ti.com. For information on pricing and availability, contact the nearest TI field sales office or authorized distributor.

9.3 Documentation Support

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The following documents describe the TDA4VM devices.

Technical Reference Manual

J721E DRA829/TDA4VM/AM752x Processors Silicon Revisions 2.0, 1.1, and 1.0 Technical Reference Manual Details the integration, the environment, the functional description, and the programming models for each peripheral and subsystem in the TDA4VM family of devices.

Errata

J721E DRA829/TDA4VM/AM752x Processors Silicon Revision 1.0 Silicon Errata Describes the known exceptions to the functional specifications for the device.

9.4 サポート・リソース

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9.7 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Revision History

Changes from August 28, 2021 to April 22, 2024 (from Revision J (August 2021) to Revision K (April 2024)) **Page**

- グローバル:ドキュメントのタイトルを更新 1
- グローバル:文書全体にわたってシリコン リビジョン 2.0 (SR2.0) デバイス固有の情報を追加 1
- グローバル:「改訂履歴」セクションをドキュメントの末尾に移動 1
- グローバル:すべての OLDI/LVDS コンテンツを削除、このデバイス スイートに該当なし 1
- グローバル:「消費電力の概略」セクションを削除 (セクション 6.5「動作性能ポイント」の後) 1
- (特長):「最高 3733MT/s の速度をサポート」の箇条書き項目を「3733MT/s」から「4266MT/s」に更新 / 変更 1
- (特長):「イーサネット スイッチを内蔵」の箇条書き項目と副項目を更新 / 変更 1
- (特長):EMIF モジュールの下の「インライン ECC 付き ... 32 ビット データ バス」の箇条書き副項目を更新 / 変更 1
- (概要):導入の文を更新 3
- (パッケージ情報):「製品情報」表を「パッケージ情報」表に更新 / 変更し、表の内容を新しいフォーマットに更新 3
- (デバイスの比較):SDK ソフトウェア ビルド シートの注を追加 4
- (Device Comparison): Updated/Changed the MSMC capacity for TDA4VM**67** and TDA4VM**21** devices to "8MB". Now all devices: TDA4VM88, TDA4VM67, and TDA4VM21 are "8MB (On-Chip SRAM with ECC)" 6
- (Device Comparison): Added SDK software build sheet Note 6
- (Pin Attributes): Added the secondary pin multiplexing functions for the DSI and controlled by CTRLMMR regs 11
- (Pin Attributes): Added the secondary pin multiplexing functions for the MCU_ADC and controlled by CTRLMMR regs 11
- (Pin Attributes): Added "The MUXMODE field is not used to select …" footnote for the WKUP_GPIO0_[68:83] signals in the *Pin Attributes* table 11
- (Pin Attributes): Added reset states to the BALL RESET STATE column for mmc0_* pins in the *Pin Attributes* table 11
- (WKUP Domain GPIO0 Signal Descriptions): Added missing WKUP_GPIO0_[68:83] signals 84
- (Power Supply Signal Description): Added "±10%" to the "*This pin must always be … capacitor to VSS*" footnote 131

- (Connections for Unused Pins): Added the "VMON_ER_VSYS" (M26) and "VMON_IR_VEXT" (V19) signals to the "Each of these balls must be connected to VSS .." CONNECTIONS REQUIREMENT.....150
- (Connections for Unused Pins): Updated/Changed "All VMON and power balls must be …" Note deleting "VMON and"..... 150
- (Pin Connectivity Requirements): Updated/Changed the section title (*was "Connections for Unused Pins"*) 150
- (Connectivity Requirements (ALF Package)): Updated/Changed the table title (*was "Unused Balls Specific Connection Requirements"*).....150
- (Pin Connectivity Requirements): Added "as a boot source" to the Note specifying MMC1_SDCD and MMC2_SDCD should be pulled down to work properly..... 150
- (Absolute Maximum Ratings): Moved "VMON_IR_VEXT" and "VMON_ER_VSYS"signals ***from*** "Steady State Max. Voltage at all other IO pins" ***to*** "Steady State Max. Voltage at all fail-safe IO pins"..... 153
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- (Absolute Maximum Ratings): Updated/Changed "JESD78D (Class II)" to " JESD78**E** (Class II)" in the "For current pulse injection: .." footnote..... 153
- (Abs Max Ratings): Updated/Changed the UNIT specified for the Latch-Up Performance MAX parameter from "mV" to "V".....153
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- (I2C, Open-Drain, Fail-Safe (I2C OD FS) Electrical Characteristics): Updated/Changed the V_{OL}, Output low-level voltage under the **3.3-V MODE** MAX value from "0.4 × VDDSHV" to "0.4" V.....161
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- (I2C OD FS Electrical Characteristics): Added both the MIN and MAX input slew rate value and added associated footnotes to describe the SR_I parameter for 3.3-V MODE..... 161
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11 Mechanical, Packaging, and Orderable Information

11.1 Packaging Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TDA4VM88TGBALFR	Last Time Buy	Production	FCBGA (ALF) | 827	250 | LARGE T&R	-	Call TI	Level-3-250C-168 HR	-40 to 105	TDA4VM88TGBALF 942
TDA4VM88TGBALFRQ1	Last Time Buy	Production	FCBGA (ALF) | 827	250 | LARGE T&R	-	Call TI	Level-3-250C-168 HR	-40 to 125	TDA4VM88TGBALFQ1 942
TDA4VM88TGCALFR	Active	Production	FCBGA (ALF) | 827	250 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 105	TDA4VM88TGCALF 942
TDA4VM88TGCALFR.B	Active	Production	FCBGA (ALF) | 827	250 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 105	TDA4VM88TGCALF 942
TDA4VM88TGCALFRQ1	Active	Production	FCBGA (ALF) | 827	250 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	TDA4VM88TGCALFQ1 942
TDA4VM88TGCALFRQ1.B	Active	Production	FCBGA (ALF) | 827	250 | LARGE T&R	Yes	Call TI	Level-3-250C-168 HR	-40 to 125	TDA4VM88TGCALFQ1 942

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TDA4VM, TDA4VM-Q1 :

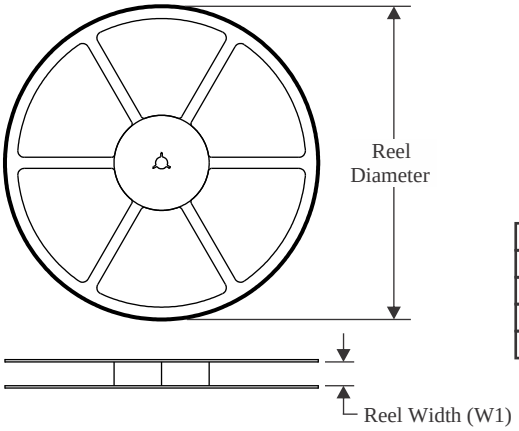
- Catalog : TDA4VM
- Automotive : TDA4VM-Q1

NOTE: Qualified Version Definitions:

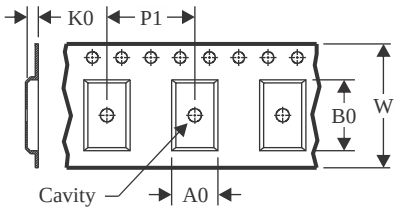
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

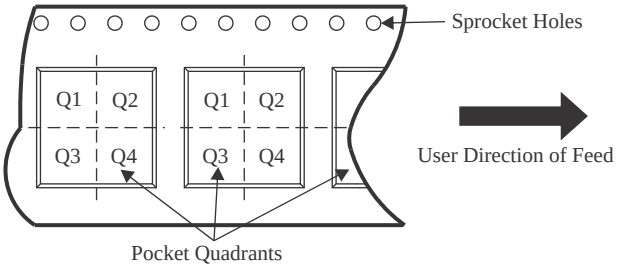


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

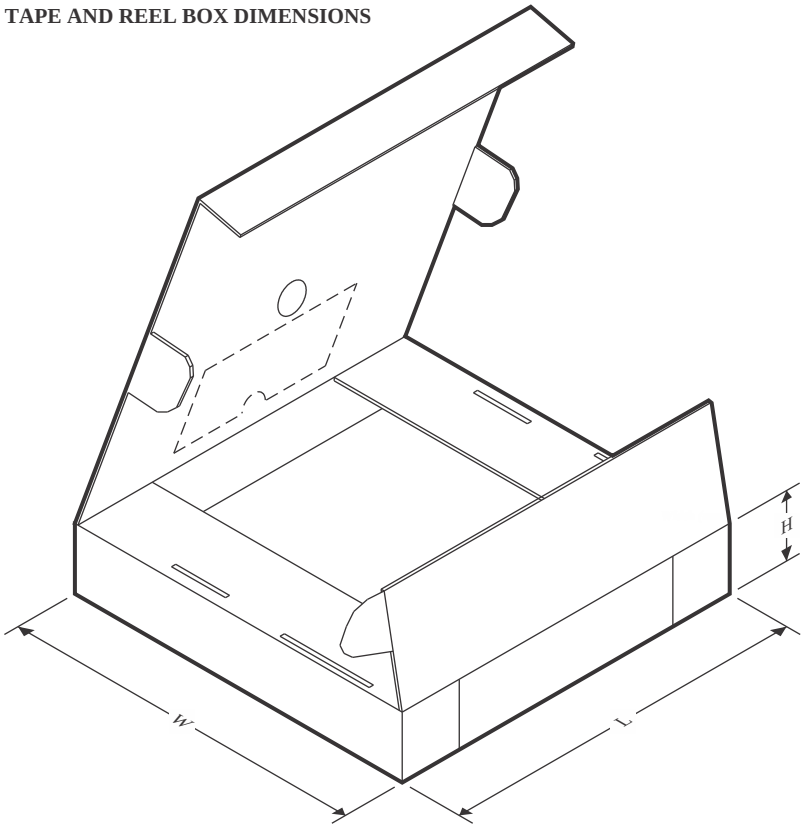
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

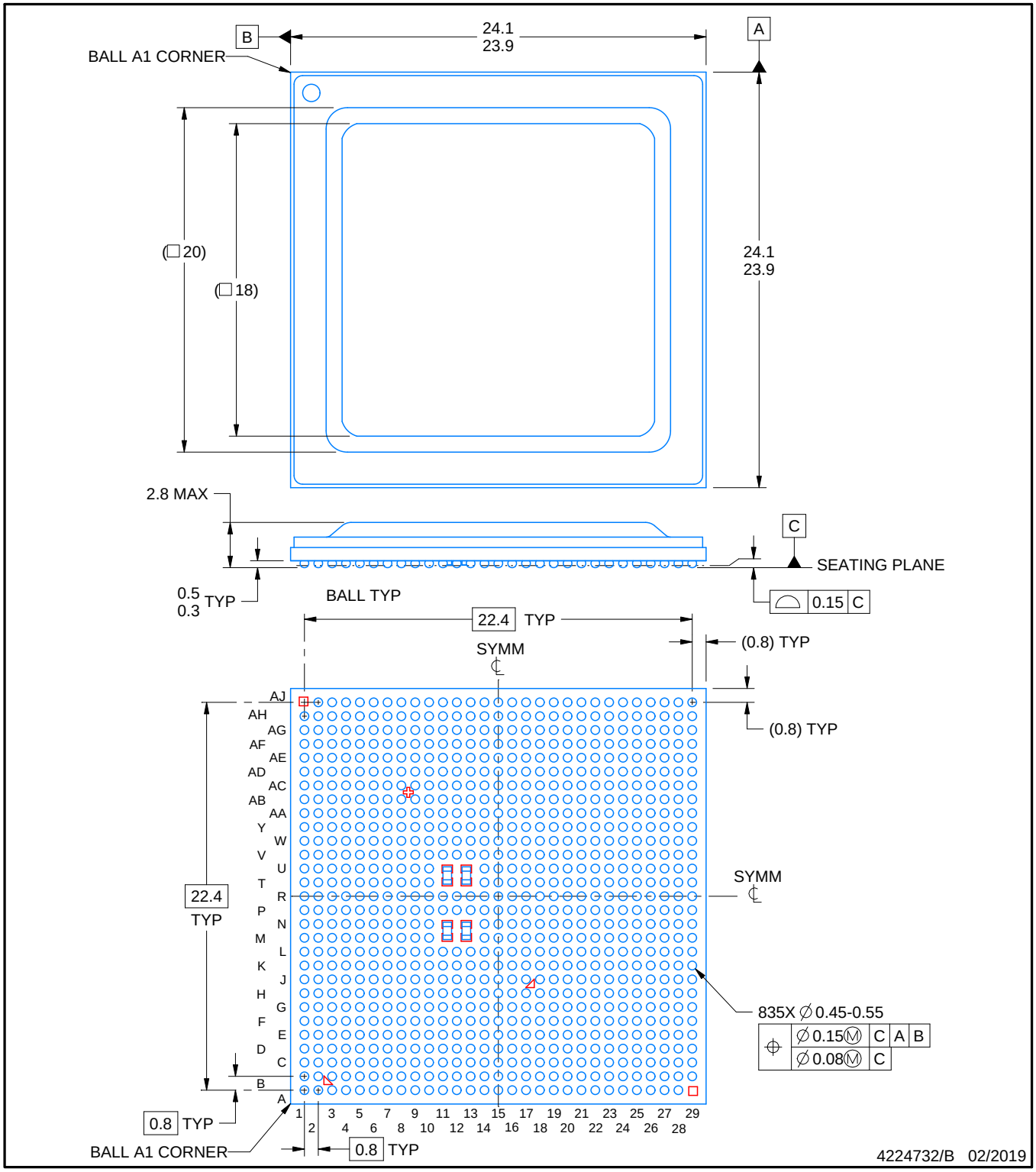
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TDA4VM88TGBALFR	FCBGA	ALF	827	250	330.0	44.4	24.5	24.5	4.5	32.0	44.0	Q1
TDA4VM88TGBALFRQ1	FCBGA	ALF	827	250	330.0	44.4	24.5	24.5	4.5	32.0	44.0	Q1
TDA4VM88TGCALFR	FCBGA	ALF	827	250	330.0	44.4	24.5	24.5	4.5	32.0	44.0	Q1
TDA4VM88TGCALFRQ1	FCBGA	ALF	827	250	330.0	44.4	24.5	24.5	4.5	32.0	44.0	Q1

TAPE AND REEL BOX DIMENSIONS



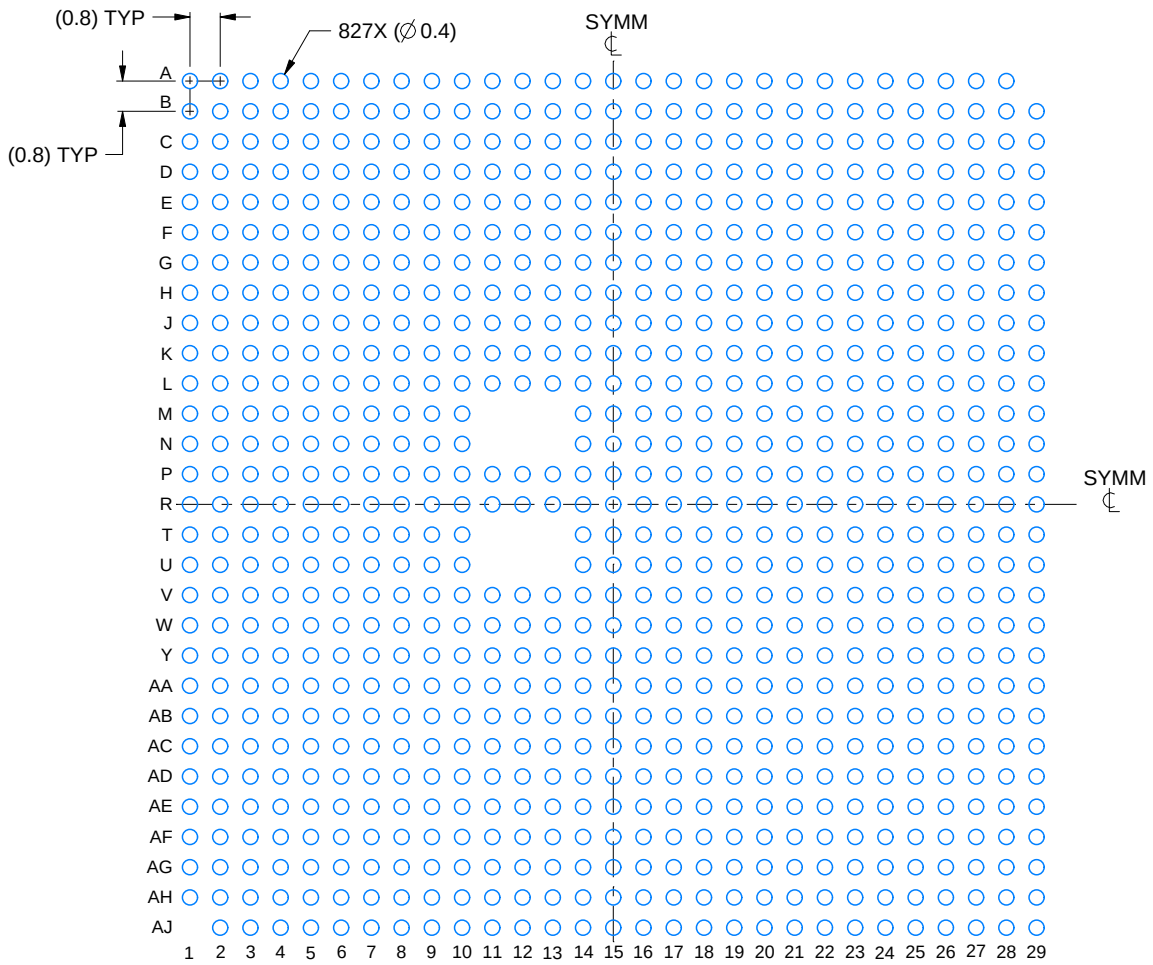
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TDA4VM88TGBALFR	FCBGA	ALF	827	250	336.6	336.6	53.2
TDA4VM88TGBALFRQ1	FCBGA	ALF	827	250	336.6	336.6	53.2
TDA4VM88TGCALFR	FCBGA	ALF	827	250	336.6	336.6	53.2
TDA4VM88TGCALFRQ1	FCBGA	ALF	827	250	336.6	336.6	53.2

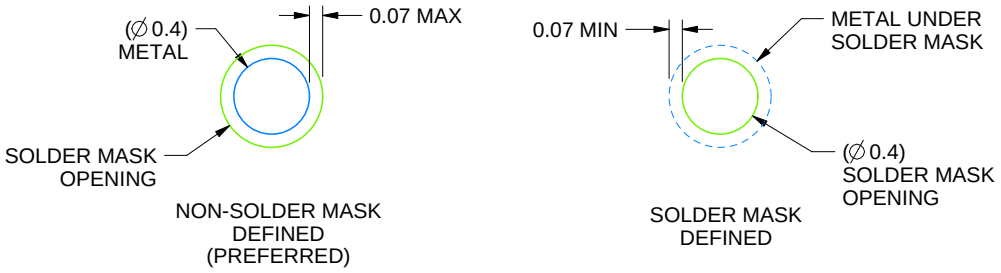


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pb-Free die bump and Pb-Free solder ball.



LAND PATTERN EXAMPLE
SCALE:5X

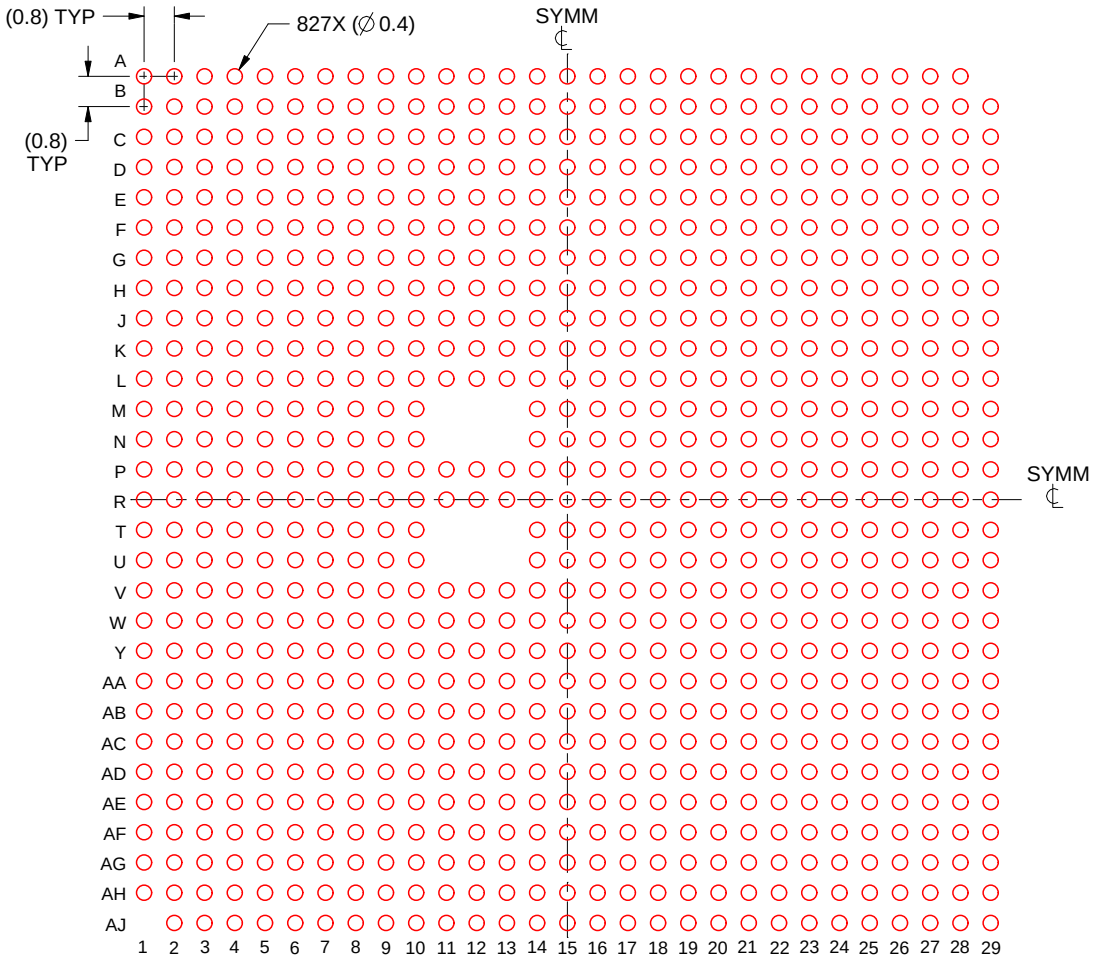


SOLDER MASK DETAILS
NOT TO SCALE

4224732/B 02/2019

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:5X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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