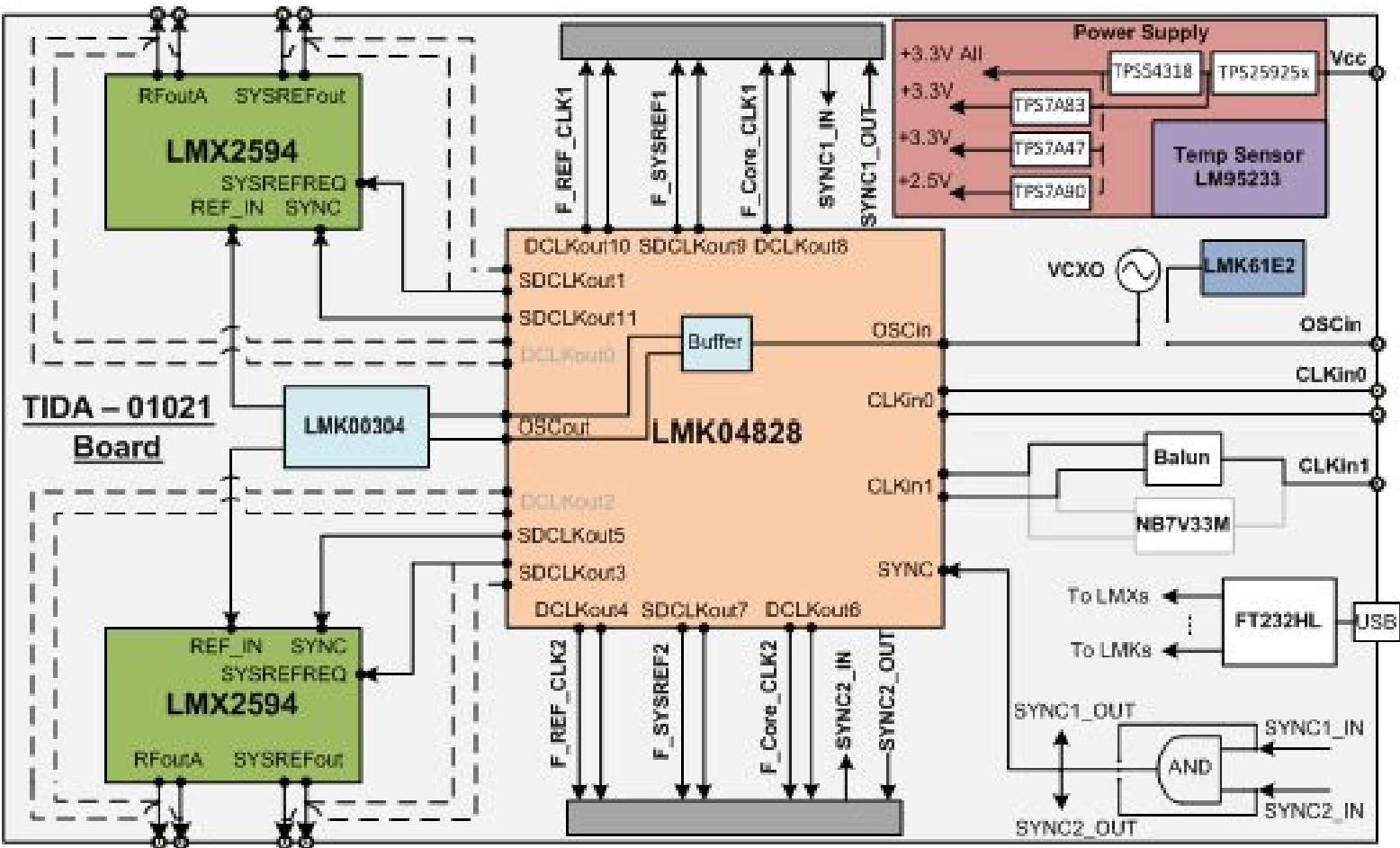
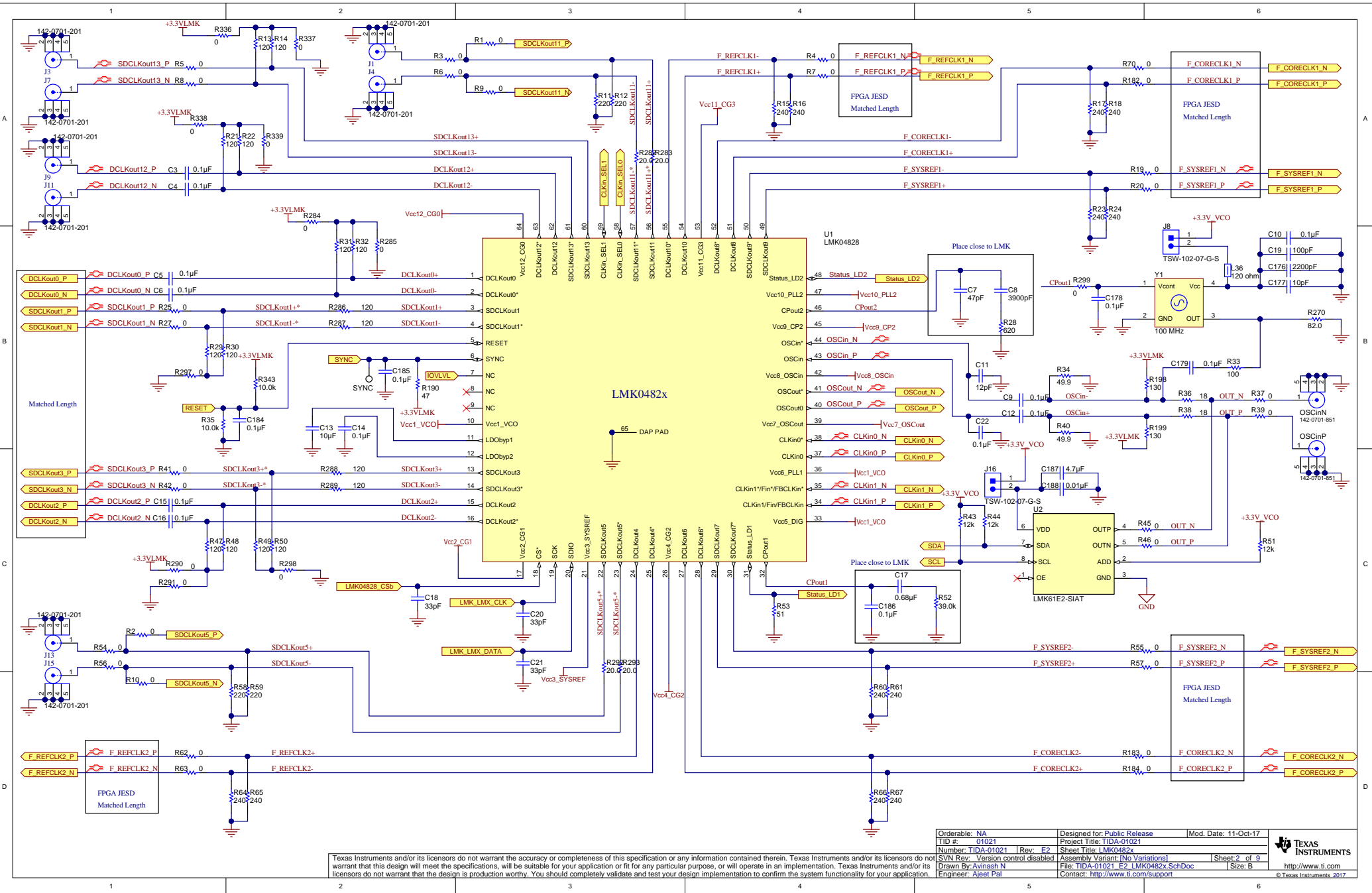


Revision History				
Rev	ECN #	Approved Date	Approved by	Notes
N/A	N/A	N/A	N/A	N/A



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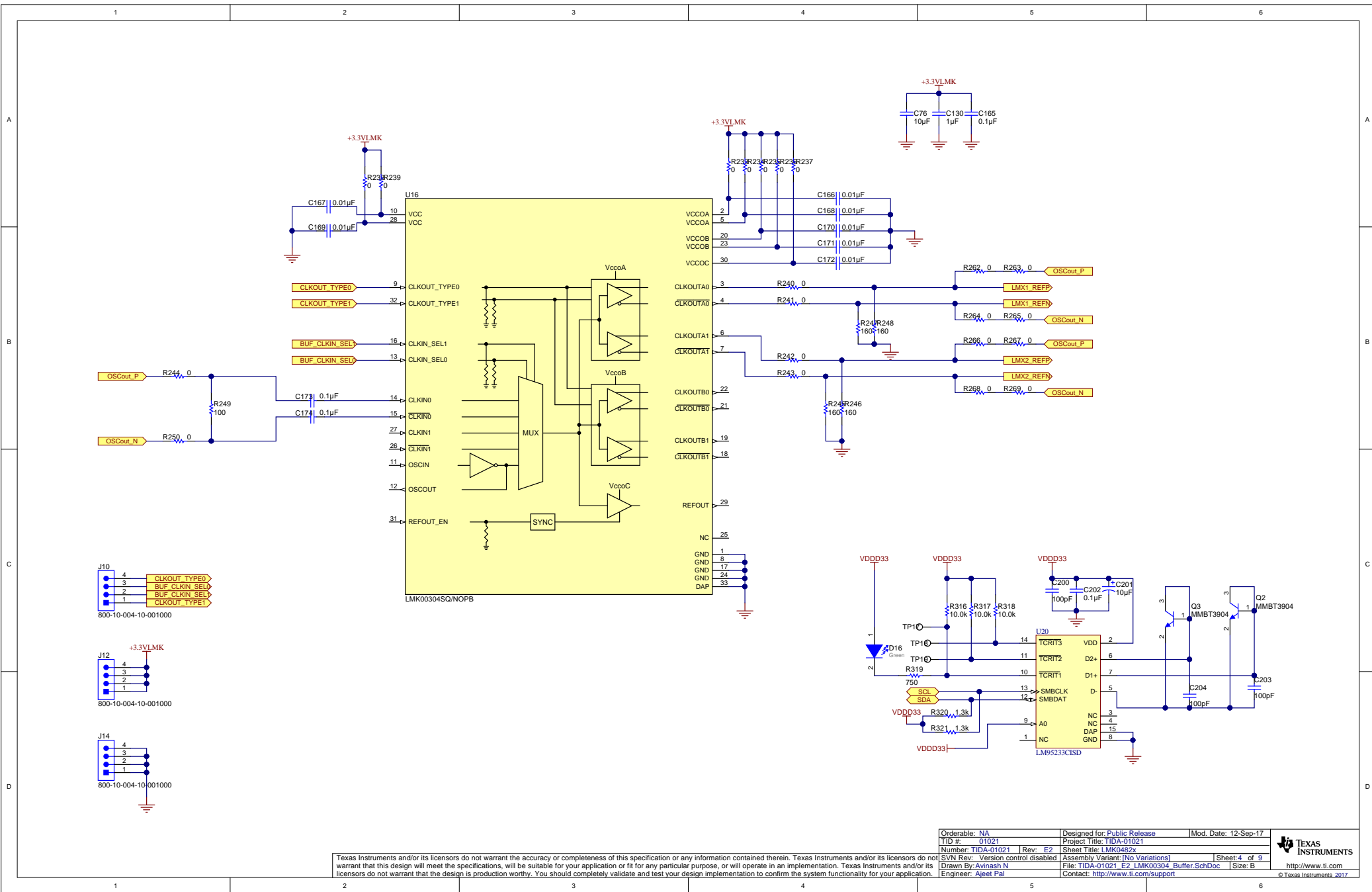
Orderable: NA	Designed for Public Release	Mod. Date: 06-Oct-17
TID #: 01021	Project Title: TIDA-01021	
Number: TIDA-01021 Rev: E2	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 1 of 9
Drawn By:	File: TIDA-01021_E2_CoverSheet.SchDoc	Size: B
Engineer: Ajeet Pal	Contact: http://www.ti.com/support	

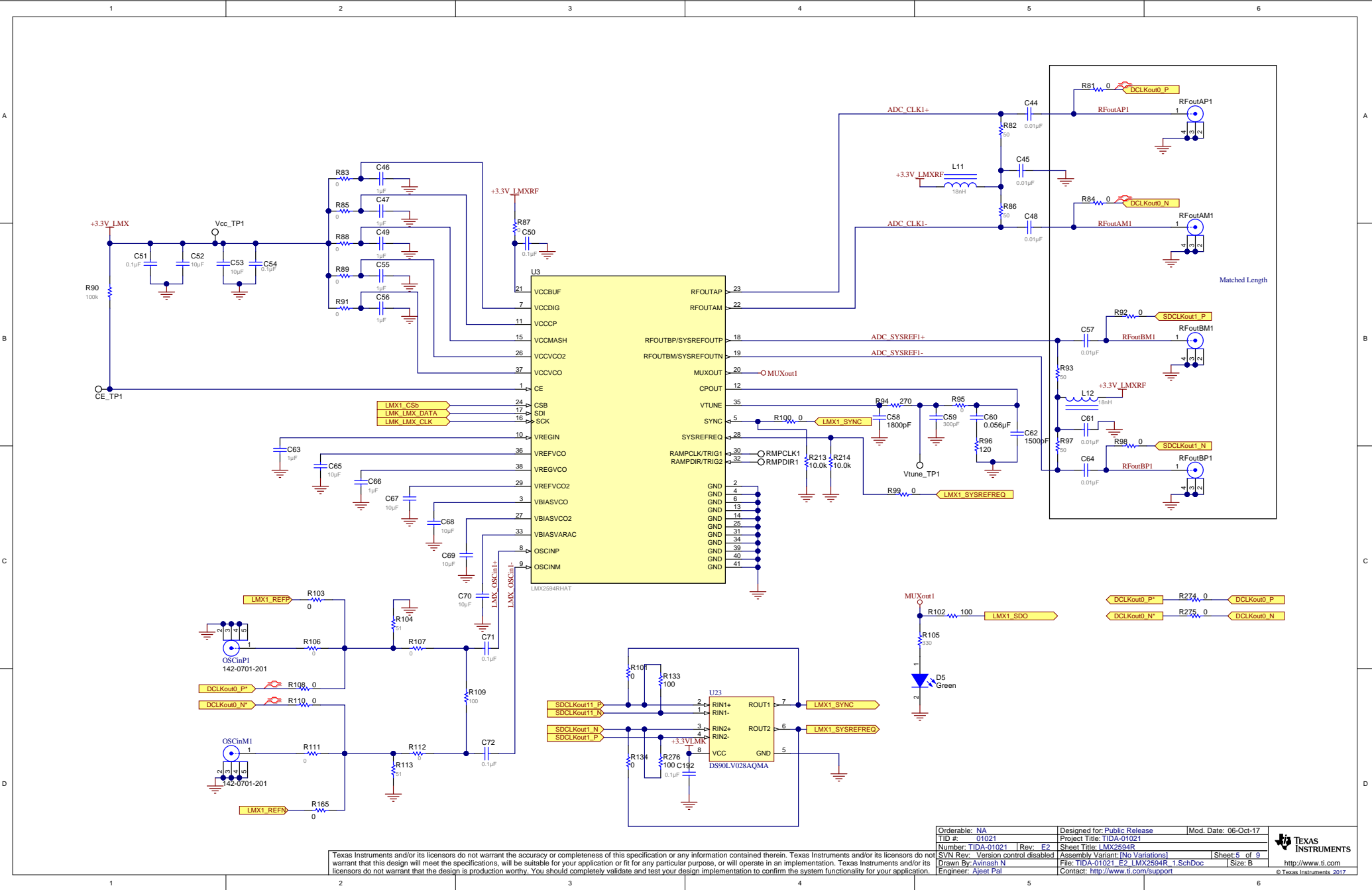


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Orderable: NA	Designed for Public Release	Mod. Date: 11-Oct-17
TID #: 01021	Project Title: TIDA-01021	Sheet Title: LMK0482x
Number: TIDA-01021 Rev: E2	Assembly Variant: [No Variations]	Sheet: 2 of 9
SVN Rev. Version control disabled	File: TIDA-01021_E2_LMK0482x_SchDoc	Size: B
Drawn By: Avinash N	Contact: http://www.ti.com/support	
Engineer: Ajeet Pal		





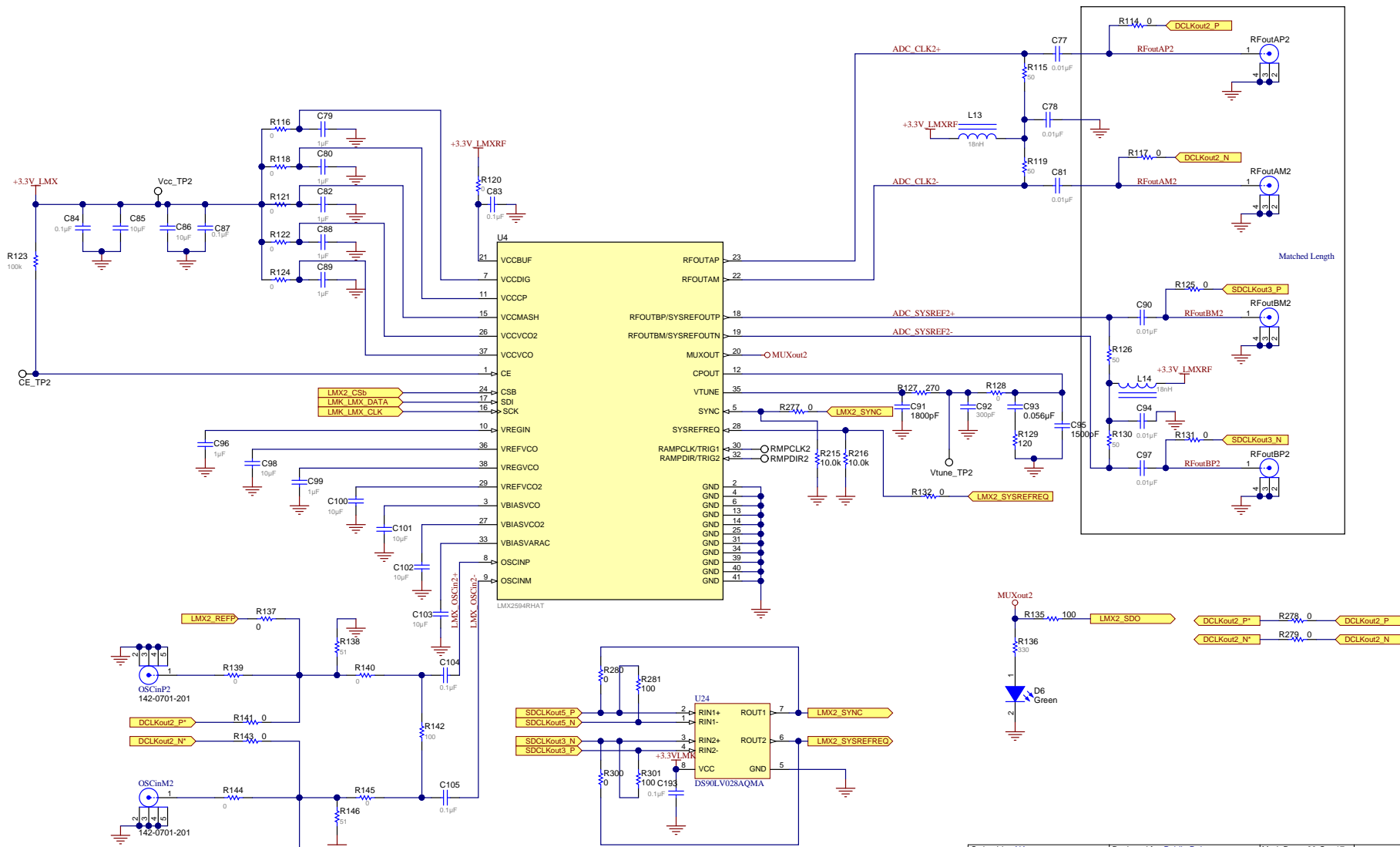


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Orderable: NA	Designed for Public Release	Mod. Date: 06-Oct-17
TID #: 01021	Project Title: TIDA-01021	
Number: TIDA-01021 Rev: E2	Sheet Title: LMX2594R	
SVN Rev. Version control disabled	Assembly Variant: [No Variations]	Sheet: 5 of 9
Drawn By: Avinash N	File: TIDA-01021_E2_LMX2594R_1_SchDoc	Size: B
Engineer: Ajeet Pal	Contact: http://www.ti.com/support	



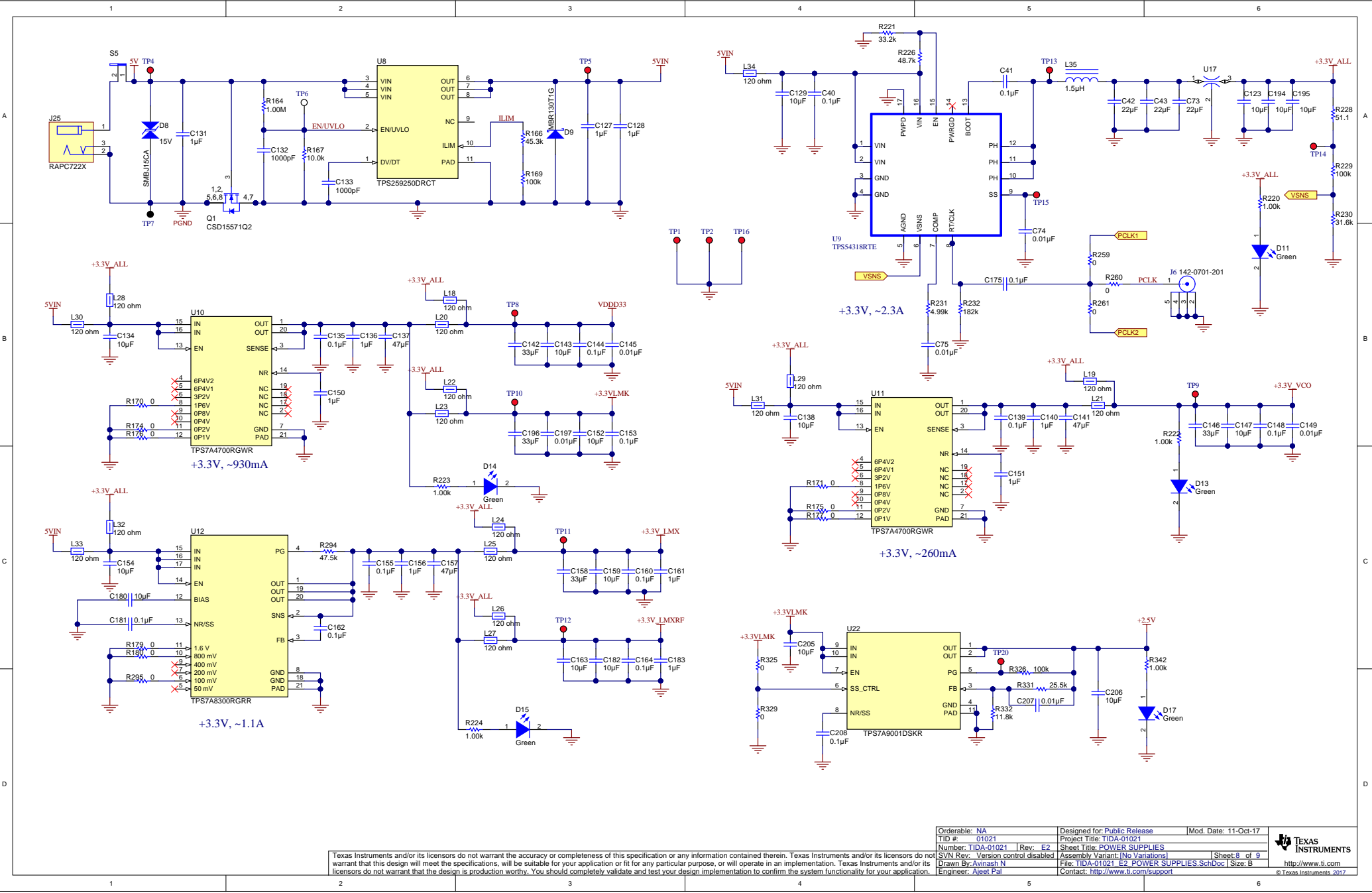
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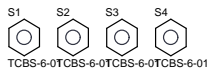


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Orderable: NA	Designed for Public Release	Mod. Date: 06-Oct-17
TID #: 01021	Project Title: TIDA-01021	
Number: TIDA-01021 Rev: E2	Sheet Title: LMX2594R	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 6 of 9
Drawn By: Avinash N	File: TIDA-01021_E2_LMX2594R_2_SchDoc	Size: B
Engineer: Ajeet Pal	Contact: http://www.ti.com/support	© Texas Instruments 2017







PCB Number: TIDA-01021
PCB Rev: E2

PCB
LOGO

Pb-Free Symbol

PCB
LOGO

FCC disclaimer

PCB
LOGO

Logo1

You should delete the nylon screws/standoffs and/or the bump-ons as needed for your design (or substitute other parts from Hardware.IntLib). Bump-ons are cheaper, but provide less clearance.

Deleting anything else from this page may result in your EVM submission being rejected (until you add them back).

Update the Label Text in the Label Table as needed for each Assembly Variant.

You should delete this note too.

Variant/Label Table

Variant	Label Text
001	ChangeMe!
002	ChangeMe!

LBL1

PCB Label

Size: 0.65" x 0.20"

ZZ1

Label Assembly Note

This Assembly Note is for PCB labels only

ZZ2

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4

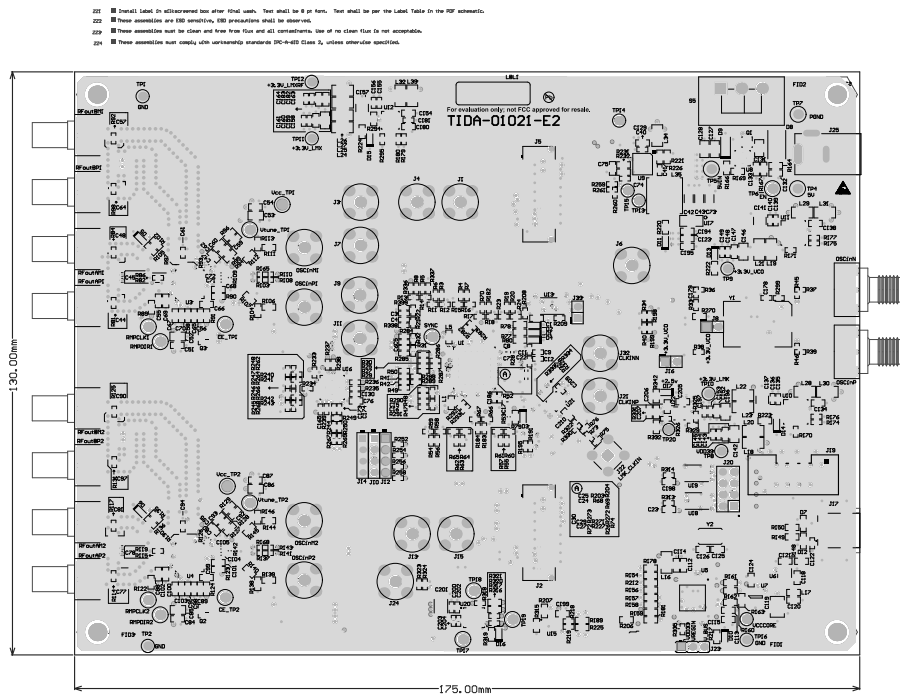
Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

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Orderable: NA	Designed for: Public Release	Mod. Date: 05-Oct-17
TID #: 01021	Project Title: TIDA-01021	
Number: TIDA-01021 Rev: E2	Sheet Title:	
SVN Rev: Version control disabled	Assembly Variant: [No Variations]	Sheet: 9 of 9
Drawn By:	File: TIDA-01021_E2_Hardware.SchDoc	Size: B
Engineer: Ajeet Pal	Contact: http://www.ti.com/support	





Layer	Name	Material	Thickness	Constant	Board Layer	Stack
1	Top Overlay					
2	Top Solder	Solder Resist	0.40mil	3.5		
3	Top Layer	Copper	1.40mil			
4	Dielectric	Rogers 4003C	12.00mil	4.2		
5	GND Layer	Copper	0.70mil			
6	Dielectric 4	FR4 370	8.50mil	4.2		
7	Signal Layer 1	Copper	1.40mil			
8	Dielectric 3	FR4 370	14.50mil	4.2		
9	Signal Layer 2	Copper	1.40mil			
10	Dielectric 5	FR4 370	8.50mil	4.2		
11	PhR Layer	Copper	0.70mil			
12	Dielectric 2	FR4 370	8.00mil	4.2		
13	Bottom Layer	Copper	1.40mil			
14	Bottom Solder	Solder Resist	0.40mil	3.5		
15	Bottom Overlay					

IMPEDANCE TABLE:—

Layer	SE IOP (CMD)	WIDTH (INCHES)	DIFF IOP (CMD)	DIFF TRACING (INCHES)	DIFF IOP (CMD)	WIDTH/SPACING (IN INCHES)	REFERENCE Layer
TOP	50ICPUD	22mil 24mil	90 ohms -	17mil trace/ 19mil space	100 ohms	12mil trace/ 8mil space	GN2 Layer
SIGNAL Layer 1	50	10.5 mil	90 ohms	-	100 ohms	5.5mil trace/ 6mil space	GN0 Layer
SIGNAL Layer 2	50	10.5 mil	90 ohms	-	100 ohms	5.5mil trace/ 6mil space	PUB Layer
BOTTOM Layer 1	50	13.5 mil	90 ohms	-	100 ohms	4.25mil trace/ 4.25mil space	PUB Layer

22 mil (CPW) width on top layer should be controlled 50 ohms +/- 5%
ALL SMA CONNECTORS TO FLUSH TO THE EDGE OF THE BOARD, NO GAP ALLOWED.
This is especially critical for: RFoutAP, RFoutAM, RFoutBP, and RFoutBM SMA connectors

DESIGN INFORMATION			
BOARD SIZE	(REFER ALSO ARRAY/PANEL PROFILING INFORMATION)		
175MM	X	130mm	
Number of Layers :	6		
MIN. TRACK WIDTH:	4.25 MIL		
MIN. CLEARANCE:	4.25 MIL		
MIN. VIA PAD SIZE:	16 MIL		
MINIMUM ANNUAL RING 5.0MM	EXTERNAL		
PER IPC-D-275 CLASS 2 LEVEL C			
REGISTRATION TOLERANCE: METAL +/-	5 MIL	HOLES +/-	3 MIL

MATERIAL:			
<input type="checkbox"/> FR-408	<input type="checkbox"/> FR-4 High Tg	<input checked="" type="checkbox"/> OTHER	ROGERS4002C and FCW 370
THICKNESS: <input checked="" type="checkbox"/> 63 MIL (1.6mm)	+/-10%		<input type="checkbox"/> OTHER
TOLERANCE:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2		
	<input type="checkbox"/> OTHER +/-		
BOW & TWIST:	<input checked="" type="checkbox"/> ANSI IPC-6012 TYPE 3 CLASS 2		
	<input type="checkbox"/> OTHER +/-		

COPPER THICKNESS (FINISHED):

OUTER: <input checked="" type="checkbox"/> 1.4MIL (1oz)	<input type="checkbox"/> 2MIL (1.4oz)	<input type="checkbox"/> 2.8MIL (2oz)
INNER SIGNAL: <input checked="" type="checkbox"/> 1.4MIL (1oz)	<input type="checkbox"/> 0.7MIL (1/2oz)	<input type="checkbox"/> N/A

DRILLING:

REFERENCE: <input checked="" type="checkbox"/> AS SHOWN	<input type="checkbox"/> NC_DRILL FILES
PTH MIN COPPER THICKNESS: <input checked="" type="checkbox"/> 1MIL	<input type="checkbox"/> OTHER

BOARD FINISH:

SILKSCREEN: <input checked="" type="checkbox"/> TOP	<input checked="" type="checkbox"/> BOTTOM
SILKSCREEN COLOR: <input checked="" type="checkbox"/> WHITE	<input type="checkbox"/> OTHER

SOLDER RESIST COLOR:

<input type="checkbox"/> GREEN	<input checked="" type="checkbox"/> BLUE	<input type="checkbox"/> OTHER
--------------------------------	--	--------------------------------

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG)
 ☐ ENEPG || ☐ IMM. TIN/SILVER OR EQUIV | ☐ OTHER |

ARRAY/PANEL:

<input type="checkbox"/> CUT AND TRIM PER MECH. LABEL 1	
<input type="checkbox"/> N.C. ROUTE	<input type="checkbox"/> V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:

<input checked="" type="checkbox"/> ANSI IPC-A-600F CLASS ->	<input type="checkbox"/> 1	<input checked="" type="checkbox"/> 2	<input type="checkbox"/> 3
<input checked="" type="checkbox"/> RoHS	<input type="checkbox"/> OTHER	PER ORDER	

ADDITIONAL REQUIREMENTS: VIA TENTING: YES ☐ NO ☒

MICROSECTION: ☐ YES ☒ IMPEDANCE CONTROL: YES ☐ NO ☒

BAR CODE BLDG. ELEC. TEST: ☐ NONE ☐ X ☒ REQUIRED ☐ PER ORDER

MANUFACTURERS' UL: ☐ RAIL ☐ METAL ☐ SLK



TIDA-01021	
DESIGNED FOR: Public Release	
FILE NAME: TIDA-01021_E2.PcbDoc	
ENGINEER: Ajeet Pal	LAYOUT BY: Avinash N
SCALE: 1.00	ALTIM DESIGNER VERSION: 16.1.9.221