

FAB NOTES :

1. THE SOLDER MASK IMAGES THAT ARE THE SAME SIZE AS THE COMPONENT PADS MAY BE ENLARGED AS PER THE MANUFACTURING CAPABILITIES BUT NOT BEYOND 0.08MM PER SIDE OR 0.15MM OVERALL. ALL OTHER SOLDER MASK IMAGES SHALL NOT BE MODIFIED.

LAYER STACK-UP :

Layer	Name	Material	Thickness	Constant	Board Layer Stack
	Top Overlay				
	Top Solder	Solder Resist	1.00mil	3.5	
1	Top Layer		1.85mil		
	Dielectric 1		5.48mil	4.2	
2	L02_GND		1.26mil		
	Dielectric 2		42.82mil	4.2	
3	L03_PWR		1.26mil		
	Dielectric 3		5.48mil	4.2	
4	Bottom Layer		1.85mil		
	Bottom Solder	Solder Resist	1.00mil	3.5	
	Bottom Overlay				

THIS IS AN IMPEDANCE CONTROLLED BOARD.

NOTE :

1. ALL CORE AND PREPREG THICKNESSES ARE UP TO FAB SHOP TO SELECT.
2. EXTERNAL LAYER CU THICKNESSES ARE FINISHED THICKNESS AFTER PLATING.

IMPEDANCE TABLE

LAYER NO	CONDUCTOR WIDTH	SPACING	IMPEDANCE +/- 10%	REFERENCE GND
1	10.25	15.5 mil	50 OHMS	GND

DRILL CHART :

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Hole Tolerance
□	741	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
▽	13	8.00mil (0.203mm)	PTH	Round	Top Layer - Bottom Layer	
⊗	7	12.00mil (0.305mm)	PTH	Round	Top Layer - Bottom Layer	+0.00mil/-4.00mil
●	2	16.00mil (0.406mm)	PTH	Round	Top Layer - Bottom Layer	
⊗	10	27.95mil (0.710mm)	PTH	Round	Top Layer - Bottom Layer	
⊗	2	33.47mil (0.859mm)	PTH	Round	Top Layer - Bottom Layer	
⊗	20	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	+/-7.87mil
○	40	40.16mil (1.020mm)	PTH	Round	Top Layer - Bottom Layer	
⊗	19	45.28mil (1.150mm)	PTH	Round	Top Layer - Bottom Layer	
◇	2	23.62mil (0.600mm)	PTH	Slot	Top Layer - Bottom Layer	
	856 Total					

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 4 MIL
MIN. VIA PAD SIZE: 14 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL

MATERIAL:

☐ FR-408 ☒ FR-4 High Tg ☐ OTHER
THICKNESS: ☒ 62 MIL (1.6mm) +/-10% ☐ OTHER
TOLERANCE: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-
BOW & TWIST: ☒ ANSI IPC-6012 TYPE 3 CLASS 2
☐ OTHER +/-

DRILLING:

REFERENCE: ☒ AS SHOWN ☒ NC_DRILL FILES
PTH COPPER THICKNESS: ☒ 20-30 um ☐ OTHER

BOARD FINISH:

SILKSCREEN: ☒ TOP ☒ BOTTOM
SILKSCREEN COLOR: ☒ WHITE ☐ OTHER
SOLDER RESIST COLOR: ☐ GREEN ☒ OTHER RED
☒ MATTE ☐ SEMI-GLOSS

SURFACE FINISH: ☒ IMMERSION GOLD (ENIG) ☐ ENEPIG
☐ IMM. TIN/SILVER OR EQUIV ☐ OTHER

ARRAY/PANEL: ☐ CUT AND TRIM PER M1 BOARD OUTLINE
☒ N.C. ROUTE ☐ V. SCORE

CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBs TO MEET OR EXCEED THE REQUIREMENTS OF:
☒ ANSI IPC-A-600F CLASS -> ☐ 1 ☒ 2 ☐ 3
☒ RoHS ☐ OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:

MICROSECTION: ☐ YES
BARE BOARD ELEC. TEST: ☐ NONE ☒ REQUIRED ☐ PER ORDER
MANUFACTURER'S UL: ☐ RAIL ☐ METAL ☒ SILK



PROJECT TITLE:

BP-CC33xxMOD

DESIGNED FOR:

Public Release

FILE NAME:

BP-CC33xxMOD.PcbDoc

ENGINEER:

Andy Bui

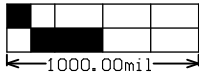
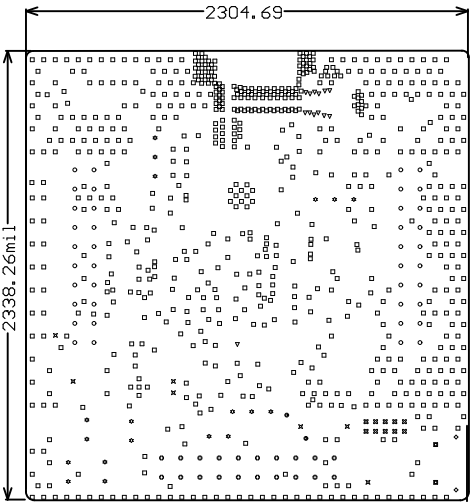
LAYOUT BY:

Jonathan Cohen

SCALE: 1.00

ALTUM DESIGNER VERSION:

23.1.1.15



ALL ARTWORK VIEWED FROM TOP SIDE

BOARD #: MCU135

REV: A

SUN REV: c8872701c31a49ee63b39f683482a30c1b53cfd

LAYER NAME = 000000-135-01

TID #: N/A

PLOT NAME = Fabrication Drawing

GENERATED : 3/10/2025 3:15:00 PM

TEXAS INSTRUMENTS

Texas Instruments (TI) and/or its licensors do not warrant the accuracy or completeness of this specification or any information contained therein. TI and/or its licensors do not warrant that this design will meet the specifications, will be suitable for your application or fit for any particular purpose, or will operate in an implementation. TI and/or its licensors do not warrant that the design is production worthy. You should completely validate and test your design implementation to confirm the system functionality for your application.