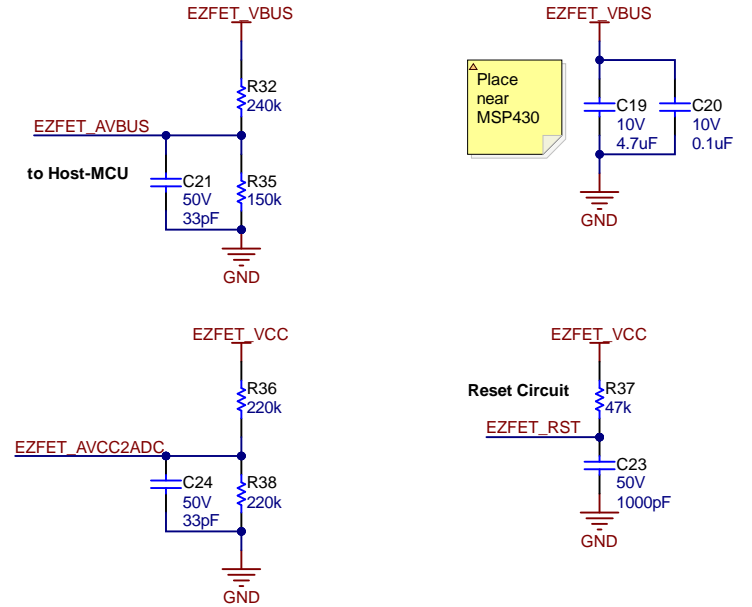
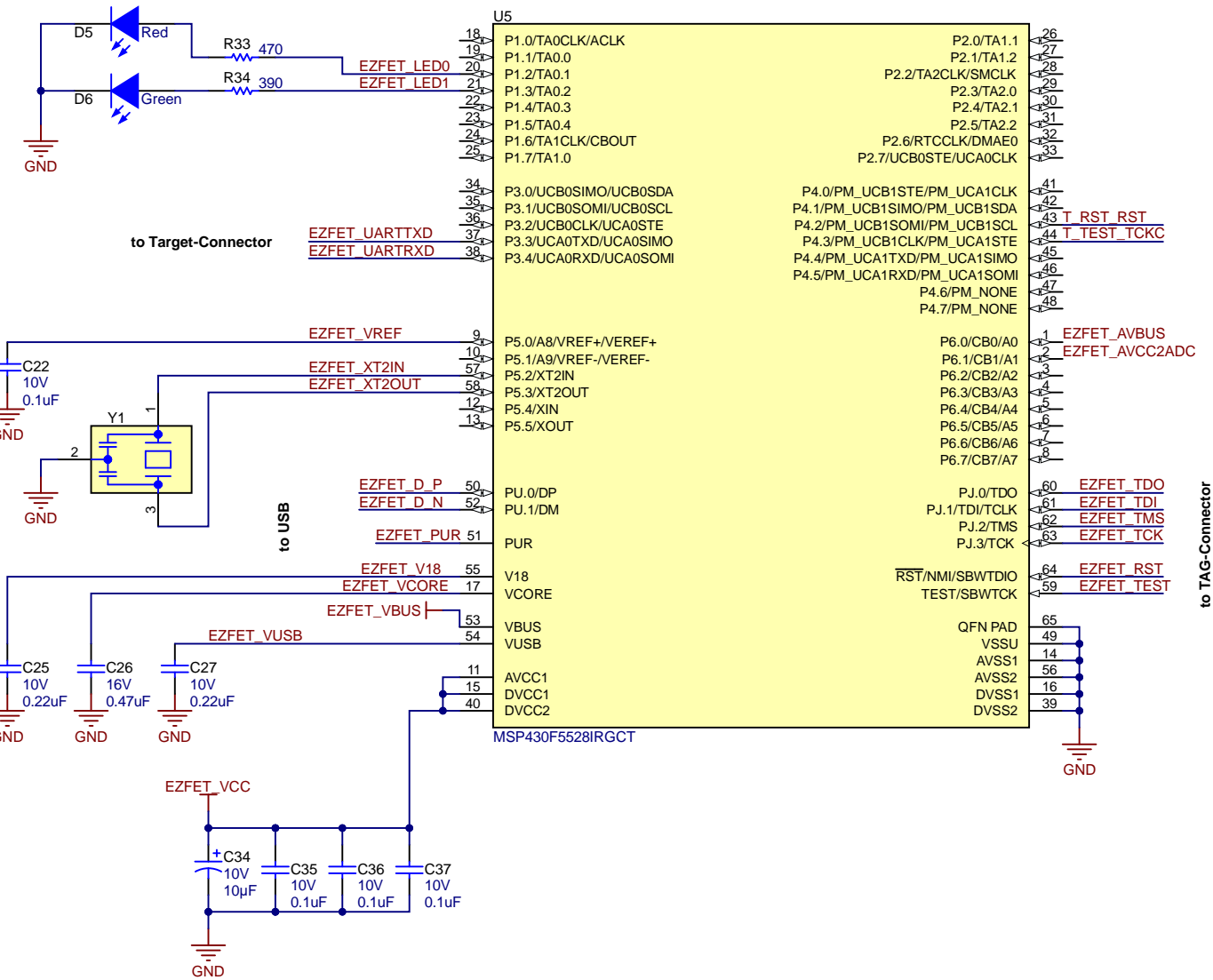
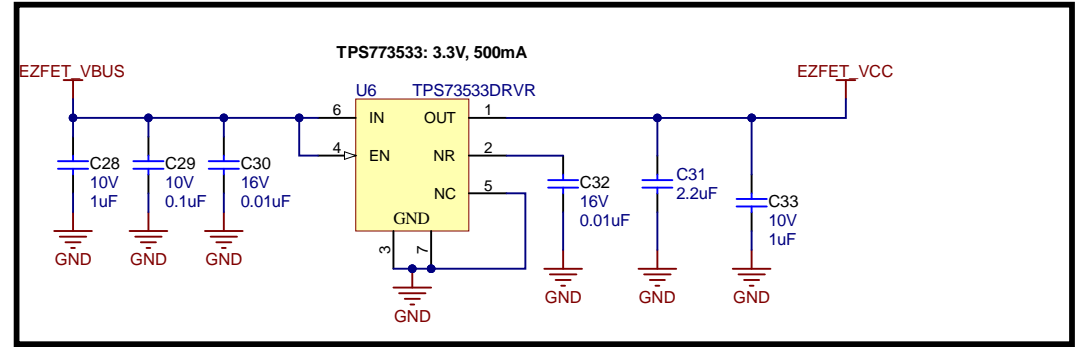


# Host MCU for Emulation

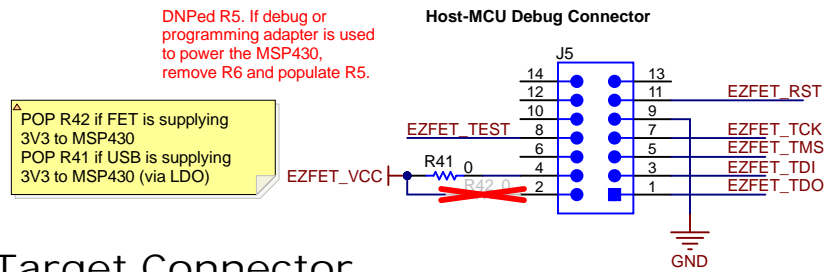


## 3.3V Power (EZFET\_VCC)

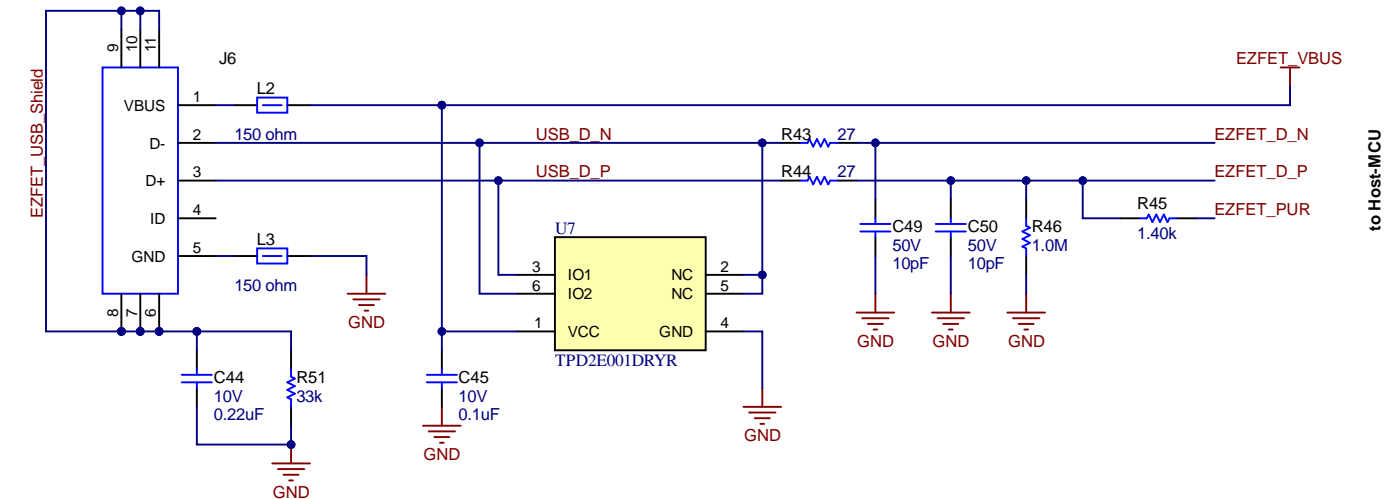


## JTAG-Connector (Host Debug)

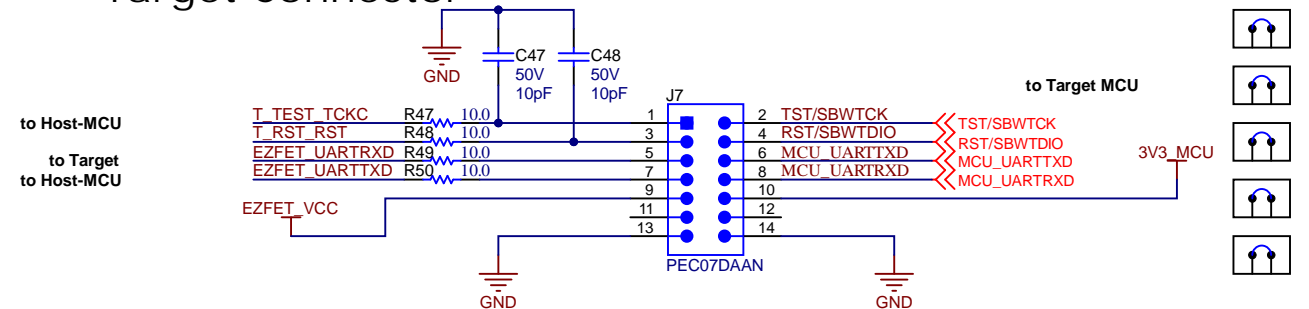
DNPed R5. If debug or programming adapter is used to power the MSP430, remove R6 and populate R5.



## USB-I nterface



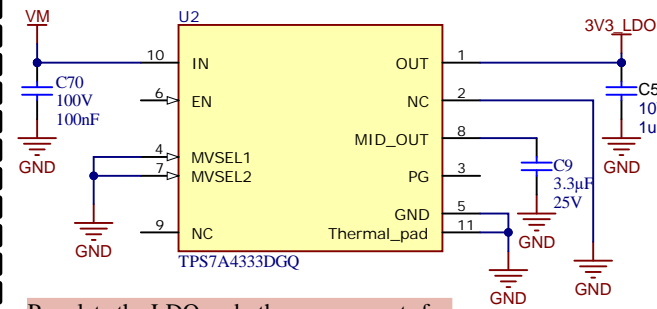
## Target Connector



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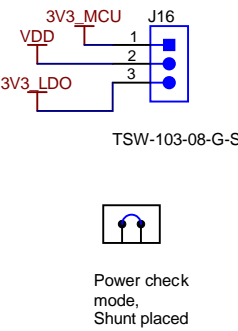
Orderable: DRV8263S-Q1EVM	Designed for: Public Release	Mod. Date: 6/20/2024
TID #: N/A	Project Title: DRV8263S/H-Q1EVM VQFN	
Number: MD093	Rev: E1	Sheet Title:
SVN Rev:	Assembly Variant: 001	Sheet: 1 of 3
Drawn By:	File: ezFET.SchDoc	Size: B
Engineer: Jacob Thompson	Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>	<a href="http://www.ti.com">http://www.ti.com</a>

### 3.3V LDO

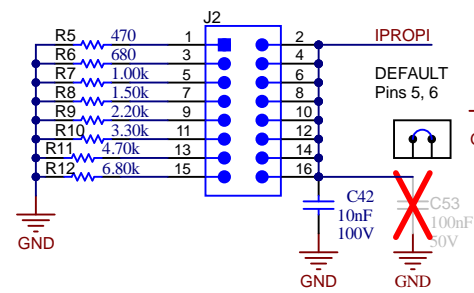


Populate the LDO and other components for prototype testing. Consider DNP it for production.

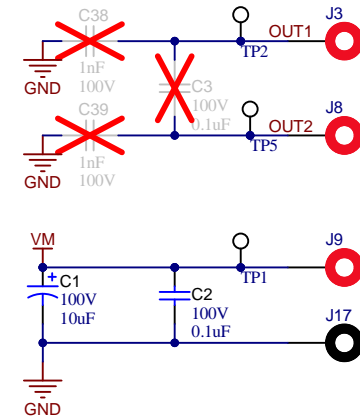
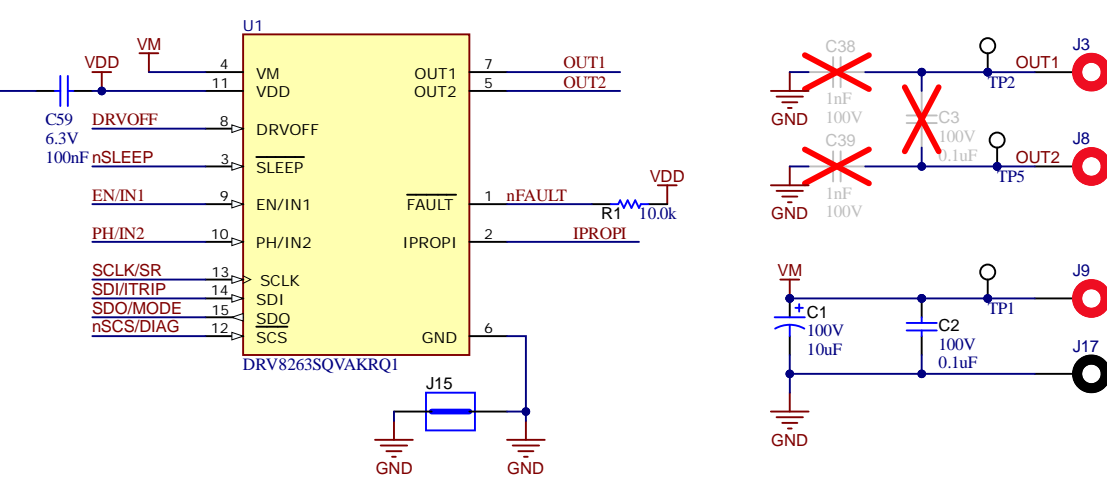
## Power Check



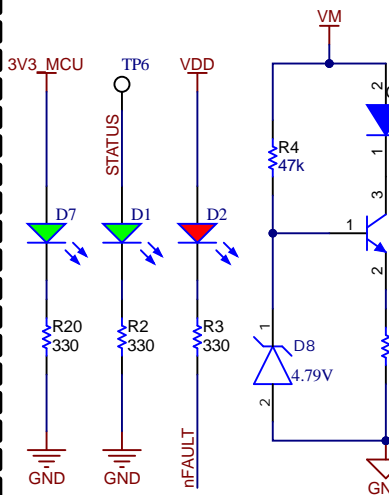
$$ITRIP = V(TRIP)/R(IPROPI) * A\_IPROP$$



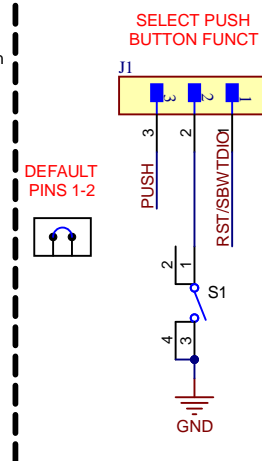
## DRV8263S/H-Q1 VQFN



## LEDS



## BUTTON

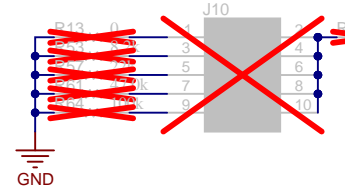


## ANALOG CONTROL SIGNALS (H-variant only)

ITRIP  
Levels  
1 0v  
2 1.65v  
3 1.98v  
4 2.31v  
5 2.64v  
6 2.97v

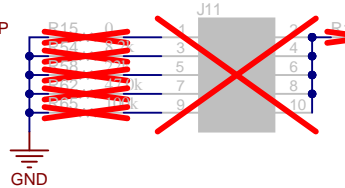
ITRIP	
PINS	ITRIP
1, 2	LVL1
3, 4	LVL2
5, 6	LVL3
7, 8	LVL4
9,10	LVL5
DNI	LVL6

DEFAULT  
Pins 3, 4



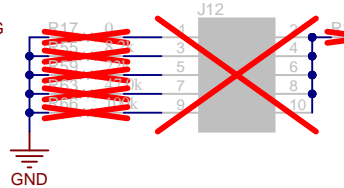
DIAG	
PINS	DIAG
1, 2	LVL1
3, 4	LVL2
5, 6	LVL3
7, 8	LVL4
9,10	LVL5
DNI	LVL6

DEFAULT  
Pins 3, 4



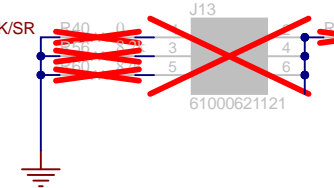
SLEW RATE	
PINS	SR
1, 2	LVL1
3, 4	LVL2
5, 6	LVL3
7, 8	LVL4
9,10	LVL5
DNI	LVL6

DEFAULT  
Pins 3, 4

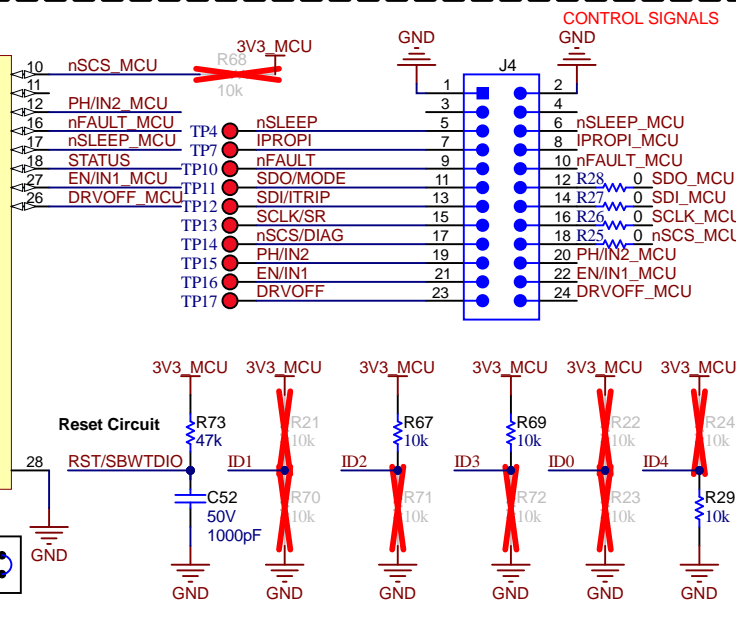
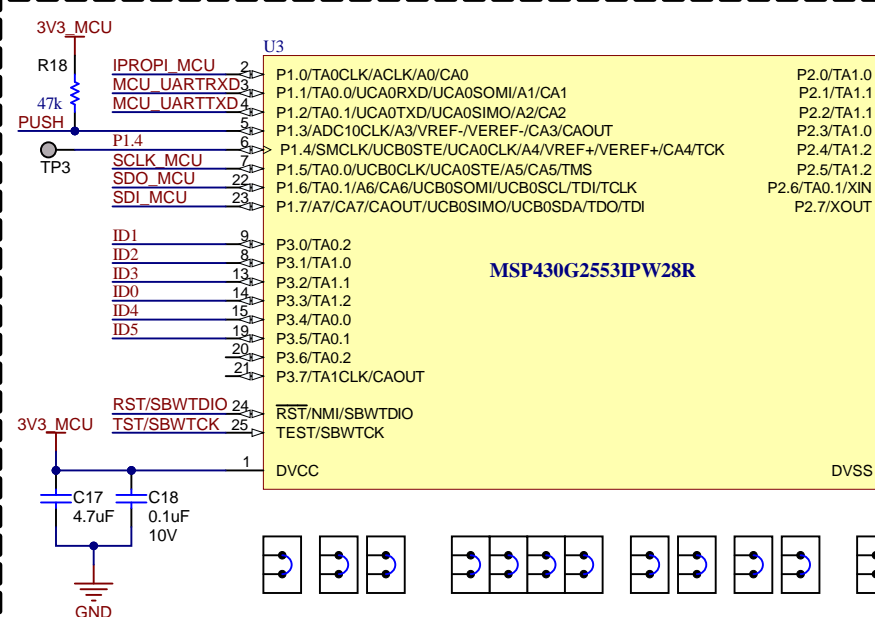


PINS	MODE
1, 2	LVL1
3, 4	LVL2
5, 6	LVL3
DNI	LVL4

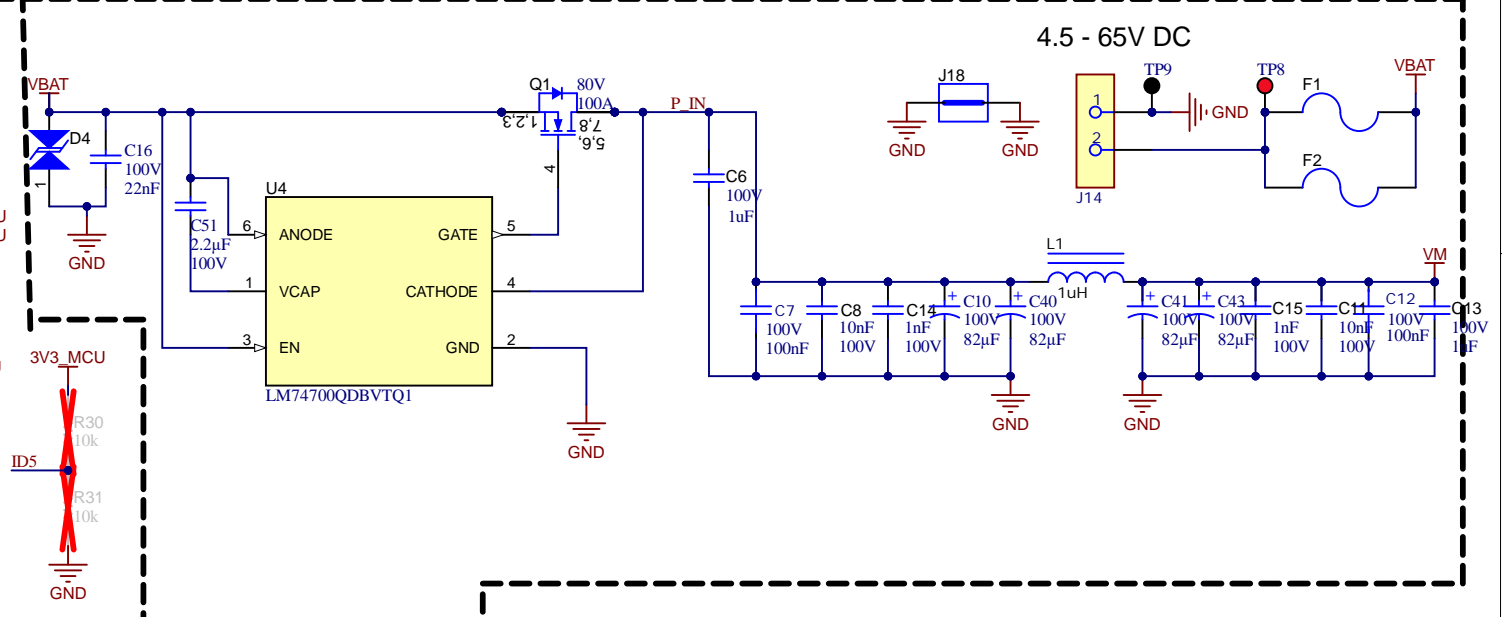
DEFAULT  
Pins 5,6



## MSP430



## MAIN INPUT SUPPLY REVERSE PROTECTION & FILTER



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Orderable: <b>DRV8263S-Q1EVM</b>	Designed for: <b>Public Release</b>	Mod. Date: 6/26/2024		
TID #: <b>N/A</b>	Project Title: <b>DRV8263S/H-Q1EVM VQFN</b>			
Number: <b>MD093</b>	Rev: <b>E1</b>	Sheet Title:		
SVN Rev: <b>Unknown revision</b>		Assembly Variant: <b>001</b>		Sheet: <b>2</b> of <b>3</b>
Drawn By:		File: <b>MD093E1_DRV8263-Q1EVM_VQFN.SchDoc</b>		Size: <b>B</b>
Engineer: <b>Jacob Thompson</b>		Contact: <a href="http://www.ti.com/support">http://www.ti.com/support</a>		<a href="http://www.ti.com">http://www.ti.com</a> © Texas Instruments 2024

H1  
SJ-5303 (CLEAR)

H2  
SJ-5303 (CLEAR)

H3  
SJ-5303 (CLEAR)

H4  
SJ-5303 (CLEAR)

FID1

FID2

FID3

PCB Number: MD093

PCB Rev: E1

PCB  
LOGO

Texas Instruments

CE Mark

PCB  
LOGO

FCC disclaimer

PCB  
LOGO

WEEE logo

CAUTION HOT SURFACE

PCB  
LOGO

CAUTION. READ USER GUIDE BEFORE USE

LBL1

PCB Label

THT-14-423-10

Size: 0.65" x 0.20 "

ZZ1

Label Assembly Note

This Assembly Note is for PCB labels only

ZZ2

Assembly Note

These assemblies are ESD sensitive, ESD precautions shall be observed.

ZZ3

Assembly Note

These assemblies must be clean and free from flux and all contaminants. Use of no clean flux is not acceptable.

ZZ4

Assembly Note

These assemblies must comply with workmanship standards IPC-A-610 Class 2, unless otherwise specified.

Variant/Label Table	
Variant	Label Text
001	DRV8243S-Q1EVM
002	DRV8243H-Q1EVM

1

2

3

4

5

6