

NOTES, UNLESS OTHERWISE SPECIFIED:

1. The netname "P12V" represents connection to the +12V power plane.
2. The netname "P3P3V" represents connection to the +3.3V power plane.
3. The netname "P1P8V" represents connection to the +1.8V digital power plane.
4. The netname "P1P1V" represents connection to the +1.1V power plane.
5. The netname "P1P8V ITEA" represents connection to the +1.8V ITE6535 analog supply power plane.
6. The netname "F_VCCIO" represents connection to the +3V FPGA Vccio power plane.
7. The netname "P2P5V_FAUXPLL" represents connection to the +2.5V FPGA aux/pll power plane.
8. The netname "P1P8V_A" represents connection to the +1.8V controller analog supply power plane.
9. The netname "GND" represents connection to the ground plane.
10. A "Z" suffix on a signal name indicates an active low signal.
11. All components with designators "U*", "Q*", and "D*" are electrostatic discharge sensitive.



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| REVISIONS | | | |
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| REV | DESCRIPTION | DATE | APPROVED |
| A | ECO 2137507: Initial Release | 11/1/2013 | NG |
| B | ECO 2140137: Updated to rev B | 2/18/2014 | NG |
| C | ECO 2141055: Updated to rev C | 4/8/2014 | NG |
| D | ECO 2142175: Updated to rev D | 5/28/2014 | NG |
| E | ECO 2144118: Updated to rev E | 8/8/2014 | NG |
| F | Updated to rev F | 11/7/2019 | DH |
| G | Updated to rev G | 5/11/2020 | DH |

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| | | ENGR A. NG | 8/8/2014 | | | |
| | | SYST | | | | |
| | | PRJ L. Harvey | 8/8/2014 | TITLE ESD, DLPLCR900DEVM DLP043 | | |
| 2513535 | 0314PO | QA | | | | |
| NEXT ASSY | USED ON | | | A3 | DRAWING NO 2513534 | REV G |
| APPLICATION | | SW Cadence 16.6 | | | | |
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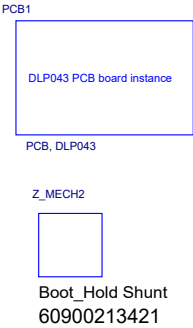
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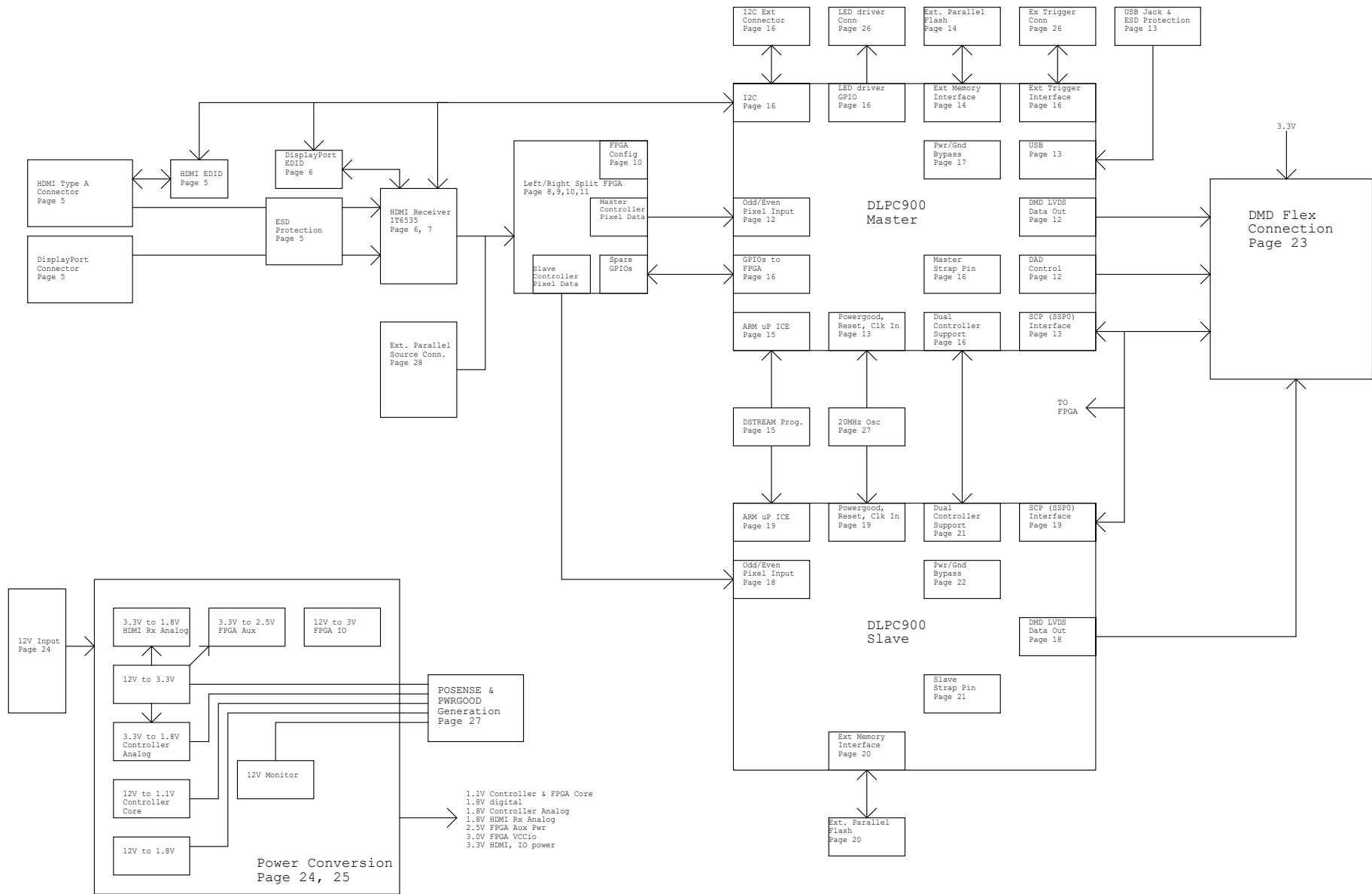
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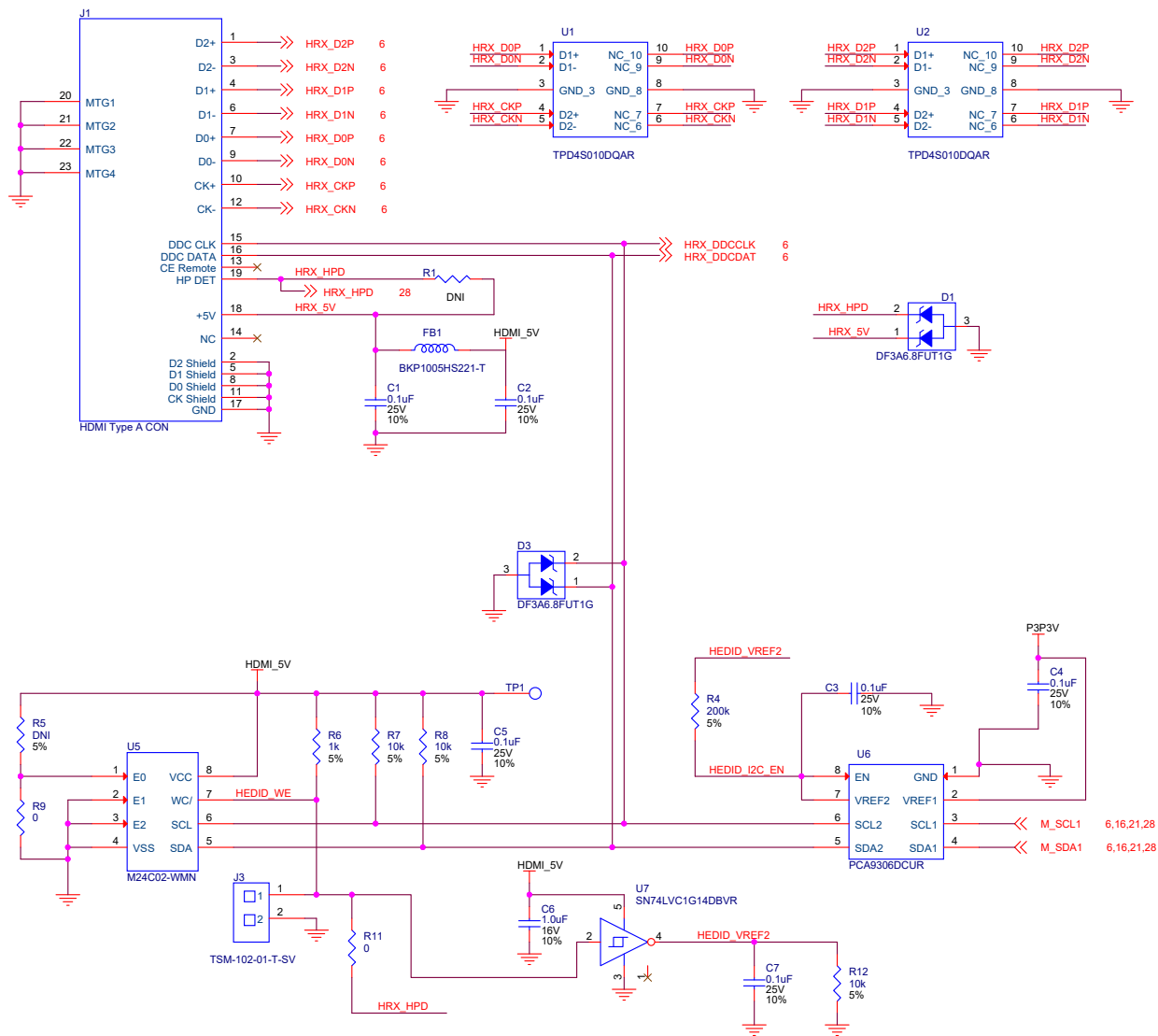




Block Diagram

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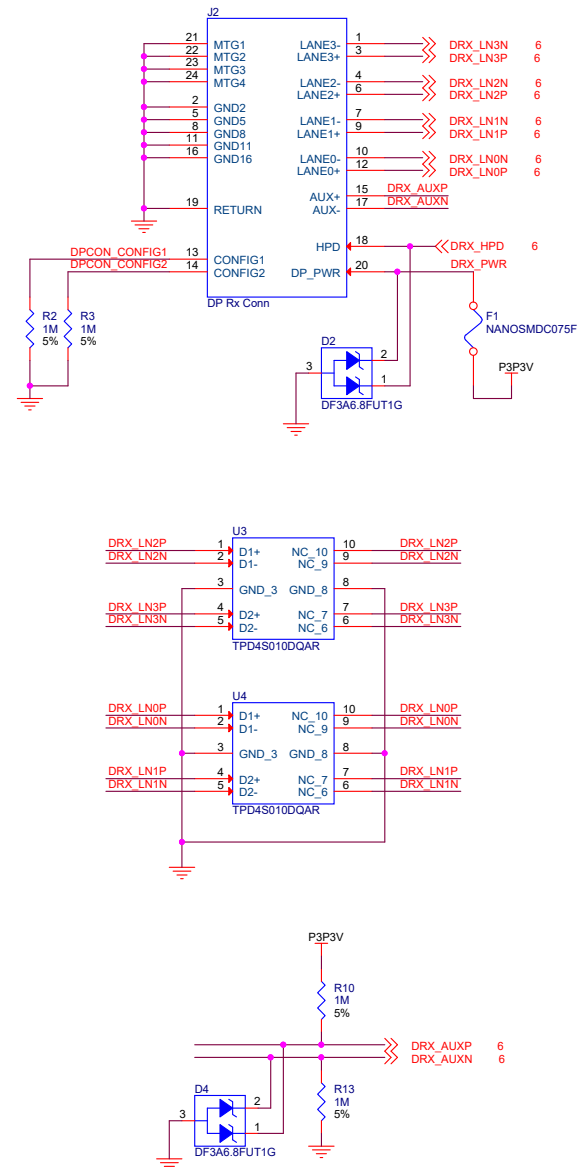
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To program HDMI EDID

- install jumper to enable PROM write and disable hot plug detect
- connect HDMI cable to supply 5V
- use TI control program to update EDID

HDMI TypeA Rx Conn, ESD, and EDID



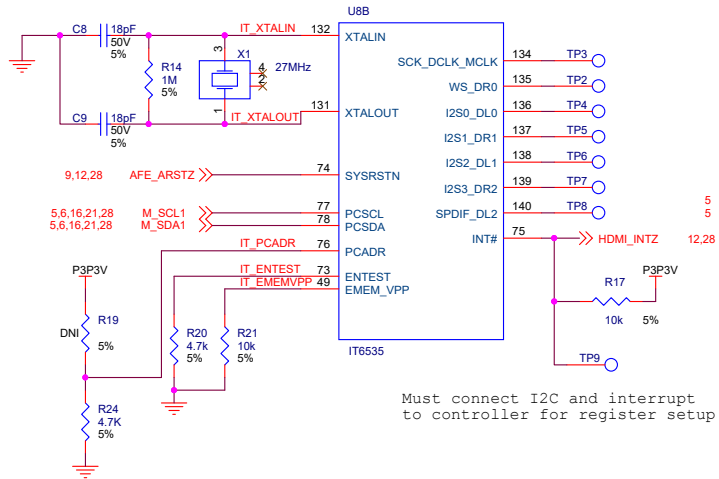
DisplayPort Rx Conn, ESD

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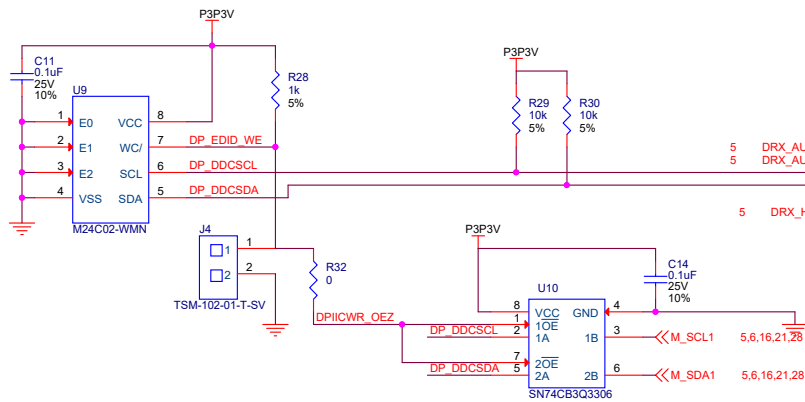
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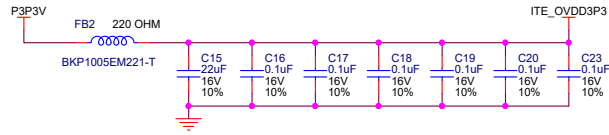
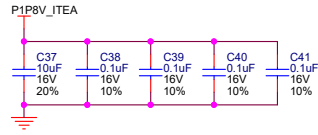
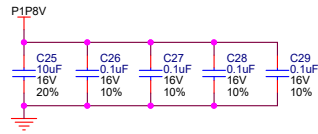
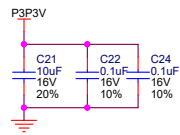
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Apply a crystal input
even audio function
is not used per ITE
recommndation

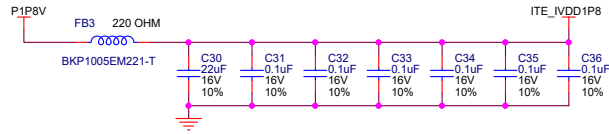


I2C address select
low = 0xB0
high = 0xB2

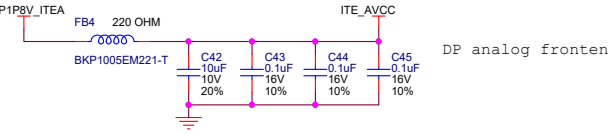




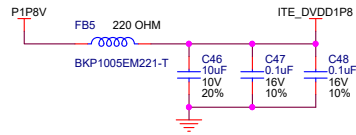
3.3V IO



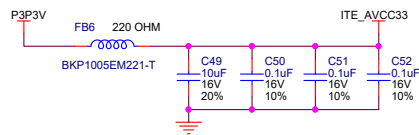
Digital logic core



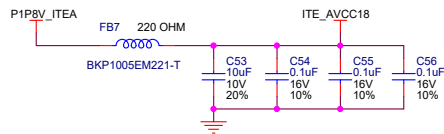
DP analog frontend



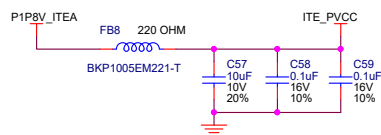
Logic power for analog frontend



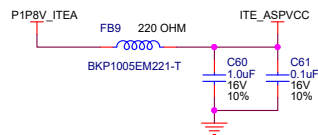
3.3V HDMI RX analog frontend



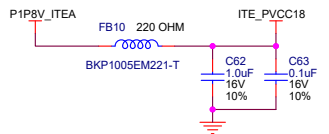
1.8V HDMI RX analog frontend



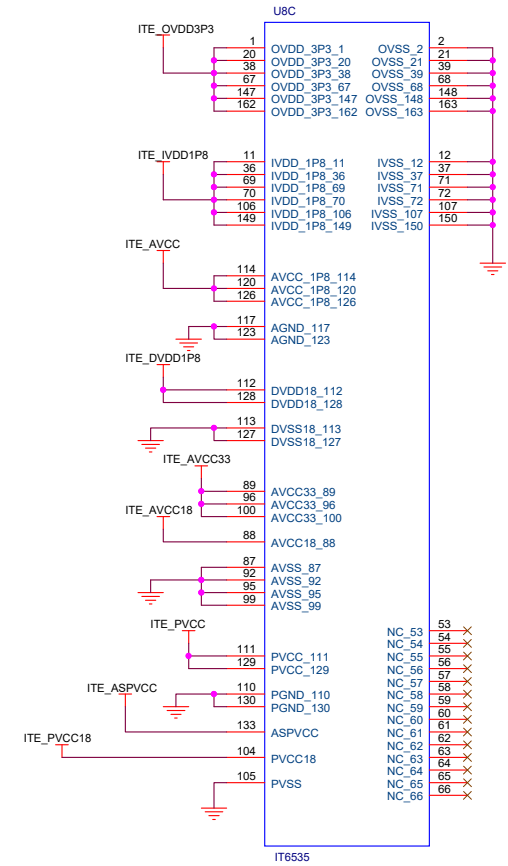
DP Rx PLL power



Crystal and audio PLL



HDMI Rx PLL power



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HDMI receiver Power / Gnd

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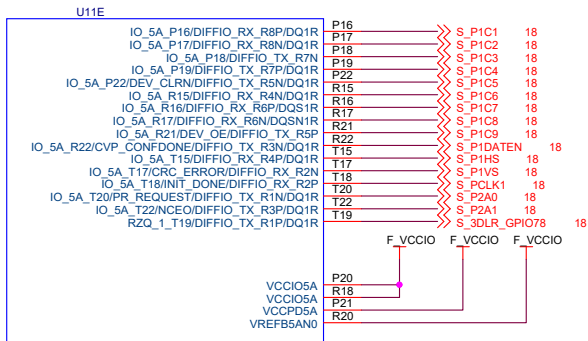
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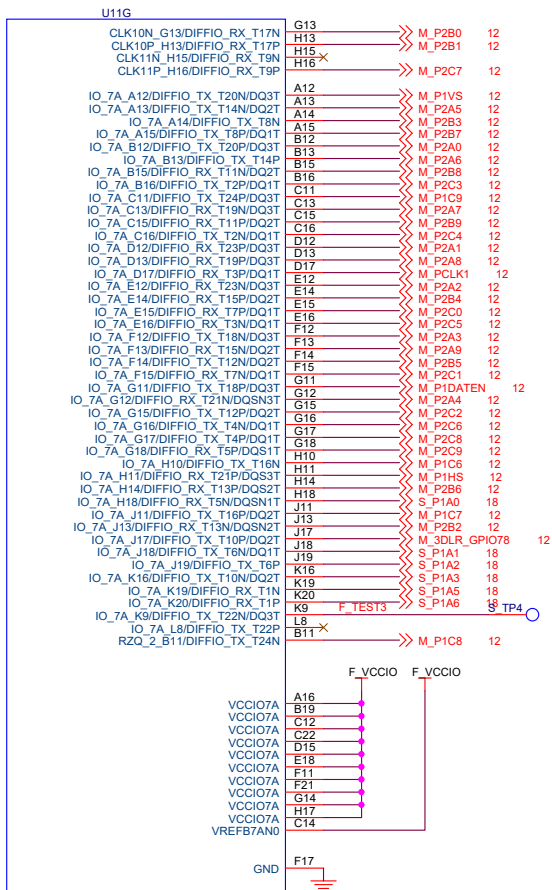
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Left/Right Split FPGA Bank 2A, 3A, 3B, 4A

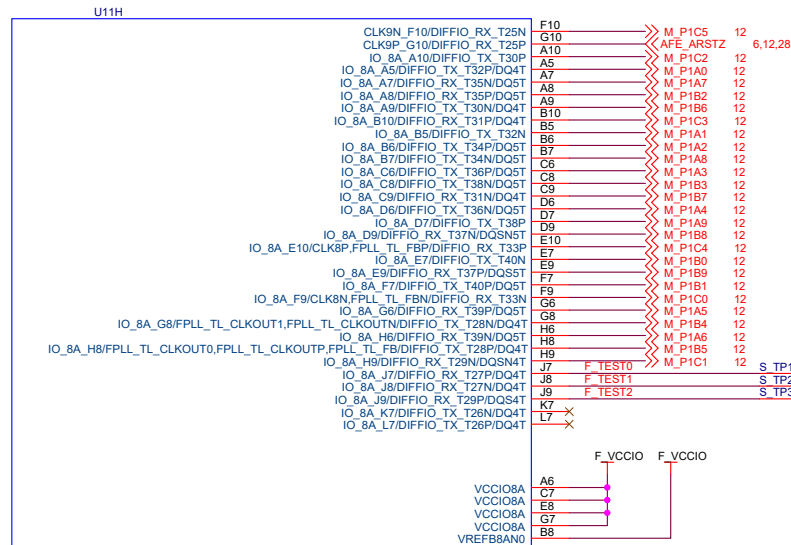
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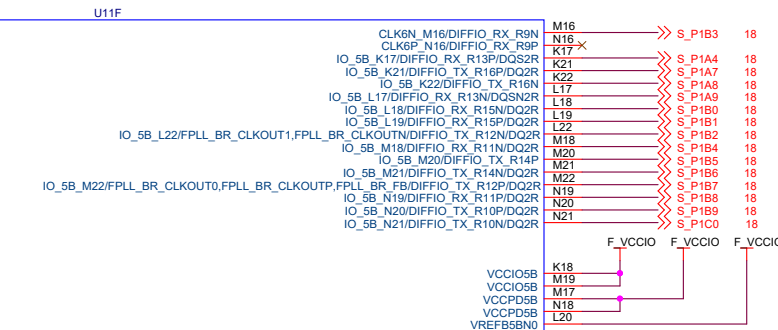
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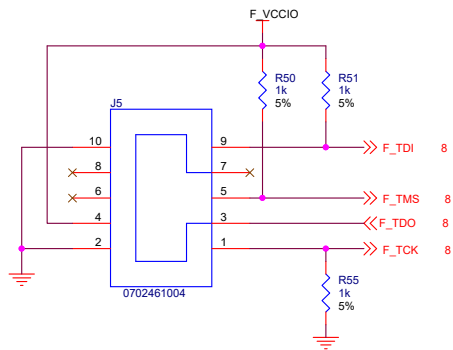
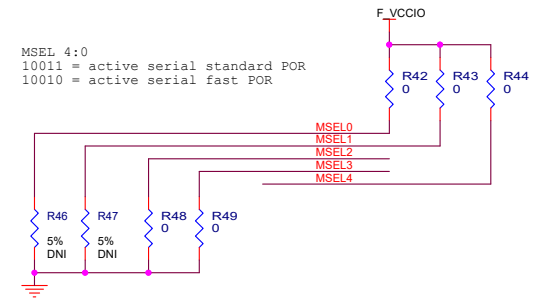
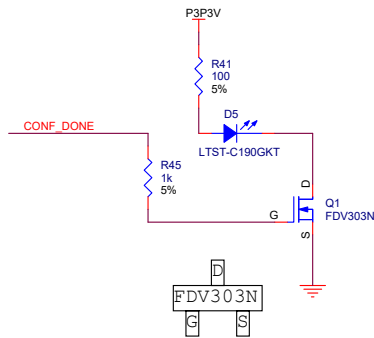
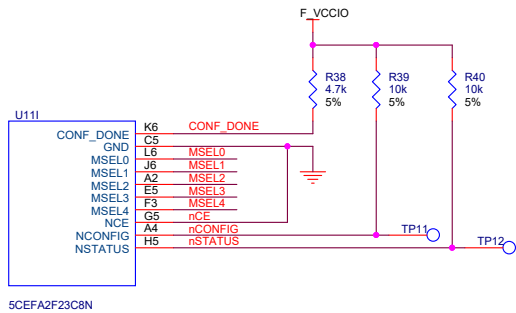


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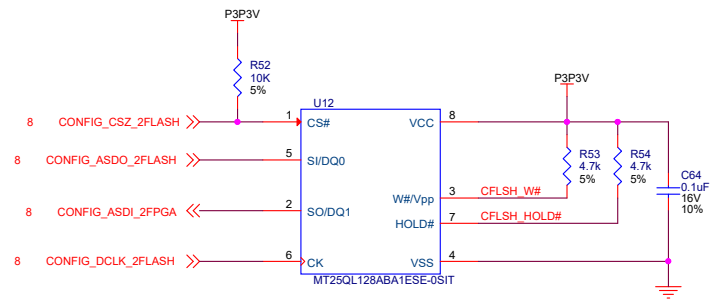
Left/Right Split FPGA Bank 5A, 5B, 7A, 8A

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Altera's USB ByteBlaster Connector

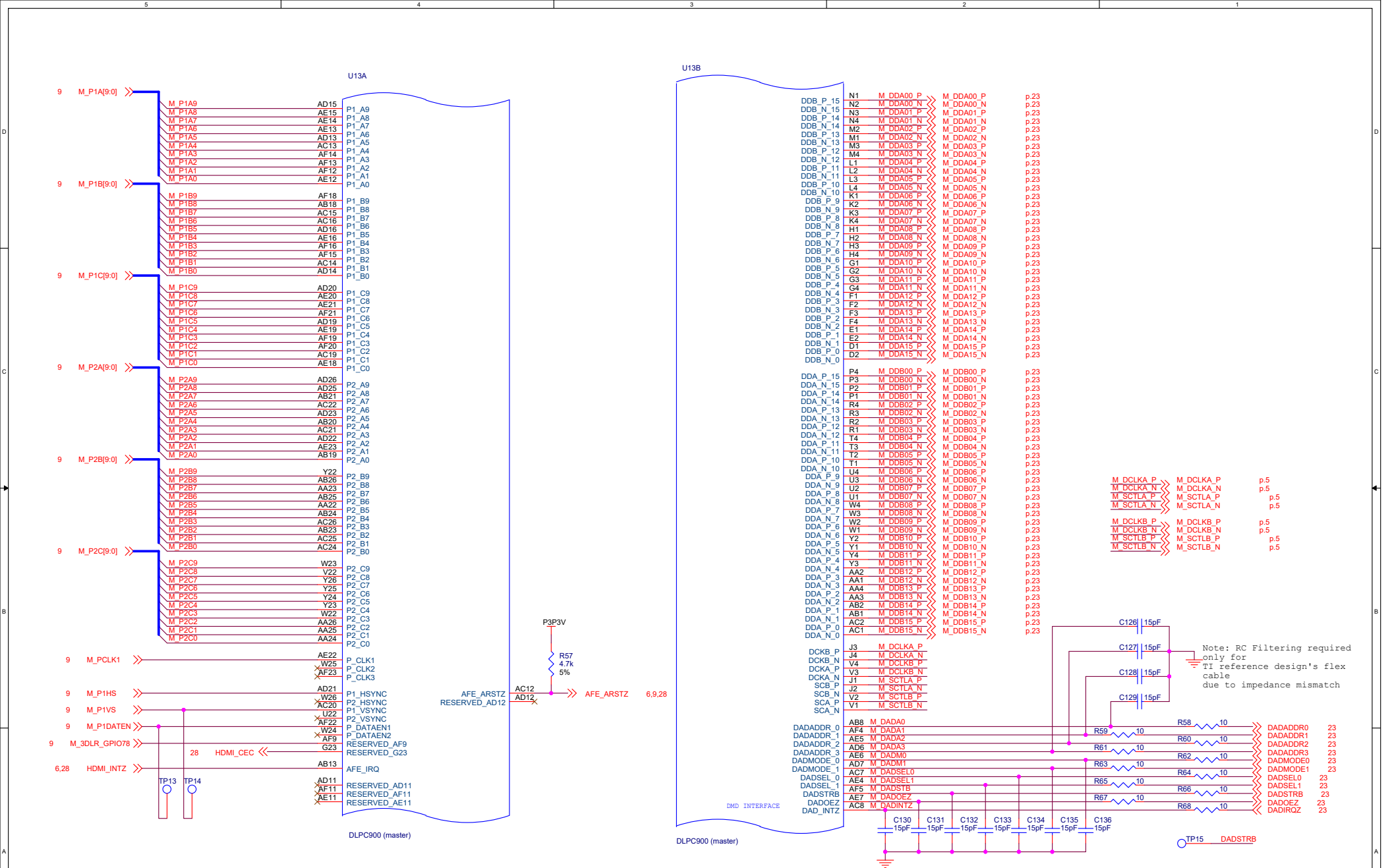


Use Altera's "Serial loader" option to update flash thru the FPGA JTAG port with Byteblaster cable

Left/Right Split FPGA Configuration

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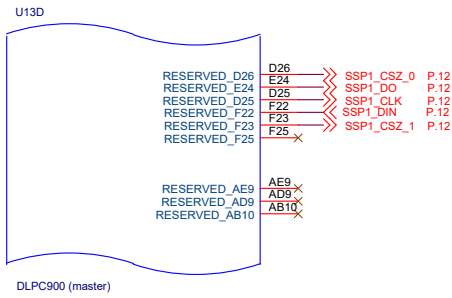
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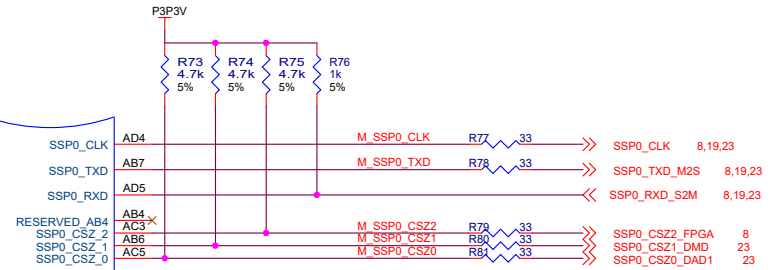
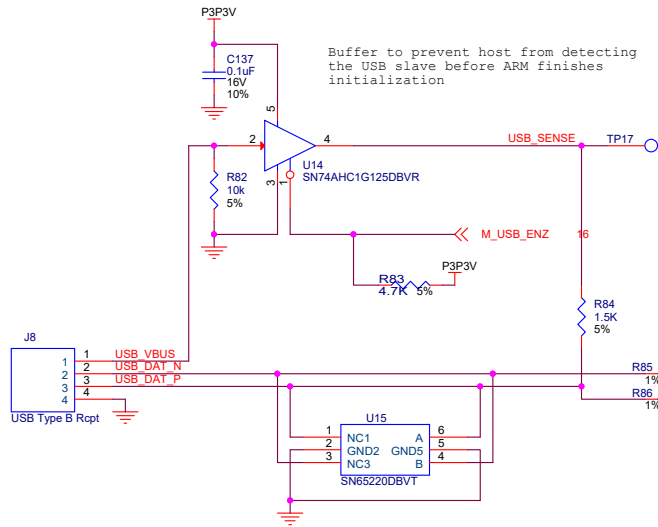
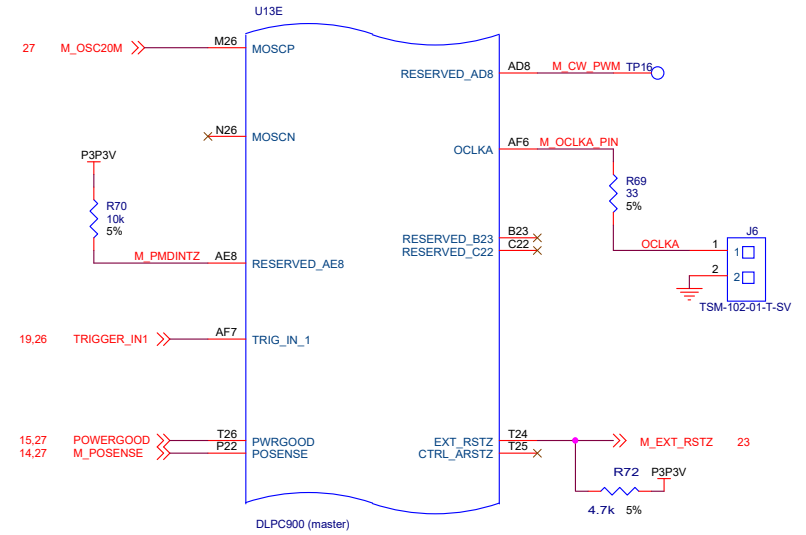
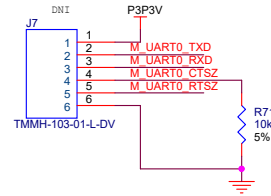
Master Controller Video Input, DMD & DAD Output

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UART debug message port,
not needed for production



Master Controller SSP0, UART0, USB, Reset, OSC

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U13F

PM_DATA_15
PM_DATA_14
PM_DATA_13
PM_DATA_12
PM_DATA_11
PM_DATA_10
PM_DATA_09
PM_DATA_08
PM_DATA_07
PM_DATA_06
PM_DATA_05
PM_DATA_04
PM_DATA_03
PM_DATA_02
PM_DATA_01
PM_DATA_00

GPIO_45 PM_ADDR
GPIO_46 PM_ADDR
GPIO_60 PM_ADDR

PM_ADDR_22
PM_ADDR_21
PM_ADDR_20
PM_ADDR_19
PM_ADDR_18
PM_ADDR_17
PM_ADDR_16
PM_ADDR_15
PM_ADDR_14
PM_ADDR_13
PM_ADDR_12
PM_ADDR_11
PM_ADDR_10
PM_ADDR_09
PM_ADDR_08
PM_ADDR_07
PM_ADDR_06
PM_ADDR_05
PM_ADDR_04
PM_ADDR_03
PM_ADDR_02
PM_ADDR_01
PM_ADDR_00

PM_BLSZ_1
PM_BLSZ_0

PM_WEZ
PM_OEZ

PM_CSZ_0
PM_CSZ_1
PM_CSZ_2

C17 M_PMDATA_15
B16 M_PMDATA_14
A16 M_PMDATA_13
A15 M_PMDATA_12
B15 M_PMDATA_11
D16 M_PMDATA_10
C16 M_PMDATA_09
E14 M_PMDATA_08
D15 M_PMDATA_07
C15 M_PMDATA_06
B14 M_PMDATA_05
A14 M_PMDATA_04
E13 M_PMDATA_03
D14 M_PMDATA_02
C14 M_PMDATA_01
B13 M_PMDATA_00

U23 M_PM_ADDR_GPIO45
Y22 M_PM_ADDR_GPIO46
H22 M_PM_ADDR_GPIO60

A12 M_PMADDR22
E11 M_PMADDR21
D12 M_PMADDR20
C12 M_PMADDR19
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C11 M_PMADDR15
E10 M_PMADDR14
D10 M_PMADDR13
C10 M_PMADDR12
B9 M_PMADDR11
A9 M_PMADDR10
E9 M_PMADDR09
D9 M_PMADDR08
C9 M_PMADDR07
B8 M_PMADDR06
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C7 M_PMADDR00

B6
A6

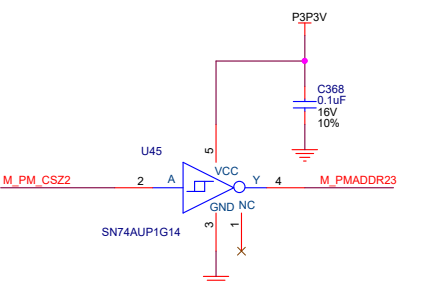
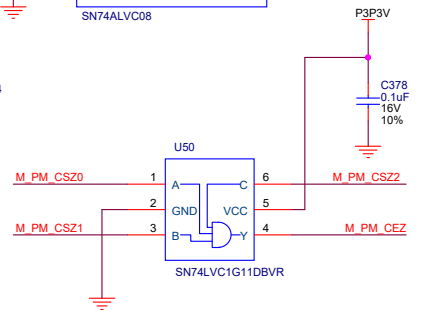
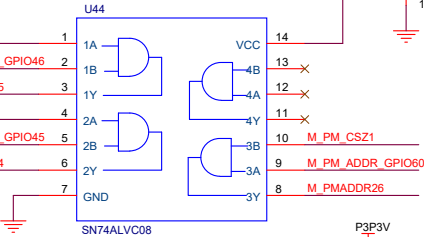
B12 M_PMWEZ_PIN
C13 M_PM_OEZ

D13 M_PM_CSZ0
E12 M_PM_CSZ1
A13 M_PM_CSZ2

R260 10k 5%
R261 10k 5%
R252 10k 5%
R253 10k 5%
R254 10k 5%

R91 22 1%
R92 10k 5%
R93 10k 5%
R94 10k 5%

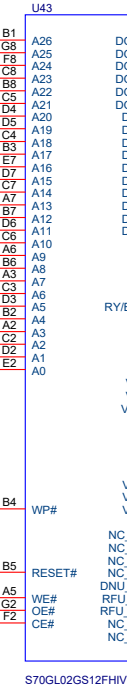
M_PM_CSZ1
M_PM_ADDR_GPIO46
M_PMADDR25
M_PM_CSZ1
M_PM_ADDR_GPIO45
M_PMADDR24



M_PMADDR26
M_PMADDR25
M_PMADDR24
M_PMADDR23
M_PMADDR22
M_PMADDR21
M_PMADDR20
M_PMADDR19
M_PMADDR18
M_PMADDR17
M_PMADDR16
M_PMADDR15
M_PMADDR14
M_PMADDR13
M_PMADDR12
M_PMADDR11
M_PMADDR10
M_PMADDR09
M_PMADDR08
M_PMADDR07
M_PMADDR06
M_PMADDR05
M_PMADDR04
M_PMADDR03
M_PMADDR02
M_PMADDR01
M_PMADDR00

R89 10k 5%
M_FLASH0_WP#

13,27 M_POSENSE
M_PM_WEZ
M_PM_OEZ
M_PM_CEZ



DQ15
DQ14
DQ13
DQ12
DQ11
DQ10
DQ9
DQ8
DQ7
DQ6
DQ5
DQ4
DQ3
DQ2
DQ1
DQ0

RY/BY#
A4 MFLASH_RYBYZ

VIO
VIO
VCC
E8
VSS
VSS
VSS
NC_A1
NC_A8
NC_C1
NC_D1
DN_U1
WE#
RFU_G1
NC_H1
NC_H8

C138 0.1uF 16V 10%
C139 0.1uF 16V 10%
C379 0.1uF 16V 10%

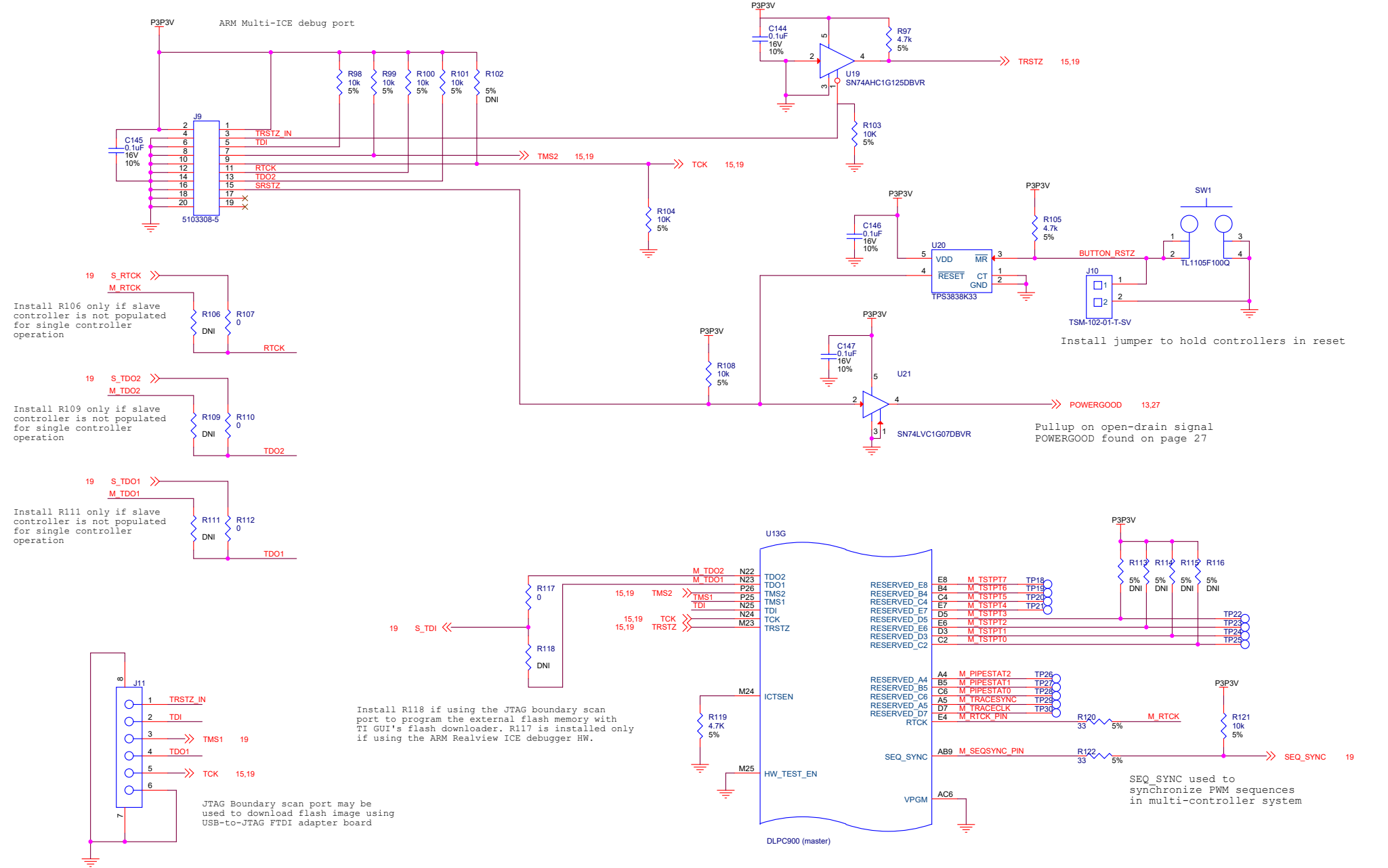
R95 10k 5%

DLPC900 (master)

Master Controller Flash Interface

TI Information
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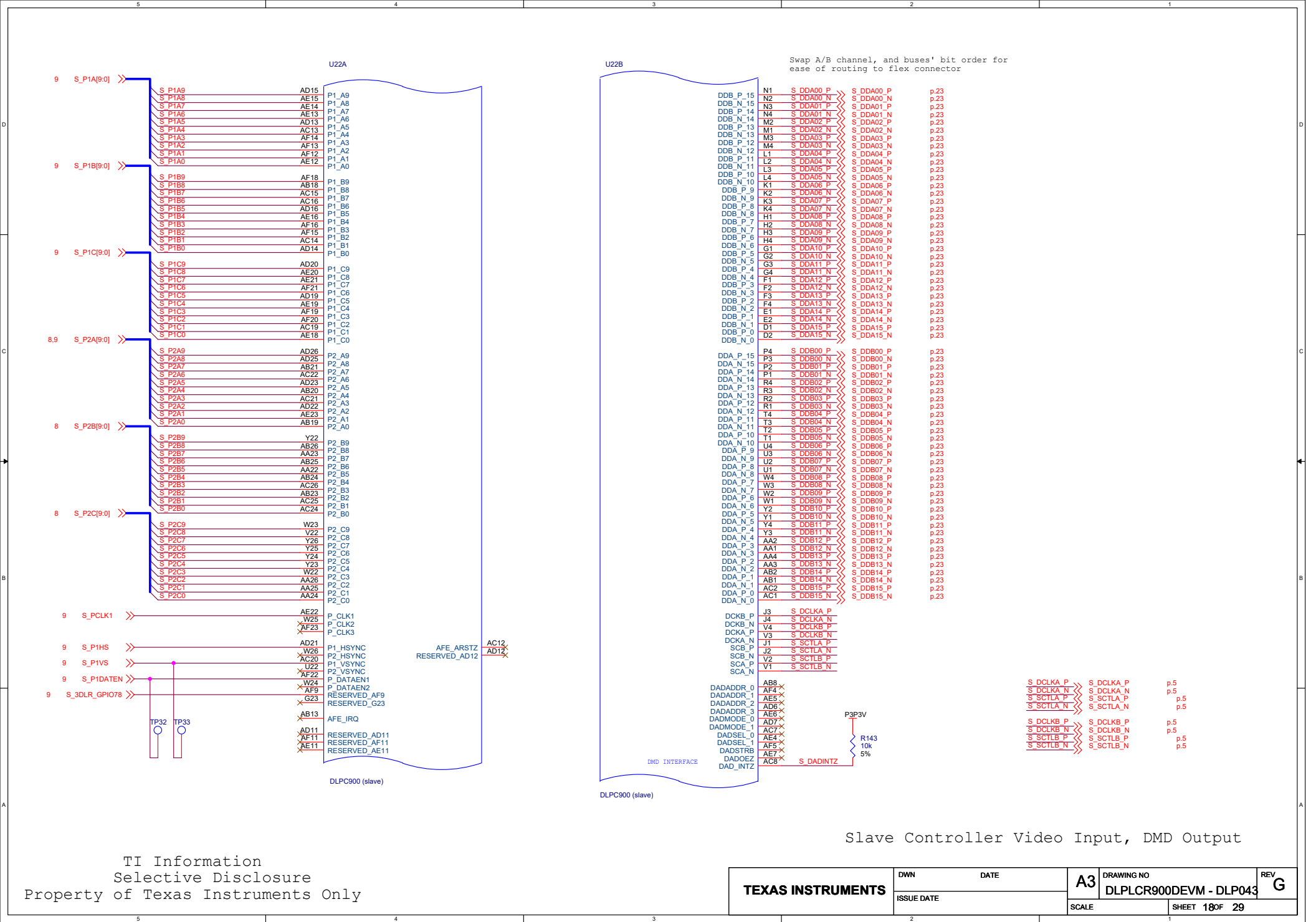
| | | | | | |
|-------------------|------------|------|----|---------------------------------------|----------|
| TEXAS INSTRUMENTS | DWN | DATE | A3 | DRAWING NO DLPLCR9000DEVM - DLP043 | REV G |
| | ISSUE DATE | | | | |
| | SCALE | | | SHEET 14 OF 29 | |

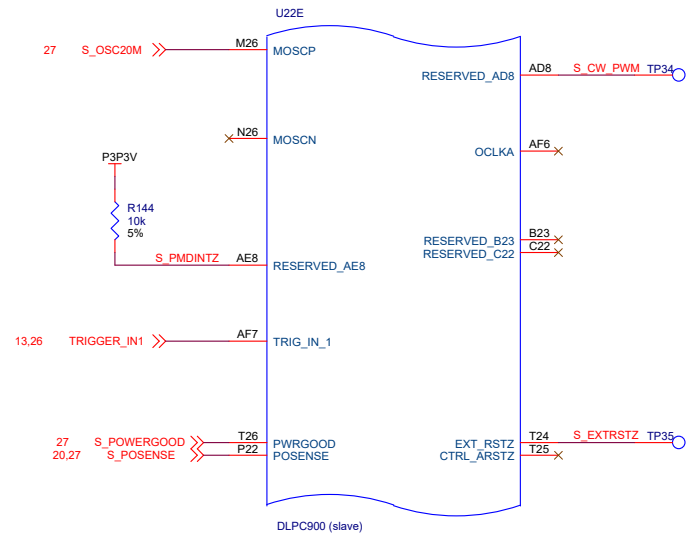
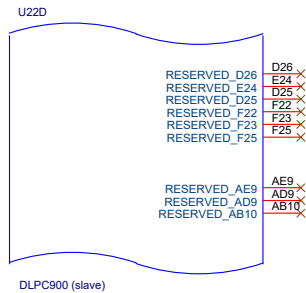


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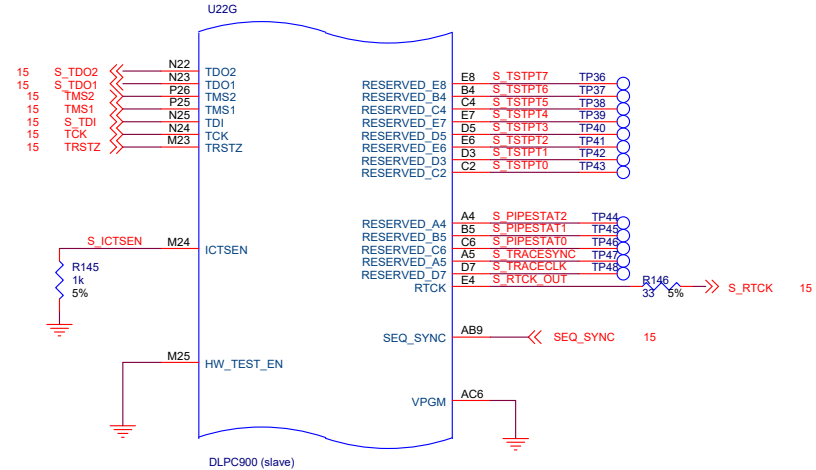
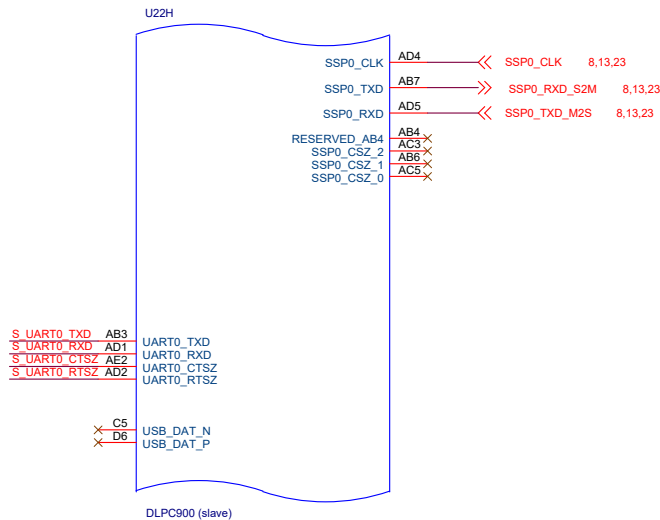
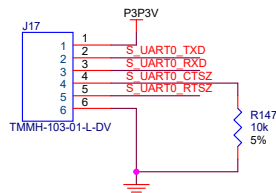
Master Controller Multi-ICE Port

| | | | | | | |
|-------------------|------------|------|----|------------------------|---------------|-----|
| TEXAS INSTRUMENTS | DWN | DATE | A3 | DRAWING NO | | REV |
| | ISSUE DATE | | | DLPLCR900DEVM - DLP043 | | |
| | | | | SCALE | SHEET 15OF 29 | |





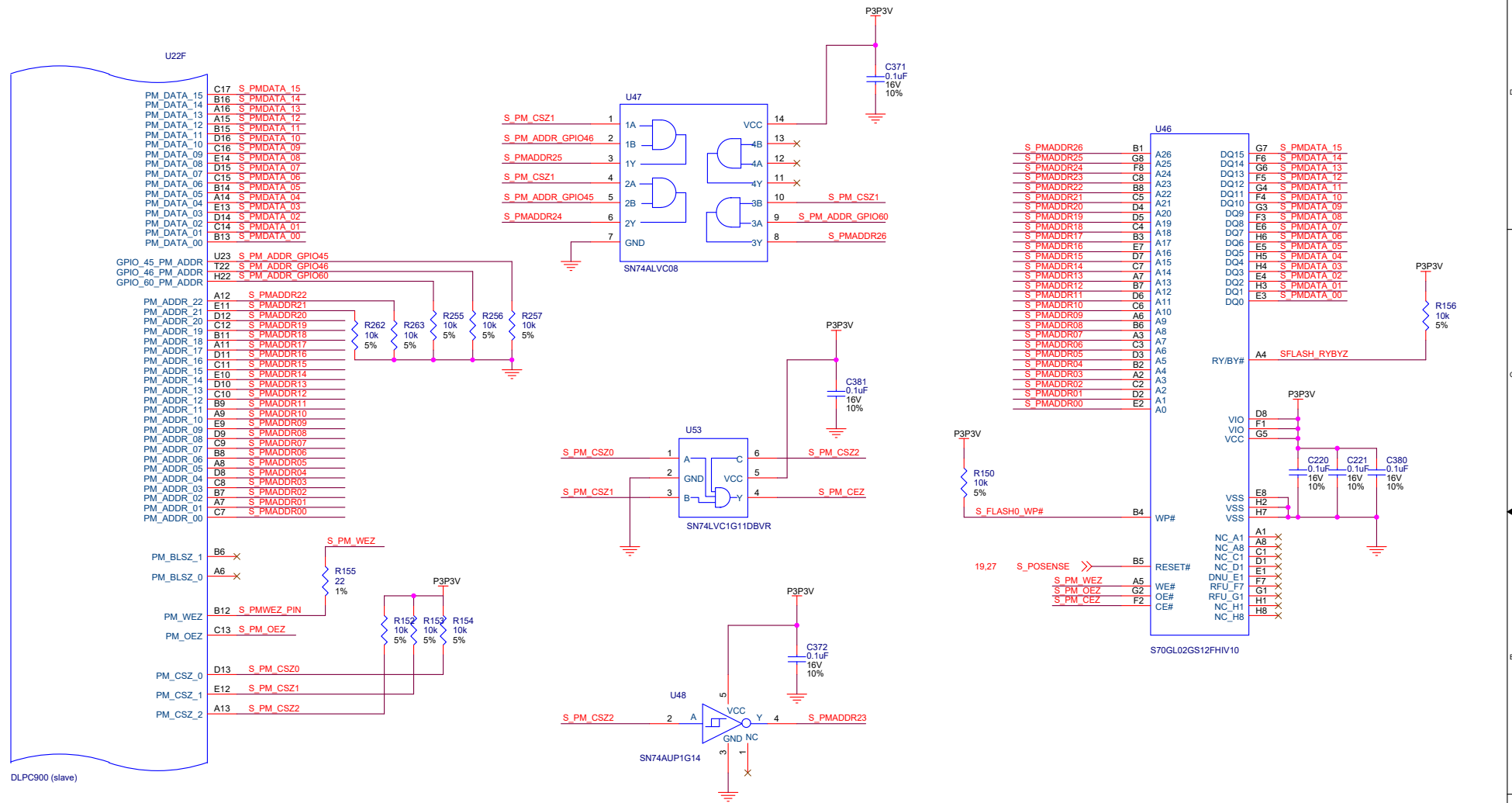
UART debug message port,
not needed for production



Slave Controller Reset, OSC, JTAG, UART0, SSP Port

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| | | | | | | |
|-------------------|------------|------|----|-------------------------|----------|-------|
| TEXAS INSTRUMENTS | DWN | DATE | A3 | DRAWING NO | | REV |
| | ISSUE DATE | | | DLPLCR9000DEVM - DLP043 | | G |
| | | | | SCALE | SHEET 19 | OF 29 |

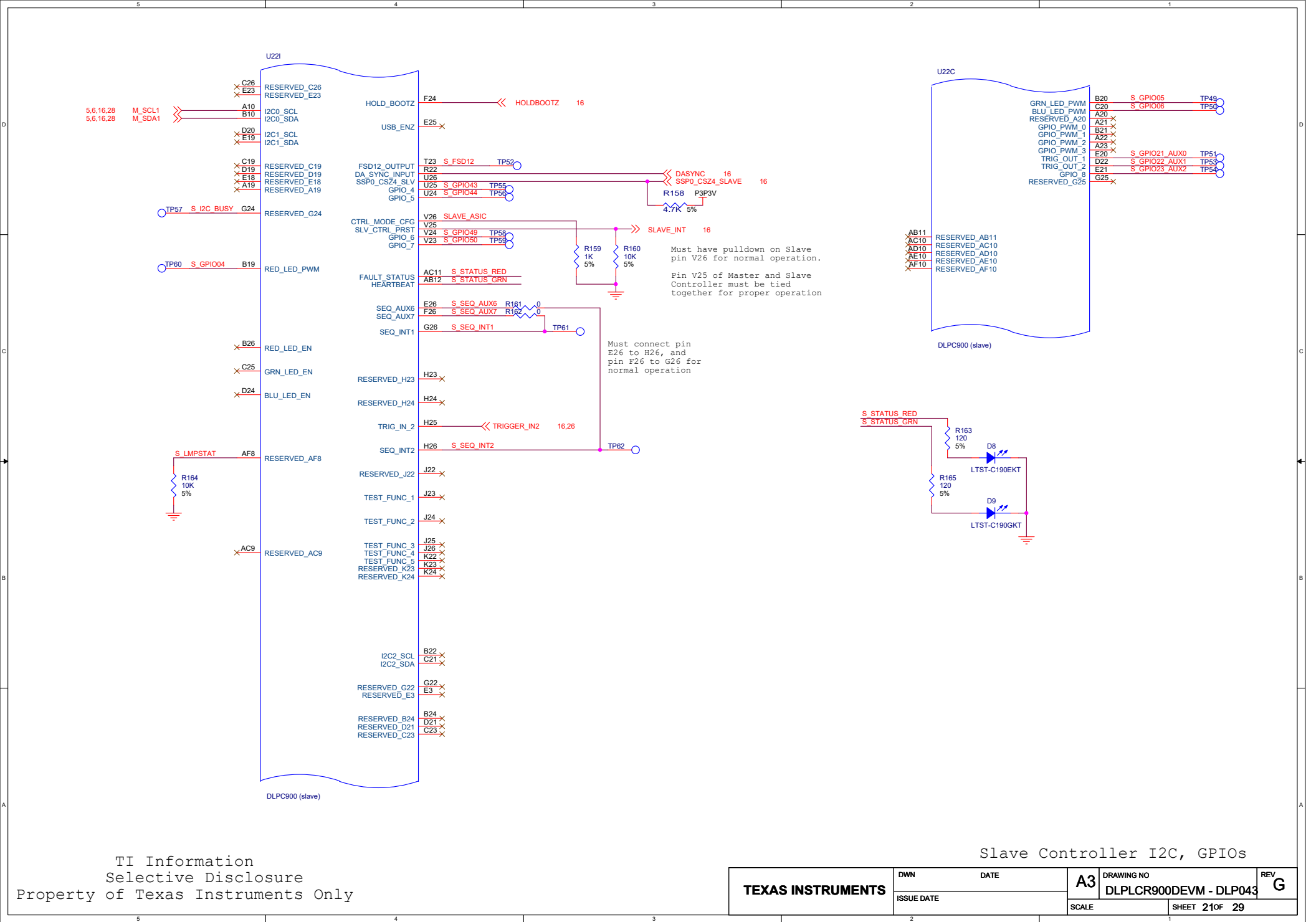


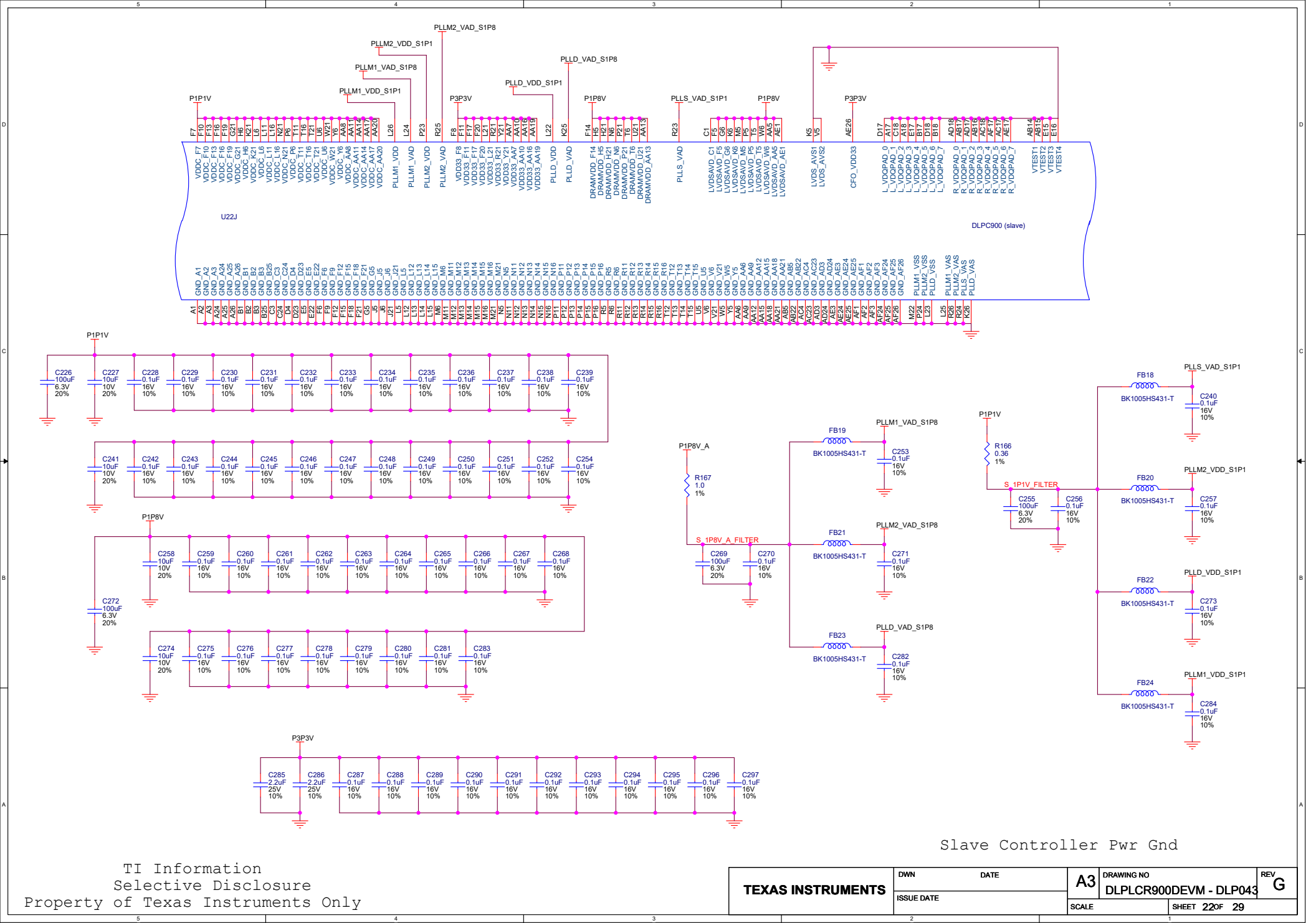
Slave Controller Flash Interface

TI Information
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TEXAS INSTRUMENTS

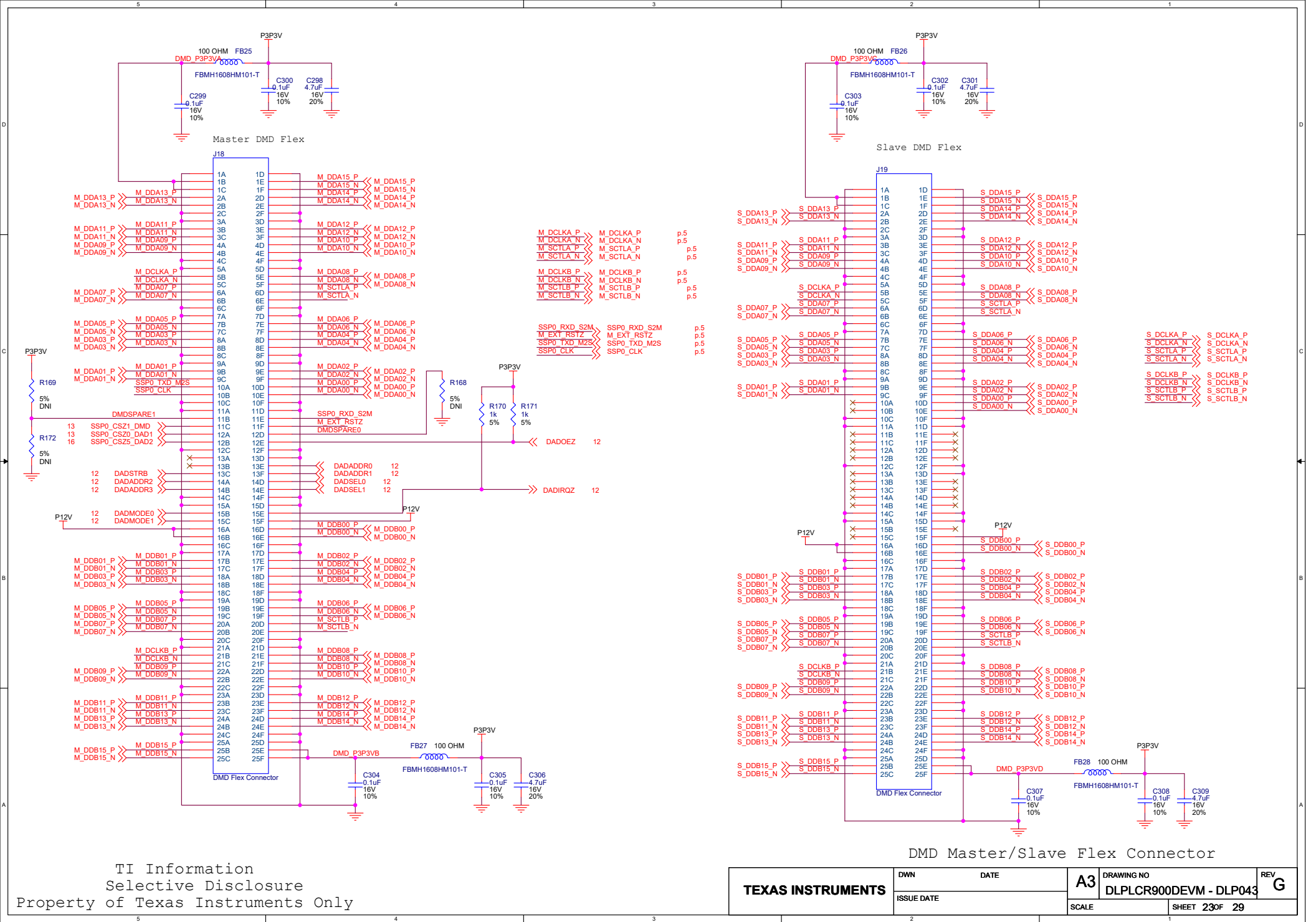
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| DWN | DATE | A3 | DRAWING NO | REV |
| ISSUE DATE | | | DLPLC900DEVN - DLP043 | G |
| SCALE | | | SHEET 20OF 29 | |

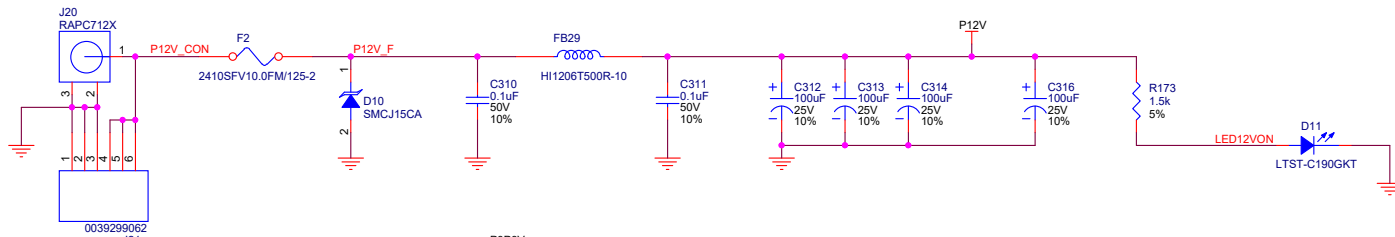




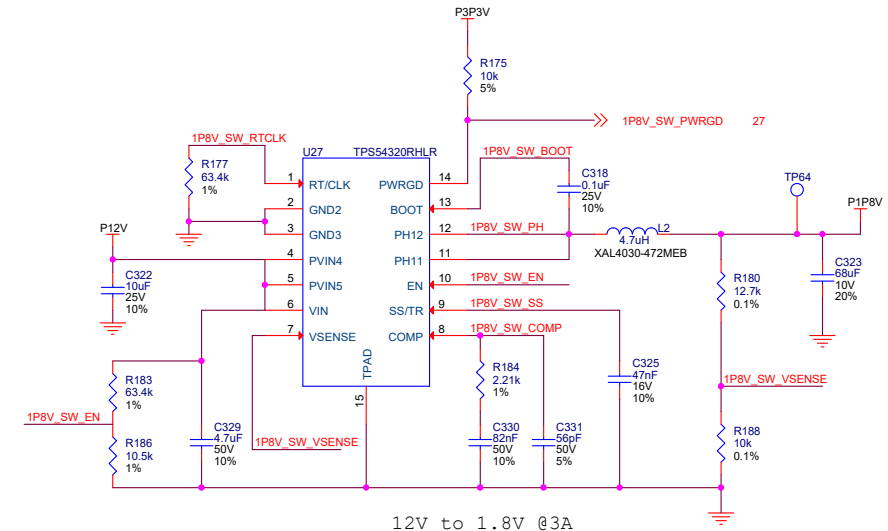
TI Information
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| | | | | | |
|-------------------|------------|------|----|--------------------------------------|----------|
| TEXAS INSTRUMENTS | DWN | DATE | A3 | DRAWING NO DLPLCR900DEVM - DLP043 | REV G |
| | ISSUE DATE | | | | |
| | SCALE | | | SHEET 22OF 29 | |

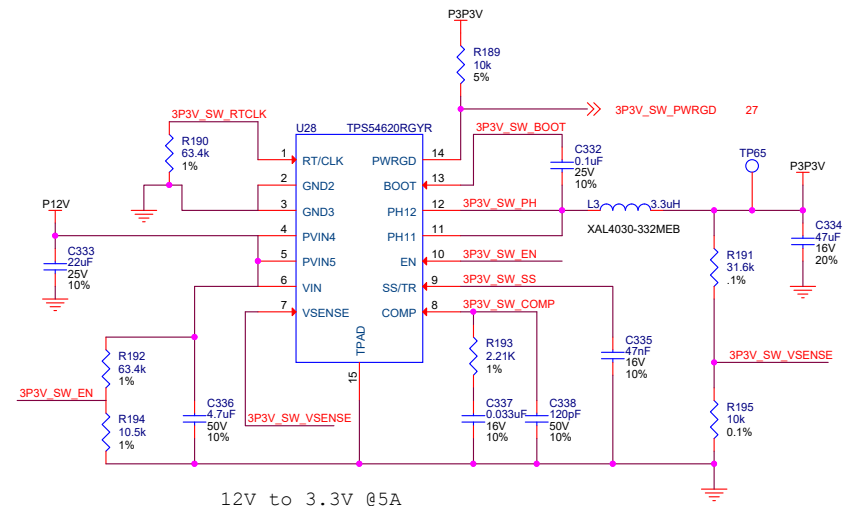




12V to 1.12V @6A
Switching Freq ~ 700KHz
Vstart/stop ~ 6.08V/5.57V
SS ~ 3.5ms



12V to 1.8V @3A
Switching Freq ~ 750KHz
Vstart/stop ~ 8.44V/7.95V
SS ~ 15ms

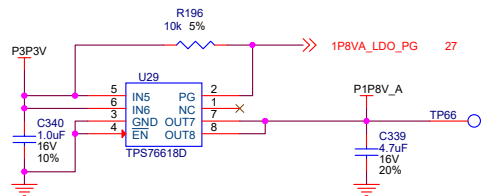


12V to 3.3V @5A
Switching Freq ~ 750KHz
Vstart/stop ~ 8.44V/7.95V
SS ~ 15ms

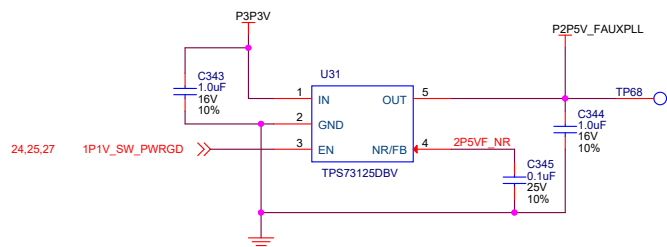
Power Generation 1.1V, 1.8V and 3.3V

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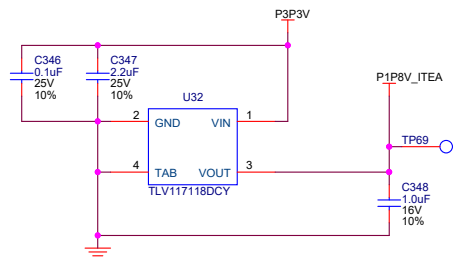
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|-------------------|------------|------------------------|----|------------|----------|
| TEXAS INSTRUMENTS | DWN | DATE | A3 | DRAWING NO | REV |
| | ISSUE DATE | DLPLCR900DEVM - DLP043 | | G | |
| | SCALE | | | SHEET | 24 OF 29 |



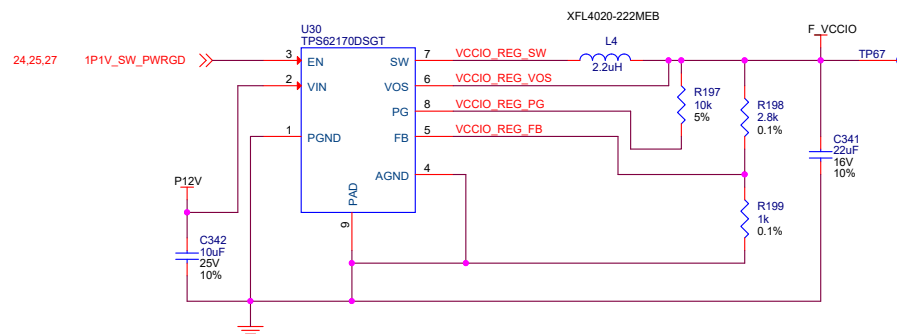
3.3V to 1.8V @250mA LDO
for controller 1.8V analog



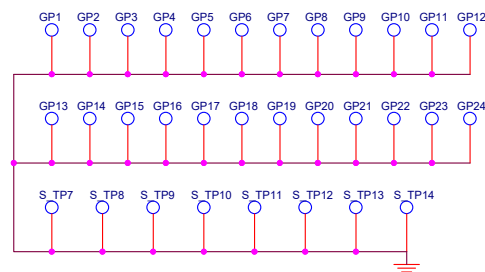
3.3V to 2.5V @150mA LDO
for FPGA 2.5V AUX/PLL power



3.3V to 1.8V @1A LDO
for HDMI Rx 1.8V analog



12V to 3V @500mA
for FPGA Vccio



Distribute ground vias around PCB

Left/Right Split FPGA Power Generation VCCIO, 1.8V & 2.5V LDOs

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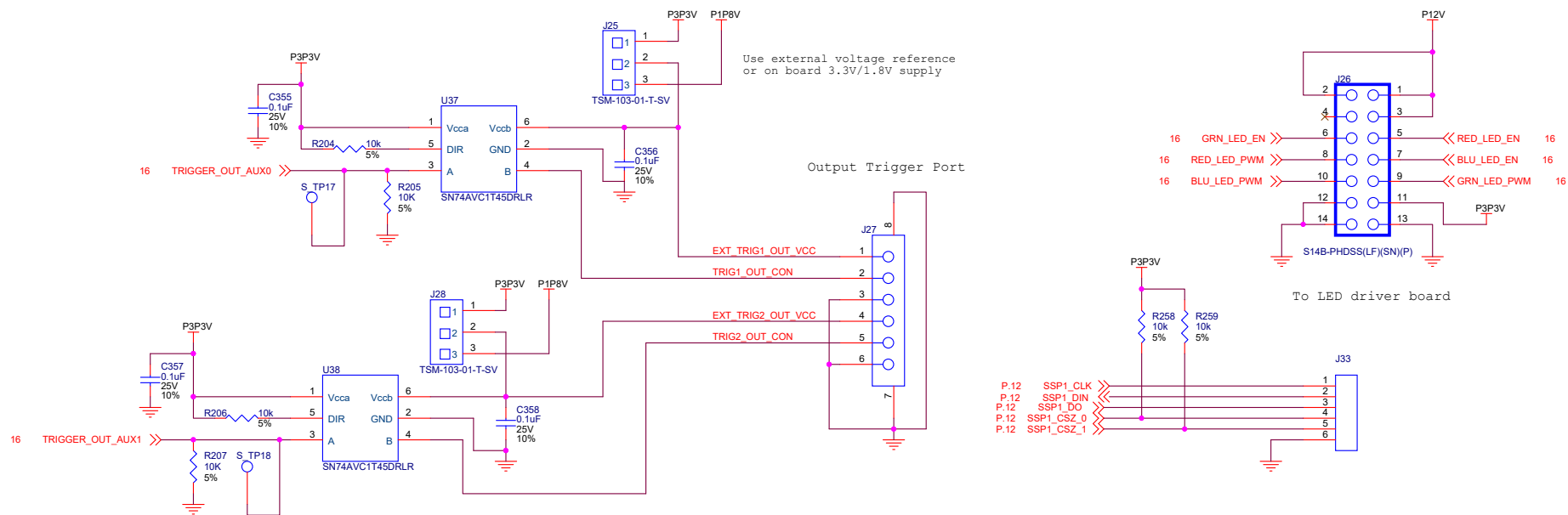
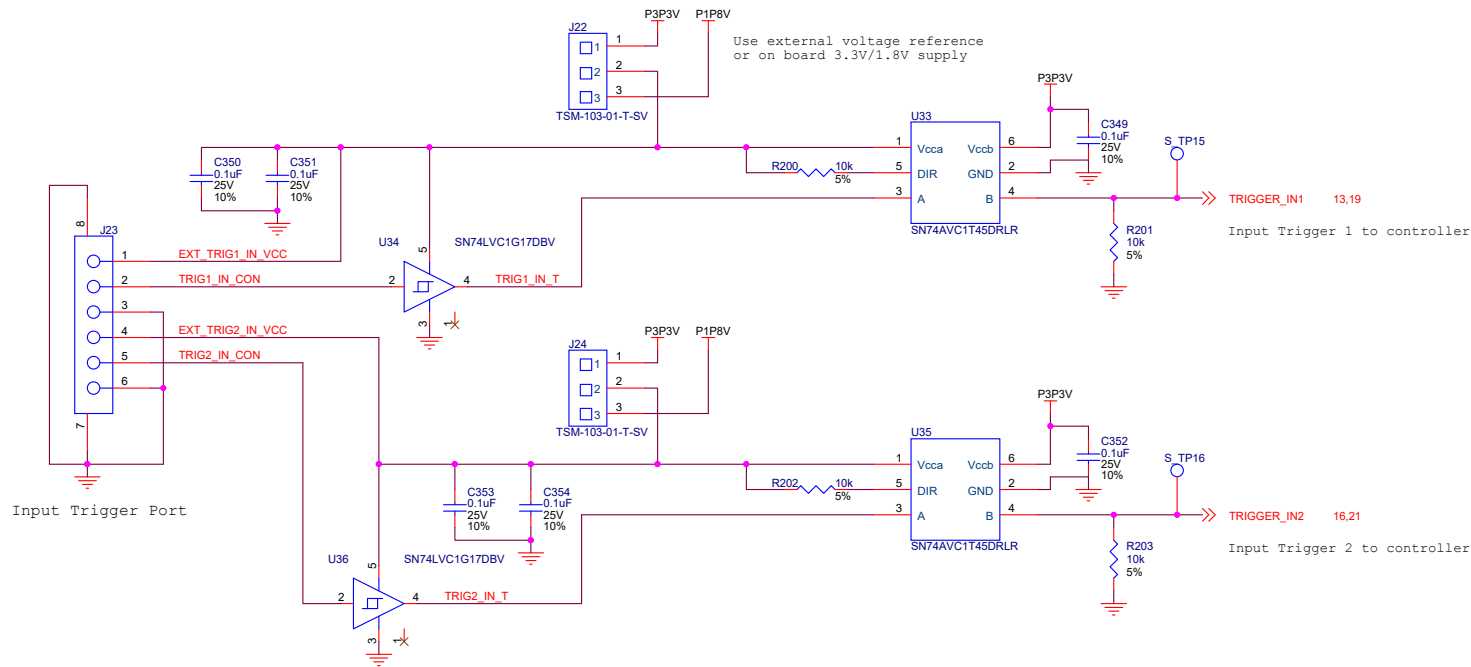
TEXAS INSTRUMENTS

DWN DATE
ISSUE DATE

A3 DRAWING NO
DLPLCR900DEVM - DLP043

REV
G

SCALE SHEET 25 OF 29



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TEXAS INSTRUMENTS

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|------------|------|----|-----------------------|-----|
| DWN | DATE | A3 | DRAWING NO | REV |
| ISSUE DATE | | | DLPLCR900DEV - DLP043 | G |
| SCALE | | | SHEET 26 OF 29 | |

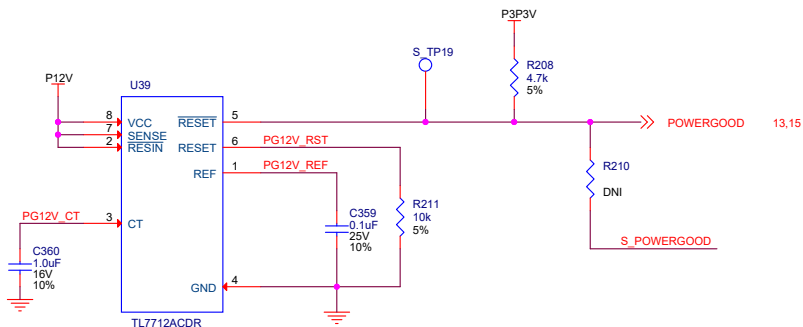
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4

3

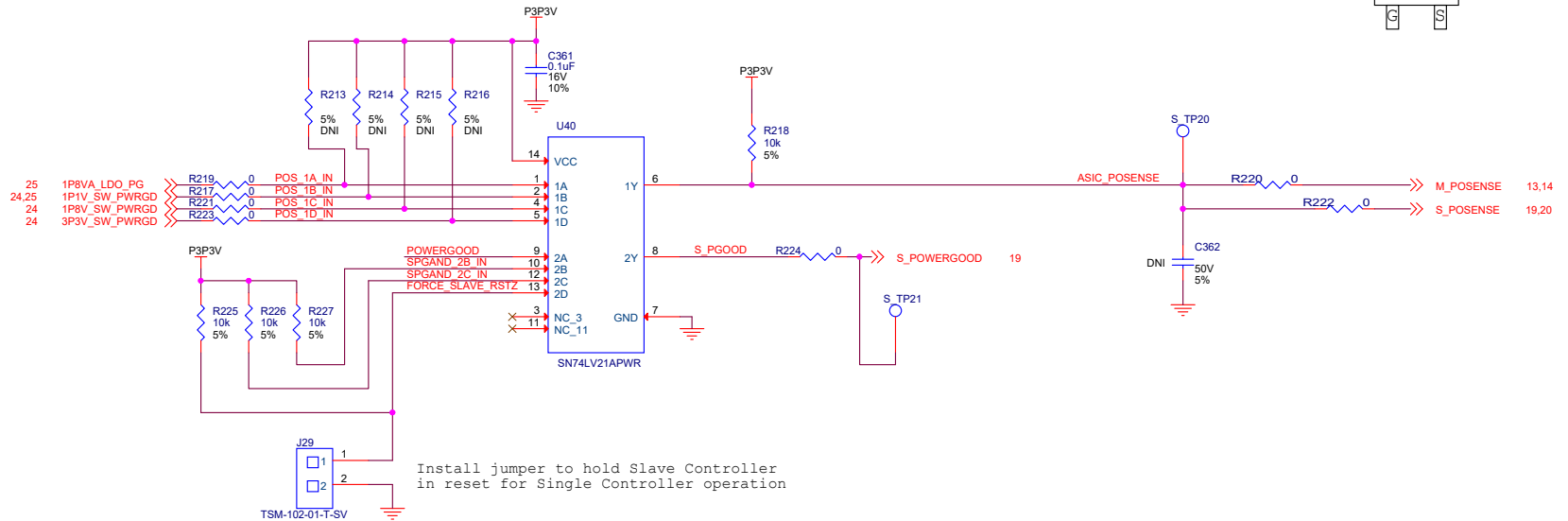
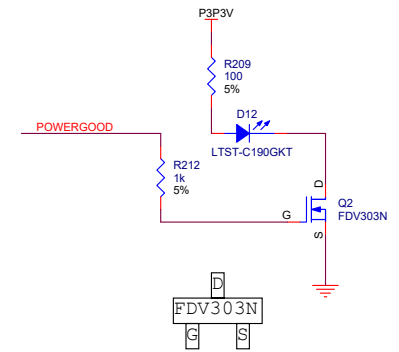
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1

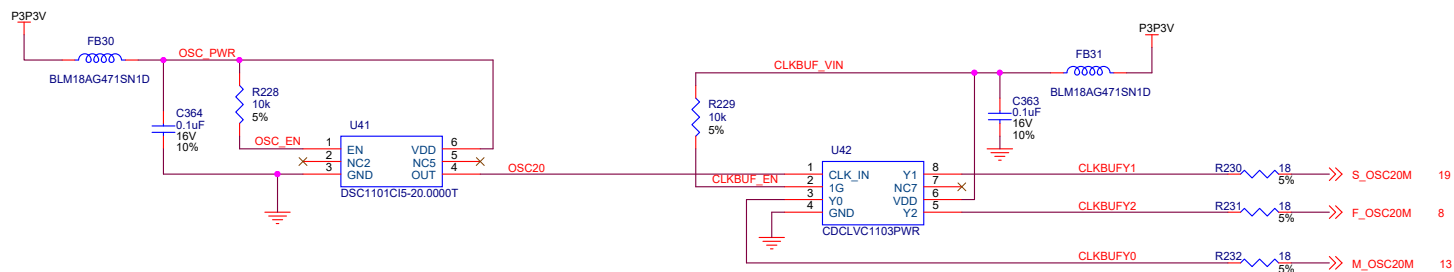


Per controller spec (Fig. 3), POWERGOOD has no impact on operation for 60ms after rising edge of POSENSE. In other words, during power up, controller will ignore the state of PG until the internal PLL is locked (require up to 60ms). Controller will then sample the PG input to begin normal operation.

During power down, POSENSE has to remain valid high for at least 500us after PG is deasserted to allow controller to complete the DMD parking procedure. The 500+ uF input caps on 12V would ensure the power monitor to trip at ~11V to deassert PG while keeping regulators operational to maintain POSENSE for > 500us.



Install jumper to hold Slave Controller in reset for Single Controller operation



Powergood, POSENSE, Controller Clocks

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TEXAS INSTRUMENTS

DWN DATE
 ISSUE DATE

A3 DRAWING NO
 DLPLCR900DEVN - DLP043

REV
 G

SCALE SHEET 27 OF 29

REVISION HISTORY

Rev A

- PAGES - ALL
- initial rev

Rev B

- PAGE 27
- new part for C360
- PAGE 26
- relocated S_TP17 and S_TP18
- PAGE 24
- new part for R179
 - removed C315, bulk cap not needed
- PAGE 25
- new part for L4
- PAGE 10
- new part for U12

Rev C

- PAGES for U13 & U22
- update pin name to match datasheet
- PAGE 15
- add comments for usage of R117 & R118

Rev D

- Remove references to DLPC910

Rev E

- Updated U7

Rev F

- Added External Parallel Video Connector and 5V source
- Sheet 12:
- Added net HDMI_CEC to U13A,G23
- Sheet 28:
- Inserted Parallel Video Connector as Sheet 28. Revisions page moved to Sheet 29.
 - Added U49
 - Added J30, J31, J32
 - Added R233, R234, R235, R236, R237, R238, R239, R240, R241, R249, R250, R251
 - Added RP16, RP17, RP18
 - Added C366, C373, C374, C376, C377
- Increased External Flash Memory to 128 MByte
- Sheet 14:
- Added net M_PM_ADDR_GPIO45 to U13F,U23
 - Added net M_PM_ADDR_GPIO46 to U13F,T22
 - Added net M_PM_ADDR_GPIO60 to U13F, H22
 - Added net BUS_SELECT to U13I,H23
- Sheet 20:
- Added net S_PM_ADDR_GPIO45 to U22F,U23
 - Added net S_PM_ADDR_GPIO45 to U22F,T22
 - Added net S_PM_ADDR_GPIO60 to U22F, H22
- Sheet 14:
- Removed U16, U17, U18
 - Removed R87, R88, R90, R96
 - Removed C140, C141, C142, C143
 - Added U43, U44, U45, U50
 - Added C367, C368, C378, C379
 - Added R252, R253, R254
- Sheet 20:
- Removed U23, U24, U25
 - Removed R148, R149, R151, R157
 - Removed C222, C223, C224, C225
 - Added U46, U47, U48, U53
 - Added C371, C372, C380, C381
 - Added R255, R256, R257
- Added Connector for SSP1 Bus
- Added J33, R258, R259

Rev G

- Sheet 5
- Changed J2 footprint to SMT
- Sheet 10
- U12 changed to Micron MT25QL128ABA1ESE-0SIT
- Sheet 14
- Added R260 and R261
 - Changed net connected to U44 pin 5 to M_PM_ADDR_GPIO45
- Sheet 20
- Added R262 and R263
 - Changed net connected to U48 pin 2 to S_PM_CSZ2