*设计指南：**TIDA-020015***

*用于 **IGBT/SiC** 栅极驱动器且具有功率级的 **4.5V** 至 **65V** 输入、紧凑型偏置电源参考设计*

说明

此参考设计是一个用于 IGBT/SiC 隔离式栅极驱动器的 4.2W、单通道、汽车 12V 电池输入反激式偏置电源。该电源可接受 4.5V 至 65V 直流的宽输入范围。输出可在负载高达 180mA 时配置为 +15V、–8V 或 +20V、–4V，以驱动 IGBT/SiC MOSFET 电源模块。该系统包含反极性保护、电子瞬变钳位以及过压和欠压保护电路。反激式控制器利用优于 ±1% 的负载和线路调节性能，实现了初级侧调节。该功率级设计包括具有 5.7kV$_{RMS}$ 增强型隔离的双通道隔离式栅极驱动器，并采用了 100mm × 62mm 的紧凑外形设计。它包括隔离式直流总线检测、隔离式温度检测、逻辑击穿保护和诊断功能。

资源

TIDA-020015	设计文件夹
TIDA-020014	设计文件夹
LM5180-Q1	产品文件夹
LM74700-Q1	产品文件夹
ISO5852S-Q1	产品文件夹
AMC1311-Q1	产品文件夹
AMC1301-Q1	产品文件夹

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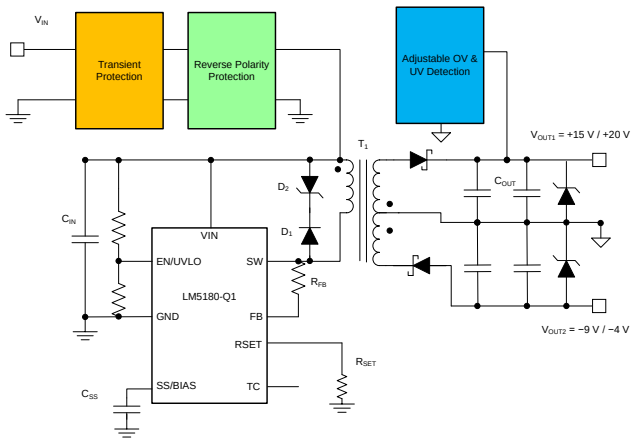
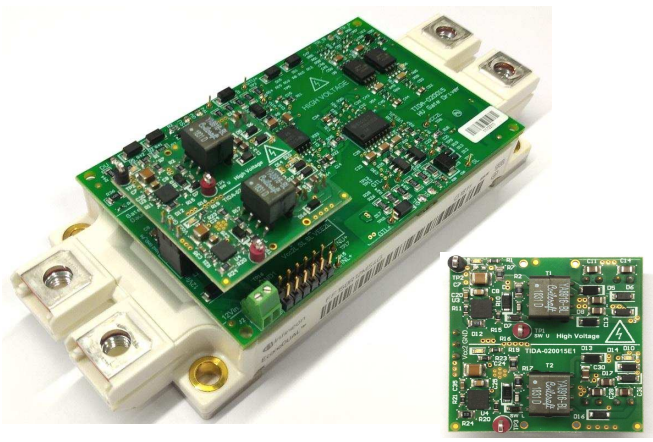
特性

- 输入电压范围为 4.5V 至 65V 直流的宽 V_{IN} 反激式转换器
- 输出可在负载高达 180mA 电源电流时配置为 +15V、–8V 或 +20V、–4V，用于 Si IGBT 和 SiC MOSFET 模块
- 具有用于将高电压传导瞬态钳位至适用于下游电路的安全级别的保护
- 具有对电源输出的可编程过压和欠压保护
- 初级侧调整不需要光耦合器，即可延长使用寿命并缩小外形尺寸
- 功率级设计包括用于高电压测试的双通道隔离式栅极驱动器、直流总线检测和温度检测

应用

- 逆变器和电机控制
- 车载充电器 (OBC) 和无线充电器
- 直流/直流转换器
- 汽油和柴油发动机平台





1 System Description

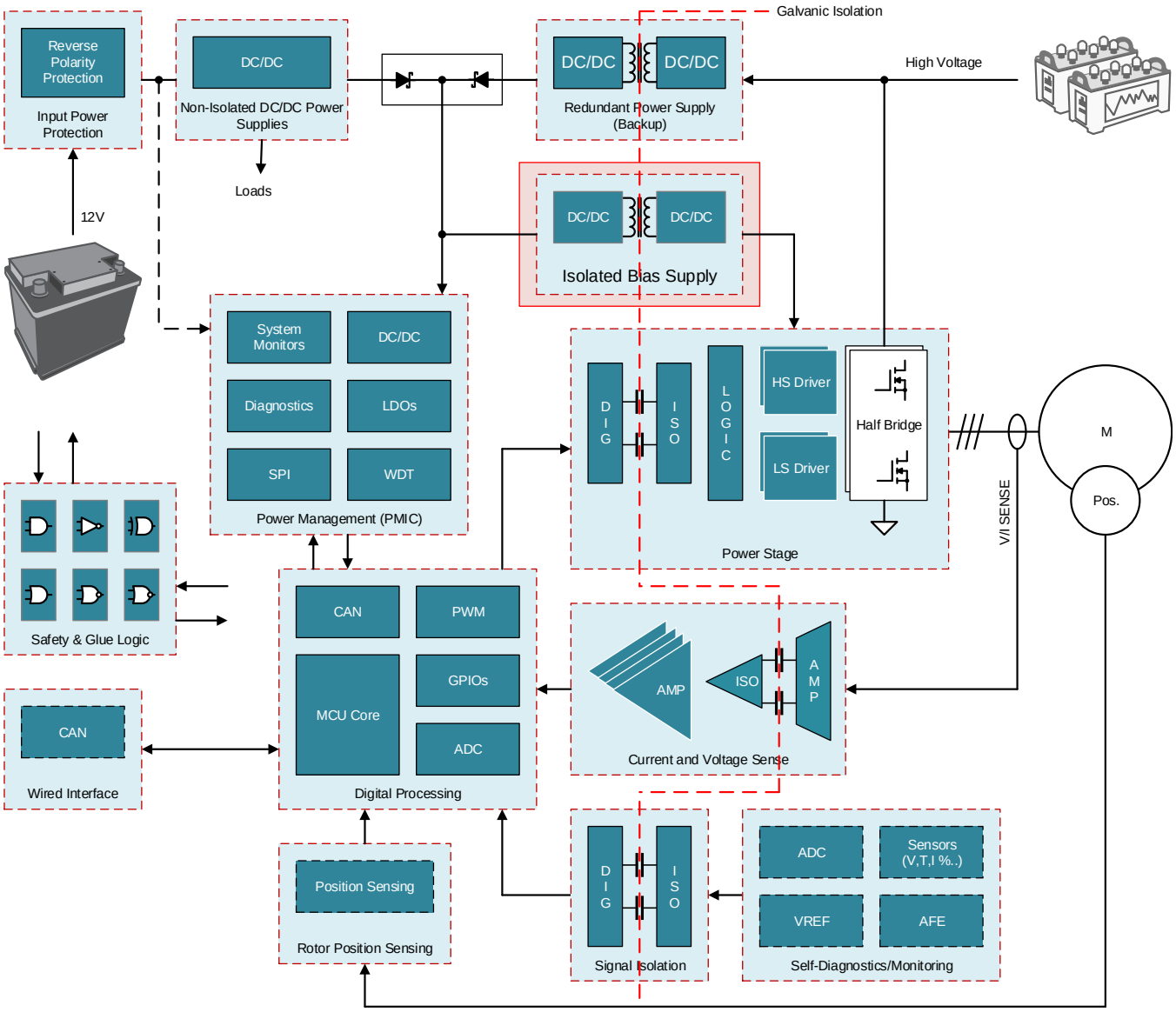
This reference design is a highly-integrated, primary side regulated (PSR) flyback bias supply powering two single channel IGBT/SiC isolated gate drivers. It can be powered directly from the 12-V car battery with a wide input range of 4.5 V to 65 V DC, electric transients suppression, and provides 15-V and –8-V isolated voltage rails with 180-mA maximum output current. The integration of a MOSFET switch, elimination of feedback loop, and elimination of bias winding makes this design very compact and attractive.

The TIDA-020015 targets at powering IGBT/SiC isolated gate drivers implemented in hybrid electric vehicle and electric vehicle (HEV/EV) systems. 图 1 shows a traction inverter reference diagram where the position of the TIDA-020015 design is highlighted. The isolated gate drivers galvanically isolate the high-voltage power switches from the low-voltage control signals. Each isolated gate driver requires a pair of positive supply and negative supply rails to fully turn on and off the IGBT/SIC power modules.

Additionally, the TIDA-0120015 design is able to handle the 12-V battery conditions which include:

- The system maintains a constant output voltage over the full DC range of battery conditions specified in ISO 16750-2:
  - Input V_{IN} (min) down to 3.0 V, (after powered up) simulating a severe cold cranking condition.
  - Input V_{IN} (max) higher than 42 V, simulating the upper range of normal battery operation.
- The system must clamp or filter high-voltage electrical fast transients and maintain operation through them:
  - These pulses include clamped load dump (up to 38 V) and other transients outlined in ISO 7637-2:2004.
- The system must properly respond to a reverse battery polarity event and shut down appropriately.

图 1. HEV, EV Traction Inverter Reference Block Diagram and the TIDA-020015 Position



1.1 Key System Specifications

表 1 shows the key system specifications.

表 1. Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
SYSTEM INPUT						
V_{IN}	Input voltage	Battery voltage range (DC)	4.5	13.5	65	V
V_{CLAMP+}	Positive clamping voltage	Positive input protection TVS clamping range	60		100	V
P_{PK}	Peak pulse power dissipation	Maximum TVS power dissipation		600		W
F_{SW}	Switching frequency		10	350	350	kHz
OUTPUT VOLTAGE						
V_{out1}		System output voltage, across load	13	15	17	V
V_{out2}		System output voltage, across load	–6.5	–8	–8.2	V
OUTPUT CURRENT						
I_{out}		Max output current. Drawing more than 180 mA is not recommended for thermal reasons. See the 节 3.2.8 testing section to see the temperature rise at full load.		180		mA

2 System Overview

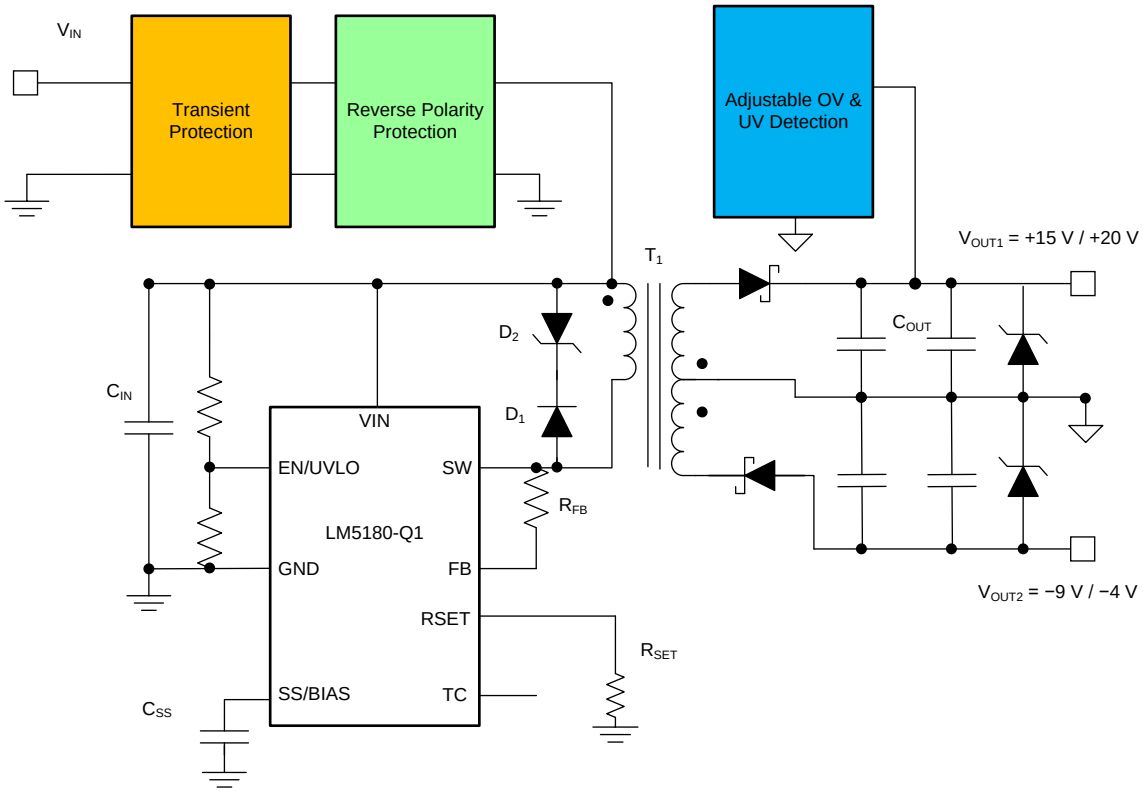
2.1 Block Diagrams

2.1.1 Bias Supply Block Diagram

图 2 shows the TIDA-020015 low-voltage board block diagram. The design consists of 4 main functional elements:

1. The transient protection which suppresses both positive and negative battery pulses as prescribed in ISO 7637-2:2004 pulses 1, 2a, and 3a, 3b.
2. The reverse polarity protection to prevent reverse-biasing components, which are sensitive to polarity, like polarized capacitors and most integrated circuits.
3. The PSR flyback converter which has an integrated MOSFET switch and high-density design with only one component crossing the isolation barrier. The converter maintains high regulation across various loads and achieves larger than 90% peak efficiency.
4. The adjustable overvoltage and undervoltage detection circuit which prevents the gate-driver voltage dropping below the minimum gate voltage to properly turn on the IGBT. Operating the IGBT with a lesser gate voltage causes excessive power dissipation in the IGBT.

图 2. TIDA-020015 Low-Voltage Board Block Diagram

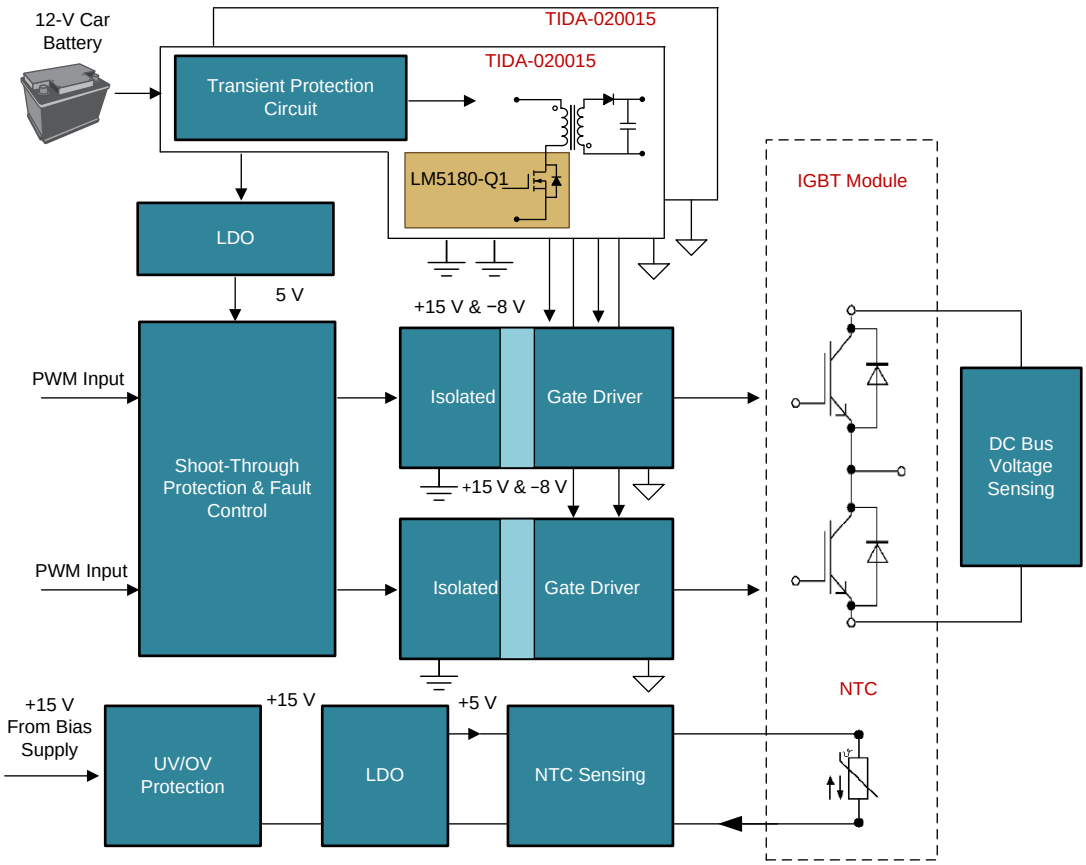


2.1.2 Isolated Gate-Driver Board Block Diagram

The TIDA-020015 design includes a power-stage companion board for high-voltage evaluation. It is a compact, dual-channel isolated gate-driver board providing drive, bias voltages, protection, and diagnostics needed for half-bridge SiC MOSFET and Si IGBT power modules housed in 150-mm × 62-mm × 17-mm packages. The HV board consists of the high-side and low-side isolated gate drivers, the DC bus voltage sensing, the shoot-through protection and fault control, the high-voltage input LDO, and the NTC sensing circuit. The connectors allow for plug-in connection to the gate drivers for easy evaluation. 图 3 shows the power stage board block diagram. The features are listed as follows:

- 20-A peak split sink and source drive current from external buffer to optimize turn on and turn off switching time
- Robust noise-immune solution with CMTI > 100 V/ns
- Supports 5-kV_{RMS}, reinforced isolation for input rail up to 1700 V
- Programmable short-circuit sensing and soft turn-off protection by the de-saturation circuit
- 2-A active Miller clamp
- Output short-circuit clamp
- Fault feedback with reset
- NTC temperature and DC bus voltage sensing

图 3. TIDA-020015 Power Stage Board Block Diagram



2.2 Design Considerations

The TIDA-020015 reference design provides bias power to the SiC or IGBT isolated gate drivers. Gate drivers must provide sufficient drive current to ensure fast charging and discharging of the gate capacitance of the IGBT or SiC transistor, hence to reduce the switching power loss. The gates of the IGBTs are supplied with a much higher voltage than the actual gate-threshold voltages, typically 15 V to 20 V to minimize the turn-on losses. To reduce the turn-off time and the turn-off losses, a negative voltage (–4 V to –9 V) is applied at the gate. A negative voltage also prevents Miller turn on of the switch. This design provides the required drive voltages, and a 4.3-W bias power which is sufficient for most of the high-power IGBT or SiC modules.

2.3 Highlighted Products

The TIDA-020015 reference design features the following TI devices.

2.3.1 LM5180-Q1

The LM5180-Q1 device is a primary-side regulated (PSR) flyback converter with high efficiency over a wide input voltage range of 4.5 V to 65 V. The isolated output voltage is sampled from the primary-side flyback voltage, eliminating the need for an optocoupler, voltage reference, or third winding from the transformer for output voltage regulation. The high level of integration results is a simple, reliable and high-density design with only one component crossing the isolation barrier. Boundary conduction mode (BCM) switching enables a compact magnetic solution and better than ±1% load regulation and line regulation performance. An integrated 100-V power MOSFET provides output power up to 7 W with enhanced headroom for line transients.

2.3.2 LM74700-Q1

The LM74700-Q1 is an ideal diode controller device that operates in conjunction with an external N-channel MOSFET as an ideal diode rectifier for low loss reverse polarity protection. The wide supply input range of 3 to 65 V allows control of many popular DC bus voltages. The device can withstand and protect the loads from negative supply voltages down to –65 V. With a low $R_{DS(on)}$ external N-channel MOSFET, a very low forward voltage drop can be achieved while minimizing the amount of power dissipated in the MOSFET.

2.3.3 TPS3700-Q1

The TPS3700-Q1 is a wide-supply voltage window comparator which operates over a 1.8-V to 18-V range. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for overvoltage and undervoltage detection. The TPS3700-Q1 device can be used as a window comparator or as two independent voltage monitors; the monitored voltage can be set with the use of external resistors.

2.3.4 ISO5852S-Q1

The ISO5852S-Q1 device is a reinforced, isolated gate driver that is capable of driving a 1200-V IGBT module with current ratings from 50 A to 200 A. The device offers:

- High isolation ratings in the industry
  - 5.7 kV_{RMS} isolation voltage
  - 8000 -V_{pk} maximum transient isolation voltage

  - 2121-V_{pk} maximum transient isolation voltage
- Split outputs
- 2.5-A peak source and 5-A peak sink currents
- 100-kV/μs minimum common-mode transient
- The device also includes the Miller clamp, soft turnoff, UVLO, DESAT detect, fault feedback, and ready-status feedback features.

2.3.5 AMC1301-Q1

The AMC1301 is a fully-differential, precision, isolated amplifier. The input stage of the device consists of a fully differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bit stream. The drivers transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains.

2.3.6 AMC1311-Q1

The AMC1311-Q1 is a precision, isolated amplifier with an output separated from the input circuitry by an isolation barrier that is highly resistant to magnetic interference. This barrier is certified to provide reinforced galvanic isolation of up to 7 kV peak according to VDE V 0884-11 and UL1577. Used in conjunction with isolated power supplies, this isolated amplifier separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage. The high-impedance input of the AMC1311-Q1 is optimized for connection to high-voltage resistive dividers or other voltage signal sources with high output resistance.

2.3.7 TPS7B8250-Q1

The TPS7B82-Q1 device is a 40-V_{IN} 300-mA low-dropout linear regulator with ultra-low quiescent current. This voltage regulator consumes only 3 μA of quiescent current at light load, and is quite suitable for the automotive always on application. The device operates with a wide input-voltage range from 3 V to 40 V (45-V load dump protection).

2.4 System Design Theory

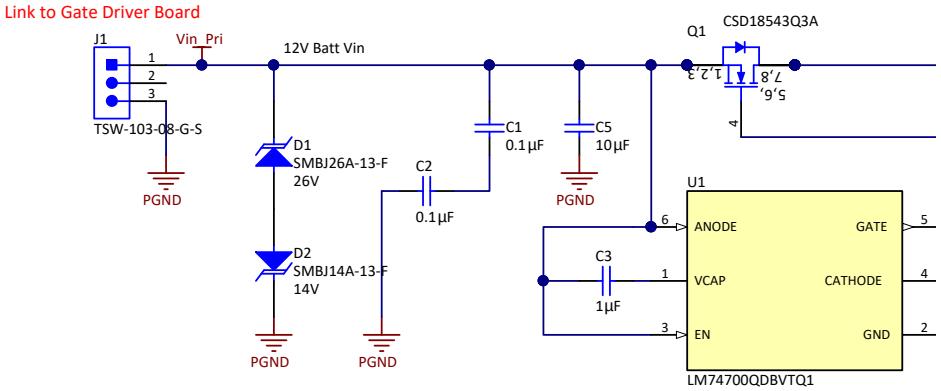
2.4.1 Reverse Polarity Protection

Reverse battery protection is required in every electronic subsystem of a vehicle, both by OEM standards, as well as ISO 16750-2, an international standard pertaining to supply quality. The goal is to prevent reverse-biasing components which are sensitive to polarity, like polarized capacitors and most integrated circuits.

图 4 shows the schematic of the reverse polarity protection circuit. It consists of an N-channel MOSFET (Q3) which is driven by the LM74700-Q1 smart diode controller. Traditional methods which implement a blocking diode result in large power dissipation due to the typical 400- to 700-mV forward voltage drop. The smart diode solution decreases the losses as per the $R_{DS(on)}$ of the MOSFET. The LM74700-Q1 controller provides a gate drive for an external N-channel MOSFET and a fast response internal comparator to discharge the MOSFET gate in the event of reverse polarity. A unique advantage of this scheme is that it is not referenced to ground and thus has Zero I_q. The N-channel MOSFET is selected according to the following criteria:

- Continuous current rating higher than 10 A which is the maximum input current at minimum input voltage in this design
- The V_{GS} threshold should be 2.5 V maximum
- Source-to-drain voltage V_{SD} should be at least 0.48 V at 2 A

图 4. Reverse Polarity Protection Circuit Schematic



2.4.2 Electrical Transient Protection

TVS diodes are implemented on the supply input of the system to protect against both positive and negative electrical transients as prescribed in ISO 7637-2:2004 pulses 1, 2a, and 3a, 3b. OEM specifications will define a “class of operation” for each test which defines the required operational status during and after the event. The TVS diodes are placed aiming at shut the transients while maintaining the downstream circuits operation.

The TVS diode is selected based on the following criteria:

- The diode breakdown voltage is lower than the breakdown voltage of the downstream circuits.
- The positive clamping voltage is above twice of the input battery voltage (for jump start) and clamped load dump voltages.
- The negative clamping voltage is slightly lower than the battery voltage in reverse connection so that it will clamp all negative voltages while it does not create short circuit during a reverse battery condition.
- The power rating of the TVS diode is higher than the power dissipation during the transient clamping.

The important parameters for calculating the TVS diode power rating are: the clamping voltage, the voltage of the pulse it is clamping, and the source impedance of the pulse. One severe scenario according to the ISO7637 pulse 2a standard is:

- V_{Pulse} = 75 V
- R_{Source} = 4 Ω
- V_{Clamp} = 33 V

  where:

  - V_{Pulse} is the voltage of the pulse that TVS diode is clamping
  - R_{Source} is the source impedance of the pulse
  - V_{Clamp} is the clamping voltage from TVS diode

The worst-case assumption is that the load is drawing zero current and all the current flows through the TVS diode. Thus, the power rating of the diode is calculated as:

$$P_{TVS} = \frac{V_{Pulse} - V_{Clamp}}{R_{source}} \times V_{clamp} = 346.5\ W \quad (1)$$

Two SMB-sized TVS diodes with 600-W peak power rating are selected for positive and negative clamping respectively for the design. For detailed testing results and waveforms, see the *Automotive Wide V_{IN} Front-End Power Reference Design w/Cold Crank Operation and Transient Protection* reference design.

2.4.3 LM5180-Q1 Flyback Converter

The bias supply solution 1 is the flyback converter based on the LM5180-Q1 device which has integrated MOSFET and internal compensation. The converter provides isolated output voltages with tight regulation crossing load. 表 2 shows the design specifications. Highlights of the converter are summarized as:

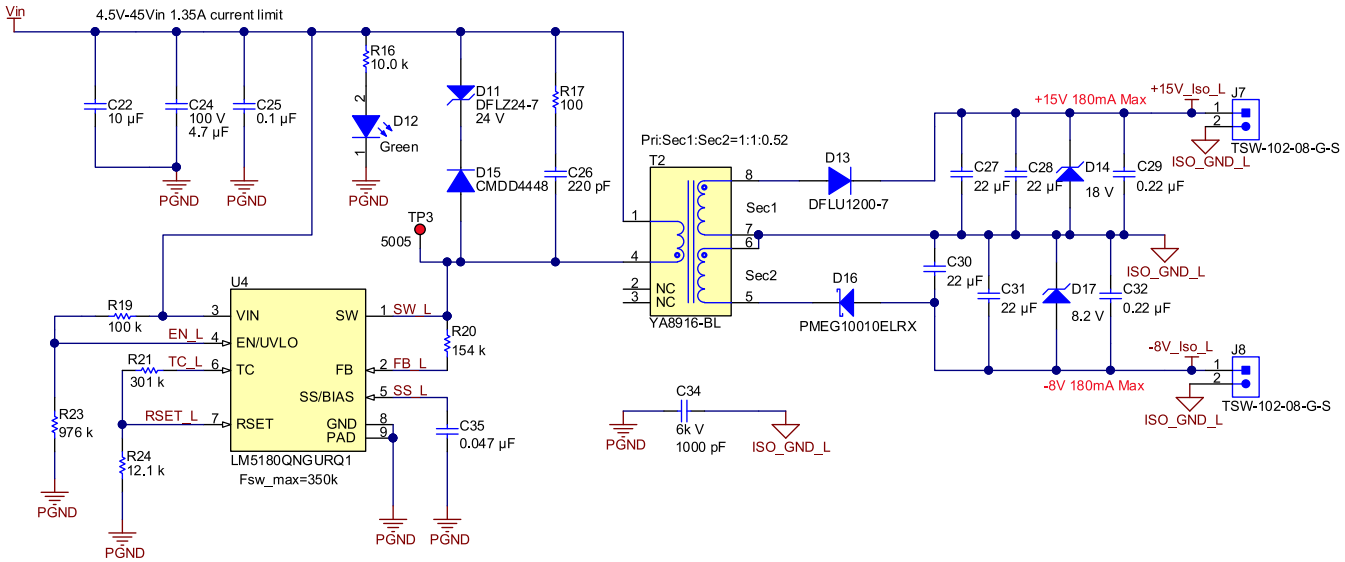
- Boundary conduction mode (BCM) control architecture provides fast line and load transient response
  - Peak current-mode control
  - Quasi-resonant switching for reduced power loss
  - Internal loop compensation
- Integrated 100-V flyback power MOSFET
  - Provides large headroom for input voltage transients
- Cycle-by-cycle overcurrent protection (OCP)
- Low transformer primary-to-secondary (inter-winding) capacitance to accommodate high dv/dt secondary-side common-mode swings.

图 5 shows the schematic of the converter.

表 2. Flyback Converter Specifications

PARAMETER	SPECIFICATION
Input voltage (V_{IN})	4.5 V–65 V DC (for flyback converter only, TVS limits the system input to 26 V DC)
Output voltage (V_{OUT})	+15 V, –9 V
Output ripple	±3%
Maximum output current (I_{out_max})	180 mA
Switching frequency	< 350 kHz
Output power (P_{out_max})	4.2 W
Efficiency	> 86% peak, 82% at full load

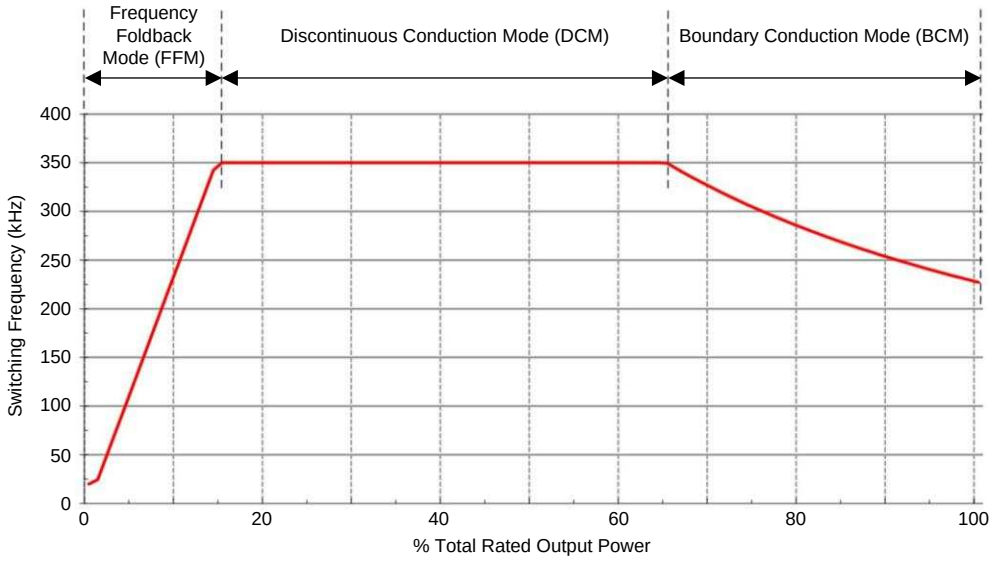
图 5. LM5180-Q1 Based Flyback Converter Schematic



2.4.3.1 Modes of Operation and Switching Frequency

The LM5180-Q1 device uses a variable-frequency, peak current-mode (VFPCM) control architecture with three possible modes of operation as 图 6 illustrates.

图 6. LM5180-Q1 Flyback Converter Operation Mode



At high loads, the LM5180-Q1 device operates in quasi-resonant boundary conduction mode. The power MOSFET turns on when the current in the secondary winding reaches zero. The MOSFET turns off when the peak primary current reaches the level dictated by the output of the internal error amplifier. As the load is decreased, the peak current decreases and the frequency increases to maintain BCM operation.

2.4.3.2 Transformer Design

Key parameters to design the transformer include turns ratio, primary side inductance, switching frequency, saturation current and so forth.

If ignoring the drop voltage across the switching MOSFET, the winding turns ratio is calculated as:

$$V_{IN\_Min} \times T_{on} = (V_{OUT} + V_D) \times T_{off} \times N_{PS} \quad (2)$$

where

- V_{IN_Min} is the minimum input voltage
- T_{on} is the switch-on time of the switching MOSFET
- T_{off} is the off time of the switching MOSFET
- N_{PS} is the turns ratio of the transformer
- V_D is the output rectification diode

Considering $D = \frac{T_{on}}{T_{on} + T_{off}}$ is the duty cycle, and choosing the maximum duty cycle 75% at minimum input voltage, the turns ratio of the transformer primary winding to the secondary winding is calculated as:

$$N_{PS} = \frac{V_{IN\_Min}}{V_{OUT} + V_D} \times \frac{D}{1-D} = 0.65 \quad (3)$$

Select a magnetizing inductance based on the minimum off-time constraint according to:

$$L_{MAG} \geq \frac{(V_{OUT} + V_D) \times N_{PS} \times t_{OFF\_MIN}}{I_{PRI\_PK}} = 26.5\ \mu H$$

where

- V_D is the forward drop voltage of the output rectification diode

- I_{PRI_PK} is the primary winding current when converter operates in frequency fold back mode (1.5 A according to the datasheet) (4)

The built-in MOSFET of LM5180-Q1 is rated at 100 V. In the off cycle, when the secondary (flyback) diode is on, the voltage on the drain (V_{DS}) is calculated as:

$$V_{DS} = V_{IN(MAX)} + V_{REF} + V_{RING} = 82 \text{ V}$$

where

- $V_{IN(MAX)}$ is the maximum input voltage
- I_{REF} is the voltage reflected from the secondary side
- V_{RING} is the excited spike due to resonance (5)

The voltage across the secondary side diode is calculated as:

$$V_{Diode} = V_{OUT} + \frac{V_{IN(MAX)}}{N_{PS}} + V_{SPIKE} = 112 \text{ V}$$

where

- V_{OUT} is the maximum output voltage
- V_{SPIKE} is the excited spike due to resonance (6)

The inductance of the transformer primarily determines the modes of operation in the LM5180-Q1 as the load is varied from the minimum load to full load. An increase in the magnetic inductance generally leads to an increase in the leakage inductance of the transformer. The LM5180-Q1 has a minimum off-time ($T_{OFF(MIN)}$) of 500 ns: the magnetizing current should not decrease to zero in less than 500 ns. Therefore, the minimum primary side inductance is calculated as:

$$L_{PRI} \geq \frac{\left(V_{out} + V_{FWD}\right) \cdot T_{OFF(MIN)} \cdot N_{PS}^2}{I_{PRI\_MIN} \cdot N_{PS}} = 30 \ \ \mu\text{H}$$

where

- V_{OUT} is the nominal output voltage which is 24 V
- $T_{OFF(MIN)}$ is the minimum off time of LM5180-Q1
- I_{PRI_MIN} is the minimum peak current flowing at primary side for the LM5180-Q1 which is 0.27 A
- N_{PS} is the primary to secondary turns ratio (7)

Thus, the designed transformer should have the minimum primary inductance of 30 µH. Specifications of the designed flyback transformer are summarized in 表 3.

表 3. Flyback Transformer Specifications

PARAMETER		SPECIFICATION
Power rating		4.2 W
Input voltage		4.5 V–65 V
Maximum output current (I_{out_max})		180 mA
Switching frequency		< 300 kHz
Maximum duty cycle		75%
Primary side inductance		30 µH ±10% at 300 kHz
Leakage inductance		< 1% of primary inductance
Parasitic capacitance primary to secondary		< 20 pF
Output voltage and current		+15 V and –9 V at 180-mA average current
Turns ratio		1:1:0.52
Peak current	Primary	1.45 A
	Secondary	1 A
RMS current	Primary	1.1 A
	Secondary	380 mA

TI recommends the flyback transformer UA8916-BL from Coilcraft® for this reference design. The transformer features parasitic capacitance of 17 pF from primary to secondary side.

2.4.3.3 Input Capacitors

The input capacitor must supply the input current during the input voltage dip from the 12-V battery. Input capacitors are essential in limiting the ripple voltage while supplying most of the switch current during the MOSFET switch on-time.

The input capacitance is calculated as:

$$C_{in} = \frac{I_{pri\_pk} \times D_{on}}{F_{SW} \times \Delta V_{ripple}} = \frac{1.45A \times 0.75}{300k \times 4.5V \times 3\%} = 26.8\ \mu F \quad (8)$$

2.4.3.4 Output Capacitors

The output capacitance ensures the converter has a small transient deviation to a step change of the load transient. The minimum needed capacitance is calculated as to maintain the output voltage drop less than 3% of the nominal voltage when the output current changes abruptly from the maximum to half (I_{step}):

$$I_{step} = \frac{I_{OUT}}{2} = \frac{180\ mA}{2} = 90\ \ mA \quad (9)$$

$$V_{drop} = V_{OUT} \times 3\% = 24V \times 1\% = 0.24\ V \quad (10)$$

As any forward converters, the right-half-plan-zero (RHPZ) limits the bandwidth of the flyback. The frequency of the RHPZ is calculated as:

$$f_{RHPZ} = \frac{R_{OUT} \times (V_{IN} / V_{OUT})^2}{L_{PRI} \times 2\pi} = 24.8\ kHz$$

where

- R_{OUT} is the load impedance
- L_{PRI} is the primary inductance of the transformer (11)

The bandwidth of the system is estimated as 1/5 of the RHPZ:

$$f_{bandwidth} = \frac{1}{5} \times f_{RHPZ} = \frac{1}{5} \times 24.8\ kHz = 4.96\ kHz \quad (12)$$

As the result, the output capacitance at bandwidth frequency is calculated as:

$$C_{out\_min} = \frac{1}{2 \times \pi \times f_{bandwidth}} \times \frac{1}{\Delta V_{OUT} / \Delta I_{loadstep} - ESR_{OUT}} = 12\ \ \mu F \quad (13)$$

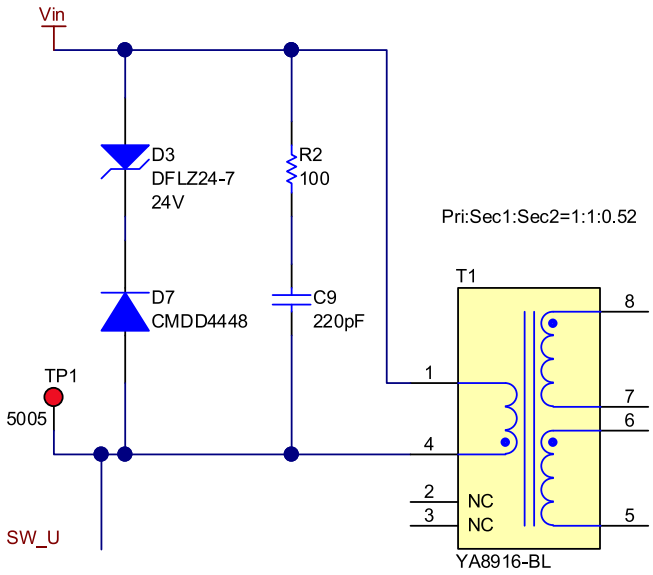
Therefore, a minimum of 12-µF capacitance is required for this design.

2.4.3.5 RC Snubber Design

When the MOSFET turns off, a high voltage spike occurs at the drain (switch node) because of the resonances between leakage inductor of the main transformer and the parasitic capacitance in the circuit. This causes excessive voltage on the drain of the MOSFET which can lead to breakdown and eventually failure of the device. The parasitic capacitance is composed of 3 components: (1) output capacitance of the MOSFET, (2) junction capacitance of the output diode which reflects to the primary side, (3) parasitic capacitance of the transformer winding.

The transformer used in this design has relatively less leakage inductance. A Zener clamp is used in this reference design as 图 7 shows, due to ease-of-design and higher light-load efficiency than the RCD snubber:

图 7. Snubber Circuit Schematic



The power dissipated in the snubber can be calculated as:

$$P_{sub} = \frac{1/2 \times L_{LK} \times I_{PK}^2 \times F_{SW}}{1 - V_{FBK}/V_{Ze}}$$

where

- L_{LK} is the leakage inductance of the transformer
- I_{PK} is the primary peak current
- F_{SW} is the switching frequency
- The Zener diode is selected as 24 V (14)

2.4.3.6 Verification on Input Voltage Range

The LM5180-Q1 device integrates a 100-V power MOSFET with maximum current of 1.5 A. The maximum drain-to-source voltage (V_{ds_max}) is calculated as:

$$V_{ds\_max} = n \times \frac{N_p}{N_s} \times (V_{OUT} + V_f) + V_{in\_max} = 102.5 \text{ V}$$

where

- n is the safe margin which is normally 1.5 or 2 times of the nominal value
- N_p/N_s is the turn ratio of the transformer primary winding to the secondary winding
- V_{out} is the output voltage
- V_f is the forward voltage of the output diode
- V_{in_max} is the maximum input voltage (15)

Therefore, the selected MOSFET breaking voltage larger must be larger than 102.5 V.

2.4.3.7 LM5180-Q1 Settings

图 8 shows the schematic with components surrounding the LM5180-Q1 device. The UVLO is connected to V_{IN} directly for lowest undervoltage lockout. With the designed turns ratio of the transformer and forward voltage of the secondary diode, the ratio between R20 (R_{FB}) and R24 (R_{RST}) determines the output voltage. R24 (R_{RST}) is selected as 12.1 kΩ according to data sheet. The output voltage is 24 V, the forward voltage drop of the secondary diode is 0.7 V. R_{FB} is calculated as:

$$R_{FB} = \frac{(V_{OUT} + V_{FD}) \times N_{PS}}{0.1 \text{ mA}} = 154 \text{ kΩ}$$ (16)

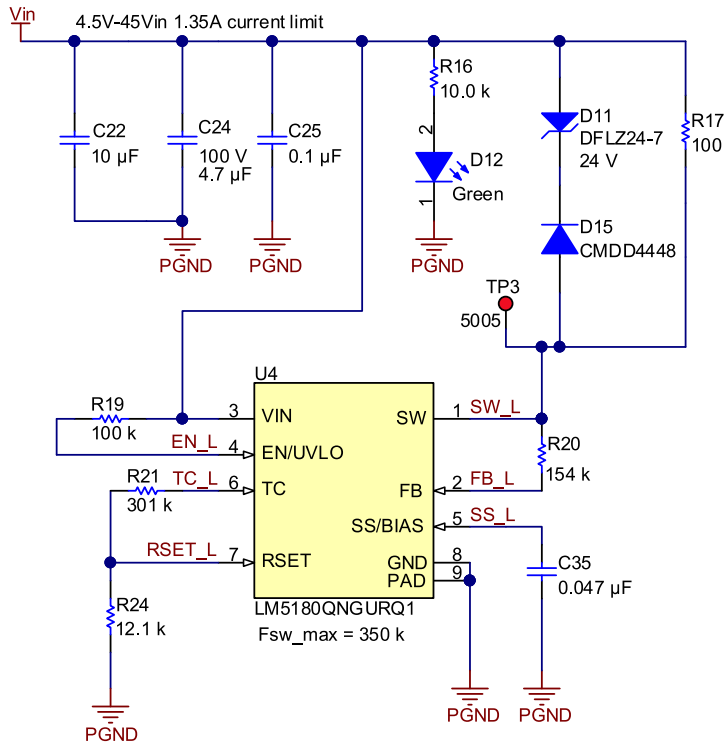
The LM5180-Q1 device employs a thermal-compensation circuit that adjusts the feedback reference based on the forward voltage thermal coefficient of the flyback diode. The thermal compensation resistor value is determined by R21 (R_{TC}) which is calculated as:

$$R_{TC} = \frac{R_{FB}}{N_{PS}} \times \frac{3\ mV/°C}{TC_{Diode}} = 301\ \ k\Omega \quad (17)$$

where

- TC_{Diode} is the absolute value of the temperature coefficient of the flyback diode

图 **8. LM5180-Q1 Settings Schematic**

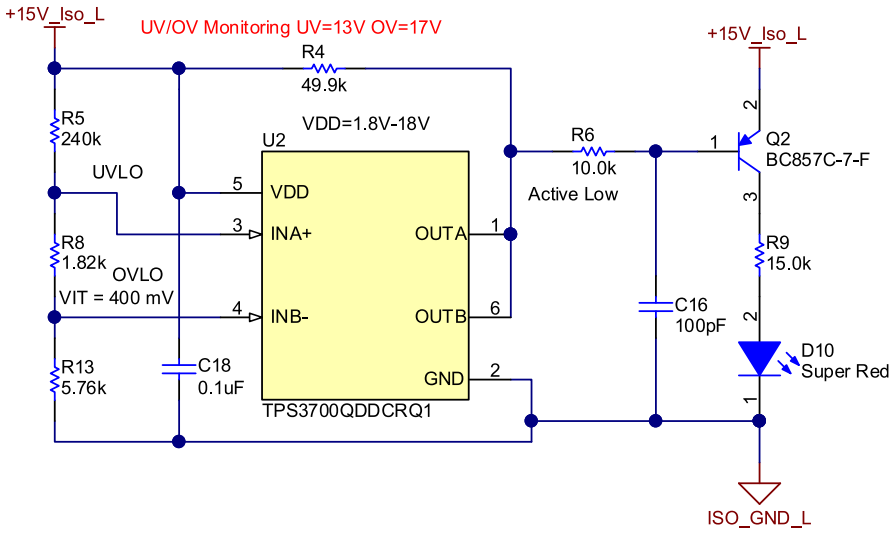


2.4.3.8 Overvoltage and Undervoltage Detection

The IGBT gate is driven from the 15-V rail to turn on the IGBT. The 15-V rail should not drop below the minimum gate voltage to properly turn on the IGBT. Driving the IGBT with lower gate voltage causes excessive power dissipation. Otherwise, excessive higher gate voltage will destroy the IGBT.

The overvoltage and undervoltage detection is designed with the window comparator TPS3700-Q1. It has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs. 图 9 shows the schematic of the detection circuit. The INA+ and INB- pins implement open-drain output. OUTA is driven low when the voltage at INA+ is below (V_{ITP} – V_{HYS}) (according to the TPS3700-Q1 data sheet). The output goes high when the sense voltage returns above the respective threshold. OUTB is driven low when the voltage at this comparator exceeds V_{ITP}. The output goes high when the sense voltage returns below the respective threshold. The undervoltage threshold is set as 13 V, and the overvoltage threshold is set as 17 V for this design. The OR logic is implemented by connecting the two open drain outputs of the TPS3700-Q1 device. OUTA and OUTB can merge into one logic signal that goes low if either output is asserted. A 49.9-kΩ pullup resistor is used to hold these lines high when the output goes to high impedance.

图 9. Overvoltage and Undervoltage Detection Schematic



3 Hardware, Testing Requirements, and Test Results

3.1 Hardware

图 10 shows the isolated gate driver board and connectors pin description. The placement of components and corresponding circuits are also described. 图 11 and 图 12 show the PCB board image of LM5180-Q1 based flyback converter from the top and bottom side, respectively. The input and output connectors are indicated.

图 10. Isolated Gate Driver Board and Connectors Pin Description

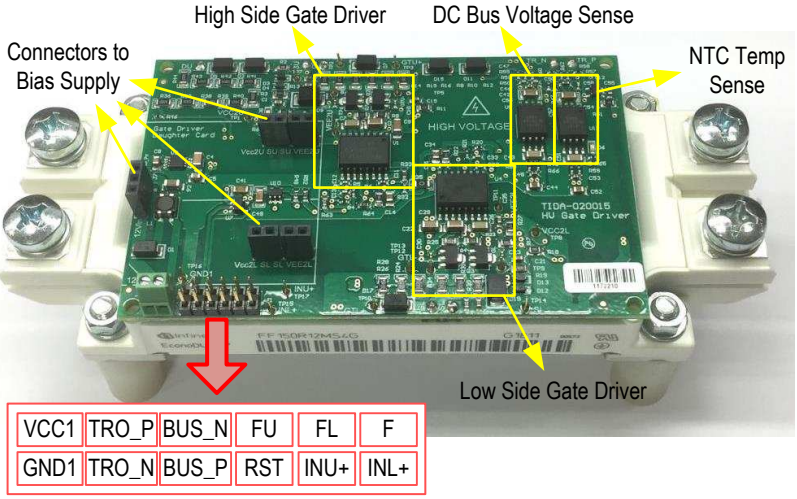


图 11. LM5180-Q1 Based Flyback PCB Board Top Side

图 12. LM5180-Q1 Based Flyback PCB Board Bottom Side

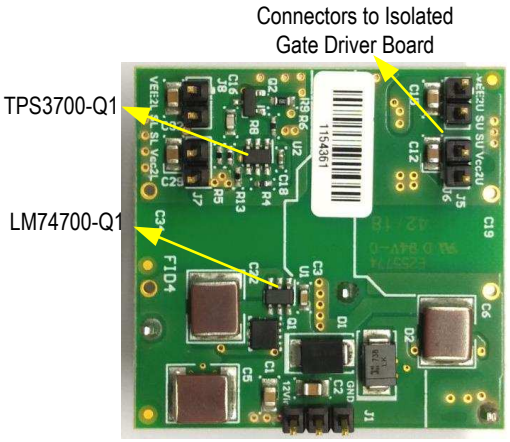


图 13 shows the LM5180-Q1 based flyback PCB board implemented on top of the isolated gate driver board and the IGBT module.

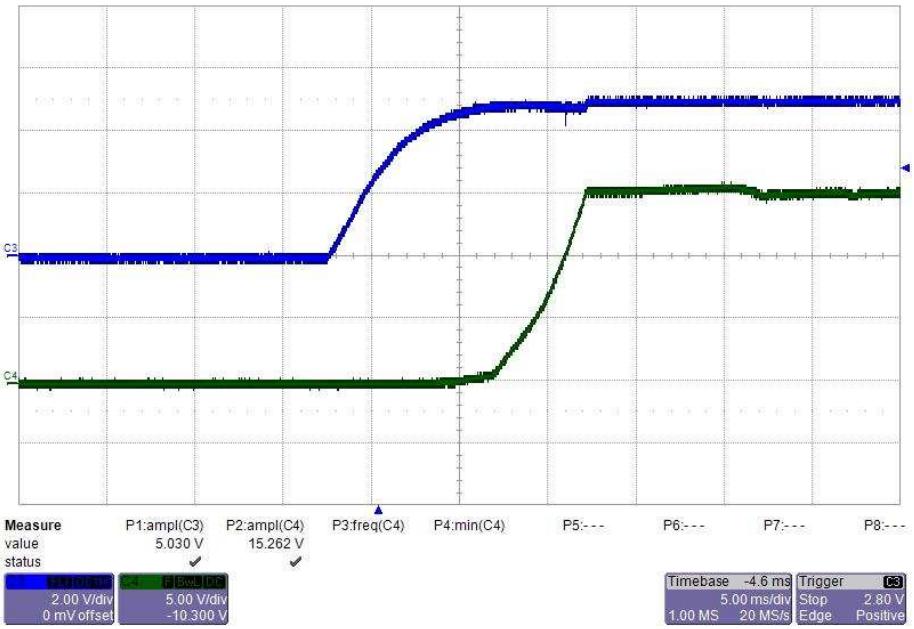
图 13. Implementation With Power Stage and IGBT Module

3.2 Testing and Results

3.2.1 Startup

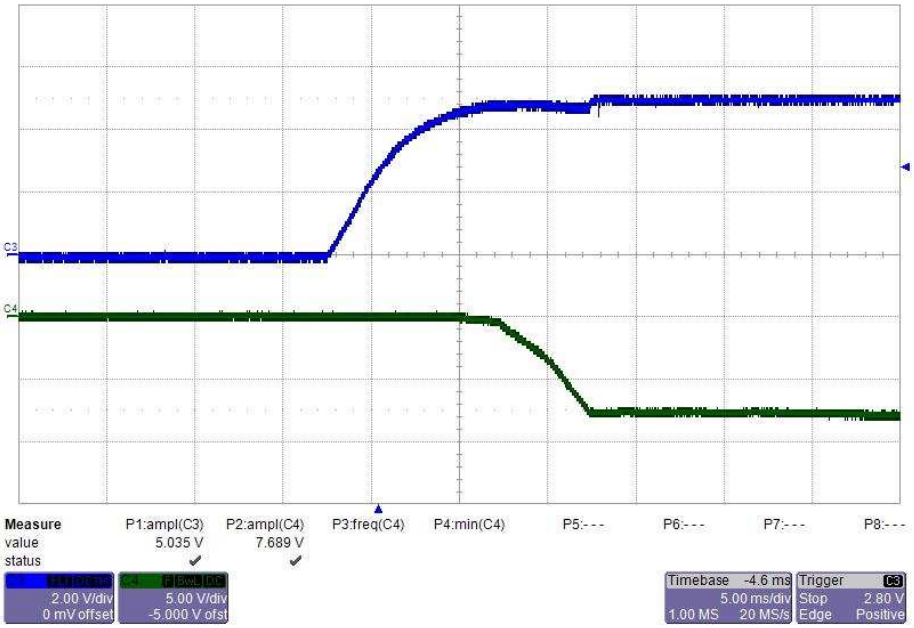
The startup waveforms of the flyback converter designed with LM5180-Q1 are measured under 5-V input and 12-V input, respectively. The 15-V and –9-V rails are measured separately.

图 **14. Start-up Waveform of the 15-V Rail With V_{IN} = 5 V and no Load**



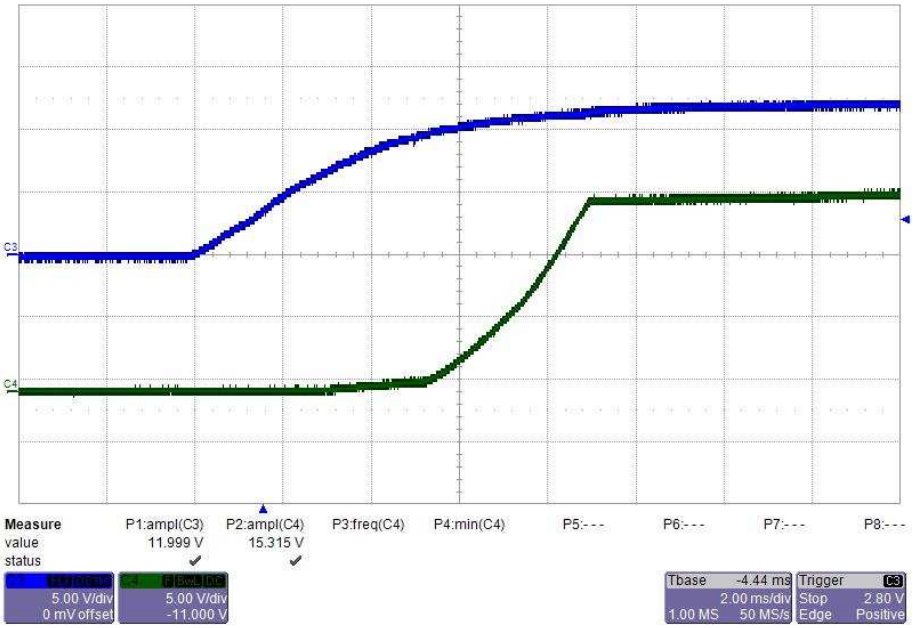
From top to bottom: CH3: input voltage 2 V/div, CH4: output voltage 5 V/div, 5 ms/div

图 **15. Start-up Waveform of the –9-V Rail With V_{IN} = 5 V and no Load**



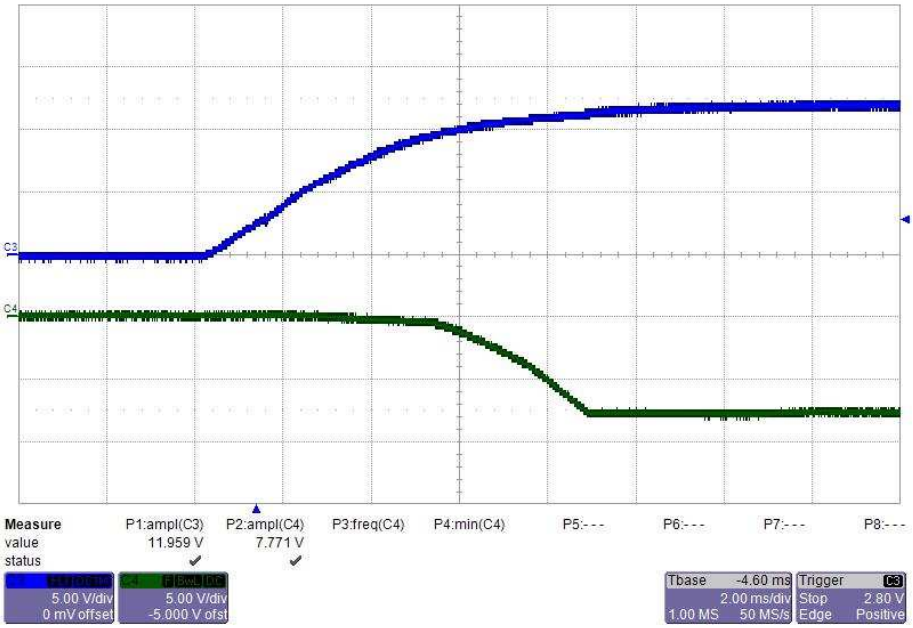
From top to bottom: CH3: input voltage 2 V/div, CH4: output voltage 5 V/div, 5 ms/div

图 16. Start-up Waveform of the 15-V Rail With V_{IN} = 12 V and no Load



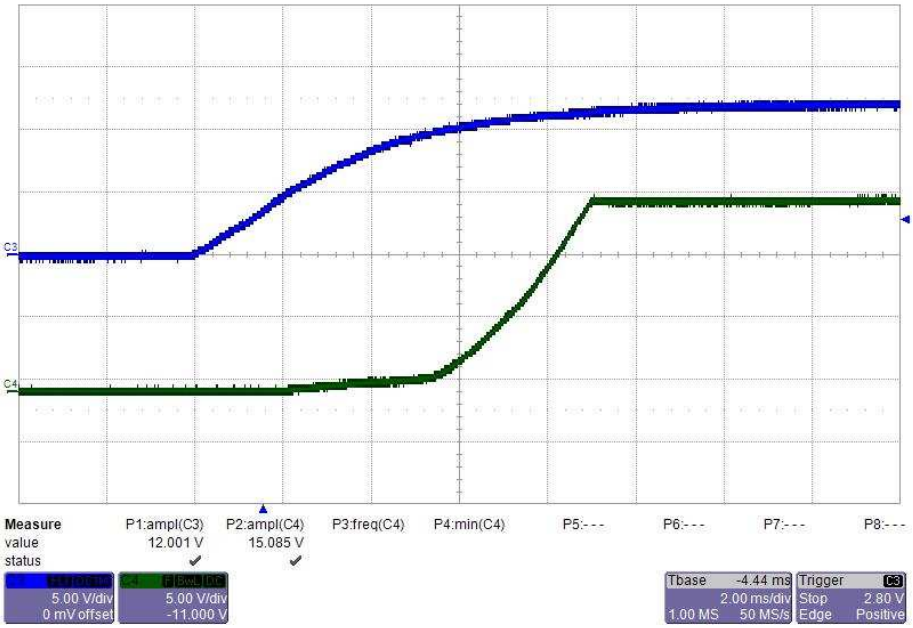
From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 2 ms/div

图 17. Start-up Waveform of the –9-V Rail With V_{IN} = 12 V and no Load



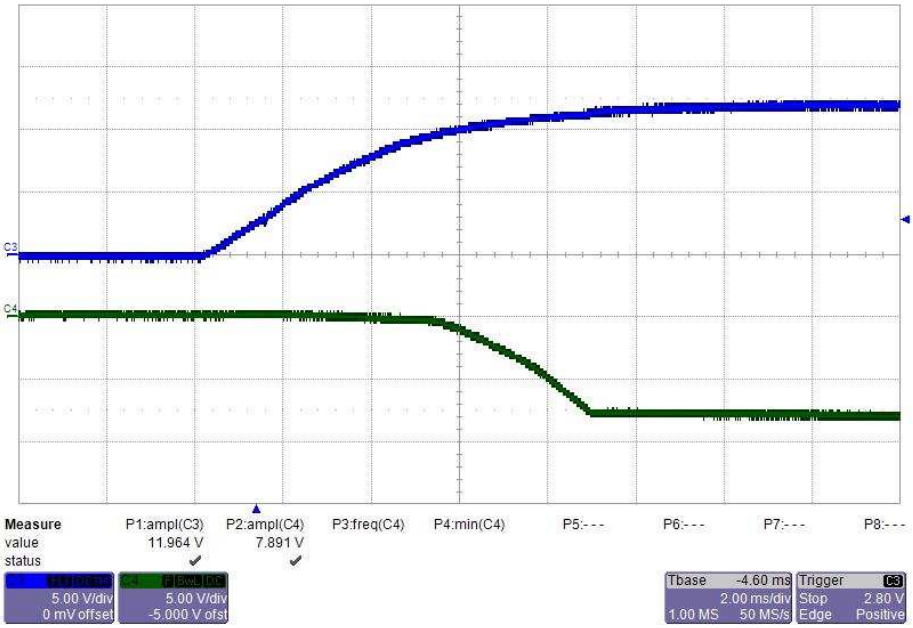
From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 2 ms/div

图 18. Start-up Waveform of the 15-V Rail With V_{IN} = 12 V and 180-mA Load



From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 2 ms/div

图 19. Start-up Waveform of the –9-V Rail With V_{IN} = 12 V and 180-mA Load

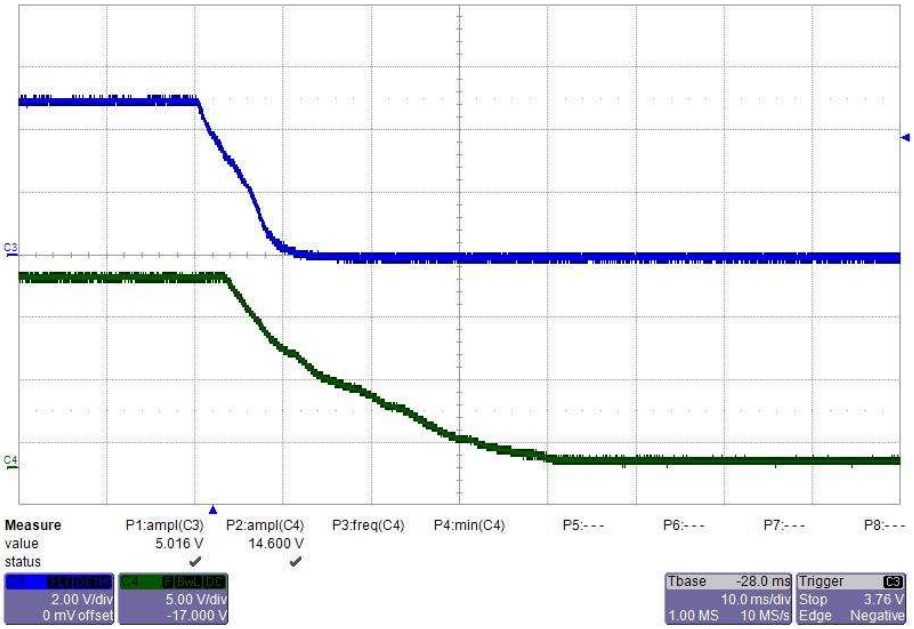


From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 2 ms/div

3.2.2 Power Down

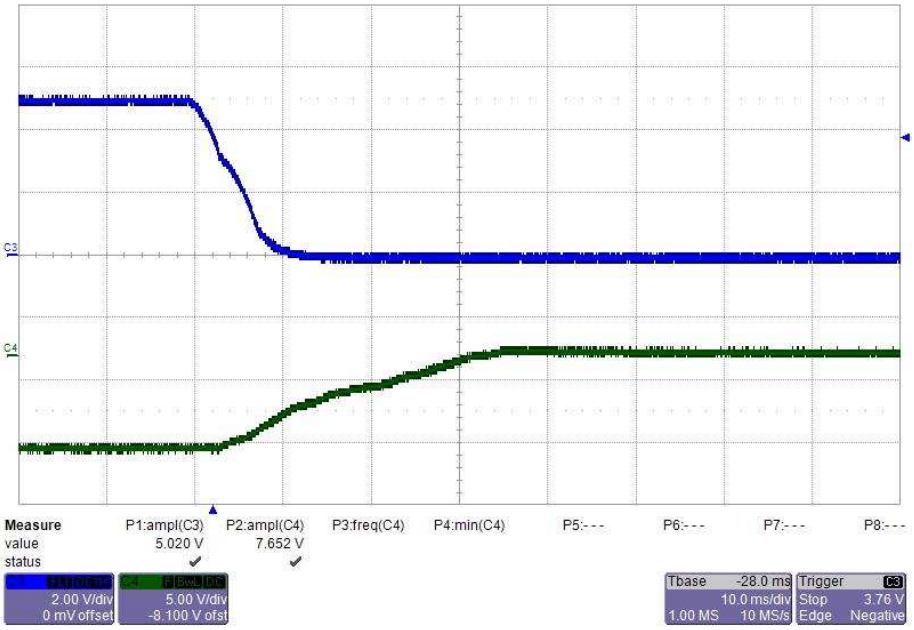
The power down waveforms of the flyback converter designed with LM5180-Q1 are measured under 5-V input and 12-V input, respectively. The 15-V and –9-V rails are measured separately.

图 **20. Power Down Waveform of the 15-V Rail With V_{IN} = 5 V and no Load**



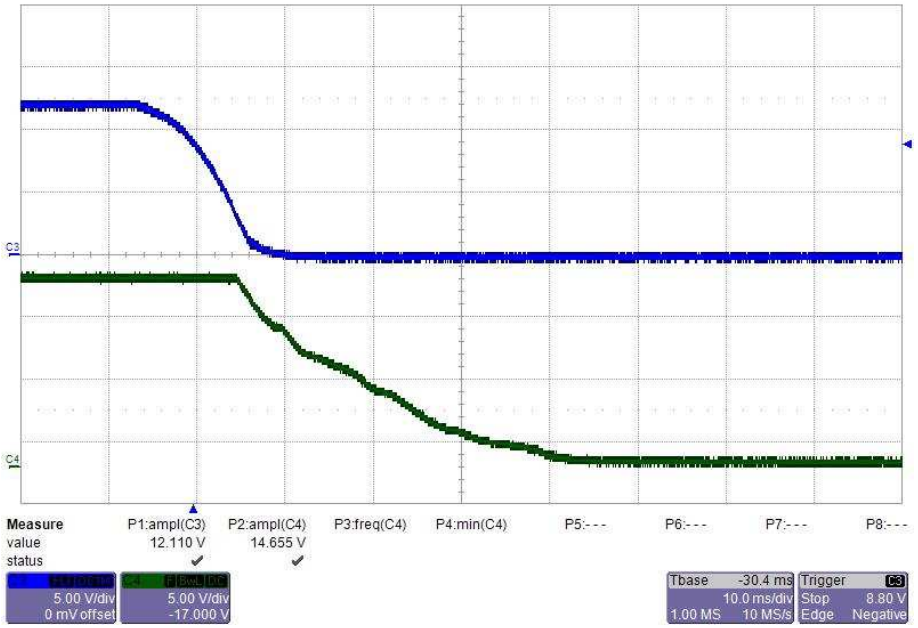
From top to bottom: CH3: input voltage 2 V/div, CH4: output voltage 5 V/div, 10 ms/div

图 **21. Power Down Waveform of the –9-V Rail With V_{IN} = 5 V and no Load**



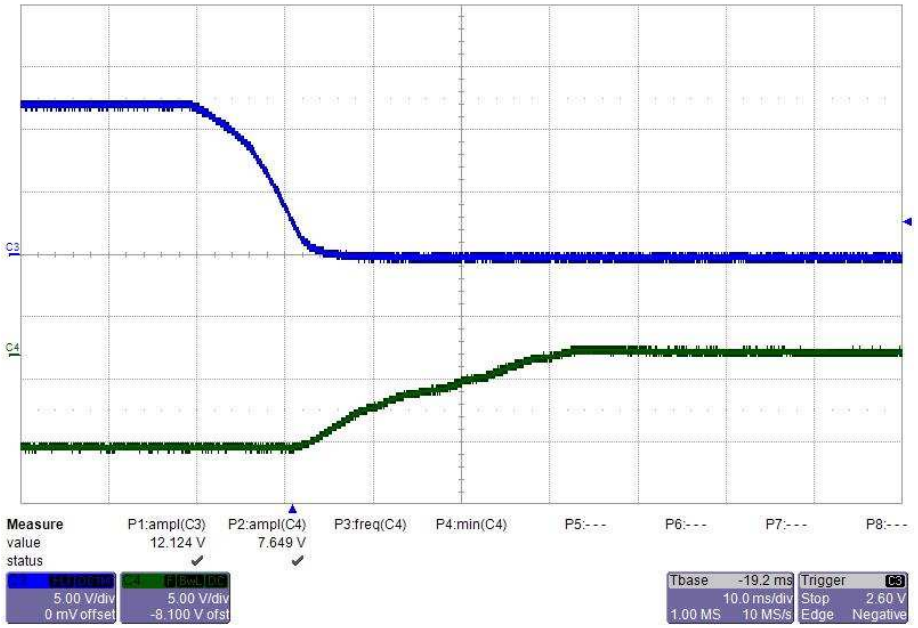
From top to bottom: CH3: input voltage 2 V/div, CH4: output voltage 5 V/div, 10 ms/div

图 22. Power Down Waveform of the 15-V Rail With V_{IN} = 12 V and no Load



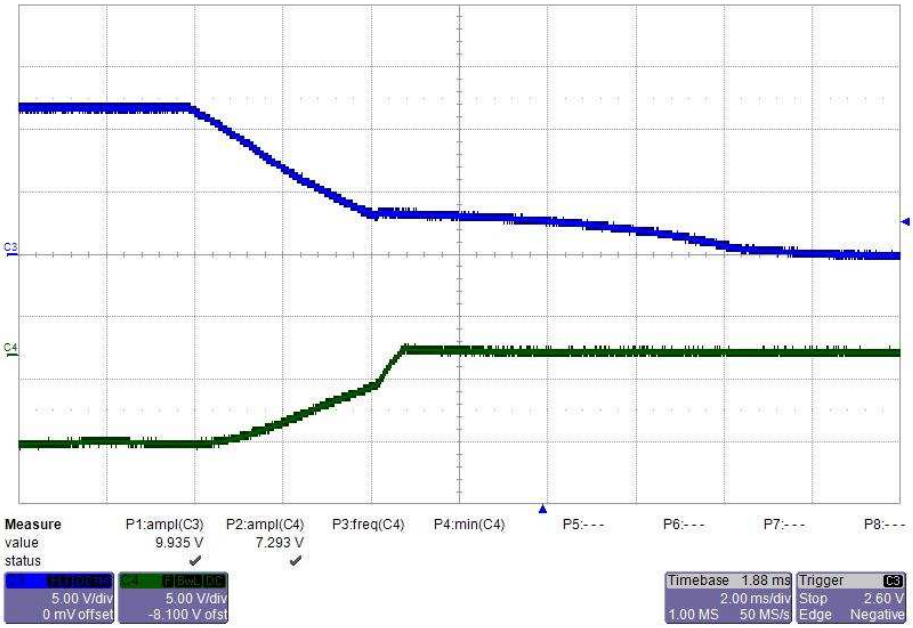
From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 10 ms/div

图 23. Power Down Waveform of the –9-V Rail With V_{IN} = 12 V and no Load



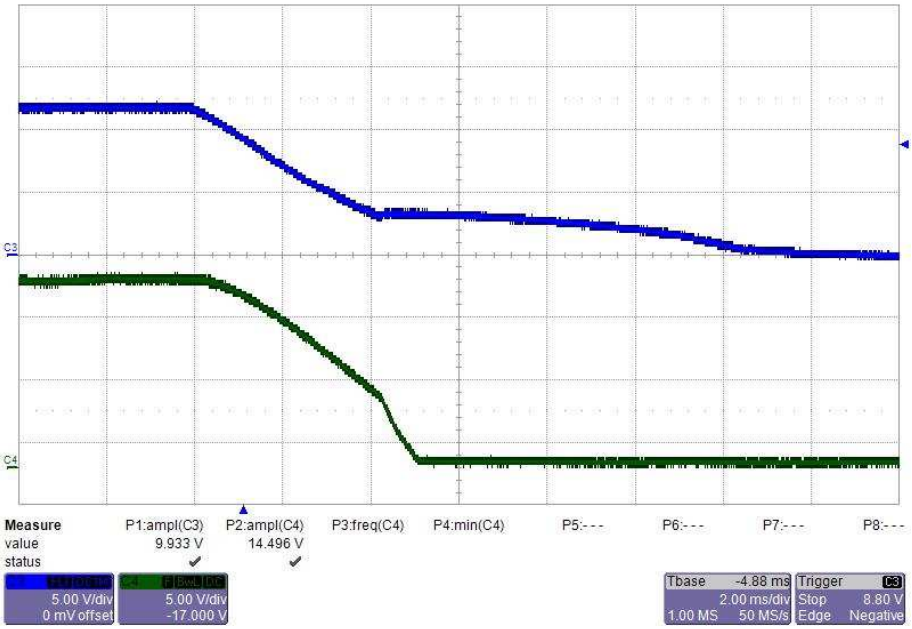
From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 10 ms/div

图 **24. Power Down Waveform of the –9-V Rail With V_{IN} = 12 V and 180-mA Load**



From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 2 ms/div

图 **25. Power Down Waveform of the +15-V Rail With V_{IN} = 12 V and 180-mA Load**

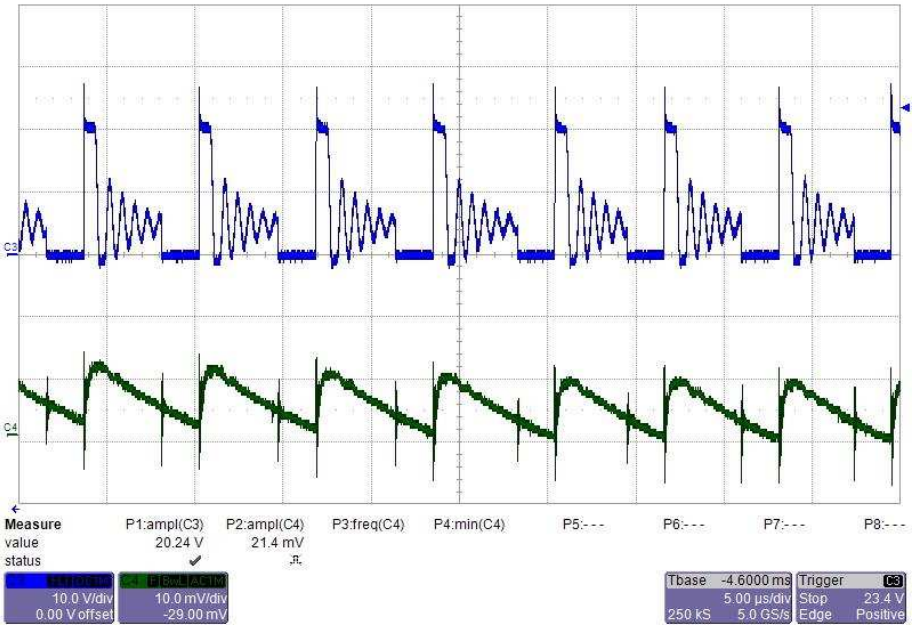


From top to bottom: CH3: input voltage 5 V/div, CH4: output voltage 5 V/div, 2 ms/div

3.2.3 Switch Node and Output Voltage Ripple

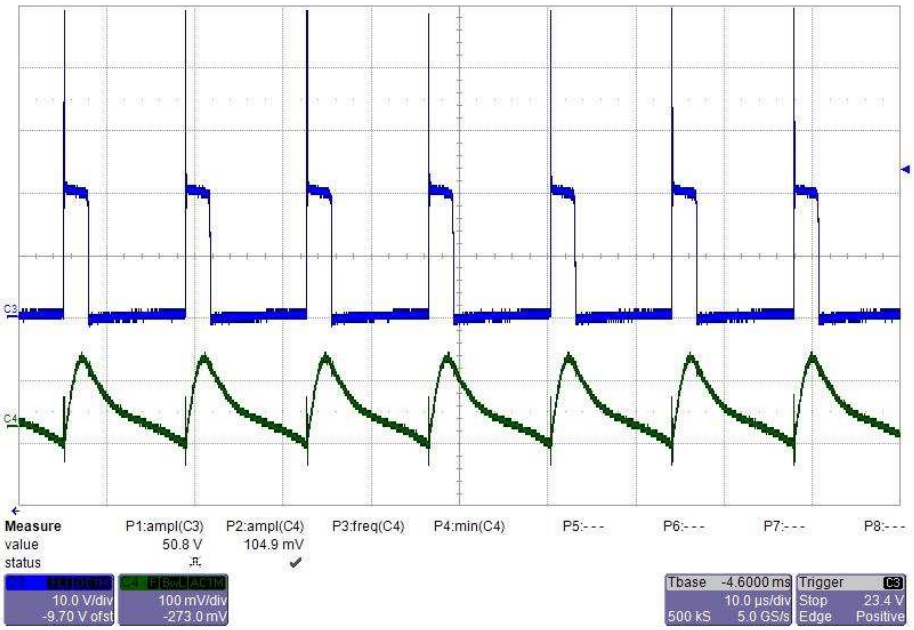
Switch node and output voltage ripple of the flyback converter designed with LM5180-Q1 are measured under 5-V input, 12-V input, and 18-V input, respectively. The 15-V and –9-V rails are measured separately.

图 26. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 5 V and no Load



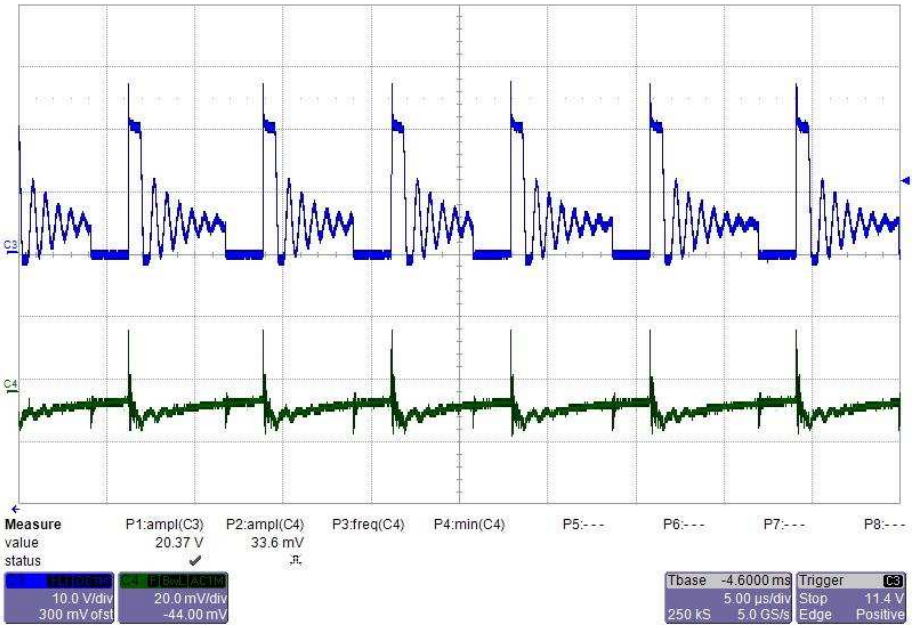
From top to bottom: CH3: switch node 10 V/div, CH4: output voltage ripple 10 mV/div, 5 µs/div

图 27. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 5 V and 85-mA Load



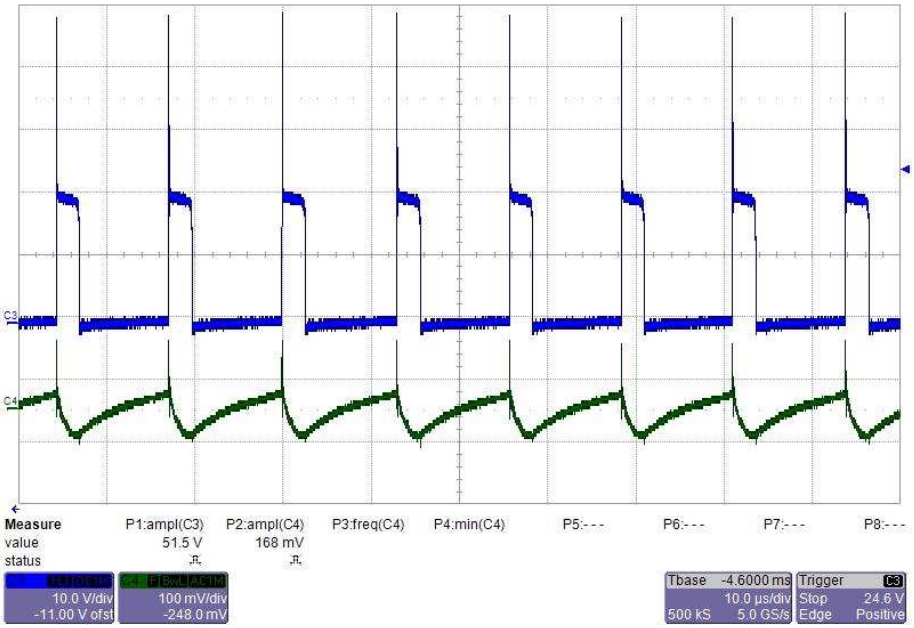
From top to bottom: CH3: switch node 10 V/div, CH4: output voltage ripple 100 mV/div, 10 µs/div

图 **28. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 5 V and no Load**



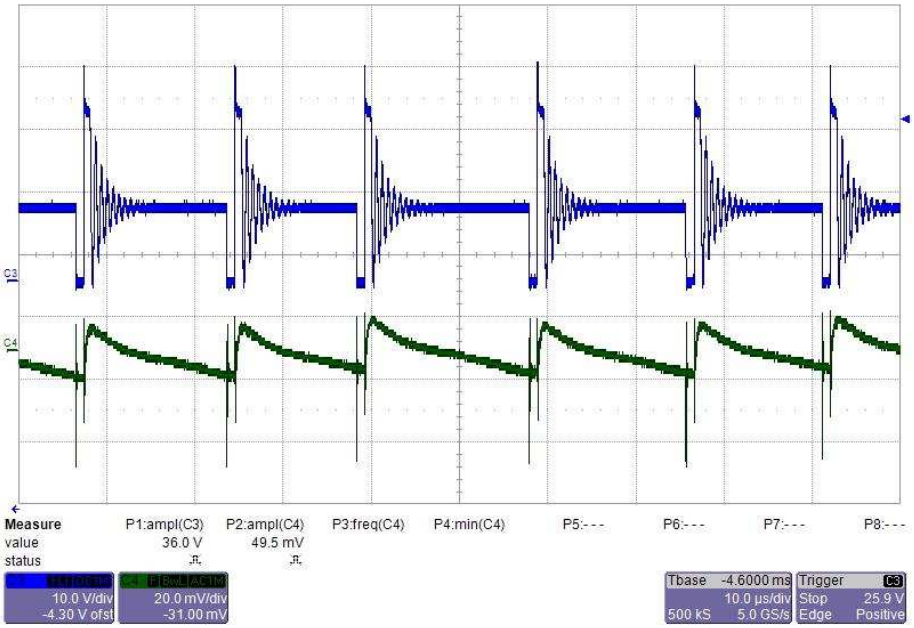
From top to bottom: CH3: switch node 10 V/div, CH4: output voltage ripple 20 mV/div, 5 µs/div

图 **29. Switch Node and Output Ripple of the –9-V Rail with V_{IN} = 5 V and 85-mA Load**



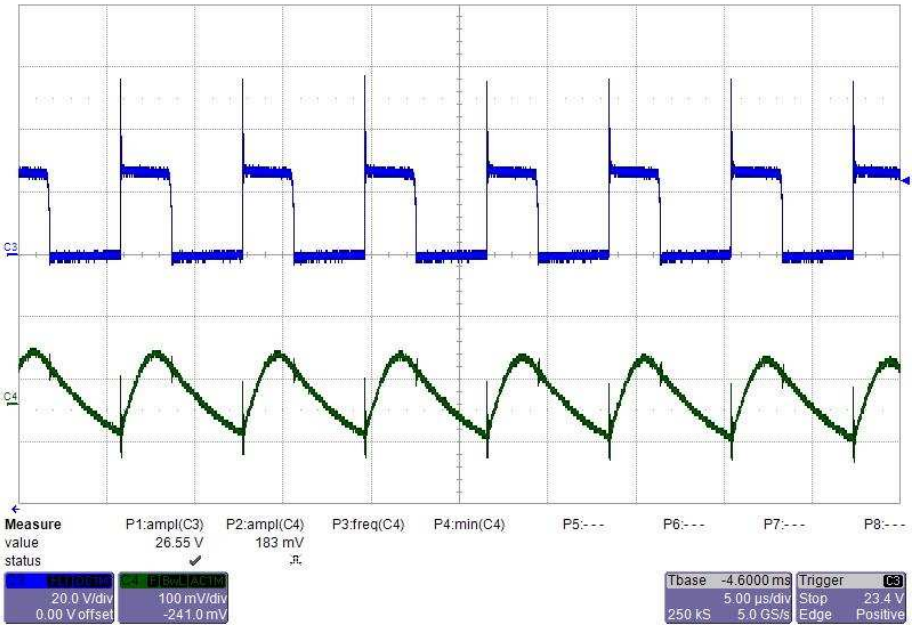
From top to bottom: CH3: switch node 10 V/div, CH4: output voltage ripple 100 mV/div, 10 µs/div

图 **30. Switch Node and Output ripple of the 15-V Rail with V_{IN} = 12 V and no Load**



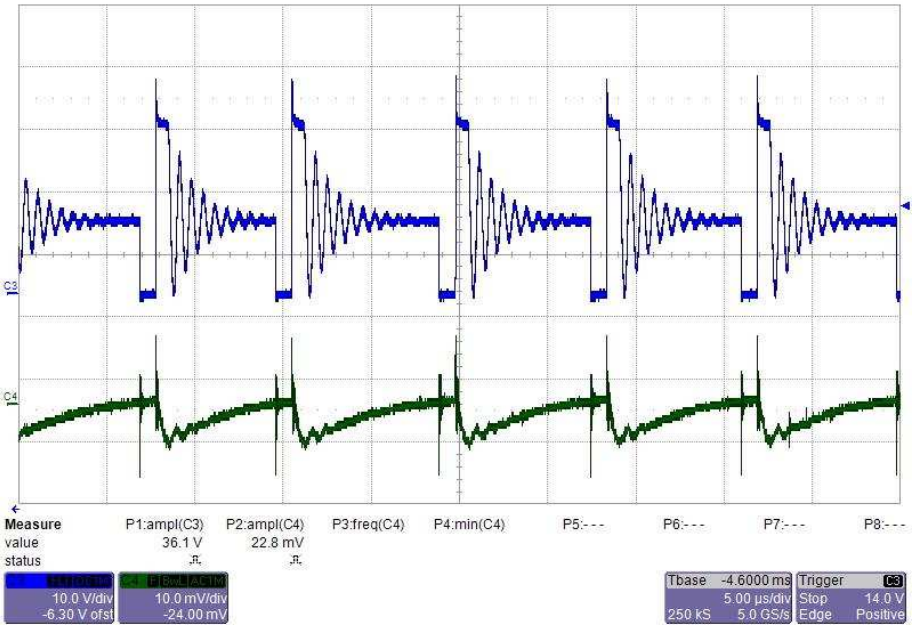
From top to bottom: CH3: switch node 10 V/div, CH4: output voltage ripple 20 mV/div, 10 µs/div

图 **31. Switch Node and Output ripple of the 15-V Rail with V_{IN} = 12 V and 180-mA Load**



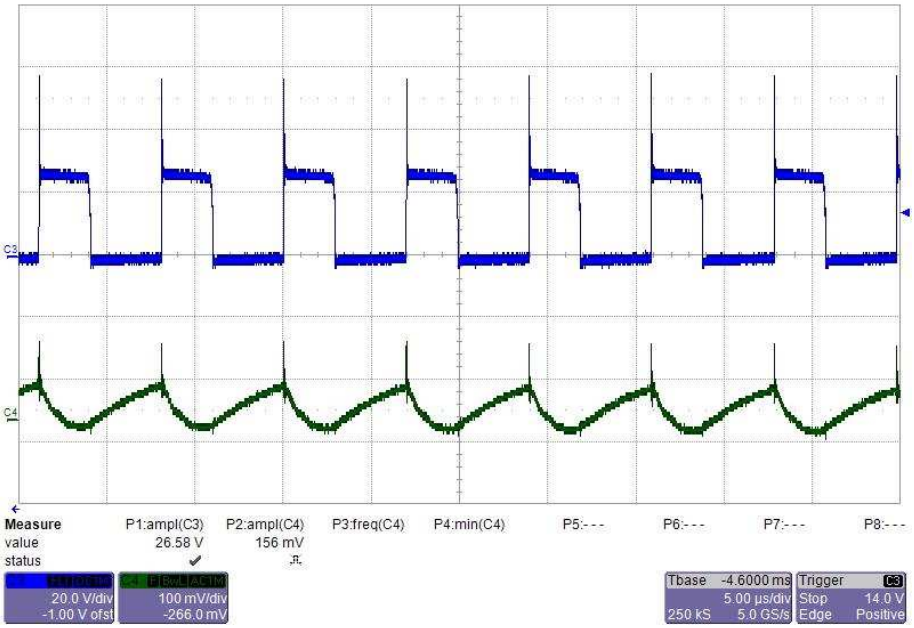
From top to bottom: CH3: switch node 20 V/div, CH4: output voltage ripple 100 mV/div, 5 µs/div

图 **32. Switch Node and Output ripple of the –9-V Rail with V_{IN} = 12 V and no Load**



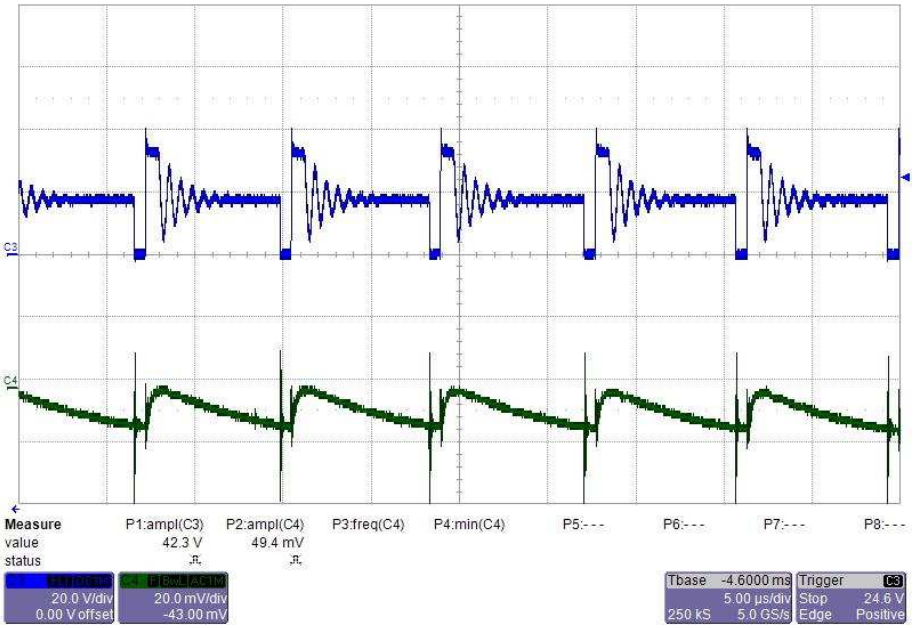
From top to bottom: CH3: switch node 10 V/div, CH4: output voltage ripple 10 mV/div, 5 µs/div

图 **33. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 12 V and 180-mA Load**



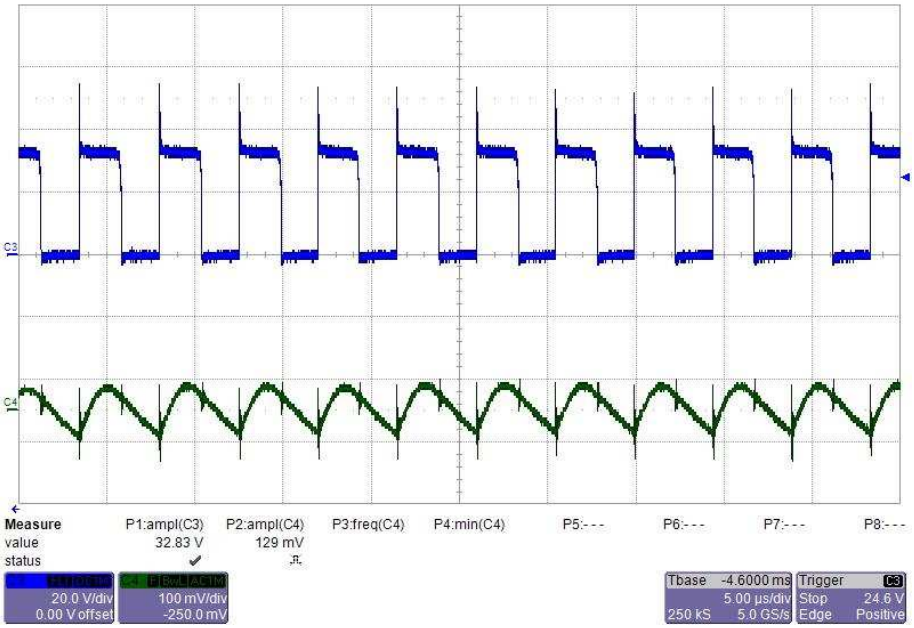
From top to bottom: CH3: switch node 20 V/div, CH4: output voltage ripple 100 mV/div, 5 µs/div

图 **34. Switch Node and Output Ripple of the 15-V Rail With V_{IN} = 18 V and no Load**



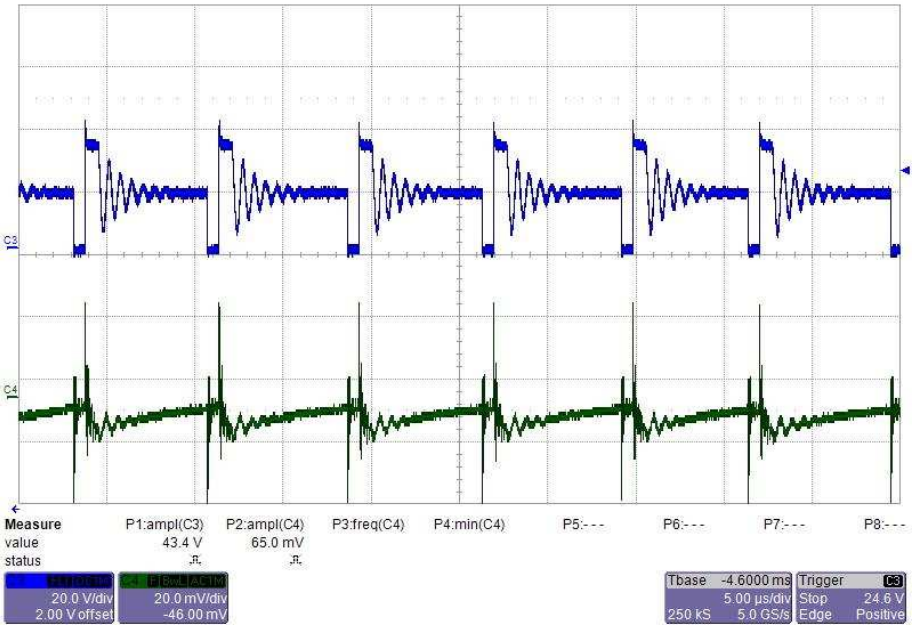
From top to bottom: CH3: switch node 20 V/div, CH4: output voltage ripple 20 mV/div, 5 µs/div

图 **35. Switch Node and Output Ripple of the +15-V Rail With V_{IN} = 18 V and 180-mA Load**



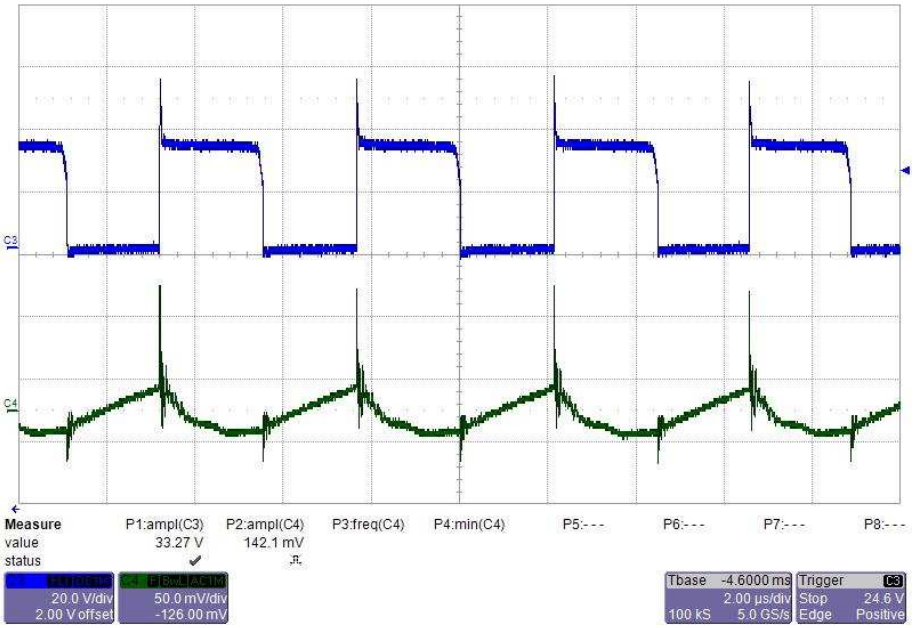
From top to bottom: CH3: switch node 20 V/div, CH4: output voltage ripple 100 mV/div, 5 µs/div

图 **36. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 18 V and no Load**



From top to bottom: CH3: switch node 20 V/div, CH4: output voltage ripple 20 mV/div, 5 µs/div

图 **37. Switch Node and Output Ripple of the –9-V Rail With V_{IN} = 18 V and 180-mA Load**

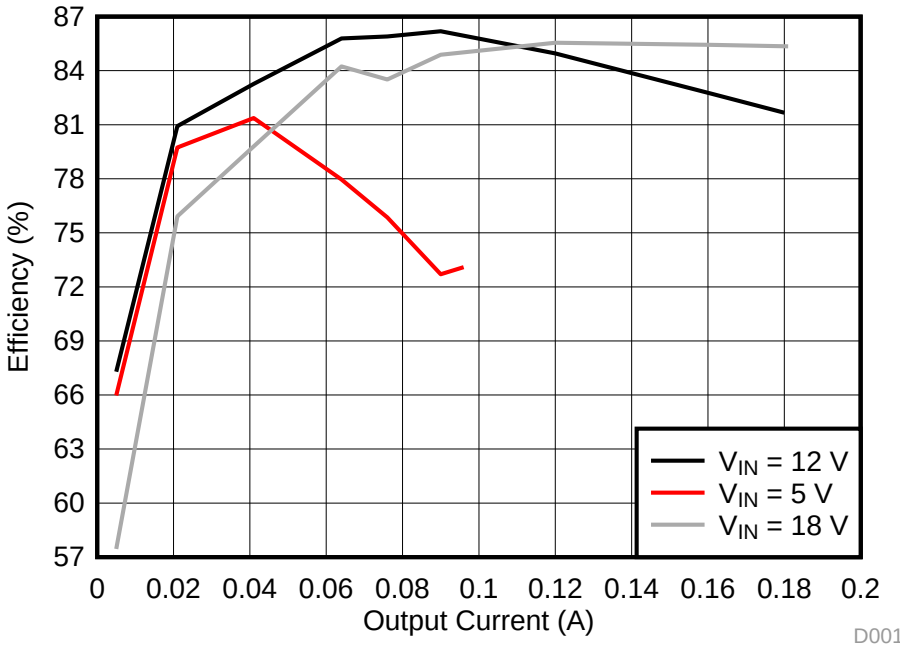


From top to bottom: CH3: switch node 20 V/div, CH4: output voltage ripple 50 mV/div, 2 µs/div

3.2.4 Efficiency

图 38 shows the measured efficiency of the flyback converter designed with LM5180-Q1 over the full load range. Around 86% peak efficiency is achieved with the input voltages of 5 V, 12 V, and 18 V, respectively.

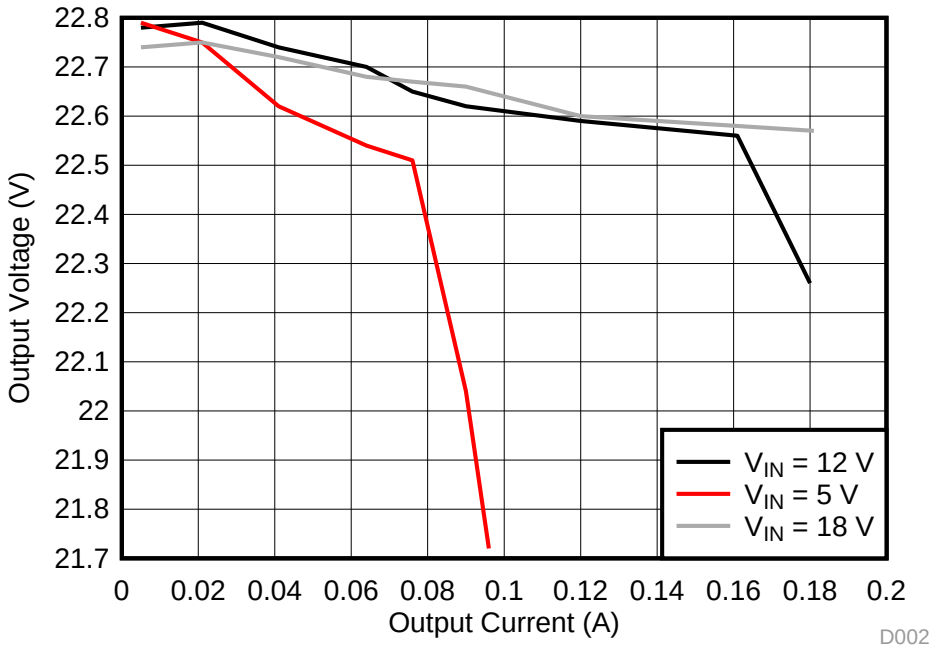
图 **38. Measured Efficiency Under Input Voltages of 5 V, 12 V, and 18 V**



3.2.5 Load Regulation

Load regulation measurements show the % deviation from nominal output voltage as a function of output current. 图 39 shows the measured result of the flyback converter designed with the LM5180-Q1 device. The load regulation is measured with the input voltages of 5 V, 12 V, and 18 V, respectively.

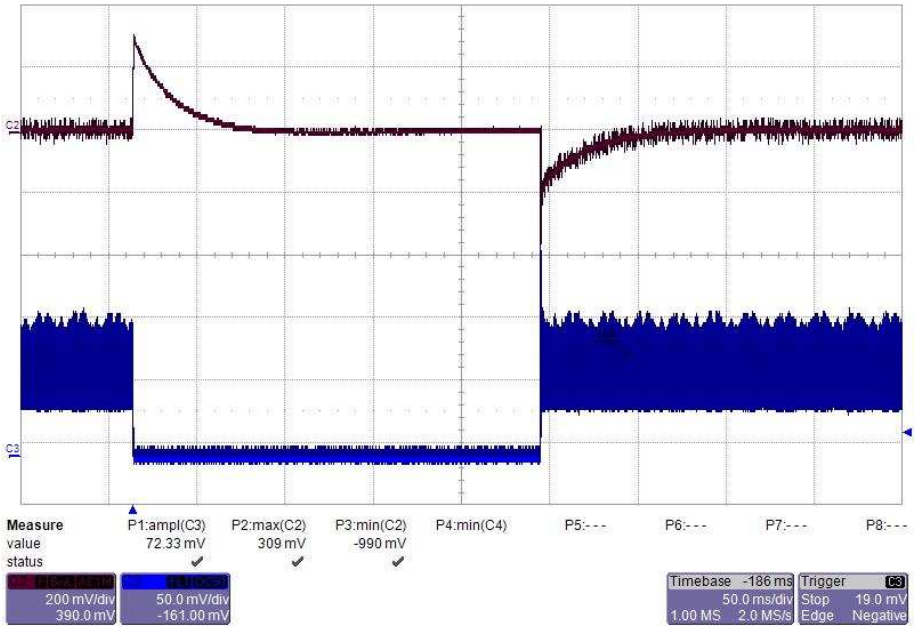
图 **39. Load Regulation Under Input Voltages of 5 V, 12 V, and 18 V**



3.2.6 Load Transients

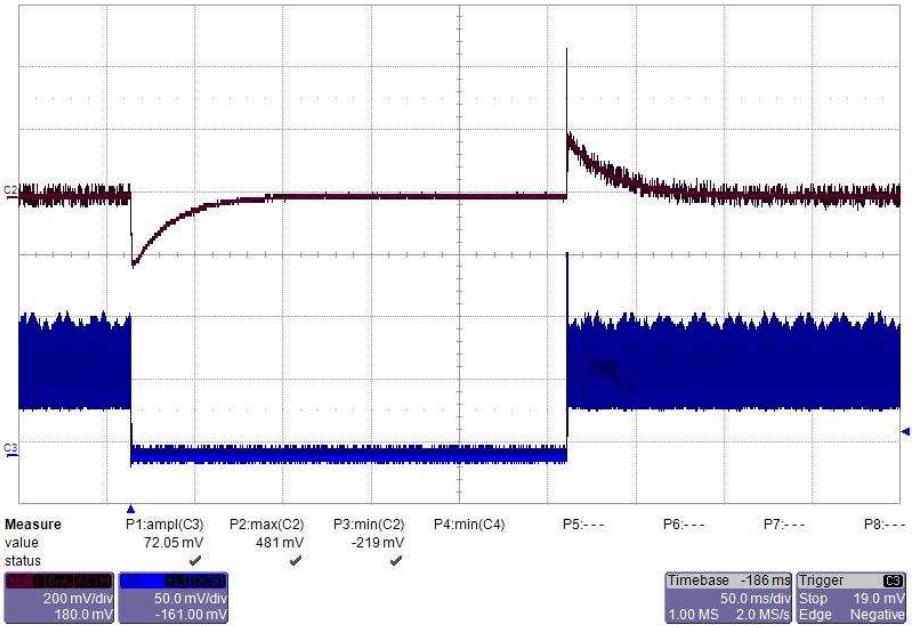
This section shows load transient measurements of the flyback converter designed with the LM5180-Q1 device. Load transient response presents how well a power supply copes with the changes in the load current demand. During the test the load is switching from 0 to full under input voltages of 5 V, 12 V, and 18 V, respectively.

图 40. Load Transient Response of the 15-V Rail Under V_{IN} = 5 V and I_{OUT} Switching Between 0 and 80 mA



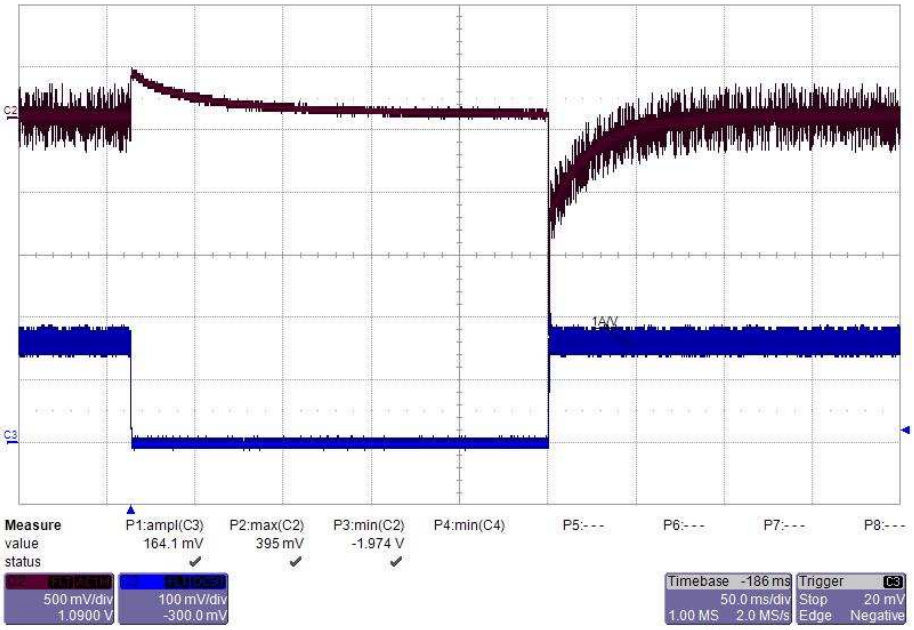
From top to bottom: CH2: output voltage 200 mV/div, CH3: load current 500 mA/div, 50 ms/div

图 **41. Load Transient Response of the –9-V Rail Under V_{IN} = 5 V and I_{OUT} Switching Between 0 and 80 mA**



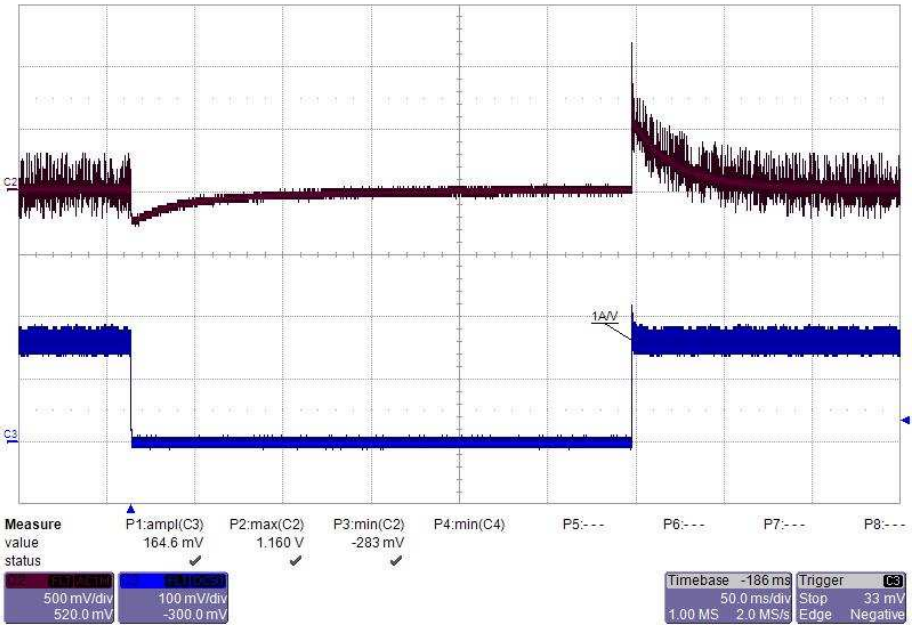
From top to bottom: CH2: output voltage 200 mV/div, CH3: load current 500 mA/div, 50 ms/div

图 **42. Load Transient Response of the 15-V Rail Under V_{IN} = 12 V and I_{OUT} Switching Between 0 and 180 mA**



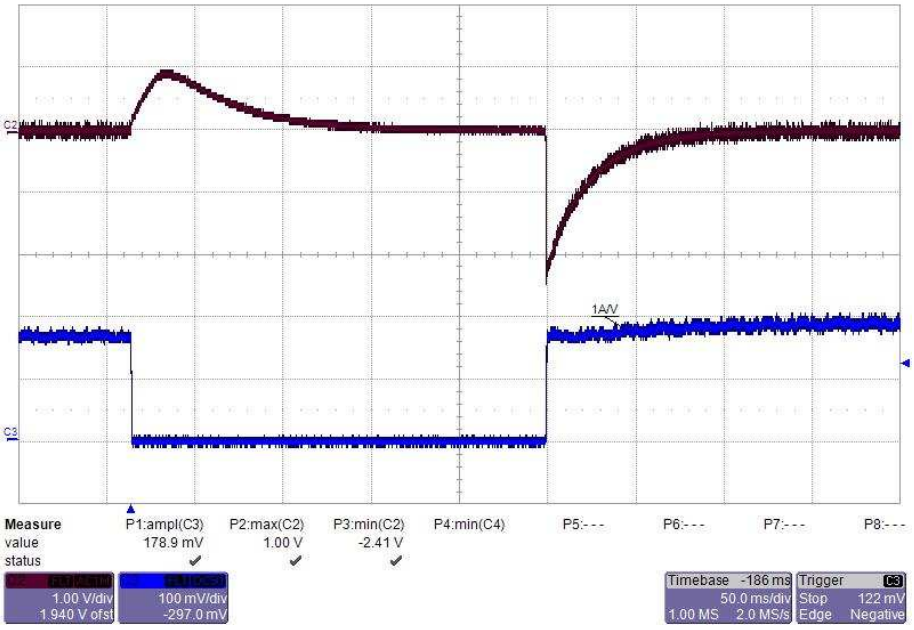
From top to bottom: CH2: output voltage 500 mV/div, CH3: load current 1 A/div, 50 ms/div

图 **43. Load Transient Response of the –9-V Rail Under V_{IN} = 12 V and I_{OUT} Switching Between 0 and 180 mA**



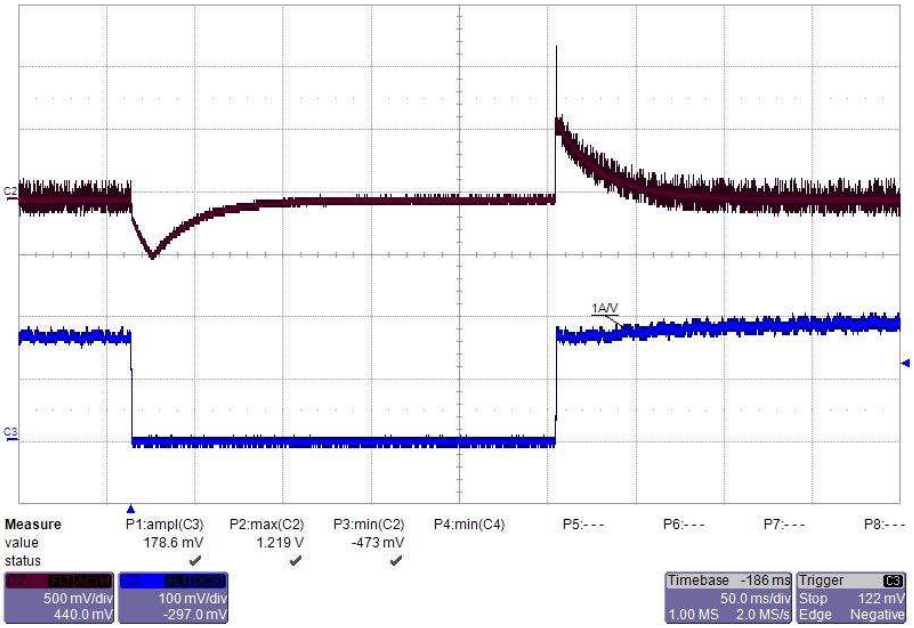
From top to bottom: CH2: output voltage 500 mV/div, CH3: load current 1 A/div, 50 ms/div

图 **44. Load Transient Response of the 15-V Rail Under V_{IN} = 18 V and I_{OUT} Switching Between 0 and 180 mA**



From top to bottom: CH2: output voltage 1 V/div, CH3: load current 1 A/div, 50 ms/div

图 **45. Load Transient Response of the –9-V Rail Under V_{IN} = 18 V and I_{OUT} Switching Between 0 and 180 mA**

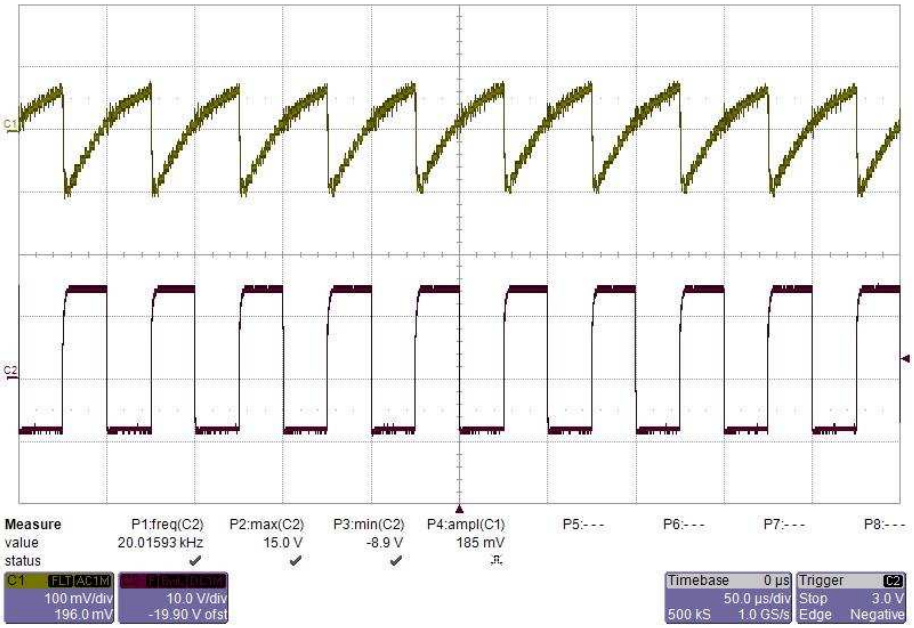


From top to bottom: CH2: output voltage 500 mV/div, CH3: load current 1 A/div, 50 ms/div

3.2.7 Voltage Ripple While Switching IGBT

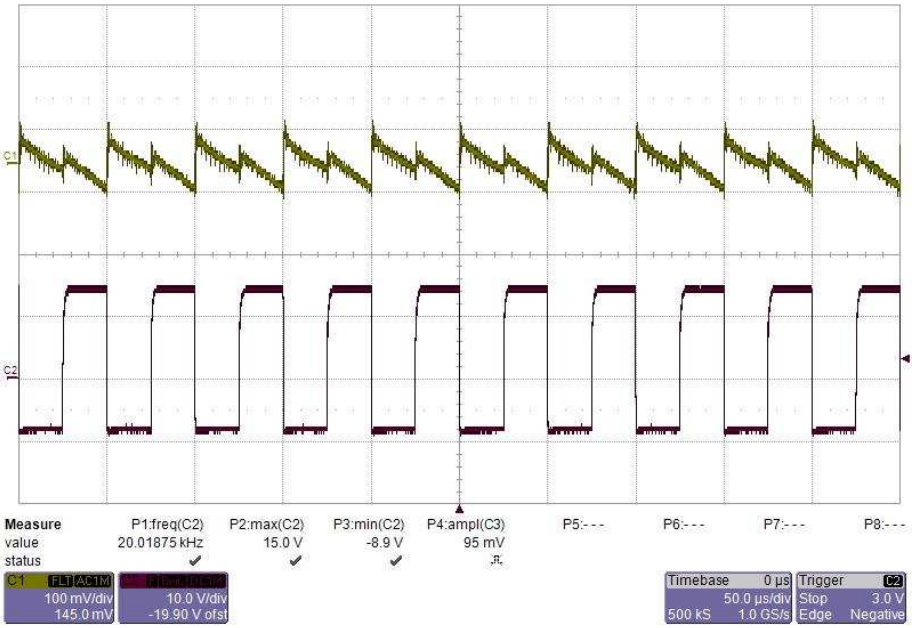
The flyback converter designed with the LM5180-Q1 device is connected to the isolated gate drivers (ISO5852S-Q1) and the 1200-V IGBT module for checking the voltage ripple during the switching transients. The IGBTs are switched at 20-kHz and 50-kHz frequency, respectively.

图 **46. Voltage Ripple of the 15-V Rail While Switching the IGBT Module at 20 kHz**



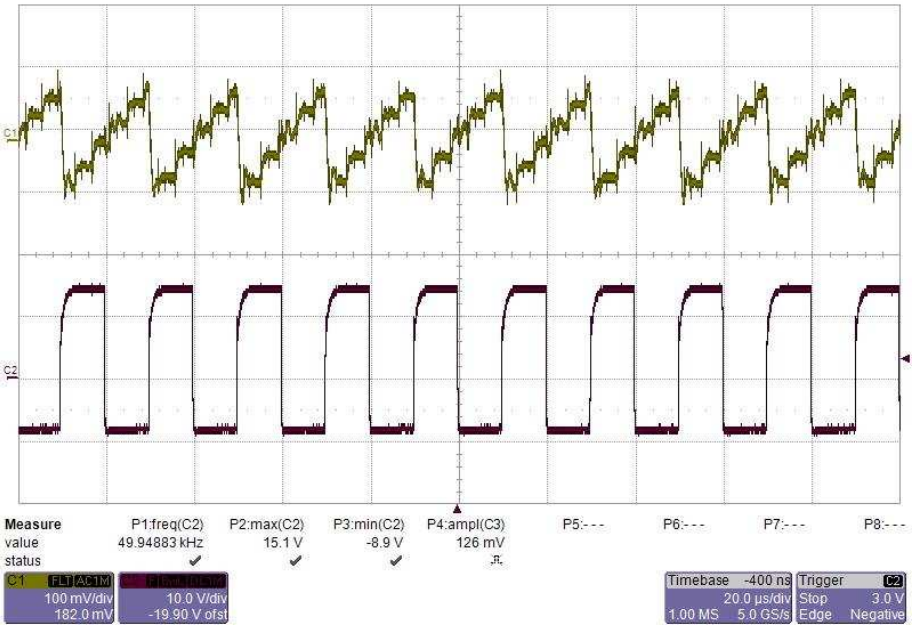
From top to bottom: CH1: output voltage 100 mV/div, CH2: gate PWM signal 10 V/div, 50 µs/div

图 **47. Voltage Ripple of the –9-V Rail While Switching the IGBT Module at 20 kHz**



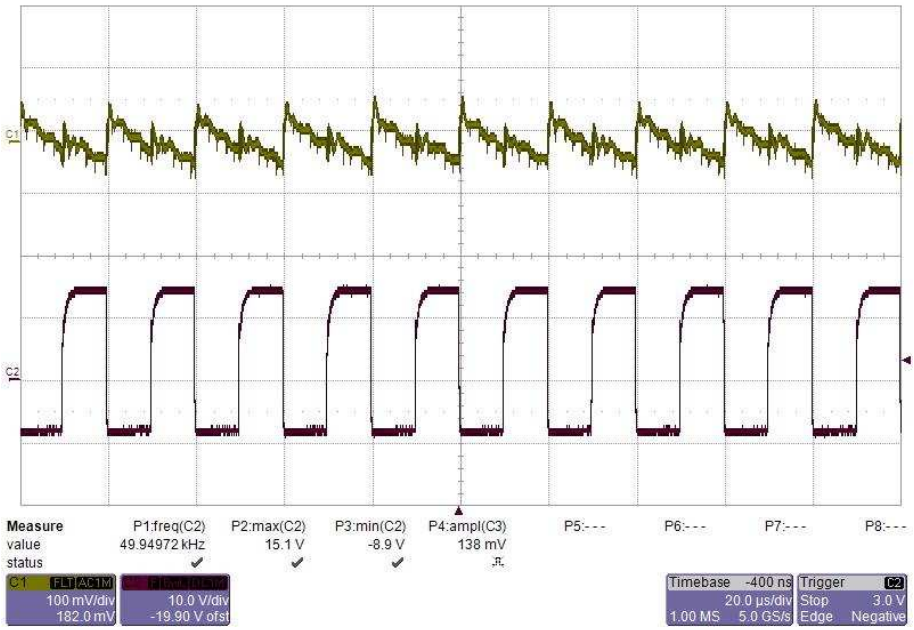
From top to bottom: CH1: output voltage 100 mV/div, CH2: gate PWM signal 10 V/div, 50 µs/div

图 **48. Voltage Ripple of the 15-V Rail While Switching the IGBT Module at 50 kHz**



From top to bottom: CH1: output voltage 100 mV/div, CH2: gate PWM signal 10 V/div, 20 µs/div

图 **49. Voltage Ripple of the –9-V Rail While Switching the IGBT Module at 50 kHz**

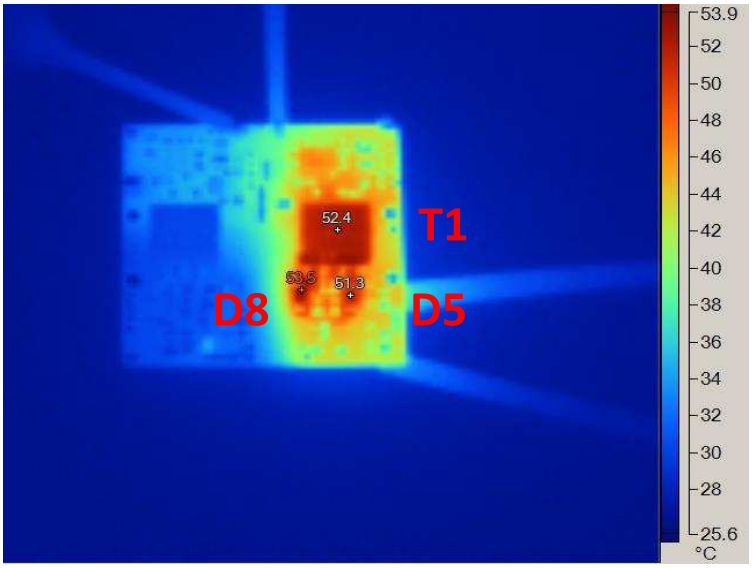


From top to bottom: CH1: output voltage 100 mV/div, CH2: gate PWM signal 10 V/div, 20 µs/div

3.2.8 Thermal Image

The thermal of the flyback converter is measured under the full-load conditions. The circuit runs at room temperature for 30 minutes. A 12-V nominal voltage is applied. The converter is loaded with 180 mA. 图 50 shows the thermal image of the board.

图 **50. Thermal Image With V_{IN} = 12 V and I_{OUT} = 180 mA**



T1: flyback transformer, D8 and D5: secondary rectification diode

3.2.9 High-Voltage Test

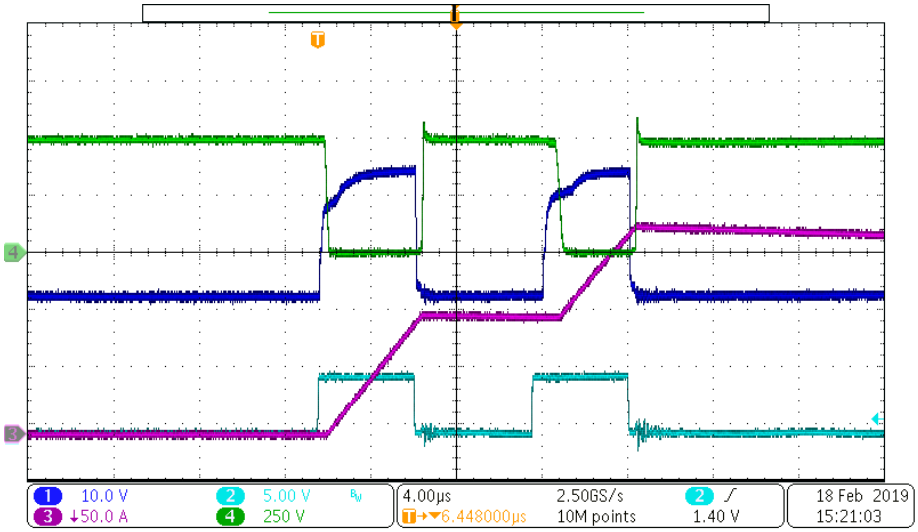
The bias supply is connected to the power stage and the IGBT module (FF150R12MS4G) for high-voltage tests.

3.2.9.1 Double Pulse Test

The double test is performed under high voltage and to evaluate the switching parameters of the IGBT and the performance of the isolated gate driver. The test is considered as one periodical snapshot of the system, and it is done with a purely inductive load. The driver parameters of switching speed, thermal, parasitic oscillations can be observed.

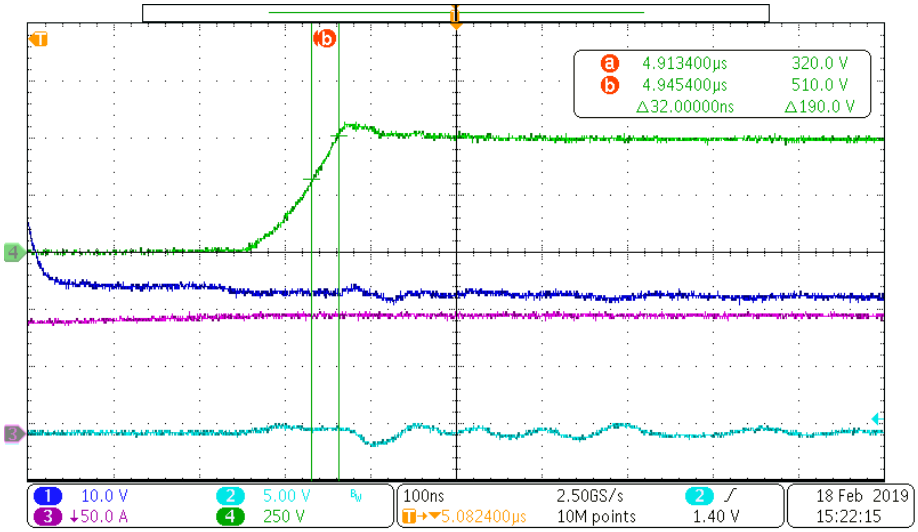
During the test, 500 V voltage is applied on the DC bus. The pulse train consists of two pulses with a repetition frequency of about 100 kHz. The widths of two pulses are both 4.5 µs. The delay is set to be 5.5 µs for the voltage and currents to settle out. The rise and fall time of the pulses are set as 5 ns.

图 **51. Double Pulse Test on the Power Stage**



(From top to bottom: CH4: IGBT Vds voltage 250 V/div, CH1: IGBT gate signal, 10 V/div, CH2: PWM signal at ISO5852s-Q1 input, 5 V/div, CH3: Inductor current, 50 A/div, 4 µs/div)

图 52. dv/dt at the IGBT Vds Voltage Turn-off Transient (6 V/ns)



CH4: IGBT Vds voltage 250 V/div, 100 ns/div

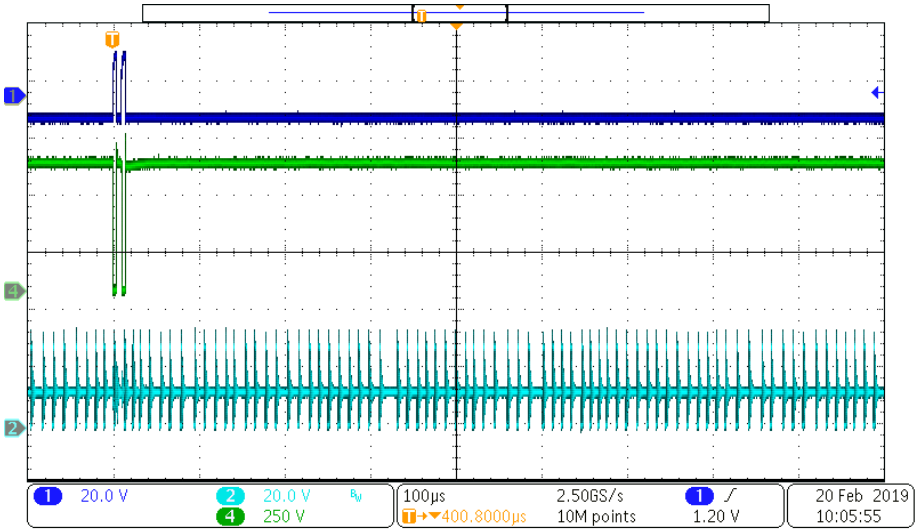
3.2.9.2 CMTI

The TI design is connected to a high-voltage DC bus for the high-voltage immunity test. Common-mode transient immunity (CMTI) is a maximum tolerable rate of rise or fall of the common mode voltage applied between two isolated circuits. The unit is normally in kV/µs or V/ns. High CMTI means that the two isolated circuits, both transmitter side and receiver side, function well when striking the insulation barrier with very high rise (positive) slew rate, or high fall (negative) slew rate. For CMTI testing, the peak common-mode voltage should not exceed the allowed maximum repetitive working voltage between the two isolated circuits.

During the test, 570-V DC bus voltage is applied on the DC bus. A 20-µH air core inductor is connected between DC bus+ and IGBT half bridge neutral to bypass the high-side IGBT. The DC bus- terminal is connected to the low voltage ground which is also the bias supply primary-side ground. The low-side IGBT is pulsed twice. Hence, a pulsed high voltage is imposed between the primary and secondary grounds of high-side bias supply. The switch node of the high side bias supply is measured.

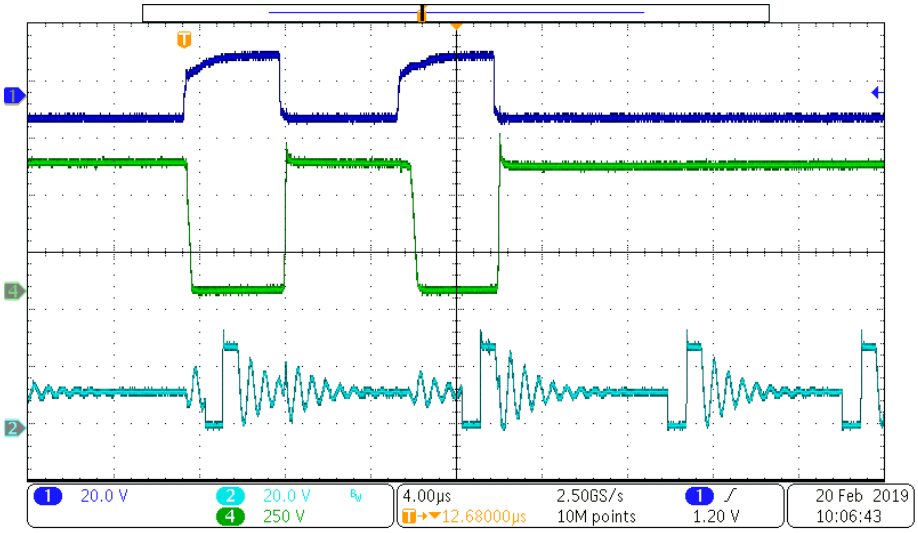
Testing waveforms on LM5180-Q1 based bias supply are shown in 图 53 through 图 55. The IGBT is switched with 570 V DC bus voltage and at 10.8 V/ns speed of dv/dt. Observe that the supply operates smoothly without interruption.

图 53. CMTI Test With Double Pulses



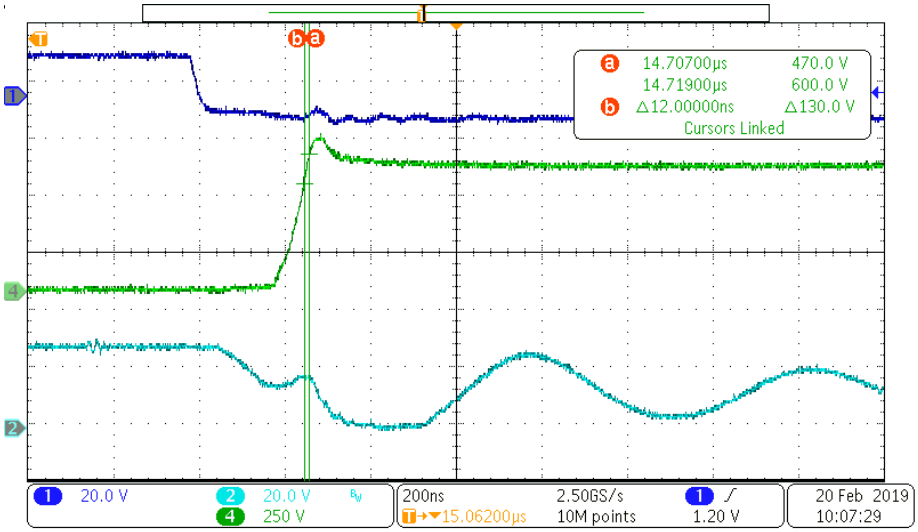
From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 250 V/div, CH2: LM5180-Q1 switch node voltage, 20 V/div, 100 µs/div

图 54. CMTI Waveforms Zoomed in



From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 250 V/div, CH2: LM5180-Q1 switch node voltage, 20 V/div, 4 µs/div

图 **55. dv/dt Transient of the CMTI (10.8 V/ns)**

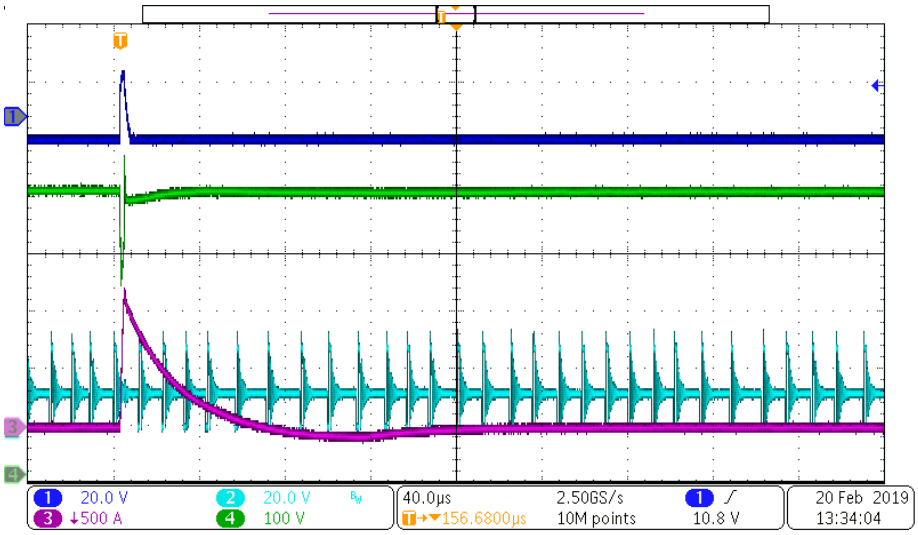


From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 250 V/div, CH2: LM5180-Q1 switch node voltage, 20 V/div, 200 ns/div

3.2.9.3 Short-Circuit Test

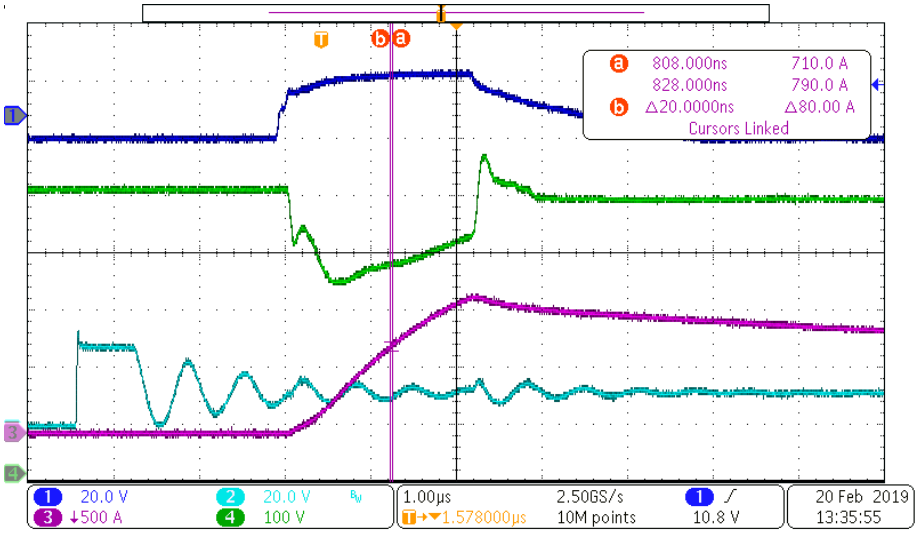
The IGBT module is turned on into short to measure the performance of power stage and the immunity of bias supplies under high di/dt. The high-side IGBT is shorted with thick cable with minimized impedance. The low-side IGBT is pulsed once and turned on into short. The switch node of the high-side bias supply is measured. The IGBT is switched with 500-V DC bus voltage and at 4 A/ns speed of di/dt. Observe that the supply operates smoothly without interruption.

图 **56. Short-Circuit Test**



From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 100 V/div, CH2: LM5180-Q1 switch node voltage 20/div, CH3: load current flowing from drain to source of the IGBT, 500 A/div, 40 µs/div

图 **57. di/dt transient during short circuit test**



From top to bottom: CH1: IGBT gate signal, 20 V/div, CH4: IGBT Vds voltage, 100 V/div, CH2: LM5180-Q1 switch node voltage 20/div, CH3: load current flowing from drain to source of the IGBT, 500 A/div, 1 µs/div

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-020015.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-020015.

4.3 PCB Layout Recommendations

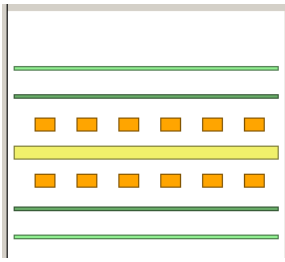
4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-020015.

4.3.2 Layout Guidelines

The TIDA-020015 implements a 2-layer PCB. The board material, copper thickness, and the dielectric distance in between are shown in 图 58.

图 **58. TIDA-020015 Layer Stack**



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask...	Surface Mat...	0.4	Solder Resist	3.5			0
Top Layer	Signal	Copper	1.4				Top	
Dielectric1	Dielectric	Core	59.2	FR-4	4.8			
Bottom Layer	Signal	Copper	1.4				Bottom	
Bottom Solder	Solder Mask...	Surface Mat...	0.4	Solder Resist	3.5			0
Bottom Over...	Overlay							

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-020015.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-020015.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-020015.

5 Related Documentation

1. Texas Instruments, *Automotive Wide V_{IN} Front-End Power Reference Design w/Cold Crank Operation and Transient Protection*
2. Texas Instruments, *HEV/EV Traction Inverter Power Stage Reference Design With 3 Types of IGBT/SiC Bias-Supply Solutions*
3. Texas Instruments, *98.6% Efficiency, 6.6-kW Totem-Pole PFC Reference Design for HEV/EV Onboard Charger Reference Design*
4. Texas Instruments, *Automotive Dual Channel SiC MOSFET Gate Driver Reference Design With Two Level Turn-Off Protection*

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6 About the Author

Xun Gong is an Automotive Systems Engineer at Texas Instruments, where he is responsible for developing reference design solutions for HEV/EV powertrain applications. Xun brings to this role expertise in the fields of onboard charger, DC/DC converter, and traction inverter with IGBT and SiC (Silicon Carbide) power transistors. Xun achieved his Ph.D. in Electrical Engineering from Delft University of Technology in Delft, Netherlands. Xun Gong won the 1st prize paper of the Academic Journal IEEE Transactions on Power Electronics in 2014.

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