设计指南：*TIDA-01028*
适用于高速示波器和宽带数字转换器的 ***12.8GSPS*** *模拟前端参考设计*

说明

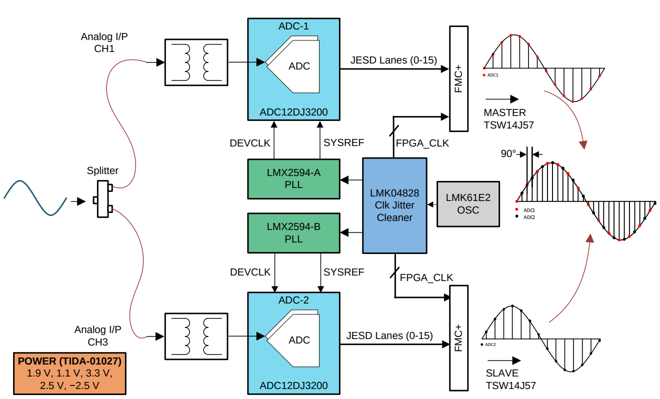
此参考设计提供了一个用于实现 12.8GSPS 采样率的交错射频采样模数转换器 (ADC) 的实用示例。这可通过对两个射频采样 ADC 进行时序交错来实现。交错需要在 ADC 之间进行相移，此参考设计通过 ADC12DJ3200 的无噪声孔径延迟调节（tAD 调节）功能来实现相移。此功能还可用于最大限度地减少交错 ADC 的典型失配问题：最大程度地提升 SNR、ENOB 和 SFDR 性能。此参考设计还采用了支持 JESD204B 的低相位噪声时钟树，该时钟树通过 LMX2594 宽带 PLL、LMK04828 合成器以及抖动清除器来实现。

节 3.4.3 中的测试结果显示，在输入带宽为 2.0GHz 且未去除交错杂散的情况下，8.0 位、12.8GSPS、高速示波器有望得到 7.5 位 ENOB 的结果。 应用的需要。

资源

TIDA-01028	设计文件夹
ADC12DJ3200	产品文件夹
LMK04828、LMX2594、LMK61E2	产品文件夹
LMH6401、LMH5401	产品文件夹
TPS259261	产品文件夹
TIDA-01027	设计文件夹
ADC12DJ3200EVM	工具文件夹
TSW14J57EVM	工具文件夹

TI E2E™ Community 有问题？请访问 E2E™ 支持论坛

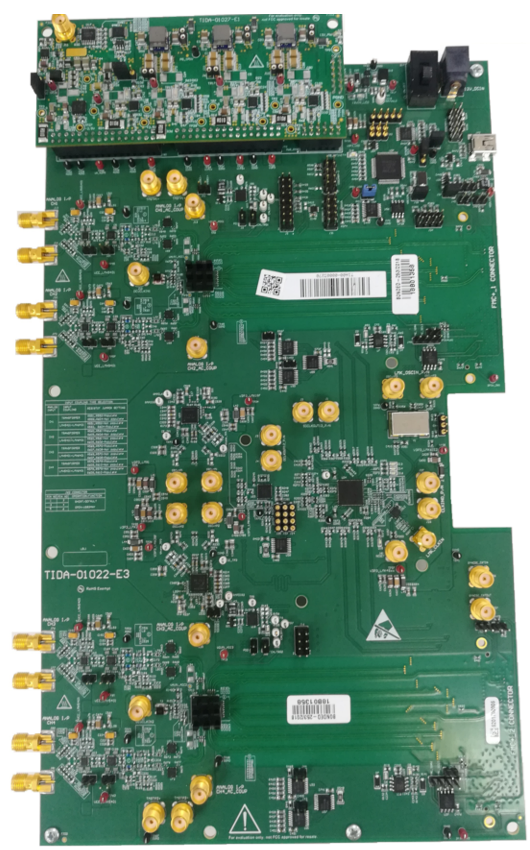


特性

- 采用时序交错 12 位射频采样 ADC，采样率高达 12.8GSPS
- 高达 6GHz 带宽的模拟前端支持
- 出色的采样时钟相位调整（19fs 分辨率）
- 多个 ADC 的相位同步
- 输入电压为 12V 时，配套电源参考设计的效率高于 85%
- JESD204B 支持 8 个、16 个或 32 个 JESD 通道，每通道的数据速率高达 12.8Gbps
- 包含与 TI 的 TSW14J57EVM 采集卡兼容的 FMC+ 连接器

应用

- 高性能示波器 (DSO)
- 高速数字转换器 (DAQ)



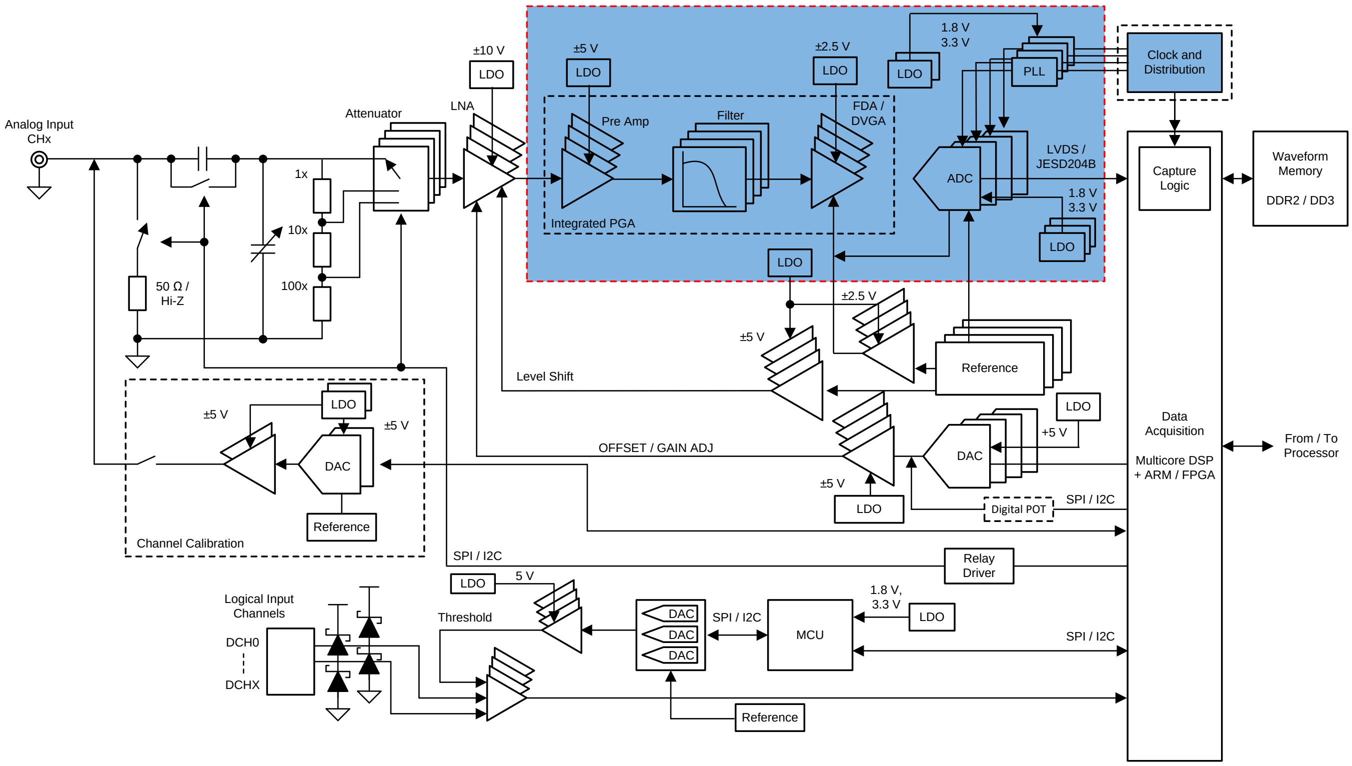
TIDUEI2 — http://www-s.ti.com/sc/techlit/TIDUEI2

该 TI 参考设计末尾的重要声明表述了授权使用、知识产权问题和其他重要的免责声明和信息。

1 System Description

图 1 and 图 2 show the subsystem block diagrams of the high-performance DSO and high-speed wideband DAQ, respectively. The analog front end (AFE) and system clocking architecture are similar for both applications and a number of similarities can be seen between these two.

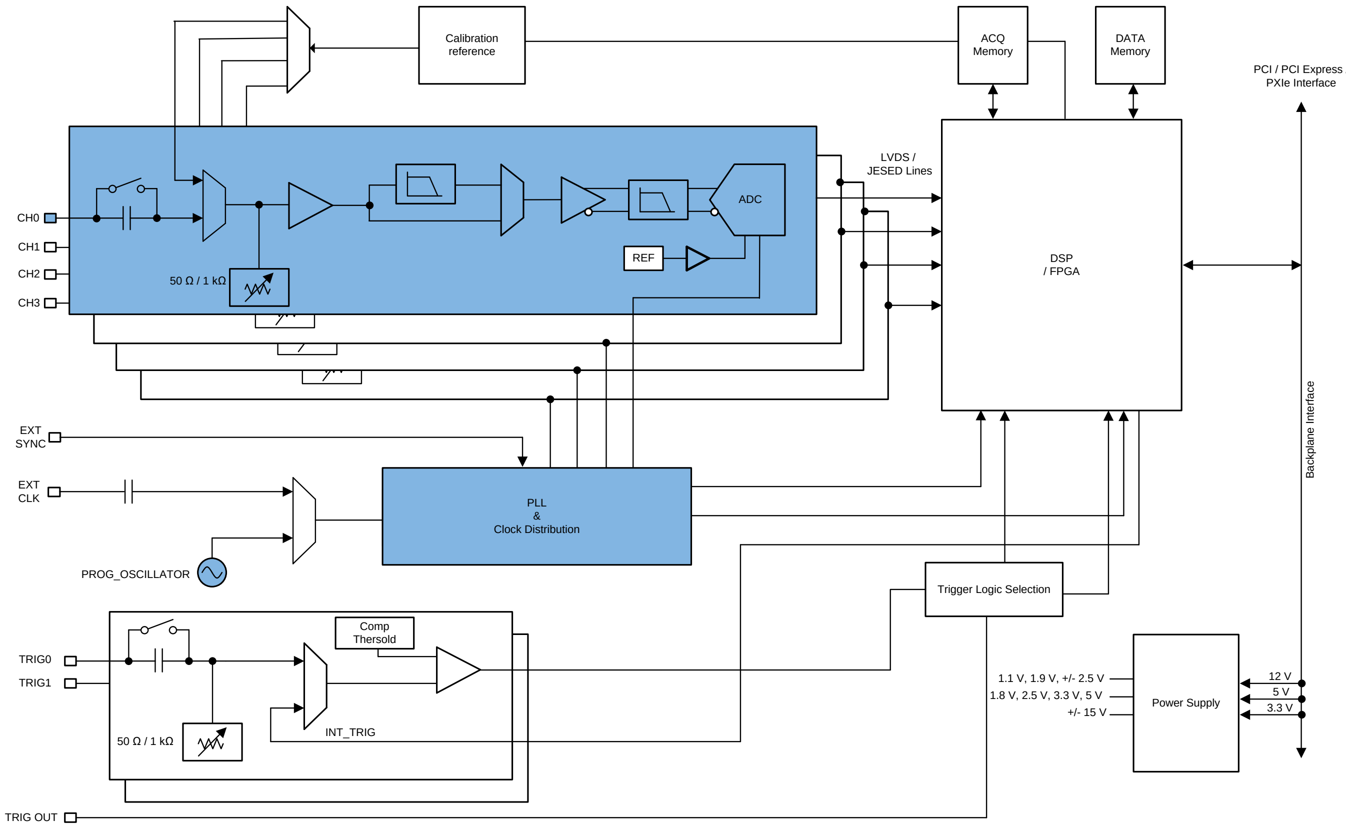
图 1. High-Performance DSO AFE Subsystem



High-performance multichannel digital storage oscilloscopes require a signal chain with a wideband AFE, high dynamic range (SFDR), high SNR, and low channel-to-channel skew. Most high-speed oscilloscopes use 8-bit vertical resolution for waveform visualization but technological development demands new generation scopes at 12- to 16-bit resolutions. The analog bandwidth in the order of the 200-MHz to 5-GHz range requires a sampling rate from 5 to hundreds of GSPS.

Typically, oscilloscopes have embedded wide displays and advanced triggering with the probing capability necessary for debugging and development for high-speed digital testing, high-speed serial protocols, and radar and wideband communication systems.

图 2. High-Performance DAQ AFE Subsystem



In contrast with digital oscilloscopes, high-speed wideband digitizers require a higher resolution and a wide dynamic range. Typically, these systems have a minimum level of front-end attenuation and their maximum input ranges are limited. The data captured is transferred to a controller via a high-speed, multi-lane PCIe bus or a high-speed SERDES interface. After post processing, results are displayed in the frequency domain. Most of the analysis is done in application software and displayed at the controller so there is no need for an embedded display which is used in an oscilloscope. The digitizer is a good choice for ATE applications and high-density multi-channel systems.

The addition of advanced triggering and user programmability enables the digitizer to be used as a wideband oscilloscope and vice versa.

The ADC is the main component limiting the performance of the system. Single ADC cores with higher sample rates and wider bandwidths require large investments. However, time interleaving multiple ADCs help achieve a higher sample rate with lower cost. Precise multi-channel clock-phase alignment capability and ADC channel characteristic matching is required to reduce interleaving errors and achieve the required system ENOB.

This TI design helps to address onboard time interleaving ADC design challenges and demonstrates how to minimize timing errors to achieve system SNR, SFDR, and ENOB performance.

1.1 Key System Specifications

表 1 lists the key system level specifications for the TIDA-01028 board.

表 1. Key System Specifications

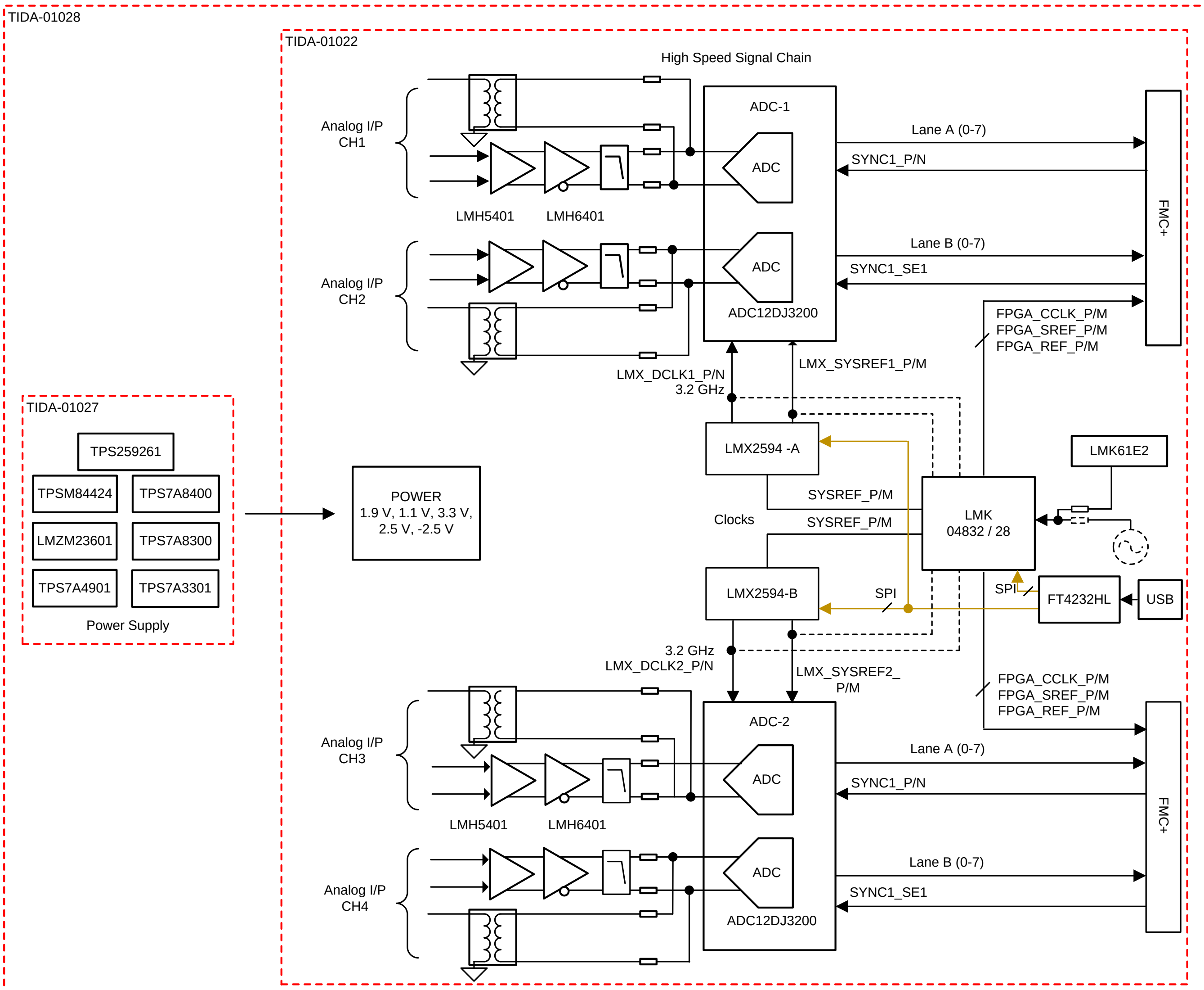
PARAMETER	SPECIFICATIONS			DETAILS
Input channels	2 channels (On-chip interleaving)			
	1 channel (Onboard interleaving)			
Input type	Single ended			
Input impedance	50 Ω			
Input analog bandwidth (–3 dB)	Transformer input			
	6 GHz			
Maximum sample rate	6.4 GSPS – 2 channels			节 3.4.3
	12.8 GSPS – 1 channel			
Resolution	12 bit			
System performance (–1 dB full scale) FS = 12.8 GHz	SNR	SFDR	ENOB	
	54.9 dB at 797 MHz	68.8 dB at 797 MHz	8.8 bits at 797 MHz	
	55.0 dB at 997 MHz	63.5 dB at 997 MHz	8.7 bits at 997 MHz	
	54.4 dB at 1497 MHz	67.6 dB at 1497 MHz	8.7 bits at 1497 MHz	节 3.4.3
Connectors	560 pin FMC+ interface connector support TSW14J57 high-speed capture card			
Power	12 V DC, 4 A			表 6
Form factor (L × W)	295 mm x 176 mm			

2 System Overview

2.1 Block Diagram

图 3 shows the system-level block diagram of the TIDA-01028 design, which was developed using the hardware from the *Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems (TIDA-01022)* along with the *Power Reference Design Maximizing Signal Chain ENOB in Very High Speed DAQ systems (TIDA-01027)*.

图 3. TIDA-01028 System Block Diagram



2.2 System Design Theory

In both high-speed oscilloscopes and digitizers, the total system performance is determined by the core ADC, jitter introduced by the clocking solution, and the analog front end signal chain, typically containing input attenuators, amplifiers, and filter blocks. To maximize system ENOB, the error sources from these companion devices must be minimized. These error sources and their impact are analyzed in the following sections.

2.2.1 Noise Sources and Coupling Path

Given an ideal data converter, the maximum SNR is determined by the quantization noise of the ADC as represented by 公式 1:

$$SNR_{QUANT} = 6.02 \times B + 1.76\ (dB) \tag{1}$$

图 4. ADC Noise Sources

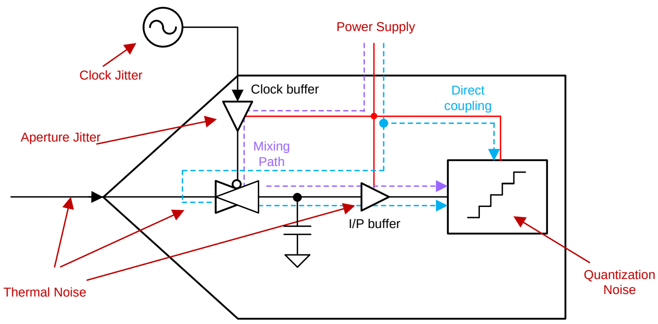


图 5. Spur due to Power-Supply Noise Coupling

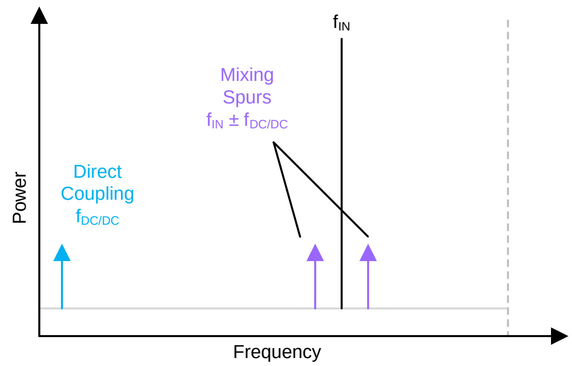


图 4, illustrates the typical noise sources degrading converter performance are thermal noise, converter aperture jitter, clocking jitter, and the quantization noise of the converter itself. Furthermore, power supply noise can be directly coupled or mixed with the input signal as 图 5 shows.

Total SNR is calculated with the sum of the individual noise sources:

$$SNR_{total} = 10\ \log\left(\frac{1}{10^{-\frac{SNR_{QUANT}}{10}} + 10^{-\frac{SNR_{JITTER}}{10}} + 10^{-\frac{SNR_{THERM}}{10}}}\right)$$

where

- SNR_{QUANT} = SNR due to quantization
- SNR_{JITTER} = SNR due to clock and aperture jitter
- SNR_{THERM} = SNR due to thermal and transistor noise (2)

图 6 shows SNR impact due to clock jitter (external clock jitter + internal ADC aperture jitter) which is calculated based on 公式 3:

$$SNR_{JITTER}[dB] = -20\log(2\pi \times F_{IN} \times T_{JITTER}) \tag{3}$$

图 6. SNR Impact of Clock Jitter

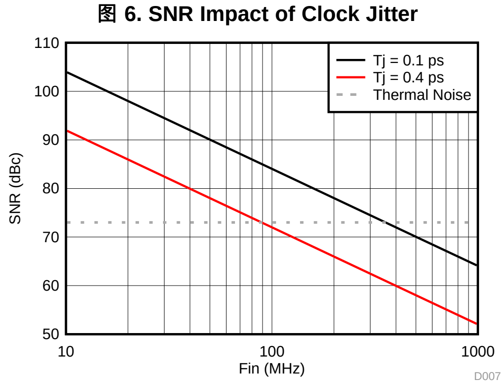


图 7. Resultant SNR due to Jitter and Thermal Noise

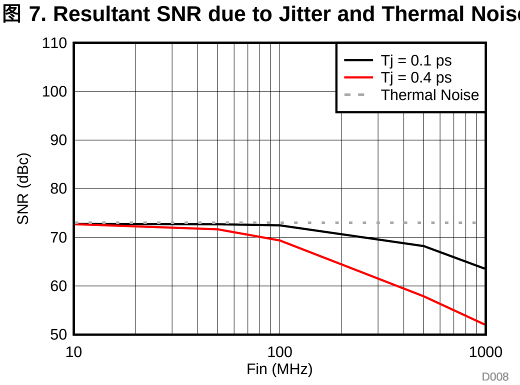


图 7 shows the resultant SNR plot due to clock jitter and thermal noise source calculated in 公式 2, SNR degrades due to noise source with increasing input signal frequency.

Also the front end noise, harmonic distortion, and interleaving distortion further reduce the effectiveness of system performance

2.2.2 Interleave Design Challenges

To achieve higher sample rates, multiple ADCs are time interleaved into a single or composite ADC. Each ADC is sampled at the same time period with equally-spaced time intervals and then the captured data is formatted to achieve higher sample rates. To achieve accurate sampling, the individual ADCs offset, gain, and phase between ADCs should be exactly matched. However, in practical terms this is not possible and mismatch must be managed and minimized, otherwise system performance is degraded by the introduction of interleaving spurs.

图 8. 2× ADC Interleaved Non-Ideal ADC

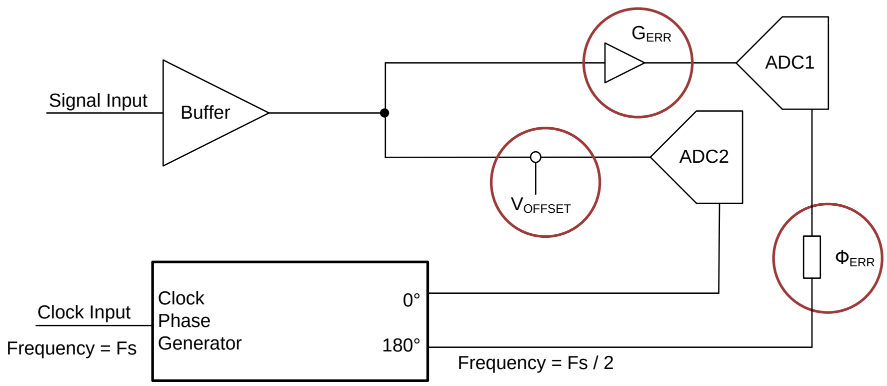


图 8 shows a two-ADC interleaved system with typical error sources like offset error, gain error, and time mismatch error between two ADCs which generate predictable spurs in the spectrum of the system.

2.2.3 Offset, Gain, Time Mismatch

Offset mismatch between the input buffer of the ADC, signal chain components like input amplifiers and attenuators create spurs at the DC, Fs/4, and Fs/2 location in the spectrum.

Gain mismatch between the ADC input buffer and input signal chain will create spurs at ±Fin, + Fs/4, and –Fin +Fs/2.

Similar to gain mismatch, time mismatch will also create spurs at ±Fin + Fs/4, and –Fin +Fs/2.

图 9. Spectrum due to Offset Error

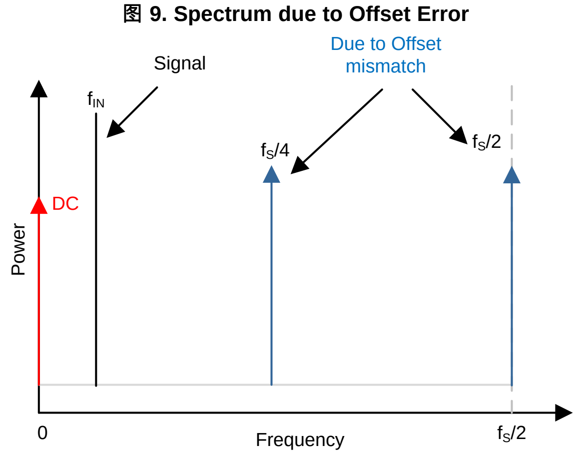


图 10. Spectrum due to Gain Error

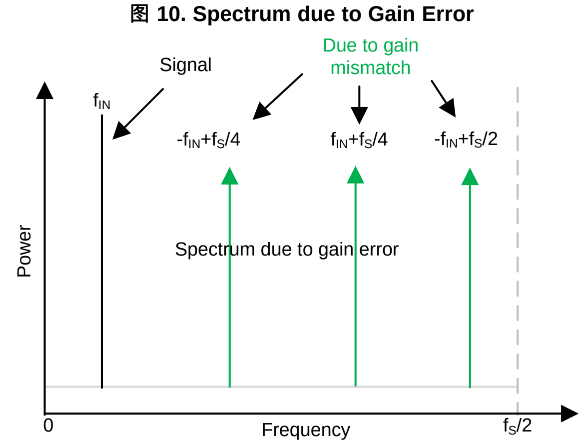


图 11. Spectrum due to Time Mismatch

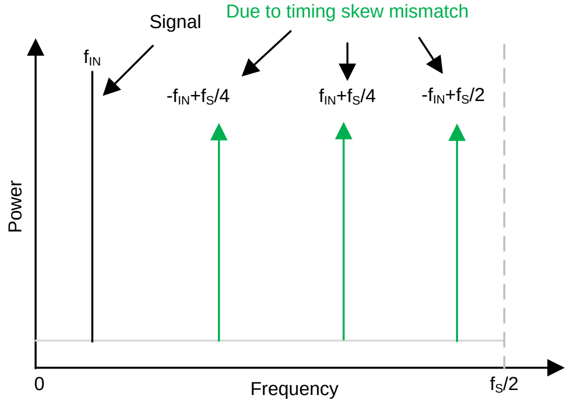


图 12. Resultant Spectrum due to Offset, Gain, Time Mismatch and Power-Supply Noise Coupling

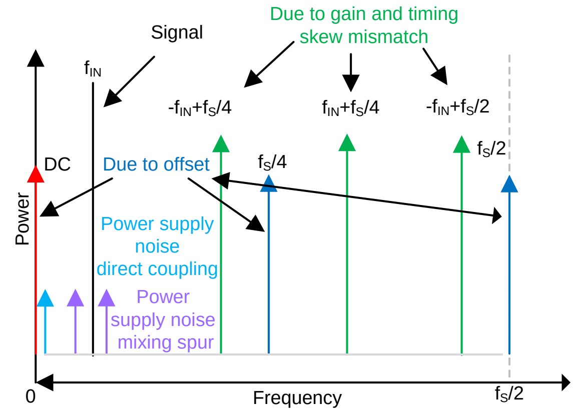
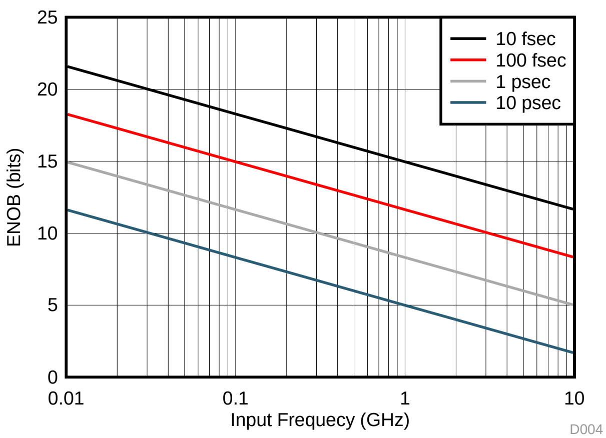


图 13 shows how the system ENOB performance changes with clock skew variations and how it depends on input signal frequency. 公式 5 shows that the system ENOB calculation is based on SNR which decreases as a square of clock skew and input-signal frequency.

$$ENOB = \frac{(SNR - 1.76)}{6.02} \; [Bits] \quad (4)$$

$$SNR = \frac{3}{2\pi^2 \Delta T^2 f^2_{sig}} \quad (5)$$

图 13. ENOB vs Input Frequency, Skew

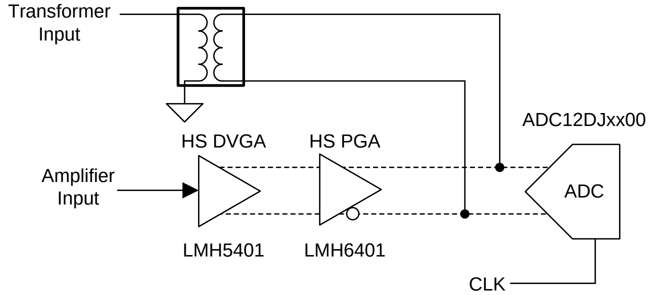


2.3 Circuit Design

2.3.1 Analog Input Front End

图 14 shows the analog front end circuit of the TIDA-01022. A flexible analog input allows validation of the system performance with two different input paths; each input can accept the signal from either the transformer or the amplifier chain, based on hardware jumper selection. All channels are well matched in terms of path delay, clock routing, and so forth.

图 14. TIDA-01022 Analog Front End



The transformer inputs are designed with Marki™ Microwave Balun BAL-0006SMG parts, which support an input signal of 500 kHz to 6 GHz. The amplifier input path supports frequencies from DC to approximately 1.5 GHz. Detailed circuit information is found in *Flexible 3.2-GSPS Multichannel AFE Reference Design DSOs, RADAR, and 5G Wireless Test Systems*, the TIDA-01022 design guide.

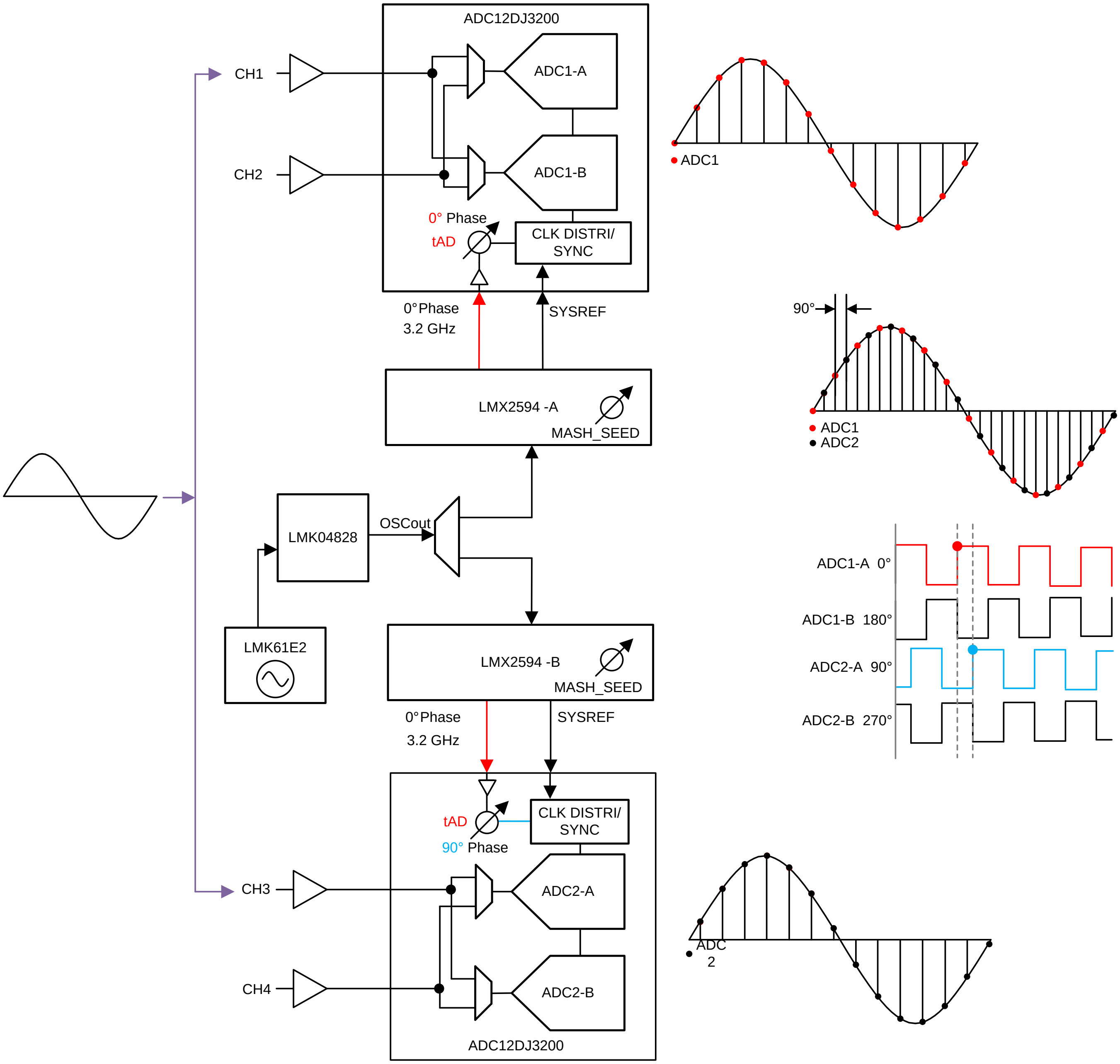
2.3.2 High-Speed Multi-Channel Clocking With Programmable Clock Phase

The TIDA-01022 hardware has a flexible clocking platform which helps designers validate system performance with various clocking source options. The default onboard clocking solution uses the LMX2594 clock synthesizer which has excellent phase noise at high frequency. A clock distribution chip, the LMK04828 device, is used to provide the reference signal to LMX2594, FPGA DCLK, FPGA_CORECLK, and FPGA_SYSREF.

2.3.2.1 Interleave Clock Requirement

图 15 shows the clock architecture of the TIDA-01022 design and the timing relation that can be used to interleave the onboard ADCs (ADC12DJ3200).

图 15. TIDA-01028 Interleave Clock Architecture



The ADC_SYSREF, FPGA_CORECLK, FPGA_REFCLK, and FPGA_SYSREF to be calculated based the ADC device clock (ADC_DEVCLK) requirement and SERDES lanes used for capture.

To achieve a 12.8-GSPS sample rate, the following clocks were generated by the onboard clocking solution provided in this design.

ADC_DEVCLK = 3.2 GHz; to operate ADC in 6.4 GSPS single-channel mode

ADC_SYSREF =40 MHz

FPGA_CORECLK = 320 MHz

FPGA_REFCLK = 320 MHz

FPGA_SYSREF = 40 MHz

SERDES lane rate = 8

Both the LMX2594-A and LMX2594-B devices are configured to generate 3.2 GHz at RFOutA for DEVCLK and 40 MHz at RFOutB for SYSREF from the 40-MHz reference at the OSCin input which is connected to the OSCout of the LMK04828 device via the LMK00304 clock buffer.

The LMK04828 device is used to provide the required FPGA clocks. 表 2, 表 3, and 表 4, show the signal definitions and clock output frequency.

表 2. LMK04828 Clock Definition for TIDA-01028

Slno	LMK04828 SIGNALS	FREQUENCY OUTPUT	REMARKS
1	OSCout p/n	40 MHz	Connected to LMX2594 reference input for generation ADC DEVCLK and SYSREF
2	DCLKOUT0 p/n	-	Not used
3	SDCLKOUT1 p/n	-	Not used, LMX SYSREF or LMX SYSREFREQ
4	DCLKOUT2 p/n	-	Not used
5	SDCLKOUT3 p/n	-	Not used, LMX SYSREF or LMX SYSREFREQ
6	DCLKOUT4 p/n	320 MHz	FPGA_REF CLK, connected slave to capture FPGA
7	SDCLKOUT5 p/n	-	SYNC signal to LMX2594-B
8	DCLKOUT6 p/n	320 MHz	FPGA_CORE CLK, connected slave to capture FPGA
9	SDCLKOUT7 p/n	40 MHz	FPGA_SYSREF, connected slave to capture FPGA
10	DCLKOUT8 p/n	320 MHz	FPGA_CORE CLK, connected master to capture FPGA
11	SDCLKOUT9 p/n	40 MHz	FPGA_SYSREF, connected master to capture FPGA
12	DCLKOUT10 p/n	320 MHz	FPGA_REF CLK, connected master to capture FPGA
13	SDCLKOUT11 p/n	-	SYNC signal to LMX2594-A
14	DCLKOUT12 p/n	-	Not used
15	SDCLKOUT13 p/n	-	Not used

表 3. LMX2594-A Clock Definition for TIDA-01028

Slno	LMX2594-A	FREQUENCY OUTPUT	REMARKS
1	OSCin p/n	40 MHz	Connected to OSCout p/n of LMK04828
2	RFoutA p/n	3200 MHz	Connected to ADC-1 device clock input
3	RFoutB p/n	40 MHz	Connected to ADC-1 SYSREF input

表 4. LMX2594-B Clock Definition for TIDA-01028

Slno	LMX2594-B	FREQUENCY OUTPUT	REMARKS
1	OSCin p/n	40 MHz	Connected to OSCout p/n of LMK04828
2	RFoutA p/n	3200 MHz	Connected to ADC-2 device clock input
3	RFoutB p/n	40 MHz	Connected to ADC-2 SYSREF input

Once all the clocks are generated, a 90° phase difference between the two ADC channels can be established with the following procedure.

The TICSPro GUI helps to create the configuration files for the LMK61E2, LMK04828, and LMX2594 devices. Download the latest *High-Speed Data Converter* (HSDC) TID GUI software from: http://www.ti.com/tool/TICSPRO-SW.

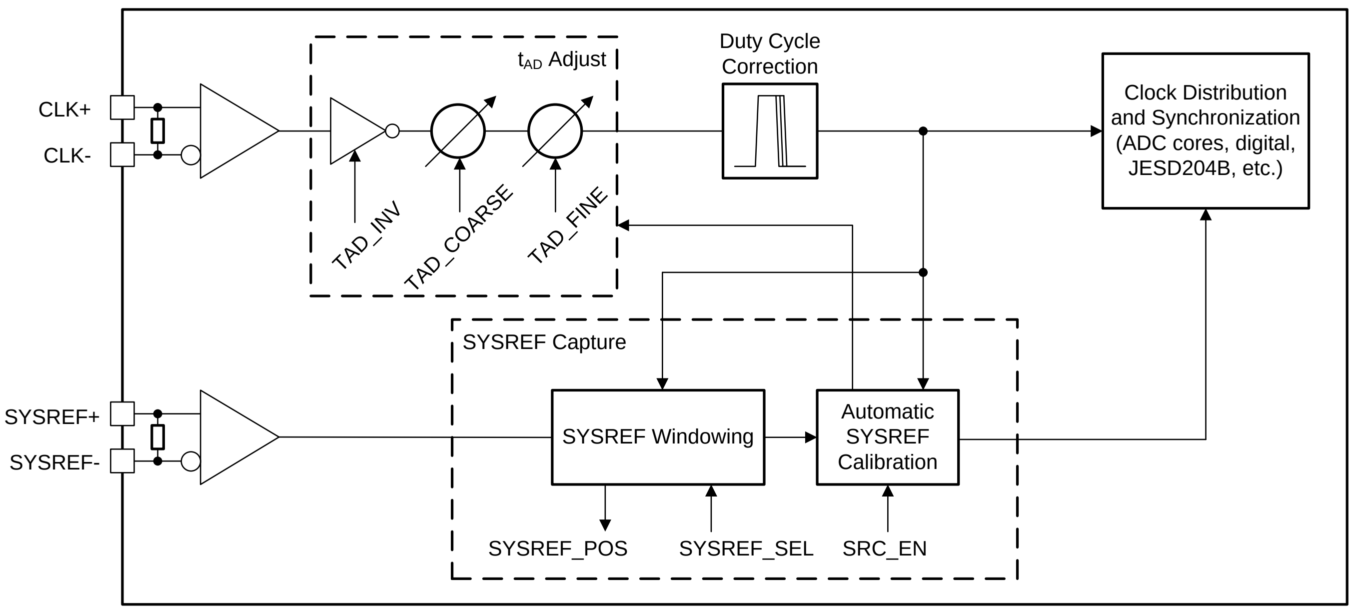
2.3.2.2 Establishing 90-Degree Phase Alignment

The TIDA-01022 hardware has a flexible clocking solution with a number of clocking options to allow users to validate system performance with various clocking configurations. One clocking option in this reference design is selected which satisfies the interleaving design clocking requirements. This clocking solution provides flexibility to adjust the clock delay in three places in the clocking path. This delay can be done on the LMK04828 output, LMX2594 output, the ADC12DJ3200, or a combination of these devices.

The LMK04828 device has both analog and digital delay elements in each clock output. The LMX2594 has a MEASH SEED register that can tune the delay in 9-ps increments and the ADC12DJ3200 device has *Noiseless Aperture Delay Adjustment* (t_{AD} adjust) features on the device clock path that can be used to shift the sampling instant in 19-fs steps.

图 16 shows the internal clock subsystem of ADC12DJ3200 and highlights t_{AD} components (TAD_INV, TAD_COARSE, and TAD_FINE). These registers allow maximum aperture delay adjustment up to $t_{AD(max)}$ = 293 ps and ultra-low aperture jitter $t_{AD(max)}$ = 70 fs to satisfy the low-phase noise requirements.

图 16. ADC12DJ3200 Clocking Subsystem



This t_{AD} feature gives the flexibility to adjust any one or both registers of the ADC to make 90° phase shift between ADCs with 19-fs resolution.

公式 6 helps to calculate the required phase delay between ADCs:

$$t_{PHASEDELAY} = \frac{t_{SAMPLECLK} \times Req\_phase}{360} \quad (6)$$

where

- $t_{SAMPLECLK}$; device clock time period . 1/Fs
- Reg_Phase; required phase shift between two ADCs
- $t_{PHASEDELAY}$; phase delay between two ADCs

To interleave the two ADC12DJ3200s onboard, a 90° phase shift between ADC clocks is required by using 公式 6 for a 3.2-GHz device clock:

$$t_{SAMPLECLK} = \frac{1}{3200,000,000\ Hz} = 312.5ps \quad (7)$$

$$t_{PHASEDELAY} = \frac{312.5 \times 10^{-12} \times 90 = 78.1ps}{360} \quad (8)$$

After SYSREF calibration, the calibrated SYSREF values are loaded to the corresponding t_{AD} register:

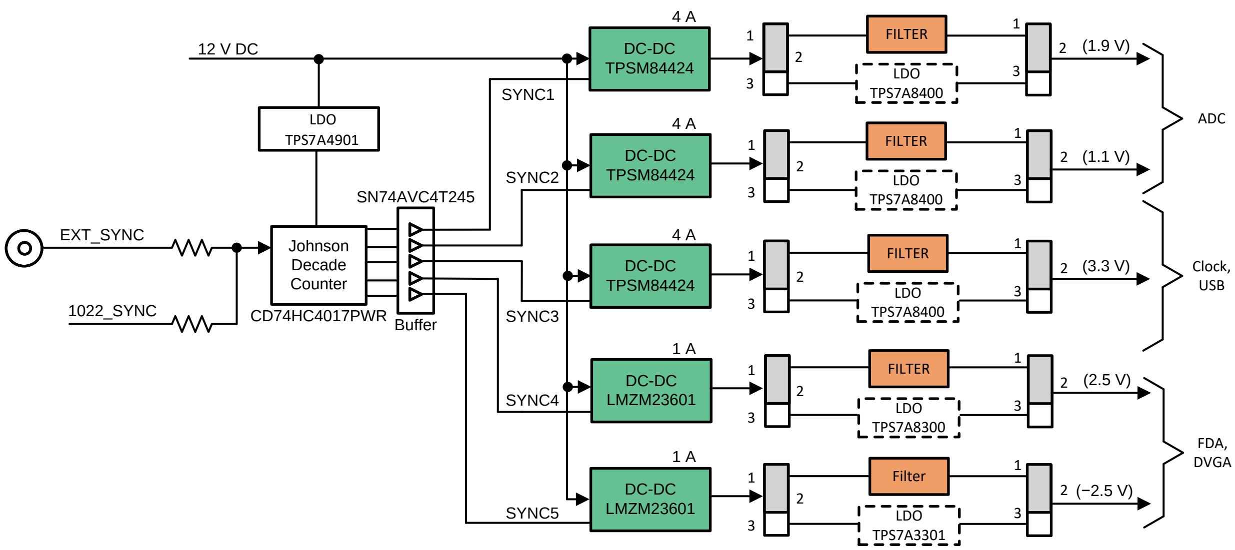
1. Enable SYSREF calibration and check for SYSREF calibration done bit in the 0x2B4 register
2. Load the SYSREF calibrated values of the coarse(0x2B6) and fine(0x2B5) register with the corresponding t_{AD} registers 0x2B3, 0x2B2 after SYSREF calibration is done
3. Disable the SYSREF calibration
4. Fine-tune the t_{AD} register for 90° (78.1 ps) phase delay between ADC1 and ADC2

2.3.3 Power Tree

This TI design uses a high-performance, optimized power solution from the TIDA-01027 reference design. This power module satisfies the power requirements of the TIDA-01022. The module contains both DC/DC and LDO regulators with an external frequency SYNC feature for synchronization of multiple switching regulators. Also a method of clock phase shifting enables users to reduce both conducted and radiated EMI.

图 17 shows the TIDA-1027 power tree. The module provides 3.3-V, 1.9-V, 1.1-V, 2.5-V and –2.5-V rails to various analog and digital sections of the TIDA-01022.

图 17. TIDA-01027 Power Tree



For more information, see the *Power Reference Design Maximizing Signal Chain ENOB in Very High Speed DAQ Systems* reference design (TIDA-01027).

2.4 Highlighted Products

2.4.1 ADC12DJ3200 - 12-Bit, Dual 3.2- GSPS or Single 6.4- GSPS, RF- Sampling ADC

The ADC12DJ3200 device is an RF-sampling giga-sample ADC that can directly sample input frequencies from DC to above 10 GHz. In dual-channel mode, it can sample up to 3200-MSPS and in single channel mode up to 6400-MSPS, full power input bandwidth (–3 dB) of 8.0 GHz, with usable frequencies exceeding the –3 dB point in both dual- and single-channel modes, allows direct RF sampling of the L-band, S-band, C-band and X-band for frequency agile systems.

2.4.2 Why choose the ADC12DJ3200? Key Features

The ADC12DJ3200 device has an integrated Noiseless Aperture Delay (tAD) Adjustment feature which allows us to shift clock instants in fine steps (19 fs) to achieve 90 degree phase between two ADCs for Time Interleave sampling.图 16 shows the ADC12DJxx00 family internal clocking subsystem.

- Automatic SYSREF calibration, uses the tAD Adjust feature to shift the device clock to maximize the SYSREF setup and hold times or align the sampling instance based on the SYSREF rising edge.
- SYSREF Position Detector and Sampling Position Selection (SYSREF Windowing) The SYSREF windowing block is used to first detect the position of SYSREF relative to the CLK± rising edge and then to select a desired SYSREF sampling instance, which is a delay version of CLK±, to maximize setup and hold timing margins.

In addition to these features, this device family offers various sampling rates starting from 1600 MHz to 5200 MHz and 8 to 12 bits of resolution with the same pinout. It allows customers the flexibility to change the data convertor speed and resolution based on their applications with the same printed circuit board (PCB). Also, there no need for much hardware and software development.

In addition to the aperture adjustment, some of the key specifications taken into account include SNR, ENOB, and so forth – other similar devices considered are listed in 表 5.

表 5. ADC12DJ3200 - Similar Devices

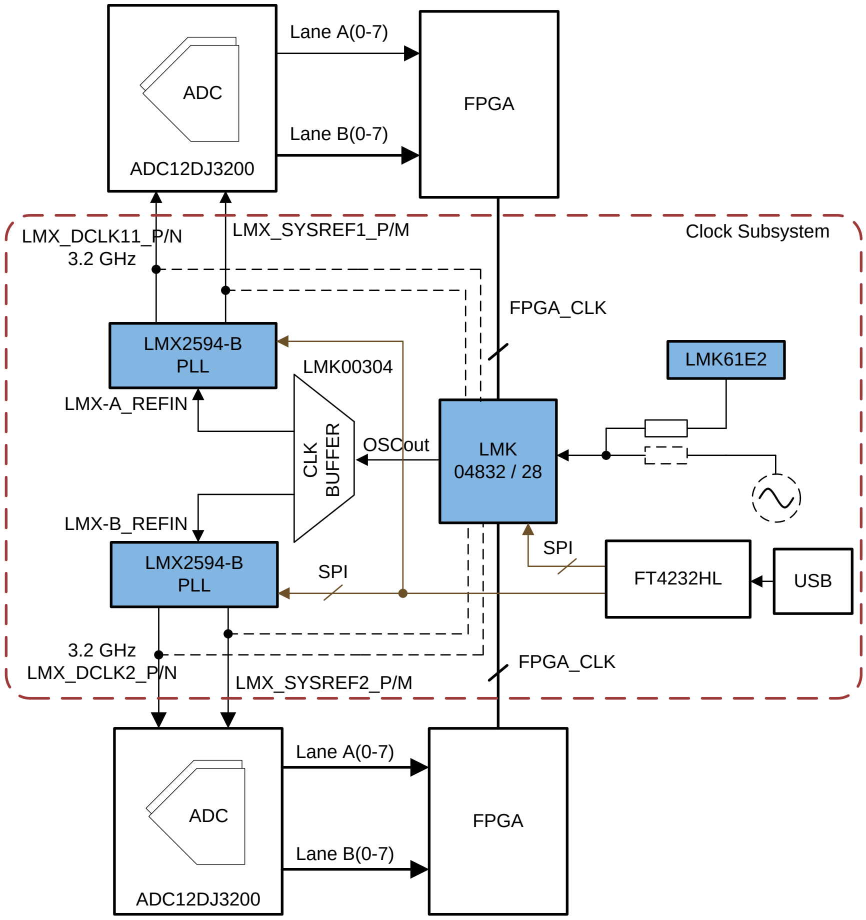
	ADC08DJ3200	ADC12DJ2700	ADC12DJ3200	ADC12J2700	ADC12J4000	ADC12J1600
	Samples & Orders	Samples & Orders	Samples & Orders	Samples & Orders	Samples & Orders	Samples & Orders
	Online Data Sheet	Online Data Sheet	Online Data Sheet	Online Data Sheet	Online Data Sheet	Online Data Sheet
	Data Sheet	Data Sheet	Data Sheet	Data Sheet	Data Sheet	Data Sheet
	Tools & Software	Tools & Software	Tools & Software	Tools & Software	Tools & Software	Tools & Software
Sample Rate (Max) (MSPS)	3200	2700	3200			
	6400	5400	6400	2700	4000	1600
Resolution (Bits)	8	12	12	12	12	12
Number of input channels	2	2	2			
	1	1	1	1	1	1
Interface	JESD204B	JESD204B	JESD204B	JESD204B	JESD204B	JESD204B
Analog input BW (MHz)	8000	8000	8000	3300	3300	3300
Features	Ultra High Speed	Ultra High Speed	Ultra High Speed	Ultra High Speed	Ultra High Speed	Ultra High Speed
SNR (dB)	49.1	56.7	56.6	55	55	55
ENOB (Bits)	7.8	9	9	8.8	8.8	8.8
SFDR (dB)	67					
	62	71	67	71	71	70
Power consumption (Typ) (mW)	2800	2700	3000	1800	2000	1600
Input range (Vp-p)	0.8	0.8	0.8	0.725	0.725	0.725
Operating temperature range (C)	-40 to 85	-40 to 85	-40 to 85	-40 to 85	-40 to 85	-40 to 85
Input buffer	Yes	Yes	Yes	Yes	Yes	Yes
Package Group	FCBGA | 144	FCBGA | 144	FCBGA | 144	VQFN | 68	VQFN | 68	VQFN | 68
Package size: mm^2: W x L (PKG)	See data sheet (FCBGA)	See data sheet (FCBGA)	See data sheet (FCBGA)	68 VQFN: 100 mm^2: 10 x 10 (VQFN | 68)	68 VQFN: 100 mm^2: 10 x 10 (VQFN | 68)	68 VQFN: 100 mm^2: 10 x 10 (VQFN | 68)

2.4.3 LMK04828- Ultra Low Noise JESD204B Compliant Clock Jitter Cleaner

The LMK0482x family is the highest performance clock conditioner with JESD204B support in the industry. The 14 outputs from PLL2 can drive up to seven JESD204B data convertors or other logic devices like FPGA. The device has both analog and digital delay in each clock output path and analog delay can be adjusted 25-ps fine steps.

图 18 shows by combining both LMK04828 and LMX2594 , we can create high-performance, low-noise clocking subsystems that drive giga-sample speed data convertors with JESD204B support.

图 18. Giga Sample Clocking Solution With LMX2594 + LMK04828



2.4.4 LMX2594- 15 GHz Wideband PLLatinum™ RF Synthesizer

The LMX2594 device is a high-performance, wideband PLL with integrated VCOs that can generate frequencies from 10 MHz to 15 GHz without using an internal doubler. The high-performance PLL with a figure of merit of –236 dBc/Hz and high-phase detector frequency can attain very low in-band noise and integrated jitter.

The LMK2594 device is an ideal companion part for the ADC12DJxx00 family. The LMK2594 generates a very low noise clock for high-speed data convertor and generates repeating SYSREF which is compliant with the JESD204B standard.

2.4.5 LMK61E2- Ultra-Low Jitter Fully-Programmable Oscillator

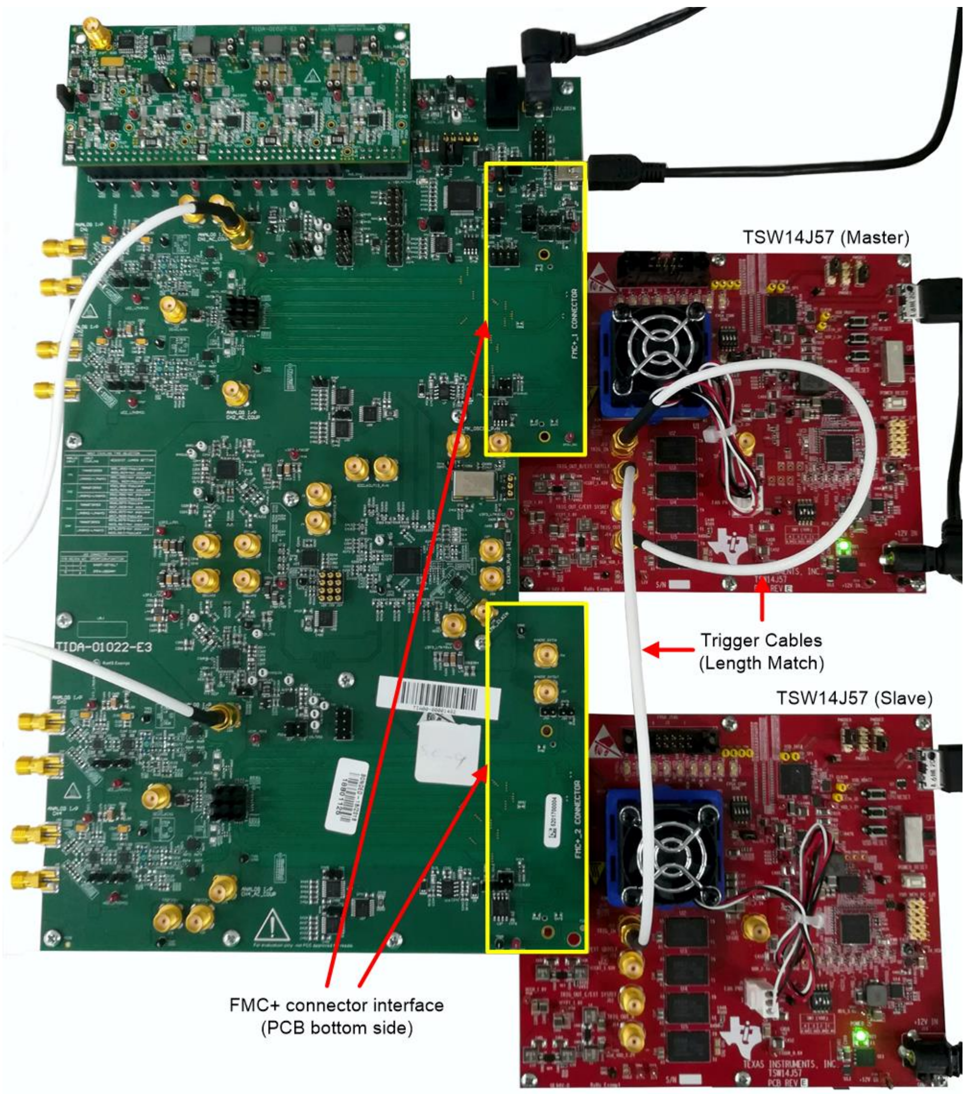
The LMK61E2 device is an ultra-low jitter PLLatinum™ programmable oscillator with a fractional-N frequency synthesizer with integrated VCO that generates commonly-used reference clocks. The outputs can be configured as LVPECL, LVDS, or HCSL. The device offers ultra-low jitter, as low as 90-fs RMS and the maximum clock output can generate up to 1 GHz with 50 ppm frequency stability. In this reference design, the LMK61E2 is used to provide a reference clock for the LMK04828.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Host Interface

The TIDA-01028 time interleaved system performance can be evaluated using TI's TSW14J57 JESD204B High-Speed Data Capture and Pattern Generator Card. Populated with an Arria® 10 device and using the Altera® JESD204B IP solution, the TSW14J57 device can be dynamically configured to support all lane speeds from 1.6 Gbps to 15 Gbps - from 1 to 16 lanes. Together with the accompanying *High-Speed Data Converter Pro Graphic User Interface* (GUI), it is a complete system that captures and evaluates data samples from the TIDA-01022 reference design. The TIDA-01022 can be directly interfaced with the TSW14J57 device using the FMC+ connector interface. 图 19 shows the TIDA-01022 interface with the TSW14J57 capture module and trigger cable connection.

图 19. TIDA-01022 Interface With TSW14J57 Capture Module



For more information on the TSW14J57 EVM, see the *TSW14J57 JESD204B high-speed data capture and pattern generator card user's guide*.

3.2 Required Hardware and Software

3.2.1 Hardware Functional Block

图 20 shows the TIDA-01022 board with the TIDA-01027 power board.

For more information about hardware functional blocks and programming details, see TIDA-01022.

图 20. TIDA-01022 Hardware Functional Block

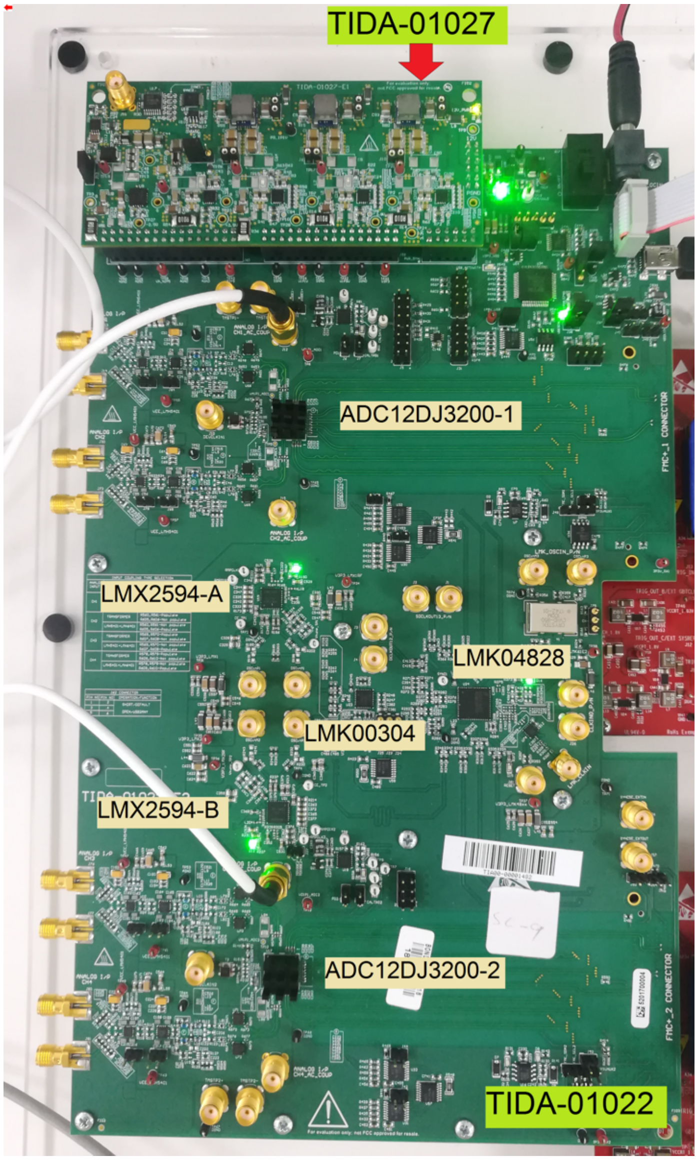


图 21 shows the TIDA-01027 board image, in this reference design the TIDA-01027 board is configured as DC/DC free running mode (default mode). The TIDA-01027 output connectors are made compatible with the TIDA-01022 power input headers J58, J59, J60, and J63.

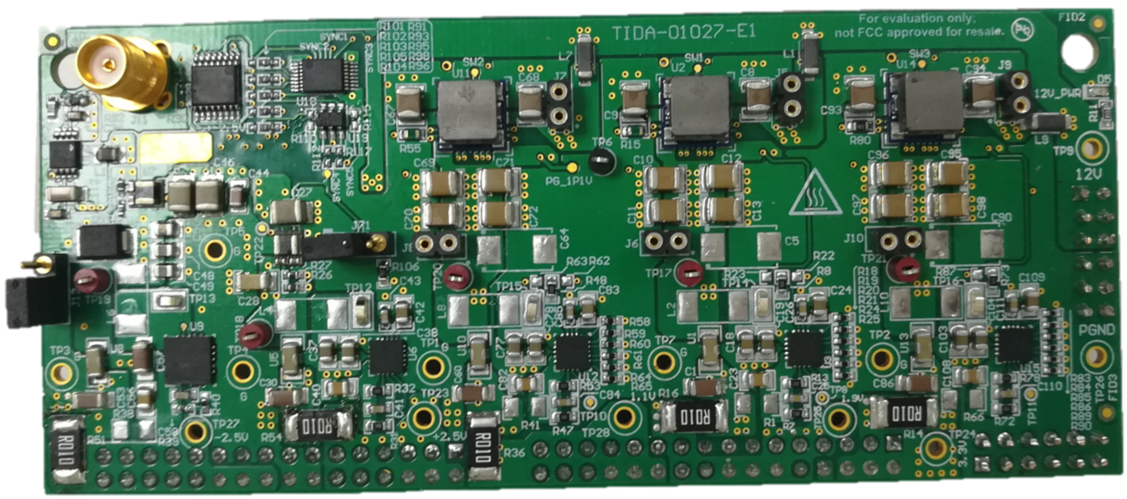
表 6 shows the input and output specification of the TIDA-01027 power supply module.

表 6. TIDA-01027 Key Specification

PARAMETER	SPECIFICATIONS
Input voltage range	5 V to 17 V
Number of outputs	5
Output voltage, Maximum output current	1.9 V, 4 A 1.1 V, 4 A 3.3 V, 4 A 2.5 V, 1 A –2.5 V, 800 mA
Efficiency	85%

The board can be connected as 图 20 shows.

图 21. TIDA-01027 Hardware Image



3.2.2 Getting Started Application GUI

The TIDA-01022 board requires three application software GUIs for validation: HSDC TID GUI, HSDC Pro GUI, and the LMK61xx Oscillator Programming Tool:

1. Use the HSDC TID GUI to configure the data converter (ADC12DJ3200), clocking devices (LMK4828, LMX2594, and LMK61E2), and digital VGA (LMH6401). Use the low-level page to program the device with the respective configuration file. Download the latest HSDC TID GUI software at:http://www.ti.com/lit/zip/tidcfb3.
2. Use the HSDC Pro GUI to capture the digitized data with the assistance of a TSW14J56 capture card and provide a spectrum and time domain plot. Download the latest HSDC Pro GUI software at: http://www.ti.com/tool/dataconverterpro-sw.
3. Use the LMK61xx Oscillator Programming Tool to program the LMK61E2 device. Download the latest LMK61xx software at http://www.ti.com/lit/zip/snac074.

图 22 and 图 23 show screen shots of starting the HSDC TID GUI configuration and the *Programming* tab for the low-level view, respectively.

图 22. HSDC TID GUI - Top-Level Navigation View

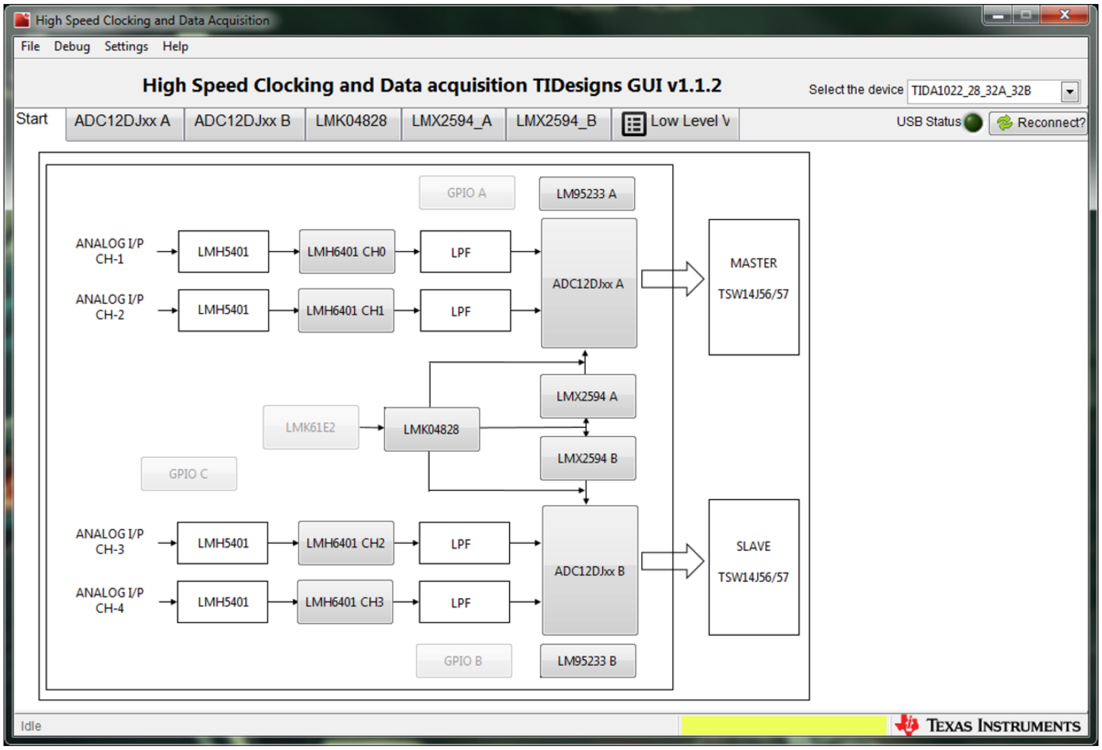


图 23. HSDC TID GUI - Low Level Programming View

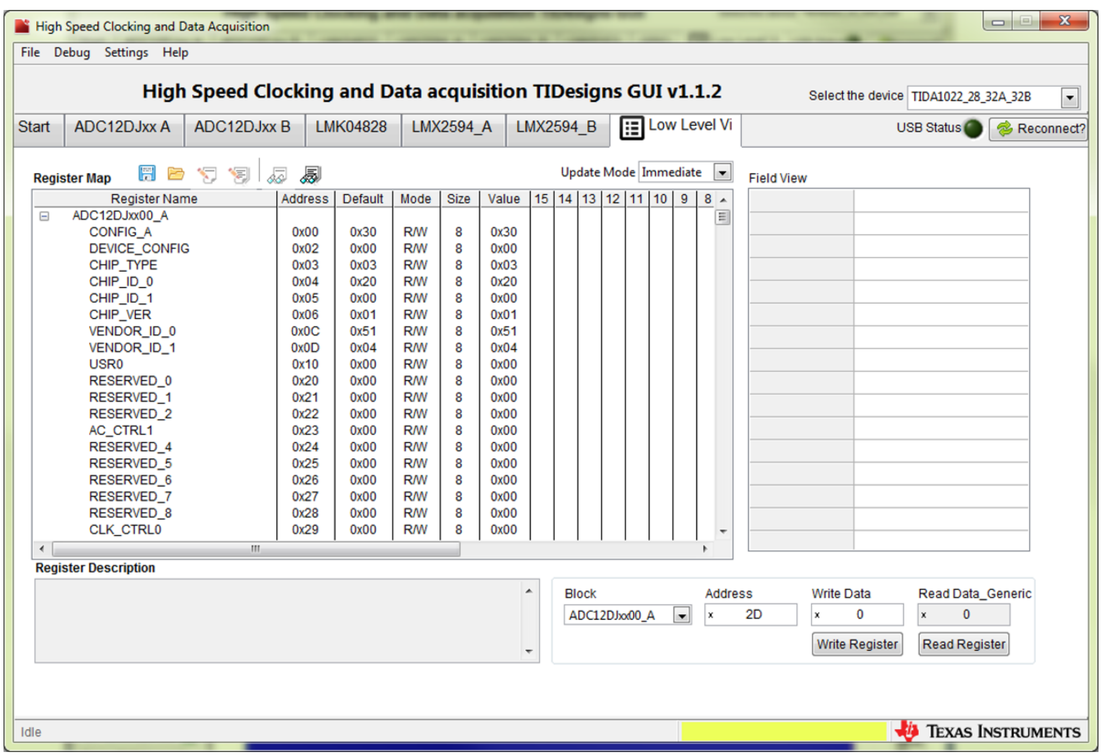
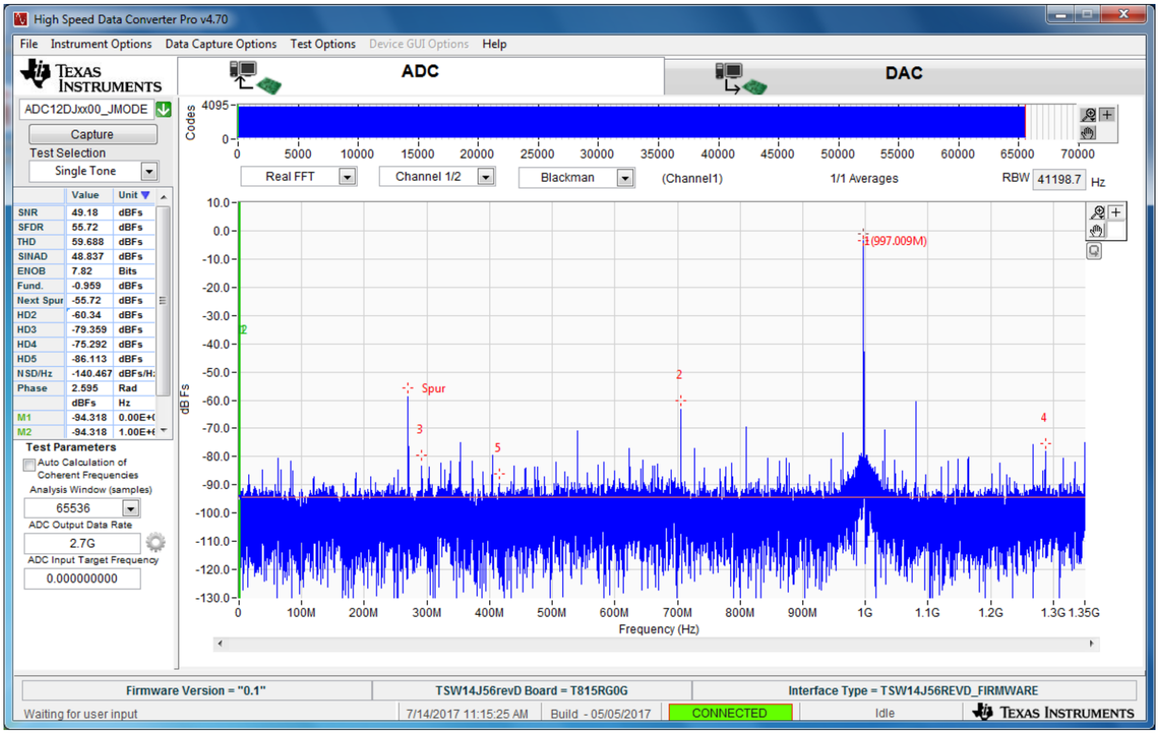


图 24 shows the ADC capture GUI, spectrum plot.

图 24. HSDC Pro ADC Capture GUI (Spectrum)



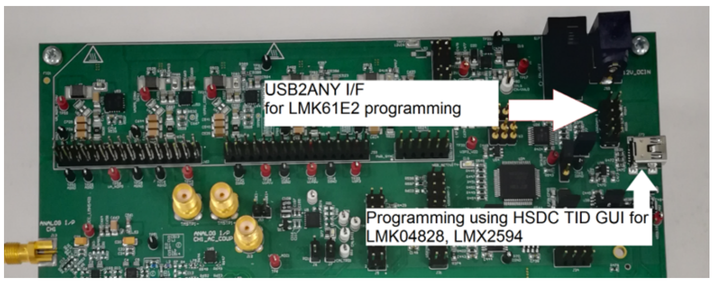
3.3 Hardware Programming

The TIDA-01022 hardware has an onboard FTDI-brand USB controller which is for programming the LMK61E2, LMK4828, and LMX2594 clocking devices and the LMH6401 amplifier using an SPI or I2C interface. The High-Speed Data Converter (HSDC TID) graphical user interface (GUI) supports low-level pages, which can be used to program these devices.

The board also features a USB2ANY programming interface which helps the user evaluate hardware by using the respective evaluation module (EVM) GUI.

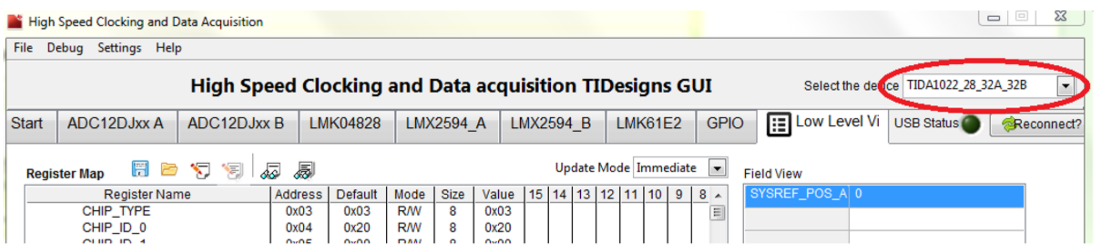
图 25 shows the location of programming connector.

图 25. Programming Connector Interface

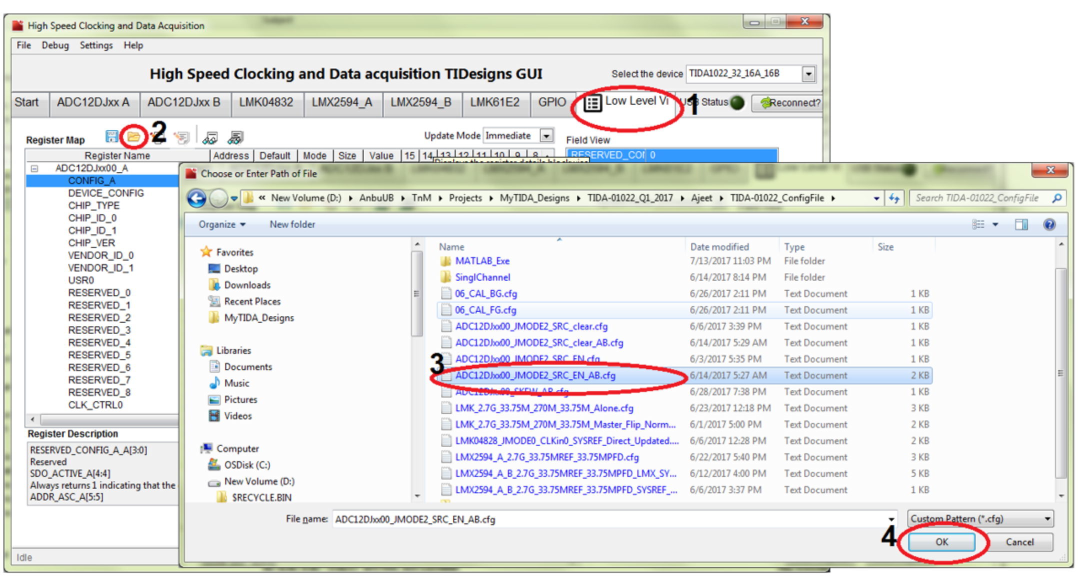


The programming procedure for the built-in programming interface follows:

1. Open the HSDC TID GUI and select the *TIDA1022_28_32A_32B* from the device selection drop-down menu.



2. Navigate to the *Low Level* tab, select the configuration files to be programmed, and click the *OK* button. Follow these steps as numbered and encircled in the following screen shot:

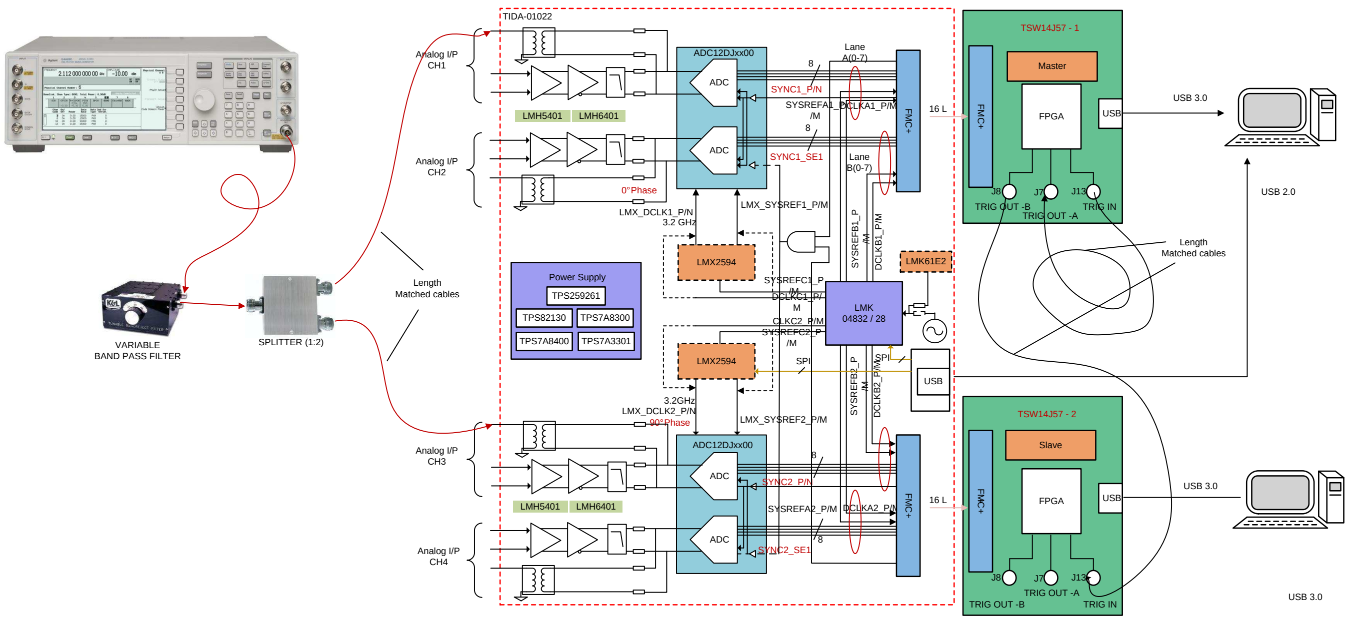


3.4 Testing and Results

3.4.1 Test Setup

图 26 shows the test setup for onboard time interleaving using the TIDA-01022 reference design with transformer input.

图 26. Test Setup for 2× ADC12DJ3200 Devices



3.4.2 Onboard Interleaving Measurement

1. Emulate the hardware setup as shown in 图 26, then provide the input signal to the J12 and J29 SMA connectors of channel 1 and 3 of the TIDA-01022 design through a variable band-pass filter and 2:1 splitter.
2. Connect a high-speed USB3.0 and USB2.0 cable to the capture PCs
3. Configure the TSW14J57 capture card as Master and Slave configuration mode
   a. Connect master TSW14J57,J7(TRIG OUT –A) to J13 (TRIG IN) using high-speed SMA cable for master self-triggering.
   b. Connect the master TSW14J57, J8 (TRIG OUT-B) to J13(TRIG IN) of slave TSW14J57 module using high-speed SMA cable.
4. Provide a 12-V, 4-A DC supply to the power connector (J55) of the TIDA-01022 and a 12-V supply to the TSW14J57 capture card.

注: As 图 26 shows, the length of cable must be length matched.

To measure the interleave performance, configure the following using the HSDC TID GUI:

1. Use the J32 connector to program the LMK61E2 device at 40 MHz using the USB2ANY programmer associated with the LMK61E2 Oscillator Programming Tool. Set the device address as 0x5A before programming.
2. Program the LMK04828 in 0-delay PLL mode at a 40-MHz SYSREF frequency to provide the SYSREFREQ and SYNC signals along with this 40-MHz OSCout as a reference to the LMX2594.
3. The LMK04828 also generates the FPGA reference at 320 MHz, the FPGA core clock at 320 MHz, and the FPGA SYSREF at 40 MHz for the FPGA capture card.
4. Program the LMX2594_A and LMX2594_B for a 3.2-GHz DEVCLK and SYSREF at 40 MHz.

5. Configure both ADC12DJ3200 JMODE-0 (single-channel mode) by loading the configuration file in the low-level page.

Establish the JESD204B link using the HSDC Pro GUI:

1. After powering the TSW14J57, establish a connection with the single-channel mode (JMODE0).
2. Provide the data rate sampling frequency of the ADC output as 6.4 GHz and the ADC input target frequency as 997 MHz.
3. After establishing the JESD204B connection, feed the input signal to channel 1 (J12) and channel 3 (J29).
4. Apply a trigger at the slave capture board and then click the capture button on the master board.
5. Export both ADC1 and ADC2 data, then extract the phase information from the spectrum using the MATLAB® program and plot the data in the time domain for a channel-to-channel skew measurement.
6. Adjust t_{AD} register values to make channel-to-channel skew as 78.1 ps for 90° phase clock shift between CH1 and CH3. See 节 2.3.2.2 for more details.
7. After establishing a 90° phase shift, combine both ADC1 and ADC2 data to form interleaved data for 12.8-GSPS sample rate.

3.4.3 Performance Test Result

In this reference design, interleaving performance is measured with Fs = 12.8 GSPS, Fin = 300 MHz to 6 GHz input signal frequency. 图 27 and 图 28 show the measured spectrum of the TIDA-01028 design at a 997-MHz input, 6.4-GSPS sample rate of ADC1 and ADC2 with 90 degree time-interval sampling.

图 27. ADC1 Spectrum 6.4 GSPS

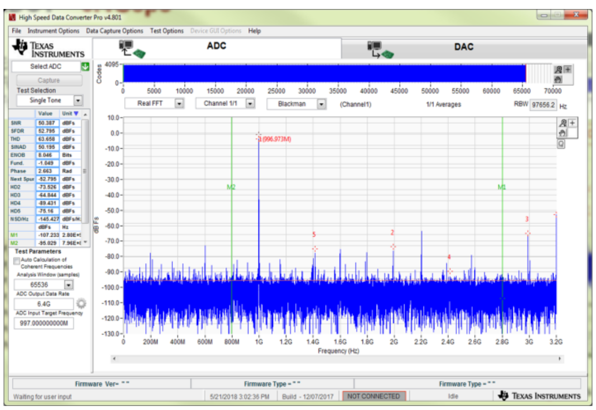


图 28. ADC2 Spectrum 6.4 GSPS 95

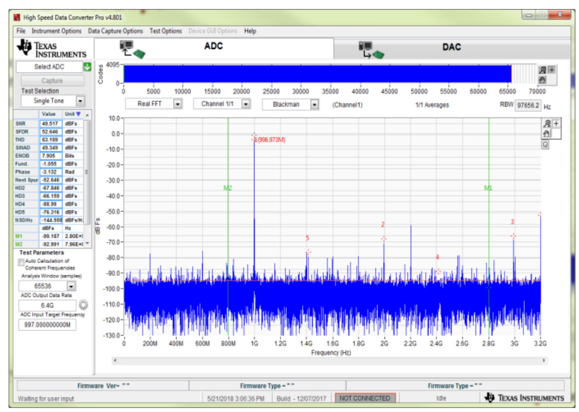


图 29 and 图 30 show the resultant spectrum of 12.8 GSPS with and without IL spur. 图 29 shows interleave spur at locations FS/2, FS/4, FS/2-FIN, FS/4-FIN, and FS/4+FIN associated with sampling clock FS = 12.8 GHz.

图 29. Fin = 977 MHz, 12.8 GSPS Interleave Spectrum With I_L Spur

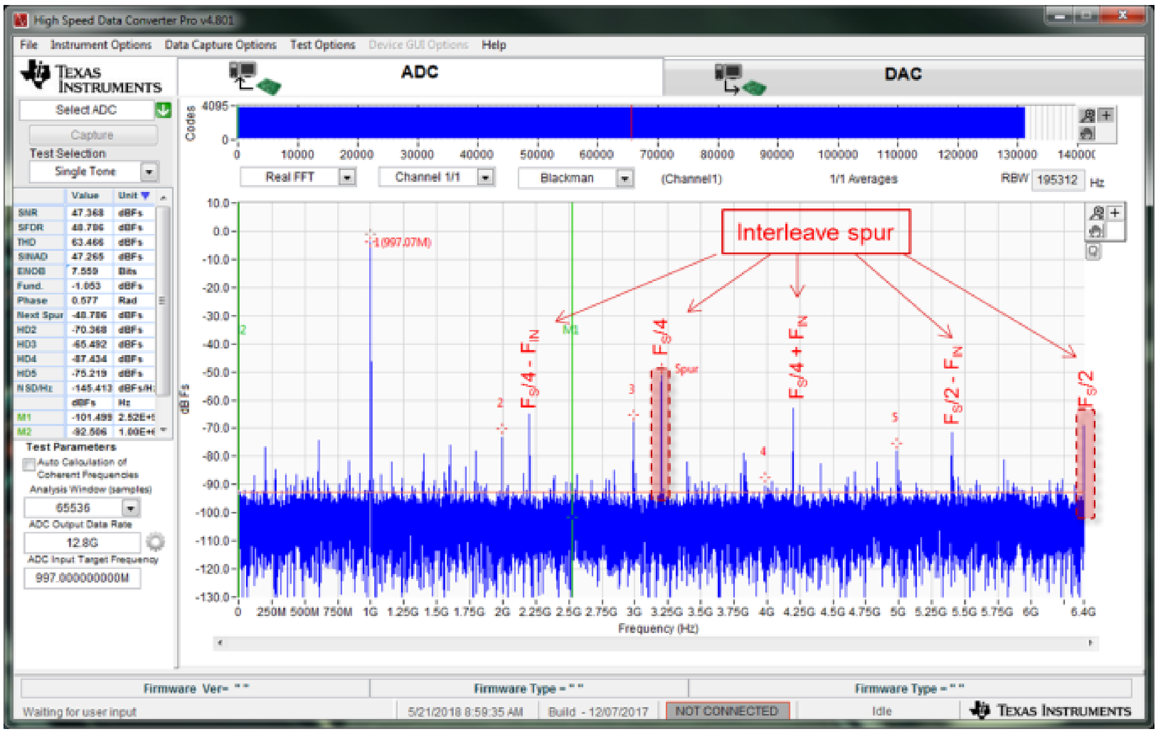
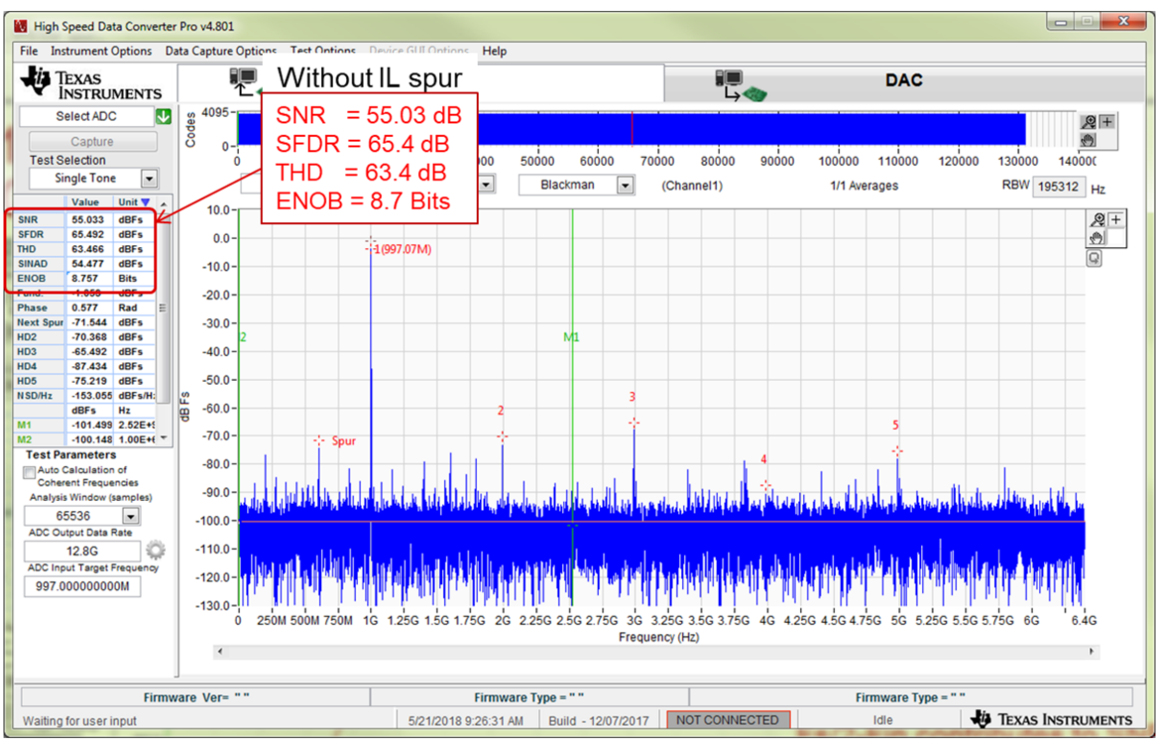


图 30. F_{IN} = 997 MHz, 12.8 GSPS Interleave Spectrum Without I_L Spur



节 2.2.2 discusses interleave spur, even when the input signal chain path and clock sample timing are closely matched, there will always be some mismatch in the system. This will vary due to temperature and process variations which can be reduced with the help of an on-line calibration process.

图 31 and 图 32 show the 12.8 GSPS interleaved plots for input signal frequencies from 300 MHz to 6 GHz with and without IL spurs. Interleaving spurs will reduce if the gain, offset, and time skew are matched. 图 31 clearly shows that greater than 7.5-bit ENOB can be achieved for the input bandwidth of 2 GHz without removing interleaving spur which is a promising result for 8-bit, 12.8-GSPS high-speed oscilloscope applications. 图 32 shows that ENOB can be improved to greater than 8.5 bits of ENOB after removing interleave spur.

图 31. 12.8 GSPS Interleave Spectrum With I_L Spur

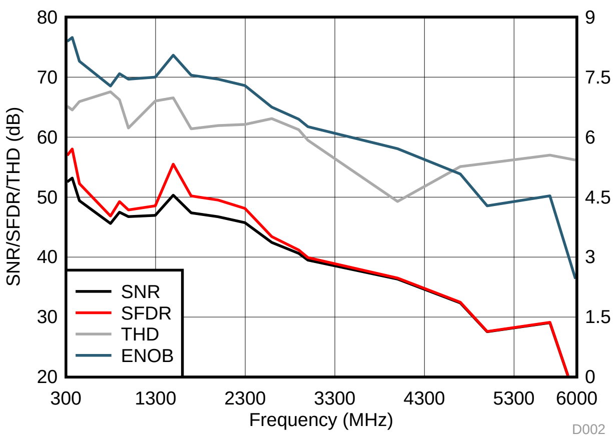
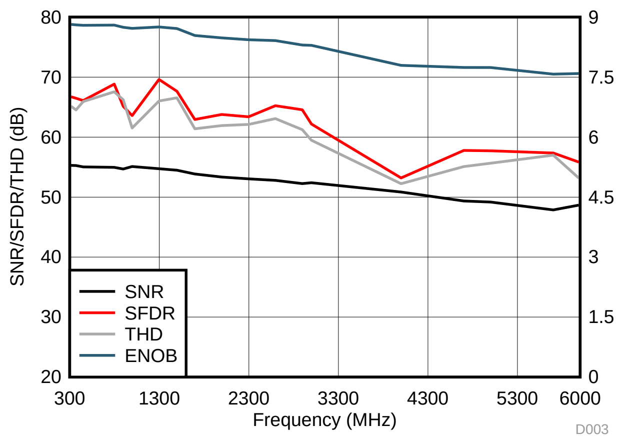


图 32. 12.8 GSPS Interleave Spectrum Without I_L Spur



In summary, the TIDA-01028 is a 12.8-GSPS interleaved reference design with an onboard high-performance clock and power solution that can be used for high-speed DSO and wideband digitizer applications where higher sampling rate and wider bandwidth is required.

This reference design demonstrates the ADC12DJ3200 interleaving features to achieve a 12.8-GSPS sample rate with usable bandwidth greater than 2.5 GHz with ENOB better than 7.5 bits, including interleaving spur.

This reference design demonstrates the flexibility and features of clock devices such as the LMK04828 and the LMX2594 that help designers to achieve low phase noise, high-frequency clocks for gigahertz interleaved sampling applications.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01028.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01028.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01028.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDA-01028.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01028.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01028.

5 Related Documentation

5.1 Related Reference Designs

1. Texas Instruments, Flexible 3.2 GSPS Multi-Channel AFE Reference Design for DSOs, RADAR, and 5G Wireless Test Systems (TIDA-01022)
2. Texas Instruments, 50-Ohm 2-GHz Oscilloscope Front-end Reference Design (TIDA-00826)
3. Texas Instruments, Multi-Channel JESD204B 15 GHz Clocking Reference Design for DSO, Radar and 5G Wireless Testers (TIDA-01021)
4. Texas Instruments, High Speed Multi-Channel ADC Clock Reference Design for Oscilloscopes, Wireless Testers and Radars (TIDA-01017)

5.2 Summary of Related Reference Designs

REFERENCE DESIGN NUMBER	MAXIMUM CLOCK FREQUENCY (GHz)	PHASE NOISE AT MAX FREQUENCY (dBc/Hz)	CLOCK SKEW (ps)	# OF CHANNELS DEMONSTRATED [THEORETICAL MAXIMUM]	SAMPLING RATE (GSPS)	SNR @ 1 GHz (dB)	SFDR (dBc)	MAXIMUM BANDWIDTH (GHz)	DESCRIPTION, FOCUS
TIDA-01028	15.0	–105.9	-	2[4]	12.8	55.0	63.5	8.0	12.8 GSPS AFE with Interleaved ADCs (ADCDJ3200)
TIDA-00626	10.0	–107.1	-	1	-	-	-	-	9.8 GHz RF CW Signal Generator
TIDA-01016	6.0	–114.0	N/A	1	3.0	60.0	-	3.2	Clocking Reference Design for ADC32RF45 (RF Sampling ADC)
TIDA-01021	15.0	–105.9	9.2	2 [6]	2.7	55.7	68.8	8.0	Clocking and Synchronization of Multiple JESD204B ADCs
TIDA-01023	15.0	–105.9	8.0	2 [42]	3.0	55.5	68.8	8.0	[Tree Structure] Clocking and Synchronization of JESD204B ADCs
TIDA-01024	15.0	–105.9	2.0	2 [18]	3.0	55.4	69.1	8.0	[Daisy Chain] Clocking and Synchronization of JESD204B ADCs
TIDA-01022	15.0	–105.9	1.0	4	3.2	55.5	71.3	8.0	Quad Channel 3.2GSPS Digitizer System (Integrating ADC, Clocking and Power)
TIDA-01027	Power design for optimal ENOB in High Speed DAQ								

5.3 Other Related Documents

1. Texas Instruments, *Interleaving ADCs for Higher Sample Rates*
2. Texas Instruments, *Maximizing SFDR Performance in the GSPS ADC: Spur Sources and Methods of Mitigation*
3. Texas Instruments, *Defining Skew, Propagation-Delay, Phase Offset (Phase Error)*

5.4 商标

E2E, PLLatinum are trademarks of Texas Instruments.
Arria, Altera are registered trademarks of Altera Corporation.
Altium Designer is a registered trademark of Altium LLC or its affiliated companies.
Marki is a trademark of Marki Microwave, Inc..
MATLAB is a registered trademark of The MathWorks, Inc..

6 About the Author

ANBU MANI is a systems engineer in the Industrial Systems Engineering team at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Anbu has experience in analog circuit design and digital circuit design for the Automatic Test Equipment in Modular platform. He is also engaged with the design and development of embedded products. Anbu earned his bachelor of engineering (BE) in electronic and communication from the Anna University, Chennai.

SANKAR SADASIVAM is a system architect in the Industrial Systems Engineering team at Texas Instruments, where he is responsible for designing and developing reference design solutions for the industrial systems with a focus on Test and Measurement. Sankar brings to this role his extensive experience in analog, RF, wireless, signal processing, high-speed digital, and power electronics. Sankar earned his master of science (MS) in electrical engineering from the Indian Institute of Technology, Madras.

7 Acknowledgment

The authors would like to thank their colleagues Bryan Bloodworth, Taras Dudar, Ajeet Pal, Victor Salomon, Jason Clark, Salvatore Finocchiaro, Matthew Guibord, Timothy Toroni, Jim Brinkhurst, Oliver Nachbaur and for their unconditional support and critical feedback during the development of this design and design guide review.

重要声明和免责声明

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122