TI Designs：TIDA-080000
使用 DLP®0.33 英寸微镜阵列的移动 1080p 显示参考设计

说明

此参考设计使开发人员能够快速实现小型 1080p 显示子系统。该器件 采用 了 DLP ®Pico0.33 英寸 TRP 1080p 显示芯片组，并在 DLP LightCrafter ™Display 3310 评估模块 (EVM) 中实现。它可用于各种 应用 ，包括移动智能电视、移动投影仪、数字标牌等等。该设计包含 DLP3310 1080p 数字微镜器件 (DMD)、DLPC3437 显示控制器，以及 DLPA3000 PMIC 和 LED 驱动器。

资源

TIDA-080000	设计文件夹
DLP3310 (DMD)	产品文件夹
DLPC3437	产品文件夹
DLPA3000	产品文件夹

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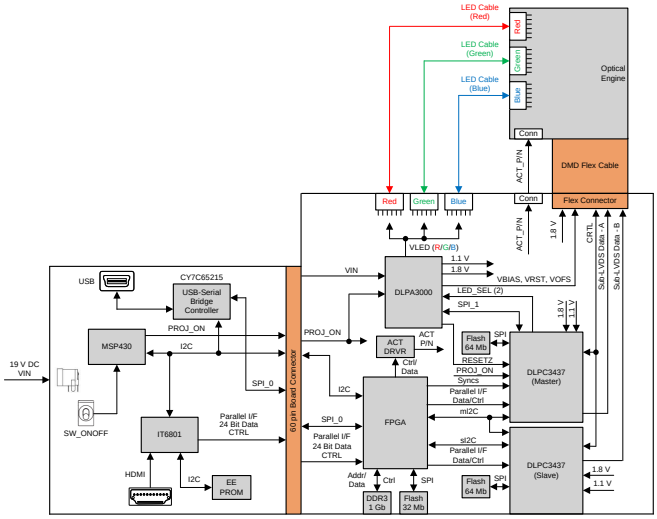
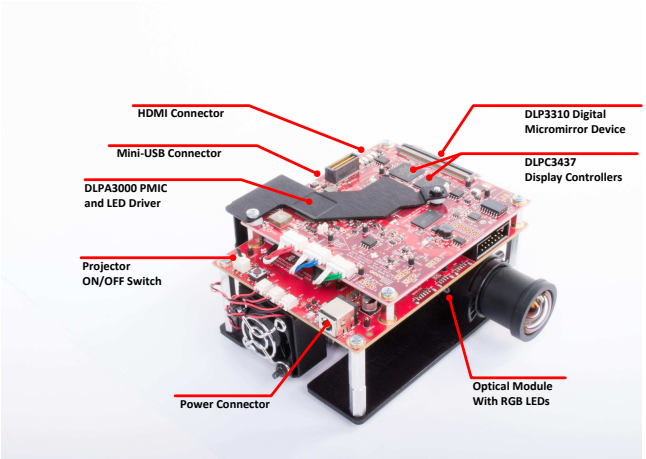
特性

- 1920 × 1080p 分辨率
- 小型总体外形尺寸（5.5 英寸 × 5.2 英寸 × 2.6 英寸）
- 亮度 300 RGB 流明（6A 红、绿和蓝 LED）
- 紧凑型 PCB 布局，支持 1080p (DLP3310) 光学引擎并包含 HDMI 和 USB 连接功能
- 用于 DLPDLCR3310EVM 布局
- 19V 输入以及高达 6A 的 LED 电流驱动
- 可通过 PC 软件 GUI 来自定义显示配置

应用

- Pico 投影仪
- 移动投影仪
- 智能移动电视
- 智能扬声器（带显示屏）
- 游戏投影仪
- 家庭/厨房显示屏
- 数字标牌显示屏
  - 零售/餐厅显示屏
  - 沉浸式电梯显示屏





1 System Description

The 0.33-inch TRP 1080p display chipset enables the use of DLP technology in a variety of applications that require full HD resolution, low power, and small form factors. This reference design provides developers with the ability to quickly implement full HD display subsystems at higher brightness levels using the DLPA3000 PMIC and LED driver.

1.1 Applications for Mobile Smart TVs and Mobile Projectors

Mobile projectors can be used as a portable big-screen display for any device with video output, such as laptops, smartphones, tablets, and gaming consoles. These projectors can offer users an easy and lightweight means to project large and colorful videos in a variety of settings.

Mobile smart TV products combine three exciting technologies: Wireless connectivity, video content streaming, and pico projection. A mobile smart TV can wirelessly stream internet content and project it onto virtually any surface. To learn more about mobile smart TVs and mobile projectors, go to the DLP Pico Applications Portal.

表 **1. DLP Features and Design Benefits for Mobile Smart TVs and Mobile Projectors**

DLP FEATURE	DESIGN BENEFIT
High optical efficiency	DMDs incorporate highly reflective and polarization agnostic aluminum micromirrors, which enable bright and power efficient display products.
Small size, high resolution	With micromirrors as small as 5.4 µm, DLP Pico chips deliver resolutions up to 1080p while enabling very compact projection designs.
High contrast	Optical modules designed with DLP Pico chips can achieve full on/off contrast ratios of over 1000:1, depending on system design. Higher contrast translates to more vivid colors and darker blacks.
Mature ecosystem	A mature global ecosystem of established optical module manufacturers eases the design process and allows product developers to go to market faster by using an existing, off-the-shelf optical engine that is already in production.

1.2 Industrial Applications

DLP Pico display chipsets can be incorporated into a variety of industrial applications.

Digital signage is a category of displays designed for commercial and industrial spaces, including retailers, stadiums, casinos, hotels, restaurants, and airports. Digital signage delivers up-to-date information such as advertising, menus, event status, and maps in locations where people gather. The low power and compact size of DLP Pico chipsets enable effective digital signage solutions that can be tucked away for free-form, on-demand displays on virtually any surface.

For more information, read *Using TI DLP® technology to make digital signage more effective*.

Integrating DLP Pico technology into appliances can enhance their effectiveness. Adding smart displays to appliances can offer many benefits such as interactive, adaptive, and reconfigurable interfaces that can replace buttons, tablets, LCD panels, and mechanical knobs in virtually every room of the house.

To learn more, read *TI DLP® Pico™ technology for smart home applications*.

2 System Overview

2.1 Block Diagram

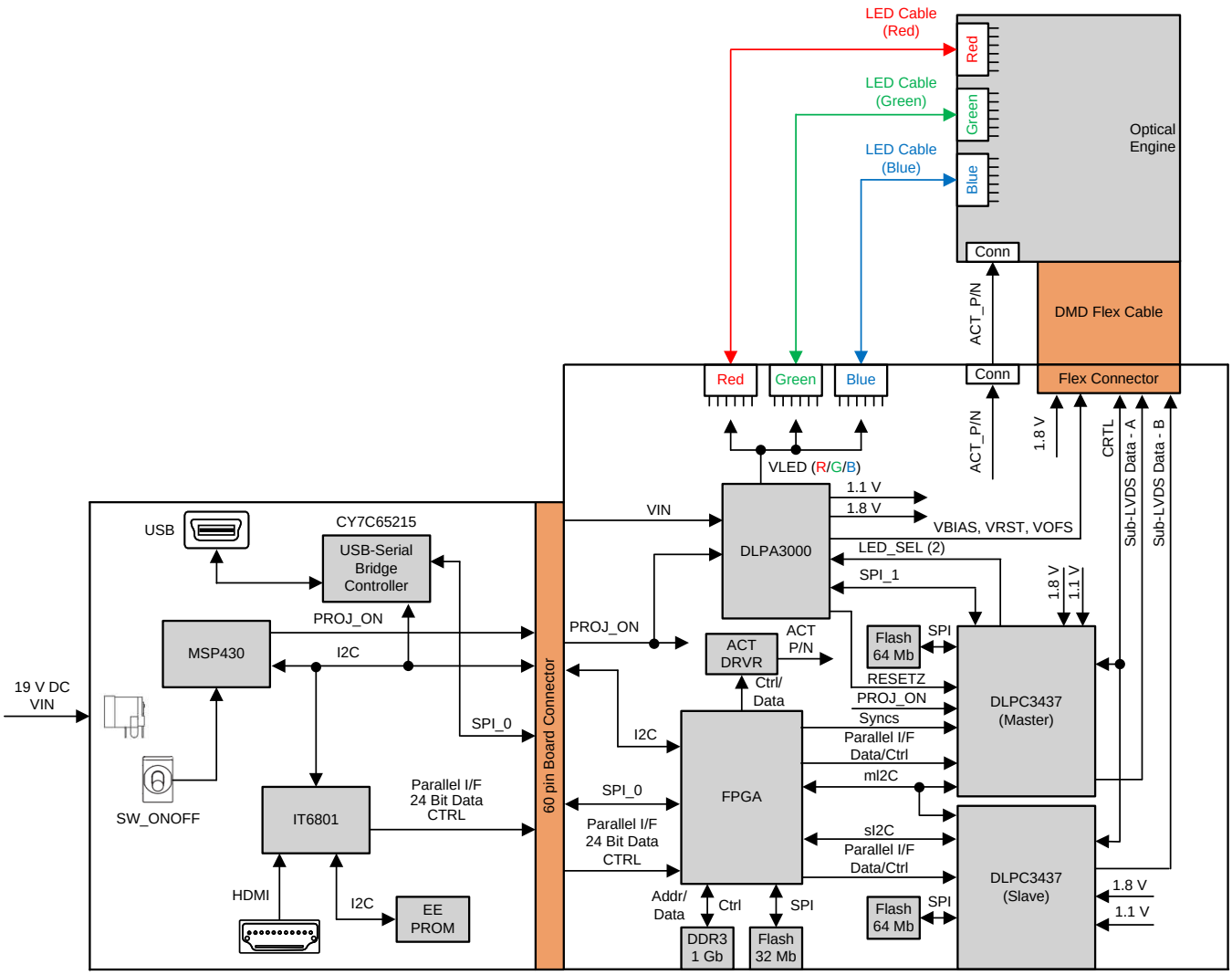


图 1. DLP LightCrafter Display EVM Block Diagram

2.2 Design Considerations (If Applicable)

See the following documents for considerations in DLP system design:

- *TI DLP® Pico™ System Design: Optical Module Specifications*
- *TI DLP® System Design: Brightness Requirements and Tradeoffs*

2.3 Highlighted Products

This chipset reference design guide draws upon figures and content from several other published documents related to the 0.33-in 1080p DLP chipset. For a list of these documents, see 6 节.

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

Assuming default conditions as shipped:

1. Provide power to the DLP LightCrafter Display 3310 EVM by applying an external DC power supply (19-V DC, 3.42 A) to the J9 connector.
   External power supply requirements:
   - Nominal output voltage: 19-V DC
   - Minimum output current: 2.5 A; maximum output current: 3.42 A
   - Efficiency level: VI

   注: TI recommends using an external power supply that complies with applicable regional safety standards such as UL, CSA, VDE, CCC, and PSE.

   注: The system is designed to operate also with an external 19-V DC power supply. The P5V_VIN (D1) and P3P3V_SB (D7) LEDs on the system board will turn on to indicate that 5-V power and 3.3-V power are applied.
2. Move the SW2 switch to the ON position to turn on the DLP LightCrafter Display 3310 EVM. When the DLP LightCrafter Display 3310 EVM is turned on, the PROJ_ON LED (D5) will turn on.
3. After the DLP LightCrafter Display 3310 EVM is turned on, the projector will default to displaying a DLP LightCrafter Display splash image.
4. The focus of the image can be adjusted manually on the optical engine.

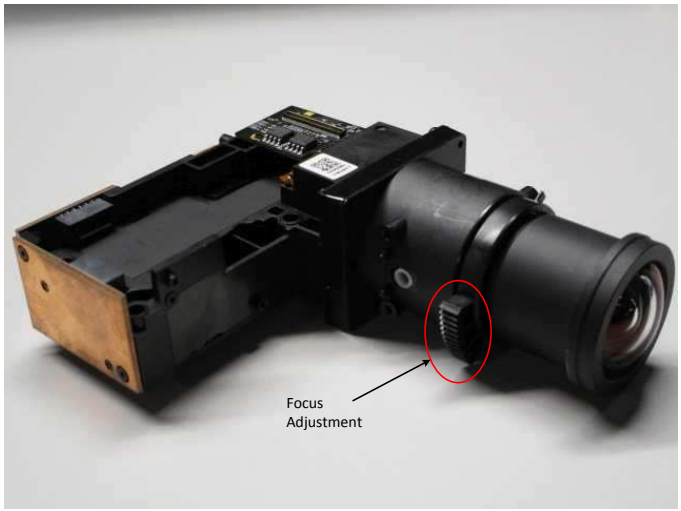


图 **2. Optical Engine With Focus Adjustment**

5. Connect the USB to the DLP LightCrafter Display 3310 EVM and open the latest GUI on the computer. If needed, connect an HDMI source to the EVM and communicate to the EVM through the GUI software.
6. When turning off the projector, turn off the SW2 switch prior to removing the power cable.

   注: To avoid potential damage to the DMD, it is recommended to turn off the projector with the SW2 switch before disconnecting the power.

There are fourteen indicator LEDs on the DLP LightCrafter Display 3310 EVM (Display and System boards), and they are defined in 表 2:

表 2. LEDs on the DLP LightCrafter Display 3310 EVM

Board	LED Reference	Signal Indication	Description
System	D1	P5V_VIN	Regulated 5-V power on.
	D3	MSP430_REQ	ON when Cypress CY65215 requests the MSP430 to give Cypress master control of the I^2C bus.
	D4	MSP430_ACK	ON when Cypress CY65215 is I^2C master. OFF when MSP430 is I^2C master.
	D5	PROJ_ON	ON when Projector is turned on via SW_ONOFF.
	D6	RESETZ	OFF when Projector is turned on via SW_ONOFF.
	D7	P3P3V_SB	Regulated 3.3-V power on.
	D8	MSP_LED2_ONZ	ON when HDMI cable is plugged in and external video is detected. OFF when external video is not detected.
	D9	GPIO_1	Blinking when PC is communicating to flash over SPI.
	D10	GPIO_0	Blinking when PC is communicating to DLPC3437 over I^2C.
Display	D1	P12V	Regulated 12-V power on.
	D2	DONE	ON when FPGA configuration is completed.
	D7	INIT_B	On when FPGA initialization is completed. OFF indicates that the FPGA is in reset or when there is a configuration error.
	D8	mHOST_IRQ	ON during master DLPC3437 boot. OFF when projector is running. Indication of master DLPC3437 boot-up completed and ready to receive commands.
	D9	sHOST_IRQ	ON during slave DLPC3437 boot. OFF when projector is running. Indication of slave DLPC3437 boot-up completed and ready to receive commands.

3.1.2 Software

The software required for this reference design is available for download in the DLPDLCR3310EVM tool folder.

3.2 Testing and Results

The results of a successful test of this system is the appearance on the display of the splash screen, as shown in 图 3.

图 3. DLP3310 System Splash Screen

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-080000.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-080000.

4.3 PCB Layout Recommendations

The layout guidelines listed in this design guide are subsets of the guidelines included in the component data sheets. For more information, refer to the DLPC3437, DLP3310, and DLPA3000 data sheets.

4.3.1 DLPC3437 Layout Guidelines

4.3.1.1 Internal ASIC PLL Power

The following guidelines are recommended to achieve desired ASIC performance relative to the internal PLL. Each DLPC3437 contains two internal PLLs, which have dedicated analog supplies (VDD_PLLM, VSS_PLLM, VDD_PLLD, VSS_PLLD). As a minimum, VDD_PLLx power and VSS_PLLx ground pins must be isolated using a simple passive filter consisting of two series ferrites and two shunt capacitors (to widen the spectrum of noise absorption). It is recommended that one capacitor be a 0.1-µF capacitor and the other be a 0.01-µF capacitor. Place all four components as close to the ASIC as possible; however, it is especially important to keep the leads of the high-frequency capacitors as short as possible. Note that both capacitors must be connected across VDD_PLLM and VSS_PLLM / VDD_PLLD and VSS_PLLD respectfully on the ASIC side of the ferrites.

For the ferrite beads used, their respective characteristics should be as follows:

- DC resistance less than 0.40 Ω
- Impedance at 10 MHz equal to or greater than 180 Ω
- Impedance at 100 MHz equal to or greater than 600 Ω

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD_PLLM and VDD_PLLD must be a single trace from the DLPC3437 to both capacitors and then through the series ferrites to the power source. The power and ground traces should be as short as possible, parallel to each other, and as close as possible to each other.

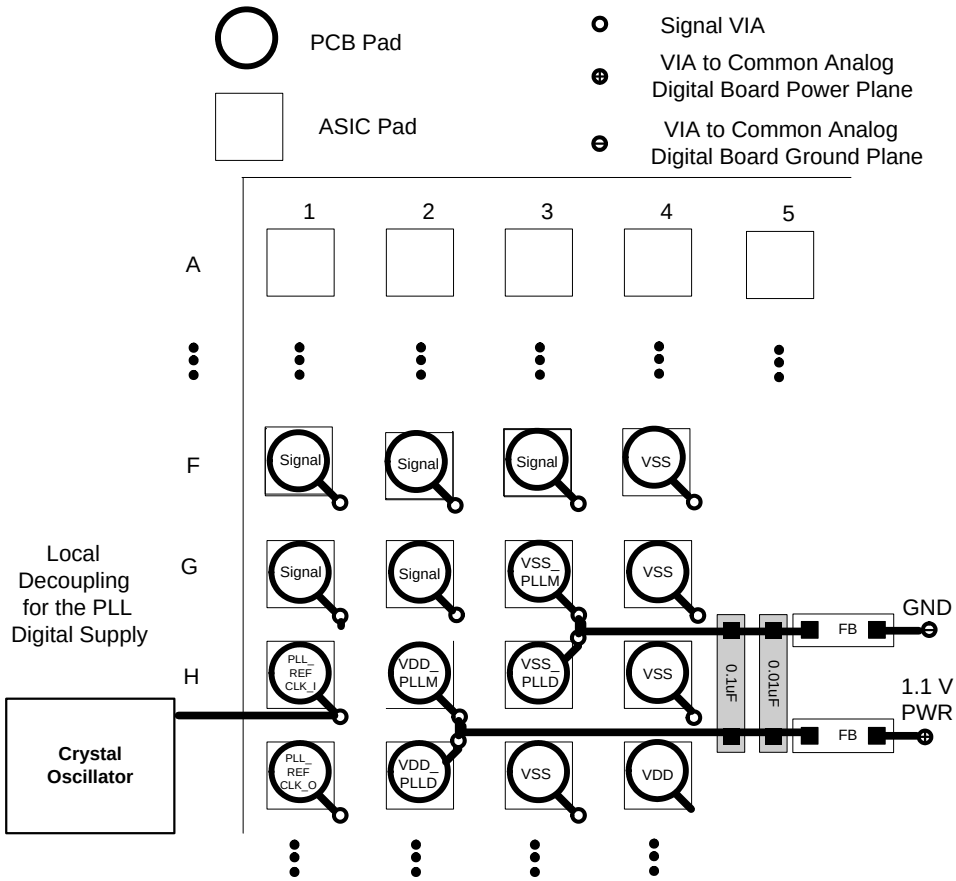


图 4. PLL Filter Layout

4.3.1.2 I^2C Interface Performance

Both DLPC3437 I^2C interface ports support a 100-kHz baud rate. By definition, I^2C transactions operate at the speed of the slowest device on the bus, thus there is no requirement to match the speed grade of all devices in the system.

4.3.1.3 DMD Interface Considerations

The sub-LVDS HS interface waveform quality and timing on the DLPC3437 ASIC is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

As an example, the DMD interface system timing margin can be calculated as follows:

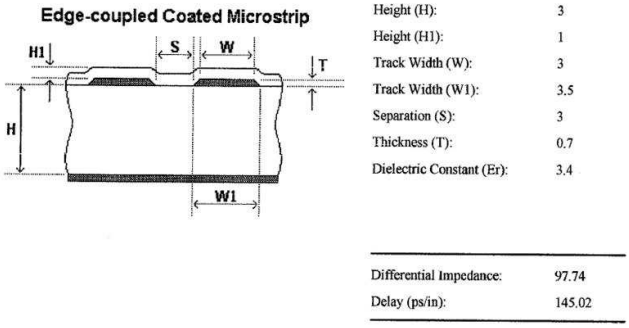
Setup Margin = (DLPC343x output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation) (1)

Hold-time Margin = (DLPC343x output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

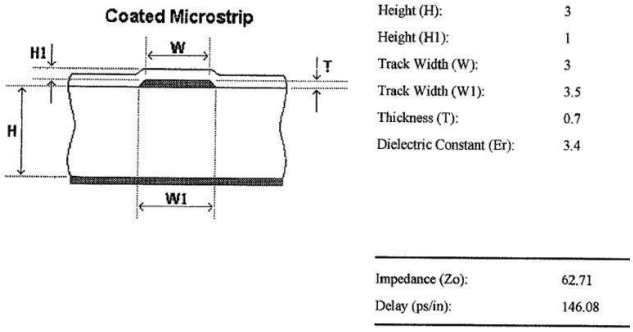
where PCB SI degradation is signal integrity degradation due to PCB effects, which includes such things as simultaneously switching output (SSO) noise, crosstalk, and inter-symbol interference (ISI) noise. (2)

The DLPC3437 I/O timing parameters as well as the DMD I/O timing parameters can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. However, PCB SI degradation is a more complicated adjustment.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that satisfy both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations can also work, but must be confirmed with PCB signal integrity analysis or lab measurements.



DMD_HS Differential Signals



DMD_LS Signals

图 5. DMD Interface Board Stack-Up Details

4.3.1.4 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends to tie unused ASIC input pins through a pullup resistor to their associated power supply or a pulldown resistor to ground. For ASIC inputs with internal pullup or pulldown resistors, do not add an external pullup or pulldown resistor unless specifically recommended.

注: Internal pullup and pulldown resistors are weak and must not be expected to drive the external line. The DLPC3437 device implements very few internal resistors, and these are noted in the pin list. When external pullup or pulldown resistors are needed for pins that have built-in weak pullups or pulldowns, use the value 8 kΩ (max).

Never tie unused output-only pins directly to power or ground. These pins can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins can become an input, then the pins must be pulled up (or pulled down) using an appropriate, dedicated resistor.

4.3.1.5 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

表 3. Max Pin-to-Pin PCB Interconnect Recommendations(1)(2)

DMD BUS SIGNAL	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 152.4	See (3)	inch (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	6.0 152.4	See (3)	inch (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	6.5 165.1	See (3)	inch (mm)
DMD_LS_WDATA	6.5 165.1	See (3)	inch (mm)
DMD_LS_RDATA	6.5 165.1	See (3)	inch (mm)
DMD_DEN_ARSTZ	7.0 177.8	See (3)	inch (mm)

(1) Maximum signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.
(3) Due to board variations, these are impossible to define. Any board designs should be SPICE simulated with the ASIC IBIS models to ensure single routing lengths do not exceed requirements.

表 4. High-Speed PCB Signal Routing Matching Requirements(1)(2)(3)(4)

INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH(5)	UNIT
DMD	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	DMD_HS_CLK_P DMD_HS_CLK_N	±1.0 (±25.4)	inch (mm)
	DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
	DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
	DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
	DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
	DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
	DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
	DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD	DMD_HS_WDATA_x_P	DMD_HS_WDATA_x_N	±0.025 (±0.635)	inch (mm)
	DMD_HS_CLK_P	DMD_HS_CLK_N	±0.025 (±0.635)	inch (mm)
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	inch (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

(1) These values apply to PCB routing only and do not include any internal package routing mismatch associated with the DLPC3437 or the DMD.
(2) DMD HS data lines are differential, thus these specifications are pair-to-pair.
(3) Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
(4) DMD LS signals are single-ended.
(5) Mismatch variance for a signal group is always with respect to reference signal.

4.3.1.6 Number of Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair must not change layers.

4.3.1.7 Stubs

- Avoid stubs.

4.3.1.8 Terminations

- No external termination resistors are required on DMD_HS differential signals.
- The DMD_LS_CLK and DMD_LS_WDATA signal paths must include a 43-Ω series termination resistor located as close as possible to the corresponding ASIC pins.
- The DMD_LS_RDATA signal path must include a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- DMD_DEN_ARSTZ does not require a series resistor.

4.3.1.9 Routing Vias

- Minimize the number of vias on DMD_HS, DMD_LS_CLK, and DMD_LS_WDATA signals to not exceed two.

- Any and all vias on these signals must be located as close to the ASIC as possible.

4.3.2 DLPA3000 Layout Guidelines

4.3.2.1 Layout Guidelines

For switching power supplies, the layout is an important step in the design process, especially when it concerns high-peak currents and high-switching frequencies. If the layout is not carefully done, the regulator could show stability issues and EMI problems. Therefore, it is recommended to use wide- and short-traces for high-current paths and for their return power ground paths. The input capacitor, output capacitor, and inductor must be placed as near as possible to the device. To minimize ground noise coupling between different buck converters, separate their grounds and connect them together at a central point under the part.

The high currents of the buck converters concentrate around pins V_{IN}, SWITCH, and P_{GND} (see 图 6). The voltage at the pins V_{IN}, P_{GND}, and FB are DC voltages while the pin SWITCH has a switching voltage between V_{IN} and P_{GND}. In case the FET between pins 52 and 53 is closed, the red line indicates the current flow while the blue line indicates the current flow when the FET between pins 53 and 54 is closed. These paths carry the highest currents and must be kept as short as possible.

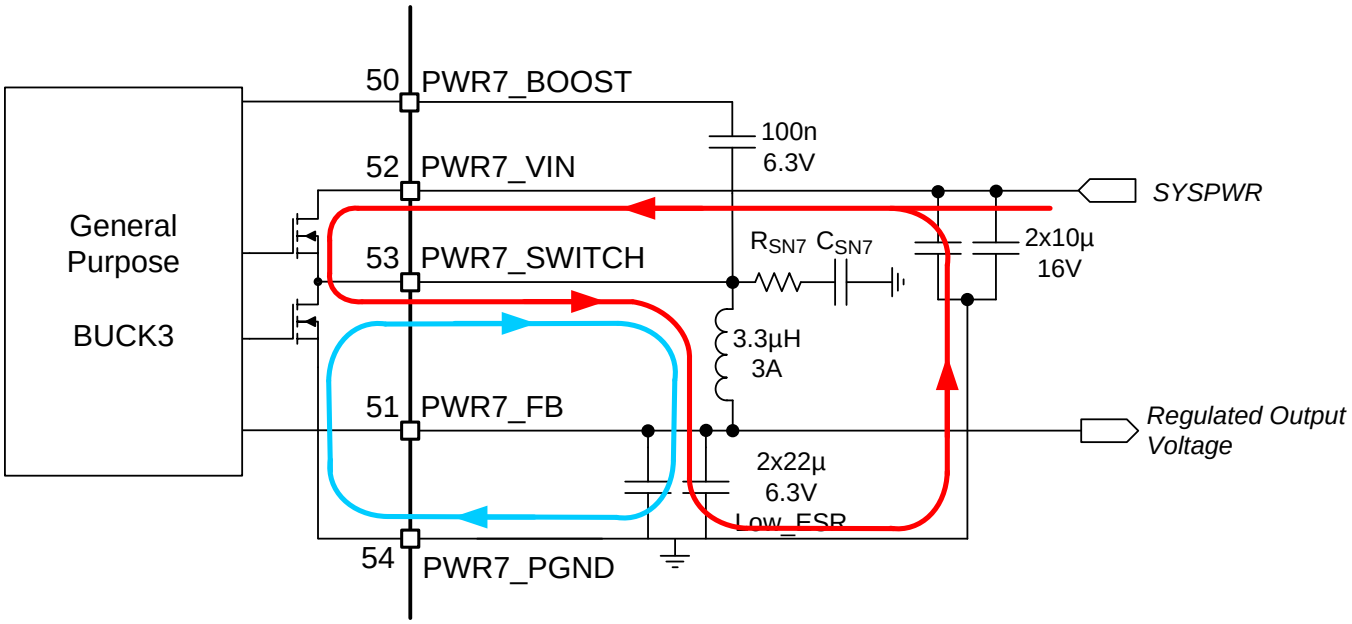


图 **6. High AC Current Paths in a Buck Converter**

The trace to the V_{IN} pin carries high AC currents. Therefore, the trace must be low-resistive to prevent voltage drop across the trace. Additionally, the decoupling capacitors must be placed as near to the V_{IN} pin as possible.

The SWITCH pin is connected alternatingly to the V_{IN} or GND. This means a square wave voltage is present on the SWITCH pin with an amplitude of V_{IN} and containing high frequencies. This condition can lead to EMI problems if not properly handled. To reduce EMI problems, a snubber network (RSN7 and CSN7) is placed at the SWITCH pin to prevent or suppress unwanted high-frequency ringing at the moment of switching.

The P_{GND} pin sinks high current and must be connected to a star ground point such that it does not interfere with other ground connections.

The FB pin is the sense connection for the regulated output voltage, which is a DC voltage. No current is flowing through this pin. The voltage on the FB pin is compared with the internal reference voltage to control the loop. The FB connection must be made at the load such that the IR drop does not affect the sensed voltage.

4.3.2.2 SPI Connections

The SPI consists of several digital lines and the SPI supply. If routing of the interface lines is not done properly, communication errors can occur. SPI lines must not pick up noise and keep possible interfering sources away from the interface.

Pickup of noise can be prevented by ensuring that the SPI ground line is routed together with the digital lines as much as possible to the respective pins. The SPI must be connected by a separate ground connection to the DGND of the DLPA3000 (see 图 7). This prevents ground noise between SPI ground references of the DLPA3000 and DLPC due to the high current in the system.

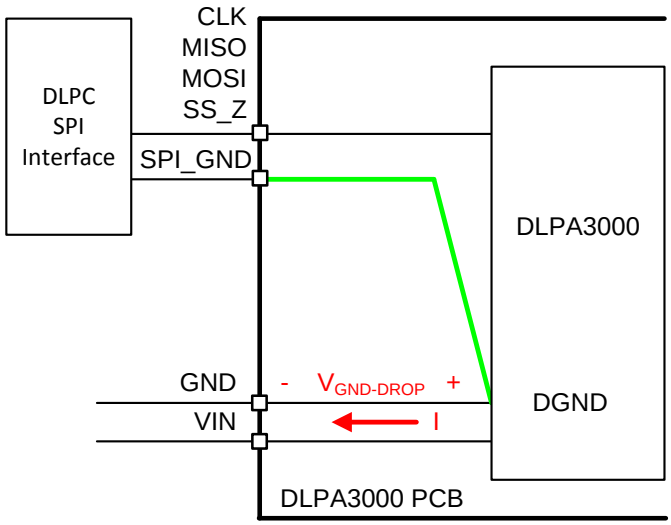


图 7. SPI Connections

Keep interfering sources away from the interface lines as much as possible. High-current lines such as neighboring PWR_6 must especially be routed carefully. If PWR 6 is routed too close to SPI_CLK, for example, it could lead to false clock pulses and thus communication errors.

4.3.2.3 R_{LIM} Routing

R_{LIM} is used to sense the LED current. To accurately measure the LED current, the RLIM_K_1,2 lines must be connected close to the top side of measurement resistor R_{LIM}, while RLIM_BOT_K_1,2 must be connected close to the bottom side of R_{LIM}.

The switched LED current is running through R_{LIM}. Therefore, a low-ohmic ground connection for R_{LIM} is strongly advised.

4.3.2.4 LED Connection

Switched large currents are running through the wiring from the DLPA3000 to the LEDs. Therefore, special attention is needed. Two perspectives apply to the LED-to-DLPA3000 wiring:

1. The resistance of the wiring, R_{series}.
2. The inductance of the wiring, L_{series}.

图 8 shows the location of the parasitic series impedances.

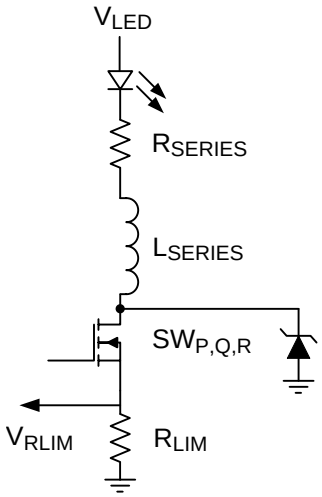


图 8. Parasitic Inductance (L_{series}) and Resistance (R_{series}) in Series With LED

Currents up to 6 A can run through the wires connecting the LEDs to the DLPA3000. Some noticeable dissipation can easily be caused. Every 10 mΩ of series resistance implies, for a 6-A average LED current, a parasitic power dissipation of 0.36 W. This dissipation can cause PCB heating, but more importantly, the overall system efficiency is deteriorated.

Additionally, the resistance of the wiring might impact the control dynamics of the LED current. The routing resistance is part of the LED current control loop. The LED current is controlled by V_{LED}. For a small change in V_{LED} (ΔV_{LED}), the resulting LED current variation (ΔI_{LED}) is given by the total differential resistance in that path:

$$\Delta I_{LED} = \frac{\Delta V_{LED}}{r_{LED} + R_{series} + R_{on\_SW\_P,Q,R} + R_{LIM}} \quad (3)$$

where

- r_{LED} is the differential resistance of the LED
- $R_{on\_SW\_P,Q,R}$ is the on-resistance of the strobe decoder switch

This expression ignores L_{series} because realistic values are usually sufficiently low to cause any noticeable impact on the dynamics.

All the comprising differential resistances are in the range of 25 mΩ to several hundred millii-ohms. Without paying special attention, a series resistance of 100 mΩ can easily be obtained. It is advised to keep this series resistance sufficiently low (< 50 mΩ for example).

The series inductance plays an important role when considering the switched nature of the LED current. While cycling through R, G, and B LEDs, the current through these branches is turned on and turned off in short-time duration. Specifically, turnoff is fast. A current of 6 A goes to 0 A in a matter of 50 ns, which implies a voltage spike of about 1 V for every 10 nH of parasitic inductance. It is recommended to minimize the series inductance of the LED wiring by using:

- Short wires
- Thick wires or multiple parallel wires
- Small enclosed area of the forward and return current path

If the inductance cannot be made sufficiently low, use a Zener diode to clamp the drain voltage of the RGB switch, so that it does not surpass the absolute maximum rating. The clamping voltage needs to be chosen between the maximum expected V_{LED} and the absolute maximum rating. Take care of sufficient margin of the clamping voltage relative to the mentioned minimum and maximum voltage.

4.3.3 DMD Interface Layout Guidelines

The DMD is connected to a PCB or a Flex circuit using an interposer. For additional layout guidelines regarding length matching, impedance, etc. see the DLPC3437 controller datasheet.

Some layout guidelines for routing to the DMD are:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. Refer to 图 9.
- Minimum of two 220-nF (35 V) capacitors - one close to V_{BIAS} pin. Capacitors C10 and C14 in 图 9.
- Minimum of two 220-nF (35 V) capacitors - one close to each V_{RST} pin. Capacitors C11 and C13 in 图 9.
- Minimum of two 220-nF (35 V) capacitors - one close to each V_{OFS} pin. Capacitors C4 and C12 in 图 9.
- Minimum of four 220-nF (10 V) capacitors - two close to each side of the DMD. Capacitors C1, C3, C2, and C5 in 图 9.

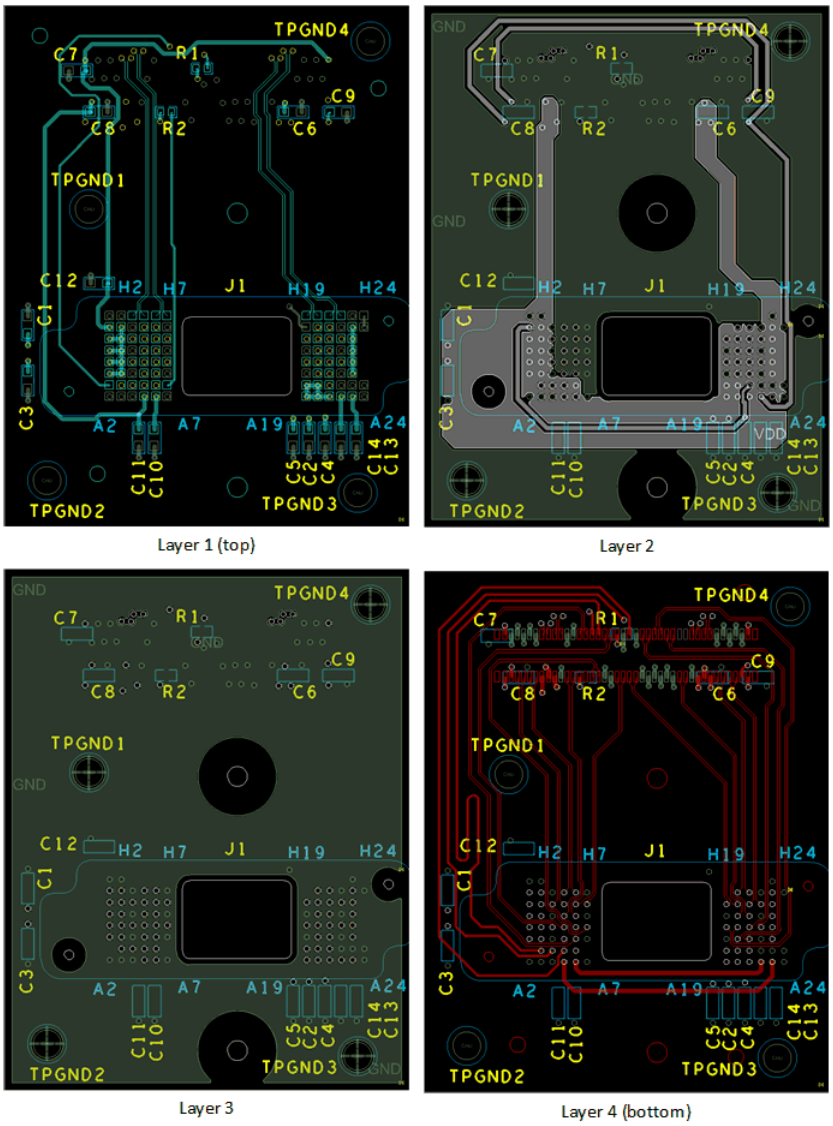


图 9. Power Supply Connections

4.3.4 FPGA - DDR3L SDRAM Interface Layout Guidelines

The FPGA to DDR3L SDRAM interface is based on a 533-MHz DDR clock rate. The Xilinx Zynq FPGA (XC7Z020-1CLG484I4493) to a Micron low power DDR3 SDRAM (MT41K64M16TW-107 IT) interface diagram is shown in 图 10 and the recommended interface layout guidelines are defined in 表 5.

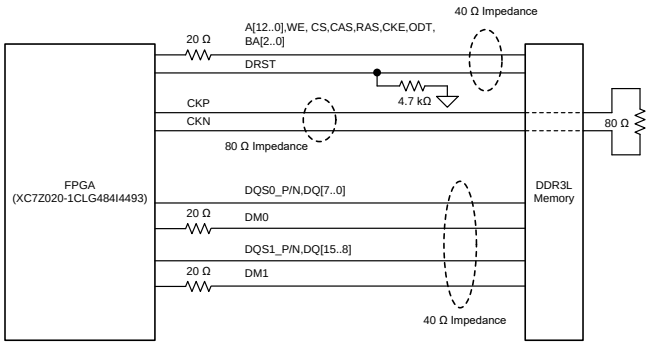


图 10. FPGA-DDR3L Interface

表 5. Recommended FPGA-DDR3L PCB Trace Delays

Net Name	Minimum Trace Delay (ps)	Maximum Trace Delay (ps)	Trace Impedance (Ω)
DDR_A(12:0)	175	225	40
DDR_BA(2:0)	175	225	40
DDR_CAS_B	175	225	40
DDR_CKE	150	175	40
DDR_CS_B	175	225	40
DDR_DRST_B	175	225	40
DDR_ODT	175	225	40
DDR_RAS_B	175	225	40
DDR_WE_B	150	175	40
DDR_CK(P,N)	208	212	80 Differential
DDR_DQS_P0, DDR_DQS_N0	180	190	40
DDR_DM0	180	200	40
DDR_DQ(7:0)	180	200	40
DDR_DQS_P1, DDR_DQS_N1	180	190	40
DDR_DM1	180	200	40
DDR_DQ(15:8)	180	200	40

Good PCB routing practices:

- Use inner PCB layers when possible.
- Route DDR_DQ(7:0), DDR_DM0 and DDR_DQS_(P,N)0 on the same layer(s).
- Route DDR_DQ(15:8), DDR_DM1 and DDR_DQS_(P,N)1 on the same layer(s).
- DDR_DQS_P0/N0 should have equal delays.
- DDR_DQS_P1/N1 should have equal delays.

4.3.5 Layout Prints

To download the layer plots, see the design files in the TIDA-080000 folder.

4.4 Cadence Project

To download the Cadence project files, see the design files in the TIDA-080000 folder.

4.5 Gerber Files

To download the Gerber files, see the design files in the TIDA-080000 folder.

4.6 Assembly Drawings

To download the assembly drawings, see the design files in the TIDA-080000 folder.

5 Software Files

To download the software files, see the design files in the TIDA-080000 folder.

6 Related Documentation

1. Texas Instruments, *TI DLP® LightCrafter™ Display 3310 EVM User's Guide*
2. Texas Instruments, *DLPC3437 Software Programmer's Guide*
3. Texas Instruments, *DLPC3437 Display Controller Data Sheet*
4. Texas Instruments, *DLP3310 0.33 1080p DMD Data Sheet*
5. Texas Instruments, *DLPA3000 PMIC and High-Current LED Driver IC Data Sheet*

6.1 商标

7 Third-Party Products Disclaimer

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