TI 设计：TIDA-080003

适用于使用 DLP® Pico™ 技术的台式 3D 打印机的小型光源引擎参考设计

TEXAS INSTRUMENTS

说明

这项低成本 3D 打印光源引擎参考设计可加快台式 3D 打印的开发速度 应用 使用 DLP Pico 技术。此设计采用了立体光刻 (SLA) 技术，将感光树脂暴露在连续的二维图形下，每次一层地创建三维对象。由于采用了分层打印，这种技术与其他技术相比，从根本上大幅提高了打印速度。此 TI 设计使用了具有新的显示和光控制器 DLPC3478 的 DLP Pico 0.3inch TRP HD 720p DMD (DLP3010)。DLP3010 DMD 提供了分辨率、尺寸和成本之间的完美平衡，它以小型台式 3D 打印机为目标，支持在消费者、专业和工业领域的各种 3D 打印用例 应用的出色解决方案。这项参考设计包含光源引擎设计示例，该设计示例囊括了电子和光学器件，以及用于生成图形集的软件，以暴露 3D 打印过程中使用的任何一种图层图像。此参考设计还包含 DLPA2005 PMIC 和 LED 驱动器。

资源

TIDA-080003	设计文件夹
DLP3010 (DMD)	产品文件夹
DLPC3478	产品文件夹
DLPA2005	产品文件夹

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特性

- 具有灵活和精确照明控制的 1280 × 720 分辨率
- 紧凑型 PCB 布局，支持 720p (DLP3010) 光学引擎且包含 HDMI 和 USB 连接功能
- 用于 DLP3010EVM-LC 布局
- 19V 输入以及高达 2.5A 的 LED 电流驱动
- 用于将任意类型的图形发送到光源引擎的 PC 软件 GUI

应用

- 个人电子产品：
  - 台式 3D 打印机
- 工业：
  - 定制部件生产

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1 System Description

Stereolithography is an additive manufacturing method that employs a photo-curable resin. Exposing the photo-resin to successive 2-dimensional object cross sections creates the 3-dimensional object a single layer at a time. The resin, composed of monomers, cross-links when exposed to light of a sufficient energy level. The cross-linking of the monomers generates a polymer chain, creating a solid material where the resin was exposed. Stereolithography was traditionally achieved by outlining the object layer with a laser. DLP technology allows an entire layer to be exposed simultaneously by dynamically masking a broad light source.

图 1 shows a typical block diagram of a 3D printing system that uses the stereolithography technique.

图 1. 3D printing system block diagram

Typical 3D printer requirements are shown in 表 1.

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表 **1. Typical 3D Printer System Requirements**

Feature	Requirements
Pattern Speed	1 -100 Hz
X-Y Resolution	50 - 100 µm
Build Area	150 mm x 80 mm
Wavelength	405 nm
Pattern	Binary or 8 bit grayscale patterns using external pattern mode

1.1 Applications for 3D Printing

DLP technology offers high precision and high printing speed in stereolithography compared to alternate technologies such as FDM (Fused Deposition Molding) or Laser-based stereolithography. The table below lists the key features of DLP technology and their corresponding benefits in 3D printing applications.

表 **2. DLP Features and Design Benefits for 3D Printing**

DLP Feature	Design Benefit
Layer-by-layer printing: Micromirror array exposes an entire layer in one shot	Faster build speed than **point-by-point** technologies and constant build time independent of layer complexity.
Easily programmable high-resolution patterns	Enables sub-50 µm resolutions on the image plane and easily adjusts layer thickness
Extended wavelength support	Compatible with a wide range of polymers and resins
Reliable MEMS technology	No expensive parts (e.g. ink jets) to replace - translates to lower cost of ownership

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2 System Overview

2.1 Block Diagram

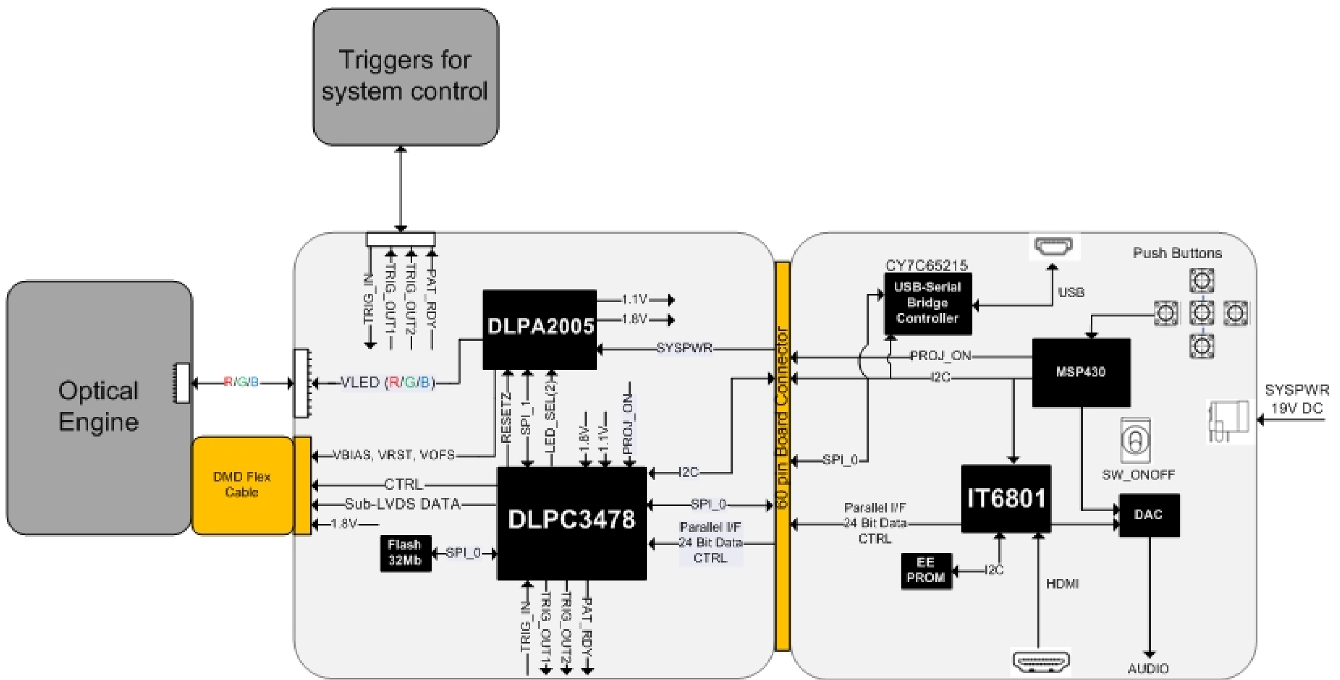

图 2. TIDA-080003 Block Diagram

2.2 Design Considerations

See the following documents for DLP system design considerations:

- *TI DLP® Pico™ System Design: Optical Module Specifications*
- *TI DLP® System Design: Brightness Requirements and Tradeoffs*

2.2.1 3D Printer Build Orientation

The 3D printer can be designed using two methods – Top-down or bottom-up build orientations.

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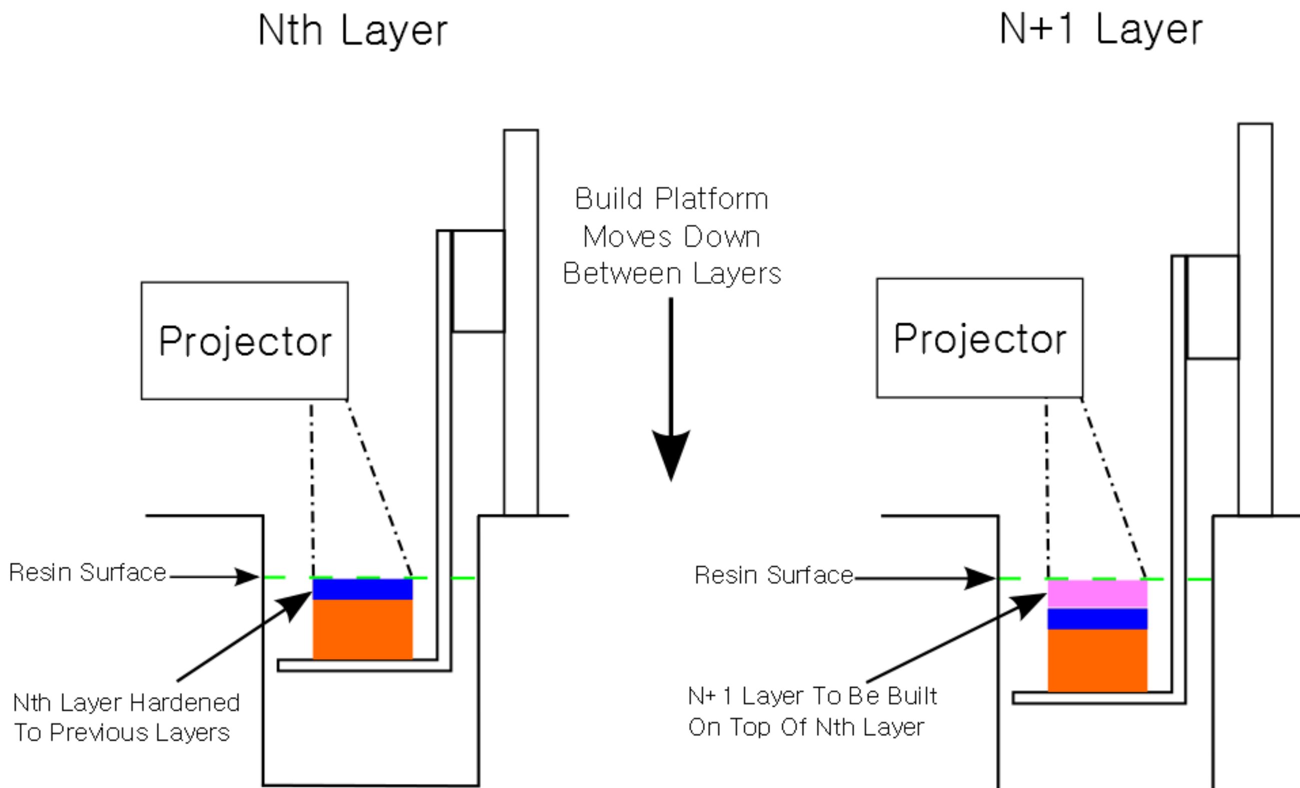

图 **3. Top-Down 3D Printing Method**

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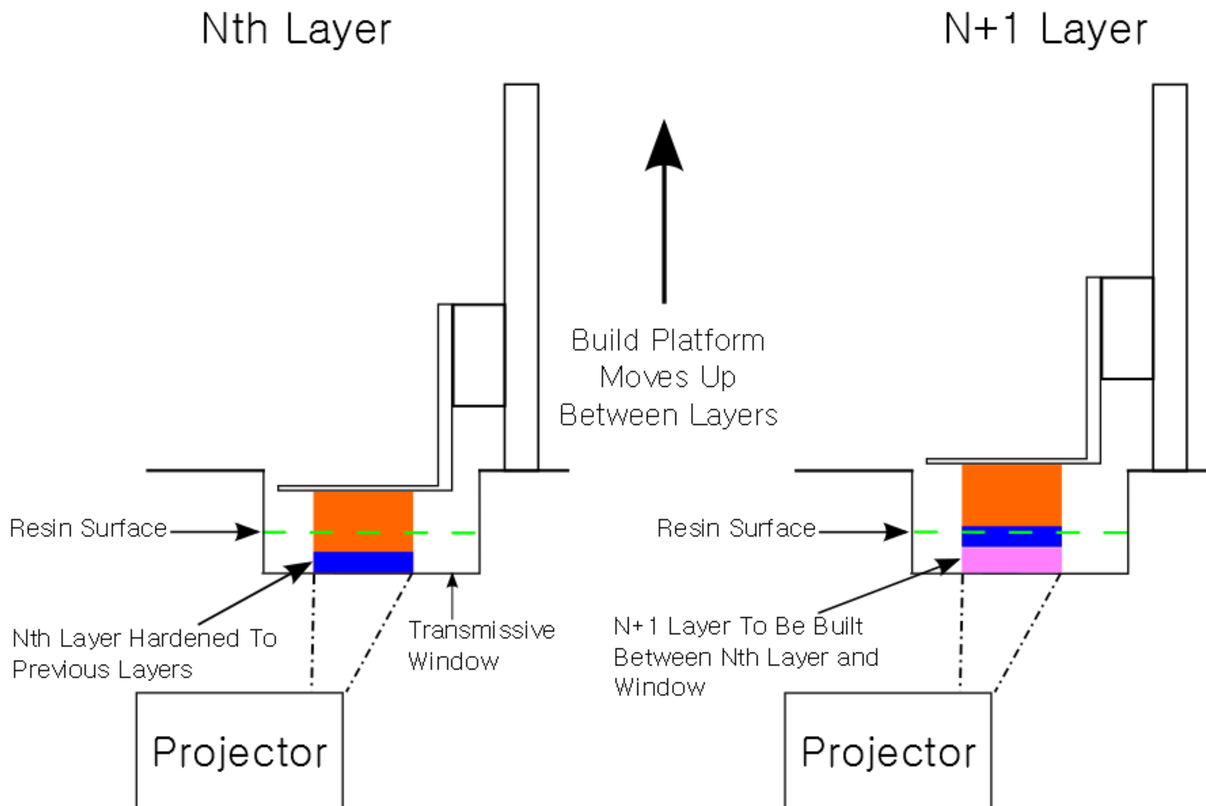

图 4. Bottom-Up 3D Printing Method

The top-down build method has its layer thickness defined by the distance from the build platform - or partially-built object - and the upper surface of the resin. This means the time for the resin's surface layer to return to level after each build platform movement must be considered.

The bottom-up build method is more popular as it solves two key issues: Resin settling time and layer thickness control. The bottom-up build orientation requires the projected layer images to be transmitted through a material into the resin vat from below. The build platform starts flush against the transmissive window and steps upward with each layer. The build platform's orientation to the window means the resin's surface does not impact the build, and the layer thickness is clearly defined between the platform and the window. The bottom-up build requires a smaller volume of resin in the vat at a time but requires the user to constantly refill the vat as resin is used. The challenge of overcoming stiction also exists between the hardened layers and the transmissive window. The solidified resin should separate cleanly, and easily, from the transmissive window or else delicate features may be destroyed during the build process. The resin should adhere strongly to the build platform material as the weight of the object will be suspended from the platform during the build. The bottom-up build method is illustrated in 图 4.

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2.2.2 Object Layer Images

Object layer images can be made by hand using a drawing utility or created by slicing STL file models. STL files are the de facto standard input file for 3D printers, and are readily available in multiple online libraries. STL files can be sliced using the Freesteel slicer utility found under following link. The output image file format recommended is BMP. The output images should have a 16:10 aspect ratio output from the slicer, but need to be resized to the DLP3010 resolution of 1280 × 720. Object features should be colored white and the background should be black. Any white pixels in the object layer images will be printed in the resin.

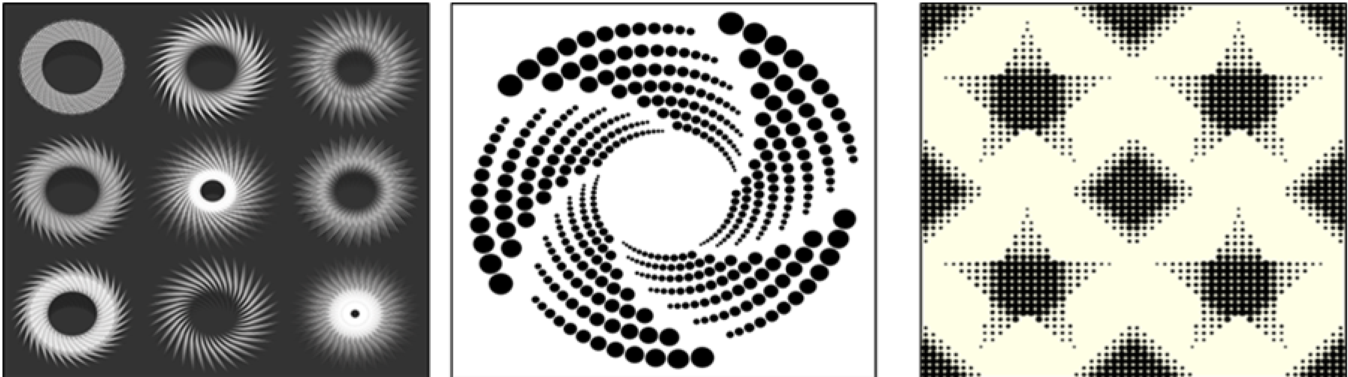

图 5. Example Layer Images

2.3 Highlighted Products

This chipset reference design guide draws upon figures and content from several other published documents related to the 0.3-in 720p DLP chipset. For a list of these documents, see 6 节.

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3 Hardware, Software and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

Assuming default conditions as shipped:

1. Power up the DLP3010 Light Control EVM by applying an external DC power supply (19-V DC, 3.42 A) to the J10 connector. The P5V_VIN (D5) and P3P3V_SB (D6) LED will turn on to indicate that 5-V and 3.3-V standby power is applied.
   External Power Supply Requirements:
   - Nominal output voltage: 19-V DC
   - Minimum output current: 3A; Max output current: 3.42 A
   - Efficiency level: VI

   NOTE: TI recommends using an external power supply that complies with applicable regional safety standards such as UL, CSA, VDE, CCC, PSE, etc.
   NOTE: The system is designed to operate also with an external 12-V DC power supply.
2. Move the SW_ONOFF switch to the ON position to turn the DLP3010 Light Control EVM on. When the DLP3010 Light Control EVM is turned on, the PROJ_ON LED D3 will turn on.
3. After the DLP3010 Light Control EVM is turned on; the projector will default to displaying a DLP Light Control splash image.
4. The focus of the image can be adjusted on the optical engine.

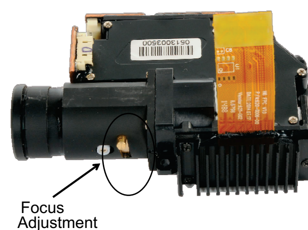

图 6. Optical Engine With Focus Adjustment

5. Connect USB to the DLP3010 Light Control EVM and open the DLP3010 Display and Light Control Graphical User Interface (GUI) on your computer. If needed, connect an HDMI source to the EVM and communicate to the EVM over the GUI software.
6. Via the GUI the EVM can be set to Video Display Mode or Light Control Mode. Install Jumper J11 to set Trigger IN/OUT voltage on the EVM (Jumper is not included by default). Refer to the GUI user's guide for further description.
7. When turning off the projector, turn off the SW_ONOFF switch prior to removing power cable.
   Note: To avoid potential damage to the DMD, it is recommended to turn off the projector with SW_ONOFF before disconnecting the power.

There are ten indicator LEDs on the DLP3010 Light Control EVM, and they are defined in 表 3:

表 3. LEDs on the DLP3010 Light Control EVM

LED Reference	Signal Indication	Description
D1	HOST_IRQ	ON during DLPC3478 boot OFF when projector is running. Indication of DLPC3478 boot-up completed and ready to receive commands
D2	RESETZ	OFF when projector is turned on vie SW_ONOFF
D3	PROJ_ON	On when projector is turned on via SW_ONOFF
D5	P5V_VIN	5-V power applied
D6	P3P3V_SB	Regulated 3V3 power on
D7	MSP2	ON when HDMI cable plugged in and external video detected. OFF when external video is not detected.

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表 **3. LEDs on the DLP3010 Light Control EVM (continued)**

LED Reference	Signal Indication	Description
D8	ACK	ON when Cypress CY3420 is I²C master OFF when MSP430 is I²C master
D9	REQ	ON when Cypress CY3420 requests the MSP430 to give Cypress master control of the I²C bus
D10	GPIO1	Blinking when PC is communicating to flash over SPI
D11	GPIO0	Blinking when PC is communicating to DLPC3478 over I²C

3.1.2 Light Engine

The optical engine in the EVM is developed by Anhua Optoelectronics and is production ready.

The light engine consists of the following components:

- 0.3-inch 720p DMD (DLP3010)
- OSRAM red, green, and blue LED

表 **4. Optical Engine Specifications**

PARAMETER	MIN	TYP	MAX	UNIT
Brightness		125		Lum
LED Current		2.4		A
Brightness Uniformity	75%			
Throw Ratio		1.2		
Offset		100%		

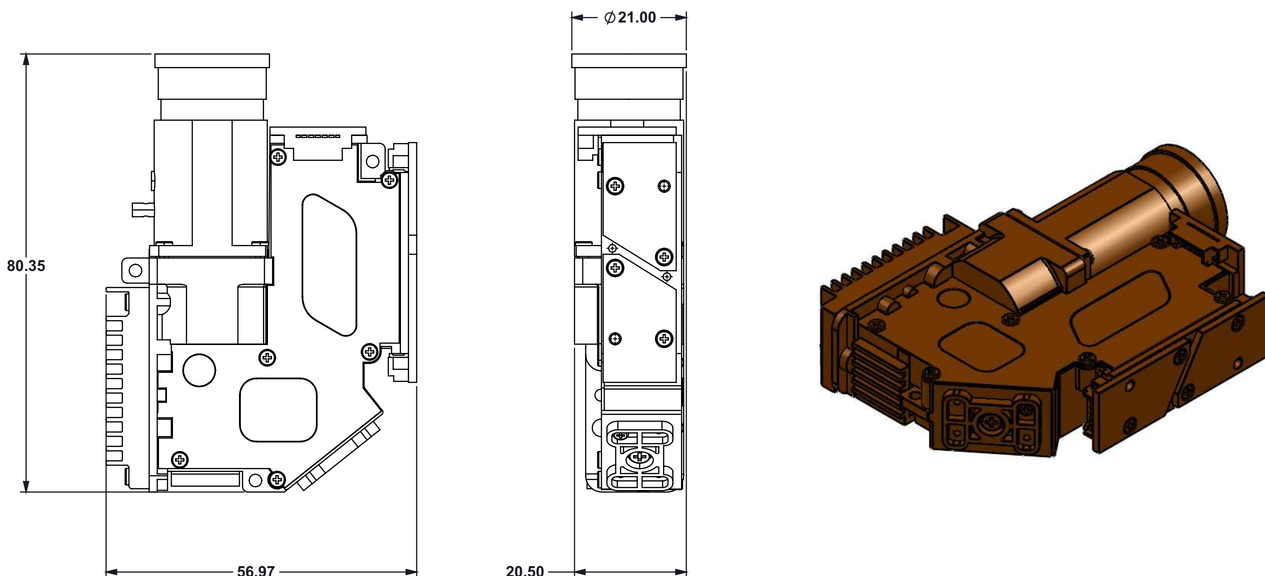

图 **7. DLP3010 Light Control EVM Optical Engine**

3.1.3 Software

The software required for this reference design is available for download on the DLP3010EVM-LC tool folder.

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3.2 Testing and Results

For 3D printer, typically a mono-chrome sequence is used unlike an RGB sequence for a display application. DLPC3478 controller is designed with these requirements in consideration. The timing diagram of a typical sequence for 3D printing applications is shown in 图 8.

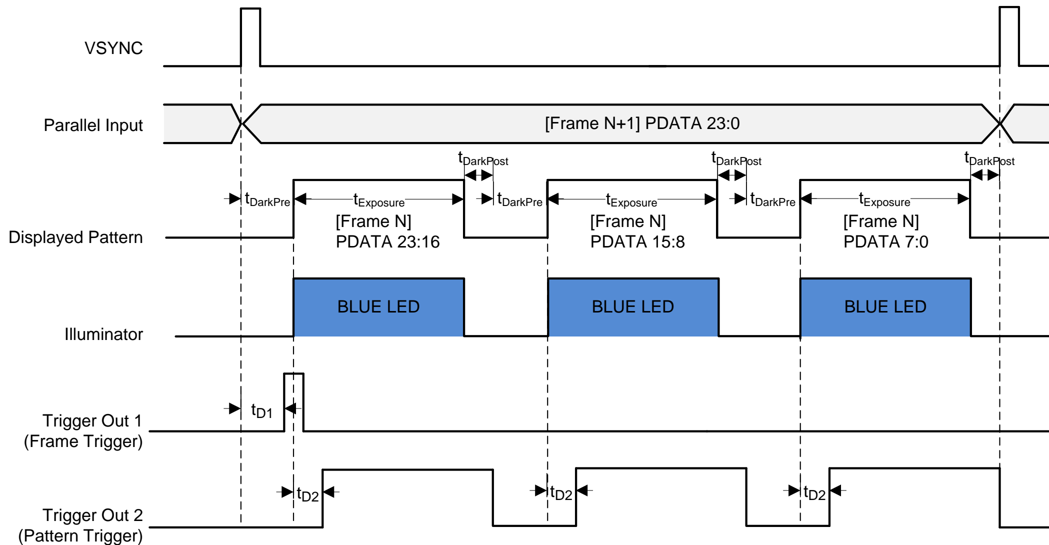

图 8. External Pattern Streaming Timing Sequence (24-bit Monochrome)

This sequence has been verified on the DLP3010 light control EVM. The Trigger Out1 configuration is shown in 图 9.

Trigger Out1

Trigger Out2

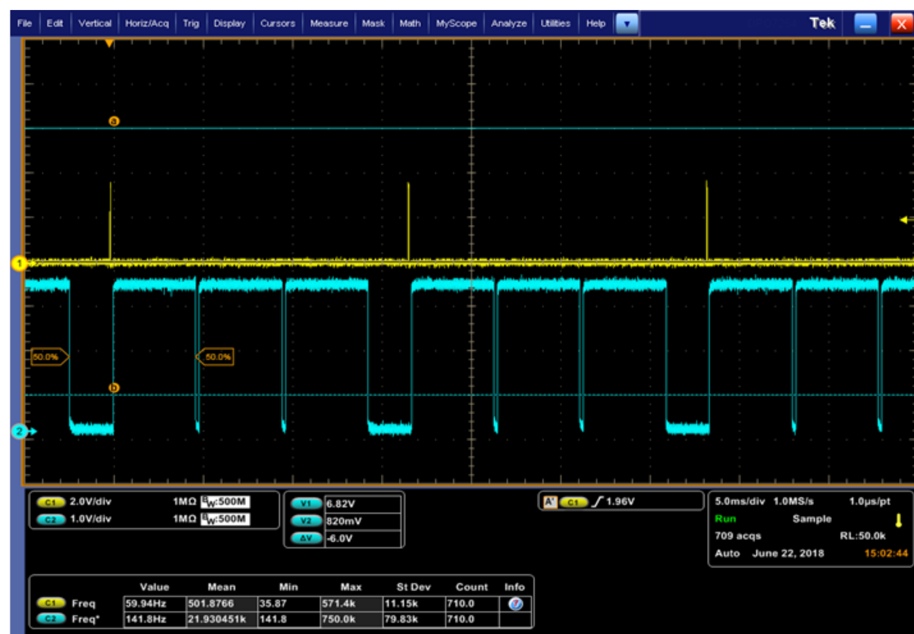

图 9. Scope plots of Trigger Out1 and Trigger Out2 (24-bit Monochrome)

Different types of mono-chrome and RGB images are tested on the light engine for good image quality as shown in 图 10.

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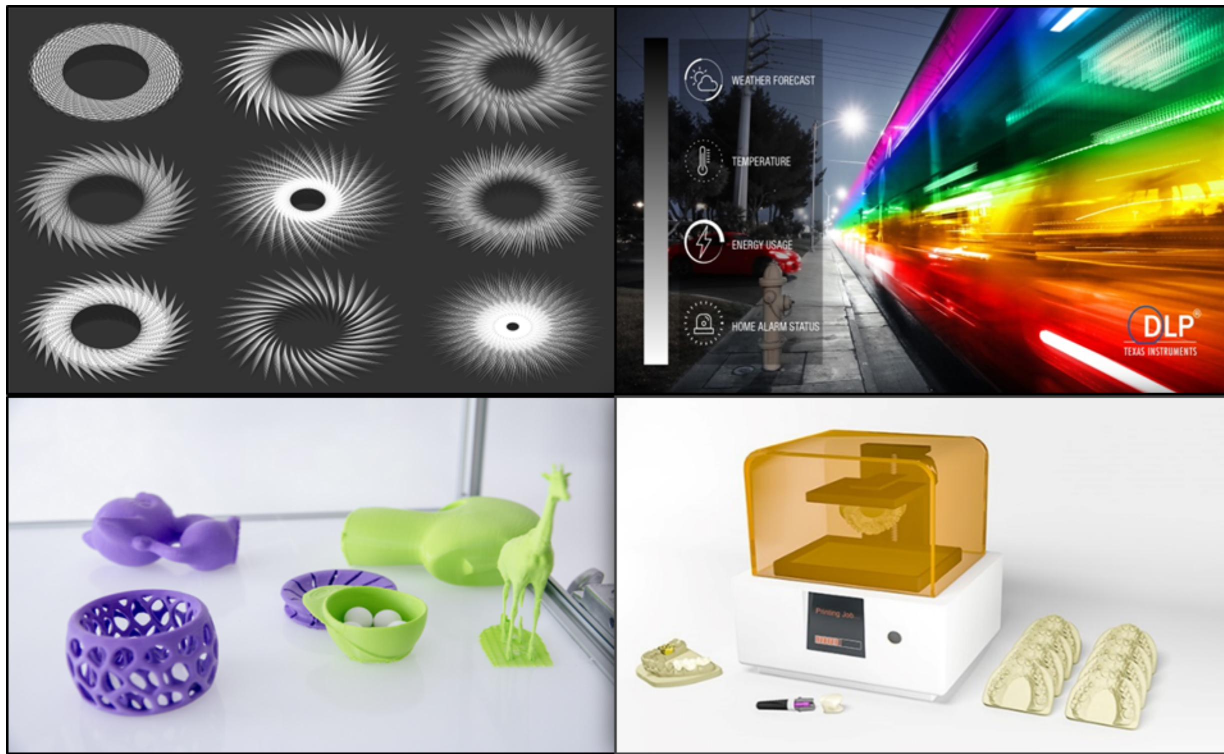

图 **10. Monochrome and RGB Image Testing**

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4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-080003.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-080003.

4.3 PCB Layout Recommendations

The layout guidelines listed in this design guide are subsets of the guidelines included in the component data sheets. For more information, refer to the DLPC3478, DLP3010, and DLPA2005 data sheets.

4.3.1 DLPC3478 Layout Guidelines

4.3.1.1 Internal ASIC PLL Power

The following guidelines are recommended to achieve desired ASIC performance relative to the internal PLL. The DLPC3478 contains two internal PLLs, which have dedicated analog supplies (VDD_PLLM, VSS_PLLM, VDD_PLLD, VSS_PLLD). As a minimum, VDD_PLLx power and VSS_PLLx ground pins must be isolated using a simple passive filter consisting of two series ferrites and two shunt capacitors (to widen the spectrum of noise absorption). It is recommended that one capacitor be a 0.1-µF capacitor and the other be a 0.01-µF capacitor. Place all four components as close to the ASIC as possible; however, it is especially important to keep the leads of the high-frequency capacitors as short as possible. Note that both capacitors must be connected across VDD_PLLM and VSS_PLLM / VDD_PLLD and VSS_PLLD respectfully on the ASIC side of the ferrites.

For the ferrite beads used, their respective characteristics should be as follows:

- DC resistance less than 0.40 Ω
- Impedance at 10 MHz equal to or greater than 180 Ω
- Impedance at 100 MHz equal to or greater than 600 Ω

The PCB layout is critical to PLL performance. It is vital that the quiet ground and power are treated like analog signals. Therefore, VDD_PLLM and VDD_PLLD must be a single trace from the DLPC3478 to both capacitors and then through the series ferrites to the power source. The power and ground traces should be as short as possible, parallel to each other, and as close as possible to each other.

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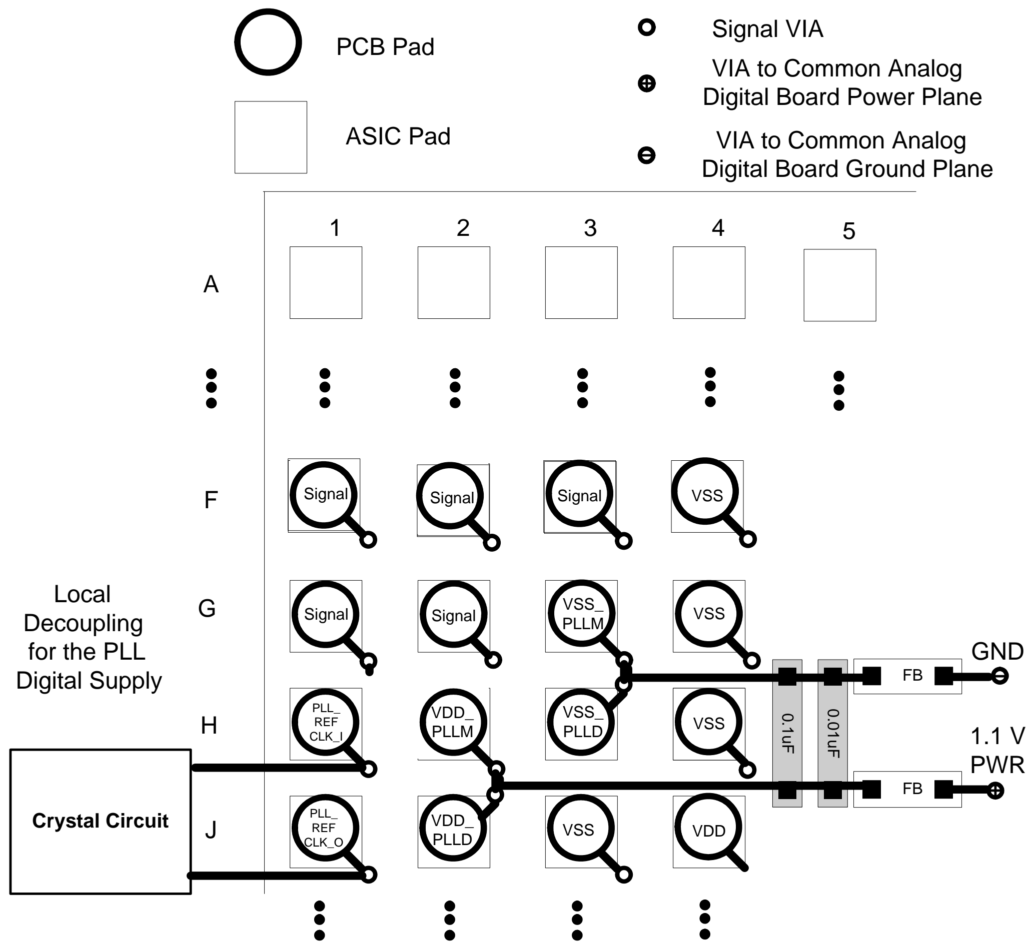

图 11. PLL Filter Layout

4.3.1.2 I²C Interface Performance

Both DLPC3478 I²C interface ports support a 100-kHz baud rate. By definition, I²C transactions operate at the speed of the slowest device on the bus, thus there is no requirement to match the speed grade of all devices in the system.

4.3.1.3 DMD Interface Considerations

The sub-LVDS HS interface waveform quality and timing on the DLPC3478 ASIC is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

Setup Margin = (DLPC3478 output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation) (1)

Hold-time Margin = (DLPC3478 output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation)

where PCB SI degradation is signal integrity degradation due to PCB effects, which includes such things as simultaneously switching output (SSO) noise, crosstalk, and inter-symbol interference (ISI) noise. (2)

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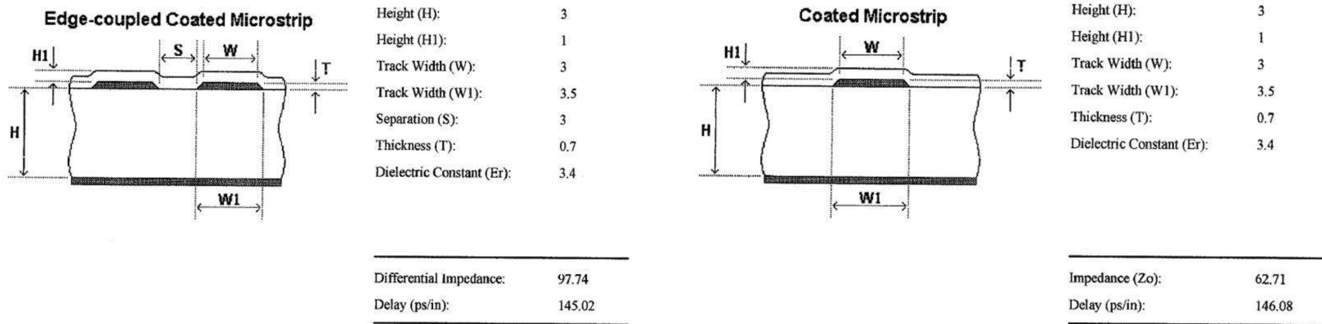
DLPC3478 I/O timing parameters as well as DMD I/O timing parameters can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. However, PCB SI degradation is a more complicated adjustment.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines are provided as a reference of an interconnect system that satisfy both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Variation from these recommendations can also work, but must be confirmed with PCB signal integrity analysis or lab measurements.



DMD_HS Differential Signals DMD_LS Signals

图 12. DMD Interface Board Stack-Up Details

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4.3.1.4 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends to tie unused ASIC input pins through a pullup resistor to their associated power supply or a pulldown resistor to ground. For ASIC inputs with internal pullup or pulldown resistors, do not add an external pullup or pulldown resistor unless specifically recommended.

注: Internal pullup and pulldown resistors are weak and must not be expected to drive the external line. The DLPC3478 device implements very few internal resistors, and these are noted in the pin list. When external pullup or pulldown resistors are needed for pins that have built-in weak pullups or pulldowns, use the value 8 kΩ (max).

Never tie unused output-only pins directly to power or ground. These pins can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins can become an input, then the pins must be pulled up (or pulled down) using an appropriate, dedicated resistor.

4.3.1.5 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

表 5. Max Pin-to-Pin PCB Interconnect Recommendations[1][2]

DMD BUS SIGNAL	SIGNAL INTERCONNECT TOPOLOGY		UNIT
	SINGLE BOARD SIGNAL ROUTING LENGTH	MULTI-BOARD SIGNAL ROUTING LENGTH	
DMD_HS_CLK_P DMD_HS_CLK_N	6.0 152.4	See [3]	inch (mm)
DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N	6.0 152.4	See [3]	inch (mm)
DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N			
DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N			
DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N			
DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N			
DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N			
DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N			
DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N			
DMD_LS_CLK	6.5 165.1	See [3]	inch (mm)
DMD_LS_WDATA	6.5 165.1	See [3]	inch (mm)
DMD_LS_RDATA	6.5 165.1	See [3]	inch (mm)
DMD_DEN_ARSTZ	7.0 177.8	See [3]	inch (mm)

(1) Max signal routing length includes escape routing.
(2) Multi-board DMD routing length is more restricted due to the impact of the connector.
(3) Due to board variations, these are impossible to define. Any board designs should SPICE simulate with the ASIC IBIS models to ensure single routing lengths do not exceed requirements.

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表 6. High Speed PCB Signal Routing Matching Requirements(1)(2)(3)(4)

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH(5)	UNIT
DMD	DMD_HS_WDATA_A_P DMD_HS_WDATA_A_N DMD_HS_WDATA_B_P DMD_HS_WDATA_B_N DMD_HS_WDATA_C_P DMD_HS_WDATA_C_N DMD_HS_WDATA_D_P DMD_HS_WDATA_D_N DMD_HS_WDATA_E_P DMD_HS_WDATA_E_N DMD_HS_WDATA_F_P DMD_HS_WDATA_F_N DMD_HS_WDATA_G_P DMD_HS_WDATA_G_N DMD_HS_WDATA_H_P DMD_HS_WDATA_H_N	DMD_HS_CLK_P DMD_HS_CLK_N	±1.0 (±25.4)	inch (mm)
DMD	DMD_HS_WDATA_x_P	DMD_HS_WDATA_x_N	±0.025 (±0.635)	inch (mm)
DMD	DMD_HS_CLK_P	DMD_HS_CLK_N	±0.025 (±0.635)	inch (mm)
DMD	DMD_LS_WDATA DMD_LS_RDATA	DMD_LS_CLK	±0.2 (±5.08)	inch (mm)
DMD	DMD_DEN_ARSTZ	N/A	N/A	inch (mm)

(1) These values apply to PCB routing only. They do not include any internal package routing mismatch associated with the DLPC3478 or the DMD.
(2) DMD HS data lines are differential, thus these specifications are pair-to-pair.
(3) Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
(4) DMD LS signals are single ended.
(5) Mismatch variance for a signal group is always with respect to reference signal.

4.3.1.6 Number of Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair must not change layers.

4.3.1.7 Stubs

- Avoid stubs.

4.3.1.8 Terminations

- No external termination resistors are required on DMD_HS differential signals.
- The DMD_LS_CLK and DMD_LS_WDATA signal paths must include a 43-Ω series termination resistor located as close as possible to the corresponding ASIC pins.
- The DMD_LS_RDATA signal path must include a 43-Ω series termination resistor located as close as possible to the corresponding DMD pin.
- DMD_DEN_ARSTZ does not require a series resistor.

4.3.1.9 Routing Vias

- Minimize the number of vias on DMD_HS, DMD_LS_CLK, and DMD_LS_WDATA signals to not

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exceed two.

- Any and all vias on these signals must be located as close to the ASIC as possible.

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4.3.2 DLPA2005 Layout Guidelines

4.3.2.1 Layout Guidelines

As for all chips with switching power supplies, the layout is an important step in the design, especially in the case of high peak currents and high switching frequencies. If the layout is not carefully done, the regulators could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current paths and for the power ground tracks. Input capacitors, output capacitors, and inductors should be placed as close as possible to the IC.

图 13 shows an example layout that has critical parts placed as close as possible to the pins they are connected to. Here are recommendations for the following components:

R1	is RLIM and is connected via a wide trace (low resistance) to the system ground. The analog ground at pin 5 should be star connected to the point where RLIM is connected to the system ground. Aim on a wide and low-ohmic trace as well, although this one is less critical (tens of mA).
L1	is the big inductor for the VLED that is connected via two wide traces to the pins
C4	are the decoupling capacitors for the VLED and they are as close as possible placed to the part and directly connected to ground.
L3/C20	are components used for the VCORE BUCK. L3 is placed close to the pin and connected with a wide trace to the part. C20 is placed directly beside the inductor and connected to the PGND pin
L2	This inductor is part of the DMD reset regulators and is also placed as close as possible to the DLPA2005 using wide PCB traces.

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4.3.2.2 Layout Example

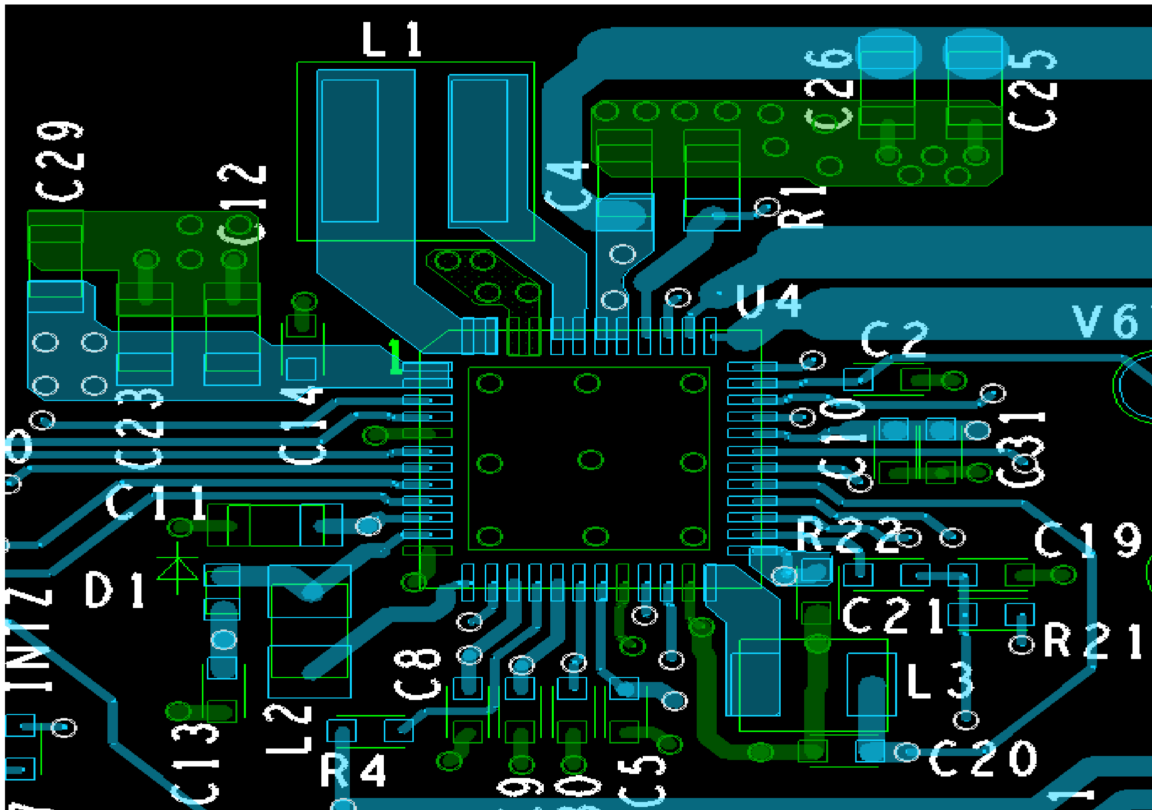

图 13. Example Layout of DLPA2005

4.3.2.3 Thermal Considerations

An important consequence of the efficiency numbers shown in 图 14.

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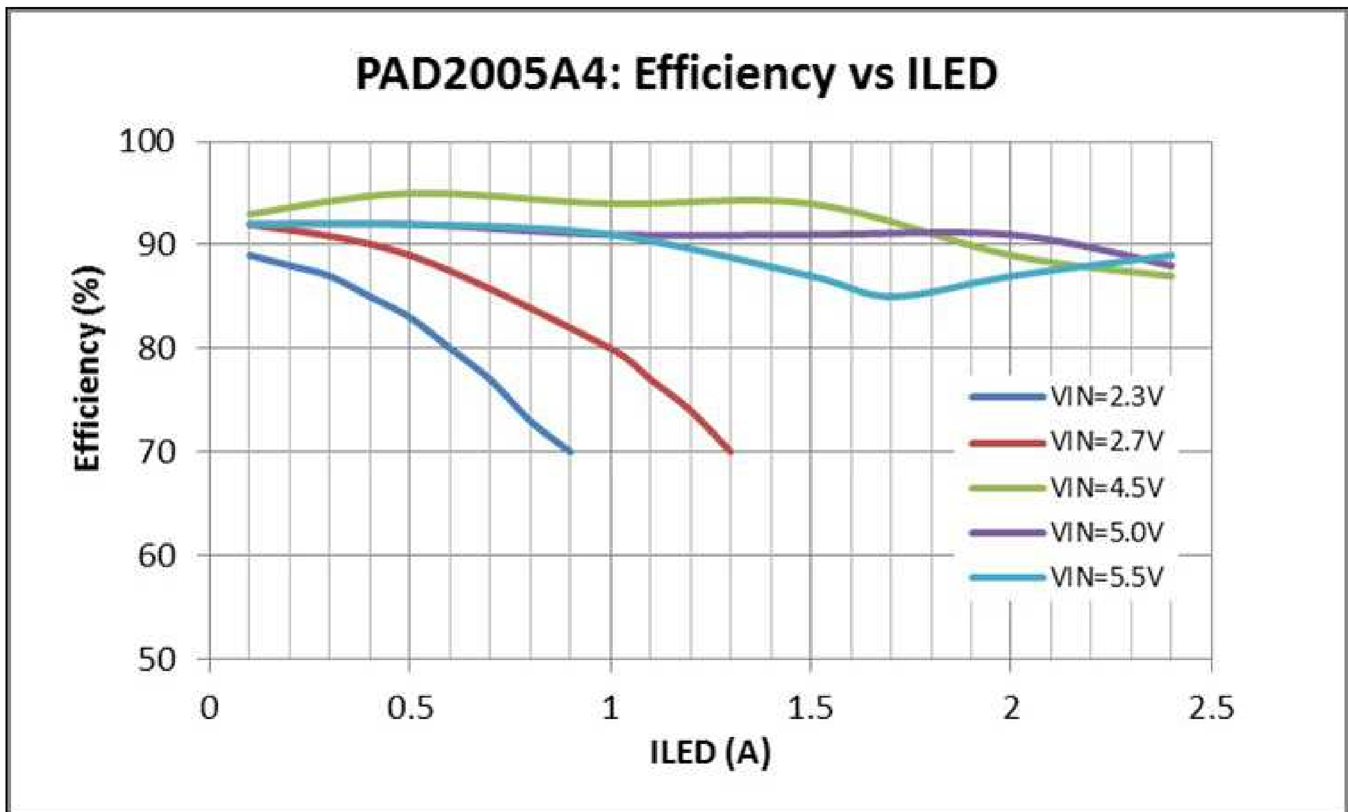

图 14. Measured Typical Power Converter Efficiency as a Function of ILED for Several Supply Voltages (V_{OUTmax} = 4.8 V for Each Supply)

is that it enables to perform DLPA2005 thermal calculations. Since the efficiency is not 100%, power is dissipated in the DLPA2005 chip. Due to that dissipation die temperature will rise. For reliability reasons it is good to aim for as low as possible die temperatures. Using a heat sink and airflow are efficient means to keep die temperature reasonably low. In cases that airflow and / or a heat sink are / is not feasible, the system designer should specifically pay attention to the thermal design. The die temperature for regular operation should remain below 120°C.

In the following an example is given of such a thermal calculation. The calculation starts with summarizing all blocks in the DLPA2005 that dissipate. Clearly, the buck-boost converter supplying the LED power is the main source of dissipation. For illustrating purposes here we assume this buck-boost converter to be the only block that dissipates significantly. For the example assume: VOUT=4.8 V (for all three LEDs), IOUT=2.4 A and VIN=5 V. From 图 14 it can be derived that the related efficiency equals about n_{eff}=88%.
The power dissipated by the DLPA2005 is then given by:

$$P_{DISS} = P_{IN} - P_{OUT} = P_{OUT}\left(\frac{100\%}{\eta_{eff}} - 1\right) = 4.8V \cdot 2.4A \cdot \left(\frac{100\%}{88\%} - 1\right) = 1.6W$$

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The rise of die temperature due to this power dissipation can be calculated using the thermal resistance from junction to ambient, M JA=27.9°C/W. This calculation yields:

$$T_{JUNCTION} = T_{AMBIENT} + P_{DISS} \cdot \theta_{JA} = 25°C + 1.6W \cdot 27.9°C / W = 69.6°C$$

It is also possible to calculate the maximum allowable ambient temperature to prevent surpassing the maximum die temperature. Assume again the dissipation of PDISS=1.6W. The maximum ambient temperature that is allowed is then given by:

$$T_{AMBIENT-\max} = T_{JUNCTION-\max} - P_{DISS} \cdot \theta_{JA} = 120°C - 1.6W \cdot 27.9°C / W = 75.4°C$$

It is again stressed here that for proper calculations the total power dissipation of the PAD2005 should be taken into account. On top of that, if components that are close to the PAD2005 also dissipate a significant amount of power, the (local) ambient temperature can be higher than the ambient temperature of the system.

If calculations show that the die temperature will surpass the maximum specified value, two basic options exist:

- Adding a heat sink with or without airflow. This will reduce 0_{JA} yielding lower die temperature.
- Lowering the dissipation in the PAD2005 implying lowering the maximum allowable LED current.

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4.3.3 DMD Flex Cable Interface Layout Guidelines

There are no specific layout guidelines for the DMD as typically DMD is connected using a board-to-board connector with a flex cable. The flex cable provided the interface of data and control signals between the DLPC3478 controller and the DLP3010 DMD.

Follow these layout guidelines for the flex cable interface with the DMD:

- Match lengths for the LS_WDATA and LS_CLK signals.
- Minimize vias, layer changes, and turns for the HS bus signals. See 图 15.
- Minimum of two 100-nF decoupling capacitor close to VBIAS. Capacitor C6 and C7 in 图 15.
- Minimum of two 100-nF decoupling capacitor close to VRST. Capacitor C9 and C8 in 图 15.
- Minimum of two 220-nF decoupling capacitor close to VOFS. Capacitor C5 and C4 in 图 15.
- Minimum of four 100-nF decoupling capacitor close to Vcci and Vcc. Capacitor C1, C2, C3, and C10 in 图 15.

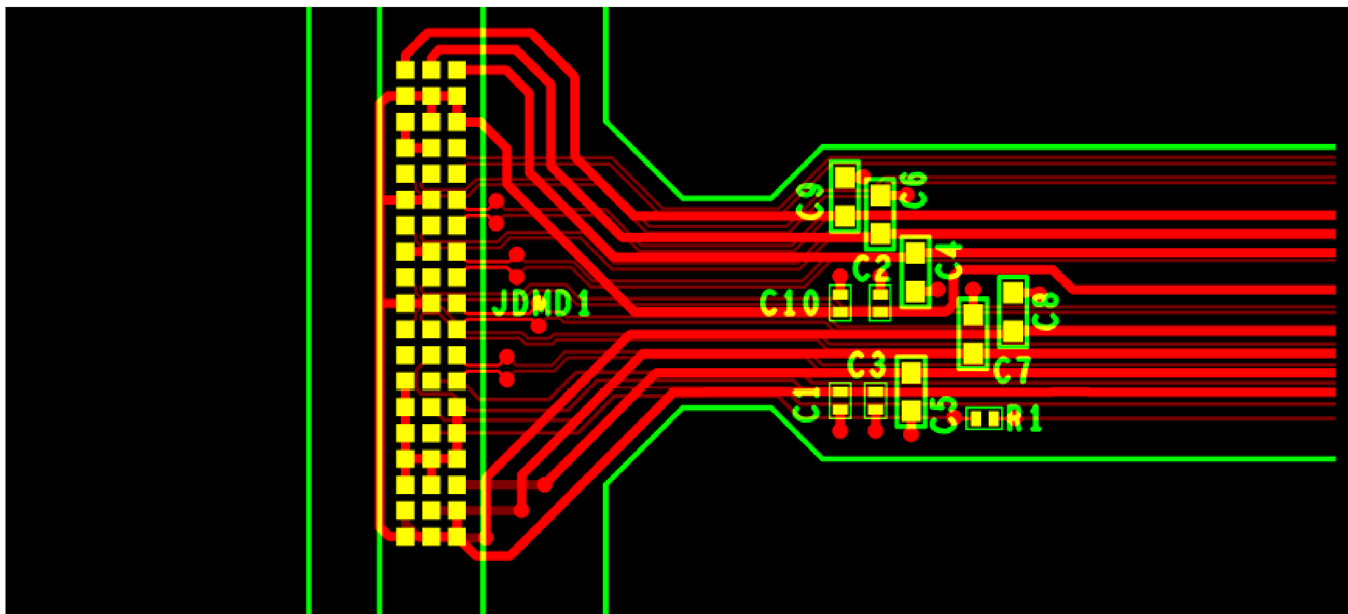

图 15. Power Supply Connections

4.3.4 Layout Prints

To download the layer plots, see the design files at TIDA-080003.

4.4 Cadence Project

To download the Cadence project files, see the design files at TIDA-080003.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-080003.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-080003.

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5 Software Files

To download the software files, see the design files at DLP3010EVM-LC.

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6 Related Documentation

1. Texas Instruments, *DLP3010 Light Control EVM User's Guide*
2. Texas Instruments, *DLPC3478 Display and Light Controller Data Sheet*
3. Texas Instruments, *DLP3010 (0.3 720p DMD) Data Sheet*
4. Texas Instruments, *DLPA2005 PMIC and LED/Lamp Driver IC Data Sheet*

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