TI Designs：TIDA-01565
有线 OR 多路复用器和 PGA 参考设计

说明

该板演示了 OPA837 运算放大器的有线 OR 多路复用器 (MUX) 和可编程增益放大器 (PGA) 应用。这些 应用 通过放大器的高阻抗输出和高阻抗反相输入实现（处于断电 (PD) 模式）。可以使用板载双列直插式封装 (DIP) 开关或 SMA 连接器的晶体管逻辑输入来选择多路复用器或 PGA 的输出。该板兼容单电源或双电源，电压高达 5.25V。输出端包含一个可选的噪声滤波器，用于消除带宽较低的 PGA 设计的宽带噪声。

资源

TIDA-01565	设计文件夹
OPA837	产品文件夹
SN74LVC1G139	产品文件夹
SN74LVC2G04	产品文件夹
TLV2362	产品文件夹

TI E2E™ Community

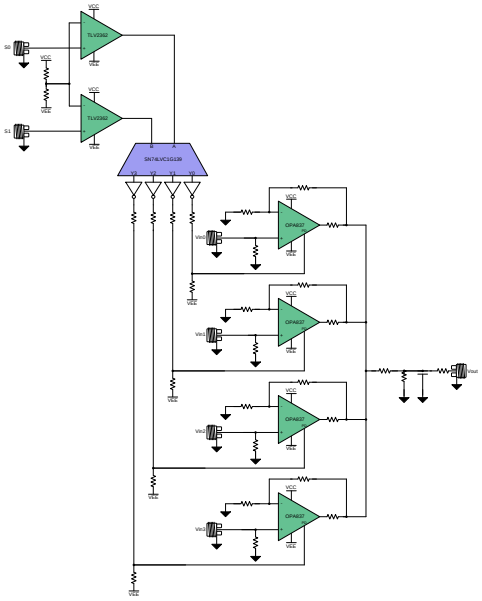
咨询我们的 E2E 专家

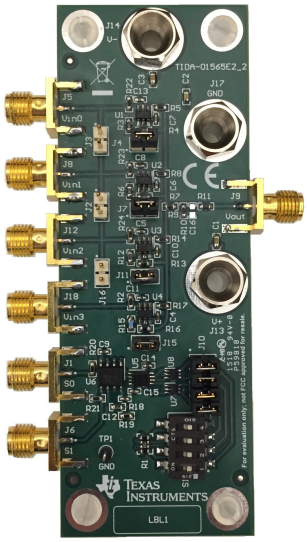
特性

- 在多路复用器和 PGA 配置之间进行了更改
- 通过单电源或双电源进行驱动
- 补充性 DIP 开关输入可提供简单的输出选择
- 实现了真正的输入与输出隔离

应用

- 宽动态范围采集系统
- 多通道输入数据采集
- 模拟视频多路复用器





该 TI 参考设计末尾的重要声明表述了授权使用、知识产权问题和其他重要的免责声明和信息。

TIDUDJ0 — http://www-s.ti.com/sc/techlit/TIDUDJ0

1 System Description

High-speed analog multiplexers are required in a wide range of applications such as data acquisition, video multiplexing, and so forth. TIDA-01565 is a basic analog multiplexing or programmable gain amplifier circuit using the OPA837. When disabled, an internal switch opens from the inverting input through the active channel, creating isolation between the input and the output. This isolation allows the OPA837 to act as a high-speed analog MUX.

A PGA is an amplifier where the gain can be externally controlled instead of using a single preset gain. This board supports this using the OPA837 devices as a PGA by tying the inputs together. Setting different gain settings for each OPA837 allows the user to have a PGA with four different gain settings. Similarly to controlling the MUX channel output, the gain setting is controlled by selecting which device turns on from the onboard DIP switch or controlling S0 and S1. For more details on configuring the board for PGA mode, see 节 4.2.1.2.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER	SPECIFICATIONS
Input power source	±2.5 V
Unity-gain bandwidth	105 MHz
Gain bandwidth product	50 MHz
Turnon time delay	300 ns
Turnoff time delay	100 ns
Multiplexer	4:1

2 System Overview

2.1 Block Diagram

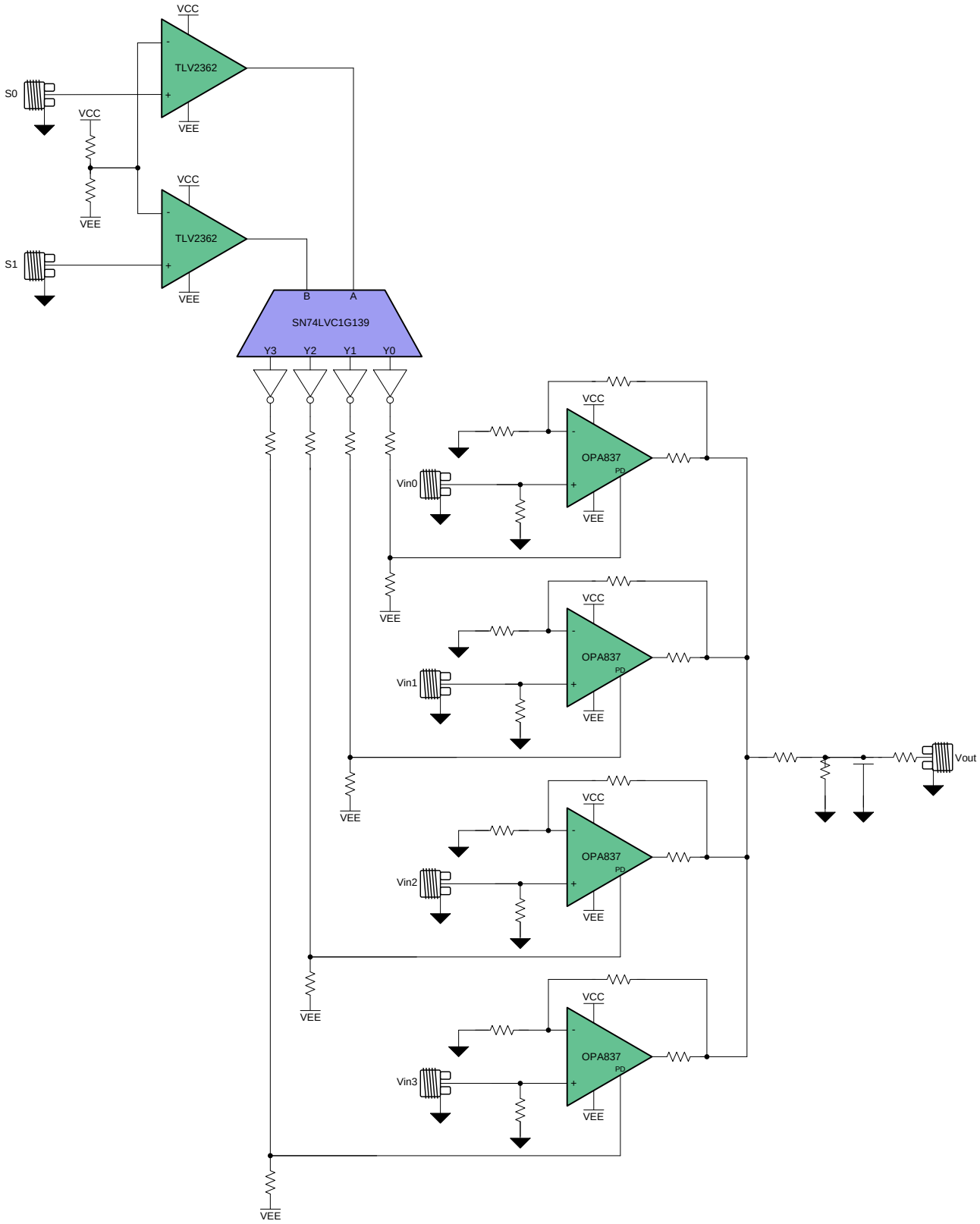


图 1. TIDA-01565 Block Diagram

2.2 Highlighted Products

2.2.1 OPA837

- Bandwidth: 105 MHz (AV = 1 V/V)
- Very Low (Trimmed) Supply Current: 600 µA
- Gain Bandwidth Product: 50 MHz
- Slew Rate: 105 V/µs
- Negative Rail Input, Rail-to-Rail Output
- Single-Supply Operating Range: 2.7 V to 5.4 V
- 25°C Input Offset: ±130 µV (Maximum)
- Input Offset Voltage Drift (DCK Package): < ±1.6 µV/°C (Maximum)
- Input Voltage Noise: 4.7 nV/√Hz (> 100 Hz)
- HD2: –120 dBc at 2 VPP, 100 kHz
- HD3: –145 dBc at 2 VPP, 100 kHz
- Settling Time: 35 ns, 0.5-V Step to 0.1%
- 5-µA Shutdown Current With Fast Recovery From Shutdown for Power-Scaling Applications
- Built-In Disable PD Pin
- When the device is powered down, the internal switch opens the inverting input

2.2.2 SN74LVC1G139

- A logic low 2-to-4 line decoder or demultiplexer
- Controls all four PD pins on the OPA837
- Short propagation delay times

2.2.3 SN74LVC2G04

- Dual inverter gate
- Inverts the logic from the SN74LVC1G139 to a logic high rather than a logic low

2.2.4 TLV2362

- Wide Bandwidth
- Wide Output Voltage Swing
- High Slew Rate

3 System Design Theory

3.1 OPA837 Power-Down

The OPA837 is selected because the device isolates the output from the signal in PD mode. Unlike most high-speed op amps that have a PD function place a high-impedance on only on the output when the amplifier is disabled, the OPA837 places a high-impedance on the output as well as an internal switch opening on the inverting input as seen in 图 2. This creates true input to output isolation.

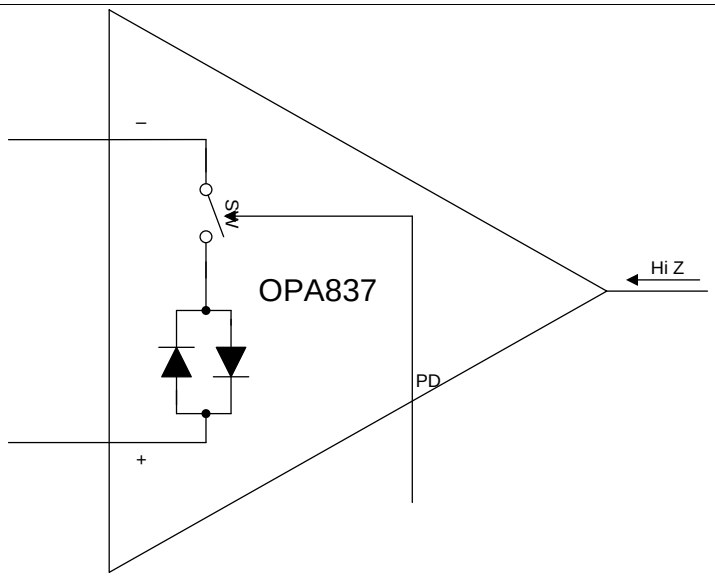


图 2. OPAx837 Power-Down Internal Switch

The turnon and turnoff time delay varies slightly from device to device. The turnoff time must be faster than the turnon time. This helps prevent two of the OPA837 devices from operating at the same time and prevents any possible damage.

To enable the OPA837, the PD pin must be higher than 1.5 V above the negative voltage rail.

图 3, 图 4, and 图 5 show that the output of the amplifier has little delay when a single ±2.5-V pulse is inserted into the PD pin of the OPA837. 图 3 shows that the OPA837 output as a high voltage spike before settling down. 节 *4.2.2* shows that this causes a noticeable distortion to the signal.

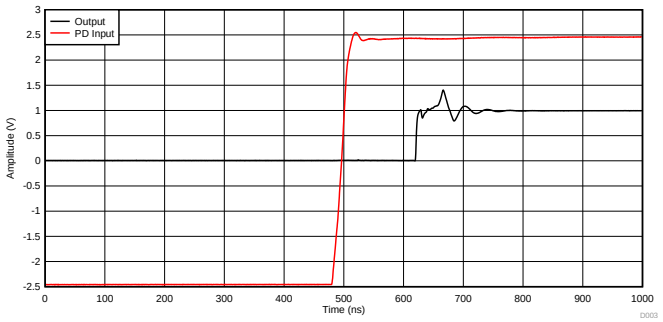


图 3. Direct PD Control: Rising Edge

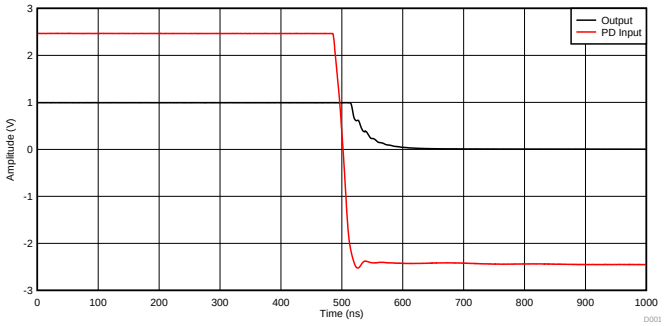


图 4. Direct PD Control: Falling Edge

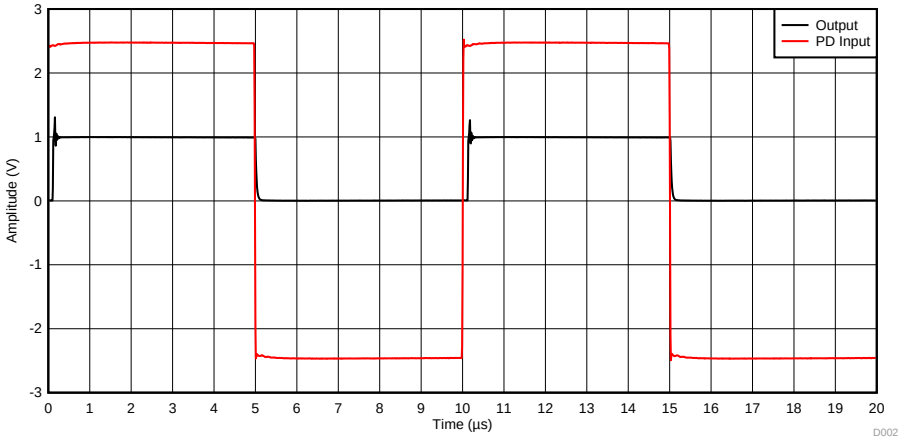


图 5. Direct PD Control: Full Pulse

3.2 Power-Down Control Circuit

The PD control circuit is essential to switch between the four OPA837 devices. The device has a 4-bit switch, but the SMA input logic control is more practical for a system with a microcontroller to control switching.

Using this built-in circuit, two inputs (S0 and S1) are required to control all four channels because of an onboard 2-to 4-bit demultiplexer. The SN74LVC1G139 has a logic low output, so an inverter along the signal path is required to output a logic high. 表 2 lists the truth table for the system after the inverters.

表 **2. Power-Down Control Circuit Truth Table**

S1	S0	CHANNEL THAT PASSES ARGUMENT
0	0	Channel 1
0	1	Channel 2
1	0	Channel 3
1	1	Channel 4

The results in 图 6 and 图 7 were achieved by applying a ±1-V 100-kHz input signal on S0 while leaving S1 floating. The output is taken on the output of the SN74LVC2G04 inverters. As shown in 3.1 节, the OPA837 must have a voltage applied to the PD pin that is 1.5 V above the negative voltage rail to turn on. In this case, 0 V satisfies this parameter and the device powers on. This circuit introduces a delay to the PD response of approximately 0.7 µs to 0.8 µs.

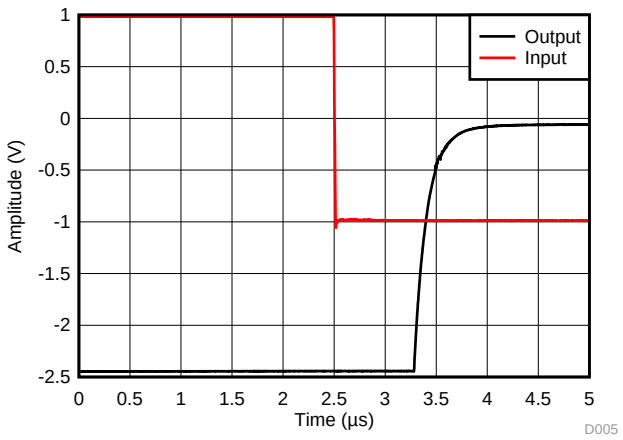


图 **6. PD Control Circuit: Rising Edge**

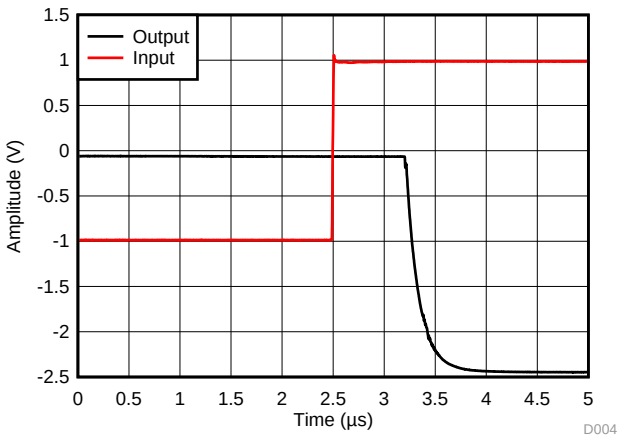


图 **7. PD Control Circuit: Falling Edge**

3.3 Different Configurations

3.3.1 MUX Operation

The TIDA-01565 is configured as a MUX with the support of up to four channels. The default is set to unity gain but can change based on system requirements. At unity gain, the system has a small-signal bandwidth of 105 MHz. 图 8 shows a simplified block diagram of the MUX circuit.

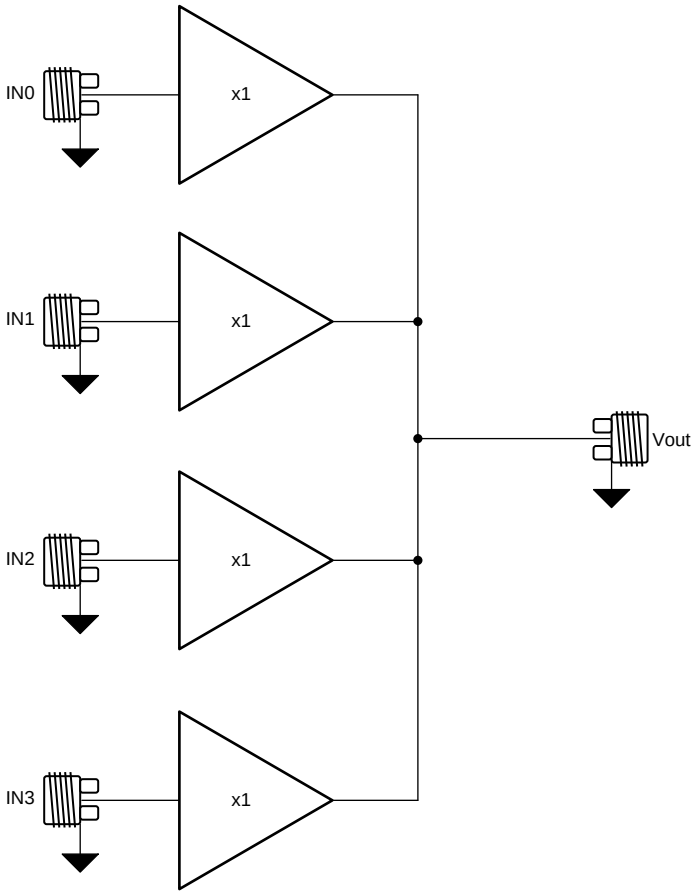


图 8. MUX-OR Block Diagram

3.3.2 PGA Operation

PGA operations are similar to the MUX operations described above except with two differences:

- The inputs are tied together, so the system requires one input.
- Generally, the OPA837 is set up with a different gain setting for each channel.

图 9 shows a simplified block diagram of the PGA mode with arbitrary gain settings.

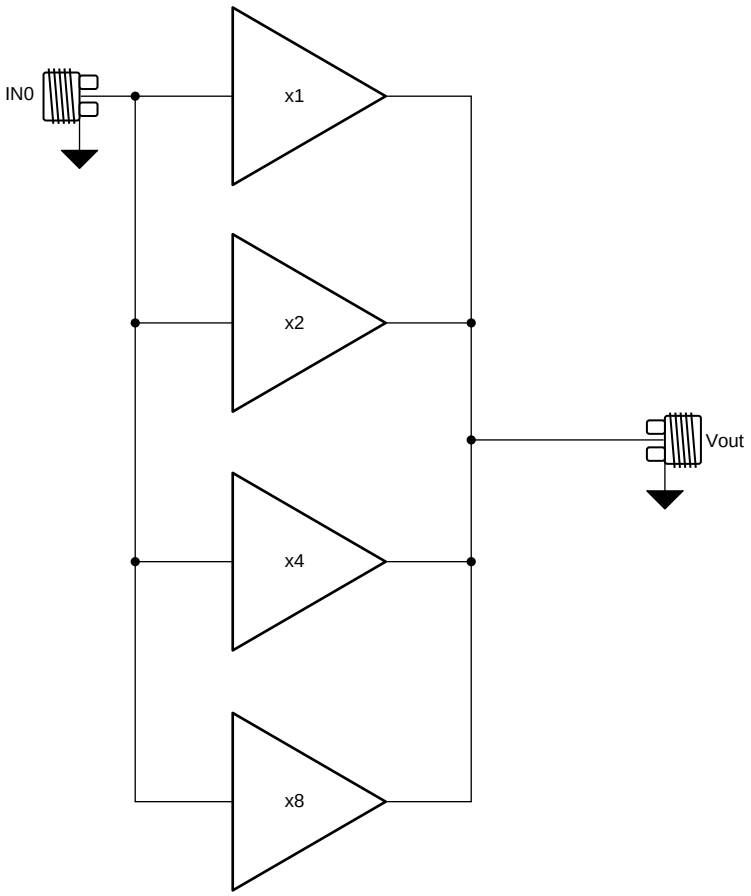


图 **9. PGA Block Diagram**

4 Hardware, Software, Testing Requirements, and Test Results

4.1 Required Hardware

表 3 lists the connector designator and the connector type.

表 **3. Connector Details for TIDA-01565**

CONNECTOR	TYPE OF CONNECTOR
J13	V+
J14	V–
J17	GND
J5, J8, J12, J18	Inputs (Vin0, Vin1, Vin2, Vin3)
J9	Output (Vout)
J1, J6	PD control inputs (S0, S1)
J10	Switch isolator jumpers
J2, J3, J16	Input tie jumpers
J4, J7, J11, J15	Unity-gain jumpers

4.2 Testing and Results

图 10 and 图 11 show the hardware setup diagram for evaluating the reference design for MUX operations and PGA operations, respectively. A **Lecroy** Pulse Generator 9210 generates two ±1-V, 100-kHz square wave to control S0 and S1. A generic dual or triple DC power supply generates a ±2.5-V supply voltage. The PGA tests use a G5100A function generator. For the MUX tests, a 1-V supply was connected to Vin0 and a –1-V supply was connected to Vin1, Vin2, and Vin3 to show the switching behavior. To show the full output swing without attenuating the output, set the oscilloscope to 1 MΩ and set the output resistor with a 20-kΩ to ground.

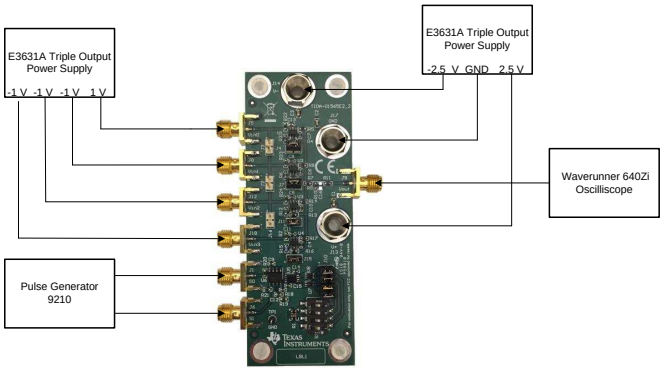


图 10. MUX Hardware Configuration

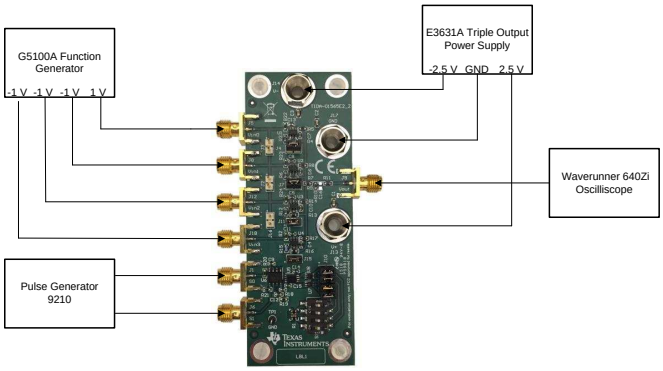


图 11. PGA Hardware Configuration

4.2.1 Test Setup

Switches or logic can control the MUX or PGA. To use the switches, disconnect the four jumpers in J10 and ensure all four switches in S1 are OFF before applying power. Then, switch on one amplifier at a time. There are make-before-break protection resistors to protect the amplifiers from damage if two are switched on at the same time. To use the logic, set all switches in S1 to OFF and connect the first two jumpers on S1. Use a logic signal to select channels 1 or 2 using SMA input J16. The logic input comparator supports single-supply 2-V to 5-V logic and ±2.5-V dual-supply logic.

To analyze resistive and capacitive load driving, use R9, R10, R11, and C16 for loading and measurement impedance matching. As shown in 图 12 to directly connect to an ADC, remove R10 and replace R9 with a 0-Ω resistor and then connect the output to the input of an ADC filter. As an alternative option, configure R9 and C16 as the input filter for the ADC.

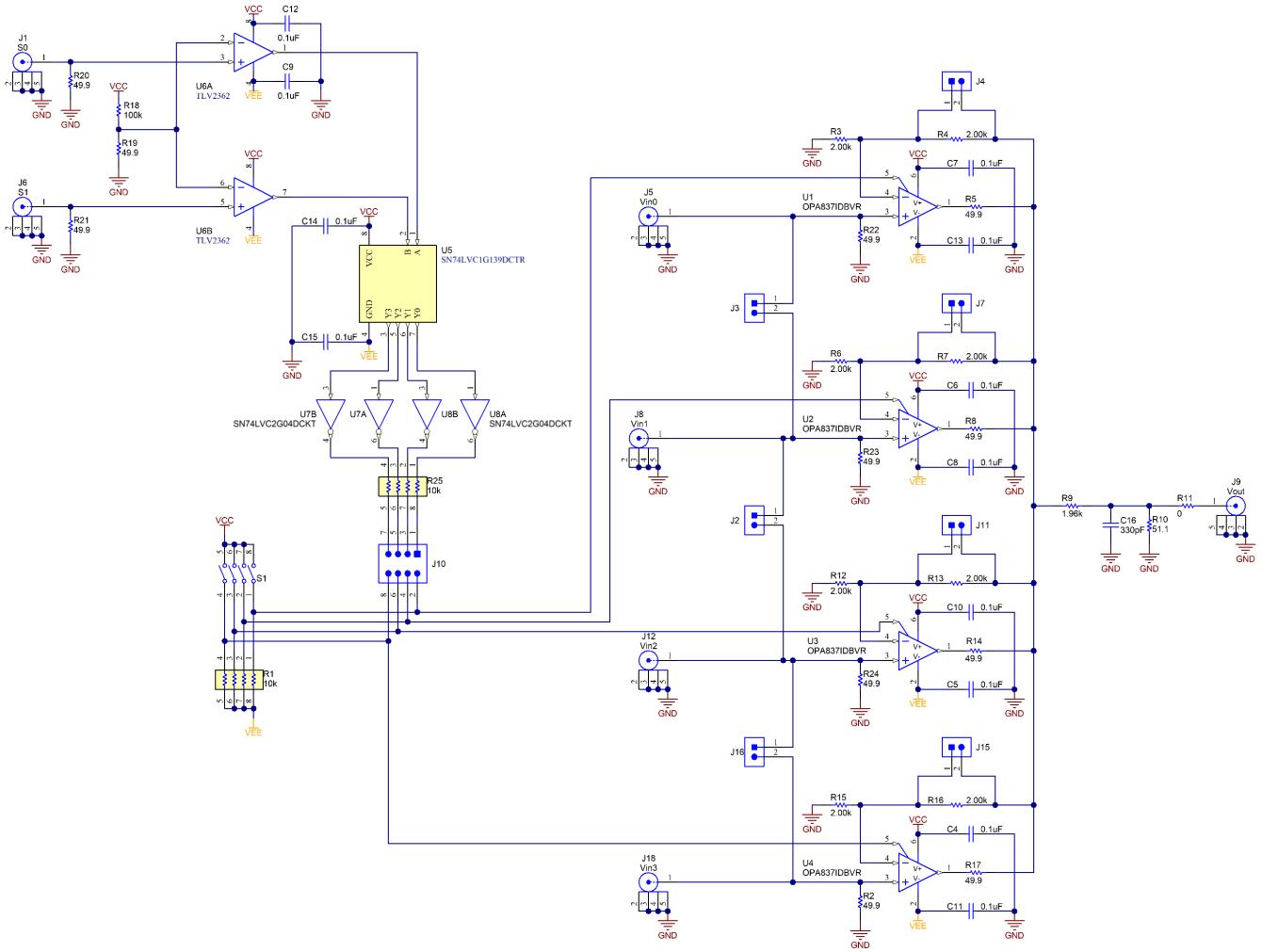


图 **12. TIDA-01565 Schematic**

4.2.1.1 MUX Test Configuration

For use as a MUX mode:

- Connect four input SMA cables to Vin0, Vin1, Vin2, and Vin3.
- Remove jumpers J2, J3, and J16 because these cables short the inputs.

This MUX is used as a buffer or with gain. To use as a buffer, connect feedback-shorting jumpers J4, J7, J11, and J15. To use with gain, remove these jumpers and select the appropriate feedback resistor values for R4, R8, R13, and R16. Select the appropriate gain resistor values for R3, R6, R12, and R16.

表 4 lists the jumper configuration for unity-gain MUX mode.

表 **4. Jumper Configuration (MUX-OR Mode)**

JUMPER	CONNECTION
J2	OPEN
J3	OPEN
J4	SHORTED
J7	SHORTED

表 **4. Jumper Configuration (MUX-OR Mode) (continued)**

J11	SHORTED
J15	SHORTED
J16	OPEN

4.2.1.2 PGA Test Configuration

For use as a PGA mode:

- Connect one input SMA cable to Vin0, Vin1, Vin2, or Vin3.
- Connect jumpers J2, J3, and J16 to short the inputs.
- Remove jumpers J4, J7, J11, and J15.
- Select the desired feedback and gain resistors for each amplifier.

表 5 lists the PGA mode jumper configurations.

表 5. Jumper Configuration (PGA Mode)

JUMPER	CONNECTION
J2	Shorted
J3	Shorted
J4	Open
J7	Open
J11	Open
J15	Open
J16	Shorted

4.2.2 Test Results

4.2.2.1 MUX Operation Results

The gain settings for all four channels are set in unity gain as 图 8 shows. Input Vin0 had 1 V applied to the input while Vin1, Vin2, and Vin3 had –1 V applied to the inputs. To see all four channels switching effects, ±1-V, 100-kHz pulses were applied to the S0 and S1 inputs . The S1 input had a 2.5-ns delay. 图 13 shows the output of the OPA837 MUX function as different channels are selected. The high frequency transient spikes are caused by the internal power down circuitry switching and can be eliminated by post-filtering. 1 V is applied to the input of Vin0 and –1 V is applied to the inputs of Vin1, Vin2, and Vin3.

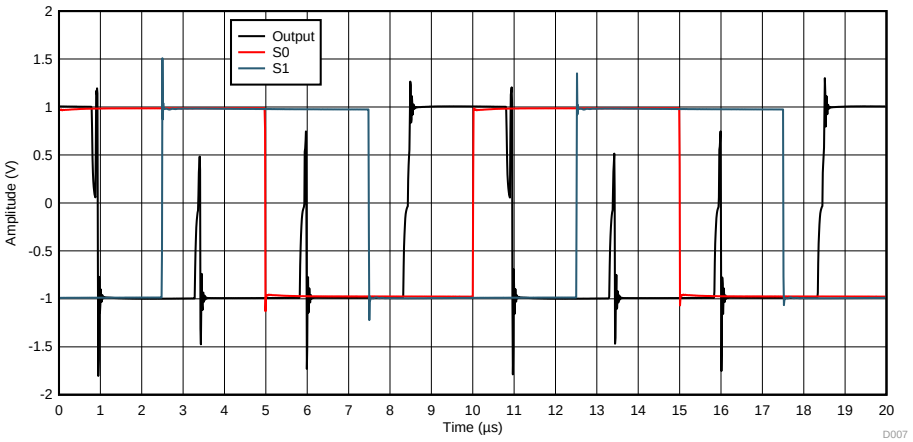


图 13. MUX-OR Operation Results

4.2.2.2 PGA Operation Results

During the PGA operation test, a 1-MHz, 1-4 V_{PP} signal is applied to the input. 图 9 shows the gain settings for this circuit. For this test, the channels are set to the following values:

- Channel 1: Unity Gain
- Channel 2: Gain of 2
- Channel 3: Gain of 4
- Channel 4: Gain of 8

±1-V, 100-kHz pulses were applied to the S0 and S1 inputs to control which output can be viewed. The S1 input has a delay of 2.5 ns. 表 6 lists the truth table for the PGA output in this configuration.

表 6. PGA Test Truth Table

S1	S0	Gain on Output
0	0	× 1
0	1	× 2
1	0	× 4
1	1	× 8

图 14 shows the output of the PGA switching between the different gian settings. Similar to the MUX function, the high frequency transient spikes are caused by the internal power down circuitry switching and can be eliminated with post-filtering.

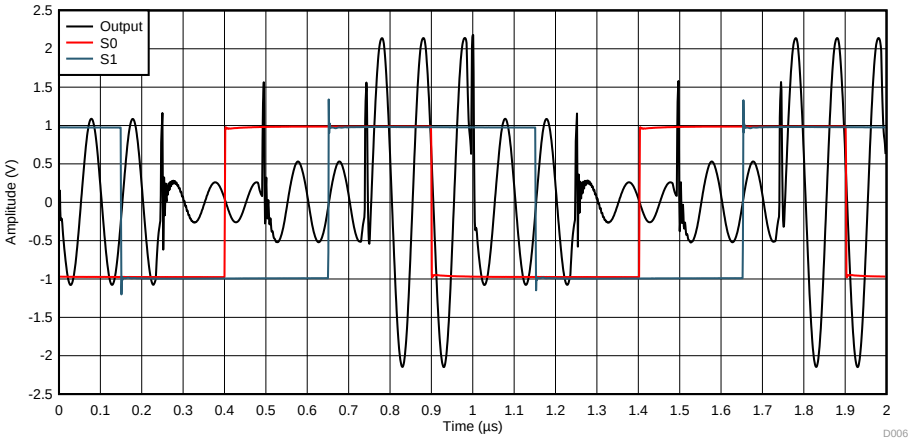


图 14. PGA Operation Results

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-01565 .

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01565 .

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01565.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-01565.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01565.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01565.

6 Software Files

To download the software files, see the design files at TIDA-01565.

7 About the Authors

Robert Clifton is an applications engineer at Texas Instruments. Robert obtained his bachelor's degree from Texas Tech University in electrical engineering.

Sean Cashin is an applications engineer at Texas Instruments. Sean obtained his bachelor's degree from University of Illinois in electrical engineering.

有关 TI 设计信息和资源的重要通知

德州仪器 (TI) 公司提供的技术、应用或其他设计建议、服务或信息，包括但不限于与评估模块有关的参考设计和材料（总称“TI 资源”），旨在帮助设计人员开发整合了 TI 产品的 应用； 如果您（个人，或如果是代表贵公司，则为贵公司）以任何方式下载、访问或使用了任何特定的 TI 资源，即表示贵方同意仅为该等目标，按照本通知的条款进行使用。

TI 所提供的 TI 资源，并未扩大或以其他方式修改 TI 对 TI 产品的公开适用的质保及质保免责声明；也未导致 TI 承担任何额外的义务或责任。TI 有权对其 TI 资源进行纠正、增强、改进和其他修改。

您理解并同意，在设计应用时应自行实施独立的分析、评价和 判断， 且应全权负责并确保 应用的安全性， 以及您的 应用 （包括应用中使用的所有 TI 产品）） 应符合所有适用的法律法规及其他相关要求。你就您的 应用声明，您具备制订和实施下列保障措施所需的一切必要专业知识，能够 (1) 预见故障的危险后果，(2) 监视故障及其后果，以及 (3) 降低可能导致危险的故障几率并采取适当措施。您同意，在使用或分发包含 TI 产品的任何 应用前， 您将彻底测试该等 应用 和该等应用所用 TI 产品的 功能而设计。除特定 TI 资源的公开文档中明确列出的测试外，TI 未进行任何其他测试。

您只有在为开发包含该等 TI 资源所列 TI 产品的 应用时， 才被授权使用、复制和修改任何相关单项 TI 资源。但并未依据禁止反言原则或其他法理授予您任何TI知识产权的任何其他明示或默示的许可，也未授予您 TI 或第三方的任何技术或知识产权的许可，该等产权包括但不限于任何专利权、版权、屏蔽作品权或与使用TI产品或服务的任何整合、机器制作、流程相关的其他知识产权。涉及或参考了第三方产品或服务的信息不构成使用此类产品或服务的许可或与其相关的保证或认可。使用 TI 资源可能需要您向第三方获得对该等第三方专利或其他知识产权的许可。

TI 资源系“按原样”提供。TI 兹免除对 TI 资源及其使用作出所有其他明确或默认的保证或陈述，包括但不限于对准确性或完整性、产权保证、无屡发故障保证，以及适销性、适合特定用途和不侵犯任何第三方知识产权的任何默认保证。

TI 不负责任何申索，包括但不限于因组合产品所致或与之有关的申索，也不为您辩护或赔偿，即使该等产品组合已列于 TI 资源或其他地方。对因 TI 资源或其使用引起或与之有关的任何实际的、直接的、特殊的、附带的、间接的、惩罚性的、偶发的、从属或惩戒性损害赔偿，不管 TI 是否获悉可能会产生上述损害赔偿，TI 概不负责。

您同意向 TI 及其代表全额赔偿因您不遵守本通知条款和条件而引起的任何损害、费用、损失和/或责任。

本通知适用于 TI 资源。另有其他条款适用于某些类型的材料、TI 产品和服务的使用和采购。这些条款包括但不限于适用于 TI 的半导体产品 (http://www.ti.com/sc/docs/stdterms.htm)、评估模块和样品 (http://www.ti.com/sc/docs/sampterms.htm) 的标准条款。

邮寄地址：上海市浦东新区世纪大道 1568 号中建大厦 32 楼，邮政编码：200122