TI Designs：TIDEP-0068
适用于 K2G 通用 EVM (GP EVM) 的 PCI-Express PCB 设计注意事项参考设计

TI Designs

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设计资源

TIDEP0068	TI 设计文件夹
高速布局指南	产品文件夹
66AK2G02	产品文件夹
66AK2G12	产品文件夹
TPS65911	产品文件夹
K2G 通用 EVM	工具文件夹
适用于 K2G 的处理器 SDK	软件文件夹

TI E2E™ Community

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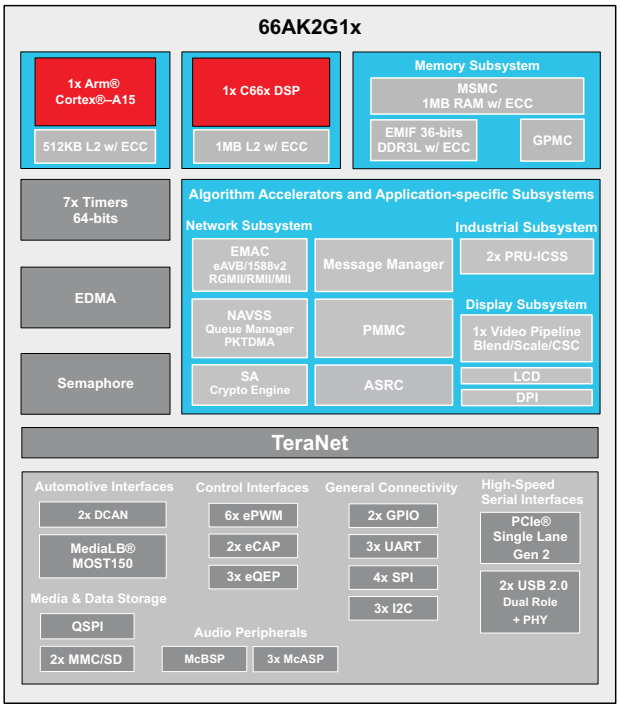
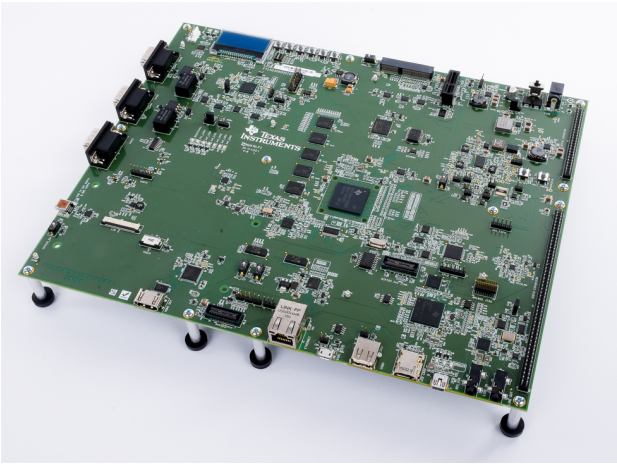
设计 特性

- 优化的高速信号路由
- 表面贴装 1 个 PCIe 插座
- 交流耦合电容器布局示例
- 建议的差分对间隔示例

特色 应用

- 电源保护
- 工业通信和控制
- 变电站自动化
- 电网通信





1 66AK2Gx and Featured Applications

The 66AK2Gx SoC supports the following features (refer to the 66AK2G1x block diagram on page 1):

- **Processor Cores and Memory**
  - Arm Cortex A15 up to 1000 MHz
    - 32 KB L1D, 32 KB L1P, 512 KB L2 cache
  - C66x DSP up to 1000 MHZ
    - 32 KB L1D, 32 KB L1P, 1024 KB L2
  - 1024KB of Shared L2 SRAM in MSMC
  - ECC on all L1, L2, and shared memory
- **Industrial and Control Peripherals**
  - 2 Industrial Communication Subsystems enable cut through, real-time and low latency Industrial Ethernet protocols
  - Programmable real-time I/O enables versatile field bus and control interfaces
  - PCIe for connection to an FPGA or ASIC that provides industrial network connections, backplane communication, or connection to another 66AK2Gx device.
- Security and Crypto
  - Standard secure boot with customer programmable OTP keys
  - Crypto
  - Package
    - 21 × 21 mm, 0.8 mm pitch BGA 625 pins

The 66AK2Gx is suited for applications such as Industrial PLC and Protection Relay as shown in 图 1 and 图 2. In these systems PCIe is used for connection to an FPGA or ASIC that provides industrial network connections, backplane communication or connection to another 66AK2Gx device.

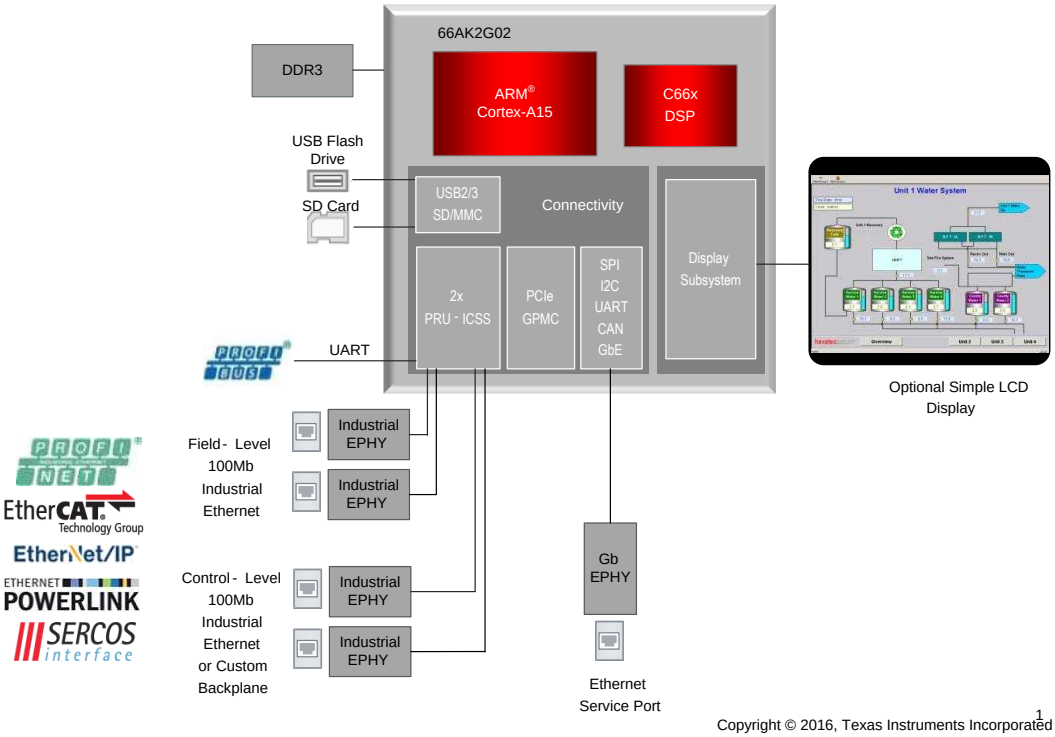


图 1. Industrial PLC System Block Diagram

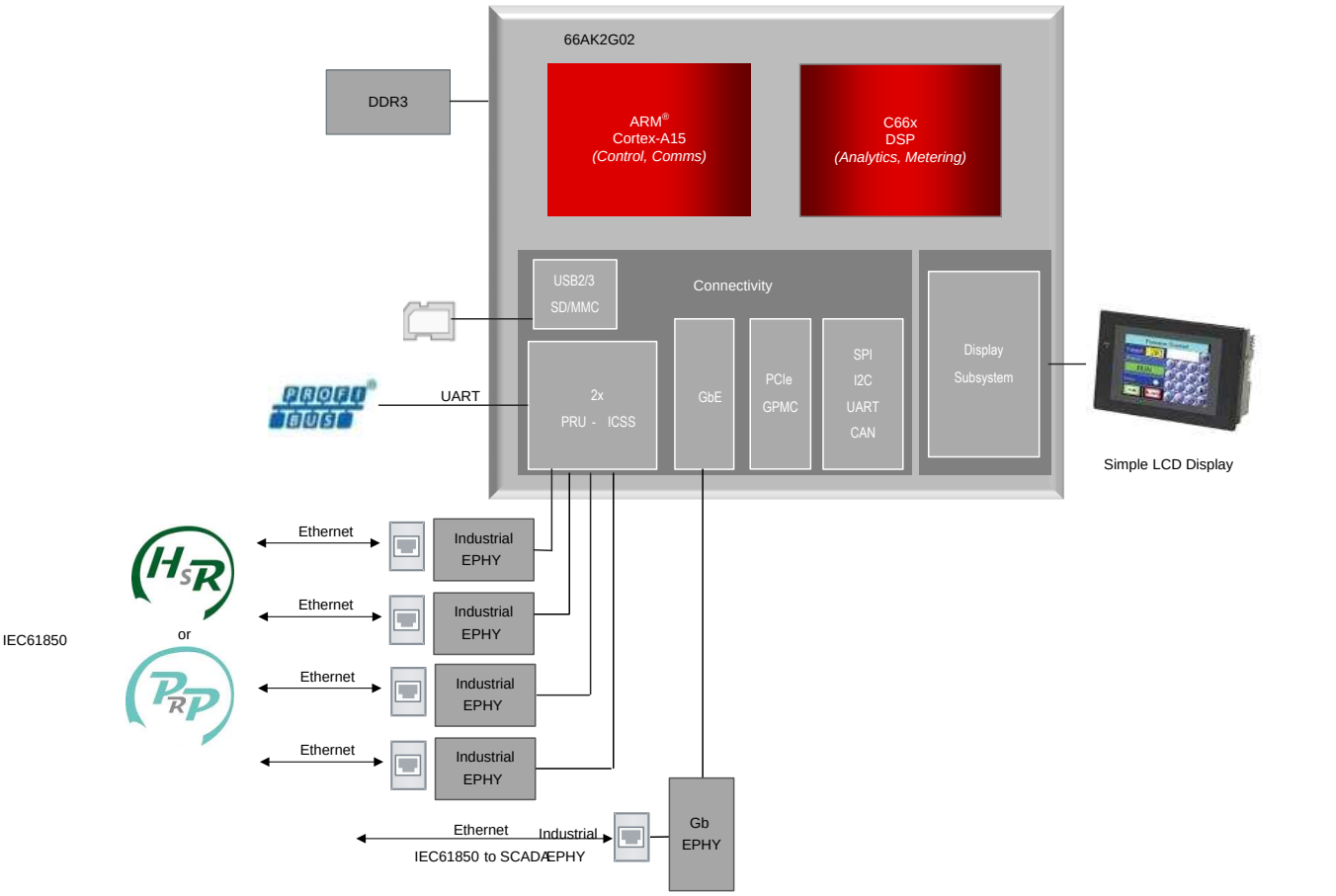


图 2. Protection Relay System Block Diagram

2 Design Overview

The K2G SoC is a high-performance, highly integrated device based on TI KeyStone™ II Multicore DSP + Arm® System-on-Chip (SoC) architecture. The device incorporates a single-lane PCI-Express (PCIe) Gen2 (5GT/s) module that may perform as either a Root Complex (RC) or End Point (EP) device. This design discusses the implementation of the PCI-Express interface on the K2G General Purpose EVM with an eye toward optimizing signal integrity of the interface.

图 3 shows the K2G General Purpose EVM PCIe signal quality.

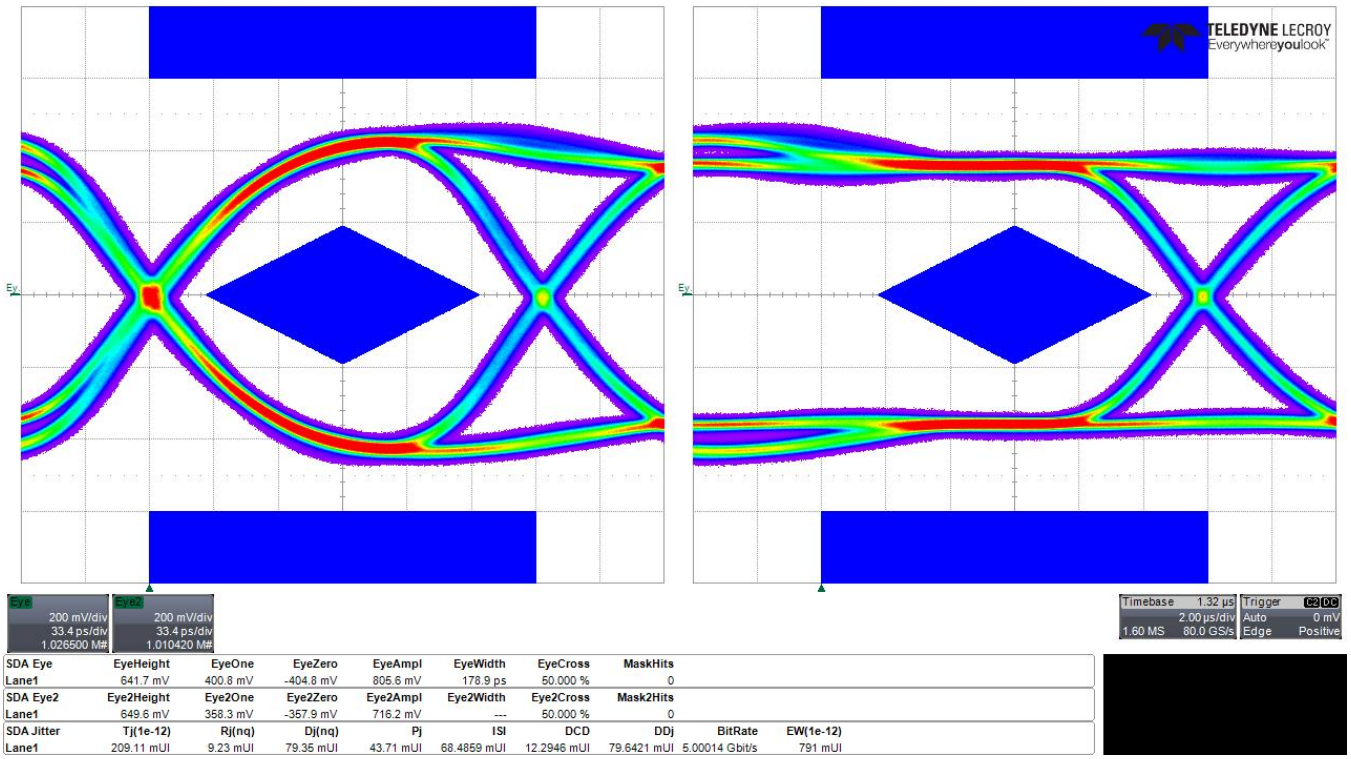


图 3. K2G General Purpose EVM PCIe Signal Quality

3 Key System Specifications

The PCI-Express module present in the 66AK2Gx device supports both Root-Complex and End Point operation on a single-lane bidirectional link interface. PCIe provides for low pin-count, high reliability, and high-speed with data transfer at rates of up to 5.0 Gbps per lane, per direction. PCIe is intended for use as a serial link on backplanes and printed circuit boards. The K2G GP EVM provides a PCIe ×1 add-in card socket to ease evaluation of PCIe EP's prior to implementation in a custom design. The GP EVM does not provide an interface for testing the device as an EP.

4 System Description

The intent of this TI Design is to provide PCB layout considerations for the PCIe portion of the 66AK2Gx System-on-Chip (SoC). The K2G GP EVM is used as a reference to discuss some of these considerations. A more detailed explanation of concepts discussed in this document as well as further information and recommendations on high-speed layout considerations may be found in the *High-Speed Interface Layout Guidelines* (SPRAAR7E).

注: As with all PCB designs, best performance with regard to signal integrity is contingent on performing a board-level simulation and reviewing the results prior to committing the design to PCB. Every PCB design must be evaluated independently as no two are alike.

5 K2G General Purpose EVM – All Layers

图 4 shows the entirety of the GP EVM design.

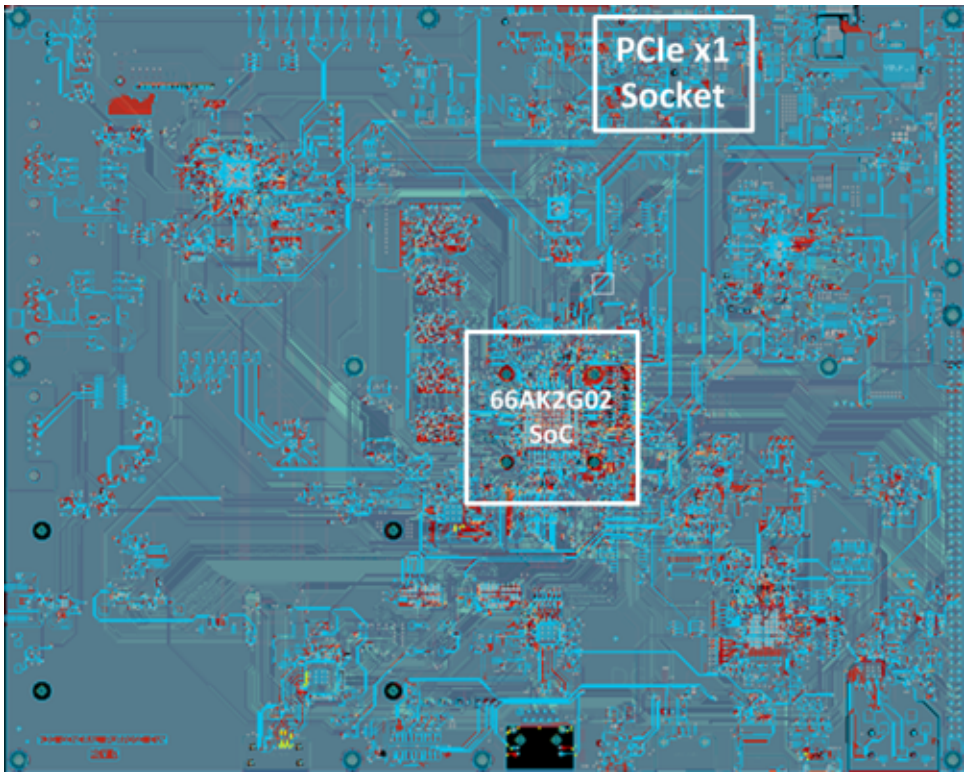


图 **4. K2G GP EVM – All Layers**

5.1 K2G GP EVM – Top Layer – Routing

When designing a PCB that incorporates one or more high-speed interfaces, it is critical that the high-speed signals are routed early in the board design process, preferably first. Routing early ensures that all signals are routed without obstructions or abutments that may force an inclusion of a via, or crossing (unnecessary extension) of the high-speed signals. Care must be given to the physical relationship of the devices that comprise the PCIe bus. 图 5 shows that the PCIe ×1 socket is placed in such a way that the PCIe signals from the SoC PCIe Root Complex to the socket flow naturally; no rotating of the SoC or socket is required. Place the socket in a position that allows it to accept the signals without the need for vias to improve signal quality. For the K2G GP EVM, the PCIe interface has been routed completely on the top layer and terminates at a surface mount connector.

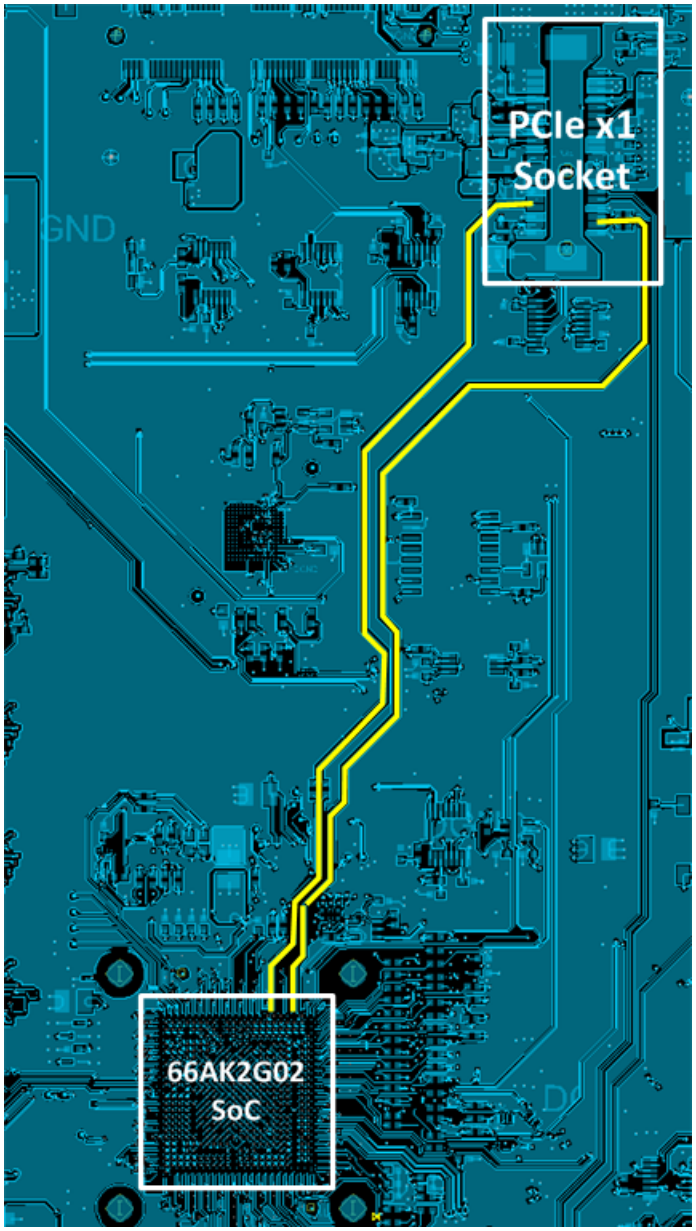


图 **5. K2G GP EVM – Top Layer Only – Zoomed**

5.2 K2G GP EVM – Top Layer – Differential Signal Spacing

To minimize crosstalk in high-speed interface implementations, the spacing between the signal pairs must be a minimum of 5 times the width of the trace. This spacing is referred to as the *5W rule*. A PCB design with a calculated trace width of 6 mils requires a minimum of 30 mils spacing between high-speed differential pairs. Also, maintain a minimum keep-out area of 30 mils to any other signal throughout the length of the trace. Where the high-speed differential pairs abut a clock or a periodic signal, increase this keep-out to a minimum of 50 mils to ensure proper isolation. When possible, the keep-out area should be maximized to further reduce the possibility of crosstalk. In the case of the K2G GP EVM, the PCB was of sufficient size to allow spacing that exceeds 65 mils in many locations. 图 6 shows the K2G GP EVM inter-pair spacing.

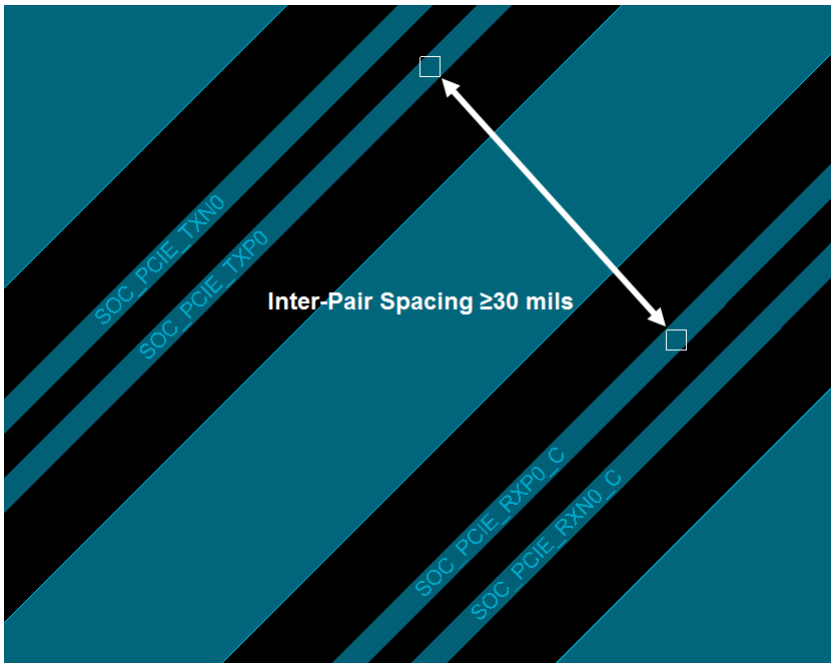


图 6. K2G GP EVM Inter-Pair Spacing

5.3 K2G GP EVM – Top Layer – Reference Plane

High-speed signals should be routed over a solid ground reference plane and should not cross or directly abut a void in the reference plane. TI does not recommend high-speed signal references to power planes. Routing across a plane split or a void in the reference plane forces return high-frequency current to flow around the split or void, which may result in the following conditions:

1. Excess radiated emissions from an unbalanced current flow
2. Delays in signal propagation delays due to increased series inductance
3. Interference with adjacent signals
4. Degraded signal integrity (that is, more jitter and reduced signal amplitude)

In keeping with the above recommendations, the K2G GP EVM routes the PCIe signals over an unbroken, ground reference plane as shown in 图 7.

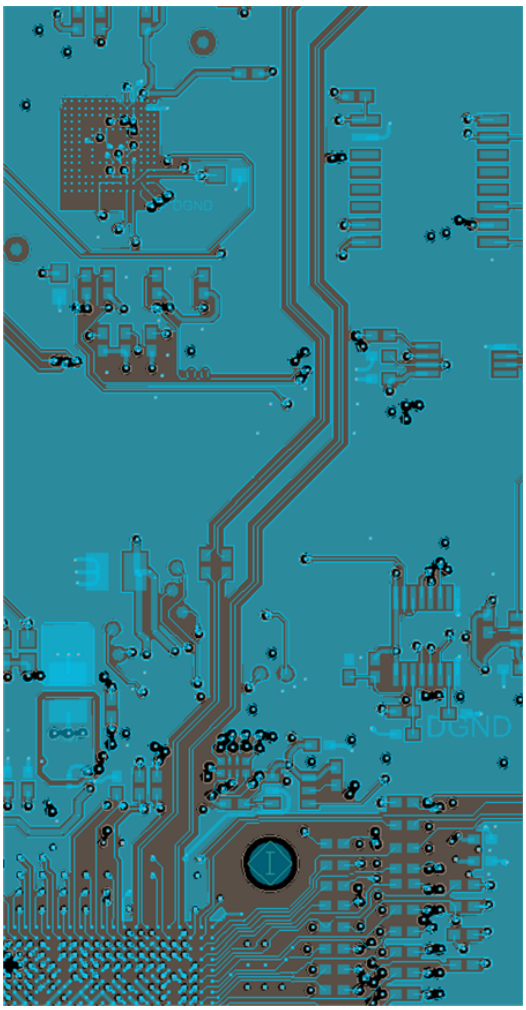


图 7. K2G GP EVM PCIe Reference Plane

5.4 K2G GP EVM – Top Layer – Symmetrical Routing

Because PCIe is a differential interface, all routing of the member pairs must be symmetrical and maintain as much parallelism as possible as they traverse the board together. In the case of the K2G GP EVM, observe in 图 8 that the *PCIE_TXN0* and *PCIE_TXP0* signals maintain symmetry and parallelism across the board up to, and including the PCIe x1 add-in card socket pads.

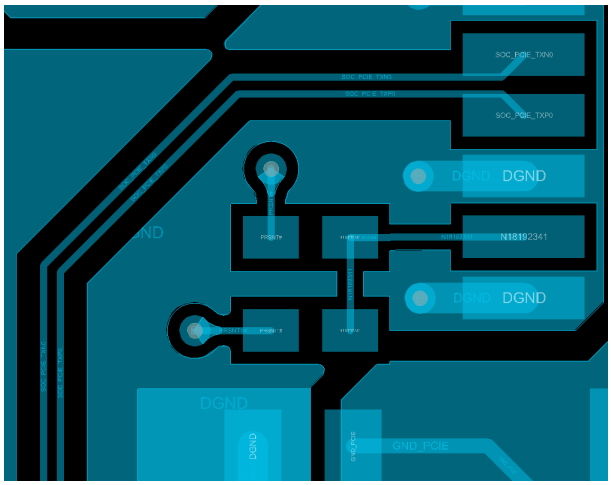


图 **8. Symmetrical Routing and Parallelism of PCIe Signal Pair**

The symmetry and requirements apply to both ends of the interface, however, it may be impossible to fully meet the requirements when routing SoC escape of the PCIe signals. In this particular case, it is permissible to deviate from both symmetry and parallelism for up to 0.25” when escaping the SoC. For K2G GP EVM, SoC escape of the PCIe signals is complete at ±28mils, well within the 0.25” (250 mil) limit.

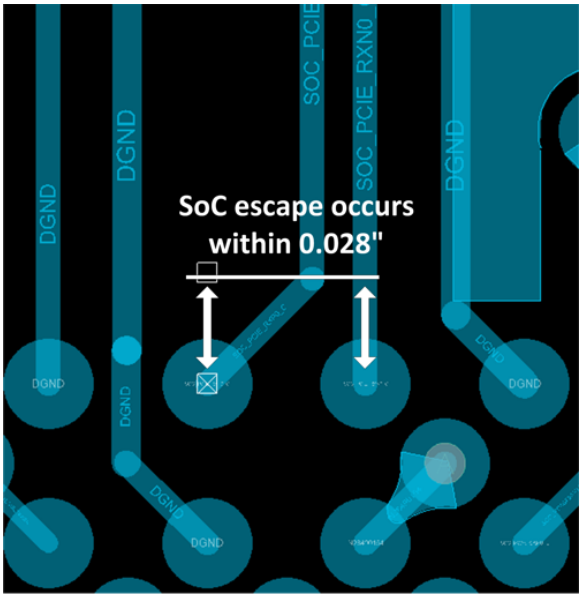


图 **9. SoC Escape**

6 Design Files

The design files for the K2G General Purpose EVM may be found at http://www.ti.com/tool/TIDEP0068.

7 Related Documentation

1. *High-Speed Interface Layout Guidelines*

7.1 商标

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8 About the Author

DAVE KING is a Senior Hardware Applications Engineer in TI's Embedded Processing organization supporting a wide array of Arm-based SoCs such as AM335x (as found on BeagleBone™ and BeagleBone Black), AM35x, AM37x, AM57xx, and AM437x. Dave brings to this role more than fifteen years of protocol, digital, and analog experience in high-speed interfaces ranging from PCI-Express to USB2.0/3.1.

修订历史记录

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Changes from Original (March 2016) to A Revision **Page**

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