TI Designs：*TIDA-01510*

双面布局参考设计可提高直流/直流转换器的功率密度

说明

此参考设计展示了设计双面直流/直流布局的正确方式，以实现更高电源密度。此设计指南重点突出了常见错误以及避免方法，同时提供的测试结果表明，在双面布局中正确使用 TPS54824 器件不会对性能产生影响。如果 TPS54824 降压转换器的 8A 电流输出过大，此设计也可以换为兼容引脚对引脚的 4A TPS54424 器件。

此解决方案非常适合用于为噪声敏感型数据转换器系统供电，例如通信设备、医疗、测试和测量以及航空电子设备等 应用 ，这些应用均需要节省布板空间。

资源

TIDA-01510	设计文件夹
TPS54824	产品文件夹
TPS54424	产品文件夹
WEBENCH®	产品文件夹

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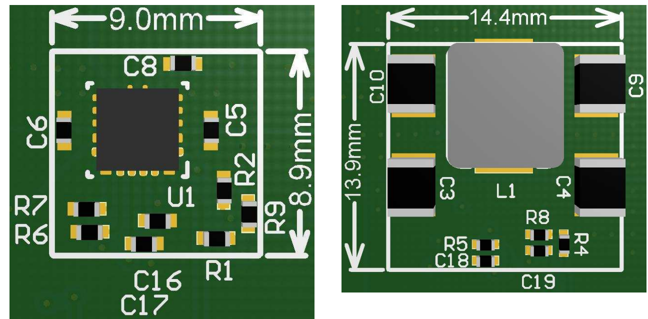
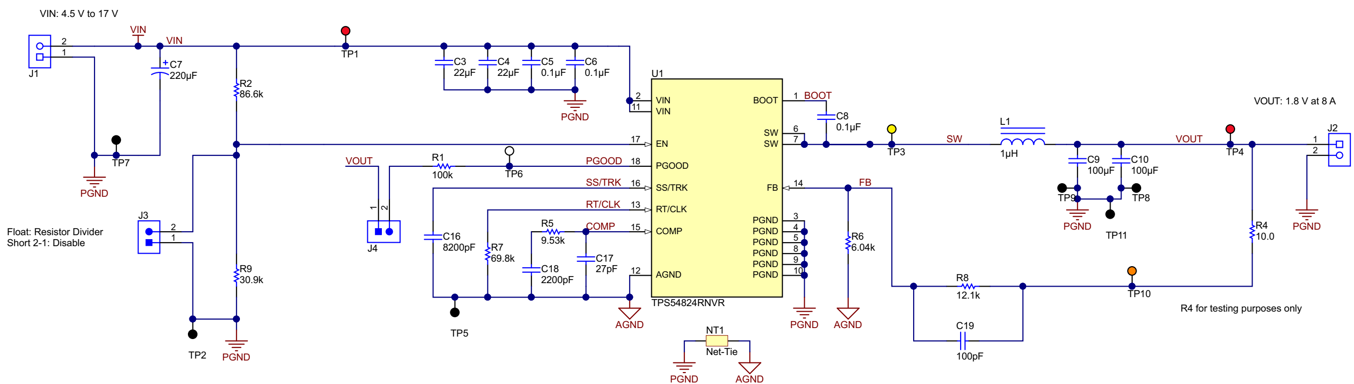
特性

- 输入范围：4.5V 至 17V，输出：1.8V_{OUT}/8A I_{OUT}
- 峰值效率：在输入电压为 5V、输出电流为 2A 时为 94.7%
- 负载调节率：< ±0.04%
- 开关频率：700kHz
- 解决方案总尺寸：280 mm^2

应用

- 医用超声波扫描仪
- 半导体测试设备
- 小型蜂窝基站
- 大规模 MIMO（有源天线系统）
- 宏远程无线电单元 (RRU)





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1 System Description

A small footprint, fixed frequency, high efficiency, and low cost are all key factors needed in power solutions for telecom, datacom, and industrial systems. This reference design focuses on creating a small form-factor while maintaining peak performance. More and more systems are being densely packed onto printed-circuit boards (PCB). A recent necessity is to have components on both sides of the PCB. Some examples of end-equipments benefitting from this are 4G and 5G remote radio units in wireless infrastructure and bench-top test equipment such as oscilloscopes or portable ultrasound equipment. However, many engineers are skeptical of separating a power design to both sides of the board due to the probable performance degradation.

This reference design guide covers the steps to properly design a two-sided layout and includes measurement results of the TPS54824 device implemented in a two-sided and one-sided layout to illustrate the small performance differences between the two options.

1.1 Key System Specifications

表 1 lists the key system specifications.

表 **1. Key System Specifications**

PARAMETER	VALUE
Output ripple	< 20 mV
Efficiency (at 12 V_{IN} / 8 A_{LOAD})	88%
Load transient	< 5% V_{OUT}
Load regulation	±0.04%
Temperature (max load)	64.7°C
Switch node overshoot	3.59 V

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2 System Overview

2.1 Block Diagram

图 1 illustrates the TIDA-01510 block diagram.

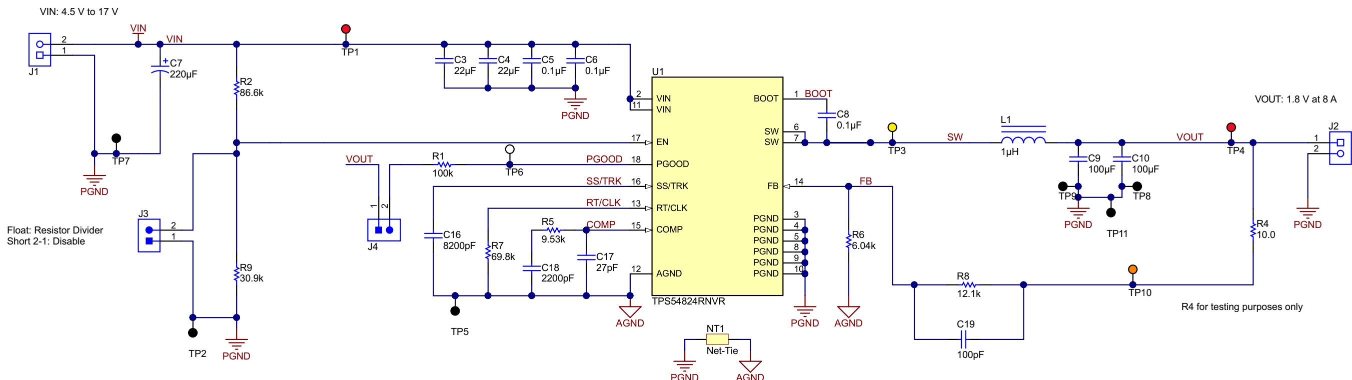

图 1. TIDA-01510 Block Diagram

2.2 Highlighted Products

2.2.1 TPS54824

The TPS54824 device is a full featured 17-V, 8-A synchronous, step-down converter in a 3.5-mm × 3.5-mm HotRod™ QFN package. The device is optimized for a small solution size through high efficiency and integrating the high-side and low-side MOSFETs. Further space savings are achieved through peak current mode control, which reduces component count, and by selecting a high switching frequency, reducing the inductor footprint.

2.3 System Design Theory

Often the recommended layout places most, if not all, components on one side of the PCB. Some applications that are space constrained or require the highest power density have to place components on the top and bottom side of the PCB. This section provides recommendations on how to do a two-sided layout.

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2.3.1 Component Placement

When designing a two-sided layout, first consider the placement of the input capacitors, inductor, and output capacitors.

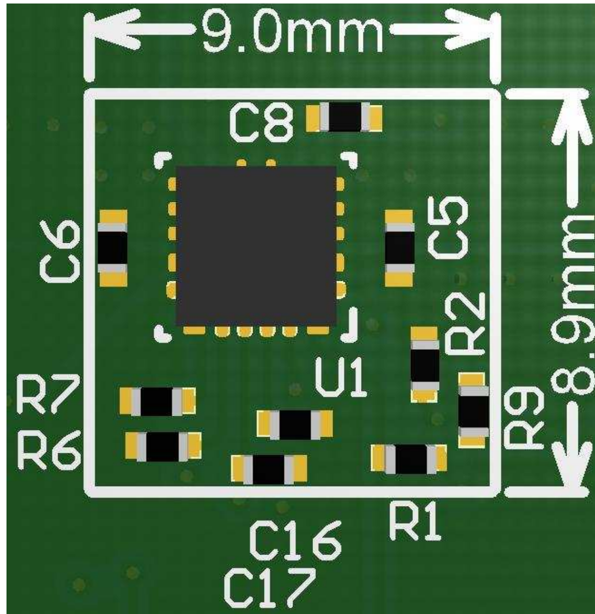

图 2. Bottom-Side Solution Dimensions

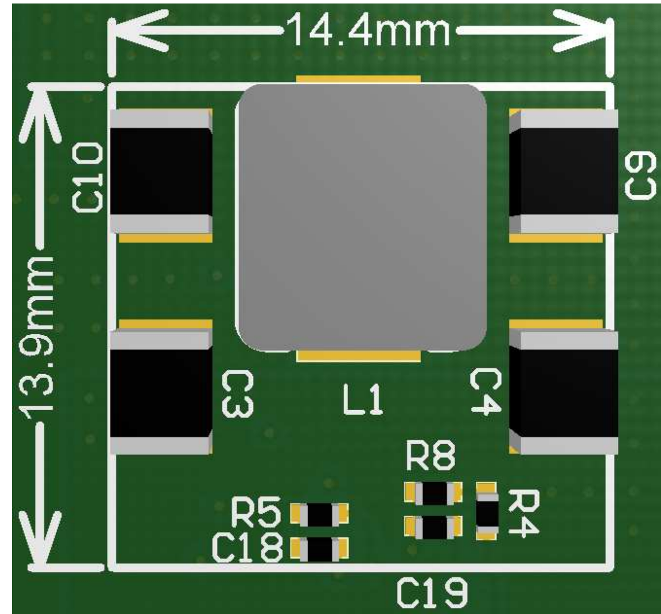

图 3. Top-Side Solution Dimensions

The larger-sized input capacitors with a 1210 package and with a larger value (C3 and C4) are placed on the top side. The IC is placed on the bottom side, and it is important to still include some bypass capacitance as close as possible to the IC. Therefore, the high-frequency bypass capacitors (C5 and C6) are placed as close as possible to the two VIN pins of the TPS54824. Use as many vias as possible between the IC and the input capacitors to reduce parasitic inductance.

The inductor is placed on the top side, opposite of the TPS54824. Placing the inductor on the opposite side is acceptable because any parasitic inductance between it and the IC is very small compared to the inductance of the inductor. For best performance, it is important to maximize the number of vias between the IC and the inductor to reduce parasitic inductance and resistance.

The output capacitors are also placed on the top-side because they are in a larger-sized 1210 package. They are placed with their connection to ground as close as possible to the ground of the input capacitors. The larger-sized components are purposely placed on the top side because it is typically the side allowing components with greater height.

Next, complete the placement of the components connected to the analog control circuits. It is important to try to place the components connected to the RT/CLK, FB, COMP, and SS/TRK pins on the same side as the IC with a short return path to AGND. There are two exceptions. R5 and C18 connected to the COMP pin are on the top side; this connection is acceptable because C17 provides bypass for the COMP pin. R8 and C19 connected to the FB pin are on the top side and this is acceptable because the size of the FB node is still kept very small. The trace from the FB divider is kept away from signals that generate noise and is connected to the output at the point of regulation. Lastly, AGND is connected to PGND outside of the critical switching loop to minimize switching noise in the control loop.

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3 Hardware, Testing Requirements, and Test Results

3.1 *Required Hardware*

图 4 and 图 5 illustrate the top and bottom of the TIDA-01510, respectively.

图 4. TIDA-01510 Board Top

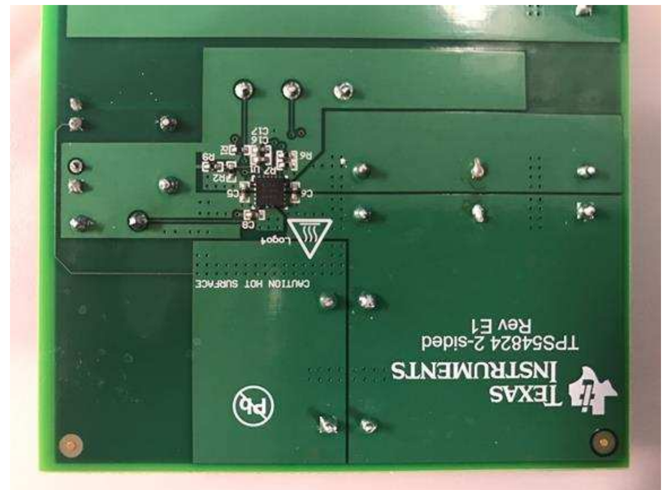

图 5. TIDA-01510 Board Bottom

3.2 *Testing and Results*

For the following tests, a TPS54824 EVM is modified to have the same LC filter with the exact components from the reference design board. This modification highlights that when done right, a two-sided layout does not have any performance degradation compared to a one-sided layout.

3.2.1 Efficiency and Power Loss

Efficiency data is taken from the design board and from the modified TPS54824 EVM to compare. 图 6 and 图 7 show the efficiency data for the reference design and EVM, respectively, at three different input voltages.

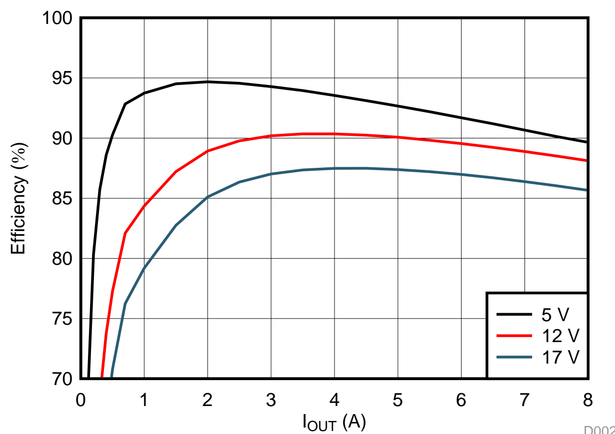

图 6. TIDA-01510 Efficiency

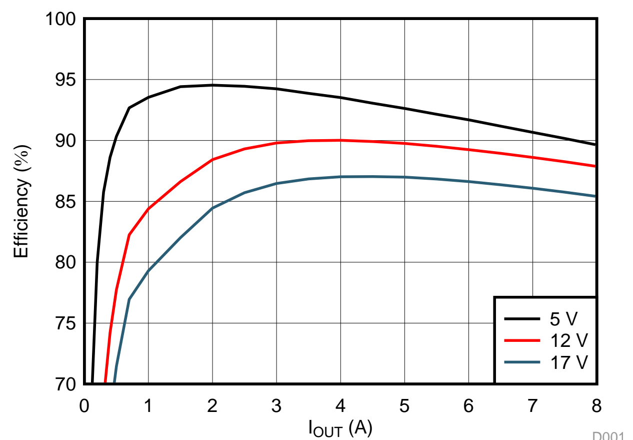

图 7. EVM Efficiency

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Power loss is also graphed for both boards to represent the amount of power being lost at different loads. The data is gathered at the same three input voltages as the efficiency testing. 图 8 shows the power loss for the reference design from a 0-A to 8-A load. 图 9 shows the power loss of the EVM with the same parameters.

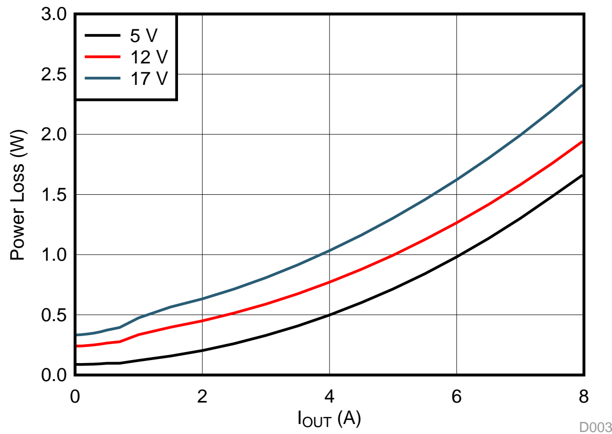

图 8. TIDA-01510 Power Loss

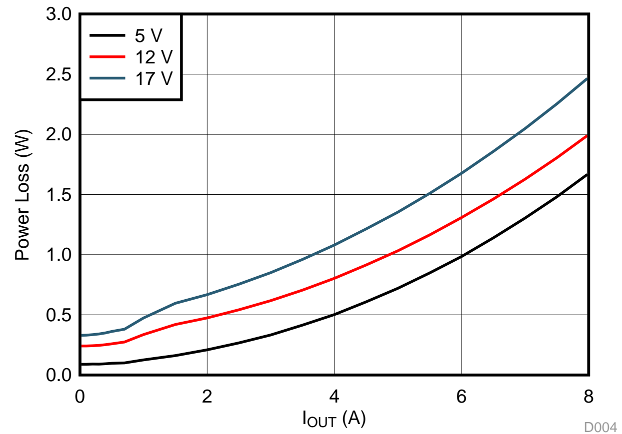

图 9. EVM Power Loss

From these graphs, the efficiency and power loss is not affected when using a well-designed, two-sided layout versus a one-sided layout.

3.2.2 Switch Node

Because the switch node is now going through the board for the TIDA-01510 board, the switching waveform is observed to compare performance with the TPS54824 EVM to verify if there is any negative impact from the vias. The waveforms are captured at 12-V input, 1.8-V output, and with a 4-A load. The oscilloscope is set to 5 V/div at 500 MHz for the vertical scale and 100 ns/div at 1 Gsps for the horizontal scale. 图 10 and 图 11 show the switching waveforms of the TIDA-01510 board and EVM, respectively.

图 10. TIDA-01510 Switch Node Waveform

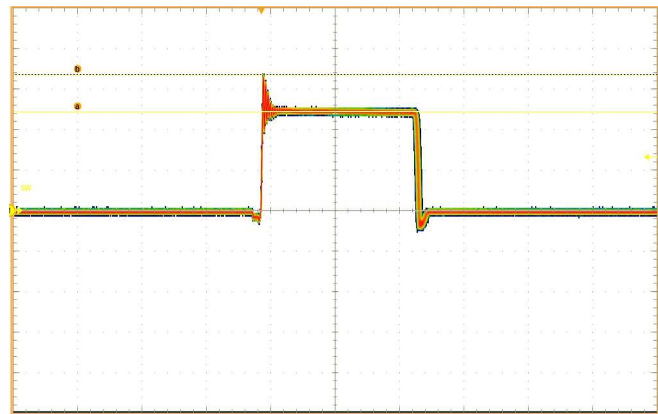

图 11. EVM Switch Node Waveform

Both boards have ringing on the switch node with a peak voltage of roughly 16.5 V. Both switch nodes are nearly identical with less than 0.5 V difference in their peak amplitudes. This value concludes that the added inductance of the vias on the two-sided layout have a negligible impact on the ringing versus the one-sided layout. This inductance results in no issues with additional EMI or stress on the MOSFET.

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3.2.3 Load Transient

This section gathers data accumulated from a load transient test to verify that the response to load transients is not affected when using the two-sided layout. The parameters of this test are as follows:

- 12-V input
- 1.8-V output
- 4-A load step from 0 A to 4 A with a slew rate of 10 A/µs

图 12 and 图 13 show the load transient results of this reference design and the EVM, respectively.

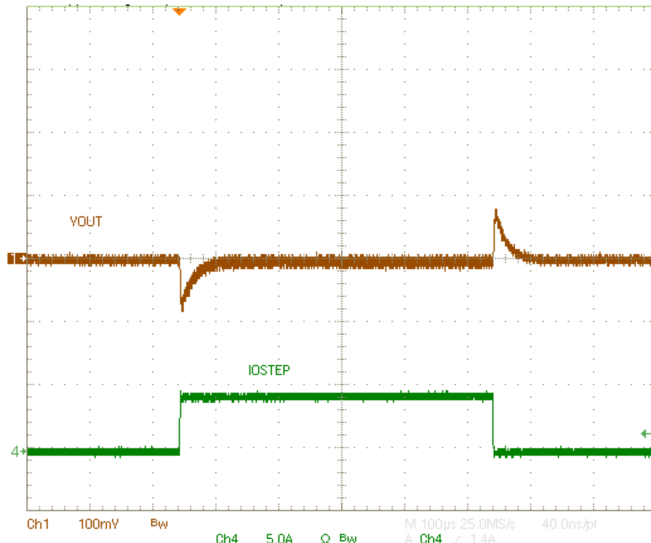

图 12. TIDA-01510 Transient Waveform

图 13. EVM Transient Waveform

Both the reference design and the EVM have an output deviation of less than 5% during the load step, and the transient response waveforms are identical. Therefore, the transient response is not affected going from a one-sided layout to a properly designed two-sided layout.

3.2.4 Thermal Performance

Thermal data is gathered for both the reference design and the TPS54824 EVM to see the difference in performance. This test is run at room temperature and no air flow with a 10-minute thermal soak period. The input is set to 12 V and the output is set to 1.8 V with an 8-A load. 图 14 and 图 15 show the temperatures of the IC and the inductor, respectively.

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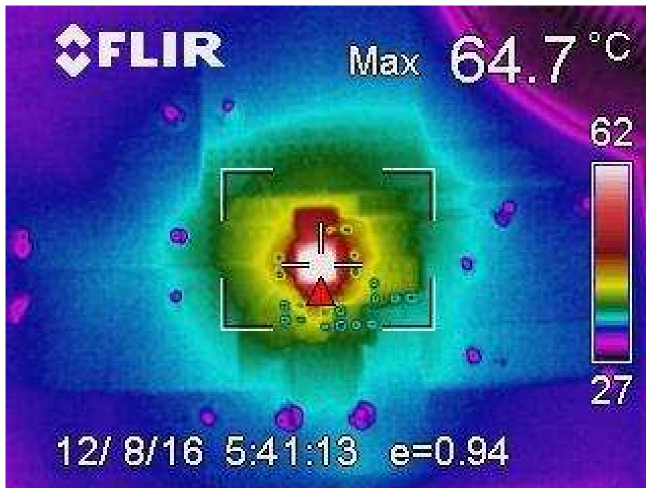

图 14. TIDA-01510 IC Thermal Readout

图 15. EVM IC Thermal Readout

These images show that the reference design suffers in thermal performance compared to the EVM. However, with roughly a 6° difference, the trade-off for having a smaller solution size is reasonable. The designer must decide because this choice limits the use of the device at higher ambient temperatures.

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4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01510.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01510.

4.3 PCB Layout Recommendations

Take special care when creating a layout for a two-sided DC/DC design. This section provides insight for a few issues that could potentially be encountered with the layout.

When putting components on both sides of the board, the via count will be high. Do not let these vias affect the integrity of the ground plane. 图 16 shows the ground plane under the TPS54824 device.

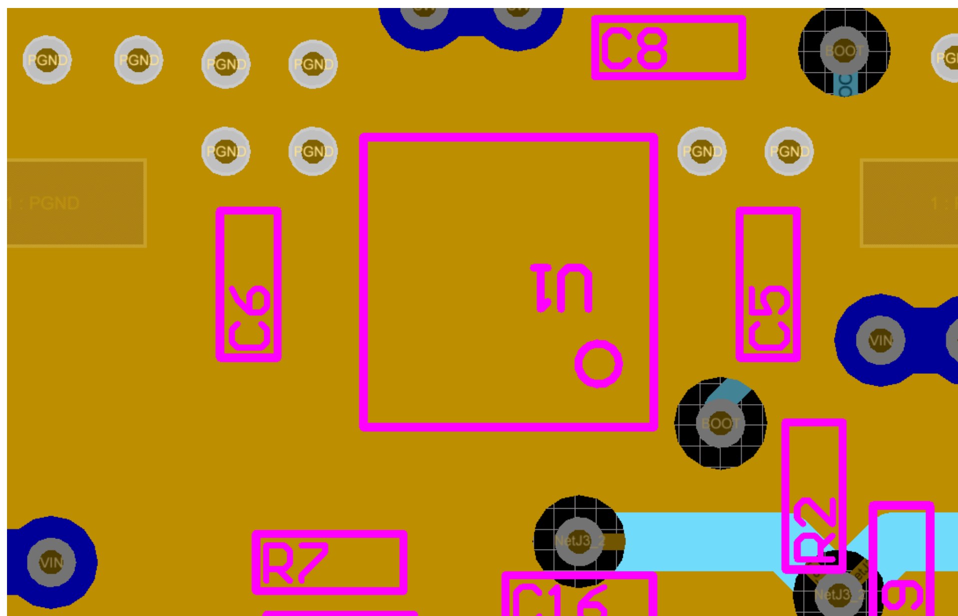

图 16. Ground Plane Layout

Notice how the ground plane is completely solid with no cutouts between the PGND pins, which are located on each side of the device near C5 and C6. This is necessary to reduce the impedance between the PGND pins. These vias can also affect the input of the device. 图 17 shows a VIN plane that connects to the input capacitors and uses vias to connect to both input pins of the device.

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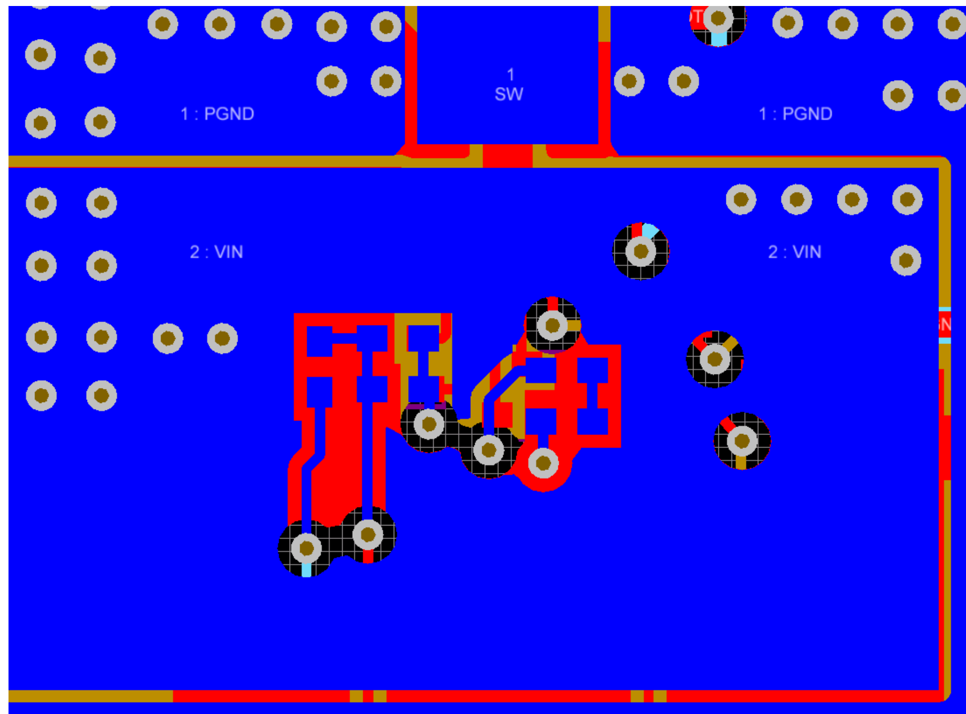

图 17. VIN Plane Layout

Keep the connection between the two VIN pins as solid as possible. With all the vias and passive components, the VIN plane can be easily cut up. Even so, this design still has enough copper left to provide a wide, short, and direct current path between the two VIN pins without adding any unwanted resistance.

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01510.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01510.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01510.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01510.

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修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Original (May 2018) to A Revision **Page**

• 已添加 在说明部分添加了第二段。 1
• 已更改 *应用* 列表 1

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