TI Designs：TIDM-01000
具有 MSP430 智能模拟组合的 4mA 至 20mA 回路供电式 RTD 温度变送器参考设计

说明

此 TI 参考设计为 4mA 至 20mA 回路供电式电阻温度检测器 (RTD) 温度变送器提供了一个组件数量少的低成本解决方案。此设备利用 MSP430FR2355 MCU 的片上智能模拟组合 (SAC) 模块控制回路电流，因此无需独立 DAC。此设计实现了 12 位输出解析度。输出电流解析度为 6µA。本设计还集成了反极性保护以及对环路电源输入的 IEC61000-4-2 和 IEC61000-4-4 保护。

TI 参考设计为您提供了所需的基础元素，包括方法、测试和设计文件，以便设计人员快速评估和定制系统。TI 参考设计还可以帮助您缩短产品上市时间。

资源

TIDM-01000	设计文件夹
MSP430FR2355	产品文件夹
ADS1120	产品文件夹
TPS7A16	产品文件夹

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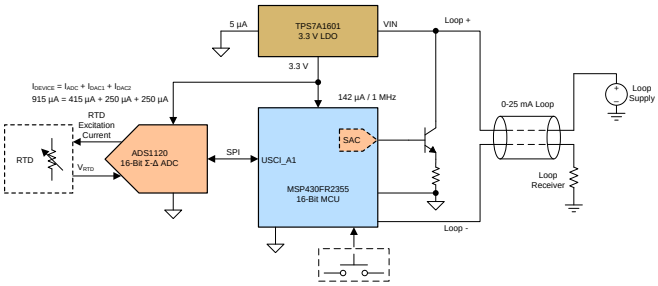
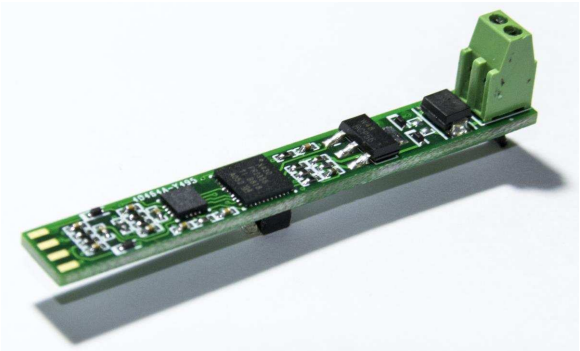
特性

- 传感器输入与 2 线、3 线或 4 线 RTD 探头兼容
- RTD 温度范围：–200°C 至 +850°C
- 最大测量误差为：<1°C
- IEC61000-4-2：ESD：空气放电：±8kV A 类
- 小封装尺寸（长 × 宽）：60mm × 8mm
- 工作温度范围：-40°C 至 +105°C

应用

- 工厂自动化和过程控制
- 传感器和现场发送器
- 楼宇自动化
- 测试和测量





该 TI 参考设计末尾的重要声明表述了授权使用、知识产权问题和其他重要的免责声明和信息。

1 System Description

A 4- to 20-mA current loop is standard for transmitting remote-sensor information to programmable logic controllers (PLCs) over long distances in industrial process-monitoring, control, and automation applications. 图 1 shows a typical RTD temperature-measurement transmitter for a 2-wire, 4- to 20-mA, current-loop system, which consists of four major blocks.

- Analog-to-digital converter (ADC): For RTD-sensor measurement, this is typically a low-power, low-noise, delta-sigma ADC with an internal PGA and programmable current source.
- Digital-to-analog converter (DAC): Output for the current-loop control, this is typically a low-power DAC with an integrated operational amplifier.
- Microcontroller (MCU): Controls the whole system operation including data processing and calibration algorithm.
- Low dropout regulator (LDO): Transmitter power supply.

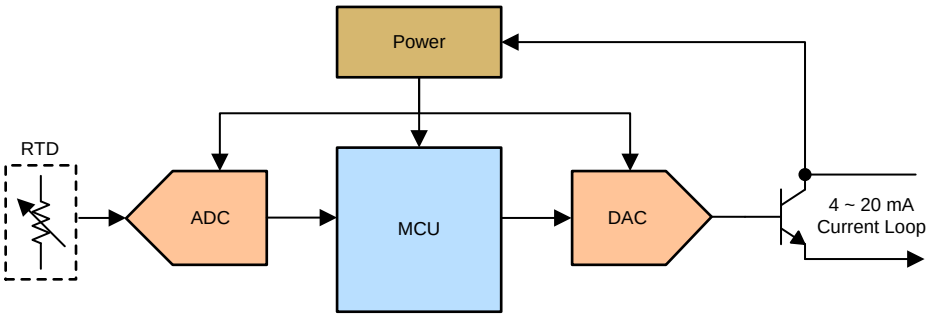


图 **1. Typical Block Diagram of RTD Temperature Transmitter**

The MSP430FR2355 device is an ultra-low-power, mixed-signal MCU from TI, with on-chip smart analog combo (SAC) modules that makes it possible to move the DAC block into an MCU. Leveraging the integrated peripherals of the MSP430FR2355 device enables a low-component count and low cost solution for the user. The MSP430FR2355 device also helps to reduce the PCB size and facilitates the layout. 图 2 shows the improved system block diagram based on the MSP430FR2355 MCU.

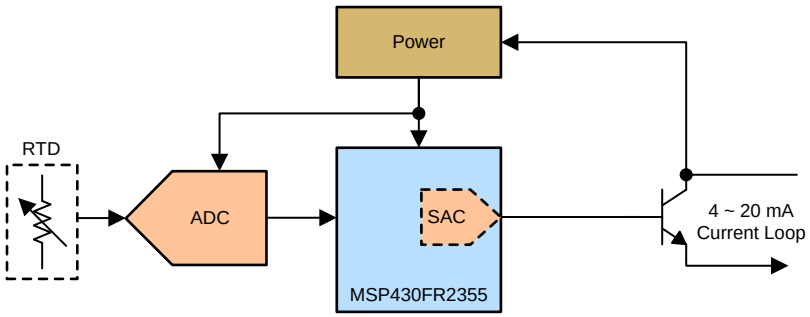


图 **2. Block Diagram of RTD Temperature Transmitter Based on MSP430FR2355**

This reference design provides a low-power consumption, low-cost, RTD temperature transmitter solution achieving a 12-bit output resolution with the integrated smart analog combo (SAC) module. The output-current resolution is 6 µA. The design also incorporates reverse-polarity protection capability as well as IEC61000-4-2 and IEC61000-4-4 protection on the loop power input.

All the relevant design files such as the schematics, bill of materials (BOM), layer plots, Altium Designer files, Gerber files, and MSP430 MCU software are provided.

1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATION
Sensor type	2-, 3-, and 4-wire RTD probes Firmware supports PT100 RTD by default.
Output signal	4 mA to 20 mA
Temperature range for RTD	–200°C to +850°C
Power-supply voltage range on loop-interface terminals	10-V to 36-V DC
Supply current consumption	< 1.6 mA (to power all the functional blocks of the transmitter)
Reverse polarity on input power	Supported
Output current resolution	6 µA
Power supply influence	Deviation of 0.24 µA from 10 V to 36 V
System accuracy or maximum measured error	Better than 1°C (–200°C to +850°C temperature range)
Calibration	Offset and gain calibration for ADC and SAC
IEC61000-4-2 ESD	Air discharge: ±8 kV (Class A)
RTD temperature linearization	–200°C to +850°C look-up table, with 1°C resolution implemented in the MSP430 firmware, to resolve nonlinearity of RTD or the Callendar-Van Dusen relationship between resistance and temperature
Interface connector	Two-pin TH connector for loop interface Four-pin SMD connector for external RTD sensor probe Four-pin SMD connector for Spy-bi-wire debug interface
Operation temperature	–40°C to +105°C
Form factor (L × W)	60 mm × 8 mm

2 System Overview

2.1 Block Diagram

图 3 shows a detailed block diagram of the 2-wire, 4- to 20-mA current-loop, RTD temperature transmitter. This reference design consists of three blocks. The selected three integrated circuits complete the transmitter signal chain. The ADC from TI (ADS1220) interfaces with a 2-wire, 3-wire, or 4-wire RTD probe. The MSP430FR2355 MCU runs the application firmware, including the algorithms for system calibration and data process. The output is controlled by an on-chip SAC module in the MSP430FR2355 device and delivers a 4- to 20-mA output current proportional to the RTD temperature reading. The LDO (TPS7A16) supplies the system with loop power. The TPS7A16 device has an input-voltage range of 3 V to 60 V, ultra-low quiescent current (5 µA), and high thermal-performance packaging.

To conform to the 4- to 20-mA communication standards, the complete transmitter must consume less than 3.3 mA of current.

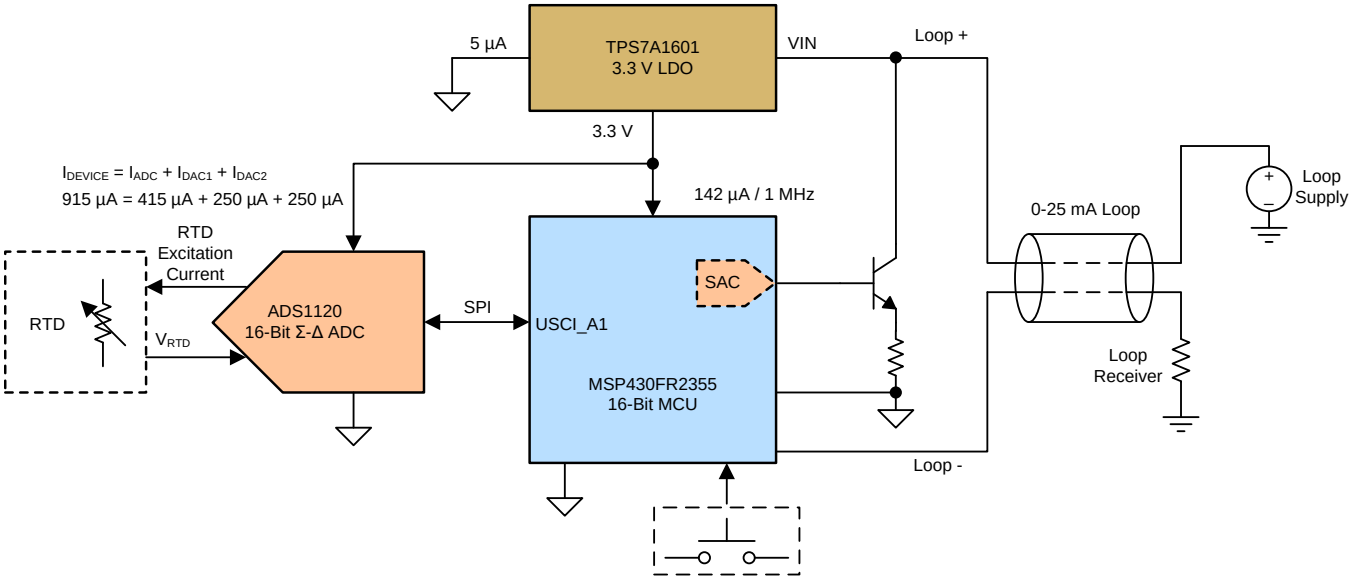


图 3. TIDM-01000 Block Diagram

2.2 Highlighted Products

This RTD temperature-transmitter reference design features the following devices:

- MSP430FR2355 – Ferroelectric RAM (FRAM)-based, mixed-signal, MSP430™ MCU
- ADS1120 – Low-power, low-noise, 16-bit, ADC
- TPS7A1633 – 3-V to 60-V input, ultra-low quiescent current, 100-mA, low-dropout (LDO) linear regulator

For more information on each of these devices, see their respective product folders at www.ti.com.

2.2.1 MSP430FR2355

The MSP430FR2355 FRAM MCU features a powerful 16-bit, RISC CPU, 16-bit registers, and a constant generator that contribute to maximum code efficiency. The digitally-controlled oscillator (DCO) lets the device wake up from low-power mode and go to active mode in typically less than 10 µs. The feature set of this microcontroller is designed for applications such as smoke detectors, industry transmitters, and portable health and fitness accessories.

In this design, an on-chip eUSCI module interfaces with the ADC1120. On-chip, 32KB-FRAM memory stores the application software, RTD loop table, and calibration data. The 16-bit, RISC architecture enables functions like arithmetic algorithms, gain and offset calibration routines, sensor linearization using look-up tables, and scaling ADC output to DAC input code. Two on-chip SAC modules control the current loop output. From a layout and routing perspective, the QFN40 package is a good choice when size does not exceed 6 mm, to fit an 8-mm wide PCB.

图 4 shows the MSP430FR2355 block diagram.

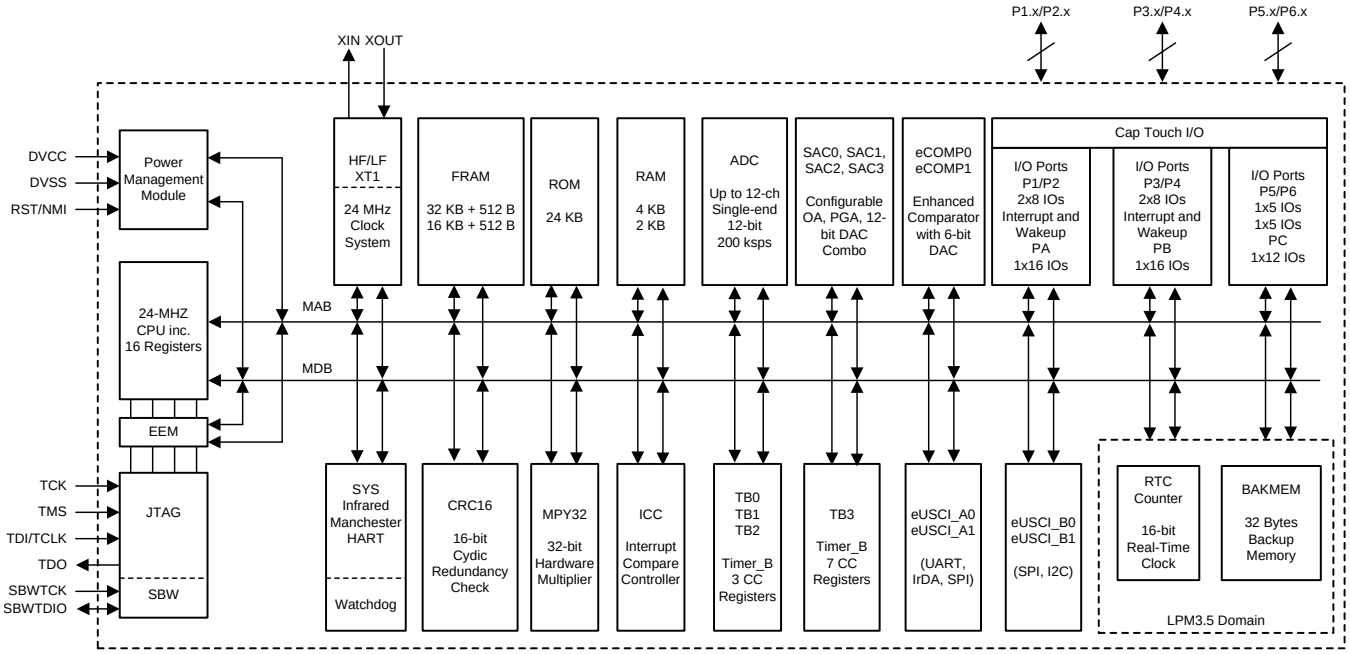


图 4. MSP430FR2355 Block Diagram

MSP430FR2355 features

- Embedded MCU:
  - 16-bit, RISC architecture up to 24 MHz
  - Wide supply-voltage range from 1.8 V to 3.6 V
  - Active mode: 142 µA/MHz
- Low-power, FRAM:
  - Up to 32KB of nonvolatile memory
  - Built-in error-correction code (ECC)
  - Configurable write protection
  - 10^{15} write-cycle endurance

  - Radiation resistant and nonmagnetic
- Intelligent digital peripherals:
  - Three 16-bit timers, with three capture and compare registers each (Timer_B3)
  - 16-bit timer, with seven capture and compare registers each (Timer_B7)
  - 16-bit, counter-only, real-time clock counter (RTC)
  - 16-bit cyclic-redundancy checker (CRC)
  - Interrupt compare controller (ICC), enables nested hardware interrupt
  - 32-bit hardware multiplier (MPY32)
- Enhanced serial communications:
  - Two enhanced USCI_A modules (eUSCI_A) support UART, IrDA, and SPI
  - Two enhanced USCI_B modules (eUSCI_B) support SPI and I^2C
- High-performance analog:
  - 12-channel, 12-bit ADC
  - Two enhanced comparators (eCOMP)
  - Four Smart Analog Combo Modules (SAC-L3)
    - Supports general-purpose operational
    - Operational amplifier (OA)
    - Rail-to-rail input and output
    - Multiple input selections
    - Configurable high-power and low-power modes
    - Configurable programmable gain amplifier (PGA) mode supports
    - Built-in, 12-bit reference DAC for offset and bias settings
    - 12-bit voltage DAC mode with optional references
- Clock system (CS):
  - On-chip, 32-kHz RC oscillator (REFO)
  - On-chip, 24-MHz DCO, with frequency locked loop (FLL)
  - On-chip, low-frequency, 10-kHz oscillator (VLO)
  - On-chip, high-frequency, modulation oscillator (MODOSC)
  - External, 32-kHz, crystal oscillator (LFXT)
  - External, high-frequency, crystal oscillator up to 24 MHz (HFXT)
  - Programmable MCLK prescaler of 1 to 128
  - SMCLK derived from MCLK, with programmable prescaler of 1, 2, 4, or 8
- General input/output and pin functionality:
  - 44 I/Os on 48-pin package
  - 32 interrupt pins (P1, P2, P3, and P4) can wake MCU from low-power modes
  - All I/Os are capacitive touch
- Package options:
  - 48-pin: LQFP (PT)

- 40-pin: VQFN (RHA)
- 38-pin: TSSOP (DBT)

For complete module descriptions, see the MSP430FR4xx and MSP430FR2xx Family User's Guide.

2.2.2 ADS1120

The ADS1120 is a precision, 16-bit ADC that offers many integrated features, to reduce system cost and component count in applications measuring small-sensor signals. The device features two differential or four single-ended inputs through a flexible input multiplexer (MUX), a low-noise PGA, two programmable excitation-current sources, a voltage reference, an oscillator, a low-side switch, and a precision-temperature sensor.

The device performs conversions at data rates up to 2000 samples-per-second (SPS), with single-cycle settling. At 20 SPS, the digital filter offers simultaneous 50-Hz and 60-Hz rejection for noisy industrial applications. The internal PGA offers gains up to 128 V/V. The PGA makes the ADS1120 designed for applications measuring small-sensor signals, such as RTDs, thermocouples, thermistors, and resistive bridge sensors. The device supports measurements of pseudo- or fully-differential signals when using the PGA. Alternatively, the device is configured to bypass the internal PGA while still providing high-input impedance and gains up to 4 V/V, which allows for single-ended measurements.

The power consumption is as low as 120 µA when operating in duty-cycle mode, with the PGA disabled. A mode-1, SPI-compatible interface establishes communication to the device. The ADS1120 device is offered in a leadless QFN-16 or TSSOP-16 package, specified from –40°C to +125°C. 图 5 shows the ADS1120 block diagram.

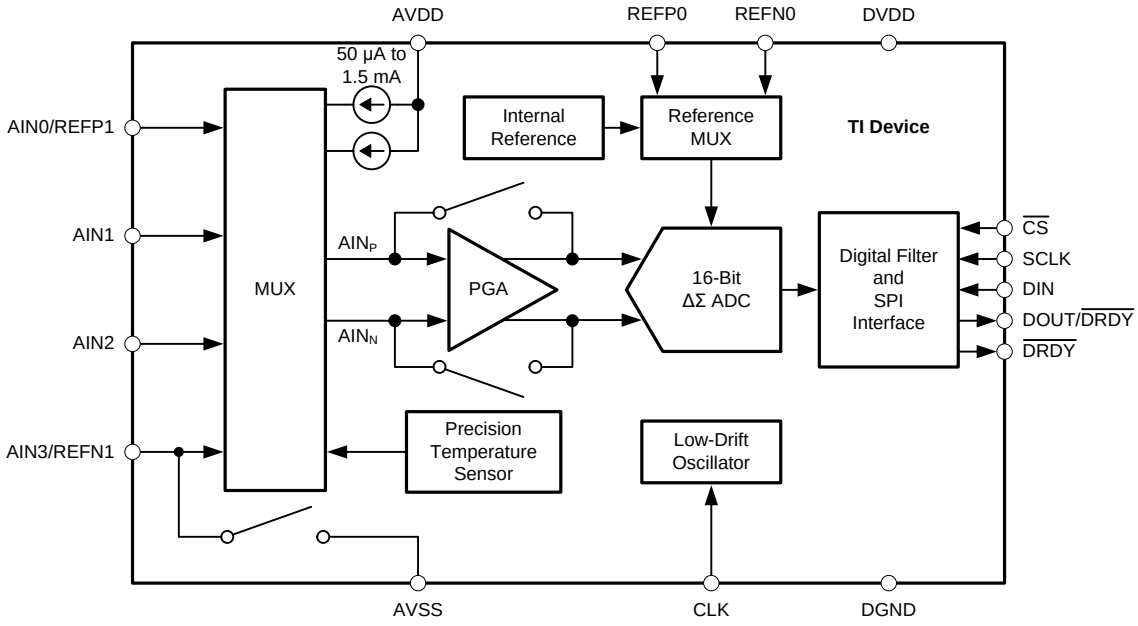


图 **5. ADS1120 Block Diagram**

ADS1120 features

- Low-current consumption:
  - Duty-cycle mode: 120 µA
  - Normal mode: 415 µA
- Wide supply range: 2.3 V to 5.5 V
- Programmable gain: 1 V/V to 128 V/V
- Programmable data rates: Up to 2 kSPS

- 16-bit, noise-free resolution at 20 SPS
- Simultaneous 50-Hz and 60-Hz rejection at 20 SPS, with a single-cycle settling digital filter
- Low-noise PGA: 90 nVRMS at 20 SPS
- Dual-matched, programmable current sources: 50 µA to 1.5 mA
- Internal 2.048-V reference: 5 ppm/°C drift (typical)
- Internal oscillator: 2% accuracy
- Internal temperature sensor: 0.5°C accuracy (typical)
- Two differential or four single-ended inputs
- SPI-compatible interface (mode 1)
- 3.5 mm × 3.5 mm × 0.9 mm QFN package

2.2.3 TPS7A16

The TPS7A16 family of devices consists of ultra-low power, LDO, voltage regulators that offer the benefits of ultra-low quiescent current, high-input voltage, and miniaturized, high-thermal performance packaging. The TPS7A16 family of devices offers an enable pin (EN) and an integrated, open-drain, active-high, power-good output (PG) with a user-programmable delay.

The TPS7A16 family of LDOs accepts a maximum input voltage of 60 V, which makes these LDOs designed for industrial applications where high-voltage transients are present.

图 6 shows the TPS7A1601 block diagram.

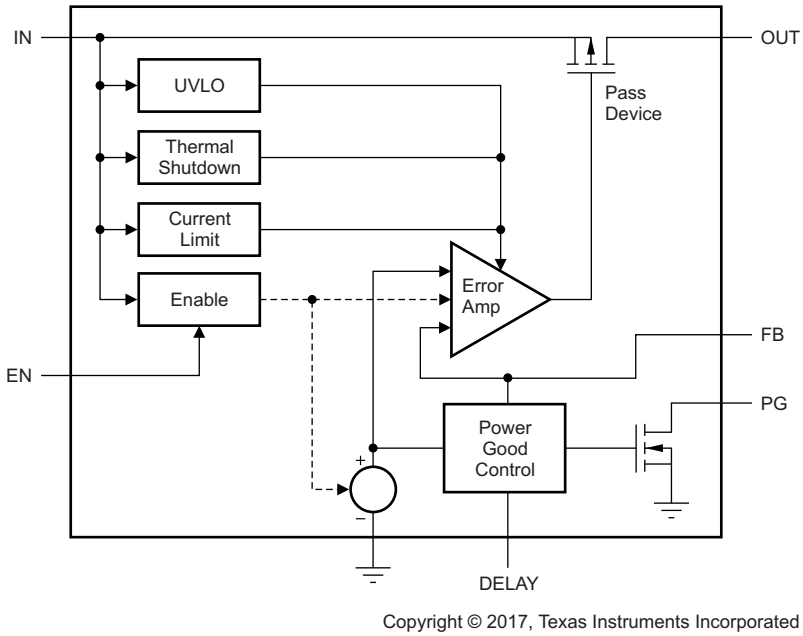


图 **6. TPS7A16 Block Diagram**

TPS7A16 features

- Wide input-voltage range: 3 V to 60 V
- Ultra-low quiescent current: 5 µA
- Quiescent current at shutdown: 1 µA

- Output current: 100 mA
- LDO voltage: 60 mV at 20 mA
- Accuracy: 2%
- Available in:
  - Fixed-output voltage: 3.3 V, 5 V
  - Adjustable version from 1.2 V to 18.5 V
- PG output with programmable delay
- Current limit and thermal-shutdown protections
- Stable, with ceramic output capacitors ≥ 2.2 µF
- Packages: high-thermal performance, MSOP-8 and SON-8 PowerPAD™
- Operating temperature range: –40°C to +125°C

2.3 System Design Theory

In this reference design, the remote sensor is an RTD temperature sensor that senses temperatures from –200°C to +850°C . This transmitter design translates the temperature to current. The relationship between the output-current value and measured temperature is set by an algorithm in the MCU. Here, 4 mA represents the minimum temperature (–200°C) and 20 mA represents the maximum temperature (850°C).

There are similar RTD temperature transmitter reference designs on TI.com. The RTD sensor-measurement and power-supply design circuits in this reference design are similar to TIDA-00095 and TIDA-00165. For the RTD measurement theory, including sensor-signal conditioning and ratio-metric measurement techniques, see RTD Temperature Transmitter for 2-Wire, 4- to 20-mA Current Loop Systems (TIDA-00095) and Small Form Factor, 2-Wire 4 to 20mA Current Loop RTD Temperature Transmitter Reference Design (TIDA-00165). This chapter focuses on how to design a current-loop control circuit with the SAC modules in the MSP4302355.

2.3.1 Smart Analog Combo

The SAC integrates a high-performance, low-power, operational amplifier (up to 33x PGA gain) and a 12-bit DAC core. The SAC can be used for signal conditioning of the input or output path.

SAC module features include the following:

- Op-Amp:
  - Rail-to-rail input
  - Rail-to-rail output
  - Multiple input selection
- PGA:
  - Configurable modes include buffer mode and PGA mode
  - PGA gain up to 33x
  - Supports inverting and noninverting modes
- DAC:
  - 12-bit DAC core

- Programmable setup time
- Internal or external reference selection
- Software selectable data loading

The SAC module has the following configurations: SAC-L1, SAC-L2, and SAC-L3 (see 表 2). SAC-L1 is the minimum feature set and SAC-L3 is the maximum feature set. Each configuration can work independently or multiple configurations can work together.

表 2. Smart Analog Combo Configuration

SAC STRUCTURE	FUNCTION
SAC-L1	Op-Amp
SAC-L2	Op-Amp and PGA
SAC-L3	Op-Amp , PGA, and DAC

图 7 shows the SAC L3 block diagram.

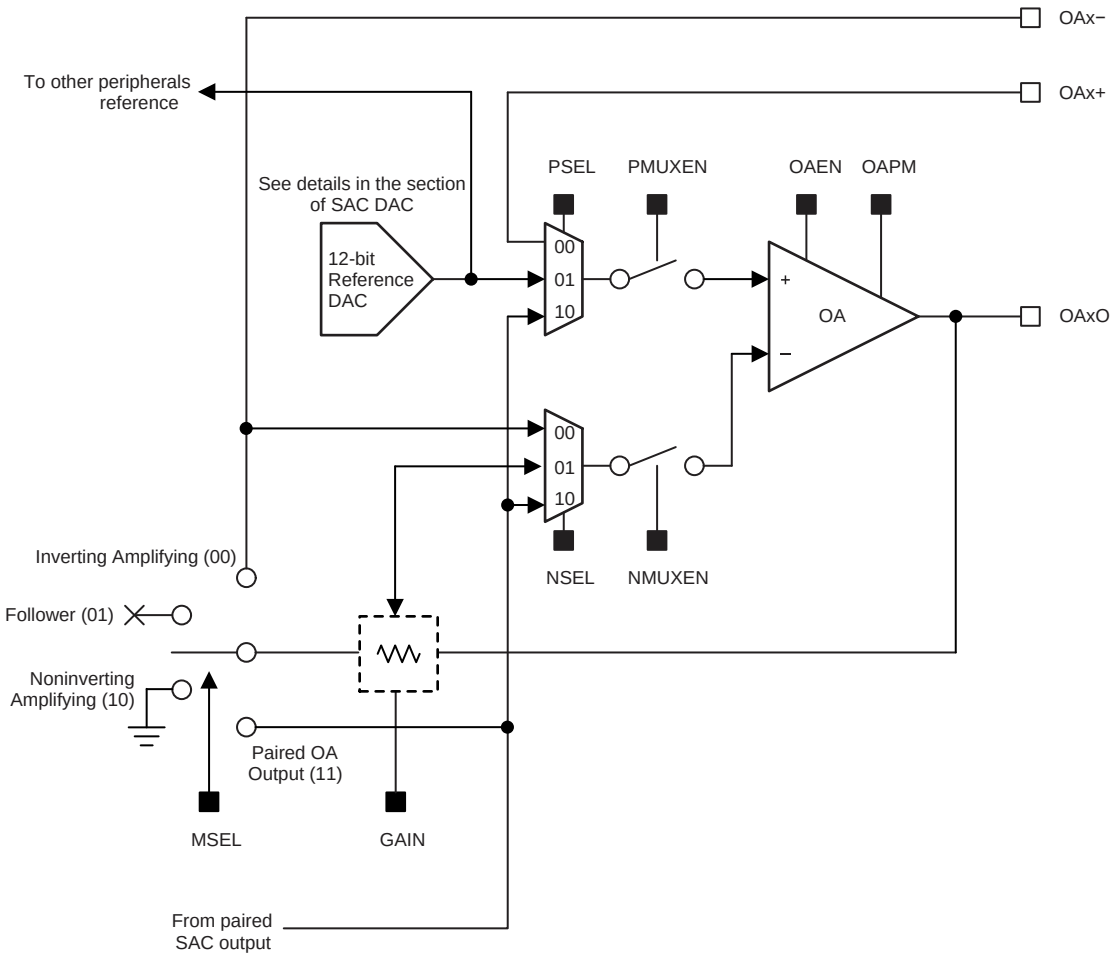


图 7. SAC-L3 Block Diagram

2.3.2 Current-Loop Control Circuit Design

As shown in 图 7, the DAC in the SAC-L3 module is a 12-bit DAC. The DAC can be used as the reference voltage and works with the Op-Amp and PGA to directly drive the output pad.

There are four SAC-L3 modules in the MSP430FR2355. In this design, two SAC-L3 modules are used. SAC3 is configured in DAC mode and Op-Amp is configured as an emitter-follower, to enhance the DAC drive capability (see 图 8).

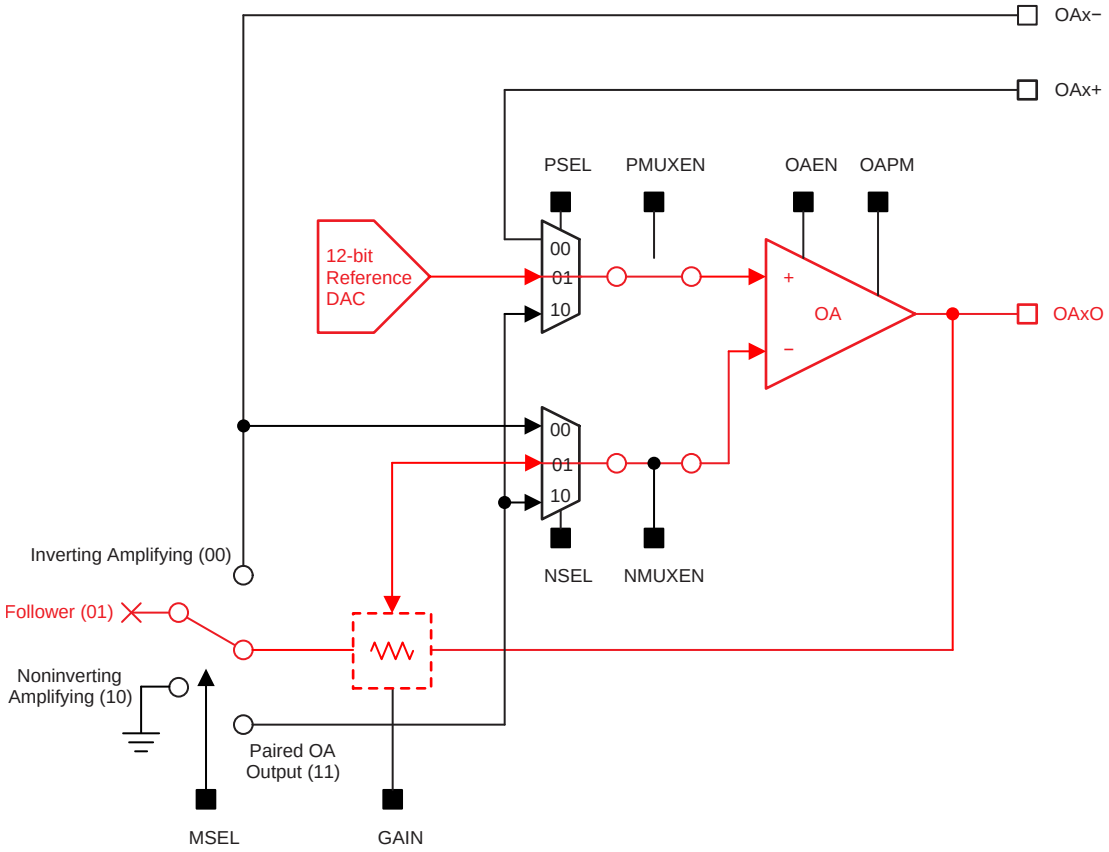


图 8. Configuration of SAC3

SAC1 is configured in general Op-Amp mode to construct an Op-Amp feedback amplifier, see 图 9.

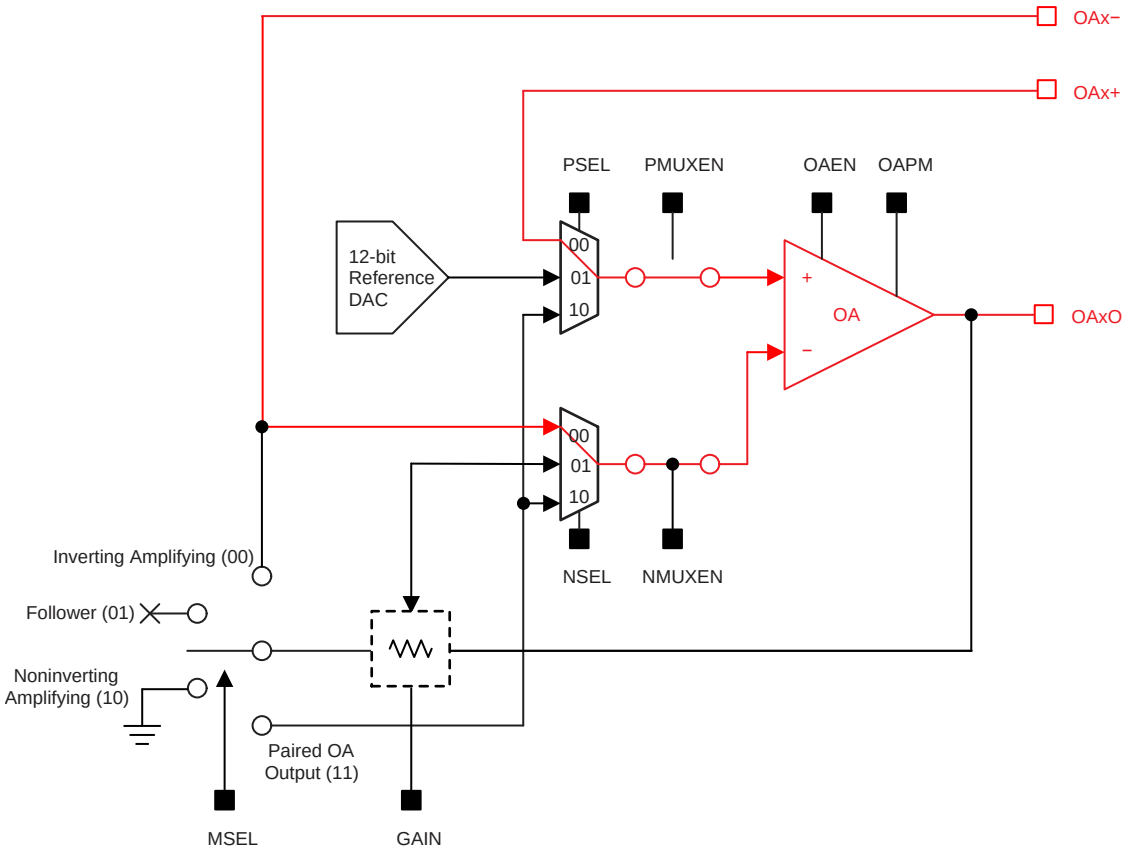


图 9. Configuration of SAC1

The output of SAC3 is connected to the positive input of the OA in SAC1. The output of the OA in SAC1 controls the gate voltage of an external transistor. 图 10 shows the block diagram.

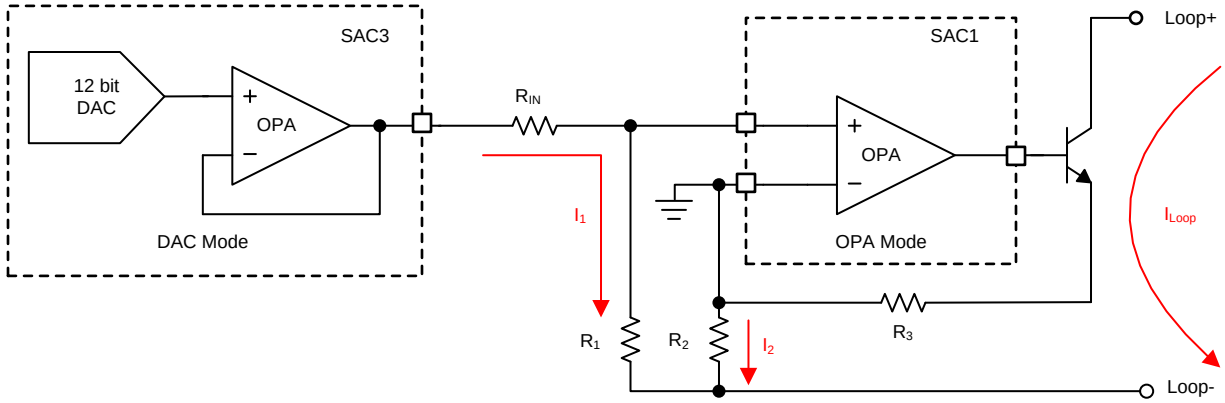


图 10. Connections Between SAC3 and SAC1

In 图 10, the loop current equals the sum of the current through R1 and R2 (see 公式 1).

$$I_{LOOP} = I_1 + I_2 \quad (1)$$

According to virtual short theory, in an OA feedback amplifier the voltage on the positive-input terminal approximately equals the negative-input terminal (see 公式 2).

$$V_{OPA+} = V_{OPA-} \tag{2}$$

Thus (see 公式 3):

$$I_1 \times R_1 = I_2 \times R_2 \tag{3}$$

And (see 公式 4):

$$I_1 = \frac{V_{DACOUT}}{R_{IN}} \tag{4}$$

Therefore, the loop current equation can be written as 公式 5.

$$I_{LOOP} = \frac{V_{DACOUT}}{R_{IN}} \times \left(1 + \frac{R_1}{R_2}\right) \tag{5}$$

DAC output voltage can be calculated using 公式 6.

$$V_{DACOUT} = \frac{V_{DAC\_CODE} \times V_{DACREF}}{2^{DAC\_resolution}} \tag{6}$$

In this design, the resolution of the DAC in the SAC module is 12 bit, and an internal 2.5-V shared reference is used as the DAC reference (see 公式 7).

$$V_{DACOUT} = \frac{2.5 \times DAC\_CODE}{2^{12}} \tag{7}$$

Which gives the following values:

R_1 = 99.9 kΩ

R_2 = 100 Ω

R_{IN} = 100 kΩ

Thus (see 公式 8):

$$I_{Loop} = \frac{V_{DACOUT}}{R_{IN}} \times \left(1 + \frac{R_1}{R_2}\right)$$

$$I_{Loop} = \frac{V_{DACOUT}}{100000} \times \left(1 + \frac{99900}{100}\right)$$

$$I_{Loop} = \left(\frac{DAC\_CODE}{2^{12}} \times 25\right) mA \tag{8}$$

The output range of SAC3 (V_{DACOUT}) is 0 to approximately 2.5 V. Therefore, the output-current resolution of the system is shown in 公式 9.

$25 / 2^{12} \approx 0.0061$ mA = 6.1 µA. (9)

2.3.3 Extend SAC Resolution

The 12-bit resolution of the DAC in the SAC-L3 module covers most use cases (see 图 11). For applications that require higher resolution, this chapter provides a solution to extend the DAC resolution with software. The DAC generates a particular ratio of the reference. Resolution (Δ or LSB) is the DAC reference divided by the total number of possible steps. For example, the DAC in the SAC module is 12 bits, so the total step number is 2^{12}. In this design, the DAC reference is 2.5 V. Therefore, the resolution (each step) is shown in 公式 10.

$$2.5\ V / 2^{12} = 0.61\ mV. \quad (10)$$

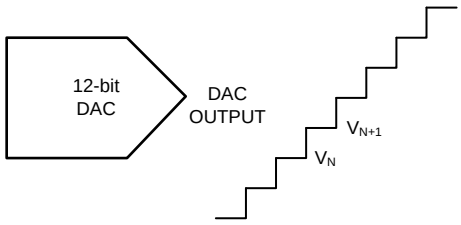


图 **11. DAC Output**

To increase the resolution, generate multiple values for each step by dithering the DAC output between V_N and V_{N+1}, similar to digital PWM and filtering the output to remove the ripples, so that a digital signal turns into a programmable analog voltage, see 图 12.

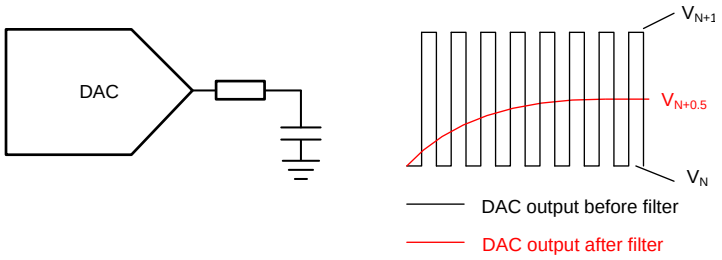


图 **12. DAC Output After Low-Pass Filter**

For example, if the DAC continuous-loop outputs 1 V_N and 1 V_{N+1}, this means two output values represent one step. After filtering with a RC low-pass filter, the output-analog voltage value is $V_{N+0.5}$. As a result, the DAC resolution is increased by 1 bit, see 图 13. If the DAC continuous loop outputs 4 or 2^2 values to represent one step, then the DAC resolution is increased by two bits, see 图 14. Thus, DAC resolution can be improved by using software to vary the PWM duty cycle.

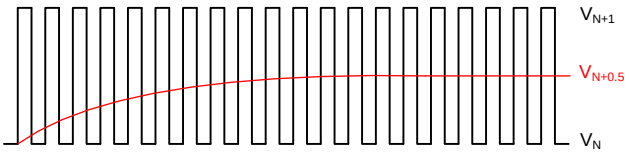


图 **13. 50% Duty-Cycle DAC Output**

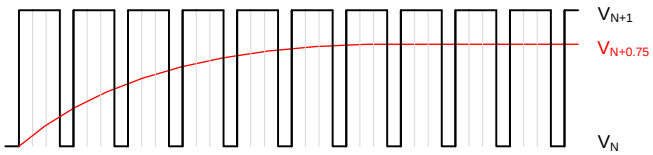


图 **14. 75% Duty-Cycle DAC Output**

Two key parameters in this solution are discussed in the following sections:

- PWM frequency
- Filter cut-off frequency

In the firmware, the DAC PWM signal is generated by the SAC3 output and timer B0. Timer B0 is configured to generate a periodic interrupt. The DAC output value is updated in the Timer B0 interrupt-service routine (ISR).

The relationship between the PWM frequency and timer-B0 interrupt frequency is shown in 公式 11.

$$F_{Timer\_B0} = F_{PWM} \times 2^n \quad (11)$$

where:

- F_{Timer_B0} is the required timer-interrupt frequency.
- F_{PWM} is the PWM-signal frequency.
- n is the desired, increased resolution of the DAC in bits.

In the firmware, an 8-element array is defined, to store the DAC-dither value, so that the DAC resolution increases by three bits in theory.

F_{PWM} is 1 kHz, and F_{Timer_B0} is 1 kHz × 2^3 = 8 kHz.

The ripple can be reduced to an acceptable level by filtering the output with a low-pass filter. In this design, use a low-pass RC filter. The values of the RC are dependent on the PWM frequency (FPWM). In this design, the PWM frequency is 1 kHz. To filter the enough harmonics, the cut-off frequency must be at least 10 times less than the PWM frequency. In this example, the cut-off frequency is 100 Hz.

2.3.3.1 Trade-Offs

A lower cut-off frequency filter results in less ripple time and longer settling time. A higher cut-off frequency filter results in more ripple time and shorter settling time. In this application, longer settling time is acceptable.

Increasing the F_{PWM} frequency moves the harmonics further from the DC offset. The trade-off is to increase F_{Timer_B0} so that the MCU power consumption increases.

For more details on the RC low-pass filter design for PWM, see the Voice Band Audio Playback Using a PWM DAC (TIDU-703A)reference design and Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x Digital Signal Controller application report. Because of the system-noise floor, the resolution cannot have unlimited increase. TI provides a SPICE-based, analog-simulation program (TINA-TI), to help users develop and simulate filter configurations. Other resources are also available online (for example, the RC Low-Pass Filter Design Tool).

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

3.1.1 Hardware

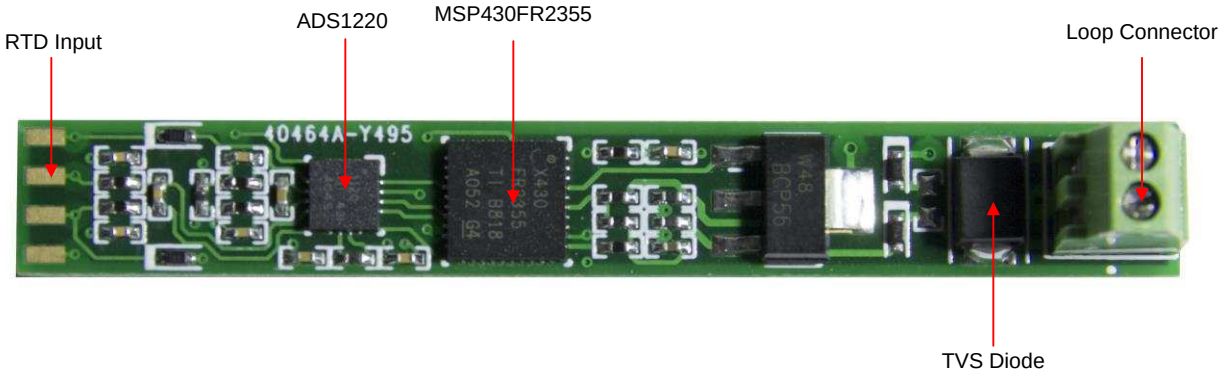


图 **15. Top-Side PCB Assembly View**

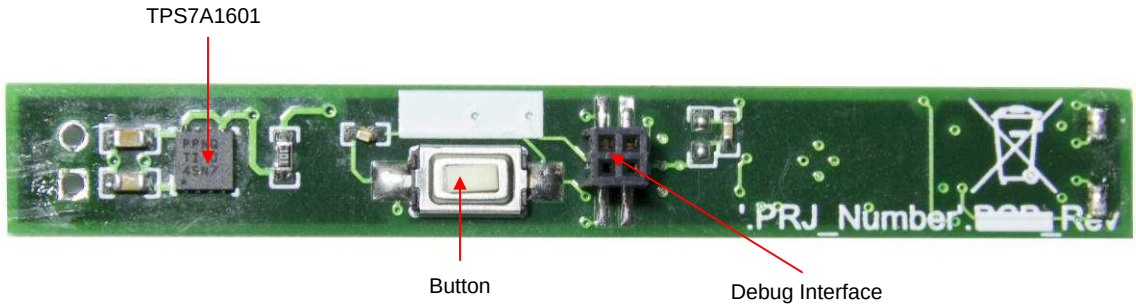


图 **16. Bottom-Side PCB Assembly View**

3.1.1.1 Getting Started

A 20- to 30-V range power supply powers the system. TI recommends setting the current limit of the power supply to 40 mA. The theoretical maximum that the system must draw from the power supply is 25 mA.

Connect a precision multimeter in series with the power supply. TI recommends a 6.5-digit multimeter.

图 17 shows the basic setup in test mode. A precision resistor (0.01%) connected to the RTD inputs emulate a 2-wire RTD connection (jumpers J4 and J2 are installed).

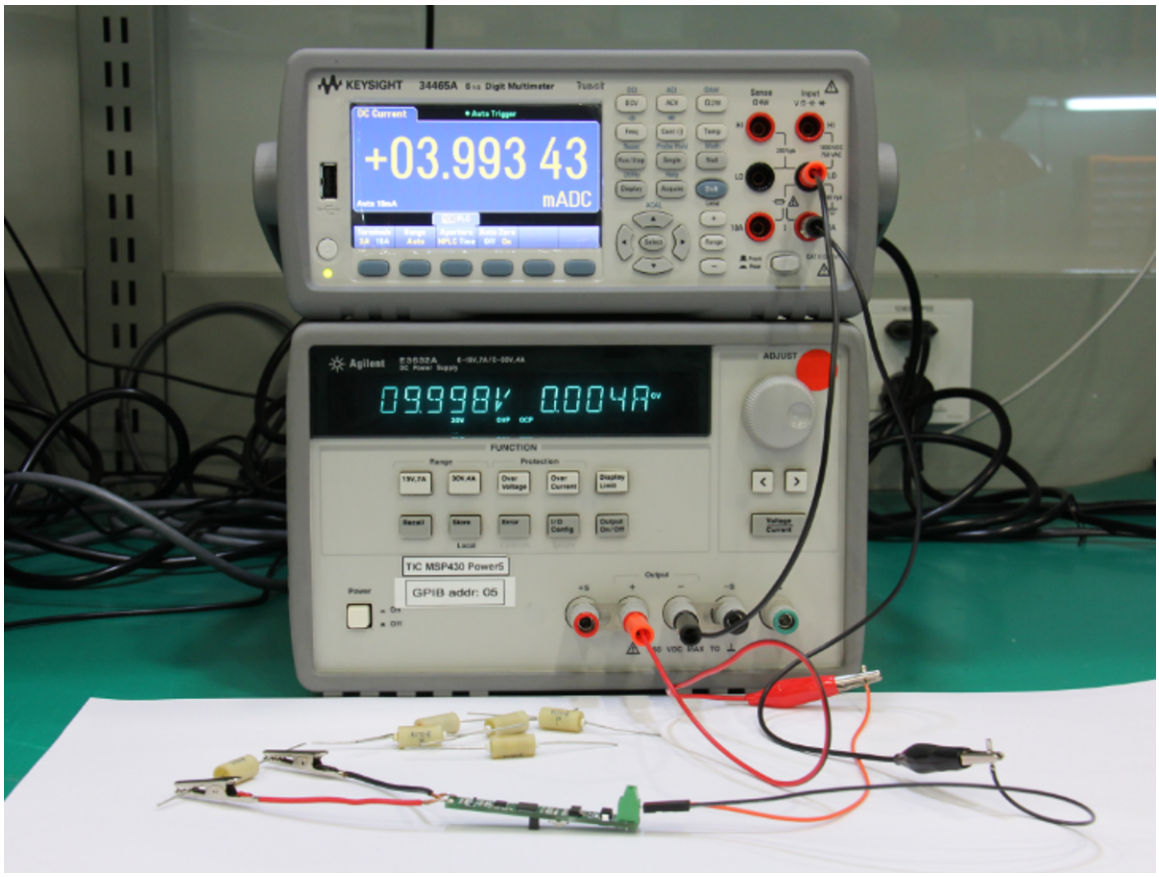


图 17. Basic Setup in Test Mode

图 18 shows the basic setup in functional mode. In this setup, the connection is a 3-wire RTD and as a result, J4 is installed and J2 is not installed, as listed in 表 3.

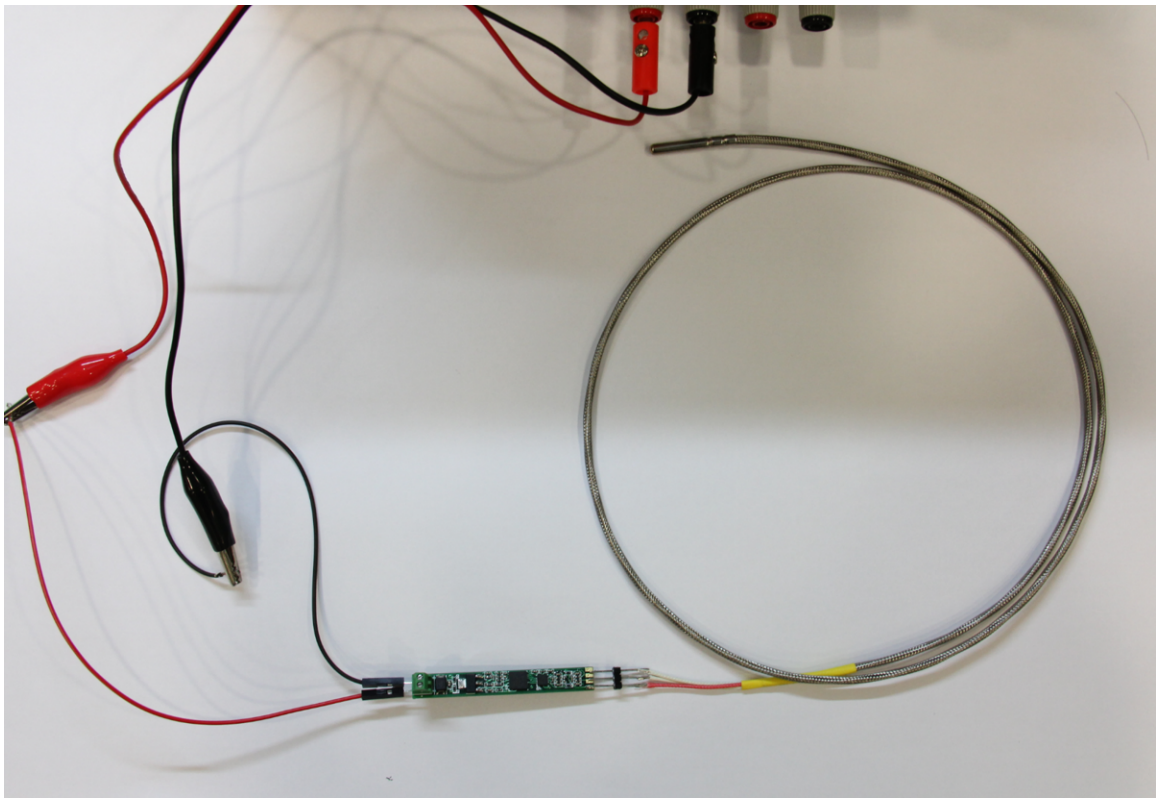


图 18. Basic Setup in Function Mode

The design supports 2-wire, 3-wire, and 4-wire RTD. 表 3 lists the jumper configurations, as shown in 图 19.

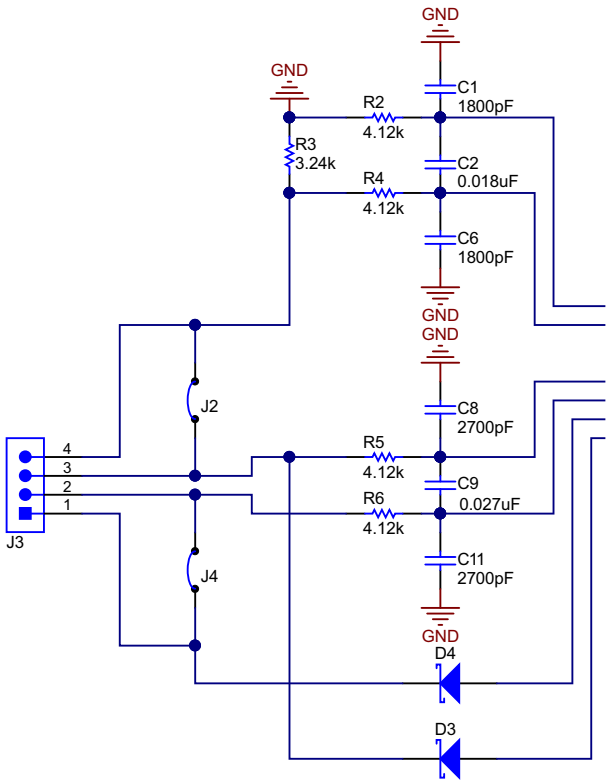


图 19. Jumper Configurations for Different RTD Sensor

表 3. 2-Wire, 3-Wire, and 4-Wire RTD Support

SETUP	CONNECTORS		RTD LOCATION
	INSTALLED	NOT INSTALLED	
2-wire	J2 and J4	—	2-wire RTD is installed between pins 2 and 3 of J3.
3-wire	J4	J2	3-wire RTD is installed between pins 2, 3, and 4 of J3.
4-wire	—	J2 and J4	4-wire RTD is installed between pins 1, 2, 3, and 4 of J3.

3.1.2 Software

The software code is designed to implement a temperature-transmitter application that highlights the ADS1120, to receive data from an RTD temperature probe and send out the temperature reading on a 4- to 20-mA signal using an SAC module in the MSP430FR2355. The software code addresses system-level calibration, offset, and gain, that is implemented to improve ADC and DAC accuracy and includes linear interpolation to address the nonlinearity of the RTD element.

The firmware project of this TI reference design can be downloaded from TIDM-01000.

For MSP430 firmware updates, TI recommends Code Composer Studio™ (CCS), see 图 20. CCS is an integrated development environment (IDE) for TI embedded-processor device families. CCS comprises a suite of tools used to develop and debug embedded applications. CCS includes compilers for each of the device families from TI, source-code editors, project-build environments, debuggers, profilers, simulators, real-time operating systems, and other features.

An MSP430 debugger interface, such as MSP-FET, is required, as shown in 图 20.

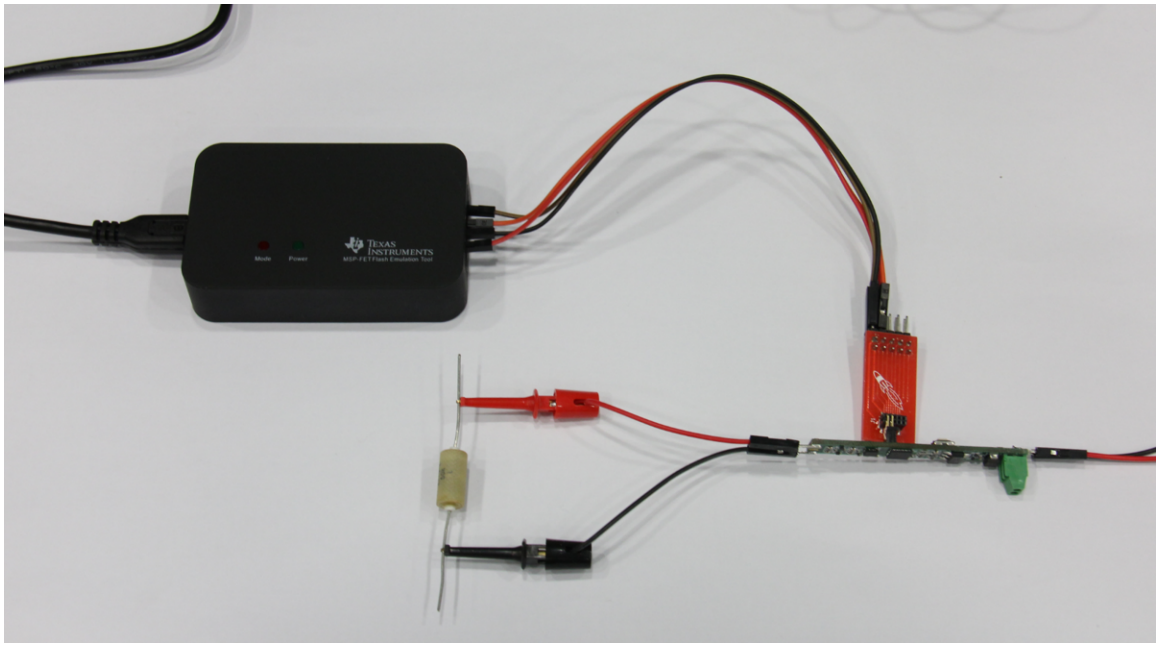


图 **20. MSP-FET to Program System**

Firmware is downloaded with the Spy-Bi-Wire (SBW) debug interface. The connector J5 on the board programs and debugs the code.

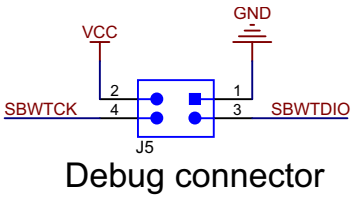


图 **21. SBW Debug Interface**

CAUTION

Be careful during debugging to avoid damages, due to different power domains in conflicts (4- to 20-mA loop power and debugger tools power). Read the following sections carefully.

3.2 Testing and Results

The overall system performance is governed by ADC accuracy, DAC accuracy, and resolution. This section characterizes the ADC for resolution and error (adjusted for offset and gain calibration). The DAC is then characterized for resolution and error (adjusted for offset and gain calibration). Finally, a full system characterization is performed, for maximum-measured error of the complete system.

注: The test data in this section was measured at room temperature using calibrated lab equipment, unless otherwise specified.

3.2.1 ADS1120 Error Characterization

To test the accuracy of the acquisition circuit alone, a series of high-precision discrete resistors were used as the input to the system. The offset error is attributed largely due to the offset of the internal PGA and ADC, while the gain error is attributed to the accuracy of the R_{REF} resistor and gain error of the internal PGA and ADC. The ADC error characterization includes corrections for any mismatches in excitation currents, offset errors, and gain errors.

The following equipment was used for the testing.

- 30-V DC power supply, with current limit set to 50 mA.
- 6.5-digit multimeter, functional as a DC ammeter and connected in series with the power supply
- 6.5-digit multimeter, to measure the high-precision resistors accurately using a 4-W resistance measurement method, as shown in 图 22
- MSP340 emulator (MSP-FET) for programming and debugging.
- 390-Ω, external-load resistor connected in series with the DC power supply and ammeter

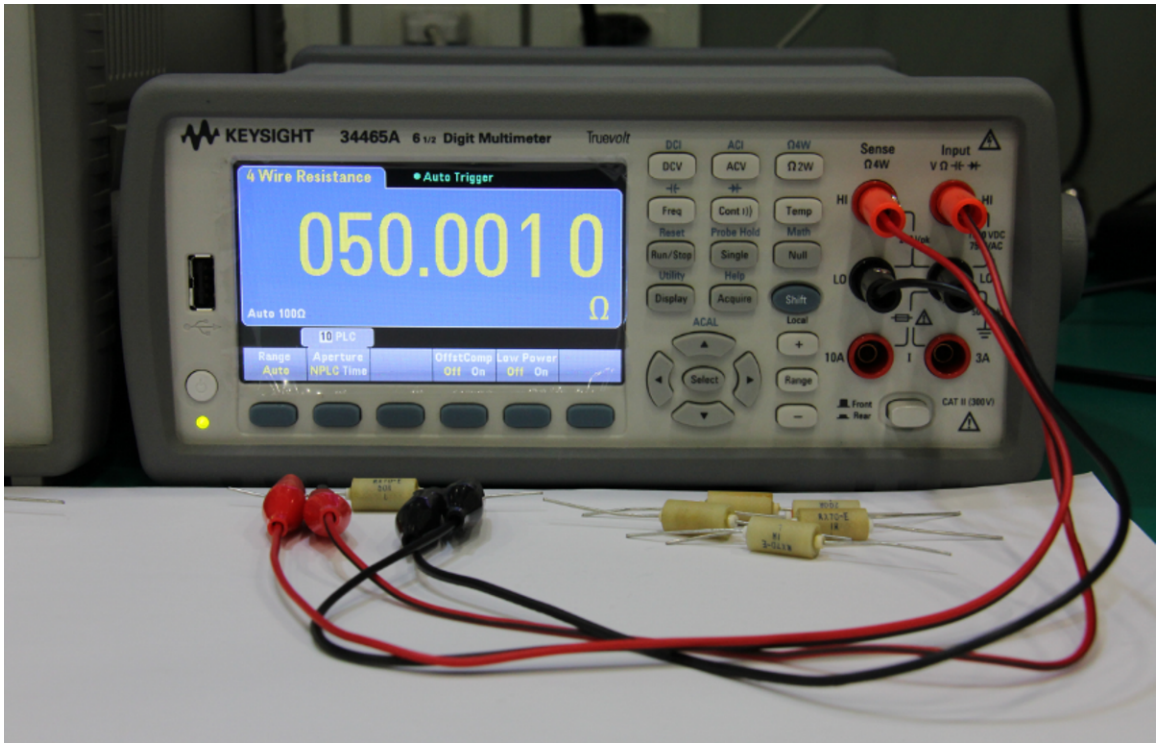


图 22. 4-Wire Resistance Measurement Using 6.5-Digit Multimeter

Use the following steps to carry out the testing.

1. Start with the smallest-value, precision resistor that represents RTD resistance at the lowest scale. Measure the resistance of the smallest-value, precision resistor using the 6.5-digit multimeter in 4-W mode, and record the measured value. Ensure that the measuring probes make secure contact with the resistor leads and avoid any human contact, because human contact may affect the resistance measurement.
2. Immediately connect the resistor already used in Step 1 to the board.
3. Power-up the board.
4. Test the software running in the MSP430 MCU, to record the excitation current and mismatch-corrected ADC code before and after offset calibration in the internal memory of the MSP430 MCU. The recorded samples are then exported to an Excel® spreadsheet using the CCS IDE on the PC. Preserve these samples safely in the Excel sheet for further calculations.
5. Repeat these steps until the highest-value precision resistor representing the RTD resistance at full-scale is obtained. Keep recording the samples in the Excel spreadsheet.

Gain calibration occurs when a full-scale precision resistor of 390 Ω is connected. A 390-Ω resistor corresponds to approximately 848.36°C in temperature, which is quite close to the full-scale temperature of 850°C. Then, the gain factor is determined by dividing the full-scale, reference-precision resistor with the measured full-scale resistance after offset calibration. Finally, the gain correction is applied to all the measured resistances after offset calibration

注: The MSP430 firmware algorithm averages a given number of measurements, with offset correction applied to an expected result, with a 390-Ω resistor connected to determine the gain calibration factor. To execute the algorithm, the S1 switch must be pressed with a 390-Ω resistor in place. The gain calibration factor is determined and stored in the FRAM. Gain calibration must be performed after compensating for offset error.

表 **4. Precision Resistors Corresponding Temperature Values**

PRECISION RESISTOR VALUE(1)	REFERENCE TEMPERATURE °C
20.0068	–196.556015
50.0061	–125.131149
70.0119	–75.798248
100.014	0.0358056
120.019	51.615582
150.017	130.492020
170.011	184.143661
199.998	266.341675
219.997	322.388092
250.026	408.526184
270.024	467.299652
300.02	557.749207
319.991	619.609375
350.035	715.373352
370.027	781.046509
390.027	848.448669

(1) As measured by the 6.5-digit multimeter (ω)

表 **5. ADC Error After Gain and Offset Calibration**

PRECISION RESISTOR VALUE (Ω)(1)	REFERENCE TEMPERATURE (°C)(2)	RTD CALCULATION (Ω) (3)	TEMPERATURE READING (°C)(4)	MEASURED ERROR OF ADC (°C)
20.0068	–196.556015	20.010223	–196.548096	0.007919
50.0061	–125.131149	50.019379	–125.098839	0.032310
70.0119	–75.798248	70.041962	–75.723290	0.074959
100.014	0.035806	100.026398	0.067514	0.031708
120.019	51.615582	120.048981	51.693459	0.077877
150.017	130.492020	150.058136	130.601440	0.109420
170.011	184.143661	170.031281	184.198608	0.054947
199.998	266.341675	200.040436	266.459534	0.117859
219.997	322.388092	220.013580	322.435089	0.046997
250.026	408.526184	250.072174	408.660400	0.134216
270.024	467.299652	270.045319	467.362946	0.063294
300.020	557.749207	300.029755	557.779114	0.029907
319.991	619.609375	320.002899	619.646606	0.037231
350.035	715.373352	350.036774	715.379089	0.005737
370.027	781.046509	370.084076	781.236145	0.189636
390.027	848.448669	390.032501	848.467468	0.018799

(1) As measured by the 6.5-digit Multimeter
(2) Based on measured precision resistor, calculated with Callendar-Van Dusen equations
(3) Based on ADC code after gain and offset calibration
(4) Running linearization after offset and gain calibration

图 23 shows the temperature error after applying the simple first-order offset and gain calibration over a –200°C to +850°C temperature range. The temperature error still shows some variations, even after applying the offset and gain calibration. The temperature error is attributed mainly due to nonlinearity errors associated with the ADC and PT100 RTD look-up table. The nonlinearity errors are difficult to correct using a simple linear equation. Higher-order polynomial approximation may be used to correct the nonlinearity errors.

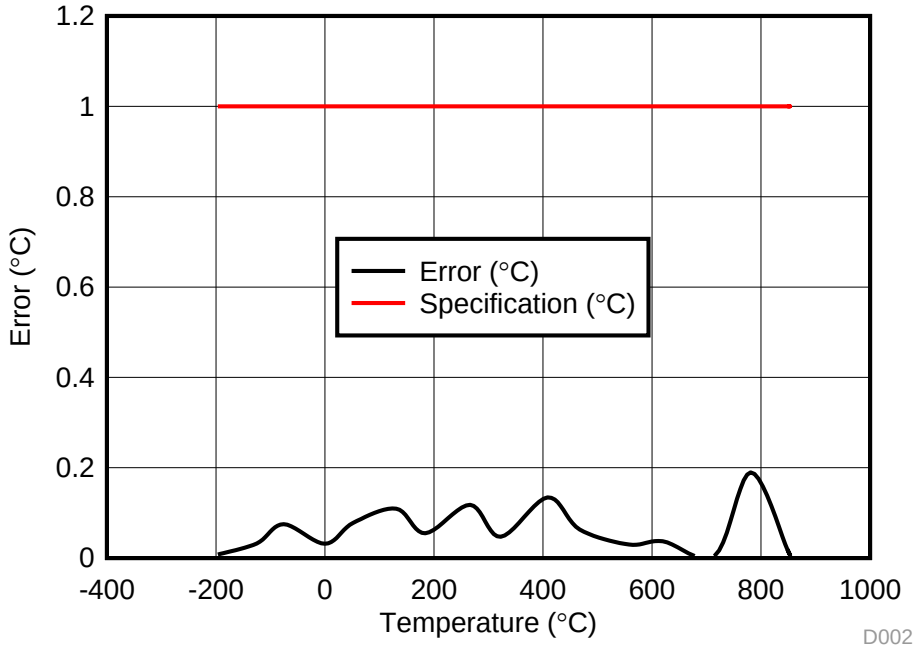


图 **23. Measured ADC Error After Calibration**

3.2.2 SAC Output Current Resolution

For this test, the SAC output was programmed for a fixed, 4-mA output current, and multiple samples were recorded over time using a 6.5-digit multimeter. The minimum and maximum currents recorded were 4.012451 mA and 4.013822 mA, respectively. Therefore, the noise-free resolution in terms of output current is 1.37 µA (see 图 24).

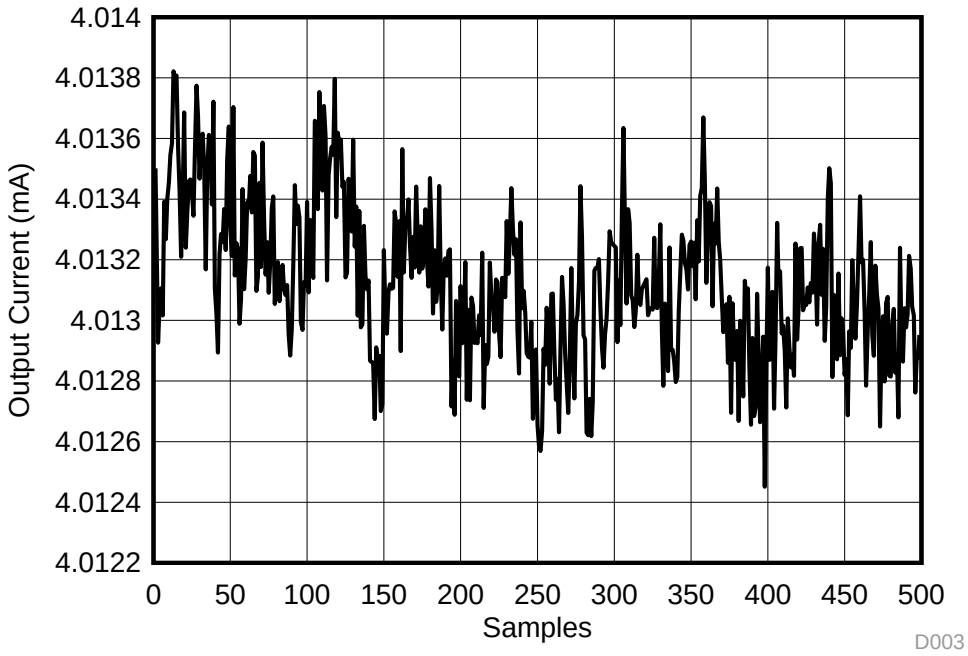


图 **24. SAC Output Resolution**

3.2.3 SAC Error Characterization

To perform SAC error characterization, the MSP430 MCU was programmed to generate the output-loop current from 4 mA to 20 mA, in steps of 2 mA (see 表 6). The output current was increased by 2 mA each time the S1 switch was pressed. The output-loop current was measured using a 6.5-digit multimeter.

表 **6. SAC Error Characterization**

SAC VALUE APPLIED (mA)	LOOP CURRENT MEASURED (mA)	
	BEFORE GAIN AND OFFSET CALIBRATION	AFTER GAIN AND OFFSET CALIBRATION
4	4.012413	4.000621
6	6.007311	6.001562
8	7.999695	8.000524
10	9.990082	9.998756
12	11.98229	12.00102
14	13.97203	13.99825
16	15.95988	15.99846
18	17.95467	17.99587
20	19.95354	19.99936

As shown in 图 25, without gain and offset calibration, an error is seen in the loop current. This error increases linearly with the loop current. A simple gain and offset calibration implemented in the MSP430 fixes this error.

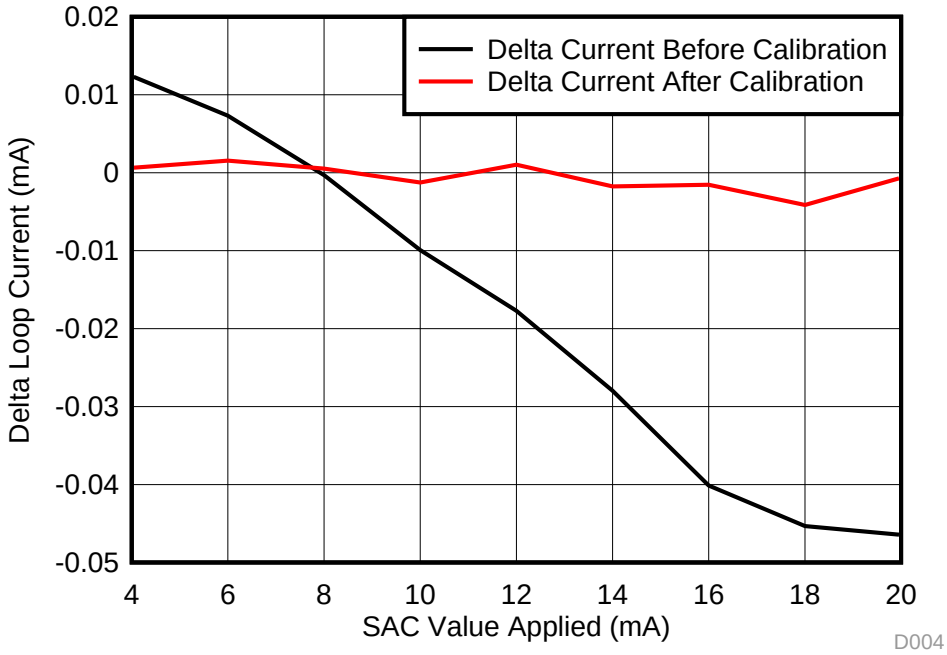


图 25. Measured Output Loop Current Error Before And After Calibration

3.2.4 Complete-System, Maximum-Measure Error

After correcting the ADC and SAC for gain and offset calibration, a complete system characterization was performed for maximum measured error. In this setup, a power supply and 6.5-digit multimeter were used for loop current measurement. As shown in 图 26, multiple precision-resistor values were used, covering –200°C to 850°C, similar to those used in 图 22.

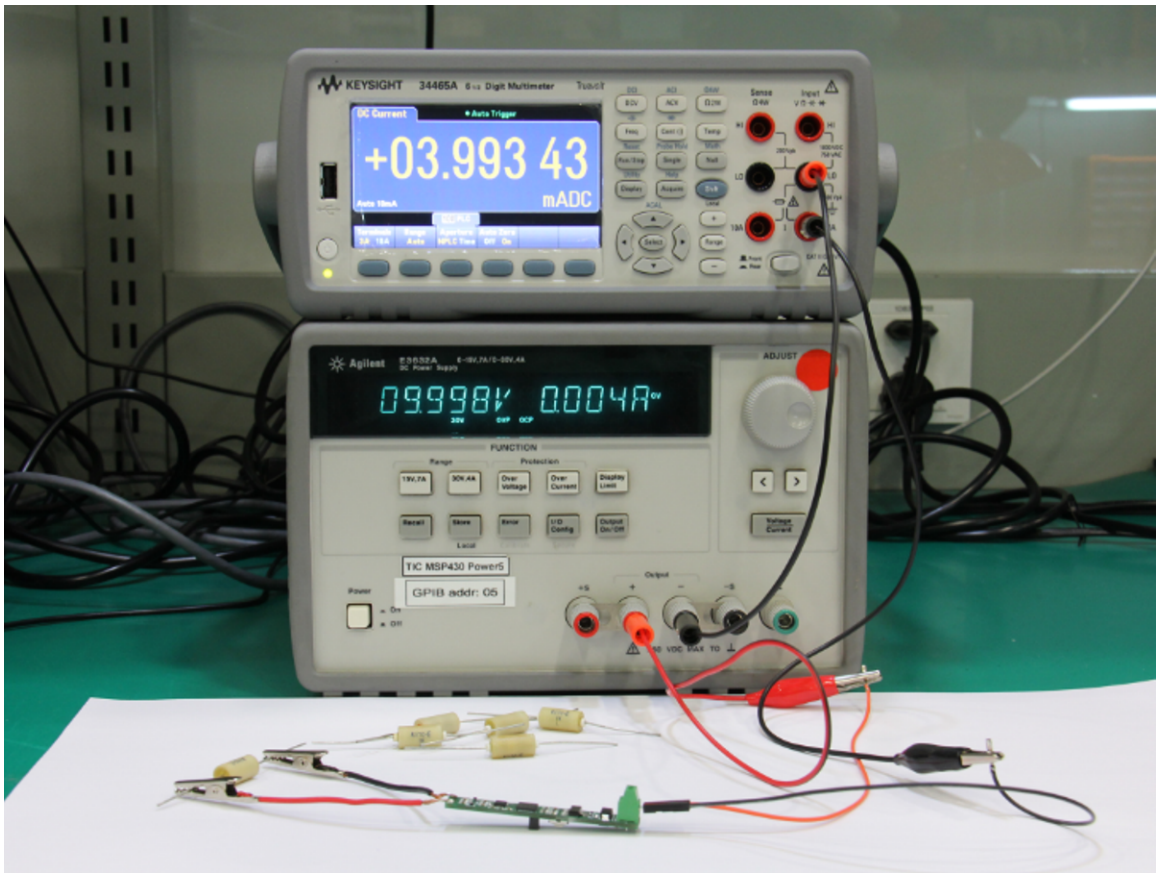


图 **26. Complete System Maximum Measured Error Test**

表 **7. Maximum Measured Error of the System**

PRECISION RESISTOR VALUE (Ω)(1)	REFERENCE TEMPERATURE (°C)(2)	IDEAL LOOP CURRENT (mA)(3)	MEASURED OUTPUT LOOP CURRENT (mA)(4)
20.0068	–196.556015	4.052480	4.052370
50.0061	–125.131149	5.140859	5.144854
70.0119	–75.798248	5.892598	5.897162
100.014	0.035806	7.048165	7.053314
120.019	51.615582	7.834142	7.836075
150.017	130.492020	9.036069	9.036823
170.011	184.143661	9.853618	9.853028
199.998	266.341675	11.106159	11.10631
219.997	322.388092	11.960199	11.95832
250.026	408.526184	13.272780	13.26872

(1) As measured by the 6.5-digit multimeter
(2) Based on the measured precision resistor
(3) Based on the reference precision resistor
(4) Current of the system for the connected, reference precision resistor

表 **7. Maximum Measured Error of the System (continued)**

270.024	467.299652	14.168376	14.16165
300.02	557.749207	15.546655	15.54218
319.991	619.609375	16.489286	16.48634
350.035	715.373352	17.948546	17.94501
370.027	781.046509	18.949280	18.94982
390.027	848.448669	19.976361	19.97589

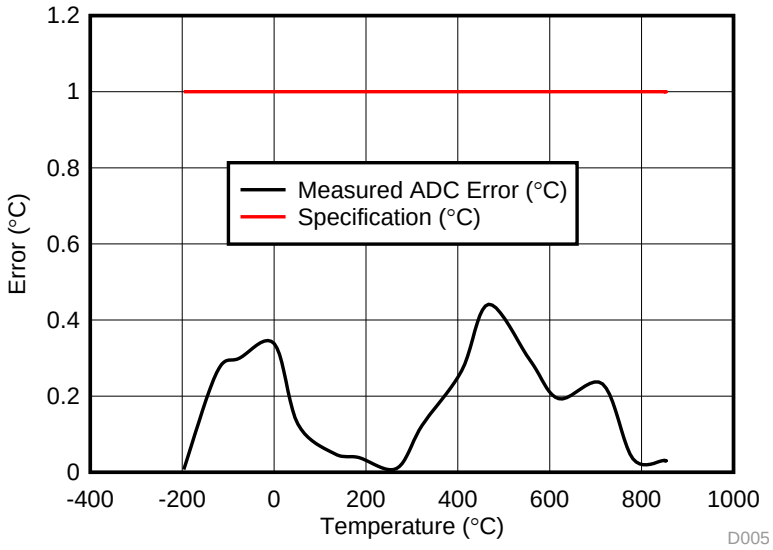


图 **27. Maximum Measured Error of Complete System**

3.2.5 Power Supply Influence

For the power-supply influence test, the power supply was vetted from 10 V to 30 V, and the corresponding loop-current change was recorded. The DAC output was programmed for a fixed 4-mA output current for this measurement. The total deviation of the loop current across the power supply range was approximately 0.24 μA, as shown in 图 28 and 图 29.

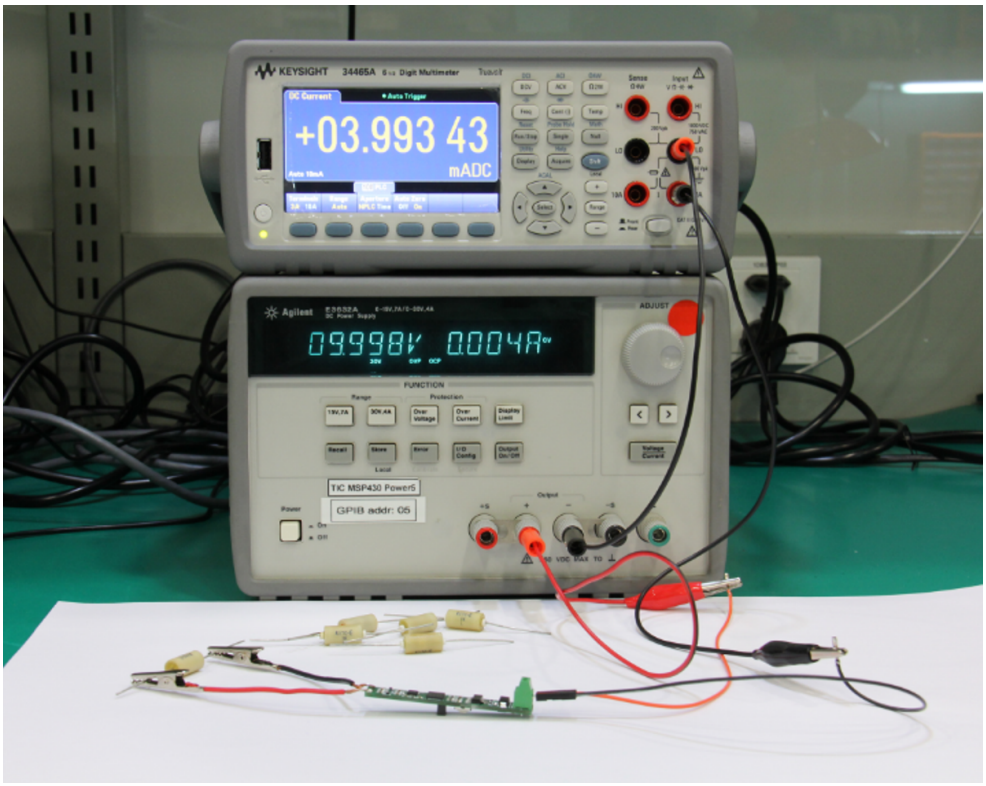


图 **28. 10-V Power Supply on Output Loop Current**

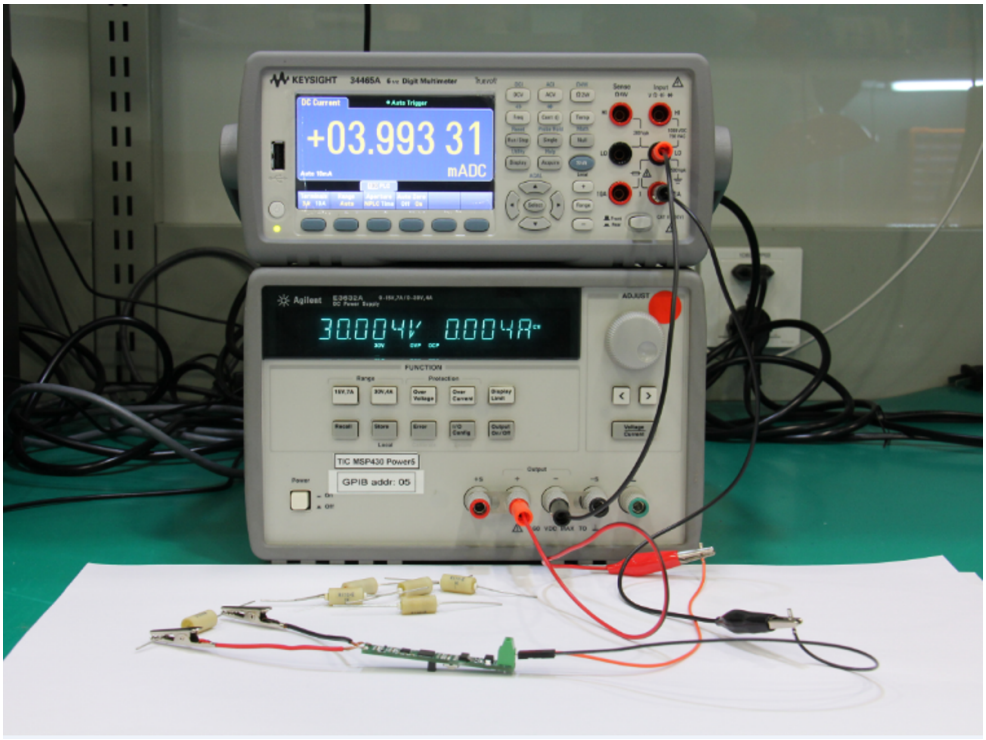


图 **29. 30-V Power Supply on Output Loop Current**

3.2.6 Reverse-Polarity Test

For this test, a 30-V power supply was connected to the J1 loop interface connector in reverse polarity, without any polarized capacitor, as shown in 图 30. The leakage current drawn by the system recorded was 14.39 nA.

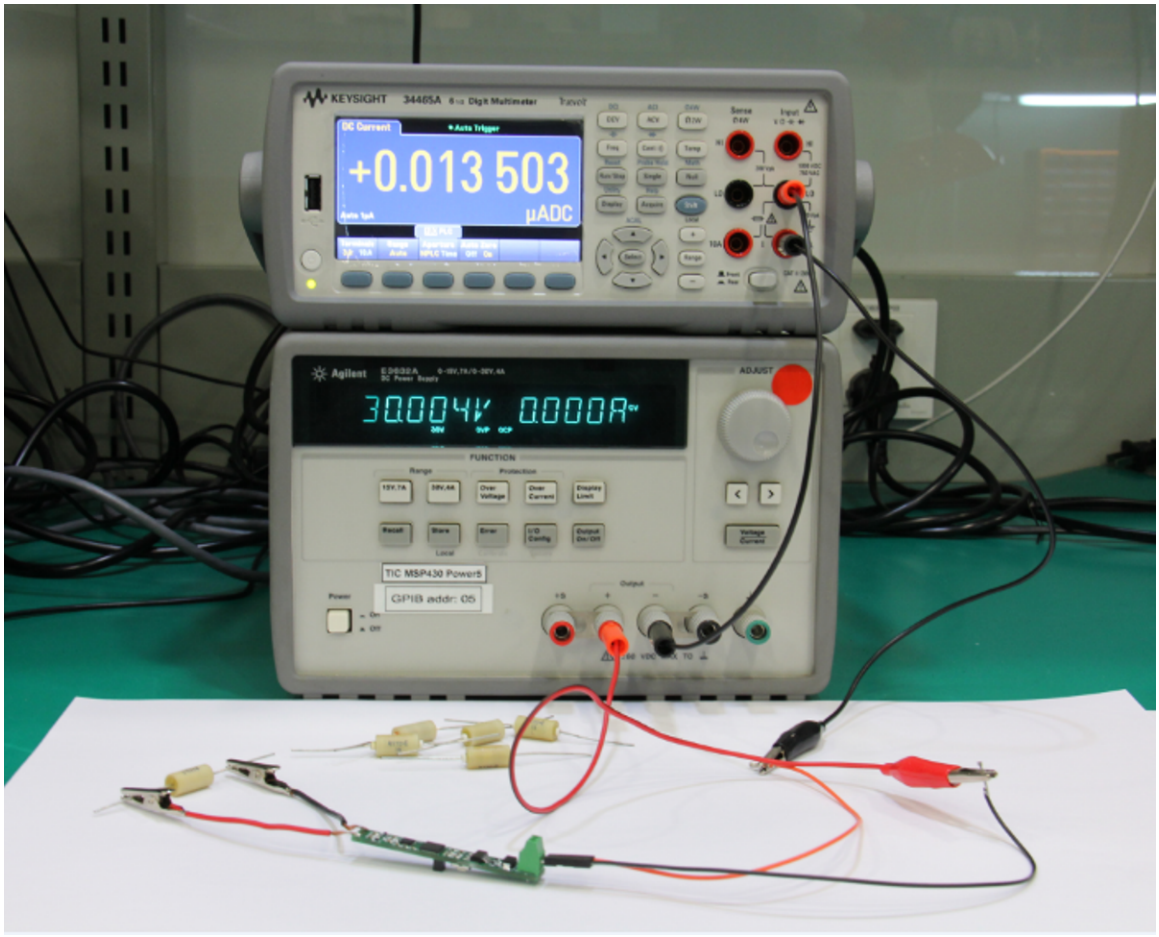


图 **30. Reverse-Polarity Protection Test**

3.2.7 Loop Power Consumption

The total loop power consumed by the design is 1.58 mA. 表 8 lists the total current consumed by each device.

表 **8. Loop Power Consumption**

DEVICE	CURRENT CONSUMPTION
ADS1120	340 µA + 75 µA + 500 µA (biasing currents) = 915 µA (PGA 16, normal mode, sample rate of 20 SPS)
MSP430FR2355	660 µA (MCU at 1 MHz, 3.3 V + DAC + 2OP + REFO + Shared REF)
TPS7A1601	5 µA

For a loop-powered system, a low-power consumption of approximately 1.6 mA ensures that the remainder of the budget (approximately [3.3 mA to 1.6 mA] = approximately 1.7 mA) can be used for system-level functions such as HART modem implementation.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDM-01000.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDM-01000 .

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDM-01000.

4.4 Altium Project

To download the Altium Designer® project files, see the design files at TIDM-01000.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDM-01000.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDM-01000.

5 Software Files

To download the software files, see the design files at TIDM-01000.

6 Related Documentation

1. Texas Instruments, RTD Temperature Transmitter for 2-Wire, 4- to 20-mA Current Loop Systems (TIDA-00095), reference design
2. Texas Instruments, Small Form Factor, 2-Wire 4 to 20mA Current Loop RTD Temperature Transmitter Reference Design (TIDA-00165), reference design
3. Texas Instruments, Voice Band Audio Playback Using a PWM DAC (TIDM-VOICEBANDAUDIO), reference design
4. Texas Instruments, Using PWM Output as a Digital-to-Analog Converter on a TMS320F280x Digital Signal Controller, application report

6.1 商标

7 About the Author

LING ZHU is an Applications Engineer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Ling brings to this role his extensive experience in embedded-processor, capacitive touch, and low-power system-level design expertise. Ling earned his Master of Science in Xidian University in Xi'an, China.

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