TI Designs：TIDA-01379
瞬态负载发生器参考设计

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资源

TIDA-01379	设计文件夹
CSD17304Q3	产品文件夹
CSD25404Q3	产品文件夹
CSD18534Q5A	产品文件夹
OPA365	产品文件夹

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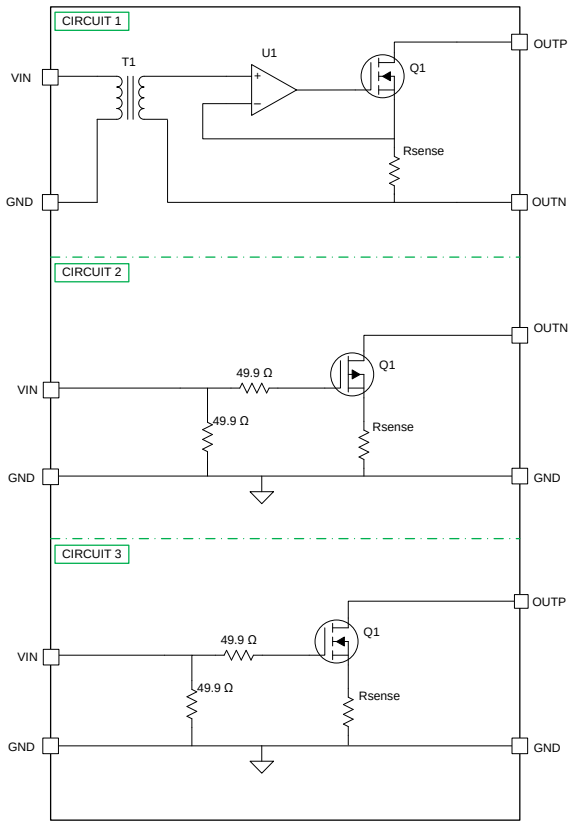
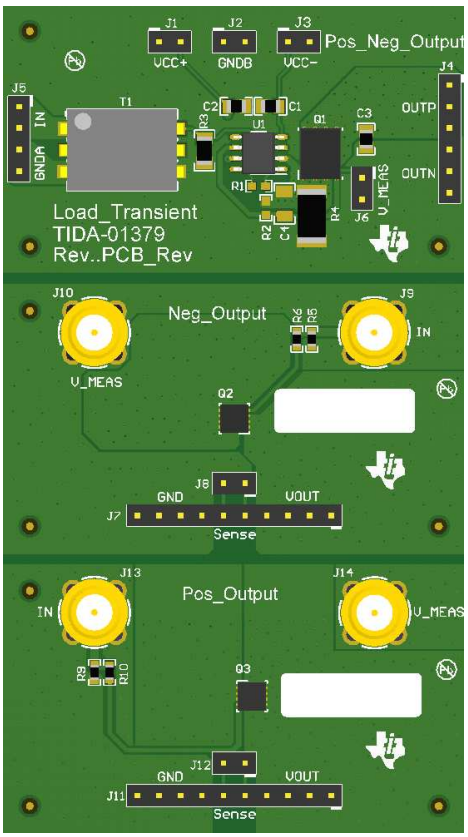
特性

- 快速瞬态
- 浮动负载和以地为基准的负载
- 稳压
- 隔离式

应用

- 电源测试





1 System Description

Power supplies are present in all electronic devices where they power the needed supply rails. These rails need to be maintained at a certain level under the specified operating conditions, including load transient events. A load transient event happens when the load current changes suddenly from one level to another. The response of a converter to such changes permits to assess its stability.

The TIDA-01379 design board includes three different circuits that are used to perform load transient measurements for different load configurations. These circuits provide faster rise and fall times than commercial transient generators at a lower cost.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER	SPECIFICATIONS
Load current	≥ 500 mA
Rise and fall time	< 1 µs
Maximum load output voltage	20 V

2 System Overview

2.1 Block Diagram

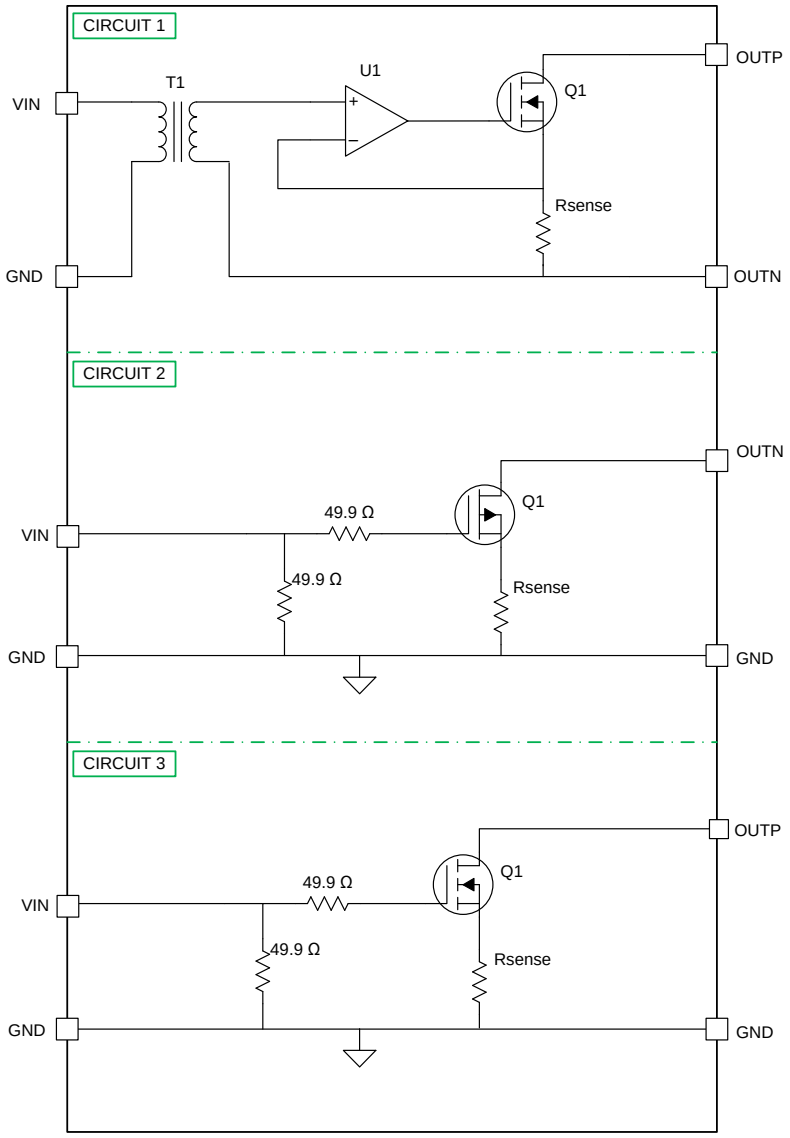


图 1. TIDA-01379 Block Diagram

2.2 Highlighted Products

2.2.1 CSD17304Q3

The CSD17304Q3 device is a 30-V, N-channel, NexFET™ power MOSFET with the following features:

- Optimized for 5-V gate drive
- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating

For further details, see the CSD17304Q3 product page.

2.2.2 CSD25404Q3

The CSD25404Q3 device is a –20-V, P-channel, NexFET power MOSFET with the following features:

- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Low $R_{DS(on)}$
- Halogen free
- RoHS compliant

For further details, see the CSD25404Q3 product page.

2.2.3 CSD18534Q5A

The CSD18534Q5A device is a 60-V, N-channel NexFET power MOSFET with the following features:

- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Logic level
- Pb-free terminal plating

For further details, see the CSD18534Q5A product page.

2.2.4 OPA365

The OPA365 device is a rail-to-rail input and output operational amplifier with a gain bandwidth of 50 MHz. This amplifier has a slew rate of 25 V/µs and can settle to 0.01% in 0.3 µs.

The OPA365 has the following features:

- Gain bandwidth: 50 MHz
- Zerø-crossover distortion topology:
  - Excellent THD+N: 0.0004%
  - CMRR: 100 dB (minimum)
  - Rail-to-rail input and output
    - Input 100 mV beyond supply rail

- Low noise: 4.5 nV/√Hz at 100 kHz
- Slew rate: 25 V/µs
- Fast settling: 0.3 µs to 0.01%
- Precision:
  - Low offset: 100 µV
  - Low input bias current: 0.2 pA
- 2.2- to 5.5-V operation

For further details, see the OPA365 product page.

2.3 System Design Theory

The following sections present three ways to generate fast transient signals for converter stability tests. These designs provide transient signals with a rise and fall time of less than 1 µs for load steps from 0 to 500 mA with a limited bill of materials.

2.3.1 Open-Loop Load Transient Generator

图 2 and 图 3 are open-loop load transient generators for ground-referenced positive or negative outputs. These generators are mainly composed of the following:

- An NMOS transistor for positive outputs
- A PMOS transistor for negative outputs
- A sense resistor to measure the load current

The transistors Q1 and Q2 are operated in their linear regions as variable resistors. The adjustment of the gate voltage permits to control the value of the resistance between drain and source, thereby setting the load current. A pulse waveform with the right levels must be applied on the IN pin to get the required load step. A pulse signal with a low duty cycle must be used to optimize the power dissipation on the transistor and the sense resistor and to avoid overheating of the board. Because this simple transient generator is always stable, it is recommended to use it for the first stability assessment of a converter when it is unknown if the converter is stable or not.

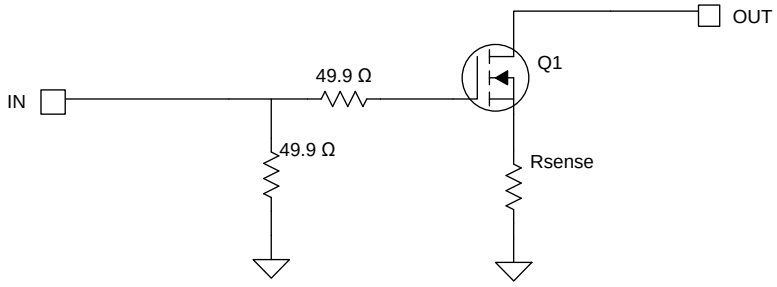


图 2. Open-Loop Load Transient Generator for Positive Outputs

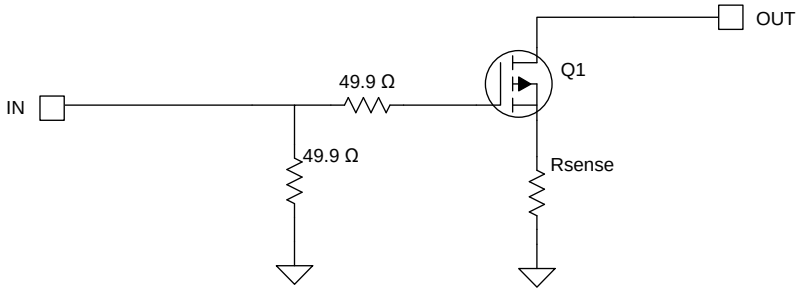


图 3. Open-Loop Load Transient Generator for Negative Outputs

2.3.2 Regulated Load Transient Generator

The circuits presented in 节 2.3.1 are unregulated, and the user needs to estimate and set the gate voltage input that is needed for each required load steps. To avoid this manual tuning, the regulated load transient generator on 图 4 is used. It is composed of mainly the following:

- An NMOS transistor
- An operational amplifier that is driving the gate of the transistor
- A transformer for galvanic isolation
- A sense resistor to measure the load current step

The gate of the transistor is driven by the amplifier and the feedback loop is between the transistor's source and the negative input of the amplifier. The transient load that is applied to the device under test (DUT) is then proportional to the sense resistor value and the amplifier input voltage. In this TI Design, R_{SENSE} = 1 Ω, which means that this design has a 1:1 equivalence between the control input voltage and the load step value.

A 1:1 transformer is added to isolate the input from the signal generator and to give the possibility to apply a transient to ground-referenced DUTs as well as floating DUTs. Adding this transformer creates overshoots and undershoots on the input signal applied to the non-inverting input of the amplifier. These are damped with the addition of a resistor (10 kΩ) across the transformer's secondary, which leads to some power loss.

To avoid that the transformer enters into saturation and a distortion of the input signal, 50% duty cycle pulse signals with symmetrical positive and negative levels must be used as input.

To select the amplifier, consider the following parameters to meet requirements in 表 1:

- Bandwidth f_{3dB} > 0.35/tr, with tr being the rise time of the input signal
- Slew rate that must be high enough to support the maximum rate of change of the amplifier's output
- Supply voltage range that shall permit to reach the expected amplifier's output voltage for the required maximum load
- Amplifier's output load capability

Consider the following parameters when selecting the transformer:

- Input level that must allow to transmit the input signal without distortion
- Frequency range of operation and volt-microsecond rating. There must be enough time between the rising and falling edges of the pulse input signal to see the complete converter response.

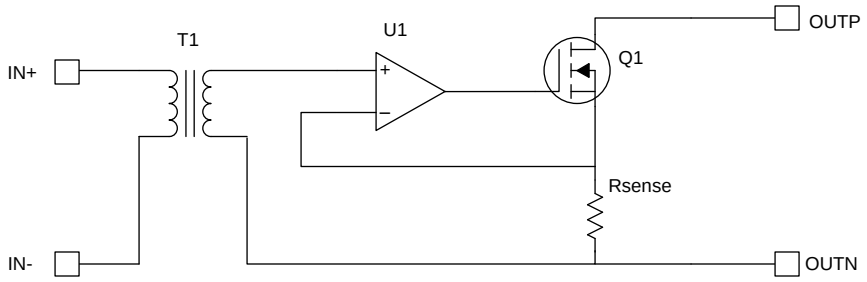


图 4. Closed-Loop Load Transient Generator

3 Hardware, Testing Requirements, and Test Results

3.1 Hardware

The TIDA-01379 design board is composed of three different load transient generators that can be split up and used separately.

3.1.1 Connectors, Jumpers, and Test Points

表 2, 表 3, and 表 4 give an overview of the connector and jumper connections of the evaluation board.

表 2. Connector Overview Circuit 1 (1)

CONNECTOR		SIGNAL	PIN	DESCRIPTION
J1	Positive power supply	VCC+	1, 2	Positive power supply
J2	Ground	GNDB	1, 2	Secondary ground or DUT negative output
J3	Negative power supply	VCC-	1, 2	Negative power supply
J4	DUT output voltage	OUTP	1, 2, 3	DUT positive output
		OUTN	4, 5, 6	DUT negative output
J5	Input	VIN	1, 2	Signal generator input
		GNDA	3, 4	Primary ground
J6	Load transient voltage	V_MEAS	1	Load transient voltage
		GNDB	2	Secondary ground or DUT negative output

(1) Circuit 1 corresponds to the top part of the board with the title "Pos_Neg_Output"

表 3. Connector Overview Circuit 2 (1)

CONNECTOR		SIGNAL	PIN	DESCRIPTION
J7	DUT output voltage	VOUT	1, 2, 3, 4	Negative output
		S-	5	Negative output sense
		GND	6, 7, 8, 9, 10	Ground
J8	DUT output voltage sense	S-	1	Negative output sense
		GND	2	Ground
J9	Gate drive input	VIN	—	Signal generator input
J10	Load transient voltage	V_MEAS	—	Load transient voltage

(1) Circuit 2 corresponds to the middle part of the board with the title "Neg_Output"

表 4. Connector Overview Circuit 3 (1)

CONNECTOR		SIGNAL	PIN	DESCRIPTION
J11	DUT output voltage	VOUT	1, 2, 3, 4	Positive output
		S+	5	Positive output sense
		GND	6, 7, 8, 9, 10	Ground
J12	DUT output voltage sense	S+	1	Positive output sense
		GND	2	Ground
J13	Gate drive input	VIN	—	Signal generator input
J14	Load transient voltage	V_MEAS	—	Load transient voltage

(1) Circuit 3 corresponds to the bottom part of the board with the title "Pos_Output"

3.2 Testing and Results

The three different circuits are used to evaluate the load transient response of the TPS65632 device. The TPS65632 is a triple-output (V_{POS}, V_{NEG}, and AVDD) power supply used to drive AMOLED displays.

3.2.1 Test Setup

To evaluate the different circuits, a signal generator, an oscilloscope, and a power supply are required.

3.2.2 Test Results

3.2.2.1 Positive Output

The circuit in 图 2 is used to evaluate the transient response of the VPOS boost converter. The load is connected between VPOS and GND as shown in 图 5. 图 6 shows that the converter is stable when a 500-mA load step with a rise and fall time of less than 250 ns is applied to it.

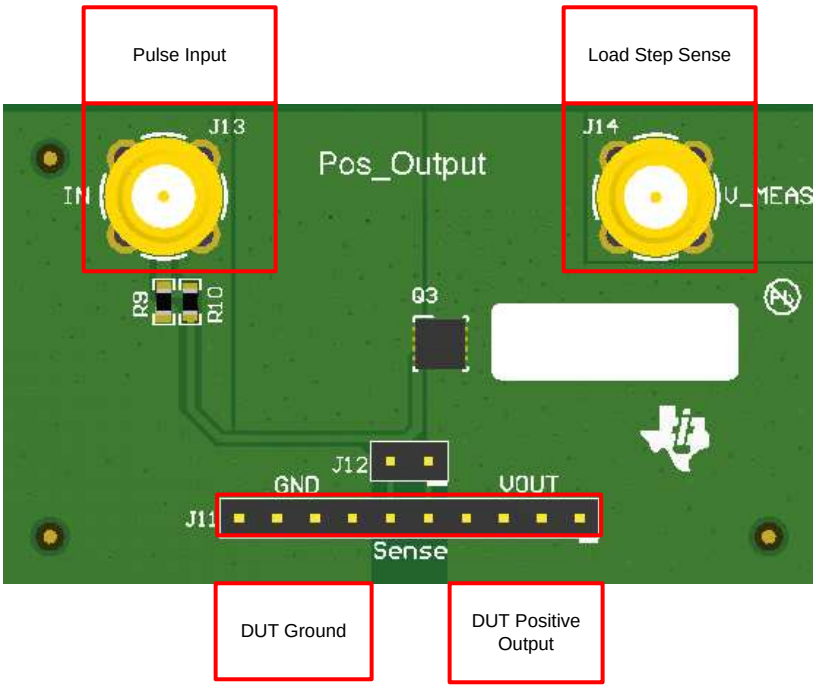


图 5. Board 3 Connection

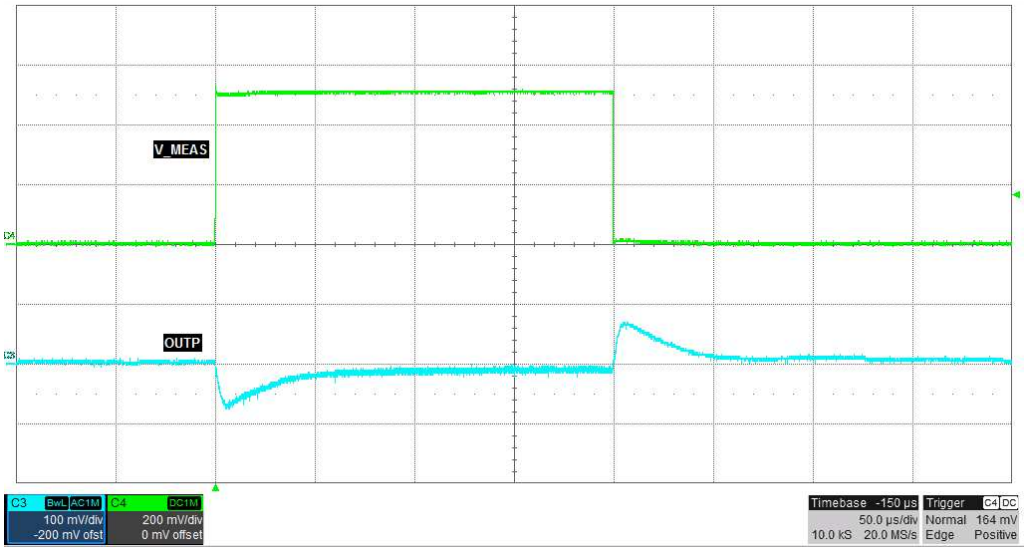


图 6. Transient Response—Load Between VPOS and GND

3.2.2.2 Negative Output

The circuit in 图 3 is used to test the transient response of the VNEG inverting buck-boost converter as shown in 图 7. The load transient signal has an amplitude of 500 mA and a rise and fall time of less than 250 ns.

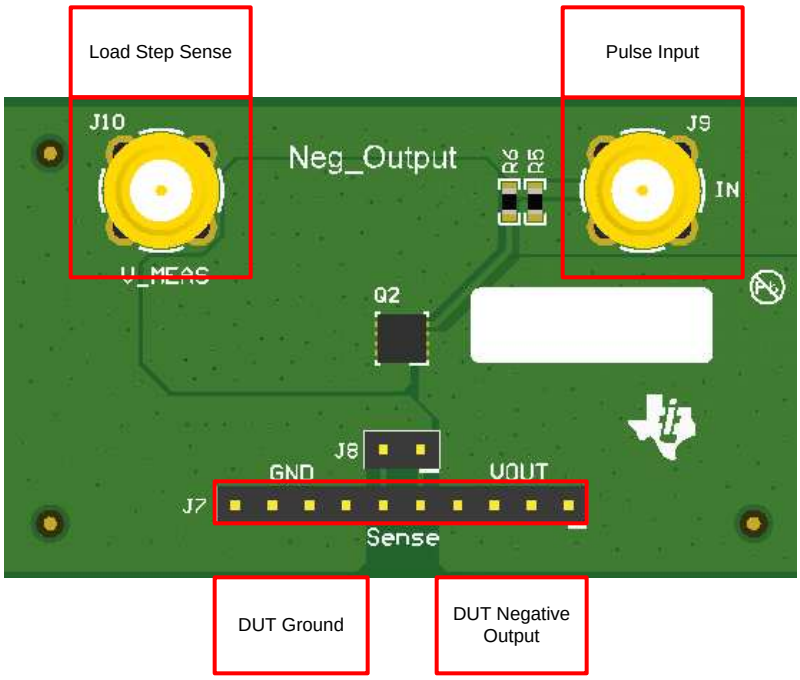


图 7. Board 2 Connection

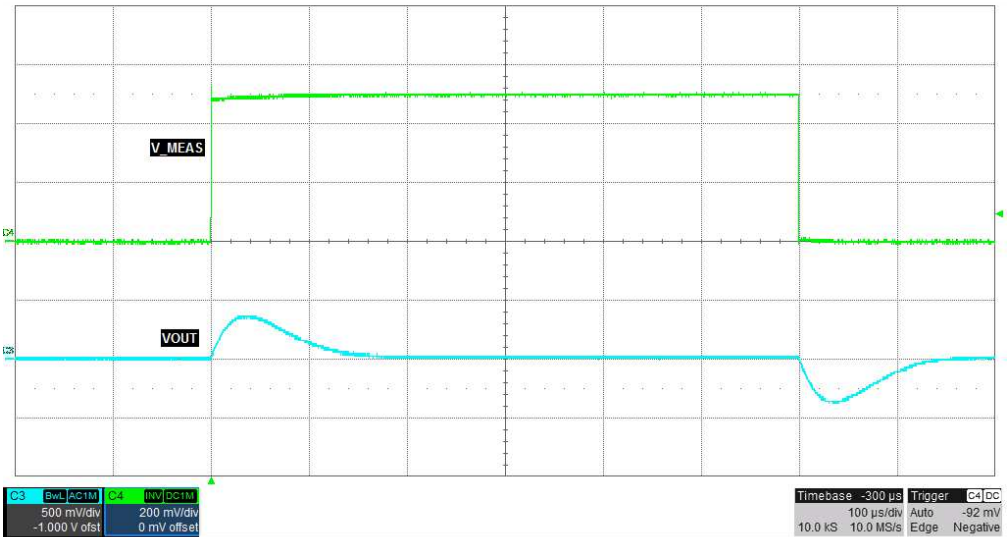


图 8. Transient Response—Load Between VNEG and GND

3.2.2.3 Positive and Negative Outputs

The circuit in 图 4 permits to generate a load transient signal for ground referenced loads as well as floating loads. It is used to test the stability of the TPS65632 converters when a 500-mA load step is applied between VPOS and GND, between VNEG and GND, and between VPOS and VNEG. 图 9 shows how to connect the different loads. 图 10, 图 11, and 图 12 show that the 500-mA load step has different rise and fall times values of 25 ns and 320 ns, respectively.

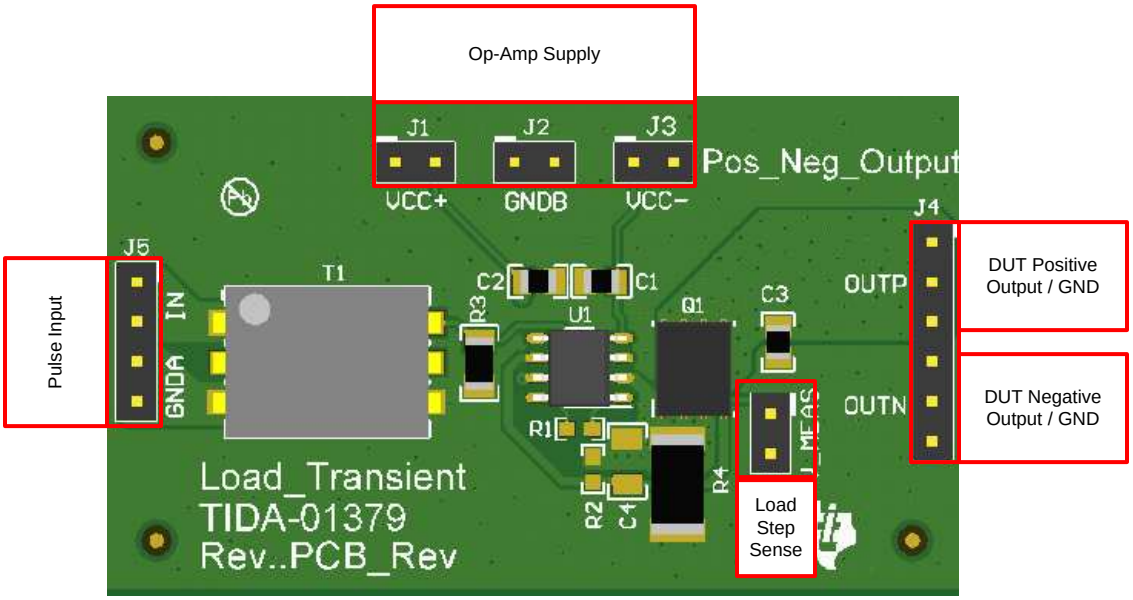


图 9. Board 1 Connection

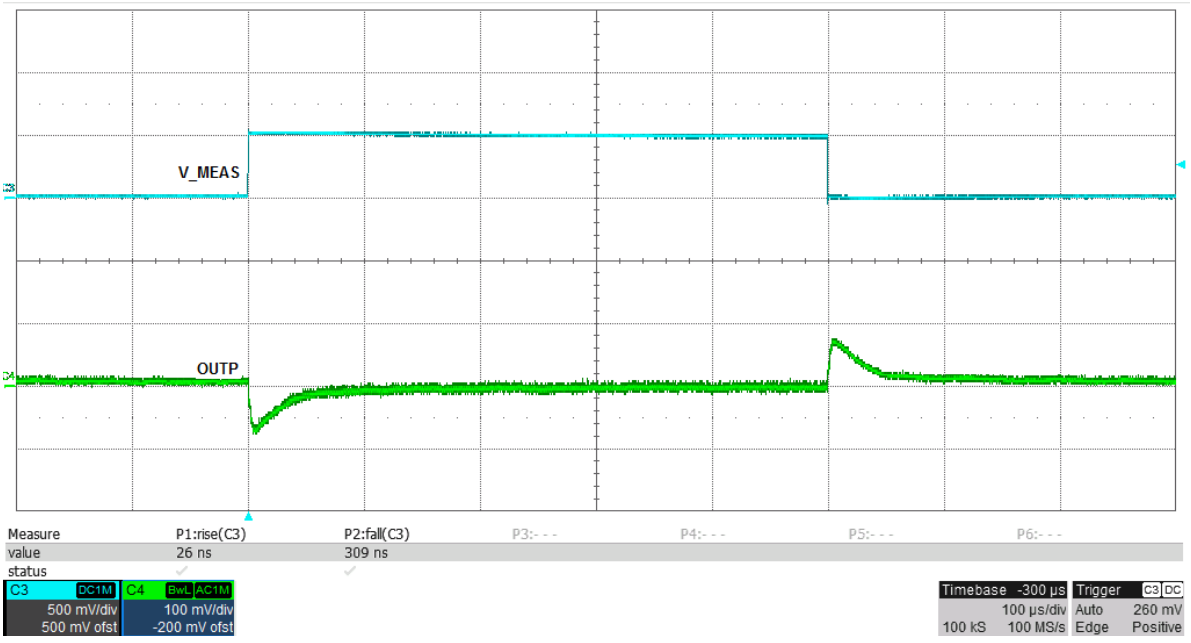


图 10. Transient Response—Load Between VPOS and GND

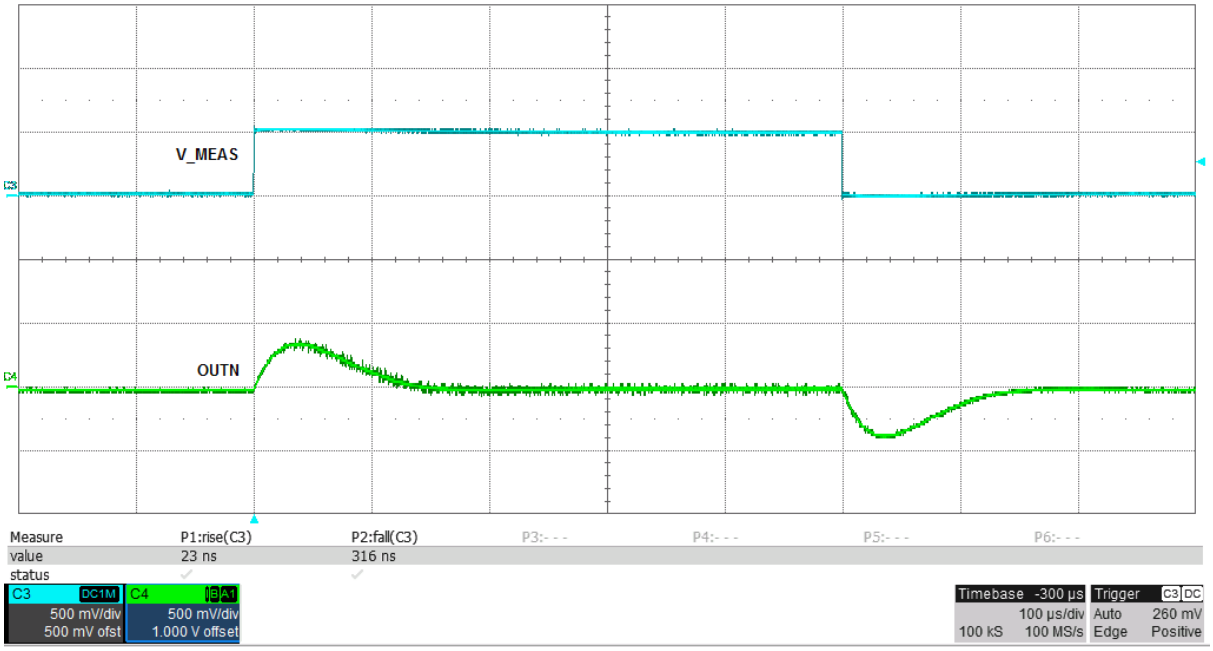


图 11. Transient Response—Load Between VNEG and GND

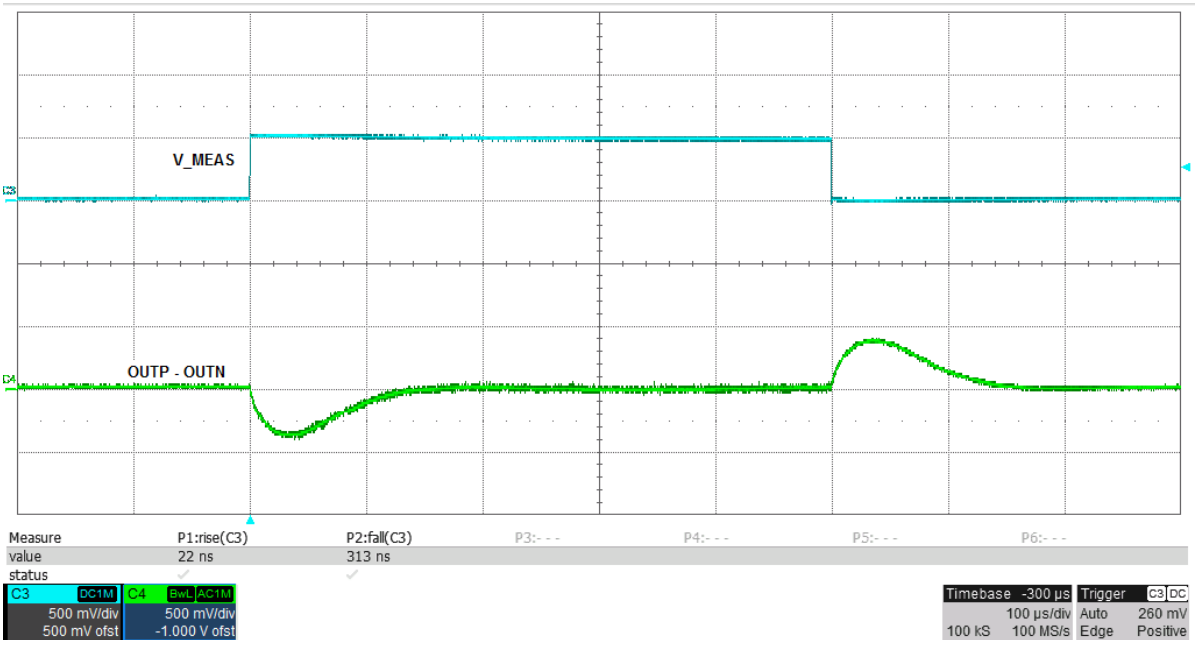


图 12. Transient Response—Load Between VPOS and VNEG

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01379.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01379.

4.3 Layout Prints

To download the layer plots, see the design files at TIDA-01379.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01379.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01379.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01379.

5 Related Documentation

1. Texas Instruments, *TPS65632 Triple-Output AMOLED Display Power Supply*, TPS65632 Datasheet (SLVSCY2)
2. Texas Instruments, *AN-1733 Load Transient Testing Simplified*, SNOA507 Application Report (SNOA507)

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