TI 设计：TIDA-01448

效率高达 93% 且具有成本效益的 5V、1A 单层 TO-247 LDO 替代产品参考设计

说明

此参考设计展示了一款具有小解决方案尺寸、高效率和低 EMI 的直流/直流模块，可用于替代主要家电中的 LDO。使用直流/直流模块替代 LDO 可以显著提高系统效率，不仅能减小解决方案尺寸并节省 BOM 成本，而且还无需使用散热器。此模块占用空间与 TO-247 封装相同，并且与 TO-220 LDO 引脚到引脚兼容，便于快速评估和缩短产品上市时间。TPS561201 电源转换器可在满载、低负载和待机状态下实现更高的输出电流并降低功耗。

此模块大小与 TO-247 封装相同，引脚与 TO-220 LDO 兼容，便于快速评估和缩短产品上市时间。

资源

TIDA-01448	设计文件夹
TPS561201	产品文件夹

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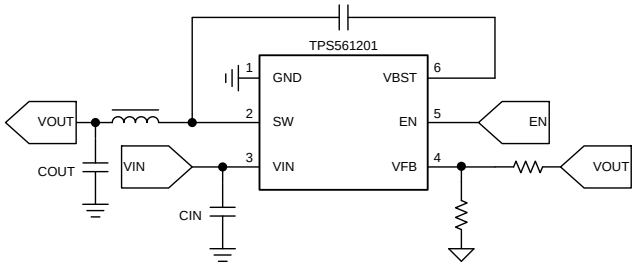
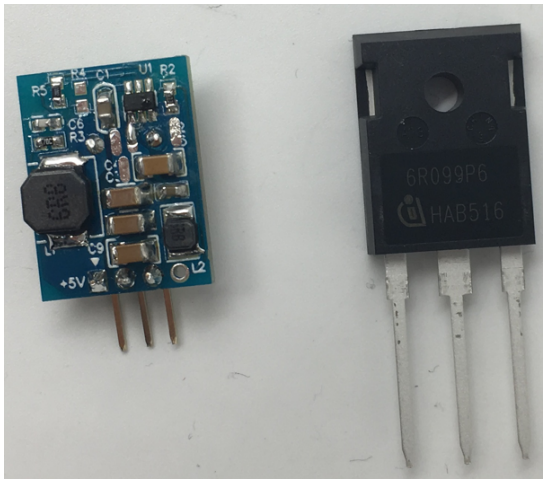
特性

- 5V 稳压，高达 1A 的输出负载
- 效率达 93%
- 1.3μA 待机电流和 472μA 无负载电流
- 外形小巧：引脚与 TO-220 兼容，大小与 TO-247 相当 (15mm × 20mm)
- 满负载时温度上升不足 35°C，无需散热器
- 降低了板载直流/直流设计的复杂性，节省了开关电源 EMC 设计的研发时间和投入（上市更快）

应用

- 洗衣机和烘干机
- 冰箱和冷冻柜
- 洗碗机
- 空调室内机





1 System Description

Traditionally, low dropout regulators (LDO) are used in home appliances to generate 5 V or 3.3 V from the 12-V rail. These LDOs are chosen mainly for their cost and size.

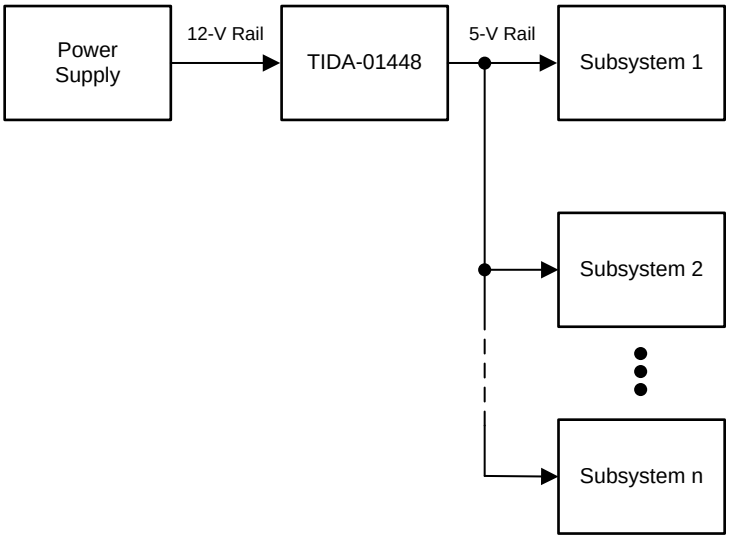


图 **1. System Diagram**

With the tightening requirements on active and standby power consumption and the increasing current needs due to the addition of new features (for example, the Wi-Fi® module), the LDOs become an obstacle to achieving stringent energy ratings.

The TIDA-01448 is developed to answer this need of higher efficiency and current capability with the additional benefit of saving space by eliminating the heat sink, which is normally used to allow the LDOs to dissipate the losses.

1.1 Key System Specifications

The specifications of the TIDA-01448 design are listed in 表 1:

表 **1. Key System Specifications**

PARAMETER	SPECIFICATIONS	DETAILS
Input voltage range	6.5 to 17 V	—
Output voltage and max current	5 V at 1 A	—
Efficiency (full load, rated load, and light load)	91.5%: 12 V → 5 V at 1 A; 82%: 12 V → 5 V at 10 mA	节 3.2.2.1
EMI performance	EN55022 class A, >4-dB margin	节 3.2.2.10
Regulation (line and load)	±3% across the input range and load current range	节 3.2.2.3
Transient response	±3% from 0.1 to 1.0 A	节 3.2.2.5
Protections	Short-circuit, hiccup mode OCP for both FETs, OTP, OVP	节 3.2.2.7
Operating ambient temperature	–30°C to 85°C	节 3.2.2.2

2 System Overview

2.1 Block Diagram

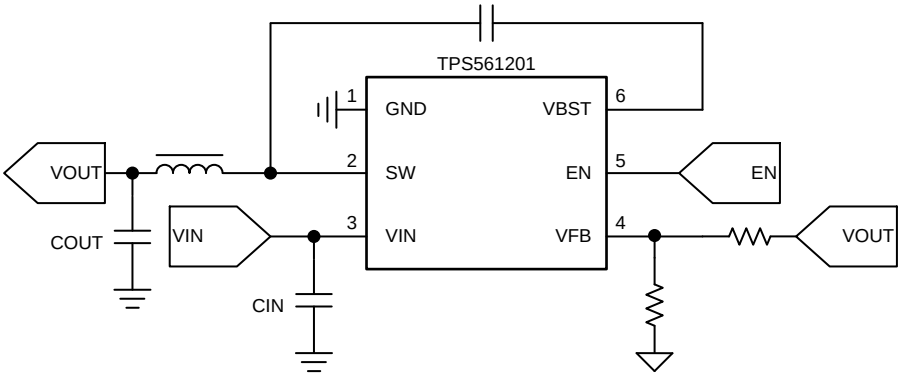


图 **2. Block Diagram**

2.2 Highlighted Products

2.2.1 TPS561201

The TPS561201 is a simple, easy-to-use, 1-A synchronous step-down converters in a SOT-23 package. The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP2™ mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

The TPS561201 operates in pulse skip mode, which maintains high efficiency during light load operation. The TPS561201 is available in a 6-pin 1.6×2.9-mm SOT (DDC) package and specified from –40°C to 125°C of junction temperature.

Features:

- 1-A converter integrated 140-mΩ and 84-mΩ FETs
- D-CAP2 mode control with fast transient response
- Input voltage range: 4.5 to 17 V
- Output voltage range: 0.76 to 7 V
- Pulse-skip mode
- 580-kHz switching frequency
- Low shutdown current less than 10 µA
- 2% feedback voltage accuracy (25°C)
- Startup from pre-biased output voltage
- Cycle-by-cycle overcurrent limit
- Hiccup-mode overcurrent protection
- Non-latch UVP and TSD protections

- Fixed soft-start: 1.0 ms

2.3 System Design Theory

LDOs are devices that regulate the output voltage while the output current is the same as the input current. This implies losses are proportional to the dropout between input and output voltage and the output current, as shown in 公式 1. These losses are the root cause of poor efficiency in LDOs. This translates to a limitation of the ratio between input and output voltage and maximum output current as well as the need of a heat sink. That heat sink adds cost and size to the overall solution.

A DC/DC switch mode power supply, including a Buck topology as in this project, present the advantage of having a higher efficiency, allowing them to be used in a wider variety of applications as well as being competitive with an LDO-based design with respect to cost and size (including all components and heat sink). Find more details on how a Buck topology works in the application report *Understanding Buck Power Stages In Switchmode Power Supplies* (SLVA057).

Compare the efficiency of the TIDA-01448 and an LDO-based design. The efficiency data for the TIDA-01448 design can be found in 节 3.2.2.1. In an LDO, the power to be dissipated can be estimated by 公式 1.

$$P_{DISSIPATED} = \left(V_{IN} - V_{OUT}\right) \times I_{OUT} \quad (1)$$

Now calculate the power dissipated by a 12-V input, 5-V output design at 1 A, 500 mA, and 100 mA to see what the performances are for the TIDA-01448 and for the LDO-based design.

For 1 A, the efficiency of the TIDA-01448 is 91.5% (8.5% loss). With 5 W at the output, 0.425 W are dissipated. For the LDO-based design, 公式 1 gives 7 W to be dissipated by the LDO.

For 500 mA, the efficiency of the TIDA-01448 is 90% (10% loss). With 2.5 W at the output, 0.25 W are dissipated. This is to be compared with 3.5 W for the LDO.

Finally for 100 mA, 0.055 W needs to be dissipated for the TIDA-01448 (86% efficiency) versus 0.7 W for the LDO-based design.

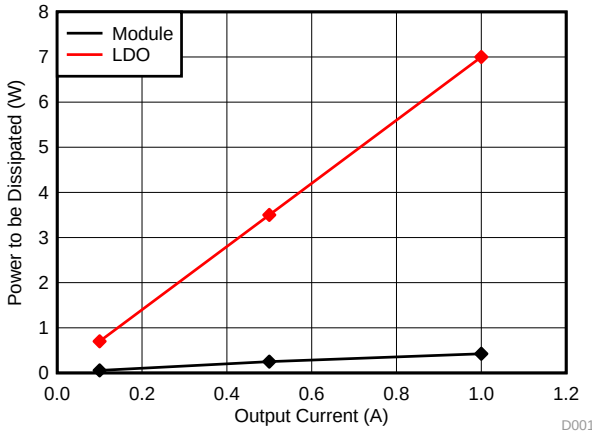


图 3. Comparison of Power Dissipated

As shown in 图 3, the LDO-based design needs to dissipate much more power than the TIDA-01448 design, which impacts both power consumption and cost and size due to the necessity of a heat sink.

2.4 Design Considerations

2.4.1 Part and Topology Selection

The first step of the design is to select the circuit topology. As cost and space are key in home appliance design and no isolation is needed for the 12-V to 5-V conversion, a Buck topology is chosen. Still, with the aim to reduce bill of material cost and size, a synchronous converter with integrated FET is preferred.

With this in mind, as well as the specification in 1.1 节, the TPS561201 is chosen. The converter includes two integrated switching FETs, internal loop compensation, and a 1-ms internal soft start to reduce component count. It integrates a 140-mΩ and a 84-mΩ MOSFET for up to 1-A continuous output current.

2.4.2 Design Steps and Passive Components Selection

The first step is to set the output voltage, which is adjusted by the resistor divider (R3 and R5). Set the range of the resistors; higher values decrease the losses in the resistor divider but make the feedback signal more sensitive to noise, while lower values will make the feedback signal more robust against noise but increase losses. On this project, a good trade-off is setting R5 at 10 kΩ and use 公式 2 to calculate R3.

$$R_3 = \left(\frac{V_{OUT}}{0.768} - 1 \right) \times R_5 \tag{2}$$

where:

- R5 = 10 kΩ
- V_{OUT} = 5 V

公式 2 gives R3 = 55.1 kΩ. A resistor value of 56.2 kΩ is then used for R3. By reversing 公式 2, an effective output voltage of V_{OUT} = 5.084 V is given.

Then comes the choice of the output filter, including the output inductor (L1) and output capacitors (C3 and C4).

The LC filter used as the output filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \tag{3}$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low-frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. D-CAP2 introduces a high frequency zero that reduces the gain roll off to –20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of 公式 3 is located below the high frequency zero but close enough that the phase boost provided be the high-frequency zero provides adequate phase margin for a stable circuit.

The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using 公式 4, 公式 5, and 公式 6. The inductor saturation current rating must be greater than the calculated peak current, and the RMS or heating current rating must be greater than the calculated RMS current. Use 580 kHz for f_{SW}. Make sure the chosen inductor is rated for the peak current of 公式 5 and the RMS current of 公式 6.

$$II_{p-p} = \frac{V_{OUT}}{V_{IN(MAX)}} \times \frac{V_{IN(MAX)} - V_{OUT}}{L_O \times f_{SW}} \tag{4}$$

$$I_{peak} = I_O + \frac{I_{p-p}}{2} \quad (5)$$

$$I_{LO(RMS)} = \sqrt{I_o^2 + \frac{1}{12} I_{p-p}^2} \quad (6)$$

For this TI Design, the inductor used is a Coilank ABG06A28M6R8 (6.8 µH) with a peak current rating of 2.94 A and an RMS current rating of 2.47 A.

An inductor between 3.3 and 4.7 µH is recommended, but during testing, a 6.8 µH show improved performance increasing the stability of the whole system. At the same time, C6 (100 pF) is also added to increase the transient response.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS561201 is intended for use with ceramic or other low-ESR capacitors. Recommended values range from 20 to 68 µF. Use 公式 7 to determine the required RMS current rating for the output capacitor.

$$I_{CO(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_o \times f_{SW}} \quad (7)$$

For this design, two MURATA 22-µF output capacitors are used.

The next step is to set the input capacitor. The TPS561201 requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from pin 3 to ground is optional to provide additional high-frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage.

For bootstrap capacitor selection, a 0.1-µF ceramic capacitor must be connected between the VBST to SW pin for proper operation. TI recommends to use a ceramic capacitor.

The last step is to select the input filter. Considering the rated input RMS current, this TI Design uses the ABG03A15M6R8 (6.8 µH) with a peak current rating of 0.88 A and an RMS current rating of 0.88 A as the input inductor and use the C3216X5R1E226M160AB (22 µF) as the input capacitor.

3 Hardware, Testing Requirements, and Test Results

3.1 Required Hardware

3.1.1 PCB Overview

A picture of the PCB with the functional blocks is shown in 图 4.

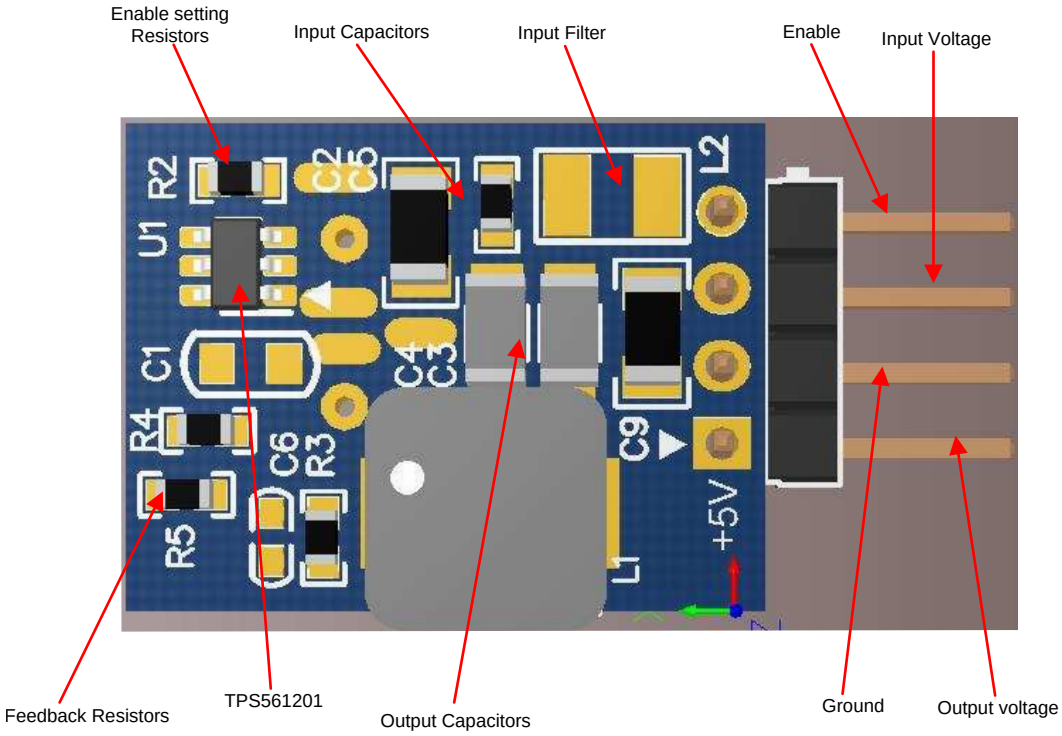


图 4. TIDA-01448 PCB With Functional Blocks

3.1.2 Connectors Settings

表 2. Connector Settings

CONNECTOR	FUNCTION
J1-1	EN
J1-2	V_{IN}
J1-3	GND
J1-4	V_{OUT}

3.2 Testing and Results

3.2.1 Test Setup

图 5 shows the setup and the test equipment used.

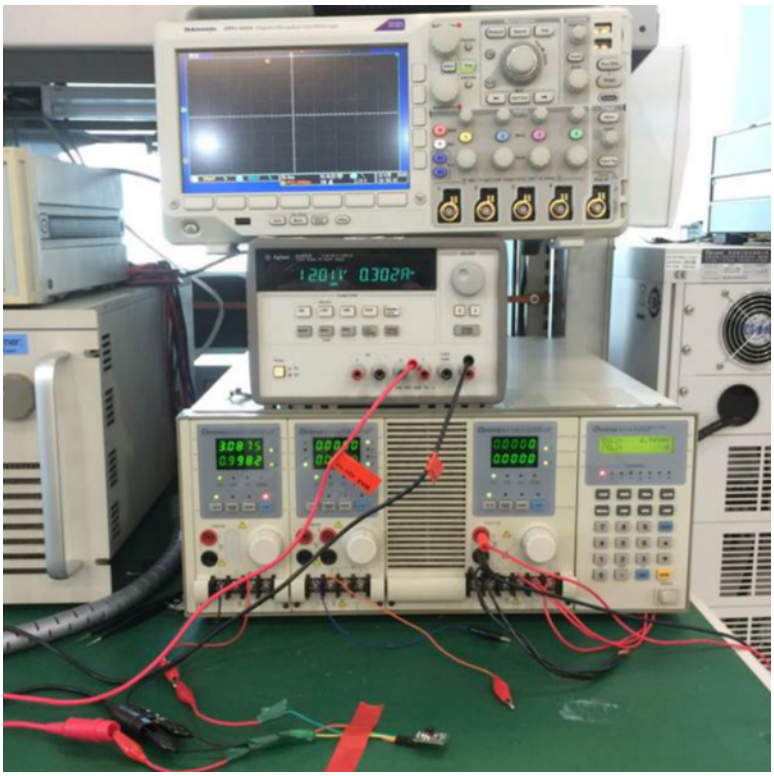


图 5. Picture of Test Setup for TIDA-01448

表 3 lists the test equipment used to test the TIDA-01448.

表 3. Test Equipment

TEST EQUIPMENT	PART NUMBER
Oscilloscope	Tektronix DPO 3054
Voltage probe	Tektronix P6139A
Current probe	Tektronix TCP202
Multimeter	Fluke 287C
Power supply	Agilent E3631A
Electronic load	Chroma 63103 and 63102
Thermal camera	Fluke TI110

3.2.2 Test Results

3.2.2.1 Efficiency

To test the efficiency, four multimeters are used: two are set up as voltmeters to measure the input and output voltages, and two are set up as ammeters to measure the input and output currents.

The measurements are done at a temperature of 28.1ºC and with the enable setting resistors (R2 and R4) not populate, with a 6-V apply to the Enable pin.

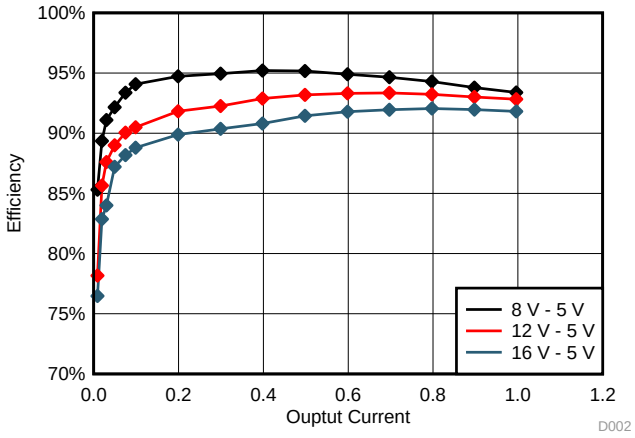


图 **6. TIDA-01448 Efficiency**

表 4, 表 5, and 表 6 list the details of the efficiency curves shown in 图 6.

表 **4. Efficiency With 8-V Input**

V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT} (mA)	η
7.930	0.6593	4.9010	0.9962	0.933845385
7.940	0.5914	4.9070	0.8975	0.937883062
7.940	0.5232	4.9130	0.7973	0.942931818
7.950	0.4556	4.9180	0.6971	0.946526469
7.960	0.3900	4.9230	0.5984	0.948950908
7.960	0.3241	4.9280	0.4982	0.951661113
7.970	0.2588	4.9340	0.3980	0.952049707
7.980	0.1950	4.9380	0.2992	0.949456719
7.980	0.1363	5.1775	0.1990	0.947271425
7.990	0.0681	5.1860	0.0987	0.940710029
7.990	0.0519	5.1760	0.0748	0.933644898
7.990	0.0346	5.1680	0.0493	0.921608658
7.990	0.0212	5.1605	0.0299	0.910920195
7.995	0.0140	5.1555	0.0194	0.893564728
7.995	0.0068	5.1530	0.0090	0.853051540

表 5. Efficiency With 12-V Input

V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT} (mA)	η
11.950	0.4453	4.958	0.9963	0.928273713
11.960	0.4005	4.964	0.8975	0.930106180
11.960	0.3553	4.969	0.7973	0.932318654
11.965	0.3105	4.975	0.6971	0.933499007
11.970	0.2668	4.980	0.5984	0.933127421
11.970	0.2227	4.986	0.4982	0.931840603
11.980	0.1782	4.982	0.3980	0.928800151
11.980	0.1415	5.227	0.2992	0.922573193
11.985	0.0945	5.226	0.1990	0.918232447
11.990	0.0472	5.189	0.0987	0.904981376
11.990	0.0359	5.182	0.0748	0.900503437
11.990	0.0239	5.173	0.0493	0.889963742
11.990	0.0147	5.164	0.0299	0.876033883
11.990	0.0098	5.161	0.0195	0.856491804
11.990	0.0049	5.160	0.0089	0.781671801

表 6. Efficiency With 16-V Input

V_{IN} (V)	I_{IN} (mA)	V_{OUT} (V)	I_{OUT} (mA)	η
15.97	0.3388	4.986	0.9963	0.918108666
15.97	0.3051	4.992	0.8976	0.919624000
15.97	0.2711	4.998	0.7974	0.920530218
15.98	0.2374	5.004	0.6971	0.919506692
15.98	0.2044	5.010	0.5984	0.917849856
15.98	0.1707	5.007	0.4982	0.914473276
15.98	0.1437	5.239	0.3980	0.908025254
15.98	0.1087	5.246	0.2992	0.903615260
15.99	0.0724	5.229	0.1990	0.898844754
15.99	0.0361	5.193	0.0987	0.887932208
15.99	0.0275	5.184	0.0748	0.881831144
15.99	0.0183	5.176	0.0493	0.872050496
15.99	0.0115	5.166	0.0299	0.840000000
15.99	0.0076	5.164	0.0195	0.828626444
15.99	0.0038	5.163	0.0090	0.764737830

3.2.2.2 Thermal

The thermal picture in 图 7 was taken at a room temperature of 28.1°C, with a 12-V input, 5 V at 1-A output without airflow.

The hottest point of the design is the TPS561201 at 61.6°C. This is an increase of 33.5°C. Because the acceptable ambient temperature range is –30°C to 85°C, no heat sink is required for the TIDA-01448 to function properly.

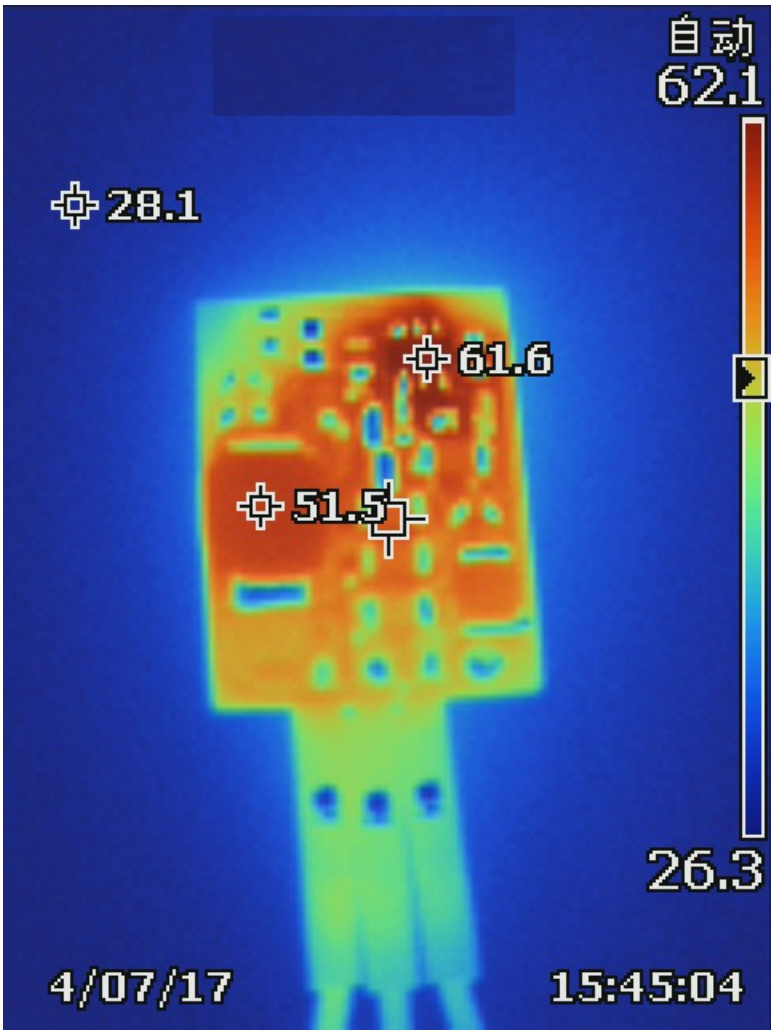


图 7. Top-Side Thermal Picture With 12-V_{IN}, 5 V at 1-A Output

3.2.2.3 Line and Load Regulation

图 8, 图 9, and 图 10 show the output voltage variation, depending on load current, input voltage, and temperature. Across all input voltages and output currents, the output voltage varies between 5.25 and 4.9 V.

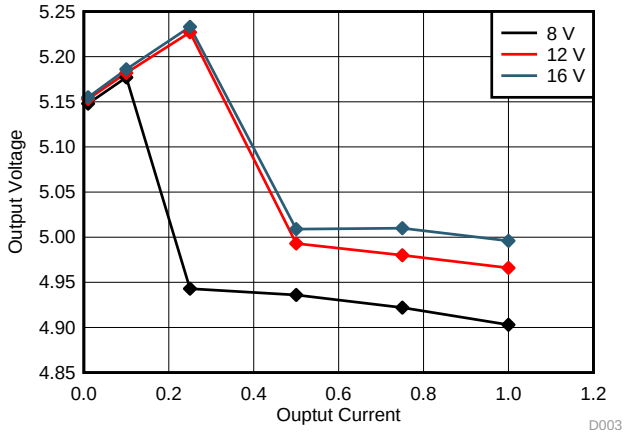


图 8. Line and Load Regulation at 85°C

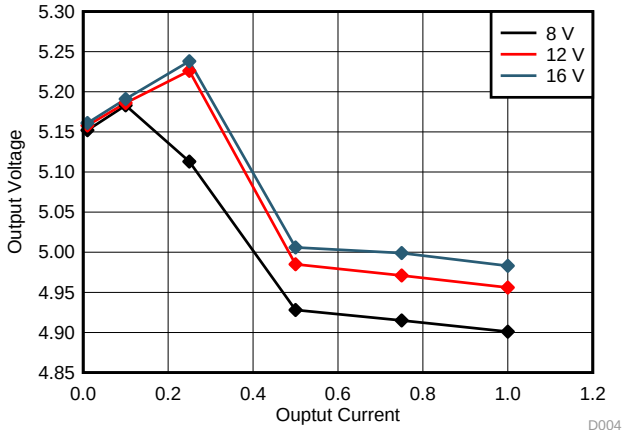


图 9. Line and Load Regulation at 23°C

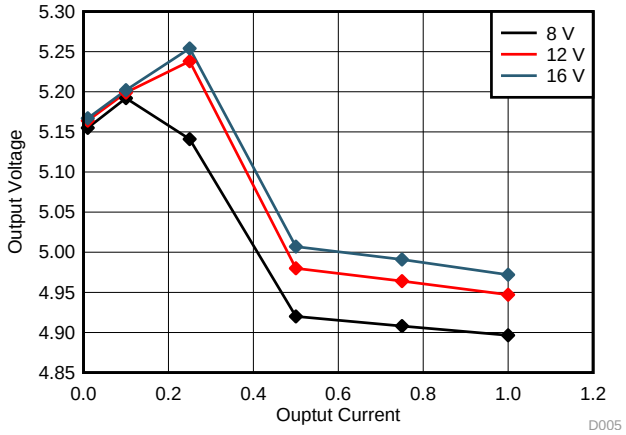


图 10. Line and Load Regulation at –30°C

表 7, 表 8, and 表 9 list the details of the regulation curves shown in 图 8 and 图 10.

表 7. Line and Load Regulation at 85°C

V_{IN}	V_{OUT}	I_{OUT}
16	4.996	1.00
16	5.010	0.75
16	5.009	0.50
16	5.233	0.25
16	5.186	0.10
16	5.155	0.01
12	4.966	1.00
12	4.980	0.75
12	4.993	0.50
12	5.227	0.25
12	5.182	0.10
12	5.153	0.01
8	4.903	1.00
8	4.922	0.75
8	4.936	0.50
8	4.943	0.25
8	5.177	0.10
8	5.148	0.01

表 8. Line and Load Regulation at 23°C

V_{IN}	V_{OUT}	I_{OUT}
16	4.983	1.00
16	4.999	0.75
16	5.006	0.50
16	5.238	0.25
16	5.191	0.10
16	5.161	0.01
12	4.956	1.00
12	4.971	0.75
12	4.985	0.50
12	5.226	0.25
12	5.186	0.10
12	5.158	0.01
8	4.901	1.00
8	4.915	0.75
8	4.928	0.50
8	5.113	0.25
8	5.183	0.10
8	5.152	0.01

表 9. Line and Load Regulation at –30°C

V_{IN}	V_{OUT}	I_{OUT}
16	4.9720	1.00
16	4.9910	0.75
16	5.0070	0.50
16	5.2540	0.25
16	5.2020	0.10
16	5.1670	0.01
12	4.9470	1.00
12	4.9640	0.75
12	4.9800	0.50
12	5.2380	0.25
12	5.1990	0.10
12	5.1640	0.01
8	4.8965	1.00
8	4.9080	0.75
8	4.9200	0.50
8	5.1410	0.25
8	5.1920	0.10
8	5.1550	0.01

3.2.2.4 Output Voltage Ripple

The output voltage ripple remains below 30 mVpp under full load (1 A), low load (10 mA), or no load. This ripple is well below the initial requirements of ±1%.

Measurements are done at 28.1ºC room temperature with a 12-V input voltage. The upper curve (1) is the output voltage with an oscilloscope in AC-coupling mode with 20 mV/div. The lower curve (2) is the switch node (pin 2 of the TPS561201) with 5 V/div.

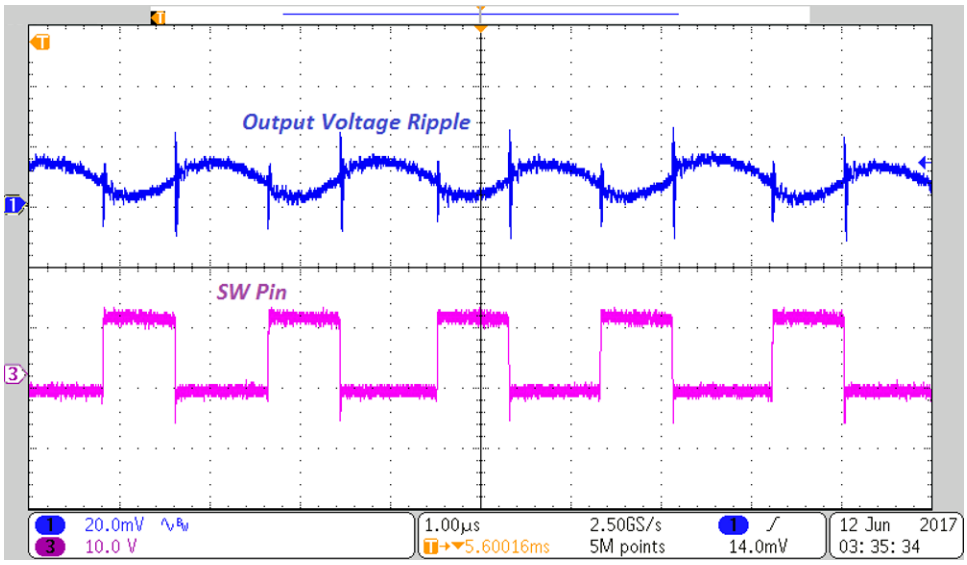


图 **11. Output Voltage Ripple at 1-A Output Load**

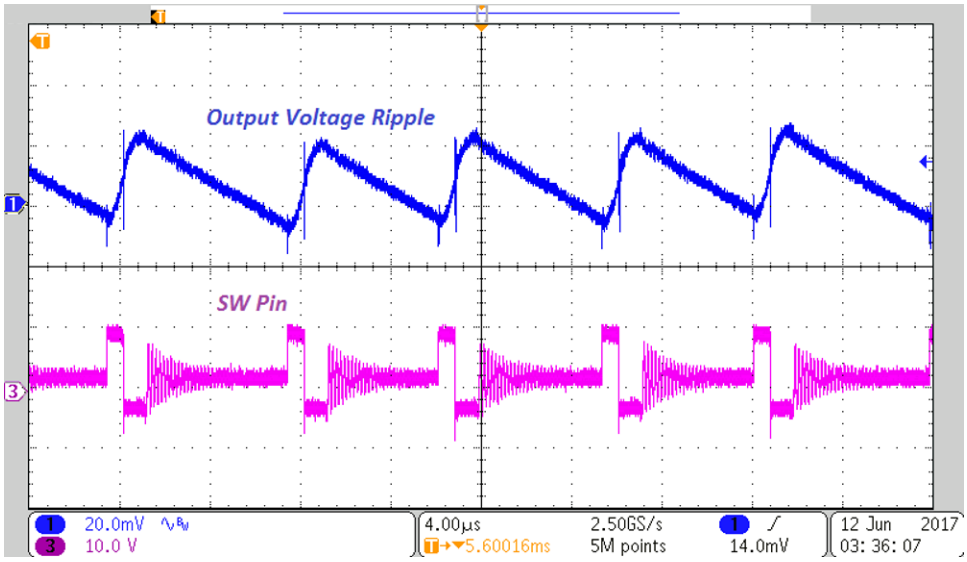


图 **12. Output Voltage Ripple at 10-mA Output Load**

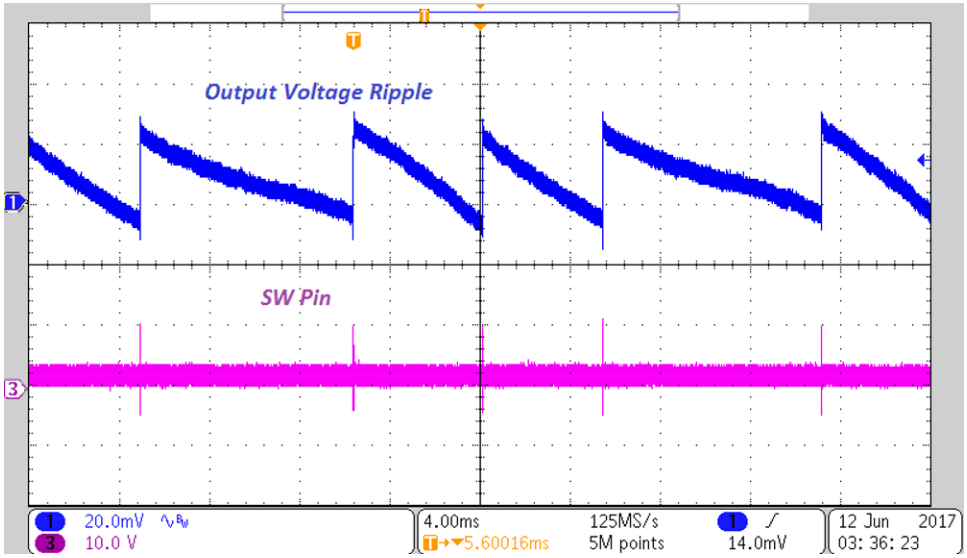


图 **13. Output Voltage Ripple at No Load Output**

3.2.2.5 Transient Response

The transient response is below ±10 mV for load steps between 10 mA and 1 A, which are the design requirements (±3%).

Measurements are done at 28.1°C room temperature with a 12-V input voltage. The upper curve (1) is the output voltage with an oscilloscope in AC-coupling mode with 10 mV/div. The lower curve (4) is the output current with 1 A/div. The load step is applied with a 1-A/ms slew rate.

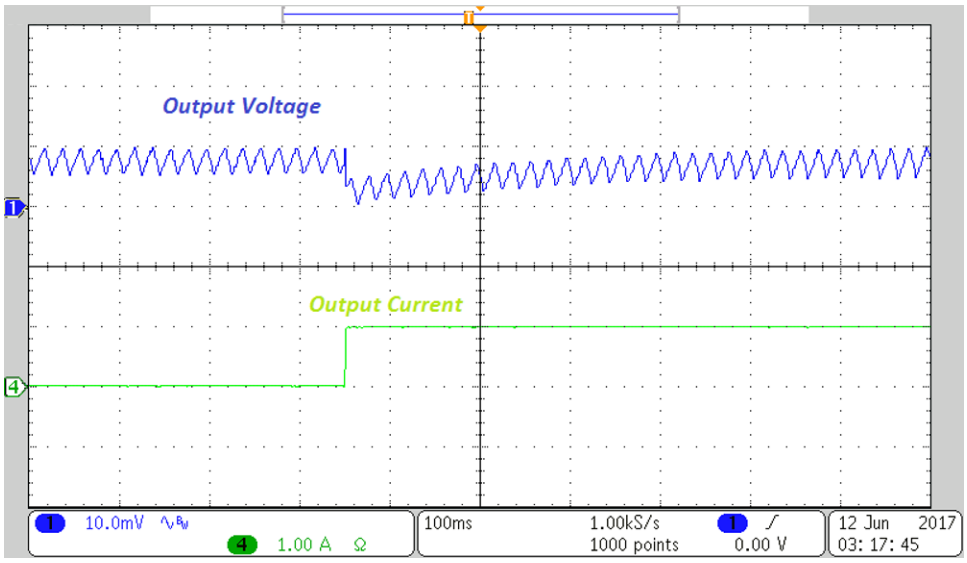


图 14. Transient Response From 10-mA to 1-A Output Load

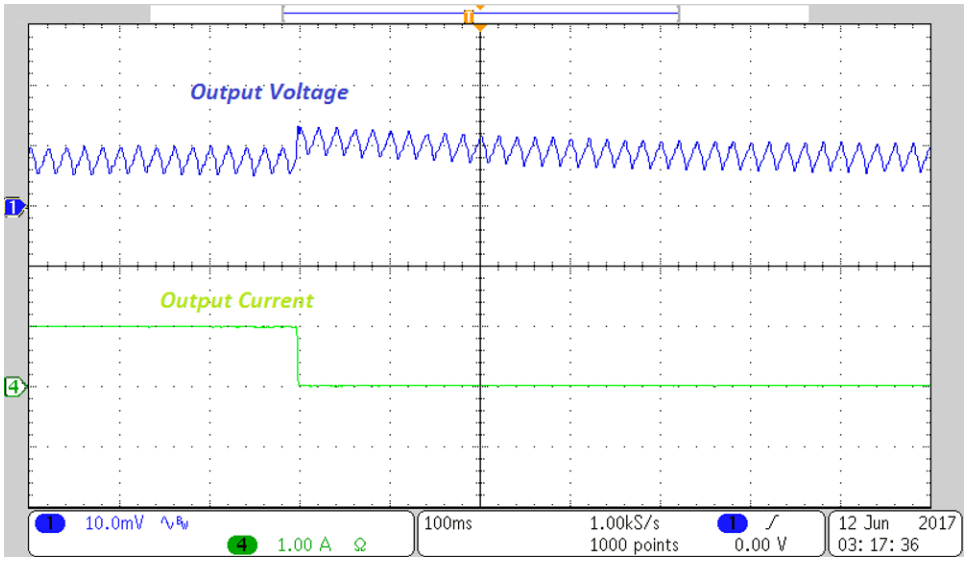


图 15. Transient Response From 1-A to 10-mA Output Load

3.2.2.6 Start-up and Shutdown

For the start-up and the shutdown behavior, 12 V is applied at the input with a 1-A load at the output.

Measurements are done at 28.1ºC room temperature. The upper curve (3) is the EN pin with an oscilloscope in DC-coupling mode with 2 V/div. The lower curve (2) is the switch node pin signal with an oscilloscope in DC-coupling mode with 10 V/div. The upper curve (1) is the output voltage with an oscilloscope in DC-coupling mode with 5 V/div. The lower curve (4) is the output current with 1 A/div.

The TIDA-01448 design takes 1.7 ms to provide 5 V. The output voltage is reached without overshoot.

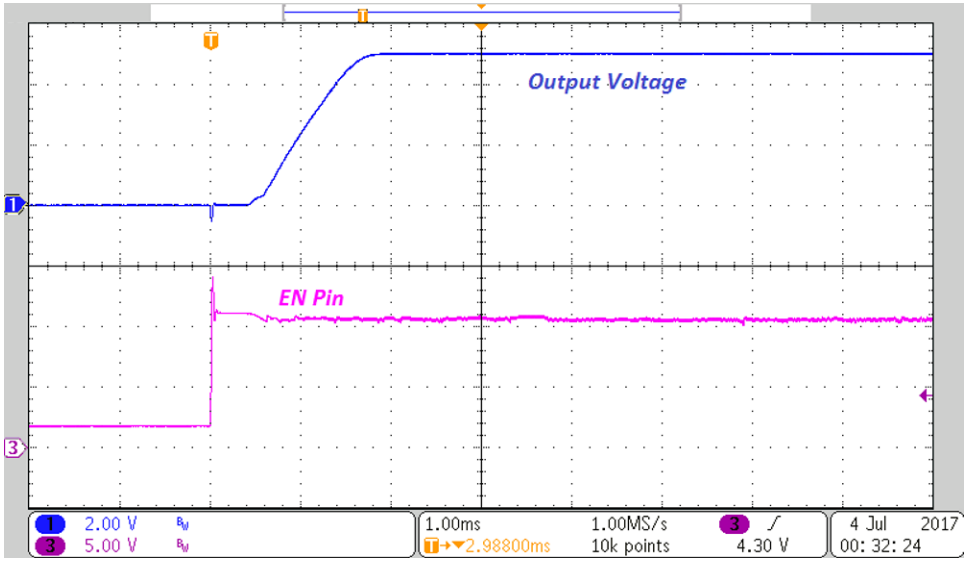


图 **16. Start-up at 12-V Input and 1-A Output Load**

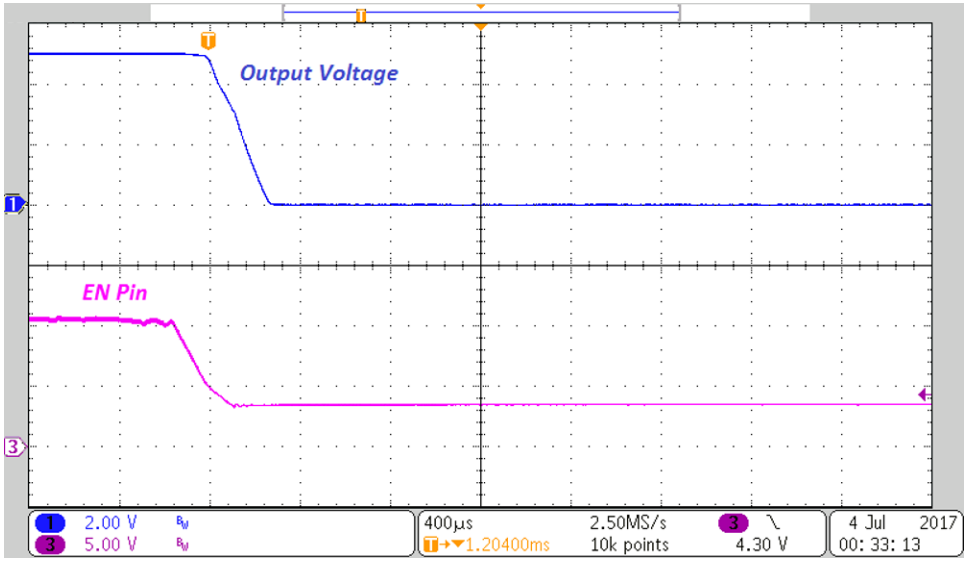


图 **17. Shutdown at 12-V Input and 1-A Output Load**

3.2.2.7 Overcurrent and Short-Circuit Test

The overcurrent protection is tested by having a transient load from a 1- to 3-A output current while the board is supplied with 12 V. The short-circuit protection is tested by shorting the output pin to ground.

The upper curve (1) is the output voltage with an oscilloscope in DC-coupling mode with 2 V/div (图 18) and 1 V/div (图 19). The lower curve (4) is the output current with 2 A/div.

As shown in 图 18 and 图 19, when the current is rising to the current limit level, the device enters overcurrent protection as described in the TPS561201 datasheet (SLVSC95). After waiting the pre-programmed time, the device tries to restart. Once the fault condition is removed, the device starts normally.

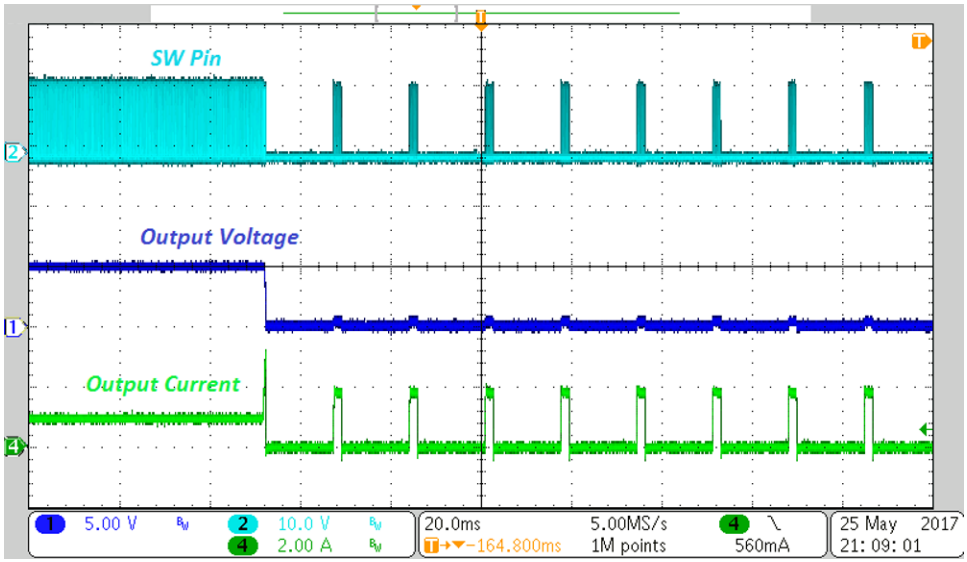


图 **18. Overcurrent Protection**

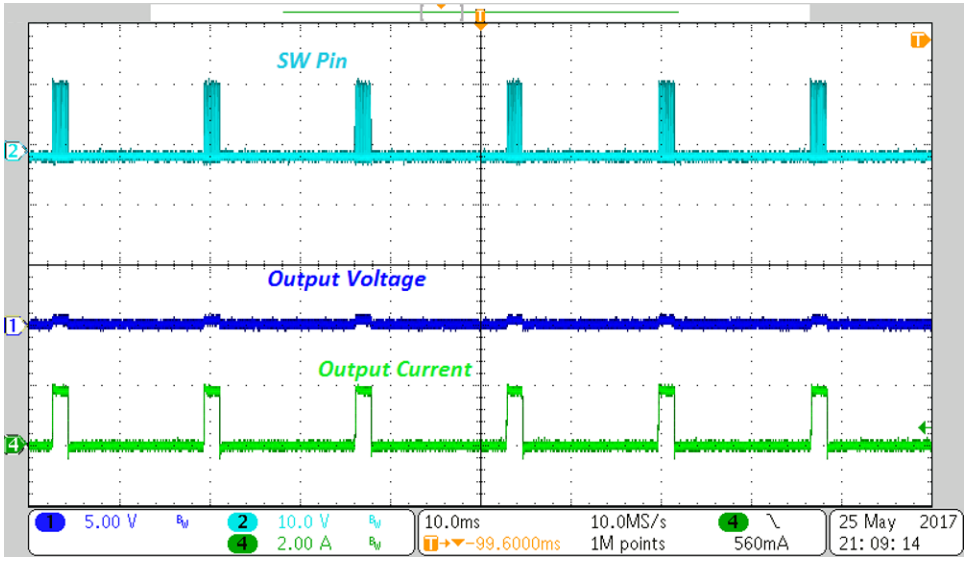


图 **19. Short-Circuit Protection**

3.2.2.8 Overvoltage Test

The overvoltage protection is tested by applying 6 V at the output of the TIDA-01448 board while the board is supplied with 12 V and with a 1-A output load.

The upper curve (1) is the output voltage with an oscilloscope in DC-coupling mode with 2 V/div. The lower curve (2) is voltage at the switch node with 5 V/div.

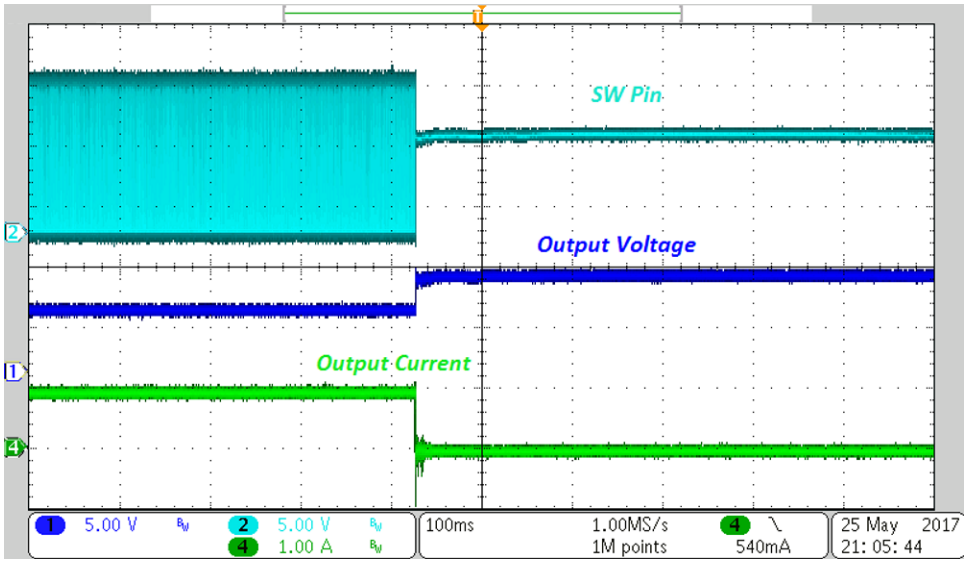


图 **20. Overvoltage Protection From 5 to 6 V**

3.2.2.9 Standby and No-Load Currents

The standby current is measured with an ammeter at 26°C room temperature with a 12-V input voltage. The enable pin was set low through the connector, and the enable setting resistors (R2 and R4) not populated. The standby current was measured at 1.3 μA.

The no-load current was measured with an ammeter at 26°C room temperature with a 12-V input voltage, with the enable setting resistors (R2 and R4) populated and no load attached at the output. The no-load current was measured at 472 μA.

3.2.2.10 EMC Tests

The TIDA-01448 TI Design has been tested for EMI according to EN55022 Class A conducted emissions. The EMC tests were performed by the Shanghai Institute of Measurement and Testing Technology Fundamental Performance Test Centre (China).

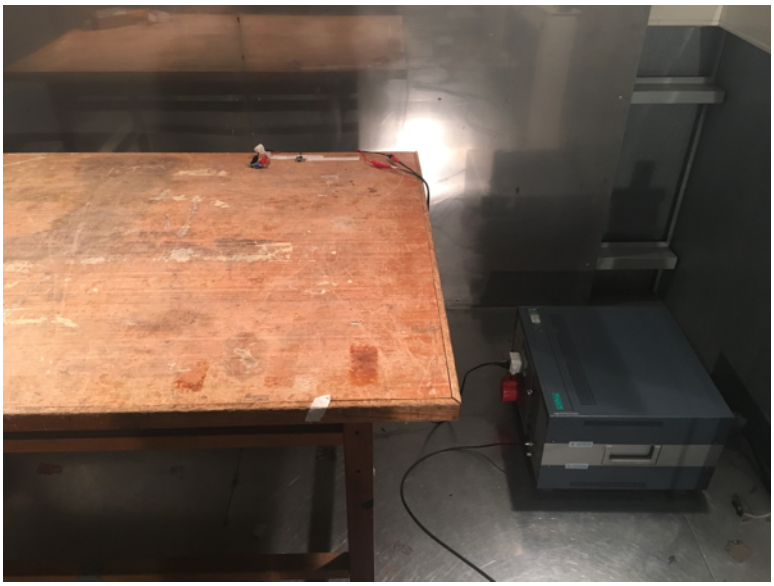


图 **21. Conducted Emission Test Setup**

The board pass the conducted emission test with more than 4 dB of margin.

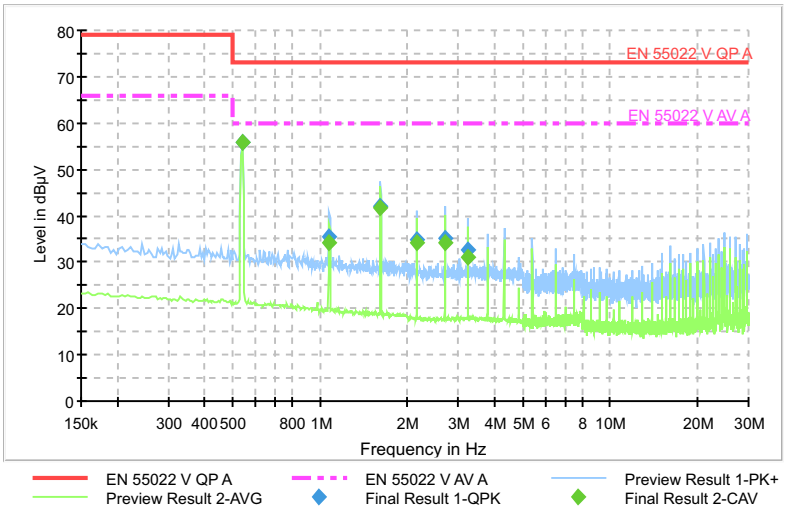


图 **22. Conducted Emission Test Result**

表 **10. Final Result 1**

FREQ (MHz)	QUASIPEAK (dBµV)	MEAS TIME (ms)	BANDWIDTH (kHz)	PE	LINE	CORR (dB)	MARGIN (dB)	LIMIT (dBµV)
0.5405	55.8	1000	9	FLO	L1	20.3	17.2	73
1.0760	35.5	1000	9	FLO	L1	20.4	37.5	73
1.1610	42.2	1000	9	FLO	L1	20.5	30.8	73
2.1560	34.8	1000	9	FLO	L1	20.6	38.2	73
2.6960	35.0	1000	9	FLO	L1	20.6	38.0	73
3.2360	32.6	1000	9	FLO	L1	20.7	40.4	73

表 **11. Final Result 2**

FREQ (MHz)	AVERAGE (dBµV)	MEAS TIME (ms)	BANDWIDTH (kHz)	PE	LINE	CORR (dB)	MARGIN (dB)	LIMIT (dBµV)
0.5405	55.9	1000	9	FLO	L1	20.3	4.1	60
1.0760	34.2	1000	9	FLO	L1	20.4	25.8	60
1.1610	41.6	1000	9	FLO	L1	20.5	18.4	60
2.1560	34.2	1000	9	FLO	L1	20.6	25.8	60
2.6960	34.0	1000	9	FLO	L1	20.6	26	60
3.2360	31.0	1000	9	FLO	L1	20.7	29	60

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01448.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01448.

4.3 PCB Layout Recommendations

In switch mode DC/DC, take care to avoid coupling between the different loops to improve performances. In a Buck topology, the input loop is particularly critical; for this reason, place the input capacitors as close as possible to the TPS561201.

This is done by separating the noise sensitive loop (feedback and enable) from the high di/dt loops (input, switch node, bootstrap). Separate these loops by placing the components and traces of the feedback and enable loop as far as possible from components and traces with high di/dt.

Also give special attention to the ground plane; try to make it as large and as solid as possible to both reduce noise sensitivity and help thermal dissipation. With regards to thermal dissipation, the input and output voltage planes must also made as large and solid as possible to help keep the board as cool as possible.

Lastly, the soldering pad for the inductor was slightly enlarged to allow the tests of several inductors.

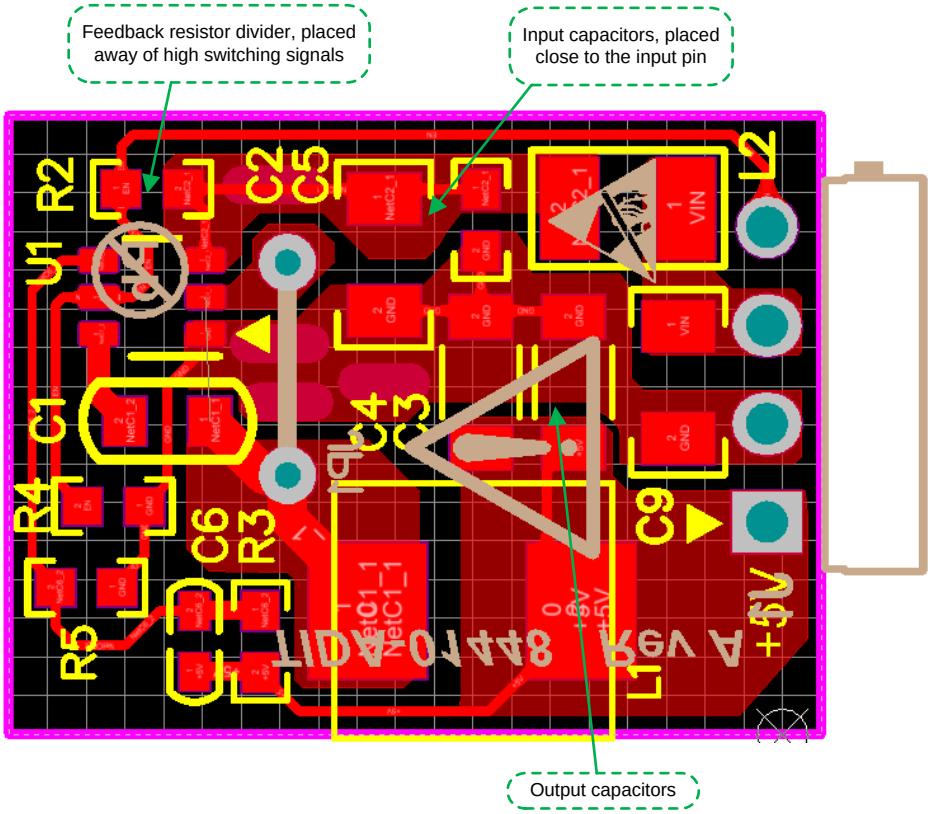


图 **23. Top Layer**

4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01448.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01448.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01448.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01448.

5 Related Documentation

1. Texas Instruments, *Understanding Buck Power Stages In Switchmode Power Supplies*, Application Report (SLVA057)
2. Texas Instruments, *Layout Tips for EMI Reduction in DC / DC Converters*, AN-2155 Application Report (SNVA638)
3. Texas Instruments, *Simple Success With Conducted EMI From DCDC Converters*, AN-2162 Application Report (SNVA489)

5.1 商标

6 About the Authors

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