

TI Designs: TIDA-00743

采用 AB 类外形的 2MHz 汽车 D 类 4 通道 21W 音频放大器参考设计



说明

TI 设计 TIDA-00743 是一个小型模块，用于评估经典 AB 类音频功率放大器模块专用系统中的数字输入 D 类音频放大器。高性能音频模数转换器 (ADC) 从四路模拟输入创建数字数据流，并为系统创建数字计时。然后 D 类放大器为系统内的扬声器提供驱动。

资源

TIDA-00743	设计文件夹
TAS6424-Q1	产品文件夹
PCM1865-Q1	产品文件夹
CDCS504-Q1	产品文件夹
TPS7B6733-Q1	产品文件夹

特性

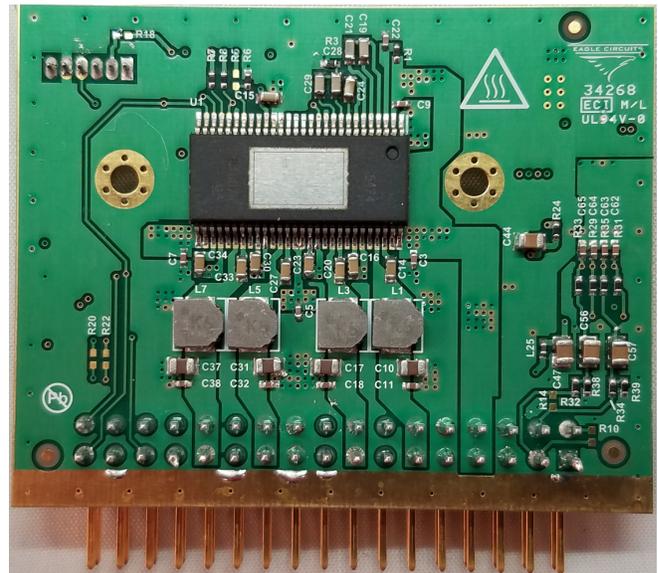
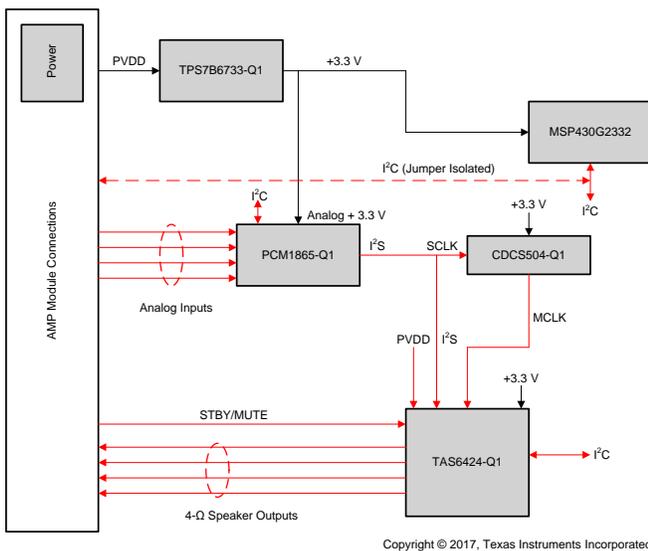
- 音频输出功率：在 14.4V 电源电压、4Ω 负载和 1% THD + N 的条件下，每通道为 21 W
- 符合汽车 CISPR25 5 类 EMI 要求
- 4.5V 至 18V 的宽电源电压范围
- 40V 负载突降保护

应用

- 音响主机
- 高级放大器



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1 System Description

The TIDA-00743 2-MHz automotive class D, four-channel, 20-W audio amplifier reference design is a subsystem module that combines a four-channel class D amplifier with a four channel audio ADC to allow evaluation of the class D amplifier in class AB applications. The size and shape of the TIDA-00743 circuit board is designed to allow the replacement of a class AB amplifier module. The TAS6424-Q1 class D amplifier stage is designed to provide 4- Ω output capability. The PCM1865 audio ADC provides the digital audio timing reference required by the TAS6424 and digitizes four channels of analog audio signals. A CDCS504-Q1 clock generator is used to create the required master clock from the I²S bit clock as required by the TAS6424. An MSP430™ microcontroller (MCU) is included to initialize the PCM1865 and the TAS6424. The MCU and the digital audio timing from the PCM1865 are provided in place of the timing and control provided by an application processor in a typical automotive head unit or premium amplifier.

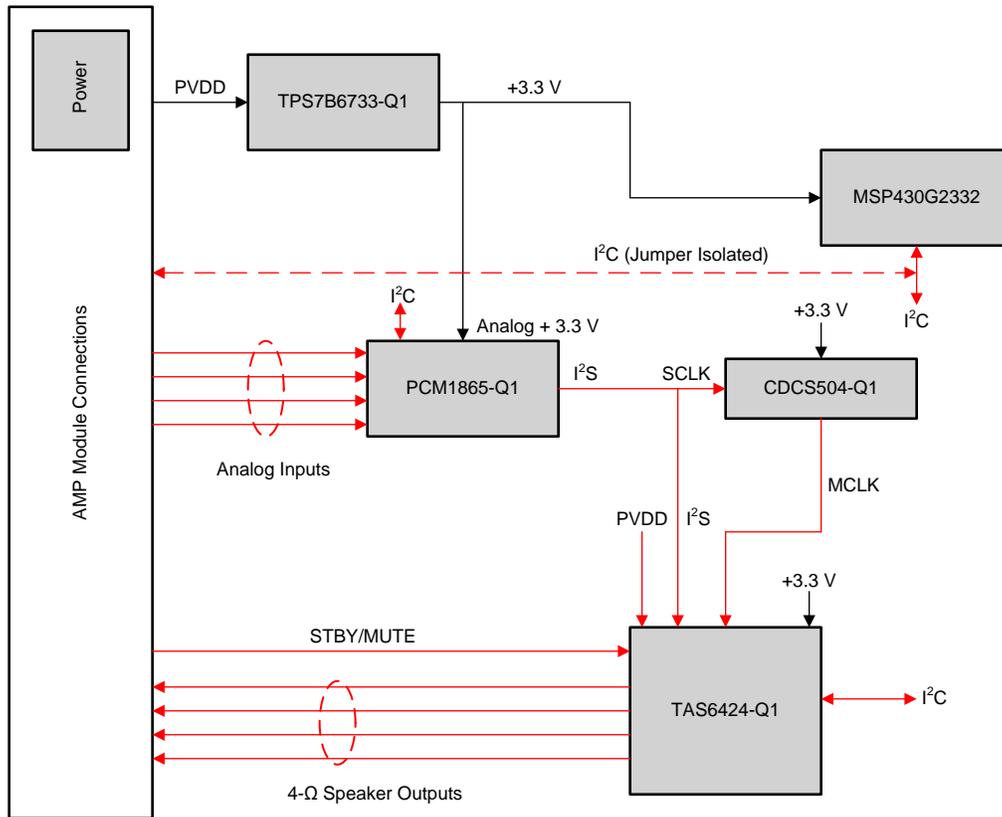
1.1 Key System Specifications

表 1. Key System Specifications

PARAMETER	SPECIFICATIONS	DETAILS
Input power source	Automobile battery 4.5 V to 18 V with transients to 40 V	节 2.3.1 , 节 2.4.1.2
Operating temperature	-40°C to 125°C	2.3 节
Total harmonic distortion plus noise (THD + N)	0.03% typical at 1-W output with a 1-kHz signal	节 3.2.1
Signal input	Analog, 2.1 V _{RMS} max	节 2.3.3
Audio power output	25 W into 4 Ω with 10% THD + N	节 3.2.1
Audio power output	20 W into 4 Ω with 1% THD + N	节 3.2.1
EMI	CISPR-25 leve-5 conducted and radiated	节 3.2.2
Form factor	42.3x53.5-mm rectangular PCB	节 2.4.1.1

2 System Overview

2.1 Block Diagram



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图 1. TIDA-00743 Block Diagram

2.2 Design Considerations

This design has several requirements beyond the specifications of the main component parts. The printed-circuit board (PCB) itself must be of a size similar to a typical Class AB amplifier module. The electronics emulate the operation of a class AB amplifier, so the board must have analog audio inputs. The analog inputs must be compatible with typical audio digital-to-analog converter (DAC) outputs or cell phone headphone outputs. I²S timing must be provided on the board so that the TAS6424-Q1 has the required timing. A 3.3-V power supply must be provided on the board to power the digital portions of the circuit. The board must also have a means to configure itself so that no external software control is required to test the board.

2.3 Highlighted Products

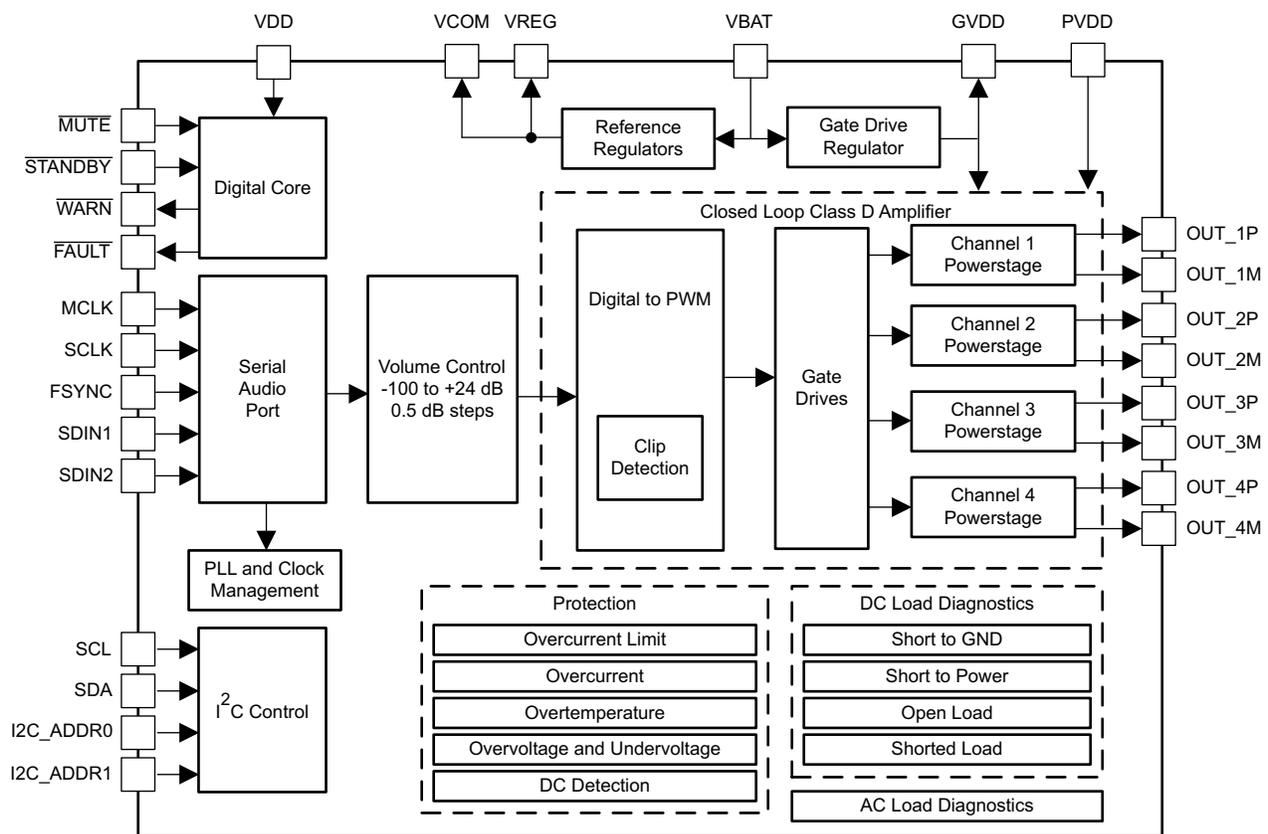
2.3.1 TAS6424-Q1

The TAS6424-Q1 device is a four-channel digital-input class-D audio amplifier designed for use in automotive head units and external amplifier modules (see 图 2). The device provides four channels at 27 W into 4 Ω at 10% THD+N and 45 W into 2 Ω at 10% THD+N from a 14.4-V supply and 75 W into 4 Ω at 10% THD+N from a 25-V supply. The Class-D topology dramatically improves efficiency over traditional linear amplifier solutions. The output switching frequency can be set either above the AM band, which eliminates the AM-band interference and reduces output filtering and cost, or below AM band to optimize efficiency.

The wide supply-voltage range from 4.5 V to 26.4 V helps minimize audio artifacts in start-stop applications.

The device incorporates all the functionality required to perform in the demanding OEM applications area. The device has a built-in load diagnostic function for detecting and diagnosing misconnected outputs as well as detecting AC-coupled tweeters to help reduce test time during the manufacturing process.

The device is offered in a 56-pin HSSOP PowerPAD™ package with the exposed thermal pad up.



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图 2. TAS6424-Q1 Functional Block Diagram

2.3.2 TPS7B6733-Q1

The TPS7B6701-Q1, TPS7B6733-Q1, and TPS7B6750-Q1 devices (TPS7B67xx-Q1) are low-dropout linear regulators designed for up to 40-V V_{IN} operations (see 图 3). These devices drive loads up to 450 mA with only 15- μ A quiescent current at light load, which greatly increases the endurance time of the automotive battery.

The TPS7B67xx-Q1 family of devices features an integrated short-circuit and overcurrent protection. Reset delay and power-good signal are implemented on power-up to indicate that the output voltage is stable and is in regulation. An external capacitor programs the delay. The enable function activates and deactivates the device with an I/O port from the MCU.

The device family operates at a temperature range of -40°C to 125°C .

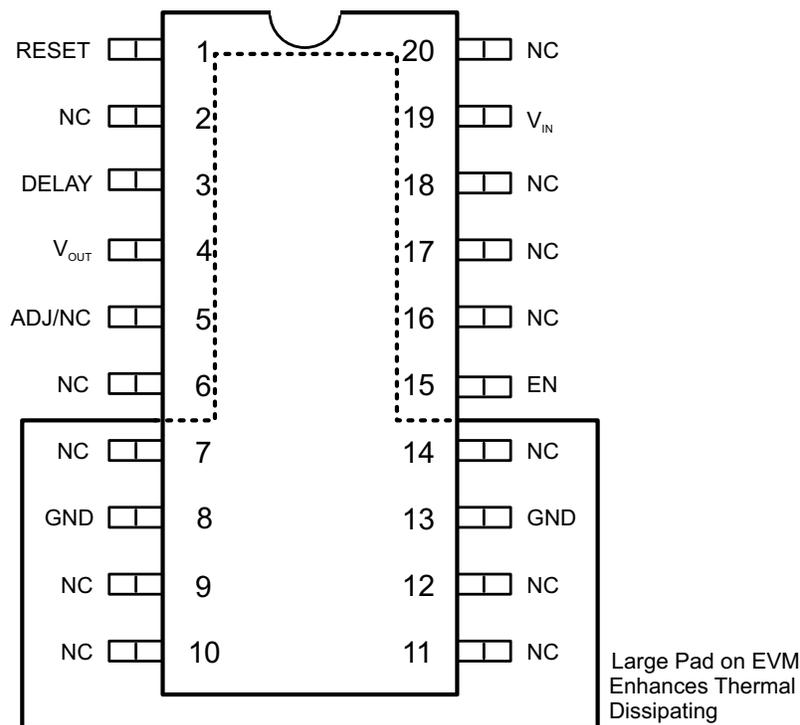


图 3. TPS7B6733-Q1 Enhanced Thermal Pad

2.3.3 PCM1865-Q1

The PCM1865-Q1 audio front-end device takes a new approach to audio-function integration to ease compliance with European Ecodesign legislation while enabling high-performance end products (see 图 4). Smaller, smarter products are becoming increasingly feasible at reduced costs without the requirement for a 5-V supply or an external programmable-gain amplifier.

The highly-flexible audio front end of the PCM1865-Q1 supports input levels from small-mV microphone inputs to 2.1- V_{RMS} line inputs without external resistor dividers. The PCM1865-Q1 integrates many system-level functions that assist or replace some digital signal processing (DPS) functions.

All of these features are available using a single 3.3-V power supply. An integrated band-gap voltage reference provides excellent power supply rejection ratio (PSRR) such that a dedicated analog 3.3-V rail may not be required.

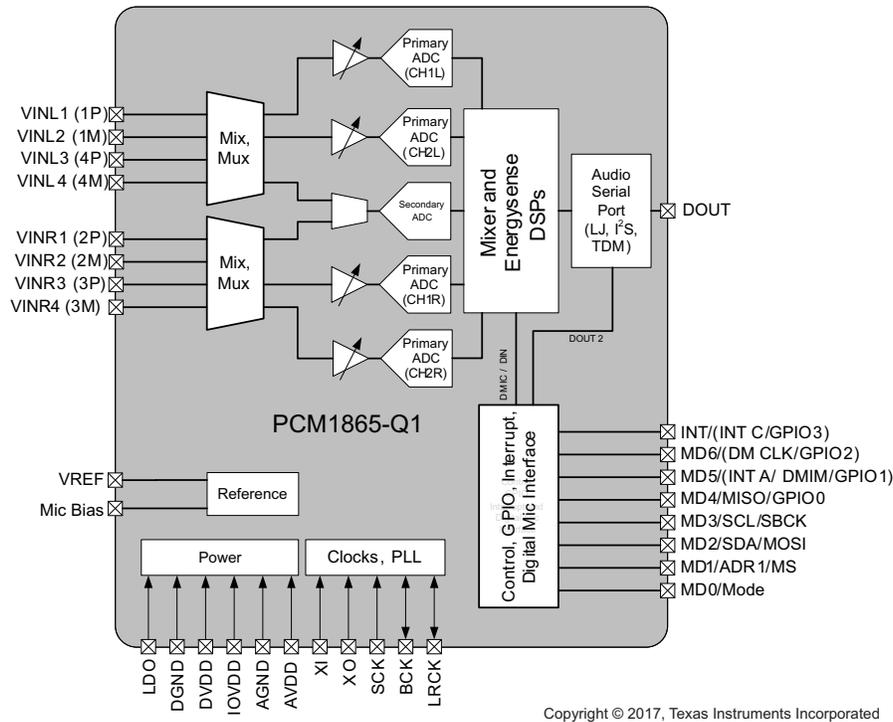


图 4. PCM1865-Q1 Simplified Block Diagram

2.3.4 CDCS504-Q1

The CDCS504-Q1 device is a LVCMOS input clock buffer with selectable frequency multiplication (see 图 5).

The CDCS504-Q1 has an output enable pin. The device accepts a 3.3-V LVCMOS signal at the input. The input signal is processed by a phased-locked loop (PLL), whose output frequency is either equal to the input frequency or multiplied by the factor of four. By this, the device can generate output frequencies between 2 MHz and 108 MHz. A separate control pin can be used to enable or disable the output. The CDCS504-Q1 device operates in a 3.3-V environment.

The device is characterized for operation from -40°C to 105°C and is available in an eight-pin TSSOP package.

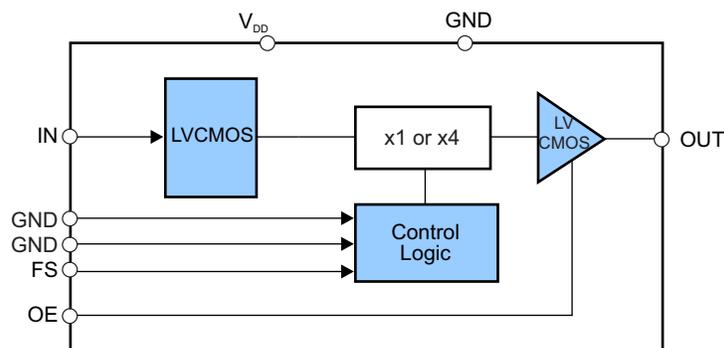


图 5. CDCS504-Q1 Functional Block Diagram

2.3.5 MSP430G2332

The Texas Instruments MSP430™ family of ultra-low-power microcontrollers consist of several devices featuring different sets of peripherals targeted for various applications. The architecture, combined with five low-power modes is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows wake-up from low-power modes to active mode in less than 1 μs.

The MSP430G2332 series of microcontrollers are ultra-low-power mixed signal microcontrollers with built-in 16-bit timers, and up to 16 I/O touch sense enabled pins and built-in communication capability using the universal serial communication interface (see 图 6). The MSP430G2332 series have a 10-bit A/D converter. See the *Available Options* table in the MSP430G2xx2 data sheet[1] for configuration details. Typical applications include low-cost sensor systems that capture analog signals, convert them to digital values, and then process the data for display or for transmission to a host system.

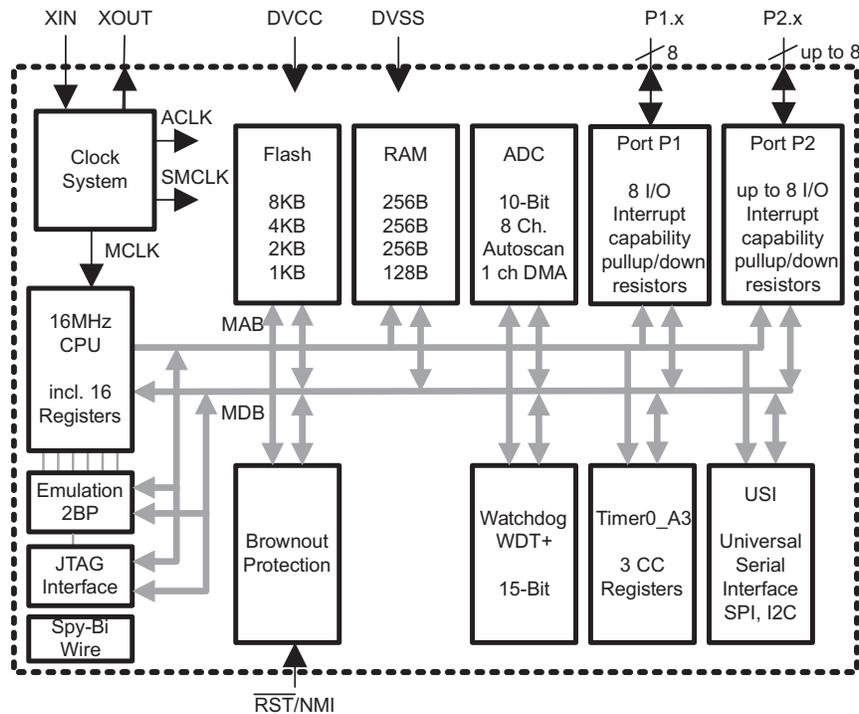


图 6. MSP430G2332 Functional Block Diagram

2.4 System Design Theory

2.4.1 Hardware Overview

The TIDA-00743 allows a user to evaluate the TAS6424-Q1 class D amplifier in systems designed to use class AB amplifier modules. Class AB amplifiers have analog inputs, while the TAS6424-Q1 has a digital input. A PCM1865-Q1 front end is included in the design to provide the I²S (Inter-IC sound) digital audio signal and timing required by the TAS6424-Q1 amplifier. When the TAS6424-Q1 is used with I²S, a master clock operating at four times the frequency of the bit clock is required. The CDCS504-Q1 multiplier and buffer provides the master clock.

图 7 shows the complete TIDA-00743 PCB.

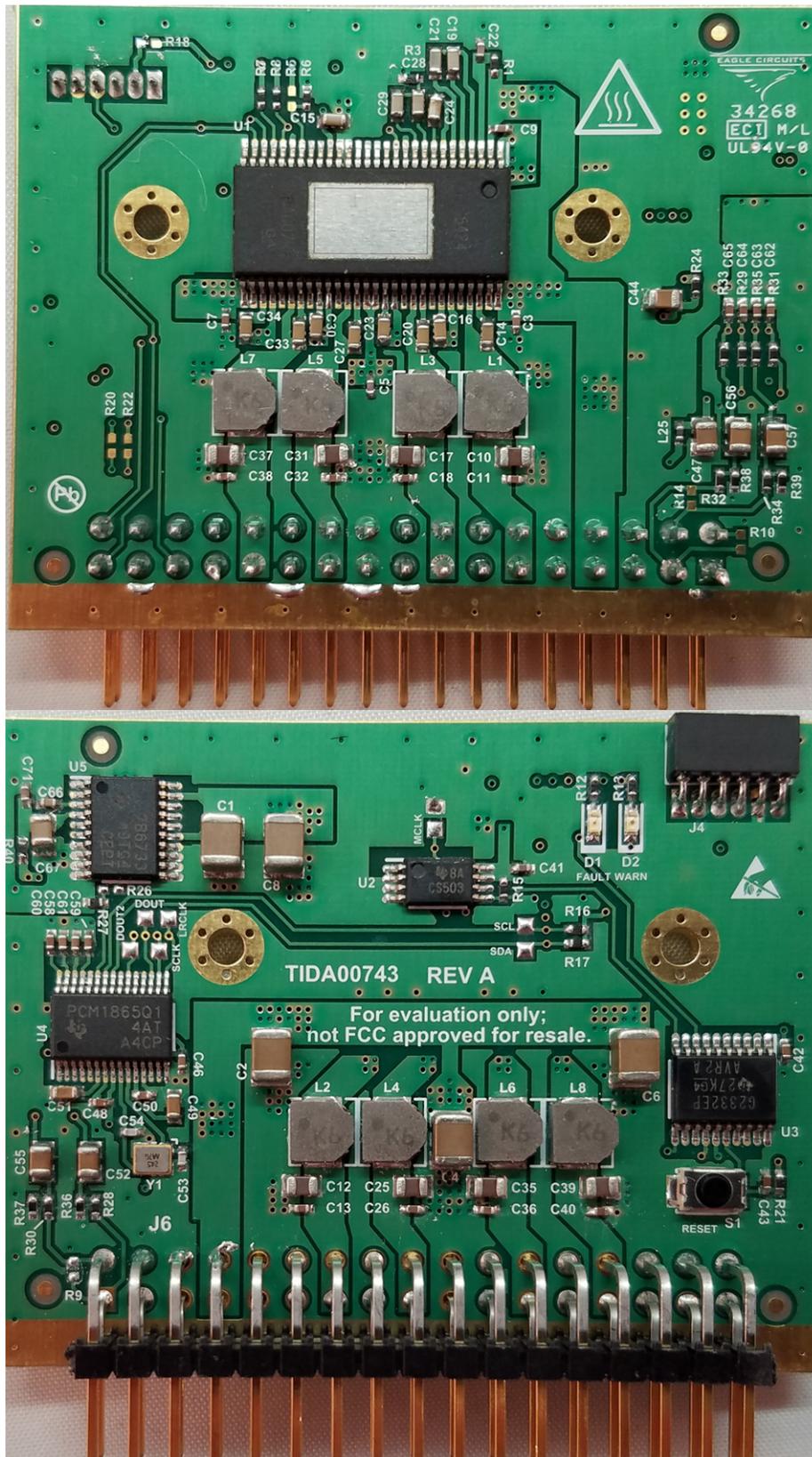


图 7. TIDA-00743 PCB

2.4.1.1 PCB Outline and Interface

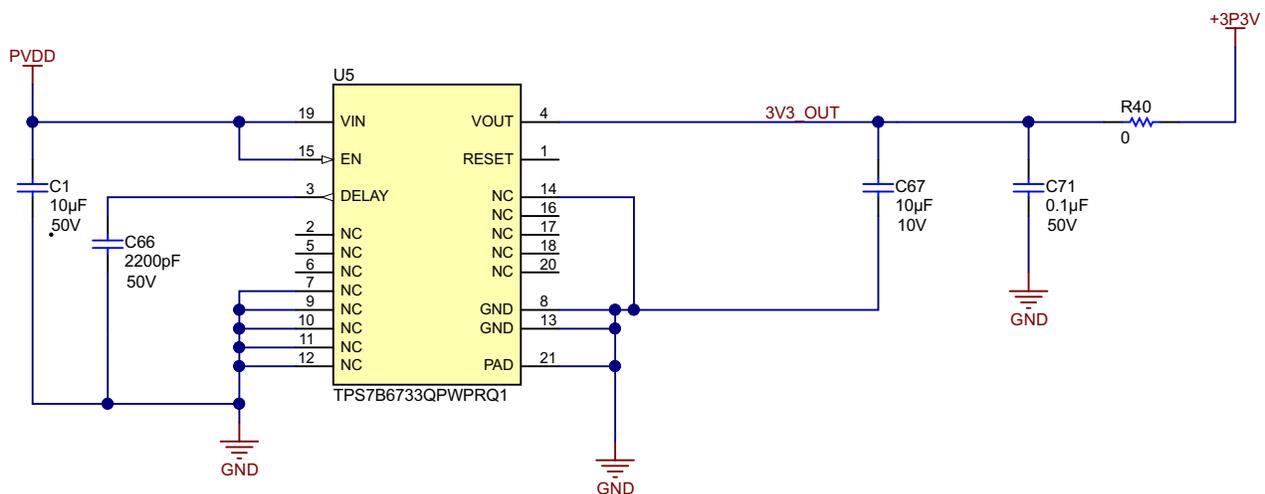
The PCB is designed to resemble a typical class AB audio power amplifier that stands vertically from a main system PCB and mounts to a heat sink. The board outline and mounting hole positions have not been copied from a specific amplifier module. The main connector is a standard two-row header connector with 2.54-mm (100-mil) pin spacing. The board size is 53.5 mm by 42.3 mm (2.11 in by 1.665 in).

2.4.1.2 Power

The power supplied to the TIDA-00743 design can be in the range of a typical automotive battery. The TAS6424-Q1 has two power rails which connect directly to a main power input. V_{BAT} is connected to the TAS6424-Q1 at pin 3. V_{BAT} can be in the range of 4.5 V to 18 V. P_{VDD} must be in the range of 4.5 V to 26.4 V. The module input voltage must be limited to less than 18 V because V_{BAT} is the limiting voltage. The rest of the components in the system operate at 3.3 V, so a regulator is provided to create 3.3 V from the input voltage.

2.4.1.2.1 TPS7B6733-Q1

The TPS7B6733-Q1 linear regulator provides the regulated 3.3- V_{DC} required by the other active parts in the subsystem. The TPS7B6733-Q1 has been selected because its input voltage range is 4 V to 40 V. The TPS7B6733 package is designed to dissipate heat through a thermal pad and extra pins on the device, which enable it to source as much as 450 mA (see 图 8). The 450-mV dropout voltage of the TPS7B6733-Q1 allows it to maintain output regulation when the input voltage drops to the 4.5-V minimum voltage for the TAS6424-Q1.



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图 8. TPS7B6733-Q1 Linear Regulator Circuit

2.4.1.3 PCM1865-Q1

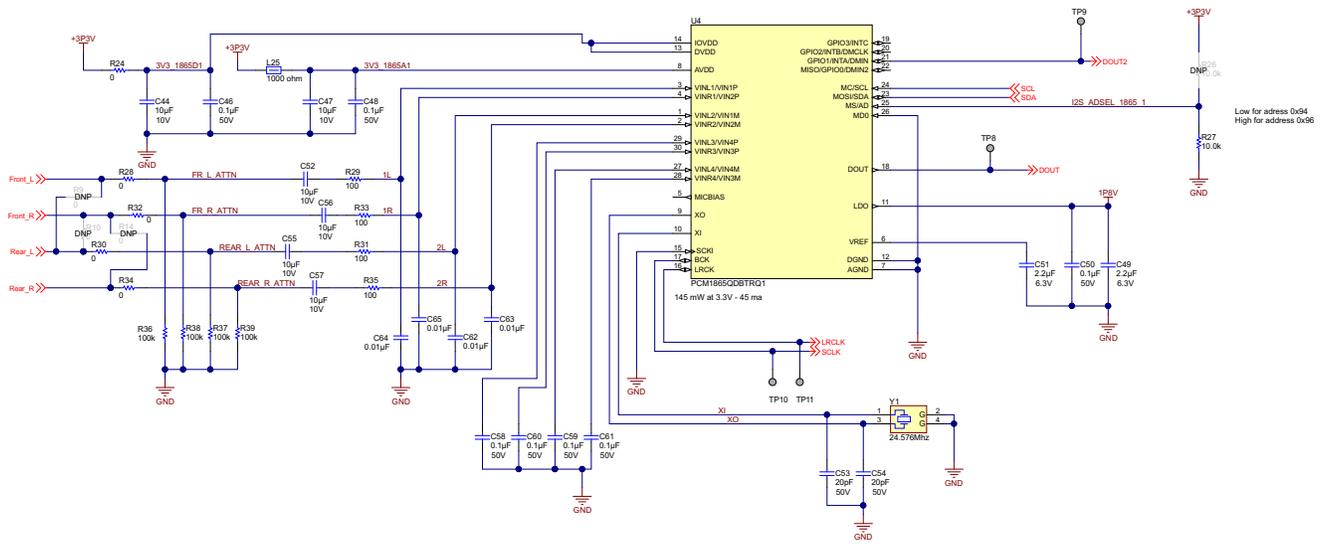
The PCM1865-Q1 is ideal for this design (see 图 9). Four ADC channels are required to provide the four channels of digital data for the TAS6424-Q1. The PCM1865-Q1 (U4) has an internal clock generator to create either I²S or time-division multiplexed (TDM) data streams. A 24.576-MHz crystal, Y1, acts as the timing reference for the PCM1865-Q1 device.

The power to the PCM1865-Q1 is +3.3 V. The digital IO and internal digital circuits are supplied through IOVDD and DVDD, which are connected together. R24 is included to allow measurement of digital current and in case extra filtering is desired. C46 acts as a bypass capacitor and is placed close to U4 pins 13 and 14. The +3.3 V for the analog section, AVDD, is filtered by L25, C47 and C48. C48 is placed close to U4 pin 8 to provide a bypass to ground.

The four analog inputs to the PCM1865-Q1 are configured as single-ended inputs. Several passive components are required to couple the analog signal into each ADC channel of the PCM1865 device. Input channel VIN1L is fed from the signal Front_L. R28 and R36 form a resistive divider for use with signals that are greater than $2.1 V_{\text{RMS}}$. R28 is populated with a 0- Ω resistor while R36 has a 100-k Ω resistor to act as the signal load. If a signal source has an amplitude higher than $2.1 V_{\text{RMS}}$, R28 and R36 can be changed to provide some attenuation to the signal before it reaches the PCM1865-Q1 device. Capacitor C52 AC-couples the input signal to prevent a DC bias from saturating or otherwise damaging the input. R29 and C64, which are 100 Ω and 0.01 μF , respectively, form a low-pass filter with a cutoff frequency of 159 kHz. The high cutoff frequency is chosen to ensure that the signal has only been attenuated by -0.077 dB at 20 kHz. All four analog inputs have the same circuit. Several unpopulated resistors can also be used to jumper the different inputs together so that one signal source can drive multiple channels. The four input channels have a corresponding output channel on the TAS6424-Q1:

- Input Front_L drives output channel 1
- Input Front_R drives output channel 2
- Input Rear_L drives output channel 3
- Input Rear_R drives output channel 4

The digital interface on the PCM1865-Q1 includes an I²C interface and the digital audio interface. The I²C interface connects to the system MCU and is used to configure the PCM1865-Q1. The digital audio interface consists of four signals: SCLK, LRCLK, DOUT, and DOUT2. SCLK is the serial or BIT clock. In some applications and on the PCM1865-Q1 data sheet, this signal is called BCLK or BCK. The LRCLK signal is the left-right clock, also known as the word clock. This clock indicates whether the current data word is the left or right channel data. The frequency of LRCLK is equal to the sampling clock frequency. DOUT and DOUT2 are the data outputs. I²S data has two data words per output, so DOUT2 is configured by software to create a data lane for the second data pair. The DOUT data words are 24 bits each, though the data stream is configured for 32-bit words. For this design, the audio sampling rate is 96 kHz. Consequently, SCLK is 6.144 MHz. The audio sampling rate can be set at either 48 kHz or 44.1 kHz if desired.

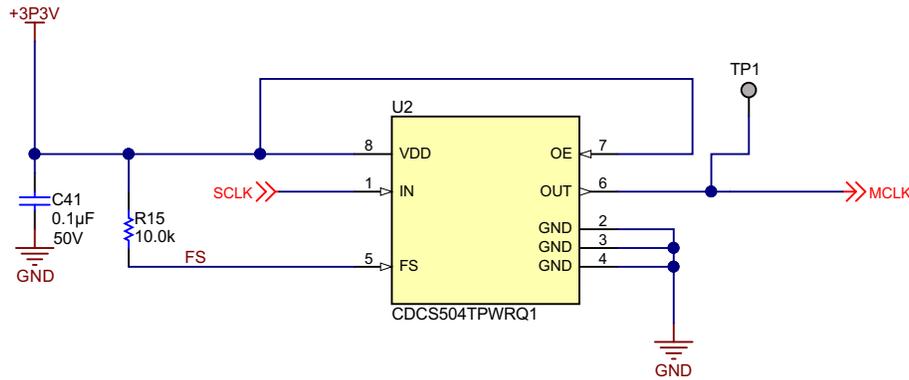


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图 9. PCM1865-Q1 Circuit

2.4.1.4 CDCS504-Q1

The CDCS504-Q1 is a clock buffer and clock multiplier IC (see 图 10). In this design, the CDCS504-Q1 is used to multiply the 6.144-MHz SCLK four times in frequency to provide a 24.576-MHz master clock, or MCLK, to the TAS642-Q1 device. If TDM operation is desired, the MSP430 MCU can set the FS signal low so that the CDCS504-Q1 device does not multiply SCLK. The SCLK is 24.576 MHz if the TIDA-00743 module board is configured for TDM mode.



FS High for 4x mult, low for TDM mode

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图 10. CDCS504-Q1 Circuit

2.4.1.5 TAS6424-Q1

The TAS6424-Q1 is a 75-W class-D audio power amplifier that operates with a switching frequency of 2.1 MHz (see 图 11). The TAS6424-Q1 has a digital audio input that is compatible with I²S and TDM digital audio data. The digital audio input enables a system designer to eliminate an analog signal chain that connects from an audio DAC, through the circuit board, and to the power amplifier. Removing this analog signal chain reduces the risk of noise interference in the audio signal. The TAS6424-Q1 has load dump protection, so the power pins for P_{VDD} and P_{VDD} can be connected directly to the car battery system.

The TAS6424-Q1 (U1) has three voltage inputs. V_{DD} is a logic-level supply connected at U1 pin 19 and must be in the range of 3 V to 3.5 V. V_{BAT} is connected to the TAS6424-Q1 at pin 3. P_{VDD} connects to U1 pins 2, 29, 30, 42, 43, 55, and 56. Other voltages are generated inside the TAS6424-Q1. V_{REG} is an internal regulator, which is bypassed to A_{REF} by C19. V_{COM} is an internal reference, which C21 bypasses to A_{REF}. The two voltages G_{VDD} form the gate drive for the output high-side MOSFETs. U1 pin 9 is the G_{VDD} for outputs 3 and 4 while pin 10 is the G_{VDD} for outputs 1 and 2. Both pins are bypassed to ground with 1-µF capacitors.

Pins 12 through 16 form the digital audio input to the TAS6424-Q1 device from the PCM1865-Q1 device. Pins 20 and 21 are the I²C interface. Pins 22 and 23 set the address for the I²C. In this design, Pin 23 is always grounded because there are no other TAS6424 devices in the system. Pin 24 is the nSTANDBY function. If this signal is set low, the TAS6424-Q1 device is in a low-power standby state. This function is not used in TIDA-00743. Pin 25 is the nMUTE function. When this signal is low, the outputs of the TAS6424-Q1 are muted, but the operating state of the device is maintained. Pins 24 and 25 must be

pulled up by resistors or a processor for the TAS6424-Q1 device to operate. Pins 26 and 27 are open-drain outputs. These pins can be used as light-emitting diode (LED) drivers, as shown in 图 11, or as processor interrupts. Pin 26 is asserted low when a defined fault condition exists. Pin 27 is asserted low when clipping occurs or if the TAS6424-Q1 has passed the overtemperature warning threshold. See the [TAS6424-Q1](#) data sheet[2] for more details.

Each output channel is a bridge-tied load (BTL) output. This topology requires a low-pass filter for both the positive- and negative-going outputs of each channel. The output inductors for TIDA-00743 have been chosen to be shorter than a TAS6424-Q1 device so that the heat sink does not create any mechanical interference form the inductors. The size of the inductors also limits the output impedance to be 4 Ω or higher. The design of the filter follows the reference schematic on the TAS6424-Q1 data sheet. The choice of inductor has a great impact on the THD of the amplifier circuit and also determines whether a lower impedance load is possible. Typically, smaller inductors yield a higher THD while larger inductors yield a lower THD and greater current capacity. The inductors chosen for this design are a balance between size and performance.

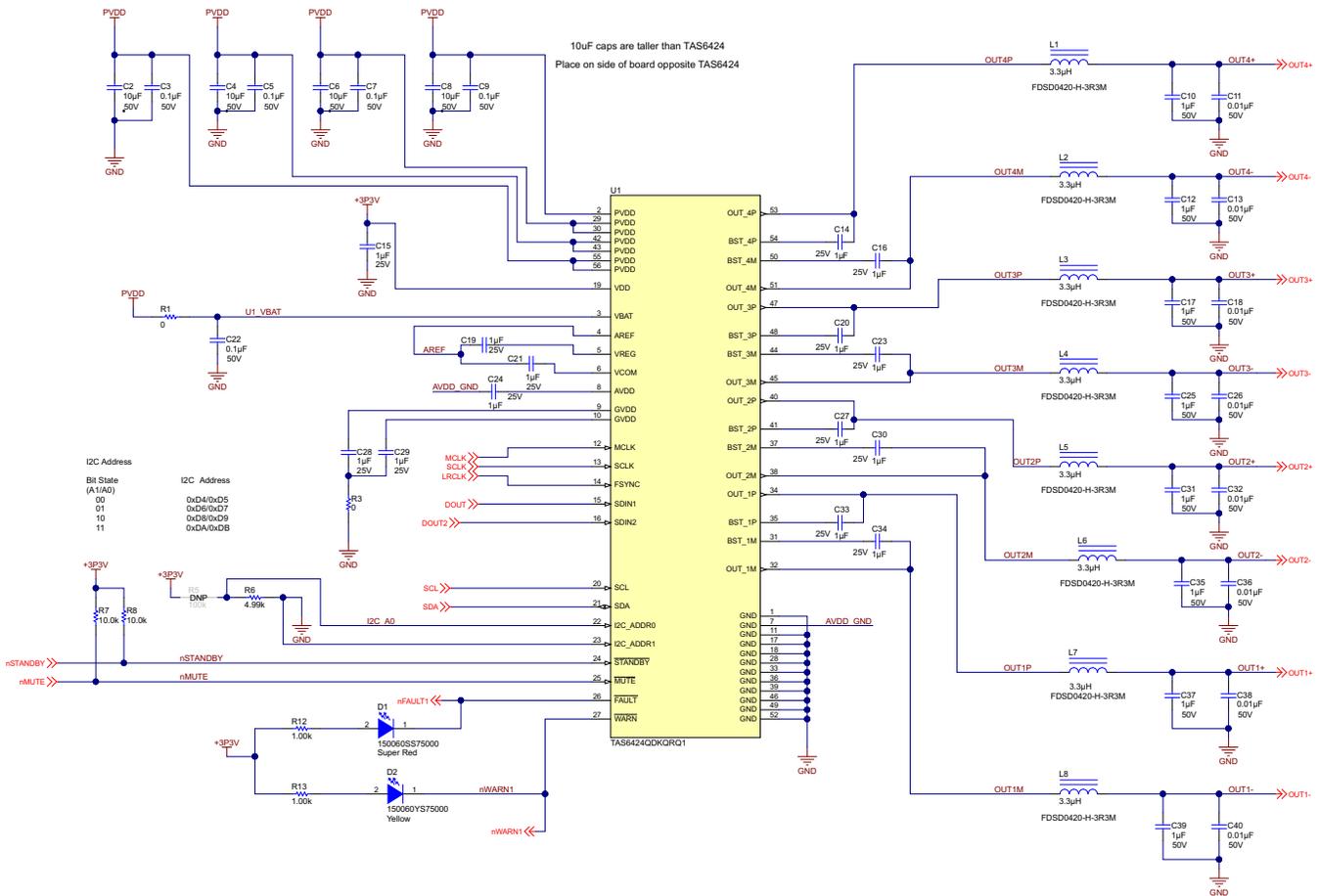
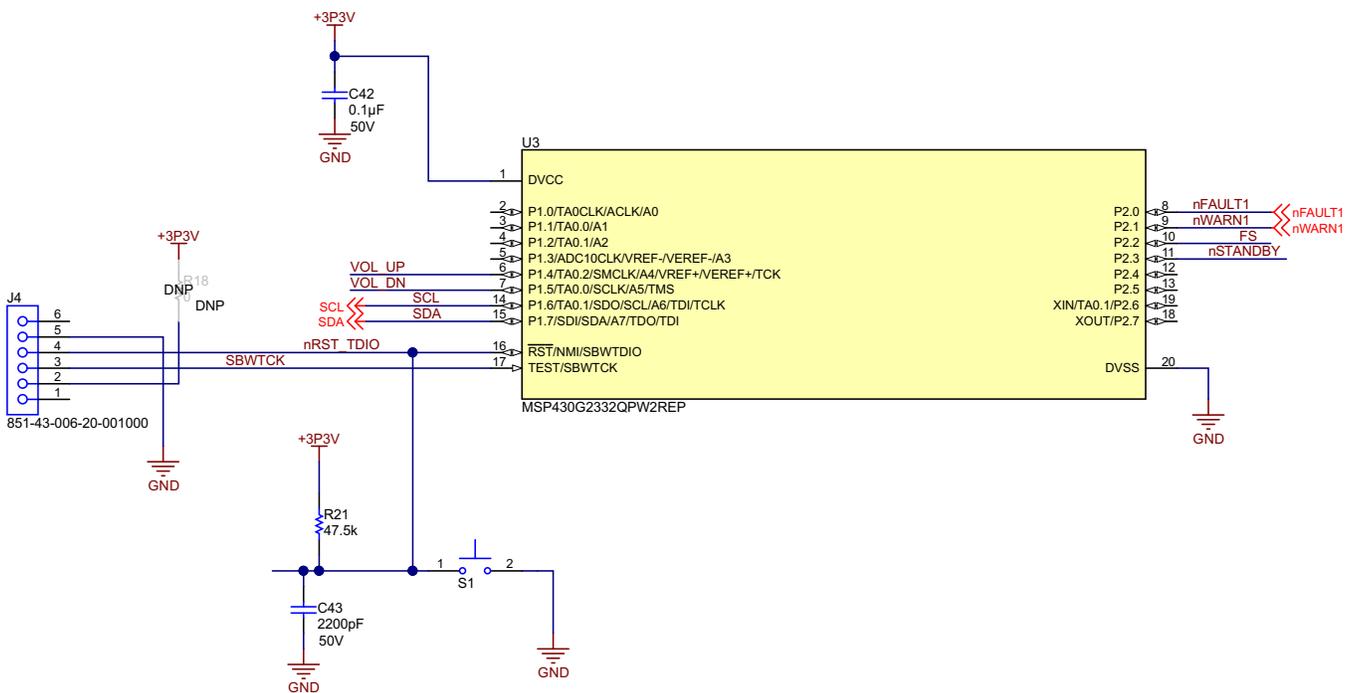


图 11. TAS6424-Q1 Class-D Power Audio Amplifier Circuit

2.4.1.6 Support Circuits

2.4.1.6.1 MSP430G2332-EP

Creating a stand-alone design requires a host processor to configure the PCM1865-Q1 and the TAS6424-Q1 at power up. The MSP430G2332-EP has been chosen because this board design is intended for an extended temperature range. The I²C interface that connects to the PCM1865-Q1 and the TAS6424-Q1 is the primary interface from the MSP430 to the other components on the board (see 图 12). J4 is the programming interface for the MSP430. R21 and C43 provide a delayed power-up reset function. Switch S1 allows a user to reset the MSP430 without cycling power to the board. The signal FS controls the multiply function on the CDCS504-Q1 as described in 节 2.4.1.4. The signals nWARN1 and nFAULT1 are routed from the TAS6424-Q1 to the MSP430, but there is no provision in the software to act upon faults or warnings.

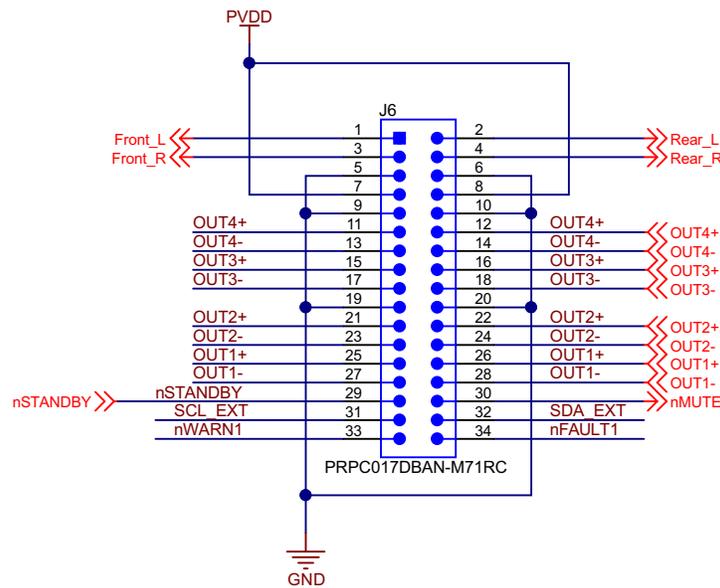


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图 12. TIDA-00743 Microcontroller

2.4.1.6.2 Interface Connector

The interface connector J6 is a standard, two-row 100-mil (2.54-mm) spacing connector (see 图 13). This type has been selected so that the TIDA-00743 circuit board has an interface that is similar to the typical package for a vertically-mounted class AB amplifier IC. The inputs are arranged so that they are isolated from the power and speaker outputs by ground pins. The speaker output pins are doubled to reduce the impedance of the output connections. the signals nSTANDBY and nMUTE are brought out to allow control of those functions on the TAS6424-Q1. The I²C interface can be connected to J6 by placing 0-Ω resistors in the positions for R20 and R22. This connection allows the PCM1865-Q1 and the TAS6424-Q1 to be controlled by a host processor that is not on the module circuit board. Signals nWARN1 and nFAULT1 are the warning and fault connections from the TAS6424-Q1.

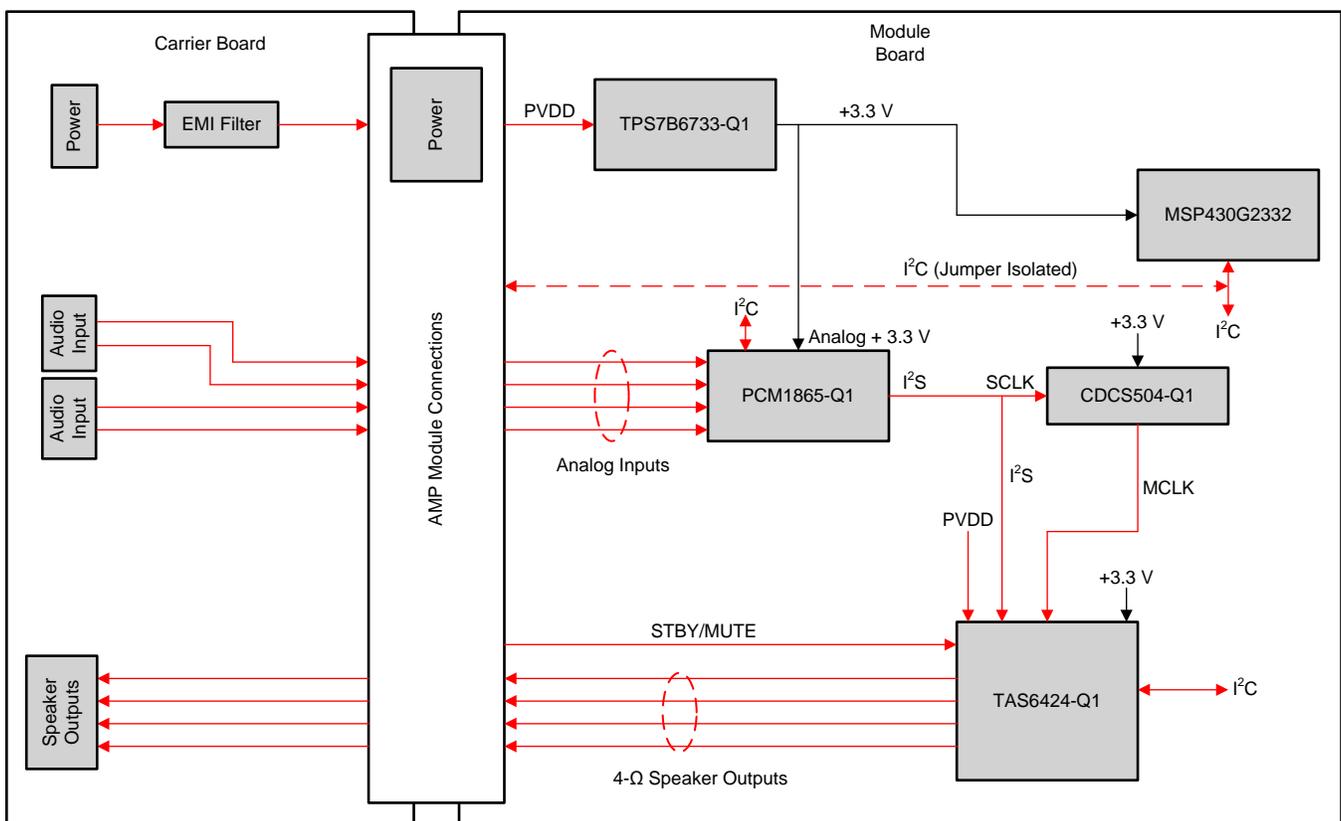


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图 13. TIDA-00743 Interface Connector

2.4.1.6.3 Carrier Board

A carrier board has been designed to add some of the power filtering found in typical systems to test the TIDA-00743 design (see 图 14). Connectors for power, audio input, and speaker outputs are also included. The carrier board is designed to allow the TIDA-00743 to be mechanically attached to a metal box. This box, a BUD CU-234, acts as both a heat sink to cool the TAS6424 and as a Faraday cage to improve electromagnetic interference (EMI) performance of the system. Extra capacitors are placed at the power input and audio power outputs to short any residual high-frequency noise back to the system ground. The ground connection on the carrier board has the solder mask cleared so that the metal box can make electrical contact with the board ground. All signal routing on the carrier board is located on interior layers to ensure that the signals do not radiate EMI. Via stitching on the carrier board creates a continuation of the Faraday cage from the edges of the metal box out to the edges of the board. A mute switch connected to the nMUTE signal on the TAS6424-Q1 provides the user with mute control of the system.



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图 14. Block Diagram for Module Board and Carrier Board

2.4.2 Software

The MSP430 used in the TIDA-00743 circuit board is required to configure the PCM1865-Q1 and the TAS-6424-Q1 at power up. The program to accomplish this is listed in the following configuration code. The configuration program for TIDA-00743 is developed using Code Composer Studio™ (CCS) integrated development environment (IDE). Some of the software directives in the program are specific to CCS.

TIDA-00743 configuration code:

```

#include <msp430.h>
#include "USI_I2C.h"

//NOTE: Address needs to be in 7 bit form to be used with the current write and read functions.

unsigned char SLV_Test_Addr = 0x48;
unsigned char PCML_Addr = 0x4a; //PCML865 Address
unsigned char TAS1_Addr = 0x6a; //TAS6424 Address

int main(void)
{
    volatile unsigned int i; // Use volatile to prevent removal

    WDTCTL = WDTPW + WDTHOLD; // Stop watchdog
    if (CALBC1_1MHZ==0xFF) // If calibration constant erased
    {
        while(1); // do not load, trap CPU!!
    }
    DCOCTL = 0; // Select lowest DCOx and MODx settings
    BCSCTL1 = CALBC1_1MHZ; // Set DCO
    DCOCTL = CALDCO_1MHZ;

    P1OUT = 0xC0; // P1.6 & P1.7 Pullups, others to 0
    P1REN |= 0xC0; // P1.6 & P1.7 Pullups
    P1DIR = 0xFF; // Unused pins as outputs
    P2OUT = 0x0C; //Set P2.2 and P2.3 High: SCLK x4, TAS operating
    P2DIR = 0xFC; //P2.0 and 2.1 inputs

    __delay_cycles(10000);

    Set_I2C();

    __delay_cycles(10000);

//PCM1865 section
    I2C_Write (I2C_BYTE, PCML_Addr, 0x26, 0x03); //Set BCLK Divider from SCK to 1/4 on PCM1865 -
    96 kHz for LR CLK
    I2C_Write (I2C_BYTE, PCML_Addr, 0x10, 0x51); // Set GPIO1 as DOUT2 on PCM1865
    I2C_Write (I2C_BYTE, PCML_Addr, 0x20, 0x91); // Set as timing master on PCM1865

//TAS6424 section
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x04, 0x55); // Mute outputs on TAS6424
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x00, 0x80); //Master Reset TAS6424.
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x21, 0x80); //Clear Clock Fault

    I2C_Write (I2C_BYTE, TAS1_Addr, 0x01, 0x31); // Set Gain to Level 2 (15V) on TAS6424 1

    I2C_Write (I2C_BYTE, TAS1_Addr, 0x02, 0x62); // Set PWM for 44x FS on TAS6424
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x03, 0x84); // Set Sampling Rate to 96 kHz on TAS6424
    __delay_cycles(100000);
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x05, 0x0f); // Turn down Channel 1 on TAS6424
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x06, 0x0f); // Turn down Channel 2 on TAS6424
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x07, 0x0f); // Turn down Channel 3 on TAS6424
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x08, 0x0f); // Turn down Channel 4 on TAS6424
    __delay_cycles(1000000); // Anti-pop delay
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x04, 0x00); // Un-mute outputs on TAS6424
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x05, 0xd1); // Turn Up Channel 1 on TAS6424
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x06, 0xd1); // Turn Up Channel 2 on TAS6424
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x07, 0xd1); // Turn Up Channel 3 on TAS6424
    I2C_Write (I2C_BYTE, TAS1_Addr, 0x08, 0xd1); // Turn Up Channel 4 on TAS6424
    LPM0;
}

```

The include file, *mcp430.h*, is part of the MSP430Ware™ software library provided by Texas Instruments as an add-on to CCS. The include file *USI_I2C.h* defines the I²C commands used by the universal serial interface (USI) block in the MSP430G2332. Next, two variables are declared to represent the I²C addresses of the TAS6424-Q1 and the PCM1865-Q1.

The main function starts after the declarations. The first commands are a test to ensure that the calibration for the MSP430 internal clock is valid. If the clock calibration is valid, the clock and the GPIO for banks 1 and 2 are set up. This step is followed by a delay to ensure that the GPIO outputs are settled. The I²C section is then set up.

The next section contains three commands to configure the PCM1865-Q1 device. The first command is:

```
I2C_Write (I2C_BYTE, PCM1_Addr, 0x26, 0x03);
```

This command sets the master clock-to-BCLK divide ratio. The command shown sets the BCLK to ¼th the value of the 24.576-MHz timing crystal, or 6.144 MHz. Note that BCLK, or bit clock, is the signal SCLK in the previous schematic images.

The second command is:

```
I2C_Write (I2C_BYTE, PCM1_Addr, 0x10, 0x51);
```

This command configures the PCM1865 GPIO1 as DOUT2, which is digital output 2. Two digital outputs are required because there are two audio channels per data output and four outputs are required.

The third command is:

```
I2C_Write (I2C_BYTE, PCM1_Addr, 0x20, 0x91);
```

This command sets the PCM1865-Q1 as the timing master for the I²S bus. The rest of the registers are allowed to keep their default settings.

The TAS6424-Q1 configuration setting is more complicated:

```
I2C_Write (I2C_BYTE, TAS1_Addr, 0x00, 0x80);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x04, 0x55);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x21, 0x80);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x01, 0x31);
```

The first command in the TAS6424-Q1 configuration setting is a master reset for the TAS6424-Q1. This command restarts the part. The second command ensures the outputs are muted so that nothing can be heard during configuration. The third command clears the clock fault register. At power up, a clock fault is registered because there is no clock input to the device until the PCM1865-Q1 device has been configured. After the PCM1865-Q1 device has been configured, the TAS6424-Q1 operates correctly, but the fault register must be cleared by the host processor. The fourth command sets the TAS6424-Q1 gain to be appropriate for a 15-V PVDD power rail. This setting ensures that the output reaches its maximum at 15 V. This setting is appropriate for the 14.4-V test level that is used to test the TIDA-00743. Other functions are also controlled in register 0x01: high-pass filter enable, global overtemperature warning control set point, overcurrent level set point, and volume rate. These other functions are maintained at their default values.

The next two commands configure the clocking for the TAS6424-Q1:

```
I2C_Write (I2C_BYTE, TAS1_Addr, 0x02, 0x62);
```

The first clock configuration command sets the pulse width modulator (PWM) frequency to 44 times f_s , where frame sync f_s is the frequency of the LRCLK. The *Output Switch Frequency Option* table of the [TAS6424-Q1](#) data sheet[2] shows that the PWM settings for either a 48-kHz sample rate or a 96-kHz sample rate results in a PWM frequency of 2.11 MHz when bits 6 through 4 of register 0x02 are set to 110, or 6_n . The other functions in register 0x02 are set for their defaults.

```
I2C_Write (I2C_BYTE, TAS1_Addr, 0x03, 0x84);
__delay_cycles(100000);
```

The second clock configuration command sets the TAS6424-Q1 sampling rate to 96 kHz. This register also sets the input format to I²S, which is the default setting. There are two other settings in this register that are applicable only for TDM mode, which is not used in the TIDA-00743 design. The clock configuration is followed by a slight delay to ensure that the TAS6424-Q1 clocks are working correctly before enabling the output.

At this point, the TAS6424-Q1 is operating correctly and the volume must be turned up. The gain setting has no effect because the four outputs are muted. Before setting the TAS6424-Q1 for a normal output volume, the four channel gains are set for a very low value. Each channel has its own register for setting gain, so four register writes are made to set all channels for the same gain:

```
I2C_Write (I2C_BYTE, TAS1_Addr, 0x05, 0x0f);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x06, 0x0f);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x07, 0x0f);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x08, 0x0f);

__delay_cycles(1000000);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x04, 0x00);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x05, 0xd1);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x06, 0xd1);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x07, 0xd1);
I2C_Write (I2C_BYTE, TAS1_Addr, 0x08, 0xd1);
```

The setting 0x0f corresponds to an output gain of –96 dB. A delay of one second is included to ensure that there is no audible pop on the outputs. The outputs are then un-muted and set for a gain of 0xd1, or +1 dB. This value is chosen to drive the audio output to reach 10% THD + N when PVDD is 14.4 V.

A final command, LPM0, sets the MSP430 MCU into a low-power standby state.

3 System Setup and Test

3.1 Hardware Setup

Two electrical setups are used to test the TIDA-00743 design: one for bench testing of operation and one for EMI testing.



3.1.1 Bench Test Setup

The primary test setup is used to characterize most of the operation parameters of the TIDA-00743 design. The TIDA-00743 module board is soldered to the carrier board defined in [节 2.4.1.6.3](#). The temperature of the TAS6424-Q1 device increases during normal operation, so a heat sink must be provided to ensure that the TAS6424-Q1 does not overheat before reaching full output power. [图 15](#) shows the TIDA-00743 module board with a heat sink. This screenshot also shows how the module board attaches to the carrier board.



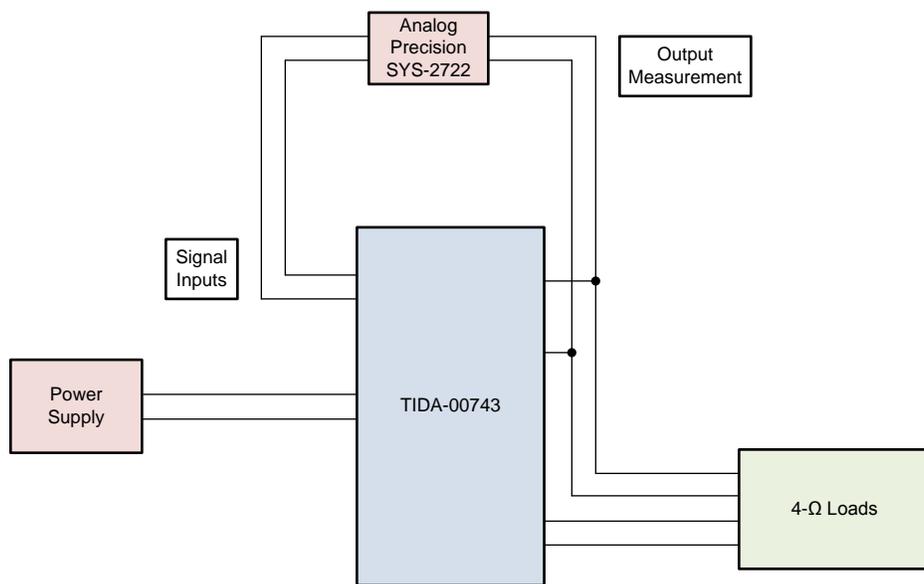
图 15. TIDA-00743 Module Board With Heat Sink Attached to Carrier Board

图 16 shows another view of the boards and the connectors on the carrier board. From left to right are the speaker outputs, the analog audio signal inputs, and the power input.



图 16. Connections for TIDA-00743 Assembly

图 17 是一个示意图，展示了如何对 TIDA-00743 设计进行电气连接。测试所用的电源必须能够提供 20V 的输出电压，且输出电流为 10A。在连接所有线路之前，必须关闭电源。输出负载必须能够耗散至少两倍于 TAS6424-Q1 的输出功率。测试中使用了若干个 100W、4Ω 的非感性电阻作为负载。使用 Audio Precision SYS-2722 提供音频信号输入并测量输出功率和 THD+N。SYS-2722 的输出连接到待测通道的输入端，而 SYS-2722 的输入端则连接到负载电阻，以测量输出功率和 THD。对于需要同时驱动所有四个通道的测试，输入端应连接在一起，使所有输入端接收相同的信号电平。使用数字万用表 (DMM) 测量电源输入端的直流电流和电压。



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图 17. Test Setup Block Diagram for Power Output and THD Tests

3.1.2 EMI Test Setup

For EMI performance testing, the TIDA-00743 design must be enclosed in a Faraday cage to ensure low emissions. 图 18 shows the TIDA-00743 and carrier board with the metal lid that forms the enclosure. The lid is part of a bud CU-234 box mentioned in section 节 2.4.1.6.3. Before connecting the board assembly to the box, resistors R9, R10, and R14 are populated with 0-Ω resistors to short all of the inputs together. The addition of these resistors allows driving the board with one input signal.

The carrier board is designed to attach to the bottom of the bud box in the place of the lid that comes with the box. The two nuts and bolts shown on the edge of the box (see 图 18) hold the module board to the side of the box to provide a heat sink for the TAS-6424-Q1 device. The copper tape around the bottom edge of the box completes the ground seal between the carrier board and the box.

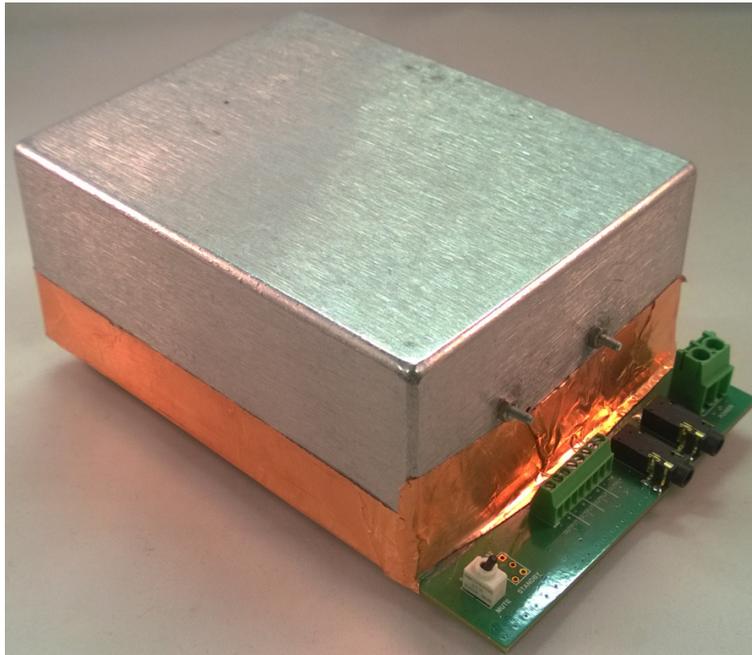
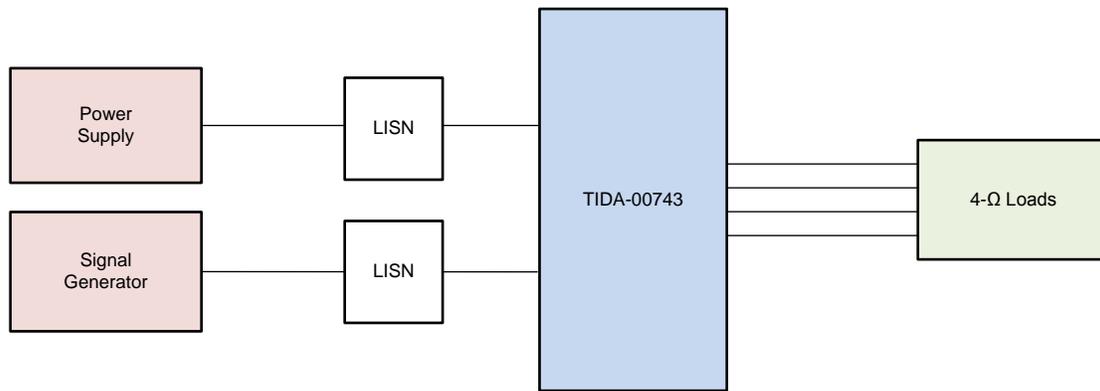


图 18. TIDA-00743 in Metal Box for EMI Tests

图 19 shows the TIDA-00743 electrical connection diagram. Power is provided by a 12-V car battery to ensure that the emissions only originate from the unit under test (UUT) and not from noise generated by the power supply. Power is routed through two line impedance stabilization networks (LISN) in accordance with CISPR 25. 4-Ω resistive loads are connected to the amplifier outputs. The EMI test is performed inside a shielded chamber. The signal generator is placed outside the chamber and the 50-Ω shielded cable for the 1-kHz sine wave test signal is routed through the wall of the chamber. The battery + terminal is connected after all other connections are made so that the system is not powered during test setup.



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图 19. Test Setup Block Diagram for EMI Tests

The two types of EMI tests are conducted emissions and radiated emissions. The conducted emissions test is performed using the voltage method described in CISPR 25. For the conducted emission test, the power wires from the LISNs to the UUT are 200-mm to 400-mm long. The load wires are kept short. Loads are placed close to the UUT. For radiated emissions tests, the loads are placed near the LISNs and the UUT is placed 1.5 m from the loads. 图 20 shows an entire EMI setup for measuring radiated emissions in a test chamber. Both types of test are conducted with the UUT and its loads placed on a 50-mm thick insulator, which is in turn placed on a table with a grounded conductive surface. See the CISPR 25 specification for more details.


图 20. Radiated Emissions Test Setup

3.2 Testing and Results

3.2.1 Power Output, Total Harmonic Distortion, and Noise (THD + N)

The power output and THD + N were tested with the setup described in section 节 3.1.1. The input signal is set for 1 kHz during these tests. 图 21 shows a plot of the THD + N versus power output in watts. The power supply is set to ensure that the voltage delivered at the power input to the board is 14.4 V when the outputs are driven to 10% THD. The outputs reach 10% THD + N at an output of 25.5 W when all channels are driven. If only one channel is driven to 10% THD, the output power can reach as high as 26.5 W. The power output is 21 W per channel at 1% THD + N with all channels driven.

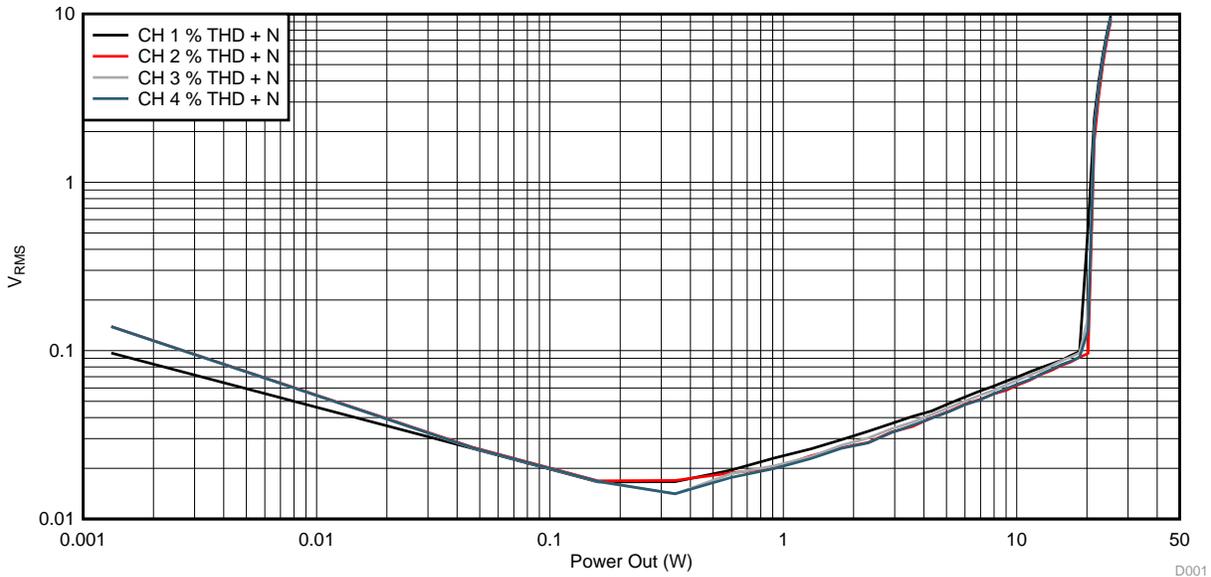


图 21. Power Output (W) versus THD + Noise (%)—Channels Driven Individually

图 22 shows a plot of the frequency response of the system. The frequency response was tested with the output set to 1 W when the input frequency was 1 kHz. This graph shows that the response drops only 0.7 dB_u at 20 Hz and only 0.2 dB_u at 20 kHz.

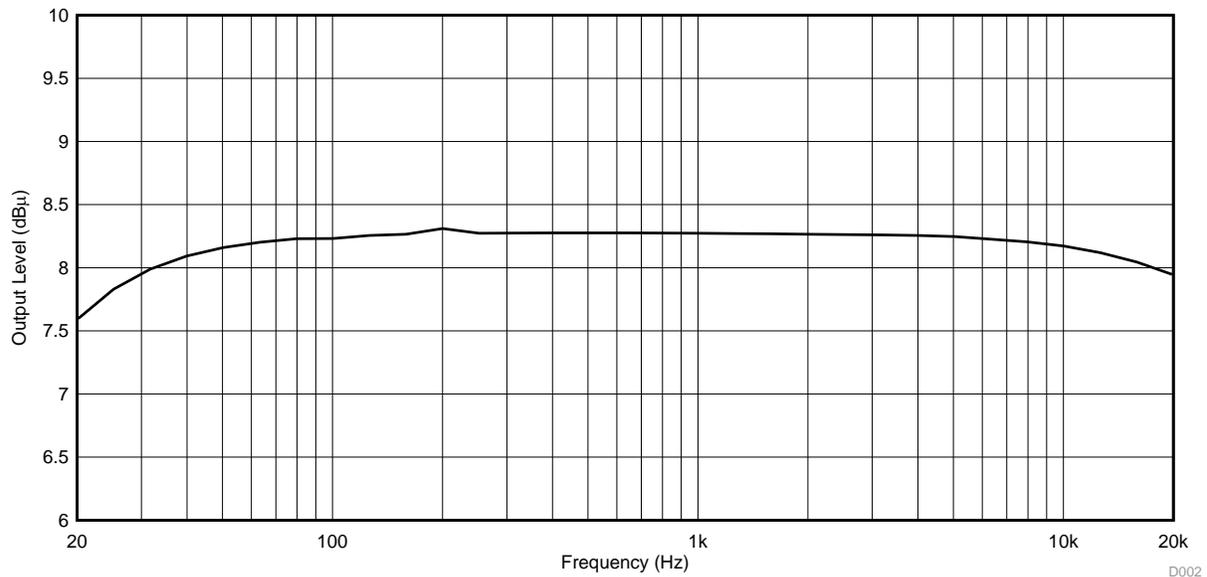


图 22. TIDA-00743 Frequency Response

3.2.2 EMI

3.2.2.1 Conducted Emissions

The EMI tests were run using the test setup described in paragraph 节 3.1.2. The following graphs of the tests show the test limits for CISPR 25 class 5. 图 23 shows the ambient scan for the test setup with the UUT unpowered. 图 24 shows the results for conducted emissions.

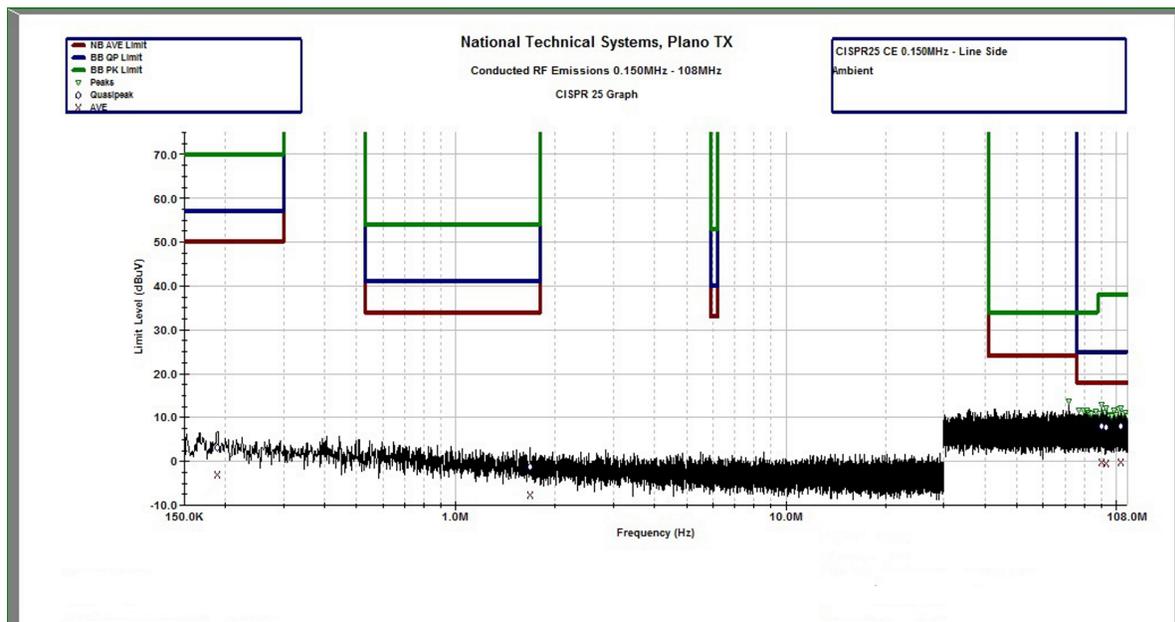


图 23. CISPR 25 Conducted Emissions Ambient Scan

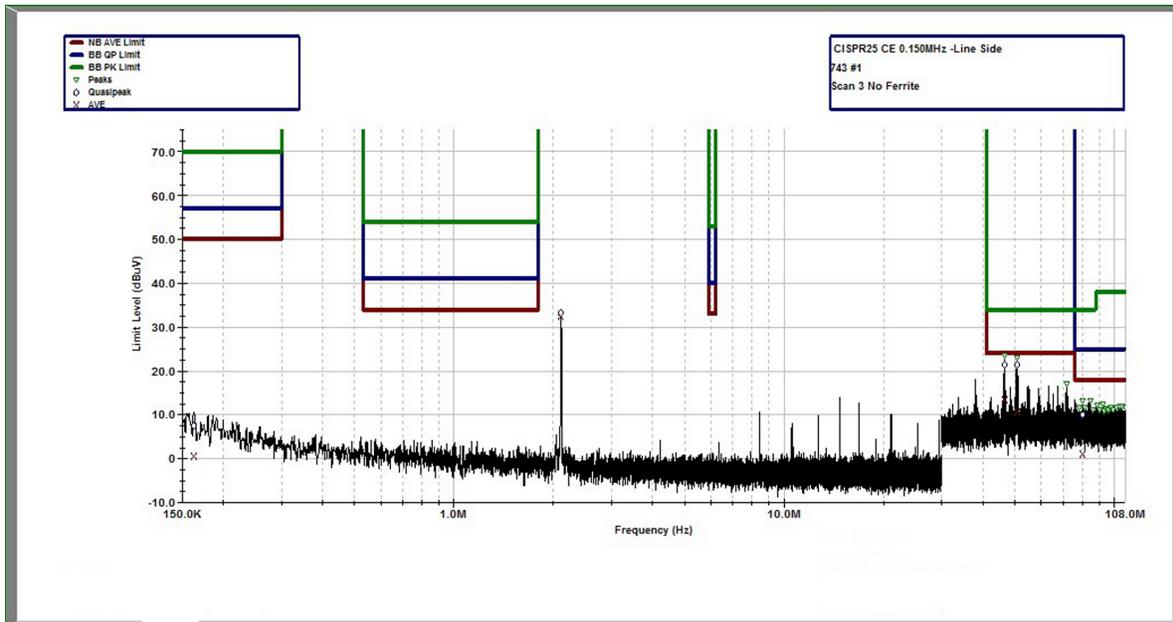


图 24. CISPR 25 Conducted Emissions

The TIDA-00743, when tested as previously described, has 10.5 dB of margin in the conducted emissions test for both average and peak levels.

3.2.2.2 Radiated Emissions

For the radiated emission tests, the UUT is set up as described in paragraph 节 3.1.2. 图 20 shows an example of the setup for radiated emissions testing.

A monopole antenna is used to receive the emissions in the frequency range of 150 kHz to 30 MHz. Only one polarization is measured for this antenna. 图 25 shows the ambient scan of the test setup with the UUT unpowered. 图 26 shows the test results.

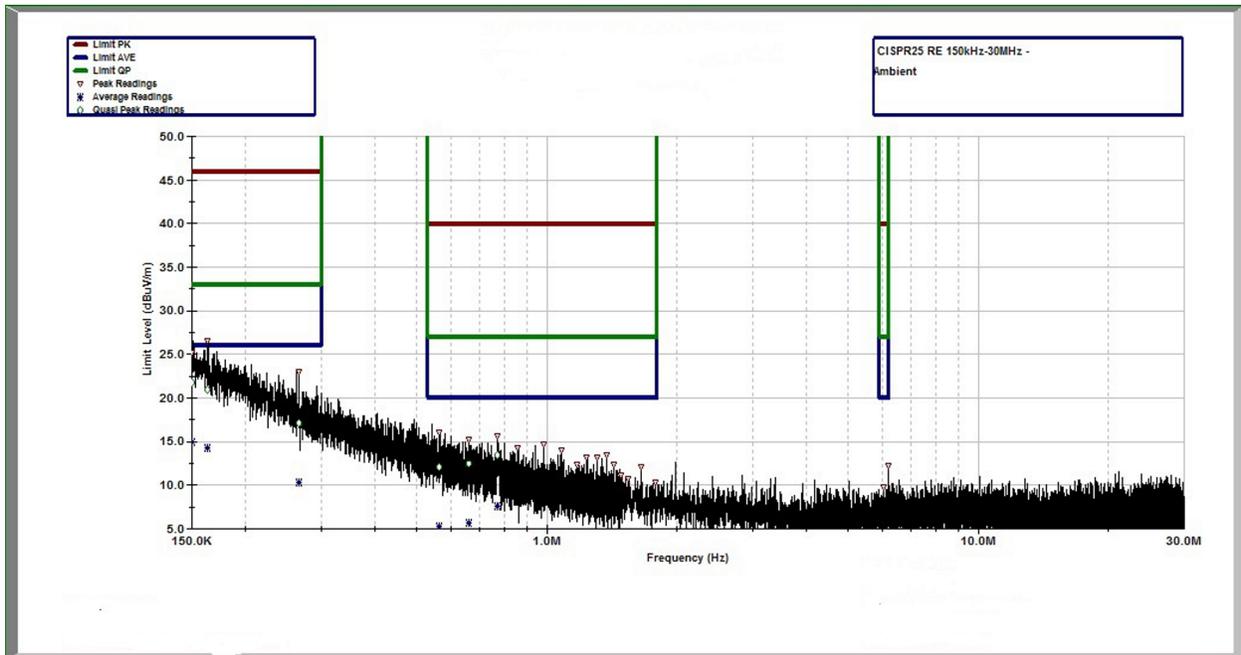


图 25. CISPR 25 Radiated Emissions: 150 kHz to 30 MHz, Ambient

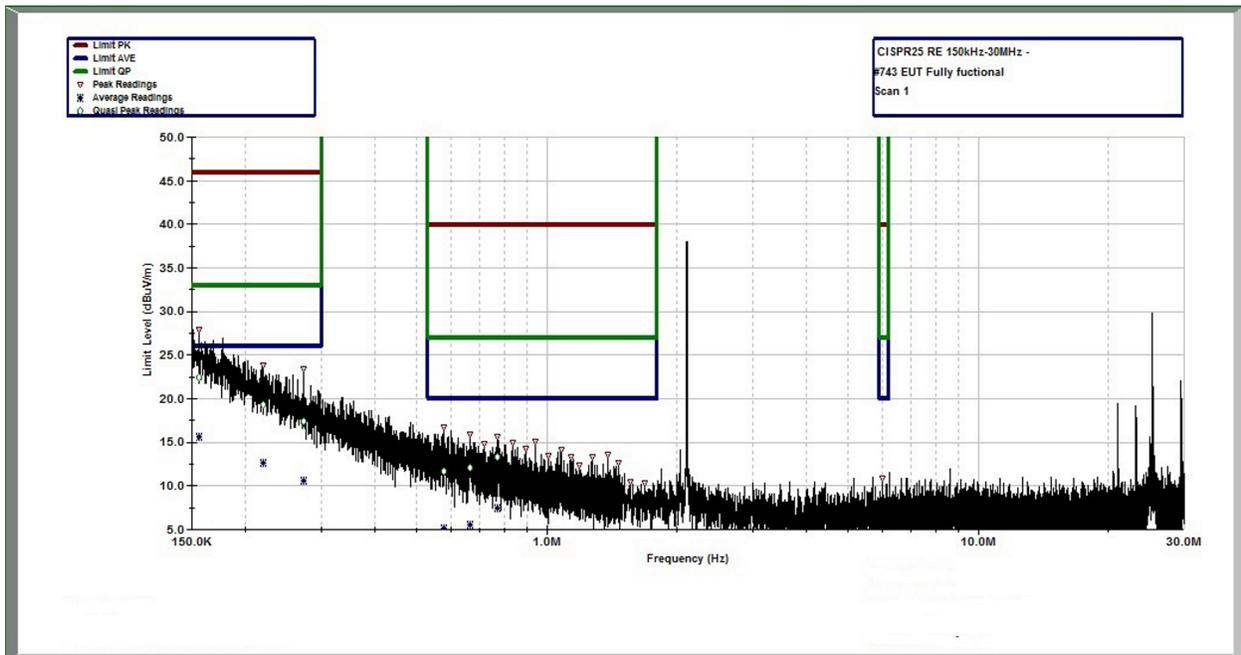


图 26. CISPR 25 Radiated Emissions: 150 kHz to 30 MHz

The average margin in the 150-kHz to 30-MHz range is greater than 10 dB for the whole range.

For the frequency range of 30 MHz to 200 MHz, a biconical antenna is used to measure the emissions. Measurements are made with the antenna polarized both horizontally and vertically. 图 27 和 图 28 show the ambient scans with the UUT power OFF. 图 29 shows the results with the antenna horizontally polarized and 图 30 shows the results with the antenna vertically polarized.

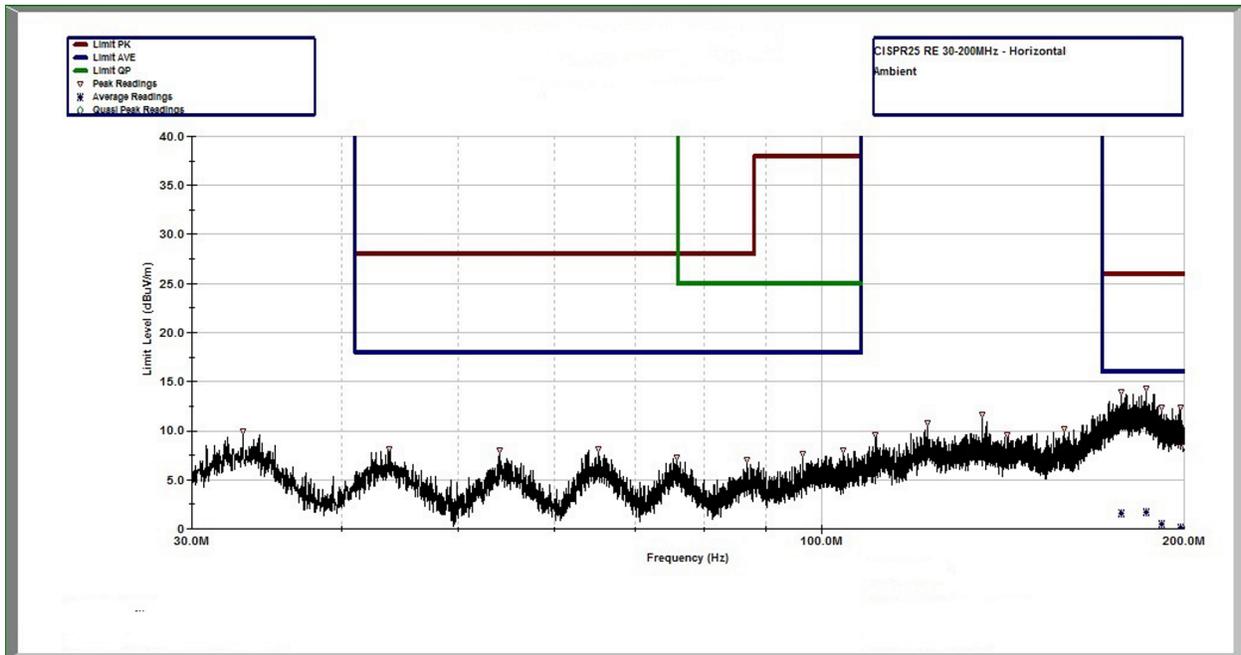


图 27. CISPR 25 Radiated Emissions: 30 MHz to 200 MHz, Horizontal Antenna Orientation, Ambient Scan

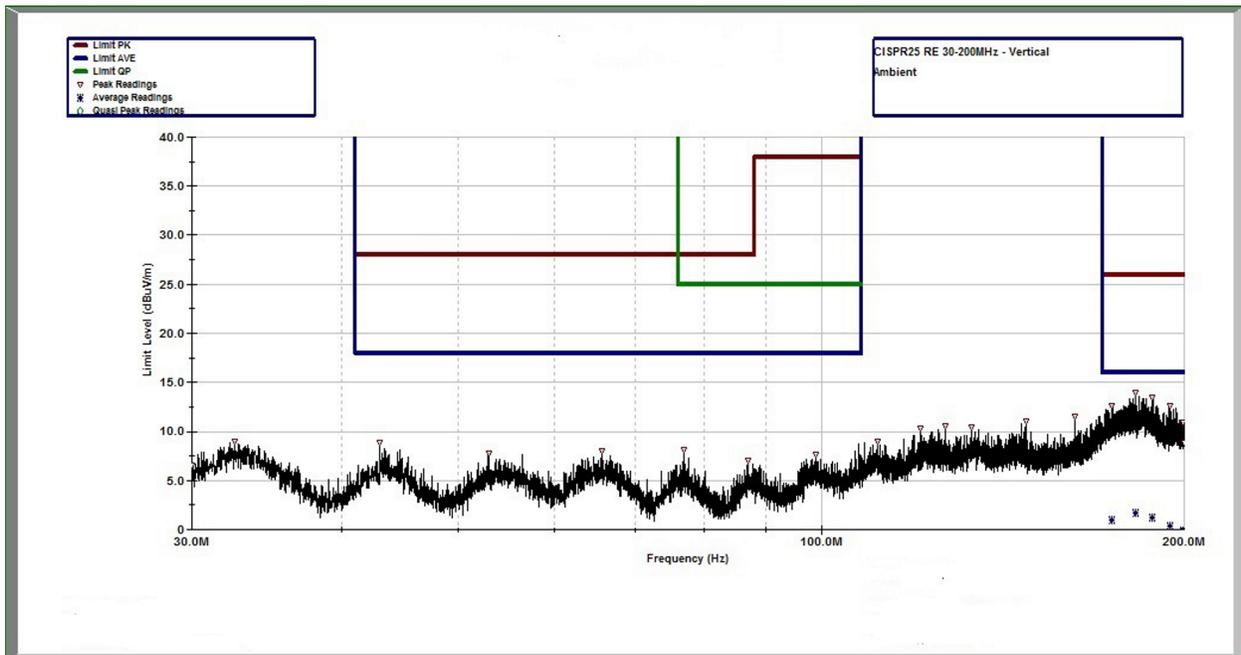


图 28. CISPR 25 Radiated Emissions: 30 MHz to 200 MHz, Vertical Antenna Orientation, Ambient Scan

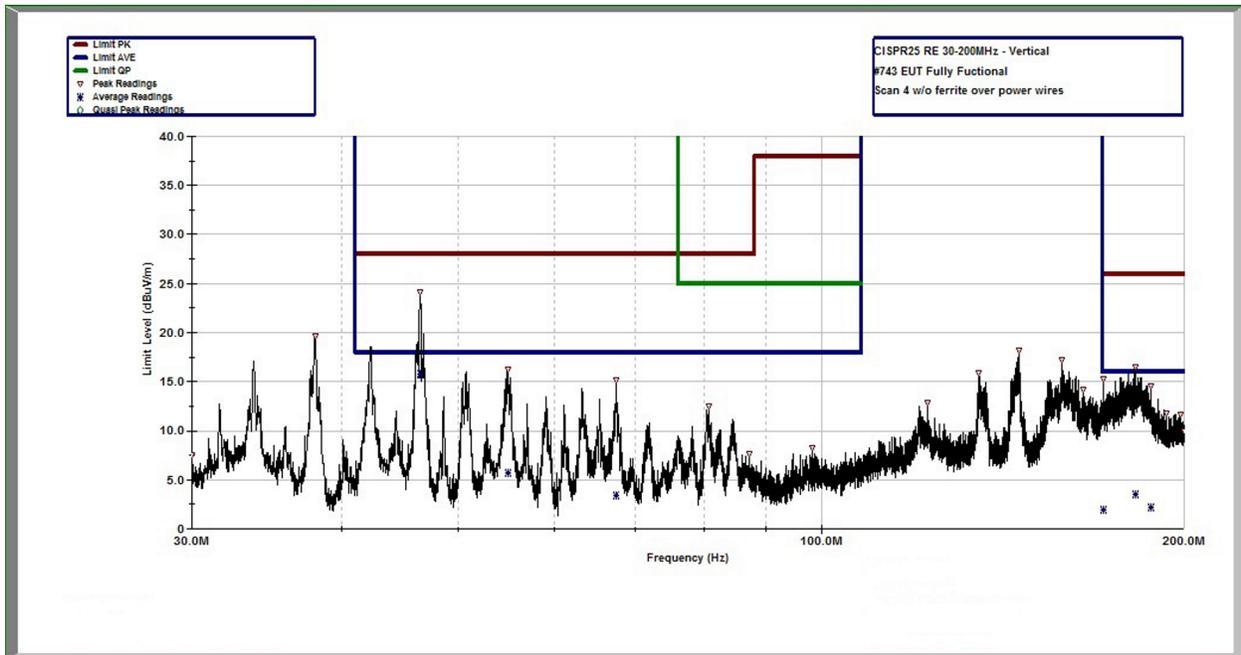


图 29. CISPR 25 Radiated Emissions: 30 MHz to 200 MHz, Horizontal Antenna Orientation

The average margin for the horizontal polarization test is greater than 2.2 dB.

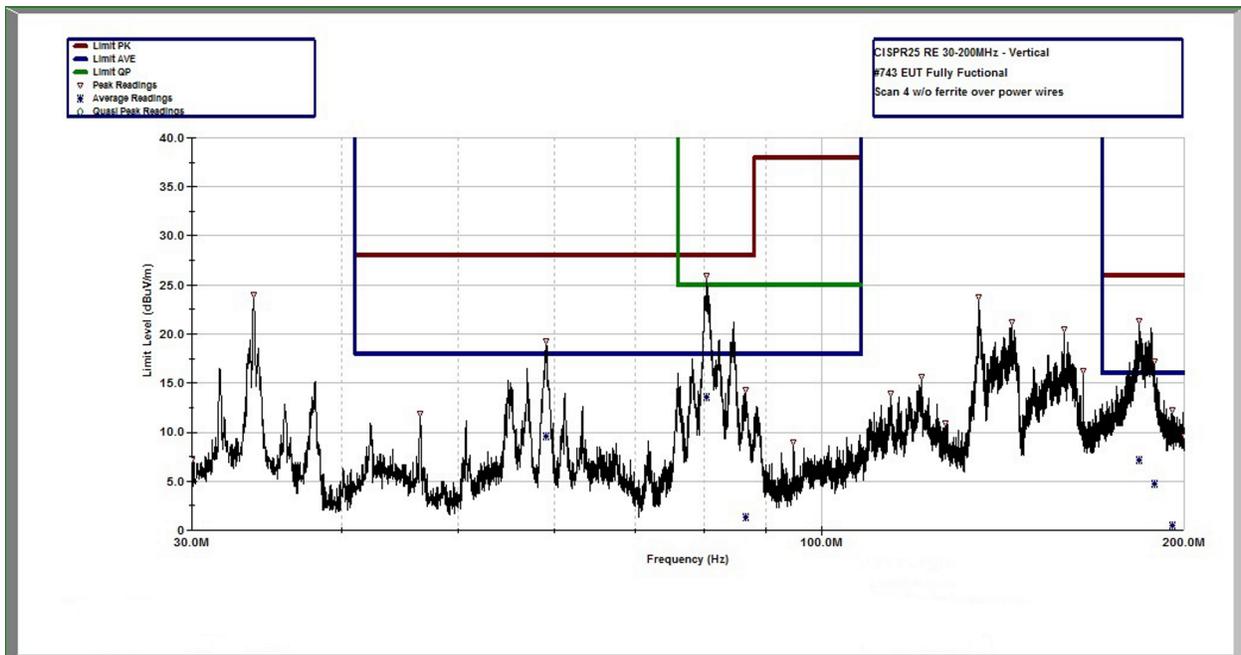


图 30. CISPR 25 Radiated Emissions: 30 to 200 MHz, Vertical Antenna Orientation

The average margin for the vertical polarization test is greater than 4.5 dB.

Emissions in the frequency range from 200 MHz to 1000 MHz are measured with a horn antenna. Both horizontal and vertical polarizations of the antenna are tested. 图 31 and 图 32 show the ambient scan when the UUT power is OFF. 图 33 and 图 34 show the actual system response.

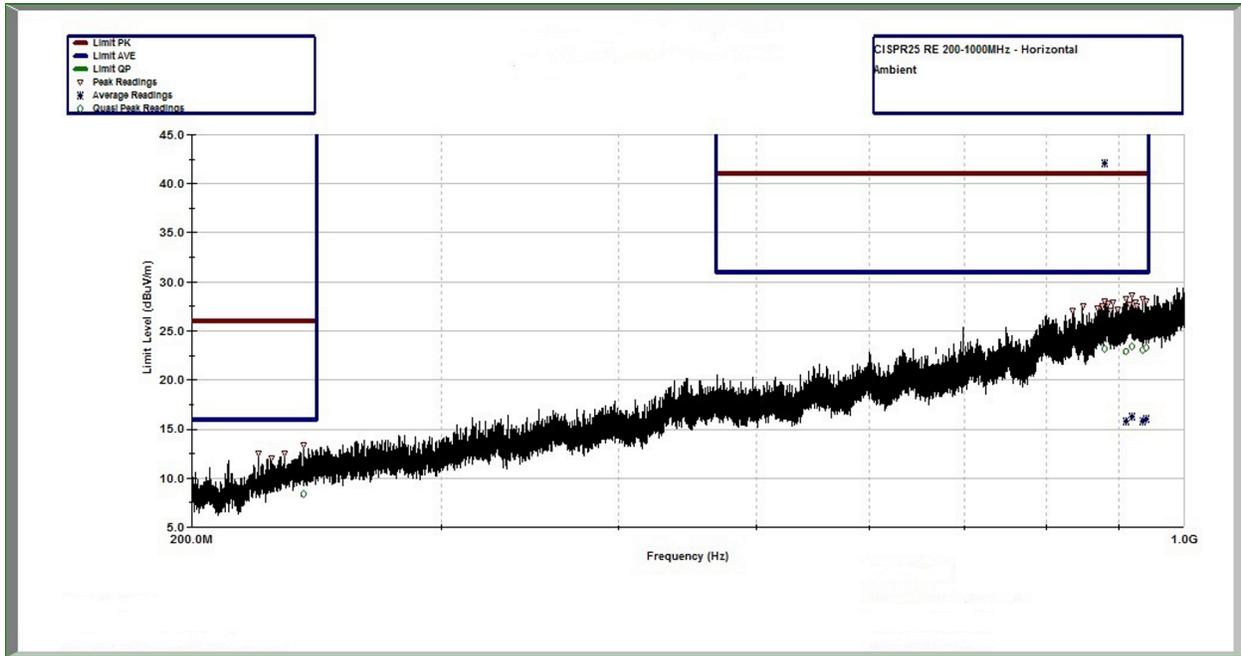


图 31. CISPR 25 Radiated Emissions: 200 MHz to 1 GHz, Horizontal Antenna Orientation, Ambient Scan

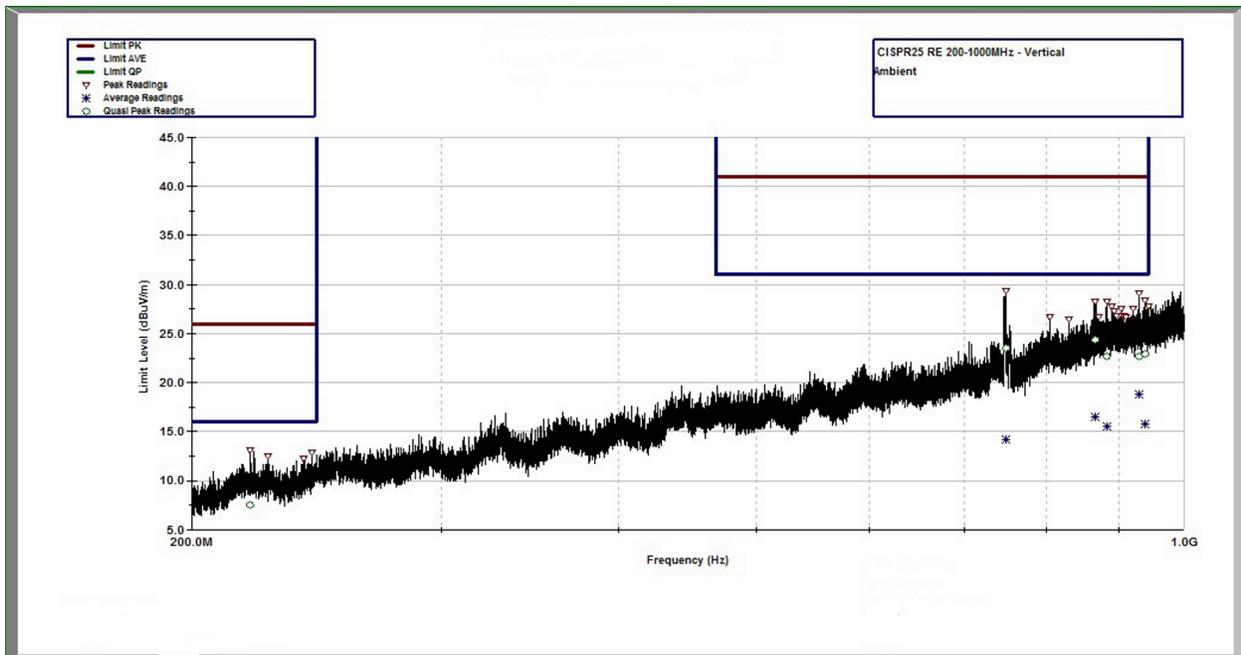


图 32. CISPR 25 Radiated Emissions: 200 MHz to 1 GHz, Vertical Antenna Orientation, Ambient Scan

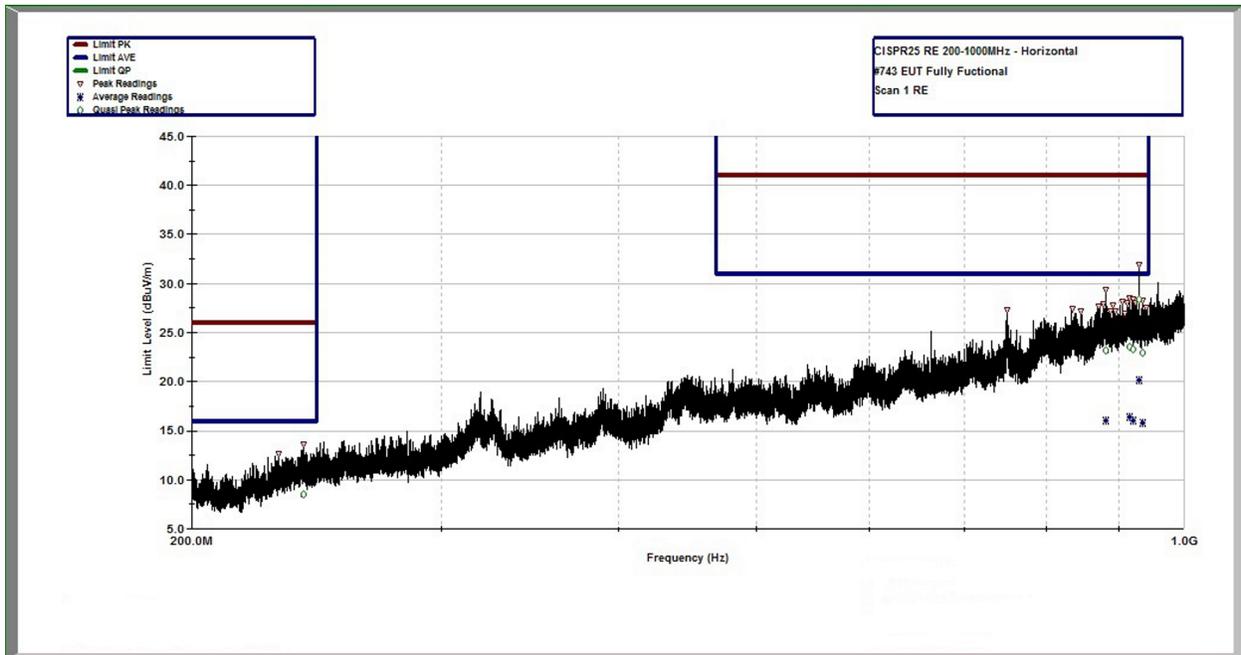


图 33. CISPR 25 Radiated Emissions: 200 MHz to 1 GHz, Horizontal Antenna Orientation

The average margin for the horizontal polarization test is greater than 10.8 dB.

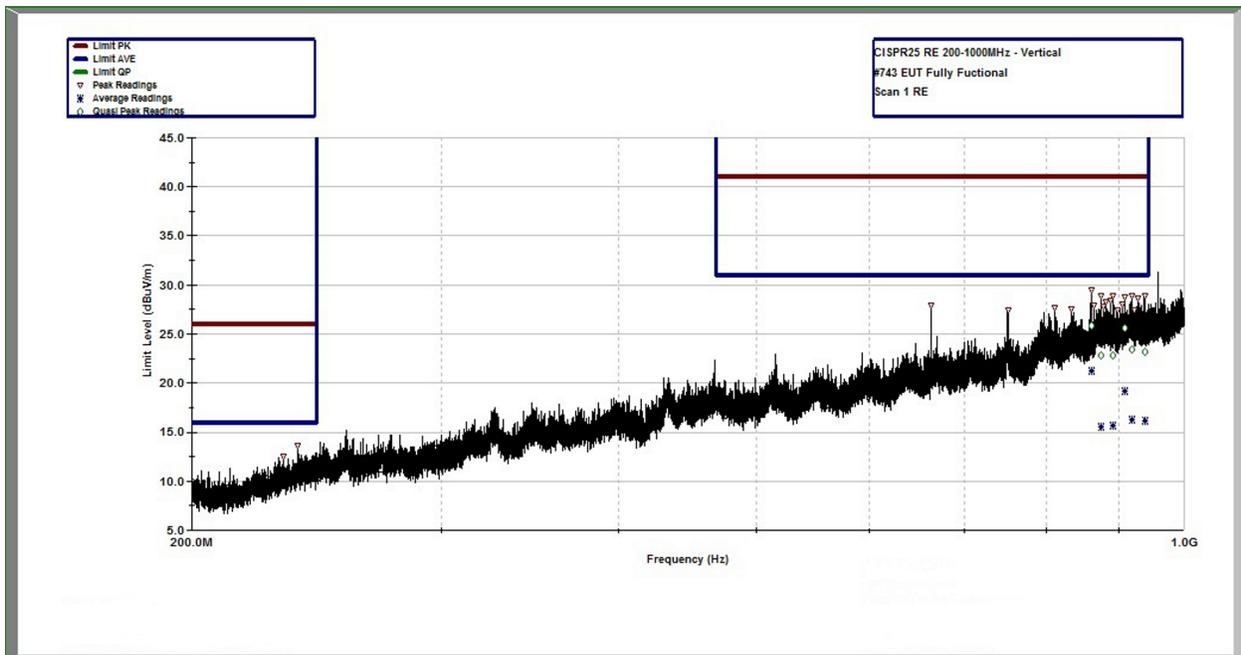


图 34. CISPR 25 Radiated Emissions: 200 MHz to 1 GHz, Vertical Antenna Orientation

The average margin for the vertical polarization test is greater than 11.8 dB.

4 Design Files

4.1 Schematics

To download the schematics, see the design files at [TIDA-00743](#).

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIDA-00743](#).

4.3 PCB Layout Recommendations

The TIDA-00743 module board has a six-layer PCB. Placement of the parts is important. Everything is spaced around U1, the TAS6424-Q1. U1 is close to the center of the board. The output section is oriented toward the main connector to keep the output routing as short as possible while still leaving room for the output filter circuits. The analog portion of U4, the PCM1865-Q1, must be kept away from high-frequency signals and high switching currents as much as possible. U4 is placed close to the audio input pins to reduce the possibility of noise coupling into the inputs. U5, the TPS7B6733-Q1 linear regulator, is placed close to U4 to keep the power routing to U4 short. U3, the MSP430, is placed to the other side of the board from U4. The placement of U3 is not critical in this design.

The PCB design requires careful consideration of signal routing, especially for the power connections. The input power net PVDD supplies approximately 8.5 A upon reaching the maximum audio power output, so the power routing on the board must be capable of supplying that current. PVDD is routed on layers 1, 3, 4, and 6 to ensure a low impedance for PVDD. At any place where PVDD is to be used by either U1 or U5, multiple vias are provided to maintain a low impedance. The extra vias are especially necessary for U1 pins 29, 30, 42, 43, 55, and 56. These pins are the source of the output current for the TAS6424-Q1. Layers 2 and 5 are ground planes. In addition to the two planes, unrouted areas on layers 1, 3, 4, and 6 are filled with ground. This ground fill is intended to help with EMI shielding and to help dissipate heat from U5. The net 3V3_OUT is routed with a wide trace from U5 to C71 and R40. From R40, net +3P3V is routed primarily on layers 3 and 4 with a 30-mil (0.76-mm) wide trace. The routing of the audio input signals is kept as short as possible and kept as far apart as possible to reduce crosstalk. The signals for front left and rear left are routed on the top layer, while front right and rear right are routed on the bottom layer. Signals SCLK, DOUT, DOUT2, and LRCLK are routed on layer 3 to reduce the chances for EMI to radiate from the signals. MCLK is generated by U2 very close to where it connects to U1, so it is routed on the surface layers. None of the other traces are very critical.

4.3.1 Layout Prints

To download the layer plots, see the design files at [TIDA-00743](#).

4.4 Altium Project

To download the Altium project files, see the design files at [TIDA-00743](#).

4.5 Gerber Files

To download the Gerber files, see the design files at [TIDA-00743](#).

4.6 Assembly Drawings

To download the assembly drawings, see the design files at [TIDA-00743](#).

5 Software Files

To download the software files, see the design files at [TIDA-00743](#).

6 Related Documentation

1. Texas Instruments, [MIXED SIGNAL MICROCONTROLLER](#), MSP430G2xx2 Data Sheet (SLAS723)
2. Texas Instruments, [TAS6424-Q1 75-W, 2-MHz Digital Input 4-Channel Automotive Class-D Audio Amplifier With Load-Dump Protection and fC Diagnostics](#), TAS6424-Q1 Data Sheet

6.1 商标

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7 About the Author

MARK KNAPP is a Systems Architect at Texas Instruments Incorporated who specializes in automotive premium audio systems and instrument clusters. He also has an extensive background in video camera systems and infrared imaging systems for military, automotive, and industrial applications. Mark earned his BSEE at the University of Michigan-Dearborn and his MSEE at the University of Texas at Dallas.

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