TI 设计：TIDA-01428
采用 CAN 的汽车分立式 SBC 预降压、后升压参考设计

说明

TIDA-01428 参考设计实施了一款分立式系统基础芯片 (SBC)，其中依次配有一个可实现 1A 电流和 3.3V 电压的宽输入电压降压转换器以及一个紧凑型低输入电压 5V 固定升压转换器，该设计可为控制器局域网 (CAN) 物理层接口供电。此设计已使用电压方法进行 CISPR 25 辐射发射和传导发射测试，并在 CAN 通讯以 500KBPS 的速率下运行时，按照 ISO 11452-4 标准进行抗大电流注入 (BCI) 测试。TIDA-01428 包含经过 EMC 审查的电源树和 CAN 参考设计，可用于许多汽车应用。

资源

TIDA-01428	设计文件夹
LM53601-Q1	产品文件夹
TPS61240-Q1	产品文件夹
TMS320F28030PAGQ	产品文件夹
TCAN1042V-Q1	产品文件夹
SN74LVC2G06-Q1	产品文件夹
CSD17313Q2	产品文件夹

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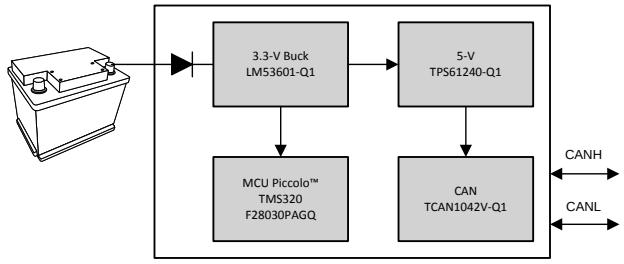
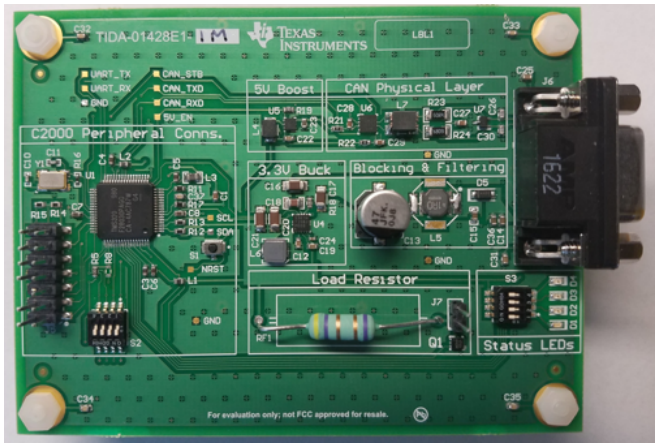
特性

- 宽输入电压，3.3V 固定降压转换器
- 低输入电压，5V 固定升压转换器
- 具有高达 5MBPS 灵活数据速率 (FD) 的 CAN 收发器
- 通过了 CISPR 25 4 类辐射发射测试
- 通过了 CISPR 25 4 类传导发射测试
- 通过了 ISO 11452-4 大电流注入测试
- 能够承受高达 42V 的负载突降电压
- 通过将电池输入电压降至 4.3V 来维持稳定的 3.3V 和 5V 电源

应用范围

- 汽车车身控制模块 (BCM)
- 汽车前置摄像机
- 汽车音响主机





该 TI 参考设计末尾的重要声明表述了授权使用、知识产权问题和其他重要的免责声明和信息。

1 System Description

A regulated 3.3-V main supply rail and a lower current regulated 5-V supply rail for just a CAN interface is becoming a more and more prevalent requirement in automotive as more microcontrollers (MCUs) transition from 5 V to 3.3 V. Additionally, the necessity to handle low-input voltage transients for start and stop applications is also becoming a more common requirement.

This reference design is an example implementation of how to create a 1-A, 3.3-V supply and a 240-mA, 5-V supply that can handle battery input voltages down to 4.3 V. Example modules where this power topology and CAN interface can be applicable include body control modules (BCMs), multi-mode radar modules, front camera modules, and head unit modules.

This TI Design passes Class 4 radiated emissions, Class 4 conducted emissions using the voltage method on both VBATT and GND, and ISO 11452-4 with greater than 106 dBµA of immunity routing VBATT, GND, CANH, and CANL through the current injection probe.

A SBC is an integrated circuit (IC) that combines many typical building blocks of a system, which includes transceivers, linear regulators, and switching regulators. While these integrated devices can offer size and cost savings in a number of applications, the integrated devices do not work in every case. For applications where an SBC is not a good fit, it might be beneficial to build a discrete implementation of these aforementioned building blocks thus making a *discrete SBC*.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER	SPECIFICATIONS	DETAILS
Input power source (VBATT)	Automotive 12-V battery system	节 2.3.1
Operational Input voltage range (VBATT)	4.3 V to 36 V	节 2.3.2
Survivable input voltage range (VBATT)	–40 V to 42 V	节 2.3.1
Regulated output voltages	3.3 V and 5 V	节 2.3.2 and 节 2.3.3
Maximum 3.3-V load current	1000 mA	节 2.3.2
Maximum 5-V load current	240 mA	节 2.3.3
Form factor	Rectangular, 4.0" × 3.0" (101.6 mm × 76.2 mm), 2-layer, 1-oz copper foil, printed circuit board (PCB)	节 3.1.1.1 and 4.3 节

2 System Overview

2.1 Block Diagram

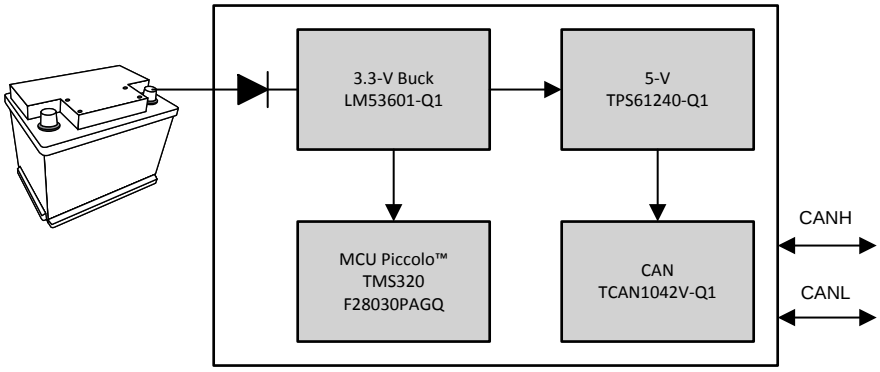


图 **1. TIDA-01428 Block Diagram**

2.2 Highlighted Products

The TIDA-01428 TI Design features the following six devices:

1. LM53601-Q1: Automotive, wide-input voltage, synchronous, step-down, DC-DC converter
2. TPS61240-Q1: Automotive, high-efficiency, low-input voltage, synchronous, step-up, DC-DC converter
3. TCAN1042V-Q1: Automotive, fault-protected, CAN transceiver with CAN FD and IO level shifting
4. TMS320F28030Q: Automotive, high-efficiency 32-bit Piccolo™ MCU
5. SN74LVC2G06-Q1: Automotive, catalog, dual inverter buffer and driver with open-drain output
6. CSD17313Q2: 30-V, N-channel, NexFET™ power MOSFET

For more information on each of these devices, see their respective datasheets in 5 节 or product folders on www.ti.com.

2.2.1 LM53601-Q1

The LM53601NQDSXRQ1 device is a synchronous buck regulator that is optimized for automotive applications and provides a fixed 3.3-V output voltage with load currents up to 1000 mA. Advanced high-speed circuitry allows the LM53601-Q1 to regulate from an input of 18 V to an output of 3.3 V at a fixed frequency of 2.1 MHz. Innovative architecture allows the device to regulate a 3.3-V output from an input voltage of only 3.8 V up to 36 V with transient tolerance of up to 42 V.

An open-drain, reset output with filtering and delayed release provides a true indication of system status. This feature reduces the necessity for additional supervisory components, which saves cost and board space. Seamless transitions between pulse width modulation (PWM) and pulse frequency modulation (PFM) modes, along with a quiescent current of only 23 μA, ensures high efficiency and superior transient response at all loads. The device requires only a few external components, which enables a compact solution size. While the LM53601-Q1 devices are Q1-rated, electrical characteristics are guaranteed across a junction temperature range of –40°C to 150°C.

图 2 shows a block diagram of the device.

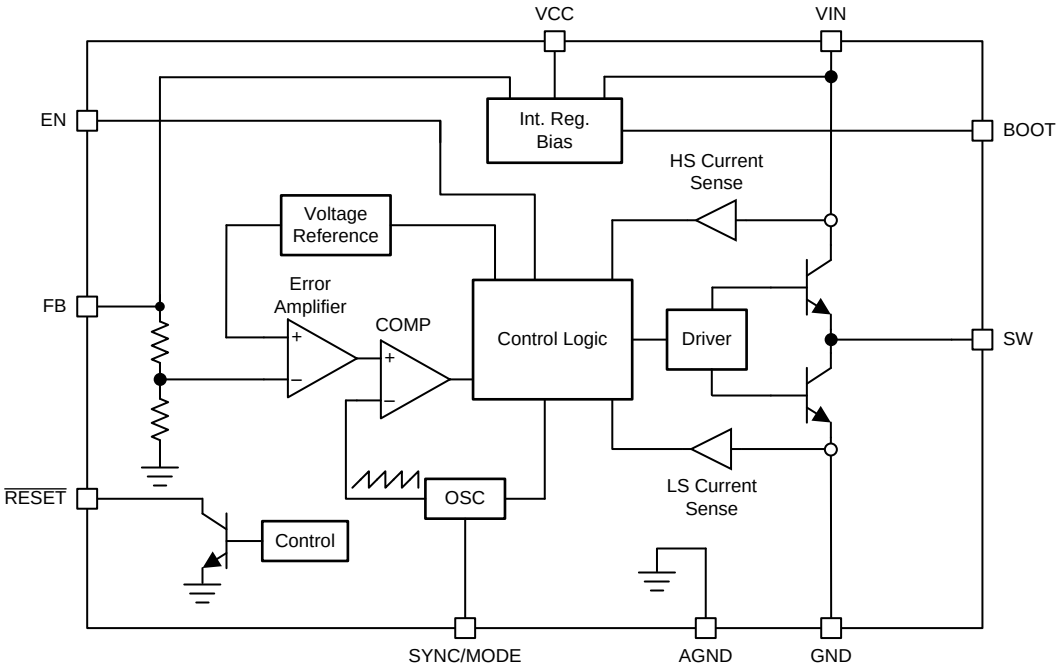


图 2. LM53601-Q1 Block Diagram

Additional features:

- AEC-Q100 qualified for automotive applications
- –40°C to 150°C junction temperature range
- Wide operating input voltage: 3.55 V to 36 V (with transient to 42 V)
- 2.1-MHz fixed switching frequency with optional spread spectrum switching
- Low quiescent current: 23 μA
- Shutdown current: 1.8 μA
- Adjustable, 3.3-V, or 5-V output variants
- 650-mA or 1000-mA versions
- Pin selectable forced PWM mode
- RESET output with filter and delay release
- External frequency synchronization
- Internal compensation, soft start, current limit, and UVLO
- 10-lead, 3-mm × 3-mm SON package with wettable flanks

2.2.2 TPS61240-Q1

The TPS61240-Q1 device is a high-efficiency, synchronous, step-up (boost) DC-DC converter with an input valley current limit of 500 mA. The device provides a fixed output voltage of 5 V with an input voltage range of 2.3 V to 5.5 V. The TPS61240-Q1 also supports batteries with extended voltage ranges up to 7 V through an overvoltage shutdown mode where the output is disabled. This protection feature disables the output when input voltages rise above 6 V, which in turn protects downstream devices from higher, overvoltage conditions.

During shutdown, the load is completely disconnected from the battery. The TPS61240-Q1 boost converter is based on a quasi-constant, on-time valley current mode control scheme. The TPS61240-Q1 presents a high impedance at the VOUT pin when shut down. This high impedance allows for use in applications that require the regulated output bus to be driven by another supply while the TPS61240-Q1 is shut down. During light loads the device will automatically pulse skip, which allows maximum efficiency at lowest quiescent currents. In the shutdown mode, the current consumption is reduced to less than 1 μA.

TPS61240-Q1 allows the use of a small inductor and capacitors to achieve a small solution size. The TPS61240-Q1 is available in a 2-mm × 2-mm WSON package.

图 3 shows a block diagram of the device.

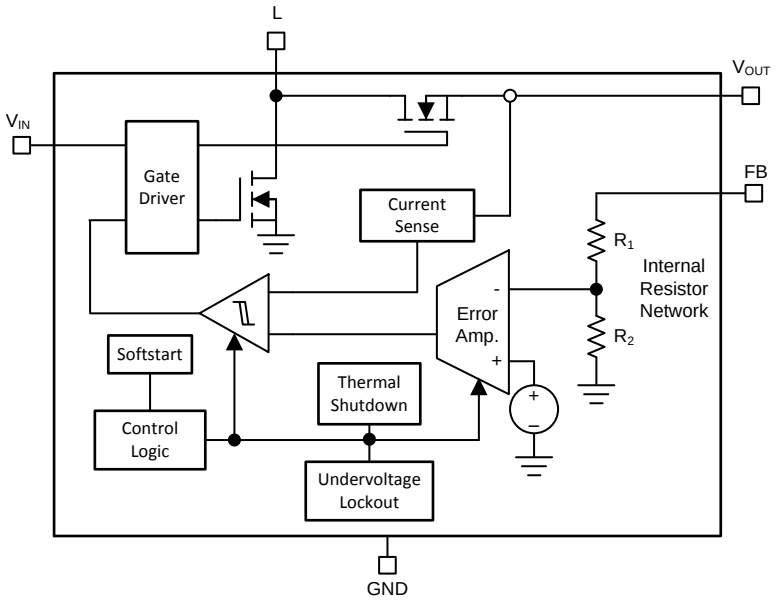


图 **3. TPS61240-Q1 Block Diagram**

Additional features:

- AEC-Q100 qualified for automotive applications
- >90% efficiency at normal operating conditions
- Total DC output voltage accuracy of 5 V ±2%
- 30-µA typical quiescent current
- Input voltage range from 2.3 V to 5.5 V
- Automatic PFM and PWM mode transitions
- Low-ripple, power save mode for improved light-load performance
- Internal 250-µs typical soft start
- 3.5-MHz typical operating frequency
- Load disconnect during shutdown
- Current overload, overvoltage, and thermal shutdown (TSD) protection
- Only three external surface-mount components required for a < 13-mm² solution size
- Available in a 2-mm × 2-mm WSON package

2.2.3 TCAN1042V-Q1

The TCAN1042 family is a CAN transceiver family that meets the ISO11898-2 (2016), high-speed, CAN physical layer standard. All devices are designed for use in CAN FD networks up to 2 Mbps (megabits per second). Devices with part numbers that include the *G* suffix are designed for data rates up to 5 Mbps, and versions with the *V* have a secondary power supply input for IO level, which shifts the input pin thresholds and RXD output level. This family has a low-power standby mode with remote wake request feature. Additionally, all devices include protection features to enhance device and network robustness, which include a TXD dominant state timeout, thermal shutdown, undervoltage lockout, short circuit current limiting, and internal pull ups for critical floating input terminals.

图 4 shows a block diagram of the device.

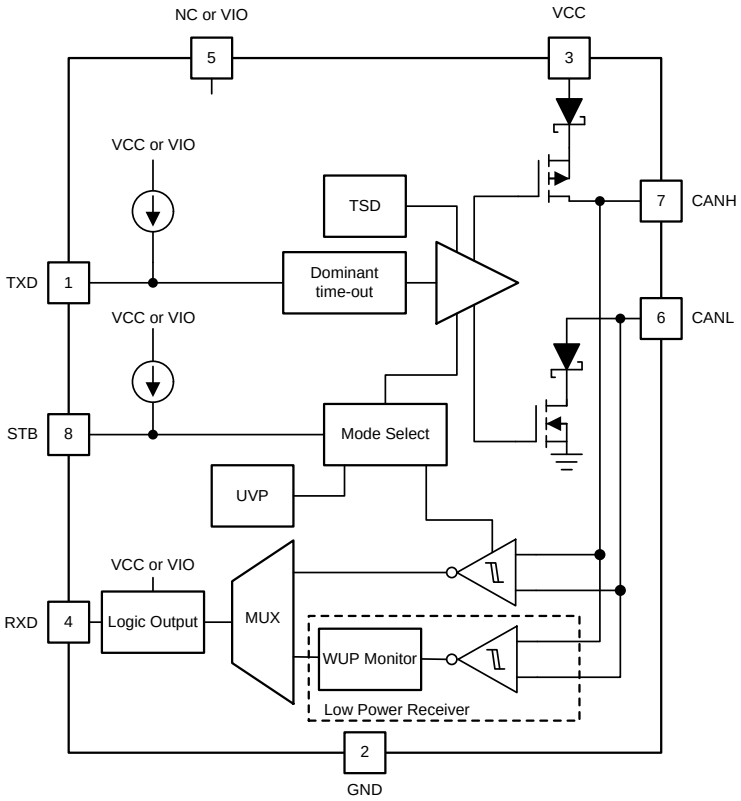


图 4. TCAN1042-Q1 Family Block Diagram

Additional features:

- AEC-Q100 qualified for automotive applications
- Meets the ISO 11898-2:2016 and ISO 11898-5:2007 physical layer standards
- All devices support classic CAN and 2 Mbps CAN FD and *G* options support 5 Mbps
- Short and symmetrical propagation delay times and fast loop times for enhanced timing margin
- IO voltage range supports 3.3-V and 5-V MCUs
- Ideal passive behavior when unpowered
- IEC electrostatic discharge (ESD) protection up to ±15 kV
- Bus fault protection: ±58 V (non-H variants) and ±70 V (H variants)
- Undervoltage protection on V_{CC} and V_{IO} (V variants only) supply terminals
- Driver dominant time out (TXD DTO) supporting data rates down to 10 kbps
- TSD protection
- Receiver common mode input voltage: ±30 V
- Typical loop delay: 110 ns
- Junction temperatures from –55°C to 150°C
- Available in SOIC(8) package and leadless VSON(8) package (3 mm × 3 mm) with automated optical inspection (AOI) capability

2.2.4 TMS320F28030PAGQ

The F2803x Piccolo family of MCUs provides the power of the C28x core and control law accelerator (CLA) coupled with highly-integrated control peripherals in low pin-count devices. This family is code-compatible with previous C28x-based code and also provides a high level of analog integration. An internal voltage regulator allows for single-rail operation. High-resolution PWM (HRPWM) enhancements allow for dual-edge control (frequency modulation). Analog comparators with internal, 10-bit references have been added and can be routed directly to control the PWM outputs. The analog-to-digital converter (ADC) converts from 0 to 3.3-V fixed, full-scale range and supports ratio-metric VREFHI and VREFLO references.

图 5 shows a block diagram of the device.

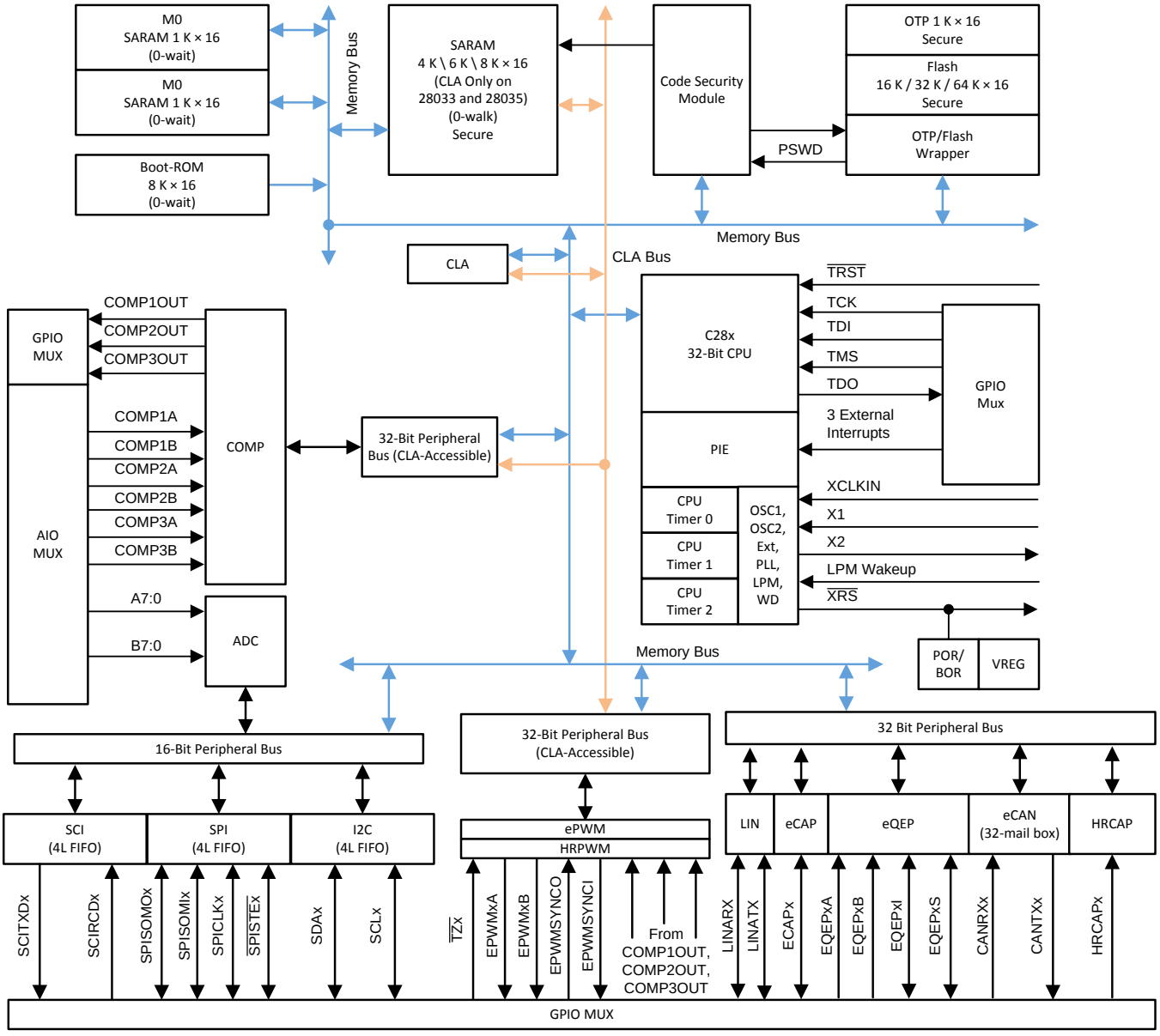


图 5. TMS320F28030PAGQ Block Diagram

- 60 MHz, 32-bit, floating-point, high-efficiency, CPU (TMS320C28x)
- 128-Bit security key and lock
- Single 3.3-V supply with no power sequencing requirement
- Integrated power-on reset and brown-out reset
- Clocking: two internal zero-pin oscillators, on-chip crystal oscillator, and external clock input
- Up to 45 individually programmable, multiplexed general purpose input output (GPIO) pins with input filtering
- Peripheral interrupt expansion (PIE) block that supports all peripheral interrupts
- Three 32-bit CPU timers and a watchdog timer module

- On-chip Flash, SARAM, OTP, and boot ROM available
- Serial port peripherals:
  - One serial communications interface (SCI) universal asynchronous receiver/transmitter (UART) module
  - Two serial peripheral interface (SPI) modules
  - One inter-integrated-circuit (I2C) module
  - One local interconnect network (LIN) module
  - One enhanced controller area network (eCAN) module
- Enhanced control peripherals:
  - ePWM
  - HRPWM
  - Enhanced capture (eCAP) module
  - High-resolution input capture (HRCAP) module
  - Enhanced quadrature encoder pulse (eQEP) module
  - ADC
  - On-chip temperature sensor
  - On-chip comparator
- Available in 56-pin VQFN, 64-pin TQFP, and 80-pin LQFP packages

2.2.5 SN74LVC2G06-Q1

The SN74LVC2G06-Q1 is a dual-inverter buffer and driver IC that is designed for 1.65-V to 5.5-V VCC operation. The SN74LVC2G06-Q1 device has an open-drain output that can be connected to other open-drain outputs to implement active-low, wired-OR or active-high, wired-AND functions. The maximum sink current is 32 mA. This device is fully specified for partial-power-down applications using I_{off} circuitry. This I_{off} circuitry disables the outputs, which in turn prevents damaging backflow current through the device when the device is powered down but voltage remains on the output (or outputs).

图 6 shows a block diagram of the device.

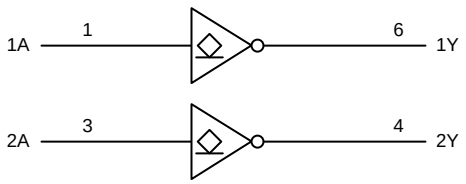


图 6. SN74LVC2G06-Q1 Block Diagram

Additional features:

- AEC-Q100 qualified for automotive applications
- Supports 1.65-V to 5.5-V V_{CC} operation
- Maximum t_{pd} of 3.4 ns at 3.3 V
- Low power consumption, 10 µA maximum
- ±24 mA output drive at 3.3 V

- Inputs and open-drain outputs accept voltages up to 5.5 V
- ESD protection exceeds 2-kV human-body model, 200-V machine model, and 1-kV charged-device model

2.2.6 CSD17313Q2

The CSD17313Q2 is a 30-V, 24-mΩ, 2-mm × 2-mm SON NexFET power MOSFET is designed to minimize losses in power conversion applications and is optimized for 5-V gate drive applications. The 2-mm × 2-mm SON offers excellent thermal performance for the size of the package.

图 7 shows a block diagram of the device.

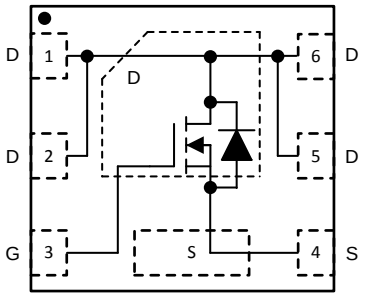


图 7. CSD17313Q2 Block Diagram

Additional features:

- VDS drain-to-source voltage of 30 V
- Ultra-low Qg and Qgd
- Low thermal resistance
- Pb-free, halogen-free, and RoHS compliant
- Threshold voltage of 1.3 V
- 31-mΩ drain-to-source on resistance at V_{GS} of 3 V
- SON 2-mm × 2-mm plastic package

2.3 System Design Theory

BCMs, multi-mode radar modules, front camera modules, and head unit modules are all composed of several sub-circuits. This design covers the battery input, voltage regulation, and CAN portions of these applications. The following subsections cover the component selection and device configuration decisions for this design.

2.3.1 Supply Protection and Filtering

图 8 shows the portion of the schematic that has the reverse battery input protection diode, input filter, and pi filter components.

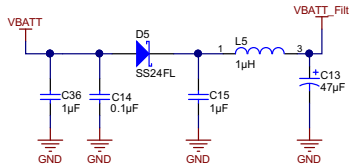


图 8. Supply Protection and Filtering Circuitry

Diode D5 is a 40-V Schottky diode for protection against reverse battery conditions. Due to the 42-V tolerant input voltage of the LM53601-Q1 in conjunction with the reverse blocking Schottky diode, the design can handle from –40 V to 42-V on the VBATT input supply.

Capacitors C36 and C14 are used for input transient filtering, and the pi filter composed of C15, L5, and C13 can be used to implement a two-pole, low-pass filter for conducted emissions. C13 and L5 were left unpopulated for the evaluation of this design.

Lastly, the VBATT net is directly tied to pin 9 of the external D-subminiature (D-sub) connector J6 as shown in 节 2.3.5.

2.3.2 Wide Input Voltage Buck Converter

图 9 shows the portion of the schematic with the LM53601NQDSXRQ1 and all of its supporting circuitry.

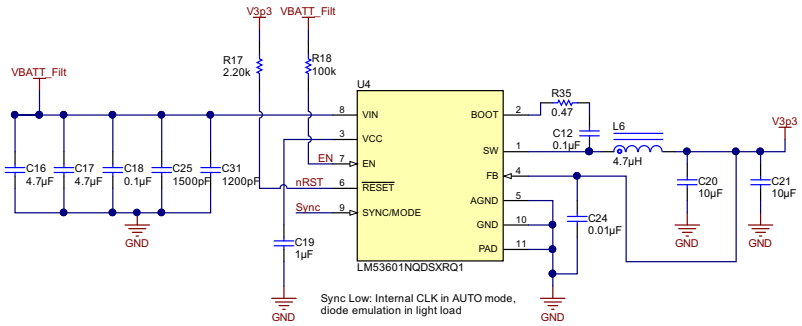


图 **9. LM53601-Q1 Synchronous Buck Converter Circuitry**

- Enable pin: R18 pulls the enable pin up to the input supply rail so that the device is always on.
- $\overline{\text{RESET}}$ pin: R17 pulls the open-drain reset output of the LM53601-Q1 up to the 3.3-V regulated output voltage. The pin is then directly connected to the $\overline{\text{XRS}}$ reset input for the Piccolo MCU to delay power up until the 3.3-V rail is in regulation.
- SYNC/MODE pin: This pin was tied directly to GPIO18 (pin 33) so that the MCU can place the device into either forced PWM mode or AUTO mode. For evaluation of the design, the pin was driven low to place the device into *Auto* mode.
- Input capacitors, output capacitors, and inductor selection was made using the *Detailed Design Procedure* section of the *LM53601-Q1 1A, 36V Synchronous, 2.1MHz, Automotive Step Down DC-DC Converter*[1] datasheet. In addition, the 1500-pF and 1200-pF 0402 capacitors were added from the VIN node to GND on the LM53601-Q1 to improve the 170-MHz to 200-MHz emissions. These capacitors remained populated for entire design evaluation.
- A series 0.47-Ω resistor was added between switch node and the boot capacitor C12 to help dampen the switching node and lower the emissions in the 180-MHz to 200-MHz frequency range.

The LM52601-Q1 is a synchronous buck regulator with both the high-side and low-side FETs integrated enabling a compact solution size. The total PCB solution size on the TIDA-01428 for the LM53601-Q1 and all of its supporting circuitry is 14 mm × 14 mm (550 mils × 550 mils). 图 10 shows a snippet of the buck converter portion of the PCB with the two added capacitors and series boot resistor.

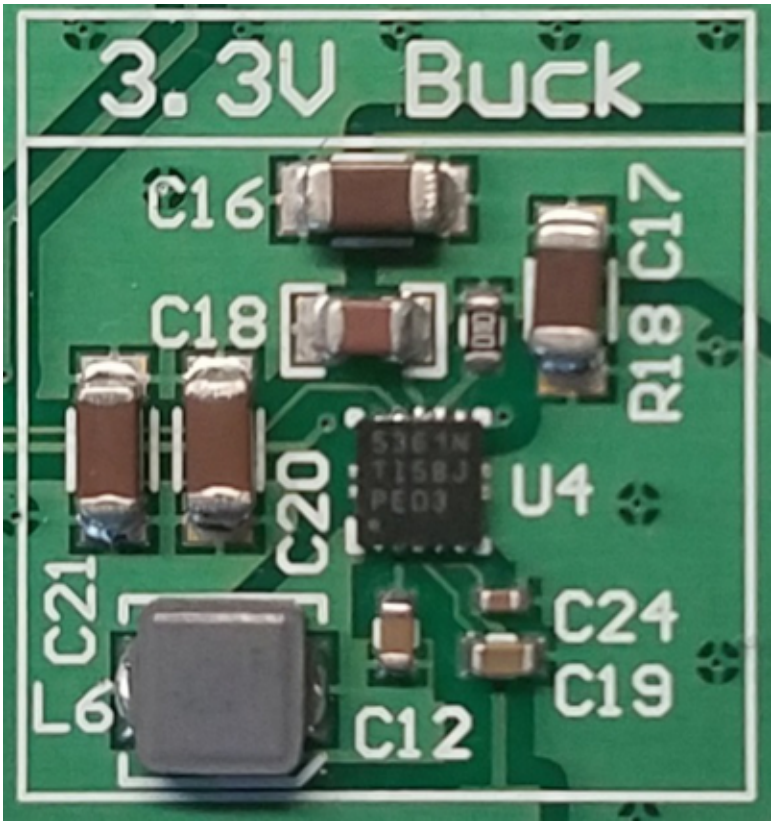


图 **10. LM53601-Q1 Buck Converter PCB Solution Size**

Lastly, the LM53601-Q is able to regulate to 3.3 V with input voltages as low as 3.8 V. Due to the series Schottky diode drop of up to 0.5 V for reverse battery protection, the module is therefore able to handle voltages as low as 4.3 V and remain in regulation.

2.3.3 Low-Input Voltage Boost Converter

图 11 shows the portion of the schematic with the TPS61240IDRVRQ1 and all of it's supporting circuitry.

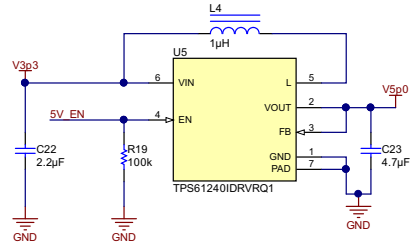


图 **11. TPS61240-Q1 Synchronous Boost Converter Circuitry**

- EN pin: R19 is used to pull the EN pin low and disable the output when the Piccolo MCU's GPIO8 (pin 35) is not actively driving the pin high or low (in a high-impedance state).
- C22: 2.2 µF is the recommended input capacitance.
- Output capacitance and inductor selection was made using the *Detailed Design Procedure* section of the *TPS61240-Q1 3.5-MHz High Efficiency Step-Up Converter*[2] datasheet.

The TPS61240-Q1 is a synchronous boost regulator with both the high-side and low-side FETs integrated, which enables a very small PCB solution size. The total PCB solution size on the TIDA-01428 for the TPS61240-Q1 and all of its supporting circuitry is 8.13 mm × 6.6 mm (320 mils × 260 mils). 图 12 shows a snippet of the buck converter portion of the PCB.

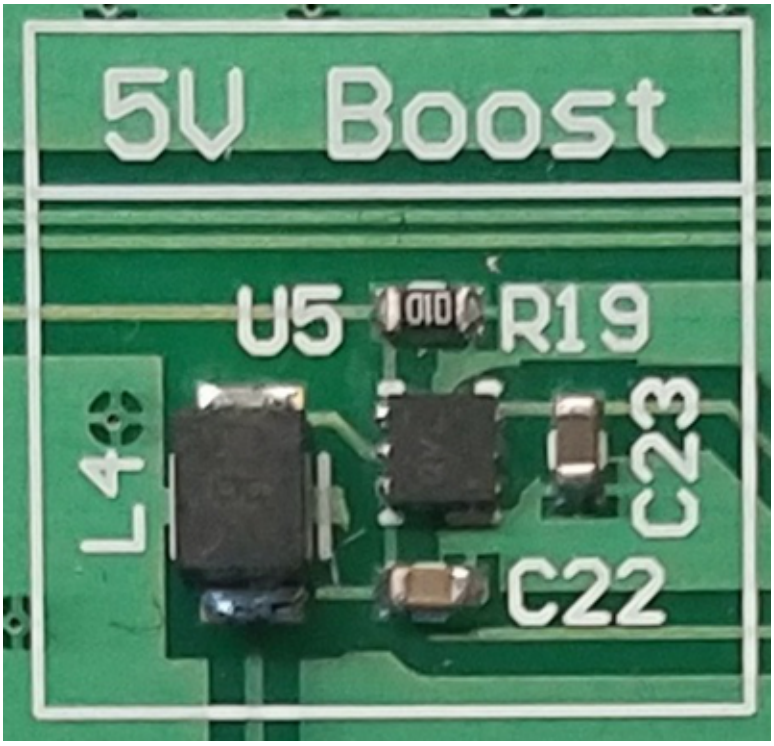


图 **12. TPS61240-Q1 Boost Converter PCB Solution Size**

2.3.4 CAN Physical Layer

图 13 shows the portion of the schematic with the CAN physical layer, which includes the CAN transceiver, filtering common mode choke (CMC), filtering capacitors, ESD protection IC, and termination components.

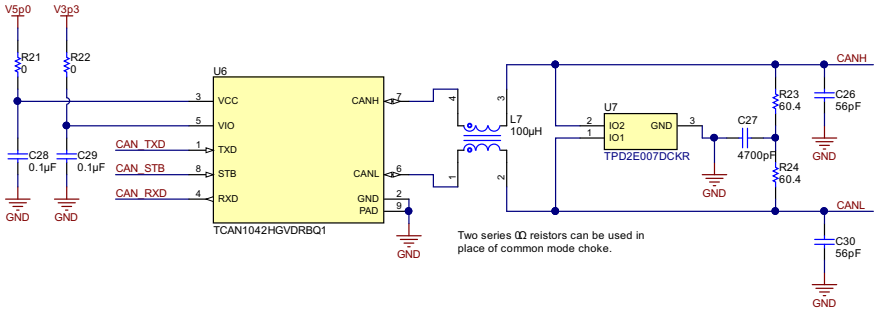


图 **13. CAN Physical Layer Circuitry**

- Transceiver U6: The TCAN1042 family comes in both an 8-pin SOIC package and a small, 3-mm × 3-mm, leadless, DFN package. This design uses the small DFN package.
- CMC L7: A standard CMC footprint was added to the CANH and CANL bus lines so that the design could easily be evaluated with a variety of CMCs. However, the design was evaluated without the CMC and instead with two series 0-Ω resistors in place of the CMC.
- ESD IC U7: A common footprint, dual-channel, bidirectional ESD protection IC was placed for optional additional protection of the CANH and CANL bus lines. However, the design was evaluated with U7 unpopulated.
- Termination components R23, R24, and C27: These components are used for terminating the CAN bus with a split termination. This technique uses two resistors that are equal to one-half the characteristic impedance of the cable (typically 120 Ω) with a capacitor placed to ground between the two resistors. This technique creates two low-pass filters on the CANH bus lines and the CANL bus line for filtering common mode noise. If standard termination is desired, capacitor C27 can be left open.
- Filtering capacitors C26 and C30: These capacitors are place from CANH to GND and CANL to GND to help filter high-frequency transients and noise from getting into or out of the module.

图 **14. CAN Physical Layer Circuitry on PCB**

2.3.5 External Power and Networking Connections

图 15 shows the external connector, which includes the VBATT input, GND connection, and the CANH and CANL connections. The pinout used for the D-sub 9 connector is the recommended pinout by CAN in Automation (CiA) document DIN 41652. 图 15 shows the pinout for both the female D-sub 9 connectors that were populated on the boards and the male connectors that were used for creating the wire harness.

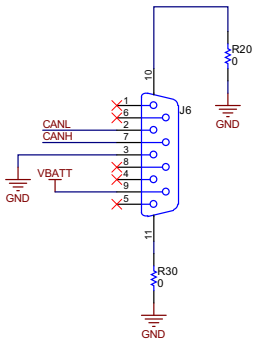


图 **15. External Connector Pinout**

图 16 shows the external connector on the TIDA-01428 PCB.

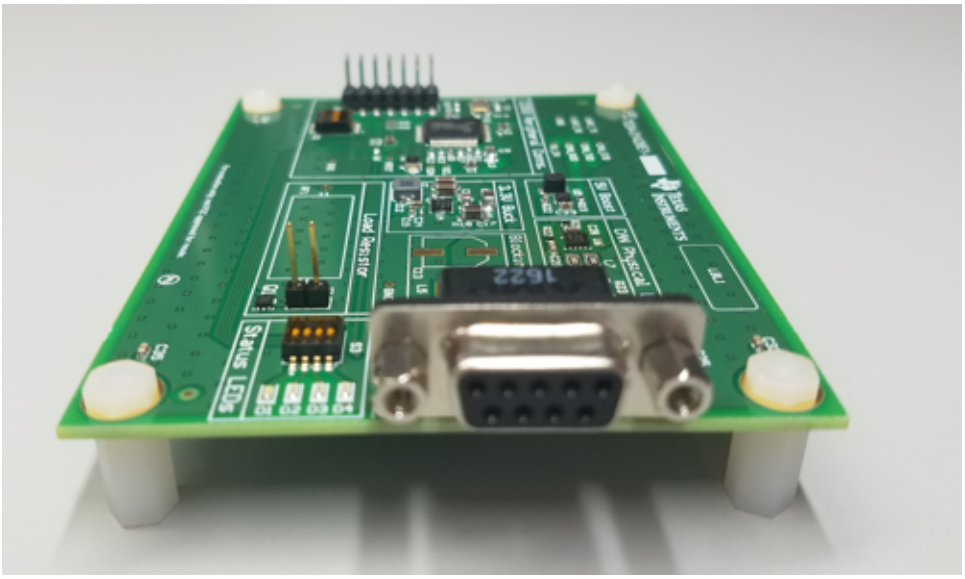


图 **16. External Connector on PCB**

2.3.6 Electronically-Controlled Dummy Load

图 17 shows the dummy load resistor and external circuitry that was used to help further evaluate the 3.3-V buck regulator. The dummy load uses a 3-W, 4.7-Ω resistor, which results in an additional load current when active on the buck regulator's output of 702 mA. This circuitry was used to evaluate the load-step transient response of the LM53601-Q1 buck converter.

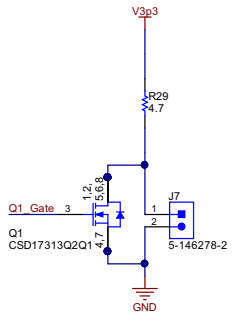


图 **17. Dummy Load Circuitry**

- J7: The two-pin, 100-mil header can be used for manually enabling and disabling the dummy load by placing a shunt across the pins.
- Q1: Additionally, the dummy load can be electronically controlled through GPIO24 (pin 64) of the TMS320F28030Q device. GPIO24 is tied to the gate connection of Q1 to enable and disable the load. Q1 is a 30-V, N-Channel NexFET power MOSFET.

The load step response oscilloscope shots using GPIO24 and Q1 were taken in 3.2 节. 图 18 shows the dummy load resistor portion of the PCB.

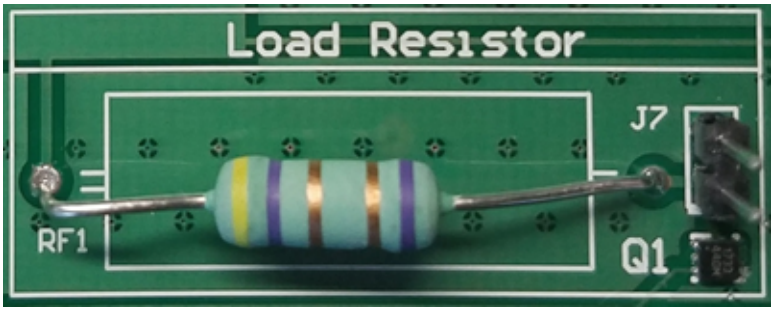


图 **18. Dummy Load Resistor Circuitry on PCB**

2.3.7 Status LEDs

Four status LEDs have been added to the design for ease of evaluation and monitoring during electromagnetic compliance (EMC) testing. 图 19 shows the status LED portion of the schematic.

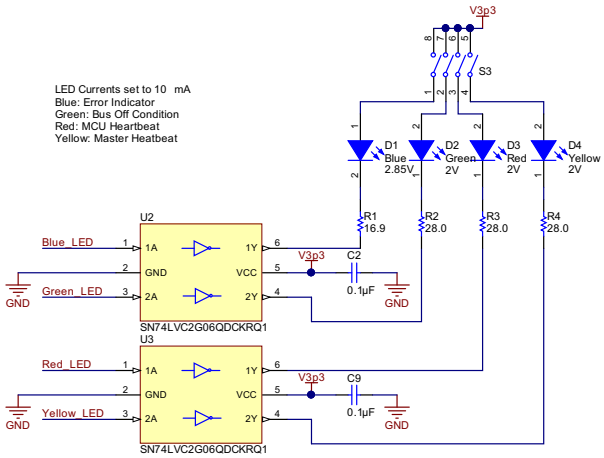


图 19. Status LED Circuitry

To ensure there would be proper drive current for the status LEDs, two SN74LVC2G06-Q1 automotive dual inverter and driver ICs were used for driving the four status LEDs. Additionally, the 3.3-V supply to each LED has been equipped with a single-pole switch that can be opened for disabling the LED. This switch is useful when taking current consumption measurements on the TIDA-01428 design.

All series resistors for the LEDs have been sized for a nominal 10 mA of LED current. 表 2 shows what status each LED was programmed to indicate.

表 2. Status LED Descriptions

LED COLOR	DESCRIPTION	BEHAVIOR
Blue	Any error status flag set in the CAN controller	Blinks at 1 Hz when any CAN error status flag is set
Green	*Bus Off* error condition in the CAN controller	Blinks at 1 Hz when the *Bus Off* flag is set
Red	MCU status LED heartbeat	Blinks at 1 Hz to indicate module is functioning properly
Yellow	Master status LED heartbeat	Blinks at 1 Hz to indicate module is configures as the master module and initiates communication

图 20 shows the status LED portion of the PCB.

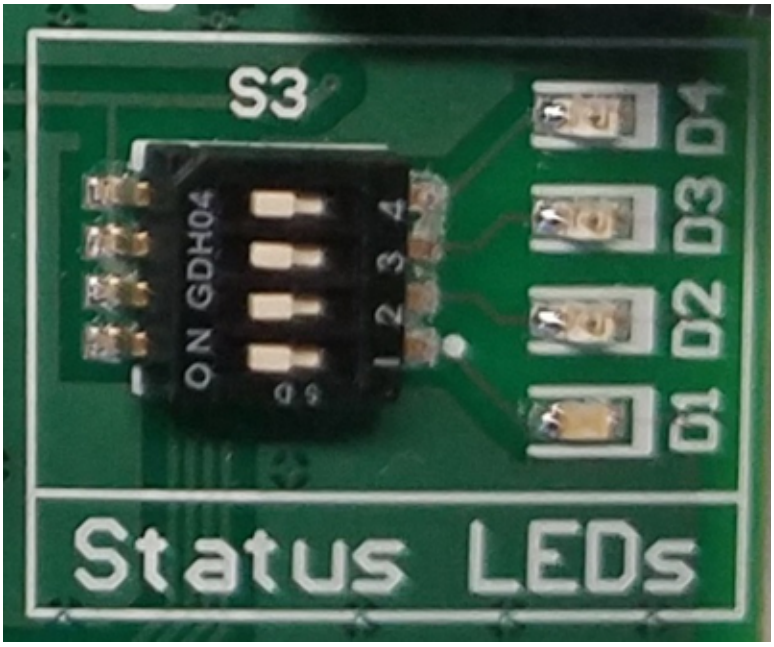


图 **20. Status LED Circuitry on PCB**

2.3.8 Piccolo™ MCU Input Power Filtering

图 21 shows the power connections circuitry for the TMS320F28030PAGQ device.

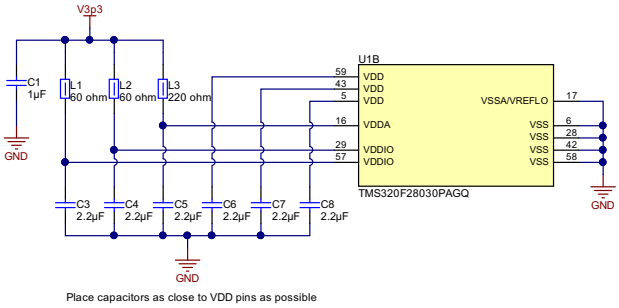


图 **21. Input Power Filtering for Piccolo™ MCU**

- Supply decoupling capacitors: It is recommended to place a dedicated 2.2-µF capacitor on each VDDIO, VDDA, and VDD input as close to the pin as possible
- Ferrite beads: Additionally, it is recommended to place a series ferrite on both VDDIO supply input pins and the VDDA supply input pin for additional filtering

2.3.9 Piccolo™ MCU Mode Selection and Programming Interface

图 22 shows the optional external crystal, the mode selection input circuitry, reset control, and the JTAG programming interface.

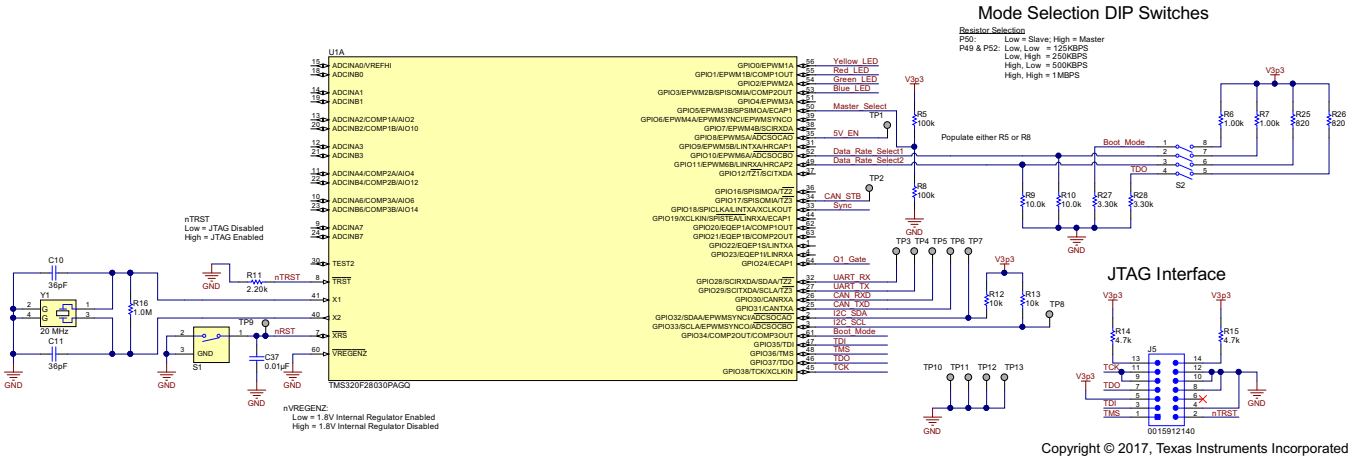


图 22. Mode Selection and Programming Interface Circuitry

- Optional external crystal: The TMS320F28030 has an internal crystal and the option to run off an external crystal. An optional, 20-MHz crystal was populated, but the internal crystal was used for evaluation.
- Mode selection circuitry: Five of the GPIOs were used for mode selection and boot mode control.
  - GPIO5: If this pin is pulled high on startup, the module will be configured as the master node. If the pin is pulled low on startup, the module will be configured as the slave node. Populate either R5 or R8 so that the pin is in a known state.
  - GPIO10 and GPIO11: The state of these two pins on startup dictates what data rate the CAN interface is configured to.
    - Low, Low: 125 KBPS
    - Low, High: 250 KBPS
    - High, Low: 500 KBPS
    - High, High: 1000 KBPS
  - GPIO37 and GPIO34: The state of these two pins on startup tells the bootloader software what boot mode to use on power up.
    - Low, Low: Parallel IO mode
    - Low, High: SCI mode
    - High, Low: Wait mode
    - High, High: GetMode

    The default behavior of GetMode is to boot to flash; therefore, once the modules were programmed (into flash) after assembly, GetMode is the mode that the modules were configured to for evaluation. For more information on boot modes, see *TMS320F2803x Piccolo™ Microcontrollers*[4].
- $\overline{\text{XRS}}$ reset input pin: Two connections were made to $\overline{\text{XRS}}$ input pin. The first is a manual push button for restarting the MCU, and the second is the open-drain, $\overline{\text{RESET}}$ output of the LM53601-Q1 device as shown in 图 9. The LM53601-Q1 holds this output low until the 3.3-V supply is in regulation. This hold ensures that the MCU only begins the boot process once a stable supply has been generated.

- JTAG programming interface: The device was programmed through a 7 × 2, 100-mil JTAG header using the XDS100V2 JTAG emulator. For more information on JTAG programming, see *TMS320F2803x Piccolo™ Microcontrollers*[4].

图 23 shows the mode selection circuitry, manual reset button, and JTAG programming header J5.

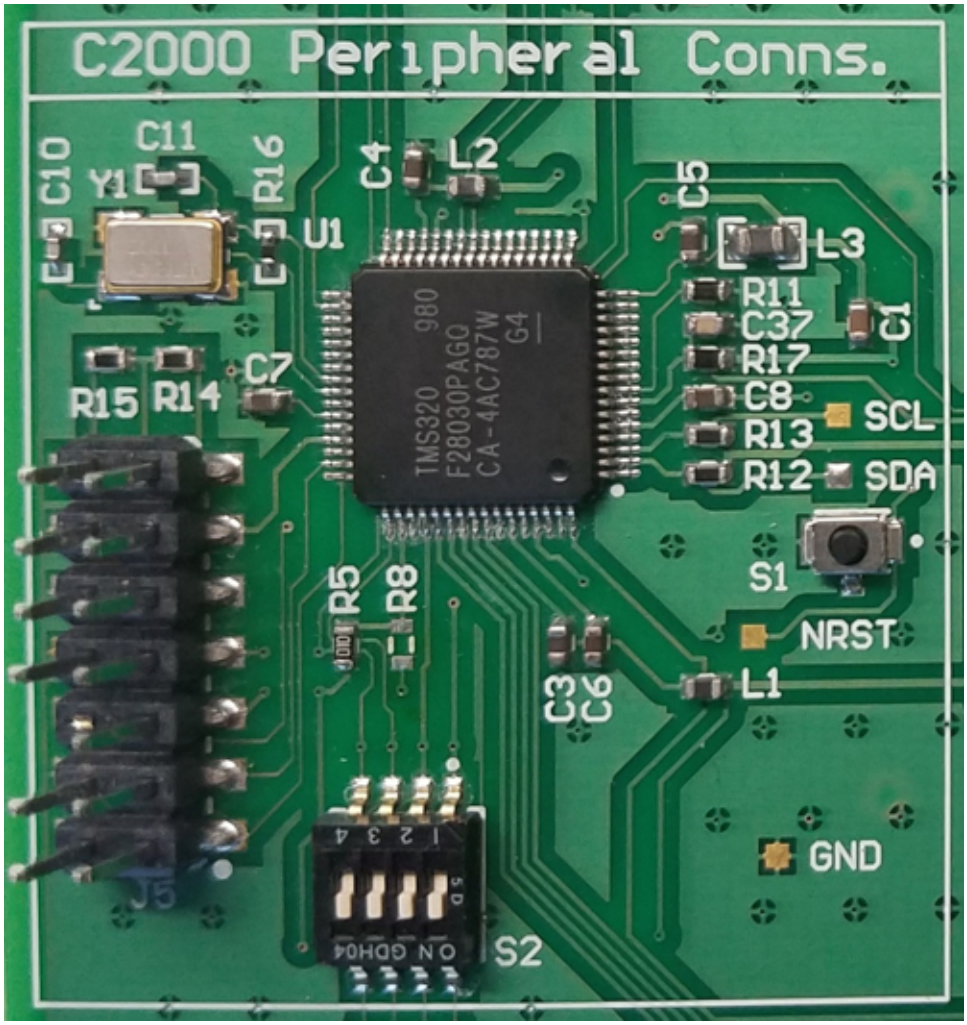


图 23. C2000™ Peripheral Circuitry on PCB

3 Hardware, Software, Testing Requirements, and Test Results

3.1 Required Hardware and Software

This section provides an overview of the TIDA-01428 board and all the external connections required to evaluate the reference design.

3.1.1 Hardware

The TIDA-01428 reference design was created to evaluate a 2-stage power tree with a CAN interface. The first stage of the power tree is a wide-input voltage buck converter to 3.3 V, and the second stage is a low-input voltage boost converter to create a 5-V supply rail for the CAN transceiver. To evaluate the CAN interface, a pair of modules must be connected to each other through a 4-wire harness.

To set up and evaluate this design the following three items were used:

1. Two TIDA-01237 PCB boards
2. A wire harness with four conductors: One unshielded twisted pair (UTP) cable for CANH and CANL and another UTP cable for VBATT and GND power connections.
3. An XDS100V2 JTAG emulator for programming the TMS320F28030PAGQ Piccolo MCU

All of these items are shown in 图 24.

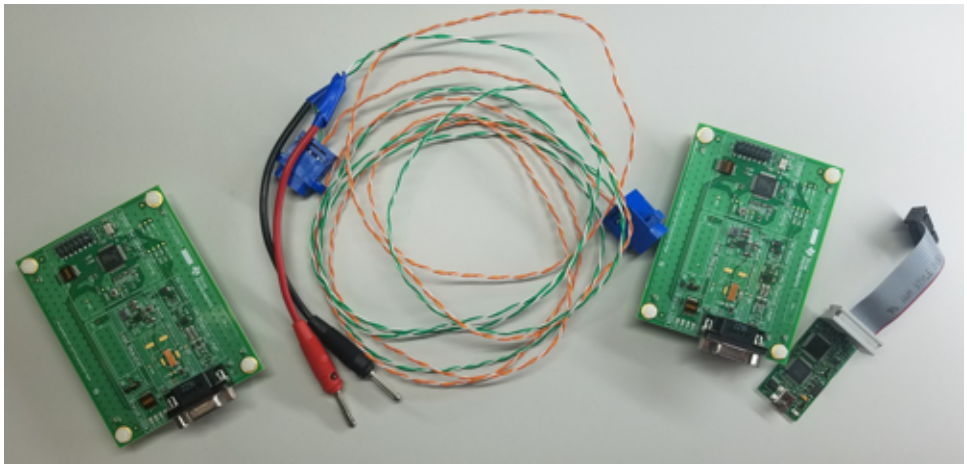


图 **24. Hardware Required for Evaluation**

3.1.1.1 TIDA-01428 PCBs

The PCB boards are 4" × 3" and have 1-oz copper foil on both sides. There are two external connectors used to interface with the board:

1. Header J5: This is a 14-pin (7 × 2), 100-mil header used for programming the TMS320F28030PAGQ device through a JTAG interface using the XDS100v2 JTAG emulator.
2. Connector J6: This is a female, 9-pin, D-sub connector (DE-9) that has four connections for power, ground, CANH, and CANL.

3.1.1.2 Mode Selection

As discussed in 节 2.3.9, three GPIO pins are used to configure the module on power up. 表 3 shows the eight possible configurations dictated by the states of GPIO 5, 10, and 11.

表 **3. Mode Selection**

GPIO5	GPIO10	GPIO11	MASTER OR SLAVE	DATA RATE (KBPS)
Low	Low	Low	Slave	125
Low	Low	High	Slave	250
Low	High	Low	Slave	500
Low	High	High	Slave	1000
High	Low	Low	Master	125
High	Low	High	Master	250
High	High	Low	Master	500
High	High	High	Master	1000

Switch S2 controls GPIO10 and GPIO11. If the switch is in the closed position, the input will be pulled high, and if the switch is in the open position, the input will be pulled low.

3.1.1.3 Wire Harness

The wire harness for connecting the two boards together was created using two 1.7-m, 24-gauge UTP cables with two male 9-pin, D-sub connectors. The pinout used is the recommended pinout by CiA document DIN 41652. 表 4 shows the pinout for the four connections that were used on each D-sub connector.

表 **4. Wire Harness Connections**

D-SUB CONNECTOR PIN	CONNECTION DESCRIPTION
Pin 2	CANL: Low-level CAN bus IO line
Pin 3	Ground power connection
Pin 7	CANH: High-level CAN bus IO line
Pin 9	Battery input power connection

图 25 shows an image of assembled wire harness used for evaluation.

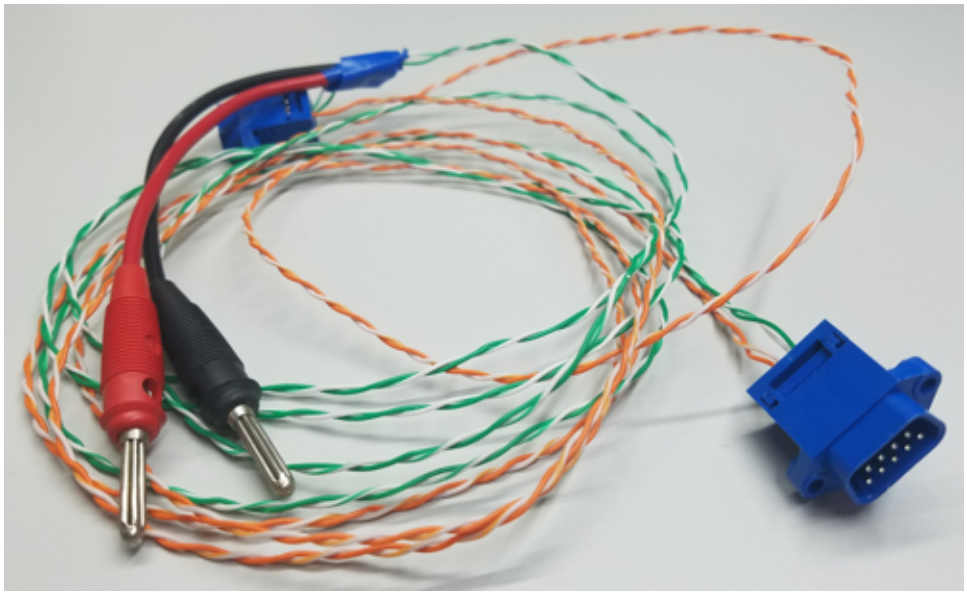


图 **25. Assembled Wire Harness**

Two banana plug pigtail power connections were added to one side of the harness for connecting to a lead-acid battery.

3.1.1.4 Power Supply Connection

The modules are powered through the banana plug pigtails that were added to the wire harness as shown in 图 25. The VBATT net and GND net are shared between both ends of the wire harness, so the supply connections must only be made on the one end of the harness to power both modules. The recommended supply voltage range is from 4.3 V to 36 V.

3.1.1.5 XDS100V2 JTAG Emulator

The XDS100V2 JTAG emulator is an emulator made by Spectrum Digital Incorporated that can be used to program a variety of MCUS using JTAG. This emulator plugs into a computer through USB and connects to the target using a standard 14-pin JTAG interface. 图 26 shows an image of the XDS100V2.

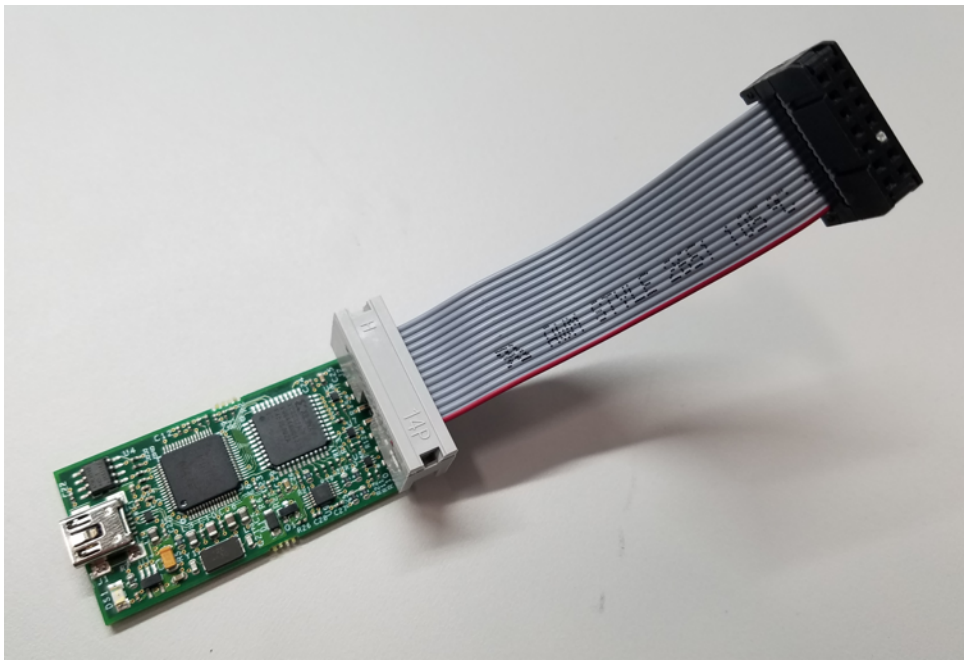


图 **26. XDS100V2 JTAG Emulator**

Once the modules are programmed in flash, the modules can be power cycled and evaluated without requiring reprogramming.

3.1.2 Software

The software was written using Code Composer Studio™ v7.1.0 in C. 图 27 shows a program flowchart for the programming of each module. As long as one module is configured as a master and one module is configured as a slave, as described in 节 2.3.9, the two modules will automatically begin communicating and error checking once powered up and connected to each other.

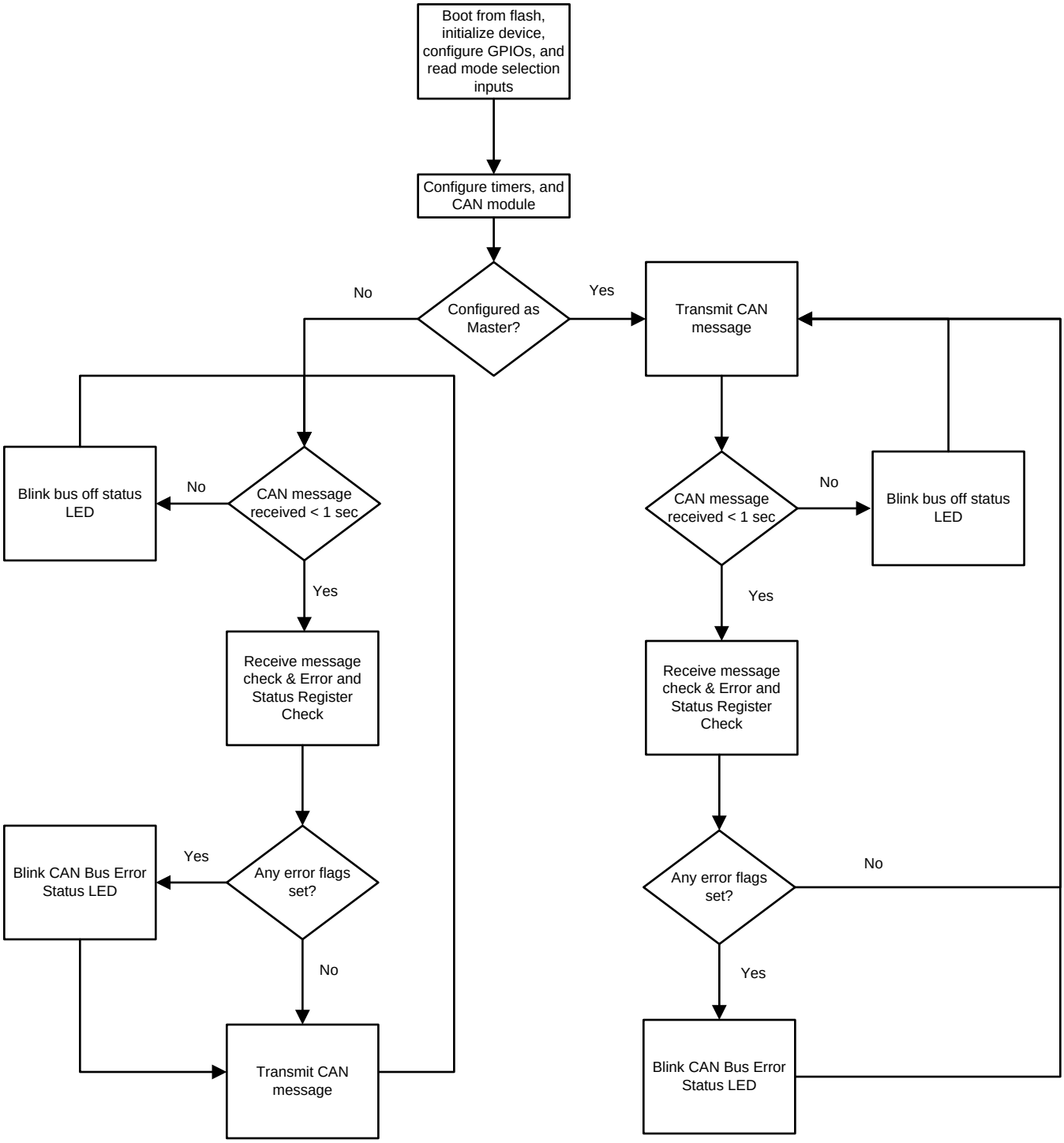


图 27. Program Flow Diagram

As soon as the modules are powered up the bootloader first checks the state GPIO34 and GPIO37. Once the modules have been initially programmed, the switches are set so both GPIO34 and GPIO37 are pulled high. This setting tells the bootloader to boot from flash.

In flash the module program first initializes the interrupts and GPIO pins. After initialization GPIO inputs GPIO5, GPIO10, and GPIO11 are read to determine how to configure the CAN module and whether the module will follow the slave program flow (left path) or the master program flow (right path) as shown in 图 27.

If the module is configured as the master node, the device will initiate traffic and indefinitely re-attempt communication if a message is not received back. There is a 1-s timer that is started after each transmission of a CAN message. If this timer expires before a message is received, an error count is set, and the error status LED will blink four times at 1 Hz. If a message is received, the contents of the data field will be checked against a preprogrammed value. If the two do not match, or if any of the error flags are set in the error and status register, an error count is set, and the CAN error status LED will blink four times at 1 Hz. Additionally, if the *Bus Off* status flag is set, the bus off status LED will blink four times at 1 Hz. This send, receive, and error check process continues indefinitely.

If the module is configured as the slave node, the device will wait to receive a message before transmitting one. If the module does not receive a message within 1 s, an error count is set, and the error status LED will blink four times at 1 Hz. Once a message is received, the contents of the data field will be checked against a preprogrammed value. If the two do not match, or if any of the error flags are set in the error and status register, an error count is set and the CAN error status LED will blink four times at 1 Hz. Additionally, if the *Bus Off* status flag is set in the error and status register, the bus off status LED will blink four times at 1 Hz. After receiving and error checking the message, the module will transmit a CAN frame and the process will start over. The 1-s timer will begin counting down, and if the timer expires before a message is received, the error status LED will blink four times at 1 Hz. This receive, error check, and transmit process continues indefinitely.

3.2 Testing and Results

The following items were evaluated on the TIDA-01428 design:

- Reverse blocking protection
- Buck converter input voltage versus input current
- Buck converter input voltage versus output voltage
- Buck converter efficiency
- Buck converter load step response
- Boost converter input voltage versus input current
- Boost converter input voltage versus output voltage
- Boost converter efficiency
- CISPR 25 Radiated Emissions (RE) Testing
- CISPR 25 Conducted Emissions (CE) Testing - Voltage Method
- ISO 11452-4 Bulk Current Injection (BCI) Immunity Testing

3.2.1 Reverse Blocking Protection

For lower current applications, a standard Schottky diode is the most cost-effective solution for reverse battery protection. A standard 60-V, 2-A Schottky diode in a SOD123 package was used. 图 28 shows the input leakage current versus the reverse polarity input voltage.

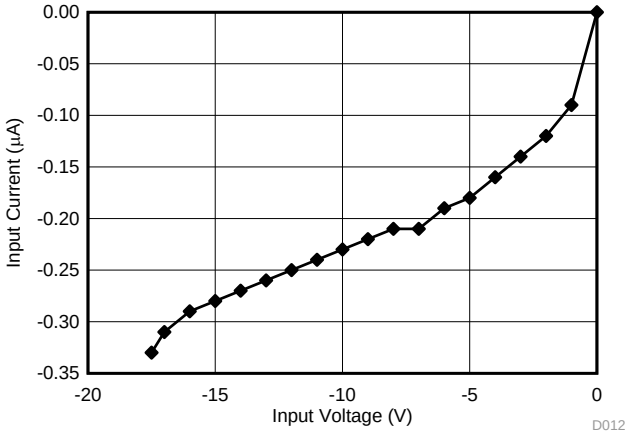


图 28. Reverse Blocking Performance

As shown in 图 28, the input leakage current with –17.5-V input voltage applied was 330 nA at room temperature.

3.2.2 Buck Converter Input Voltage Versus Input Current

The input current versus input voltage data was taken with one module initialized and sending CAN messages at 500 KBPS. The input voltage measurements are taken from the input of the module (before the Schottky diode), and all of the status LEDs were all left open for these measurements.

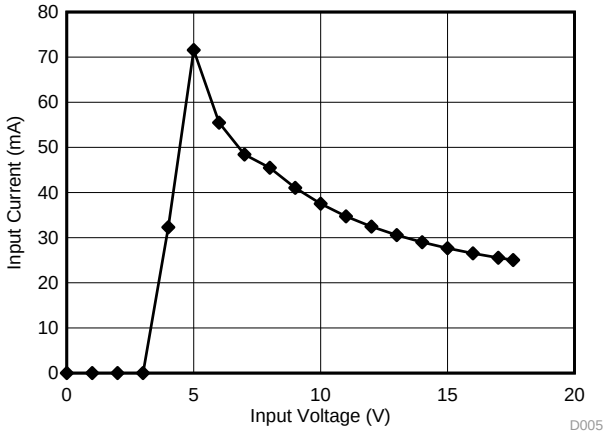


图 29. Buck Input Current Versus Input Voltage

As shown in 图 29, the buck converter begins to turn on with 4 V at the input of the module (before the Schottky diode).

3.2.3 Buck Converter Input Voltage Versus Output Voltage

The output voltage versus input voltage data was taken with one module initialized and sending CAN messages at 500 KBPS. The input voltage measurements are taken from the input of the module (before the Schottky diode), and all of the status LEDs were all left open for these measurements.

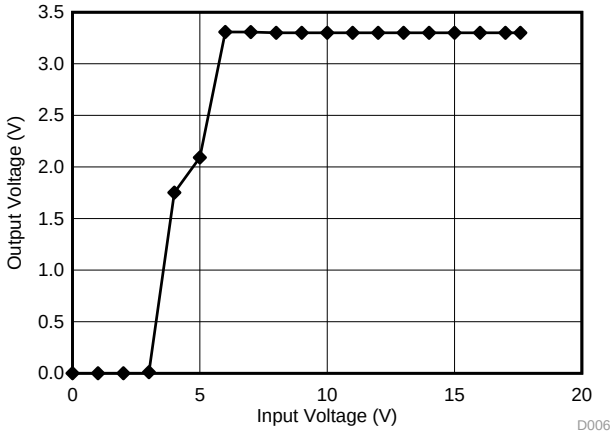


图 **30. Buck Output Voltage Versus Input Voltage**

As show in 图 30, the buck converter's output voltage begins to rise just before 4 V at the input of the module and is in regulation before 6 V.

3.2.4 Buck Converter Efficiency

The efficiency data for the buck converter was taken after completely isolating the buck converter portion of the design from the rest of the board (cutting traces). Once all of the external loads were disconnected from the output and the input voltage could be applied directly to the VIN node of the buck converter, purely resistive loads were tied from the output of the regulator to ground.

Therefore, the input voltage measurements were taken directly at the input node of the regulator, and the output voltages were taken from C21 to GND. A constant input voltage of 13.5 V was used for all efficiency measurements.

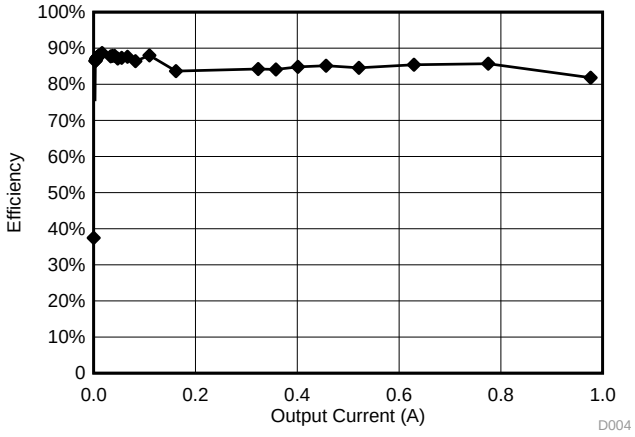


图 **31. Buck Converter Efficiency Measurements**

As shown in 图 31, the efficiency of the converter remains between 80% and 90% from very light loads (1 kΩ) all the way up to full load (3.3 Ω).

3.2.5 Buck Converter Load Step Response

Lastly, the buck converter was evaluated for output regulation accuracy when subjected to a step up in load current and a step down in load current. For this test, the dummy load resistor R29 on the board was populated with a 4.7-Ω resistor, and transistor Q1 was used for quickly turning on and off this load. The 4.7-Ω load on the 3.3-V rail results in a 702 mA load step, which is 70% of the maximum load of the regulator. The load step measurements were performed with the module initialized and sending CAN messages at 500 KBPS.

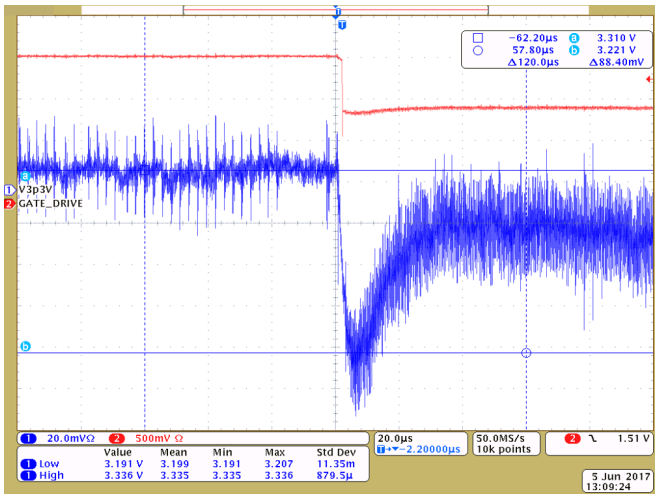


图 32. Buck Converter Load Step Increase Response

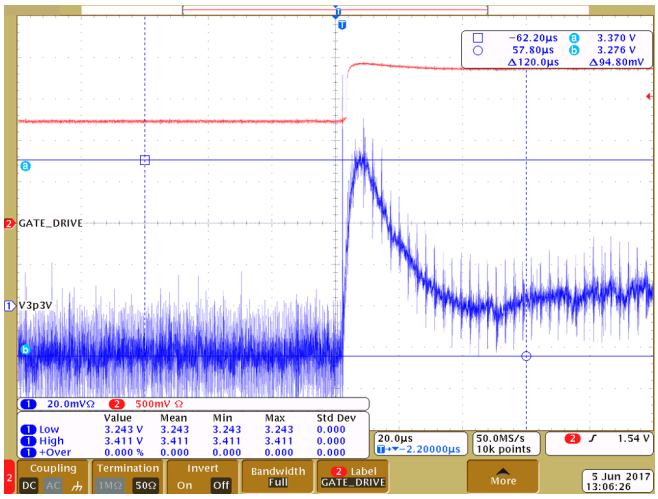


图 33. Buck Converter Load Step Decrease Response

图 32 shows the converter's response to the load's 700-mA increase. The step increase in load current causes the output voltage of the regulator to droop 88.4 mV, which is equivalent to 2.67%. 图 33 shows the converter's response when the low current is decreased by 700 mA. The step decrease in load current causes the output voltage to rise 94.8 mV, or by 2.87%.

3.2.6 Boost Converter Input Current Versus Input Voltage

To evaluate the boost converter's input current versus input voltage performance, the regulated 3.3-V output of the LM53601-Q1 was disconnected, and a power supply was fed directly to the input node of the regulator. The CAN transceiver was in normal mode in a recessive state for all input current measurements.

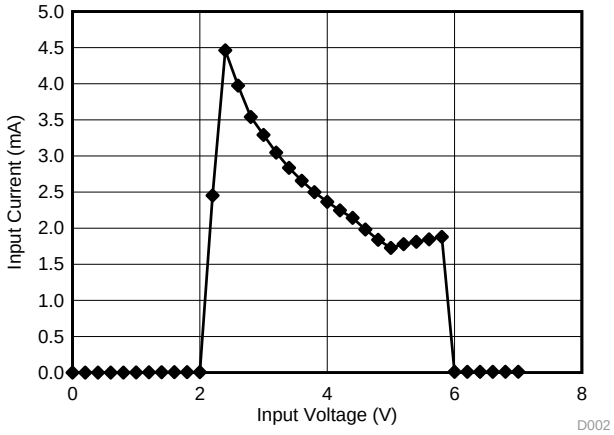


图 **34. Boost Converter Input Current Versus Input Voltage**

图 34 shows the boost converter began to turn on and draw current at 2.2 V and shut off at 5.994 V. The shut-off voltage is part of the overvoltage protection that the device has to protect downstream devices from getting damaged when input voltages get too high. Upon lowering the input voltage, the output was reenabled at 5.898 V, which shows a built-in hysteresis of 96 mV.

3.2.7 Boost Converter Input Voltage Versus Output Voltage

To evaluate the boost converter's output voltage versus input voltage performance, the regulated 3.3-V output of the LM53601-Q1 was disconnected, and a power supply was fed directly to the input node of the regulator. The CAN transceiver was in normal mode in a recessive state for all output voltage measurements.

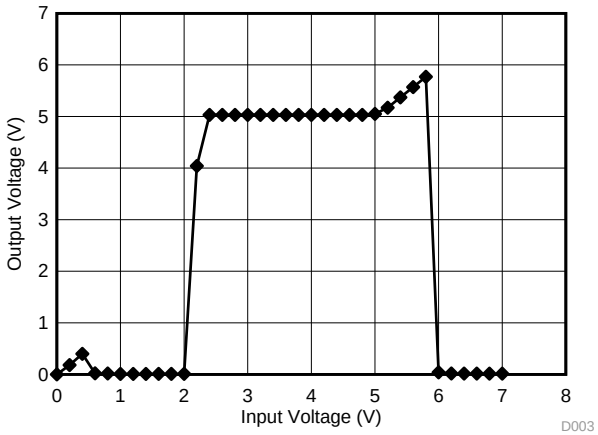


图 **35. Boost Converter Output Voltage Versus Input Voltage**

图 35 shows that the boost converter began to turn on and draw current at 2.2 V and was regulating 5 V on the output at 2.4 V in. Additionally, the device went into shutdown mode due to overvoltage on the input at 5.994 V. Again, this overvoltage protection protects downstream devices from getting damaged when input voltages get too high. Upon lowering the input voltage, the output was reenabled at 5.898 V, which shows a built-in hysteresis of 96 mV.

3.2.8 Boost Converter Efficiency

The efficiency data for the boost converter was taken after disconnecting the CAN transceiver from the 5-V output and placing varying purely resistive loads on the output of the regulator. A constant input voltage of 3.3 V was applied at the input node of the regulator for all efficiency measurements.

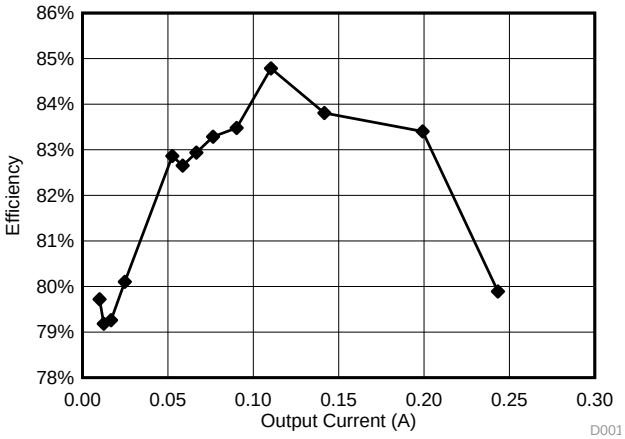


图 36. Boost Converter Efficiency Measurements

图 36 shows that for load currents between 25 mA and 240 mA, the efficiency was between 80% and 86%. With a 3.3-V input voltage the regulator was able to handle a nominal load of 240 mA before the output voltage began to fall output of regulation.

3.2.9 CISPR 25 Radiated Emissions Testing

Radiated emissions testing was performed for a pair of modules in an anechoic chamber per the absorber lined shielded enclosure (ALSE) test method in CISPR 25 Edition 4.0. In this test there are two modules placed 1.7-m apart from each other. The slave node, or equipment under test (EUT) as referred to in the standard, is placed on top of a low-relative permittivity support (raised off the ground plane by a material that resists electric fields). The master node, which is sometimes referred to as the monitoring node, is tied directly to the ground plane. This slave node setup is shown in 图 37, and the master node setup is shown in 图 38.

图 37. Slave Node Setup for RE per CISPR 25 ALSE

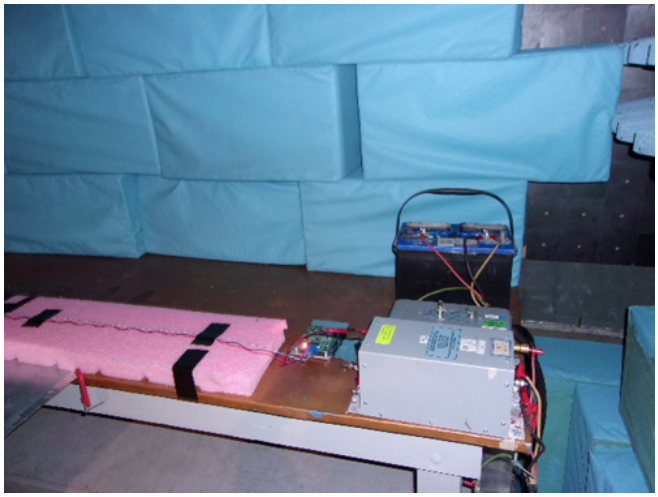


图 38. Master Node Setup for RE per CISPR 25 ALSE

The test consists of multiple frequency ranges for three different antennas with two of the antennas oriented in both the horizontal and vertical positions. The setup description for the five measurement runs are as follows:

- Test run one: 150 KHz to 30 MHz with a dipole antenna in vertical orientation
- Test run two: 30 MHz to 200 MHz with a biconical antenna in horizontal orientation
- Test run three: 30 MHz to 200 MHz with a biconical antenna in vertical orientation
- Test run four: 200 MHz to 1,000 MHz with a logarithmic antenna in horizontal orientation
- Test run five: 200 MHz to 1,000 MHz with a logarithmic antenna in vertical orientation

Each graph shows a series of three limit lines—one for each of the three detectors that are used on the spectrum analyzer to gather the data: one for the peak detector, one for the quasi-peak detector, and one for the average detector. A limited number of quasi-peak and average data points were taken to save test time. The test program selected these data points based on the frequencies where the peak detector was closest to the limit line.

The TIDA-01428 passed Class 4 CISPR 25 radiated emissions per the ALSE method without the input pi filter populated or a CMC populated on the CAN bus lines.

图 39 shows the dipole antenna that is 1 m in front of the test setup in the vertical position. 图 40 shows the radiated emissions results for test run one.

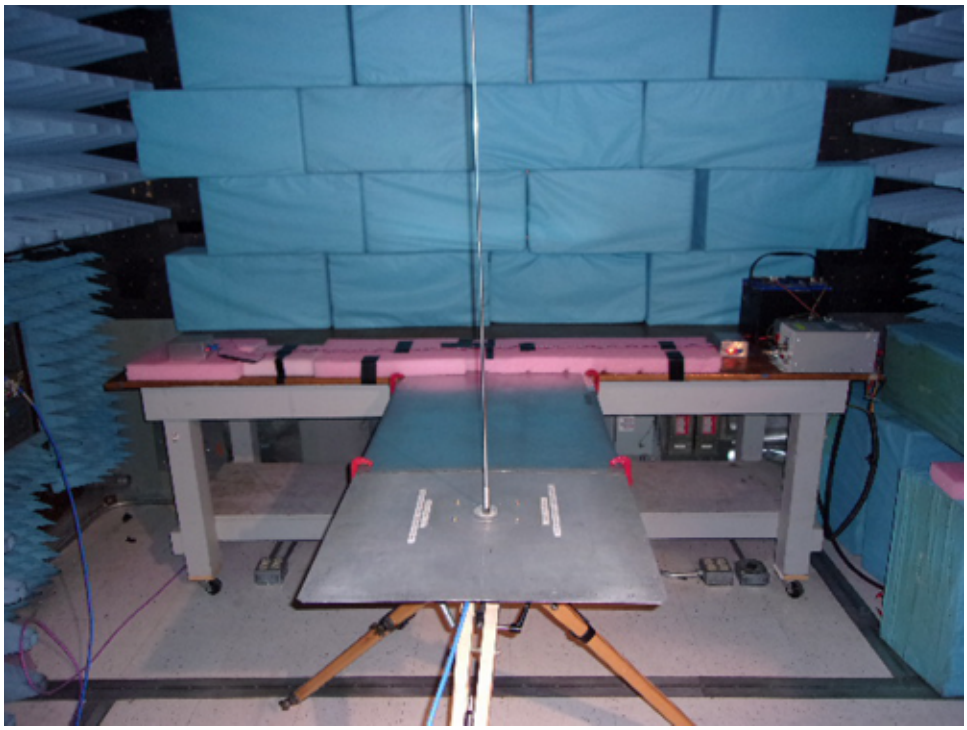


图 39. Dipole Antenna Test Setup

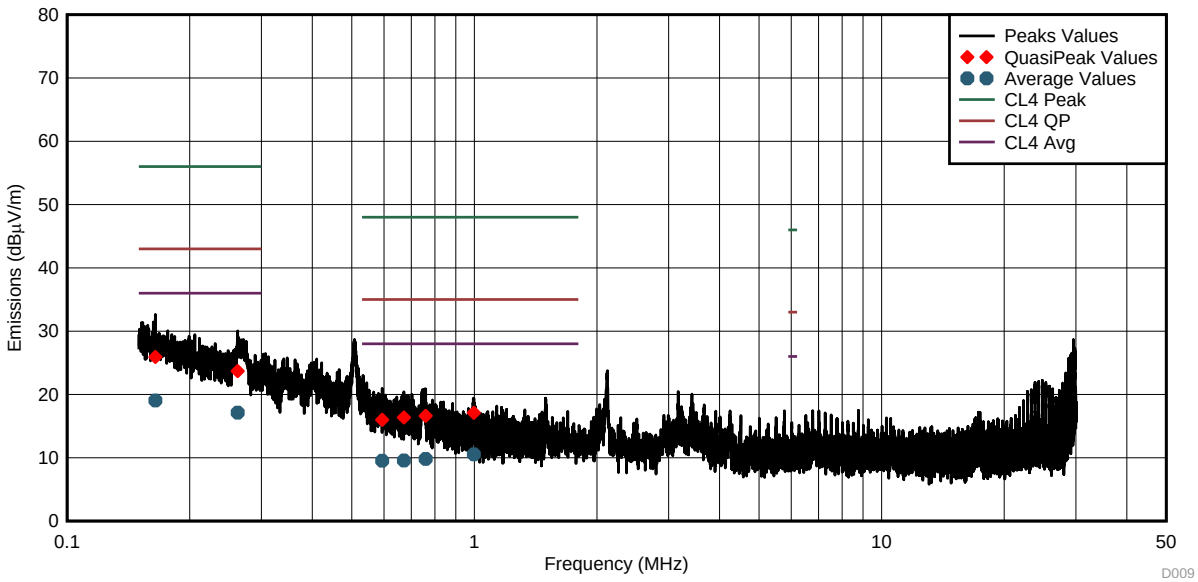


图 40. Dipole Antenna Test Results

Next to measure the emissions for the frequency range of 30 MHz to 200 MHz, a biconical antenna was used. The emissions measurements for this antenna must be performed in both the horizontal and vertical orientations. 图 41 shows the biconical antenna in the horizontal orientation that is 1 m in front of the test setup (test run two), 图 42 shows the radiated emissions results for this setup.

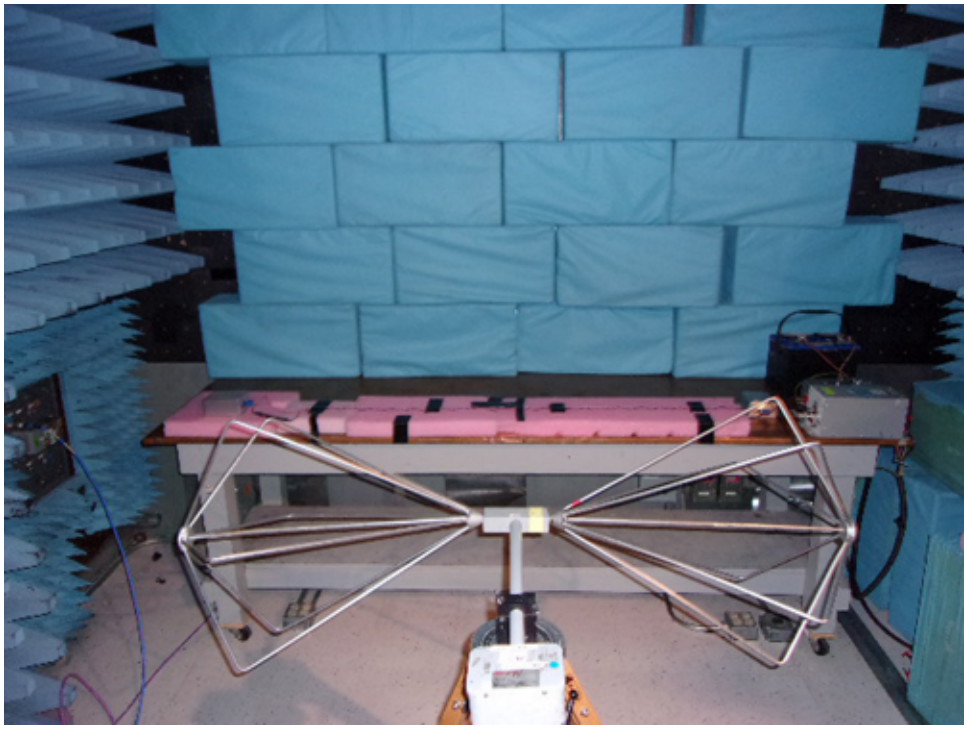


图 41. Biconical Antenna in Horizontal Orientation Test Setup

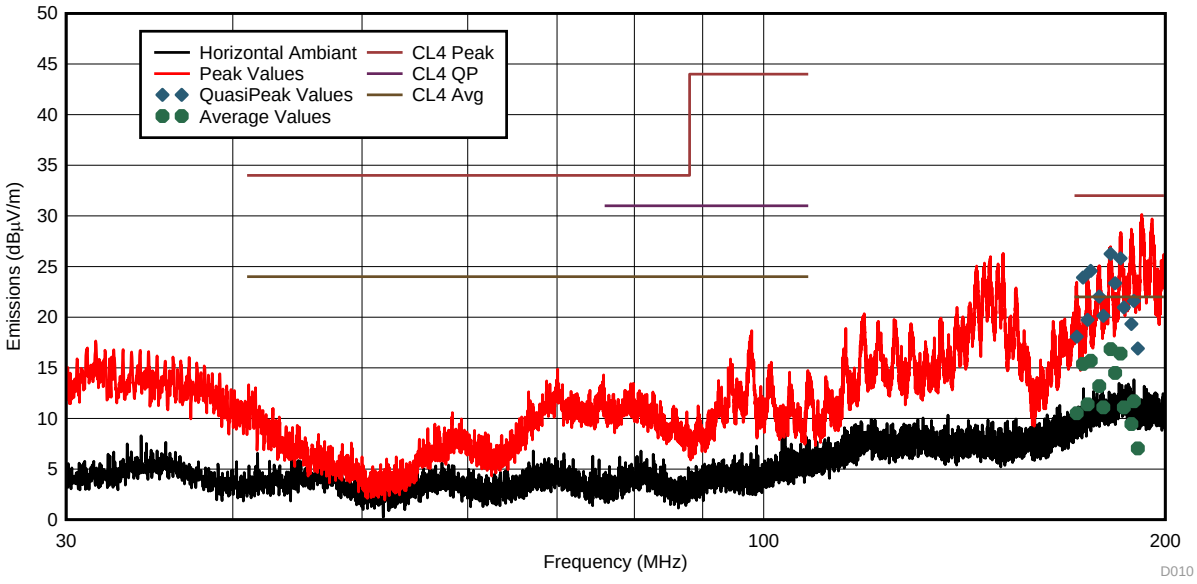


图 42. Horizontal Biconical Antenna Test Results

After running the emissions measurements in the horizontal orientation, the antenna was turned to the vertical orientation as shown in 图 43 (test run three). The results are shown in 图 44.

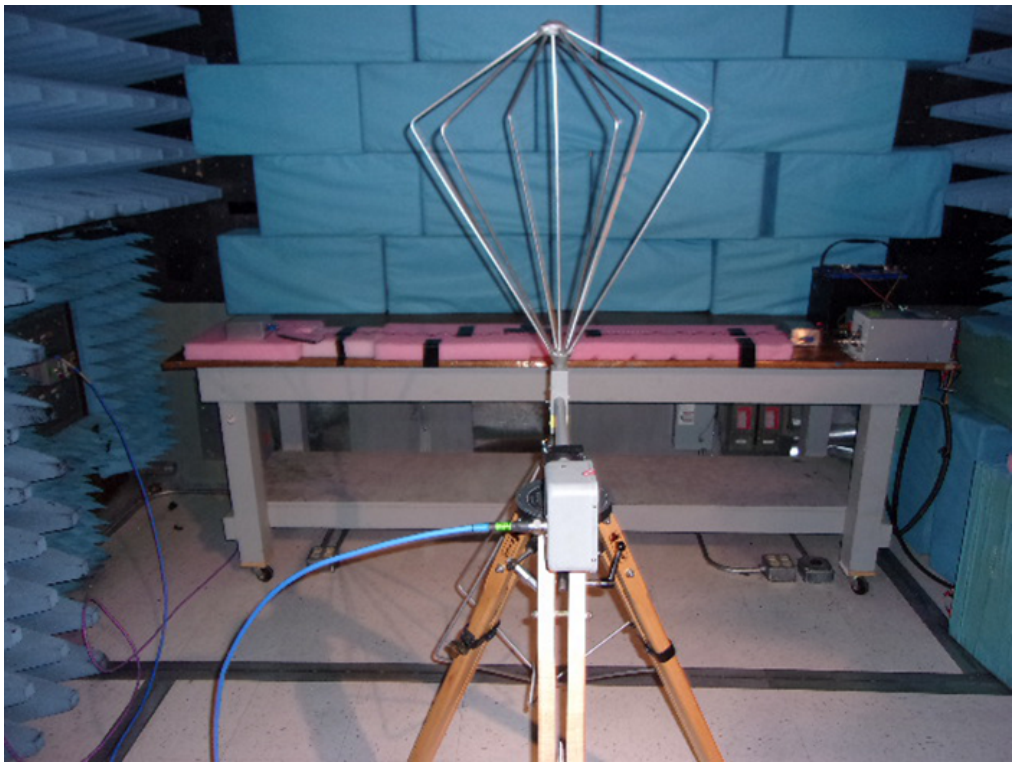


图 43. Biconical Antenna in Vertical Orientation Test Setup

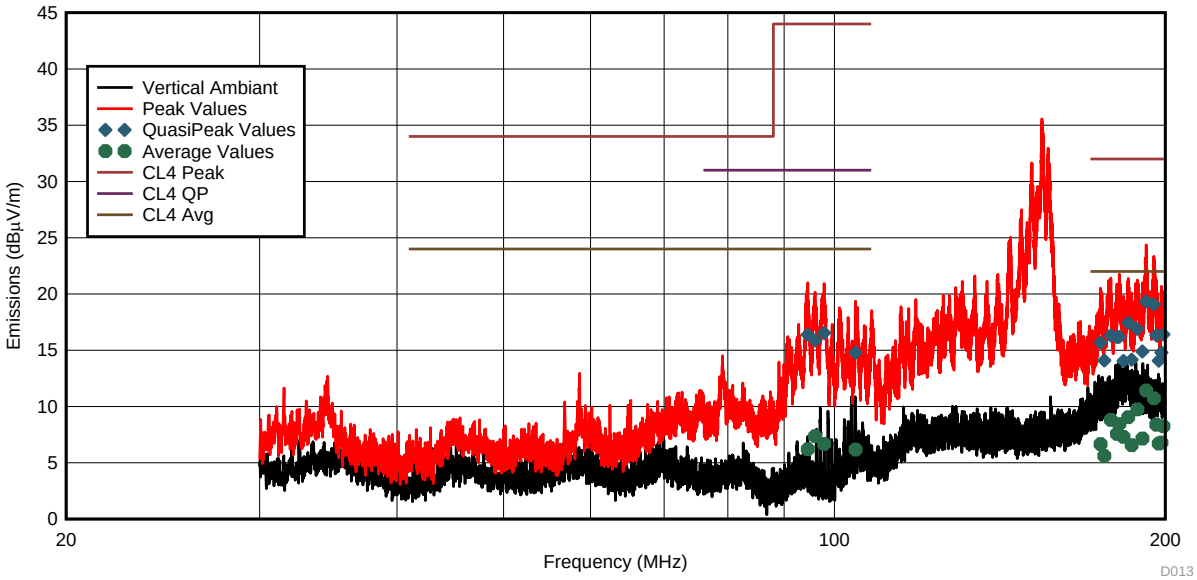


图 44. Vertical Biconical Antenna Test Results

Lastly to measure the emissions for the frequency range of 200 MHz to 1000 MHz, a logarithmic antenna was used. Again, the emissions measurements with this antenna must be performed in both the horizontal and vertical orientations. 图 45 shows the logarithmic antenna in the horizontal orientation that is 1 m in front of the test setup (test run four), and 图 46 shows the radiated emissions results for this setup.

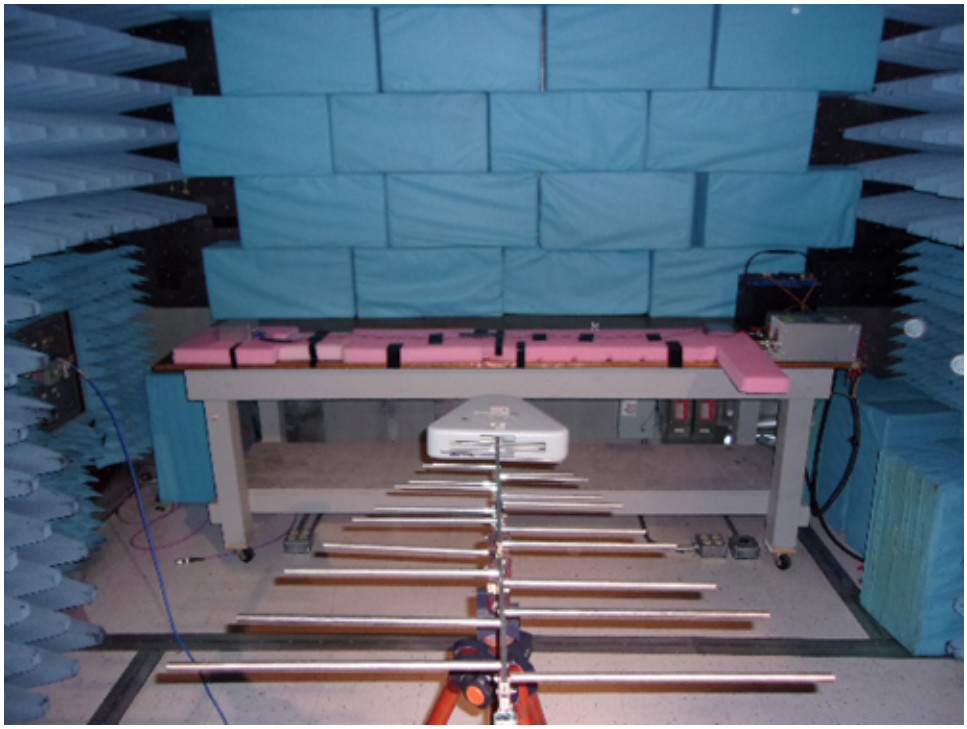


图 45. Logarithmic Antenna in Horizontal Orientation Test Setup

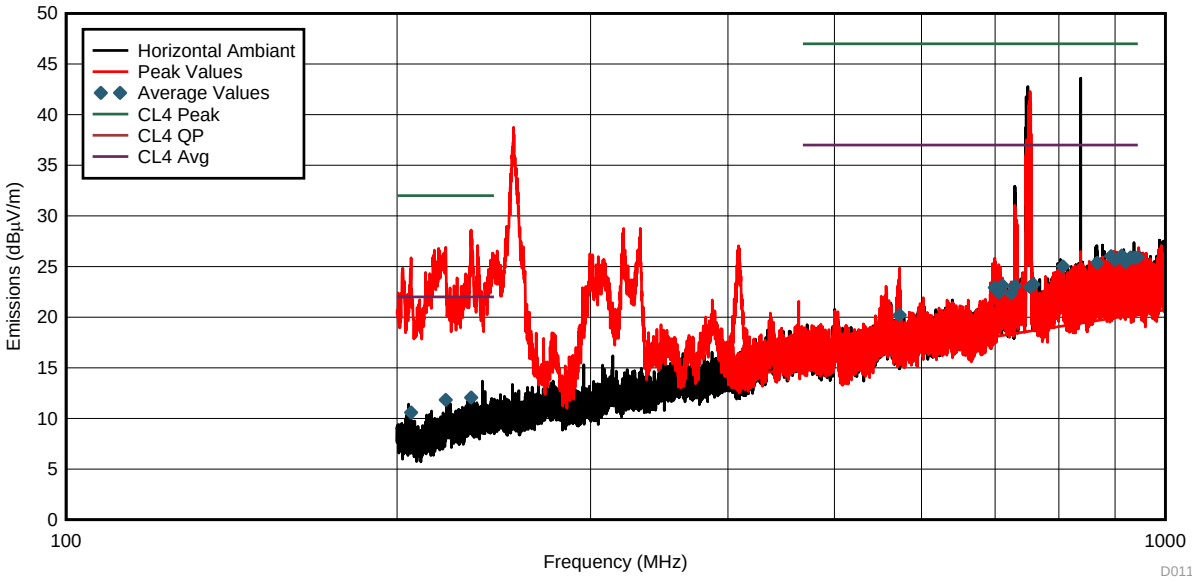


图 46. Horizontal Logarithmic Antenna Test Results

After running the emissions measurements in the horizontal orientation the antenna was turned to the vertical orientation as shown in 图 47 (test run five). The results are shown in 图 48.

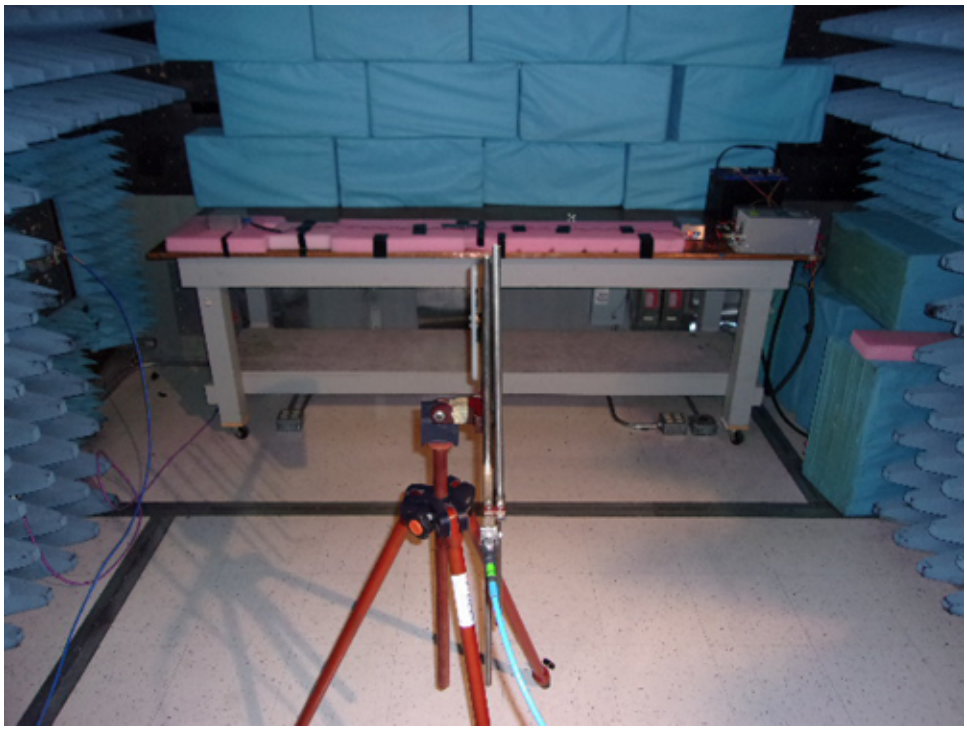


图 47. Logarithmic Antenna in Vertical Orientation Test Setup

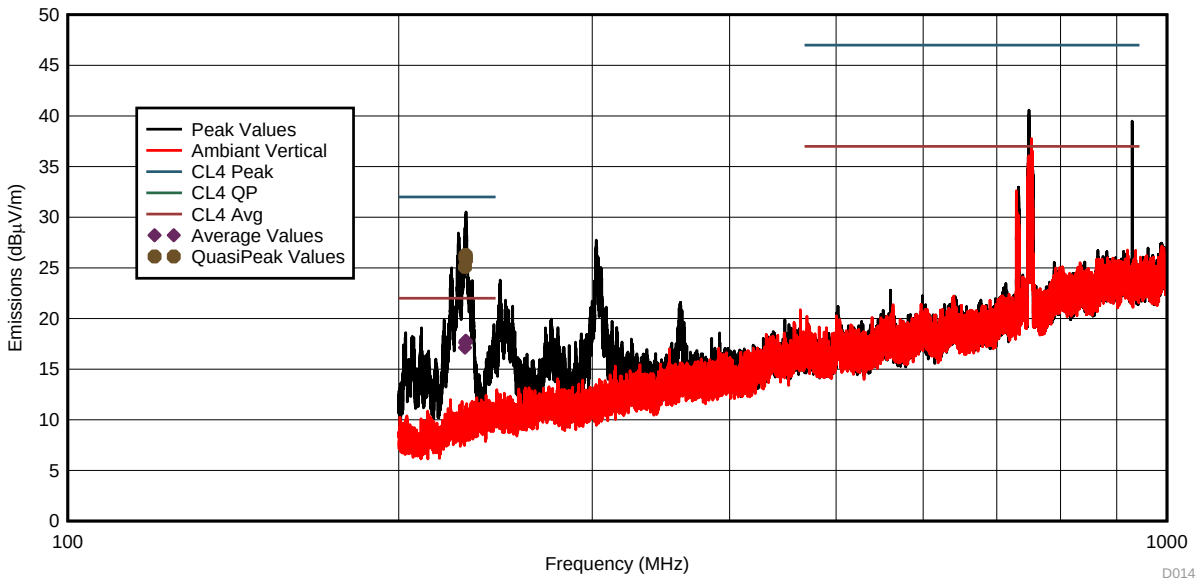


图 48. Vertical Logarithmic Antenna Test Results

3.2.10 CISPR 25 Conducted Emissions Testing - Voltage Method

Conducted emissions testing was also performed using a pair of modules in an anechoic chamber. The test methodology followed was the *Conducted emissions from components / modules - Voltage method* per the CISPR 25 Edition 4.0 standard. In this test, supply lines between the connector of the module and the artificial network (sometimes referred to as a line impedance stabilization network or LISN) must be between 200-mm and 400-mm long. The same two modules with a 1.7-m harness between them were used for this testing. Both the slave node and the master node were placed on top of a low-relative permittivity support. 图 49 shows this test setup.

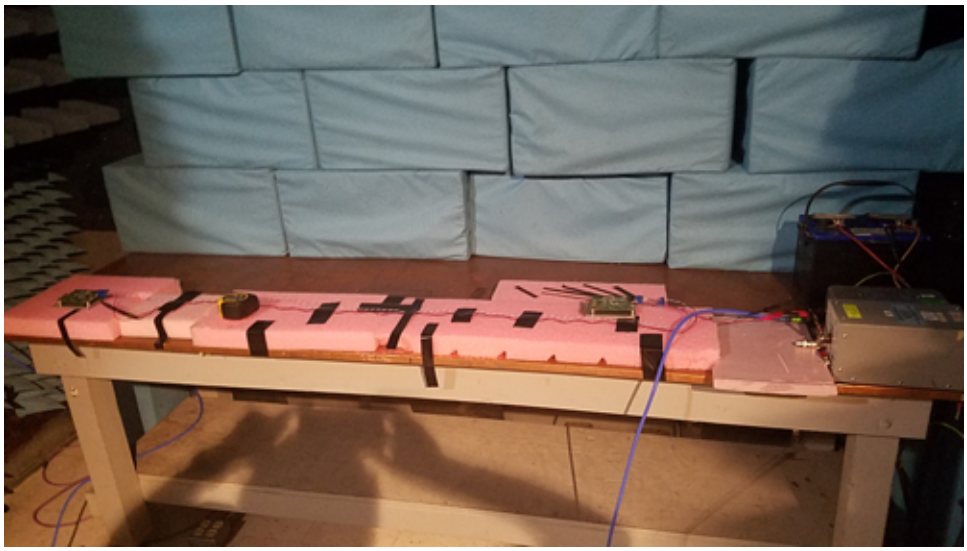


图 49. Conducted Emissions Setup

This test is performed two times—one on the positive power supply line and a second on the power return line (ground). The measurement is performed by connecting the spectrum analyzer to the measuring port of the artificial network for the battery supply line to the measuring port of the artificial network for the power return line, which is shown in 图 50.

图 50. Two Artificial Networks With Measuring Ports for Conducted Emissions Testing

As shown in 图 51 and 图 52, the TIDA-01428 passes the CISPR 25 conducted emissions using the voltage method with the Class 4 limit lines.

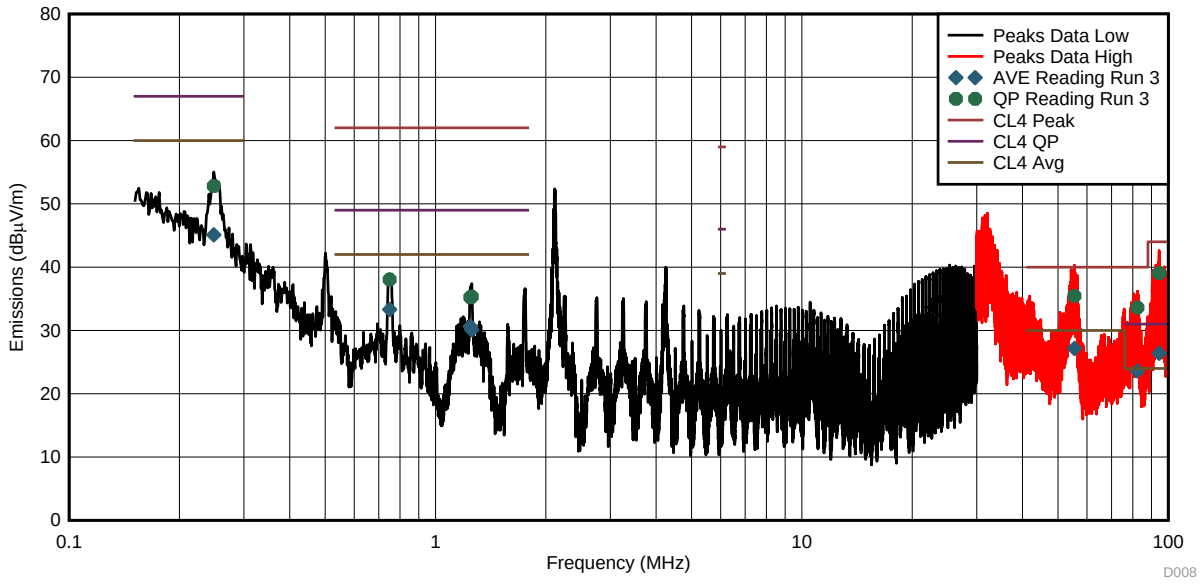


图 51. Conducted Emissions Results for Power Supply Line

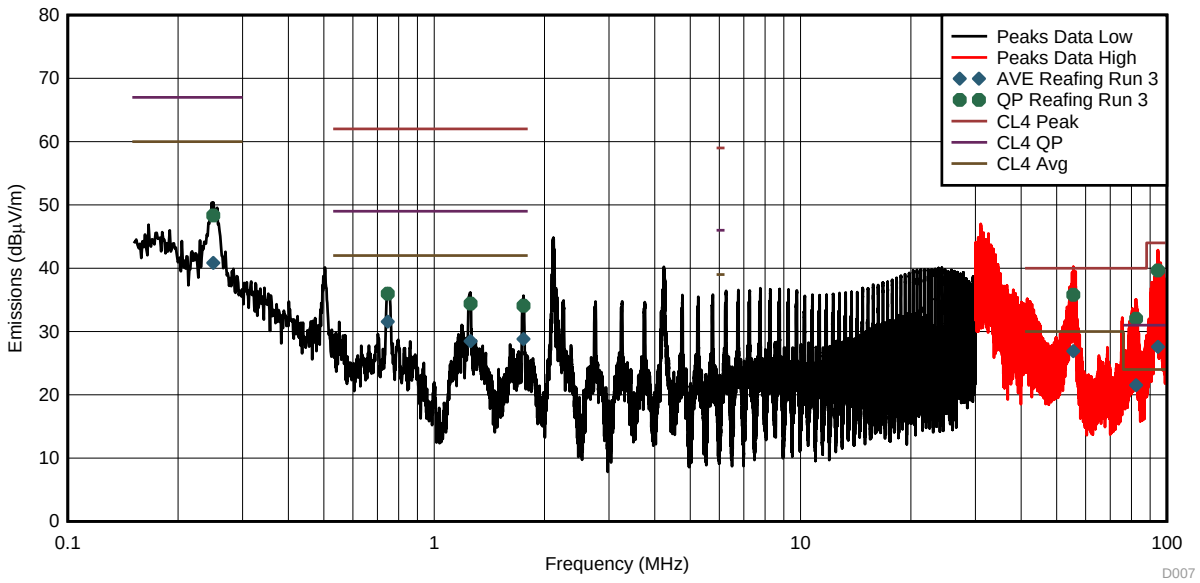


图 52. Conducted Emissions Results for Power Return Line

3.2.11 ISO 11452-4 Bulk Current Injection Immunity Testing

BCI testing is an immunity test defined by ISO 11452-4 where noise is coupled onto a wire harness through a current injection probe. The amplitude at each frequency point is increased until there is a failure or the required level has been reached. To pass this immunity test, the module must continue to operate normally at all test frequencies for amplitudes greater than or equal to the limit line. This test was performed with all four conductors of the wire harness run through the current injection probe with the probe 450 mm from the slave node and 750 mm from the slave node.

The health of the units were monitored by monitoring the status LEDs using a coaxial camera feed that was run out of the shielded room to a television.

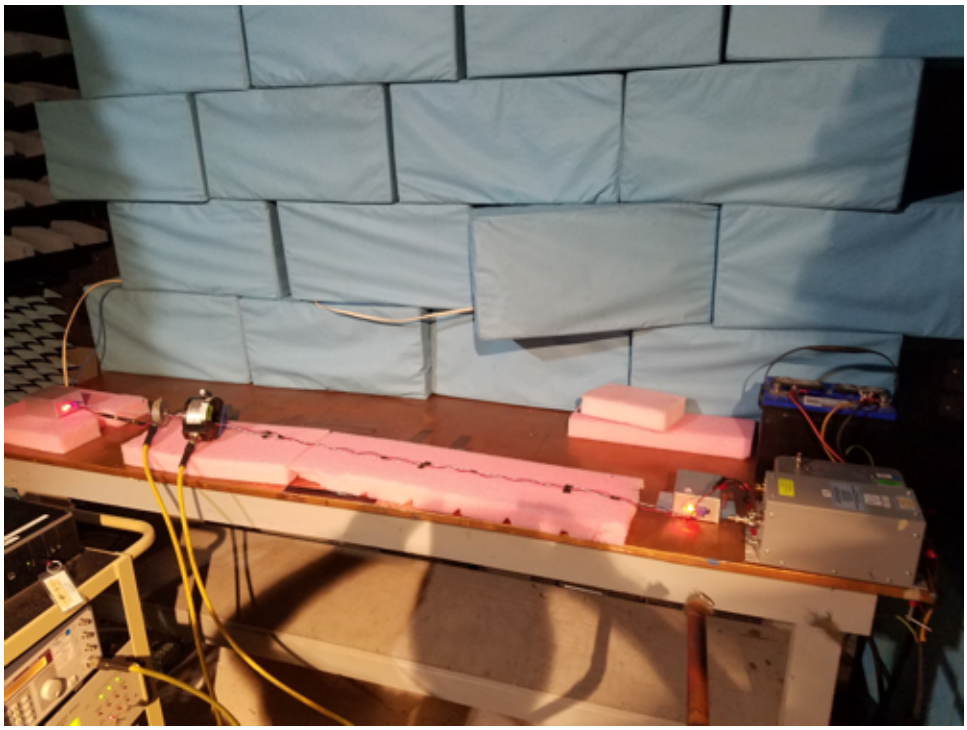


图 **53. Bulk Current Injection Test Setup**

图 54 shows the immunity performance when the current injection probe was placed 450 mm from the slave node, and 图 55 shows the immunity performance when the current injection probe was placed 750 mm from the slave node. As shown, neither test showed any deviations.

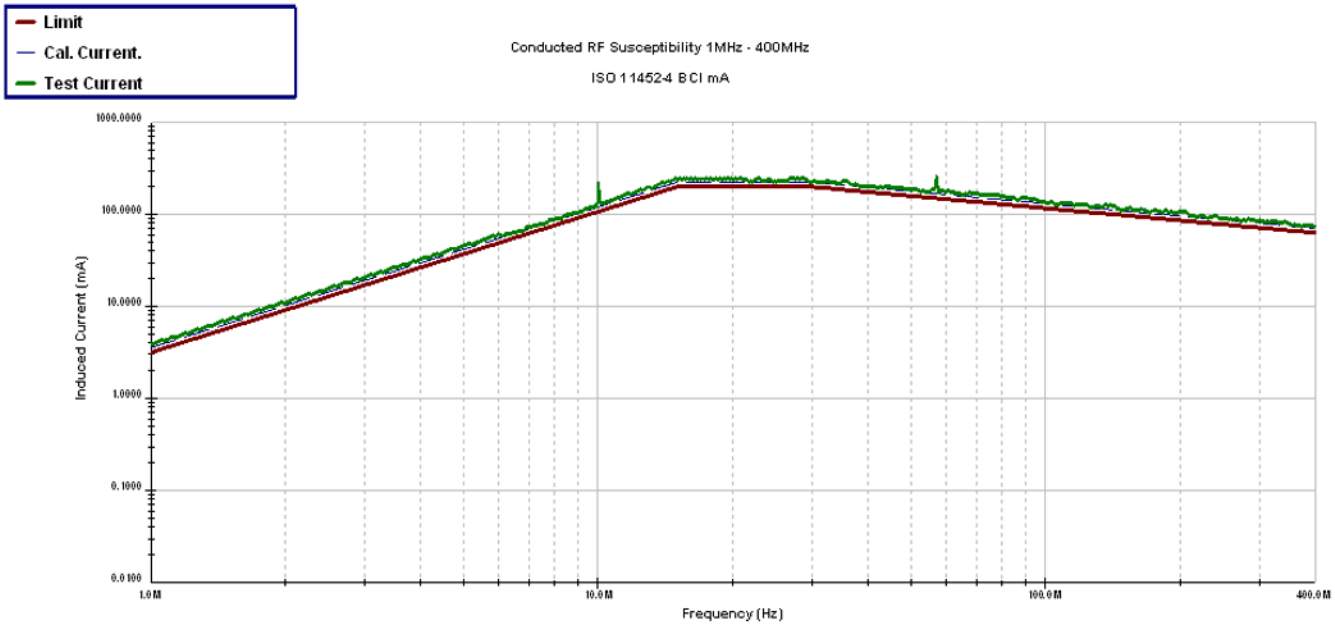


图 54. BCI Results With Probe at 450 mm

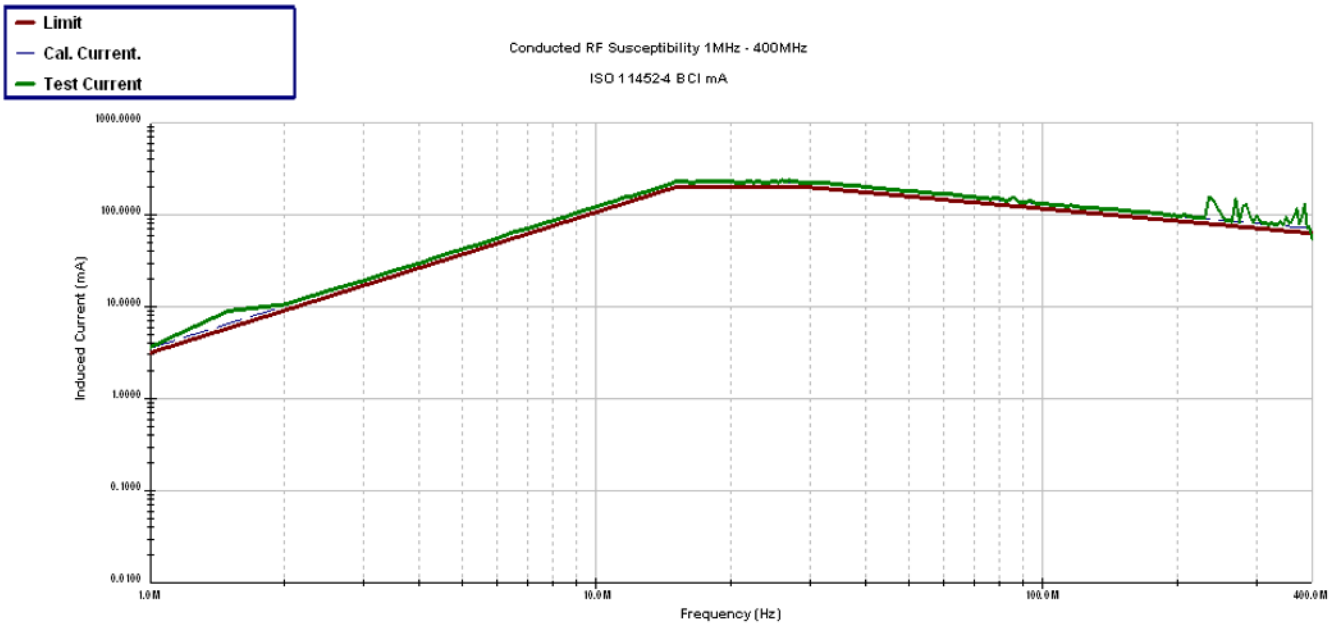


图 55. BCI Results With Probe at 750 mm

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01428.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01428.

4.3 PCB Layout Recommendations

This section will discuss the layout considerations for the buck converter, boost converter, and CAN physical layer interface, the board stackup, and link to the layer plots for the PCB.

4.3.1 Buck Converter Layout Considerations

The following list of layout recommendations is in order of importance starting with the most important items for the LM53601-Q1:

- Place high-frequency input bypass capacitor as close to the LM53601-Q1 device as possible.
- Connect AGND and GND to the DAP (exposed thermal pad) immediately adjacent to the LM53601-Q1 device.
- Do not interrupt the ground plain under the loop containing the VIN and GND pins and the high frequency input bypass capacitor of the LM53601-Q1 device.
- The boot capacitor should be close to the LM53601-Q1, and the loop from the SW pin, through the boot capacitor, and into the BOOT pin should be kept as small as possible.
- Keep the SW node as small as possible. The node should be wide enough to carry the converter's full current without significant drop.
- 4.7 μF of bypassing should be close to the input of the LM53601-Q1 devices.
- Place the VCC pin's bypass capacitor and the bypass capacitor for FB pin as close to the LM53601-Q1 device as possible.
- The first output the trace from the output inductor to the output node should run by an output capacitor before joining the rest of the output node.
- Keep 10-μF close to the output (output inductor and GND) of the LM53601-Q1 device.
- Clear the layer beneath the SW node.

4.3.2 Boost Converter Layout Considerations

The following are some guidelines to follow for the TPS61240-Q1 layout:

- Use wide and short traces for the main current path and for the power ground tracks.
- The input and output capacitor, as well as the inductor, should be placed as close as possible to the IC.
- Connect the exposed thermal pad to the GND plane and place multiple thermal vias below the thermal pad to enhance the thermal performance.

4.3.3 CAN Physical Layer Layout Considerations

Because the CAN physical layer is an external wired interface and can be subjected to transients with frequencies ranging from hundreds of Hz to 3 GHz, high-frequency layout techniques must be applied during PCB design. The following are some guidelines to follow for the TCAN1042V-Q1 layout:

- TVS diodes and bus filtering capacitors should be placed as close to the onboard connectors as possible to prevent noisy transient events from propagating further into the PCB and system.
- Provide low-inductance supply and ground connections.
- Use at least two vias in parallel when connecting a power net to another layer on the PCB. This will minimize trace inductance.
- Bypass and bulk capacitors should be placed as close as possible to the supply terminals of transceiver (VCC and VIO).

4.3.4 Board Layer Stackup

The board has been designed using two layers. Both top and bottom layers have signals and power traces routed. Additionally, a majority of the bottom layer has been used for a large, low-impedance ground plane. See 表 5 for the board stackup. The board uses standard 1-oz copper foil on top and bottom layers, and the total board thickness is approximately 63 mils.

表 5. TIDA-01237 Board Layer Stackup

LAYER NAME	TYPE	MATERIAL	THICKNESS (MIL)	DIELECTRIC MATERIAL	DIELECTRIC CONSTANT
Top overlay	Overlay	—	—	—	—
Top solder	Solder mask	Surface material	0.4	Solder resist	3.5
Top layer	Signal	Copper	1.4	—	—
Dielectric1	Dielectric	Core	59.2	FR-4	4.8
Bottom layer	Signal	Copper	1.4	—	—
Bottom solder	Solder mask	Surface material	0.4	Solder resist	3.5
Bottom overlay	Overlay	—	—	—	—

4.3.5 Layout Prints

To download the layer plots, see the design files at TIDA-01428.

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01428.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01428.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01428.

5 Related Documentation

1. Texas Instruments, *LM53601-Q1 1A, 36V Synchronous, 2.1MHz, Automotive Step Down DC-DC Converter*, LM53601-Q1 Datasheet (SNAS660)
2. Texas Instruments, *TPS61240-Q1 3.5-MHz High Efficiency Step-Up Converter*, TPS61240-Q1 Datasheet (SLVSAO4)
3. Texas Instruments, *TCAN1042-Q1 Automotive Fault Protected CAN Transceiver with CAN FD*, TCAN1042V-Q1 Datasheet (SLLSES9)
4. Texas Instruments, *TMS320F2803x Piccolo™ Microcontrollers*, TMS320F28030 Datasheet (SPRS584)
5. Texas Instruments, *Automotive Catalog Dual Inverter Buffer/Driver with Open-Drain Output*, SN74LVC2G06-Q1 Datasheet (SCES617)
6. Texas Instruments, *CSD17313Q2 30-V N-Channel NexFET™ Power MOSFET*, CSD17313Q2 Datasheet (SLPS260)

5.1 商标

6 Terminology

Body control module— An automotive electronic control unit responsible for monitoring and controlling vehicle loads. Some examples include interior lighting, exterior lighting, heating ventilation and air conditioning (HVAC), powered windows, and powered door locks.

Discrete SBC— The term Discrete SBC (System Basis Chip) is refers to the discrete implementation of functional blocks that are commonly integrated into a single IC. This included power and networking blocks.

Converter— The term converter is used when referring to a power regulator that has integrated FETs.

7 About the Author

JOHN P. GRIFFITH is a systems engineer at Texas Instruments. As a member of the Automotive Systems Engineering team, John specializes on body control modules and gateway modules, creating end equipment block diagrams, and reference designs for automotive customers. John earned his bachelor of science and master of science in electrical engineering from Rochester Institute of Technology in Rochester, New York.

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