TI Designs：TIDA-01442
采用 ADC12DJ3200 且适用于 L、S、C 和 X 频带的直接射频采样雷达接收器参考设计

说明

TIDA-01442 TI 设计利用 ADC12DJ3200 EVM 演示直接射频采样接收器，适用于在 HF、VHF、UHF L、S、C 和部分 X 频带上运行的雷达。模数转换器 (ADC) 的宽模拟输入带宽和高采样率 (6.4GSPS) 可为单接收器或 ADC 提供多频带覆盖。该 ADC 具有直接射频采样功能，取消了对多个降频转换级的需求，减少了组件数量，因此降低了系统整体的复杂性。

资源

TIDA-01442	设计文件夹
ADC12DJ3200	产品文件夹
LMK04828	产品文件夹
LMX2582	产品文件夹
TSW14J57EVM	产品文件夹

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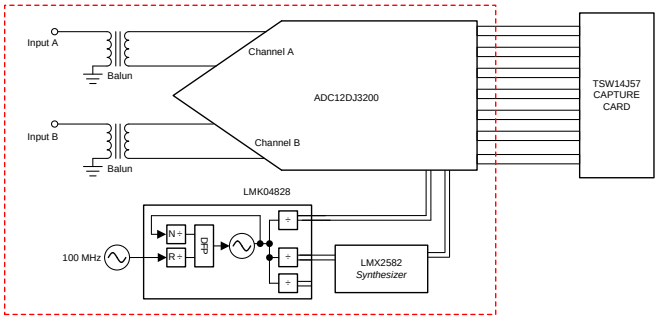
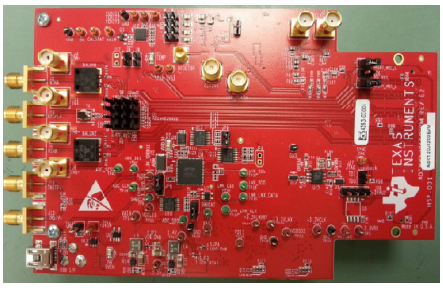
特性

- ADC 的高输入频率功能允许对从 L 频带到 X 频带的信号进行射频采样
- 单通道（交错模式）下的最大采样率为 6.4GSPS，双通道模式下的最大采样率为 3.2GSPS
- 每个 DDC 都具有四个独立的 NCO，可在多个频带中实现快速跳频
- 针对低抖动和 JESD204B 运行而优化的时钟解决方案

应用

- 军用雷达
- 气象雷达
- 空中交通控制雷达
- 测试和测量





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1 System Description

The TIDA-01442 reference design demonstrates an AC-coupled, dual-channel wideband digitizer used for radar receiver applications. This design is based on the dual-channel, 12-bit, 3.2-GSPS ADC12DJ3200. Both channel A and channel B are AC coupled using a 9-GHz bandwidth balun. This design showcases the high sample rate 6.4 GSPS and wide bandwidth capabilities of the ADC12DJ3200. Both input channels have been optimized for wide bandwidth performance. This design focuses on demonstrating the performance of the device over 9 GHz of bandwidth in addition to discussing clocking and power management.

1.1 Key System Specifications

表 **1. Key System Specifications**

PARAMETER	SPECIFICATIONS
Analog input signal bandwidth	9 GHz
Resolution	12 bit
Max sampling rate	6.4 GSPS in single channel interleaved and 3.2 GSPS in dual-channel input mode
Number of channels	2
SNR	> 44 dBFS across full bandwidth
Harmonic distortion	< –46 dBFS HD2/HD3 across full bandwidth

2 System Overview

2.1 Block Diagram

图 1 shows the block diagram for the TIDA-01442 reference design. As the figure shows, a single-ended input signal can be applied at each input channel. The single-ended input signal is converted to a differential signal with a 9-GHz bandwidth balun. Both input paths can also be modified to accept differential input signals. The clocking for ADC is also implement on the evaluation module (EVM). LMX2582 is used for clocking the ADC and LMK04828 is used for providing the SYSREF signal for the ADC and field-programmable gate array (FPGA), along with any additional clocking required by the FPGA.

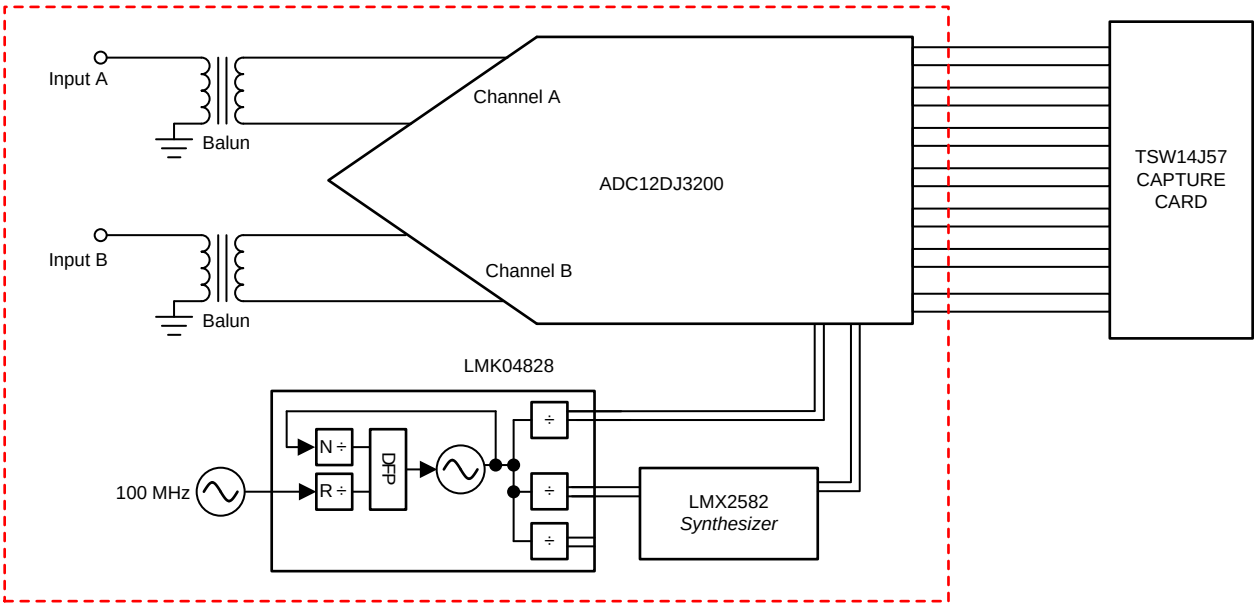

图 1. TIDA-01442 Block Diagram

2.2 Highlighted Products

2.2.1 ADC12DJ3200

The ADC12DJxx00 family are RF-sampling gigasample ADCs that can directly sample input frequencies from DC to above 9 GHz. In dual-channel mode, the ADC12DJ3200, ADC12DJ2700, and ADC12DJ1600 can sample up to 3200 MSPS, 2700 MSPS or 1600 MSPS. In single-channel mode, the devices can sample up to 6400 MSPS, 5400 MSPS, or 3200 MSPS, respectively. With a –3-dB input bandwidth exceeding 9 GHz in either dual- or single-channel mode, the ADC12DJ3200/2700/1600 can be used to sample signals in the first, second, and higher Nyquist zones.

ADC12DJxx00s use a high-speed JESD204B output interface with up to 16 serialized lanes and support subclass-1 for deterministic latency and multi-device synchronization. The serial output lanes support up to 12.8 Gbps and can be configured to trade off bit rate versus number of lanes. In dual-channel mode, optional digital-down converters can tune and decimate a band from RF to a complex baseband signal to reduce the interface data rate in bandwidth-limited applications.

2.2.2 LMK04828

The LMK0482x family is the industry's highest-performance clock conditioner with JEDEC JESD204B support. The 14 clock outputs from PLL2 can be configured to drive seven JESD204B converters or other logic devices using device and SYSREF clocks. SYSREF can be provided using both DC and AC coupling. This device is available in a 64-pin QFN package (9 mm × 9 mm).

2.2.3 LMX2582

The LMX2582 is a low-noise, wideband RF phase-locked loop (PLL) with integrated VCO that supports a frequency range from 20 MHz to 5.5 GHz. The device supports both fractional-N and integer-N modes with a 32-bit fractional divider allowing fine frequency selection. Integrated noise of 47 fs for a 1.8-GHz output allows for an ideal low-noise source. The device is available in a 40-pin WQFN (6 mm × 6 mm).

3 System Design Theory

3.1 Clocking

图 2 shows a block diagram of the clocking subsystem, which comprises an LMK04828 JESD204B clock conditioner, LMX2582 synthesizer, 100-MHz voltage-controlled crystal oscillator (VCXO), ADC, and LMK SMA clock inputs. The two main ways to clock the ADC are onboard clocking and external clocking.

Onboard clocking:

- By default, the ADC12DJ3200EVM is set up to use onboard clocking. When using the default onboard clocking option for the ADC EVM, the LMX2582 is used as a clock source for the ADC and LMK04828 is used for providing the SYSREF for the ADC and the FPGA, in addition to being used for clocking the FPGA. The VCXO is used as a reference for both LMK04828 and LMX2582. In this mode, there is an option to lock the VCXO to an external source by providing a 10-MHz reference clock to connector J38.

External clocking:

- If external clocking is desired, the clock from the external signal generator is provided to the ADC EXT CLK (J18) input connector and LMK EXT CLK (J22) connector. The LMK04828 device is used to provide the SYSREF and CLK to the FPGA as well as the SYSREF to ADC. In external clock mode, the LMX2582 is powered down. When using external clocking mode, C49 and C52 must be installed and C48, C50, C51, and C53 must be uninstalled.

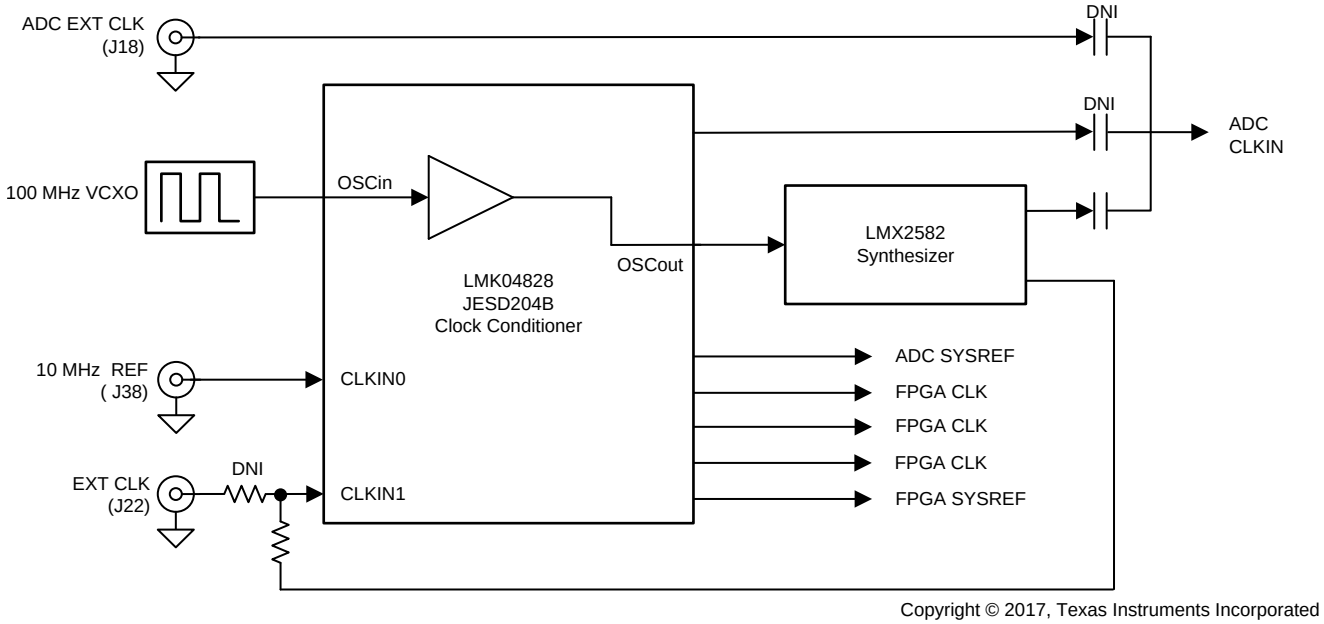

图 2. Clocking

3.2 Power

This ADC12DJ3200EVM operates from a single +5-V power supply, which powers a combination of switching and linear regulators that are used to power the various domains on the board. 图 3 shows a block diagram of the power management.

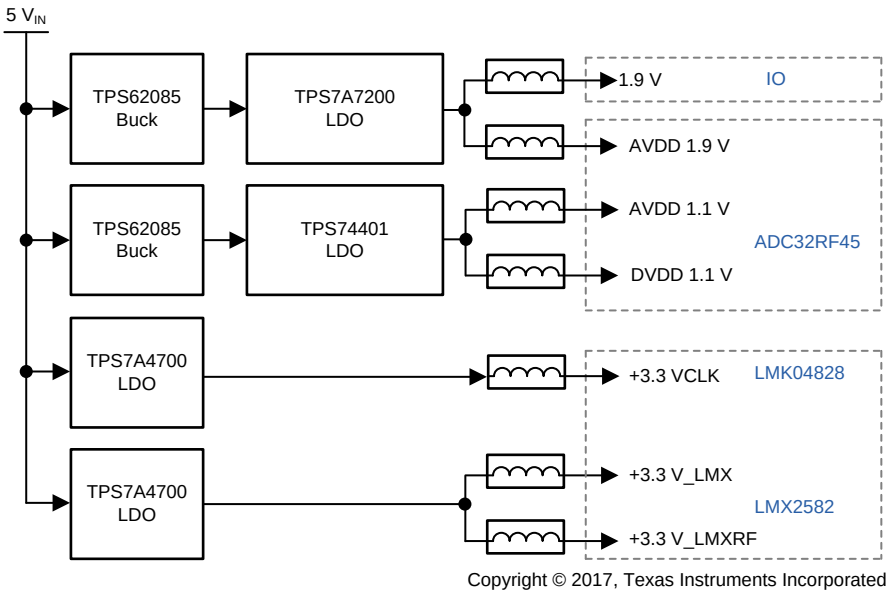

图 3. Power Management Block Diagram

4 Getting Started Hardware and Software

4.1 Required Hardware

The required hardware for the TIDA-01442 design is as follows:

- ADC12DJ3200 EVM
- TSW14J57 EVM
- Signal generator

4.1.1 ADC12DJ3200

See the ADC12DJ3200EVM tool folder at http://www.ti.com/tool/ADC12DJ3200EVM for a detailed description.

4.1.2 TSW14J57

See the TSW14J57 EVM tool folder at http://www.ti.com/tool/tsw14j57evm for a detailed description.

4.1.3 Test Setup

The performance measurements of the ADC were taken using the setup shown in 图 4. In the setup, a 3.2-GHz clock signal generated by LMX2582 (onboard) is sent to the ADC and LMK04828 (onboard). The LMK04828 is a JESD204B-compliant clock jitter cleaner and is used to provide the SYSREF signals and other required clock signals to the ADC and TSW14J57. The input signal for the ADC is provided by the Agilent Technologies E8257D signal source. The input signal is filtered using a tunable band-pass filter and applied at the channel A or channel B input of the ADC. The input signal and clock are synchronized to each other by feeding a 10-MHz reference signal from the signal source to the LMK04828 device. The ADC12DJ3200 EVM is connected to the TSW14J57 capture card to capture the output digital data of the ADC. The captured data is processed using the High Speed Data Converter (HSDC) Pro software. Both boards are powered by +5-V supplies (through barrel connectors) and connect to a PC through USB cables.

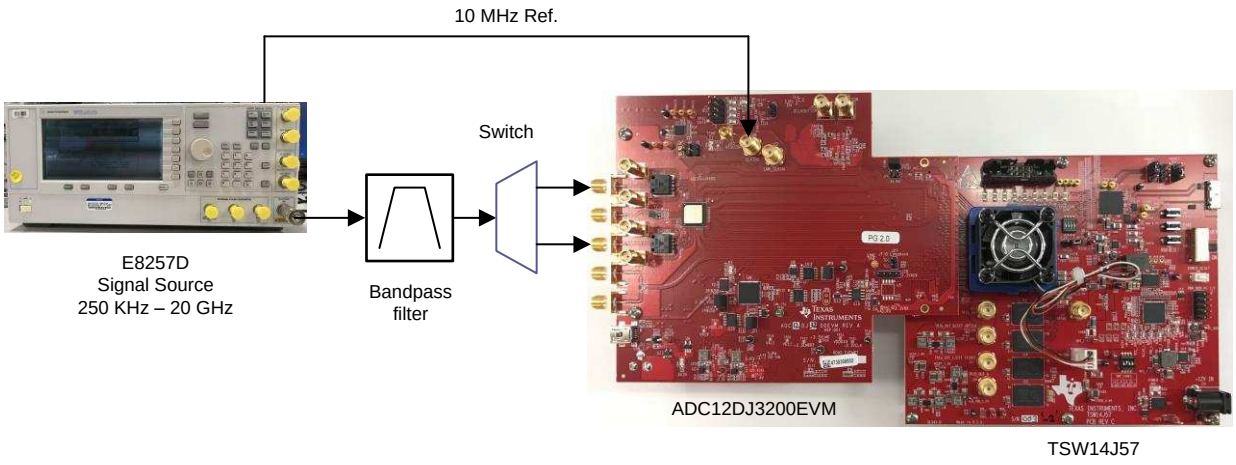

图 4. Test Setup Diagram

4.2 Software

4.2.1 ADC12DJ3200 GUI

The ADC12DJ3200EVM board must be configured through the ADC12DJ3200 GUI before conversions can be captured. After launching the GUI, the first step is to select the *On-board* option using the drop-down menu under the *#1. Clock Source* field. Then set the clocking frequency to *Fclk = 3200 MHz* using the drop-down menu under the *#2a. On-board Fclk Selection* (see 图 5). The next step is to select JMODE0 if taking single-channel interleaved measurements or *JMODE3* if taking dual-channel measurements. In single-channel interleaved mode, the input single is applied to the single input channel. In this mode, both the rising edge and falling edge of the FCLK are used to sample the input signal, thus making the effective sampling rate 6.4 GSPS with a 3.2-GHz clock. Alternatively, in dual-channel mode, both the input channels are used with each channel to sample an input signal at 3.2 GSPS with a 3.2-GHz clock. The last step is to click the *Program Clocks and ADC* button and wait for the script to finish execution. This step completes the configuration and then the user can launch and configure the HSDC Pro GUI.

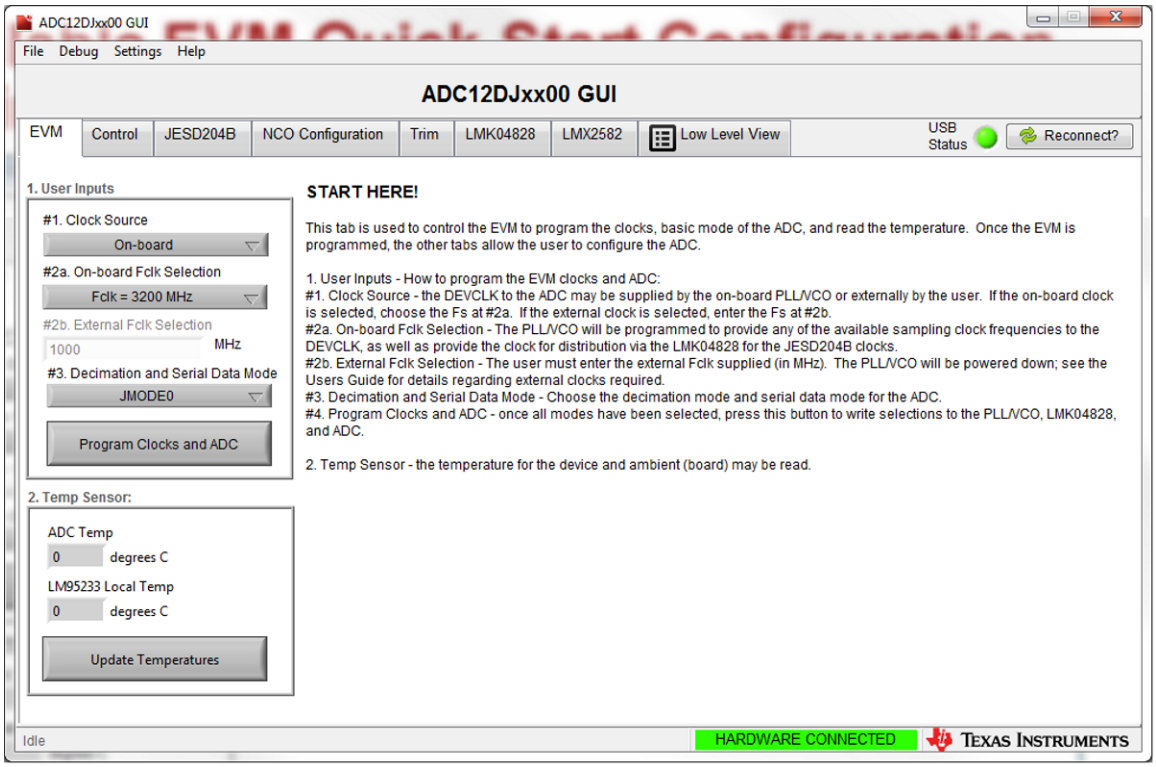

图 **5. ADC12DJ3200 GUI—Quick Setup**

4.2.2 HSDC Pro GUI

HSDCpro GUI works with a TSW14J57 capture card and is used to process and display data captured from the ADC12DJ3200. Download the HSDC Pro software from http://www.ti.com/tool/dataconverterpro-sw. As 图 6 shows, click on the drop-down menu and select "ADC32RF45_LMF_82820". Next set the *ADC Output Data Rate* to "6.4G" for single-channel interleaved mode and "3.2G" for dual-channel mode. The HSDC Pro software is now configured and data can be captured by clicking the *Capture* button.

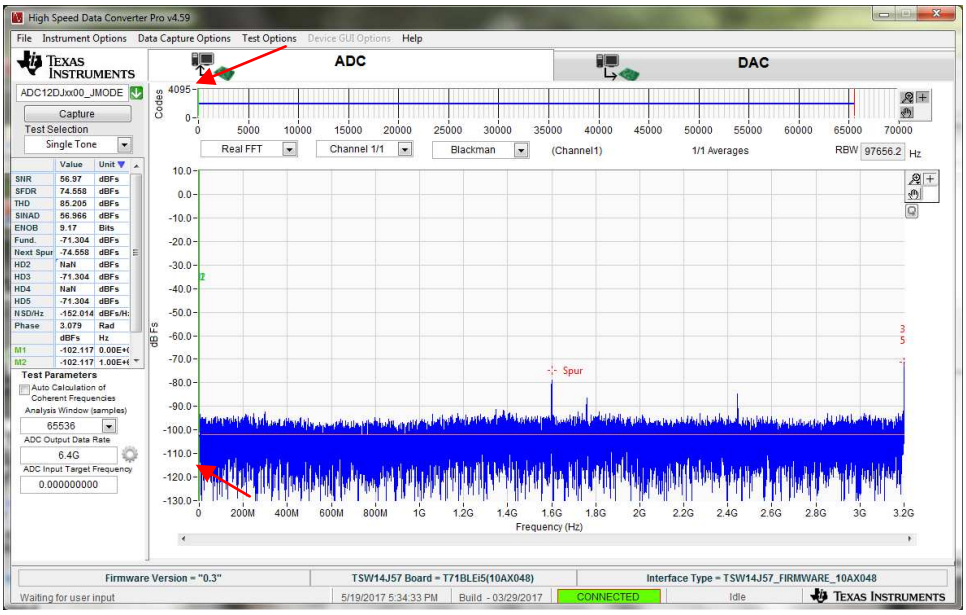

图 6. HSDC Pro GUI—Configuring Device and Sample Rate

图 6 also shows the fast Fourier transform (FFT) of captured data from the ADC12DJ3200EVM board. The HSDC Pro software provides a time domain and frequency domain analysis. The HSDC Pro software also provides single-tone FFT statistic parameters such as signal-to-noise ratio (SNR), spurious free dynamic range (SFDR), total harmonic distortion (THD), signal-to-noise and distortion ratio (SINAD), effective number of bits (ENOB), fundamental tone power, and HD2-5.

5 Testing and Results

A variety of measurements were taken to demonstrate the performance of ADC12DJ3200EVM board. A clean, filtered signal was fed into the ADC12DJ3200EVM board to test the performance and the SNR, HD2, HD3, and other various parameters were measured. The measurements were performed for both the single-channel interleaved mode (6.4 GSPS) and dual-channel mode (3.2 GSPS for each channel). JMODE0 was used for the single-channel interleaved mode. In JMODE0, the digital data from the ADC is sent to the capture card (FPGA) over eight serializer/deserializer (SerDes) lanes with a lane rate of 12.8 Gbps. JMODE3 was used for dual-channel measurements. In JMODE3, the digital data from the ADC is sent to the FPGA over 16 SerDes lanes with half the lane rate of JMODE0, which is 6.4 Gbps.

图 7 shows the SNR performance with a –1-dBFs input signal swept from 30 MHz to 10 GHz. The input signal was applied to channel A for single-channel interleaved mode. The input signal was applied to both channel A and channel B for dual-channel input measurement.

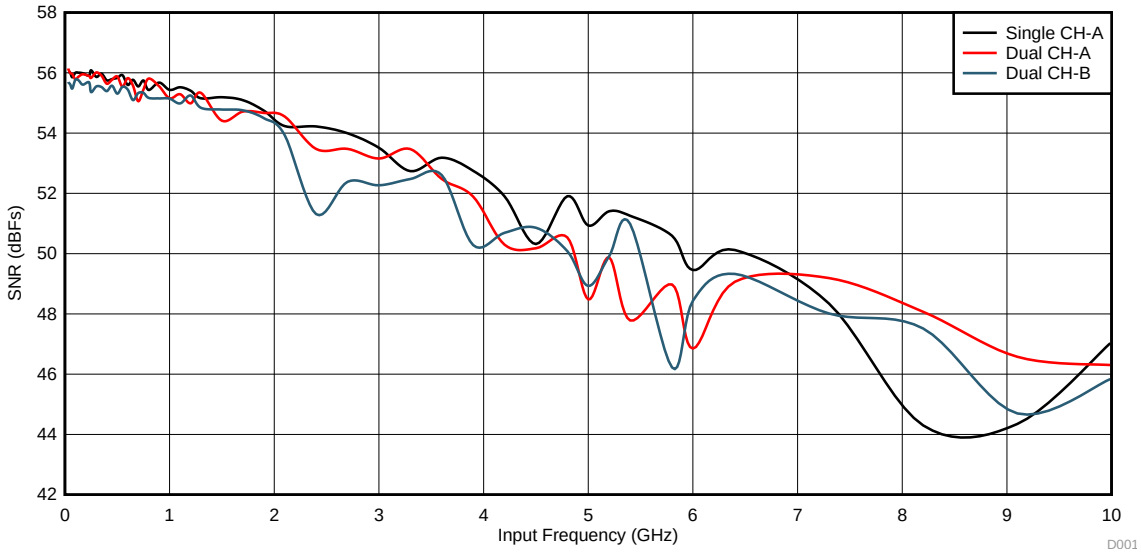

图 7. SNR for Interleaved Single- and Dual-Channel Modes

图 8 shows the THD for both single-channel interleaved mode and dual-channel mode.

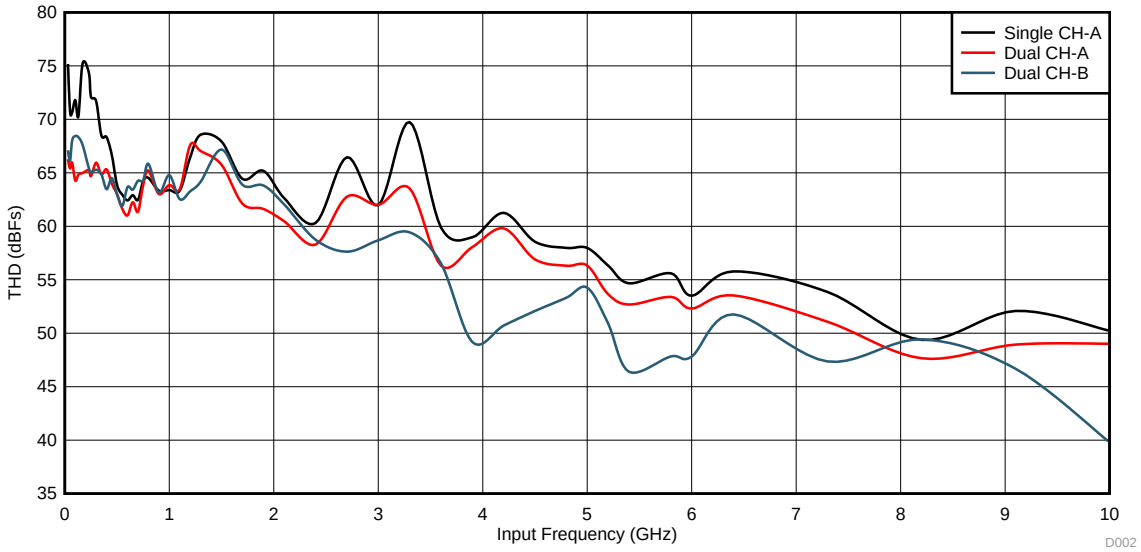

图 8. THD Performance for Single-Channel Interleaved Mode and Dual-Channel Mode

图 9 and 图 10 show the HD2 and HD3 performance for both single-channel interleaved mode and dual-channel mode.

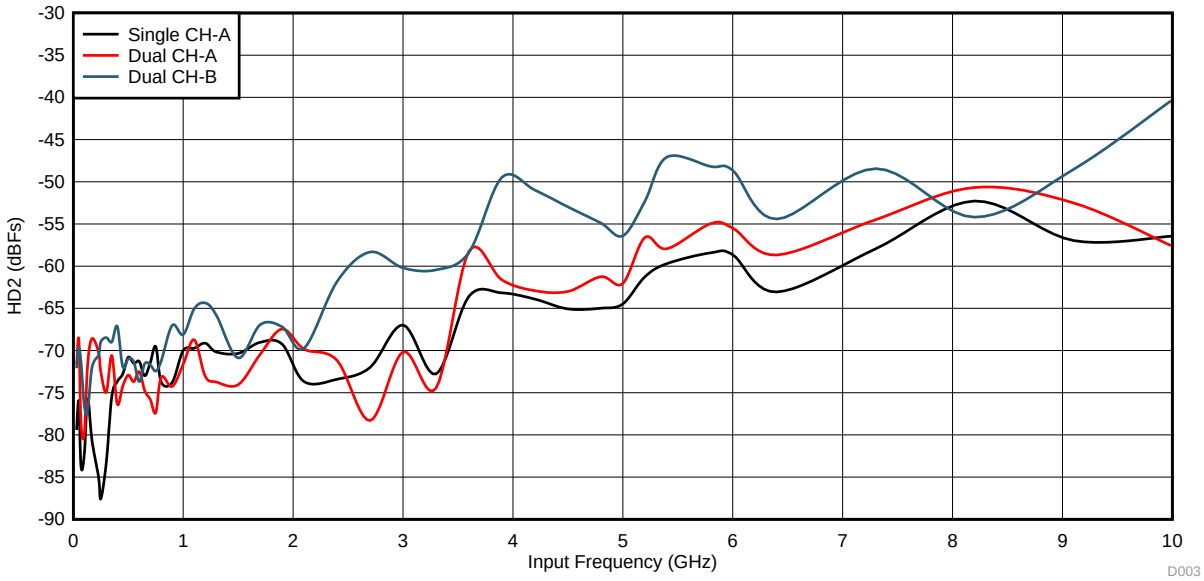

图 9. HD2 Performance for Single-Channel Interleaved Mode and Dual-Channel Mode

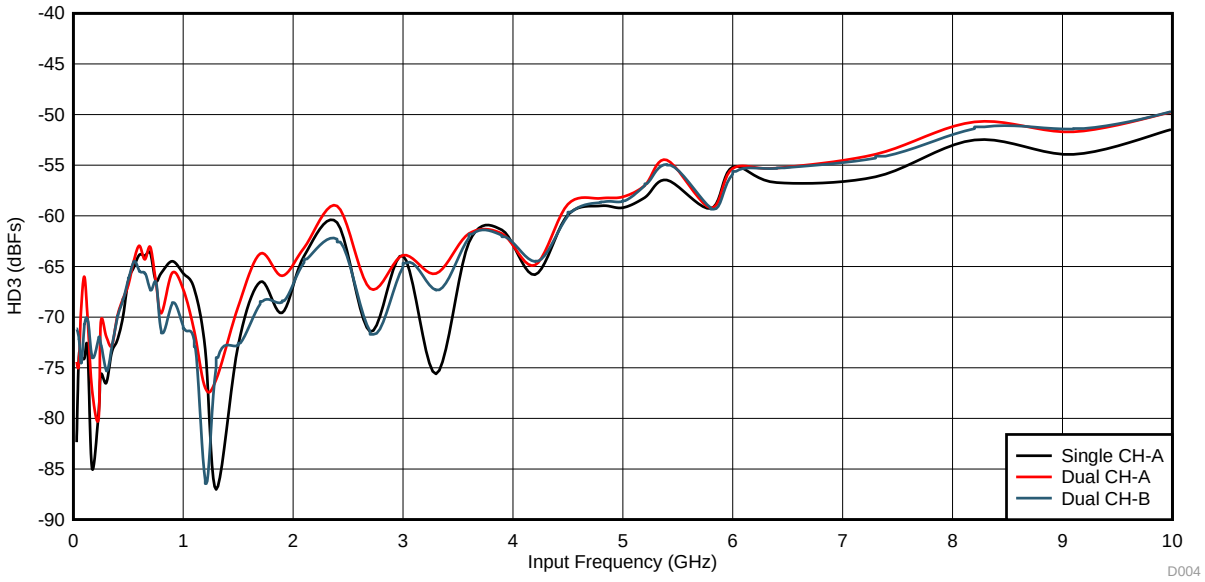

图 10. HD3 Performance for Single-Channel Interleaved Mode and Dual-Channel Mode

图 11 and 图 12 show the SFDR and SINAD performance for both single-channel interleaved mode and dual-channel mode.

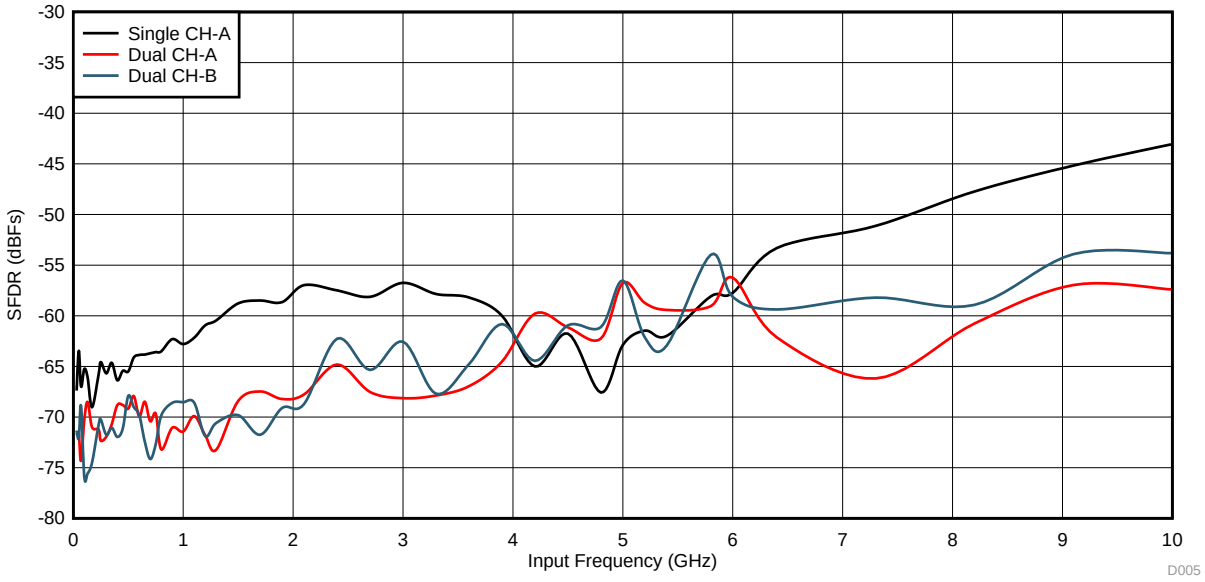

图 11. SFDR Performance for Single-Channel Interleaved Mode and Dual-Channel Mode

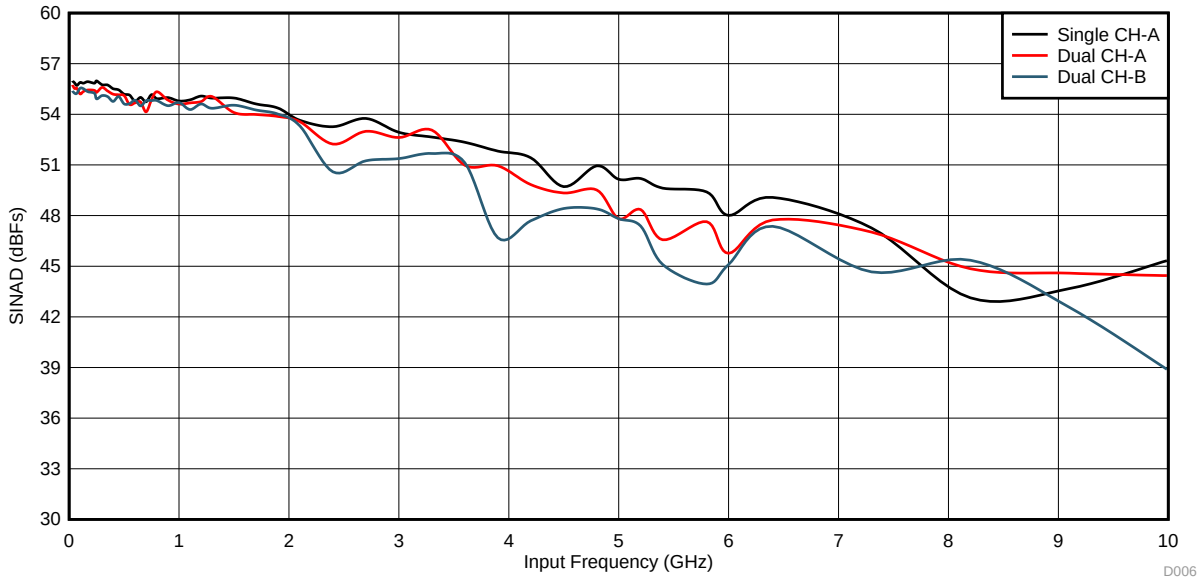

图 12. SINAD Performance for Single-Channel Interleaved Mode and Dual-channel Code

图 13 and 图 14 show the S11 and frequency response performance for both single-channel interleaved mode and dual-channel mode.

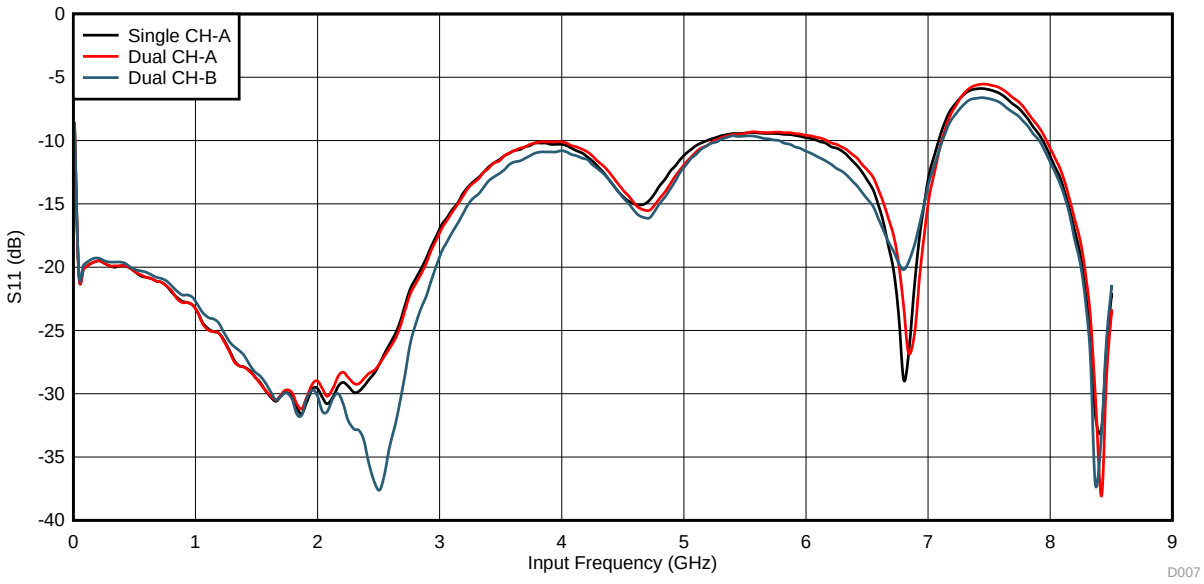

图 13. S11 Performance for Single-Channel Interleaved Mode and Dual-Channel Mode

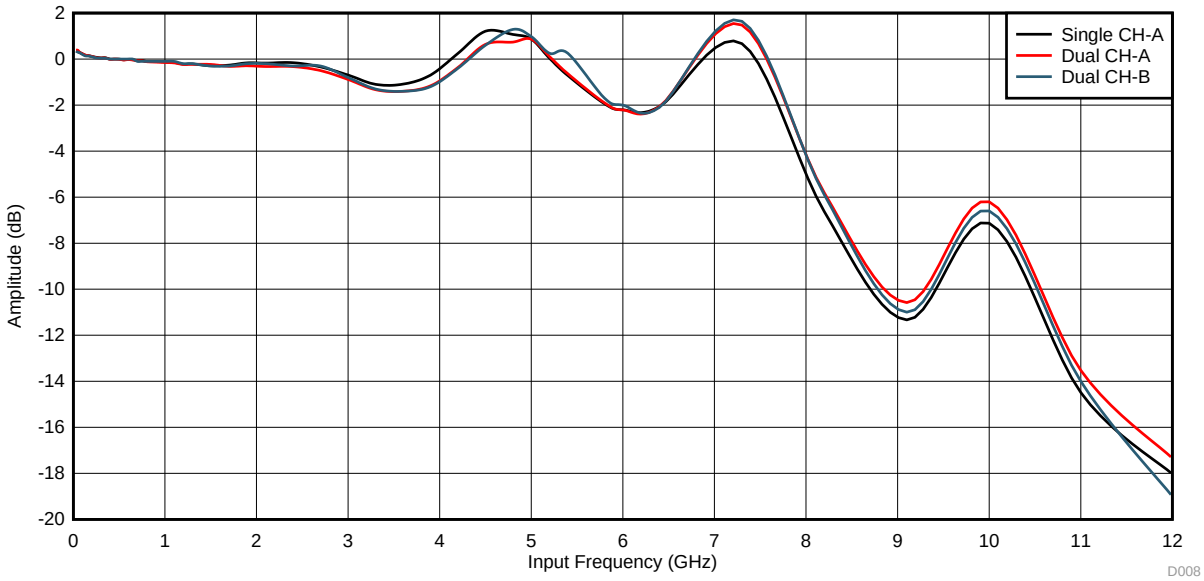

图 14. Frequency Response for Single-Channel Interleaved Mode and Dual-Channel Mode

图 15 shows the channel-to-channel isolation performance for dual-channel mode.

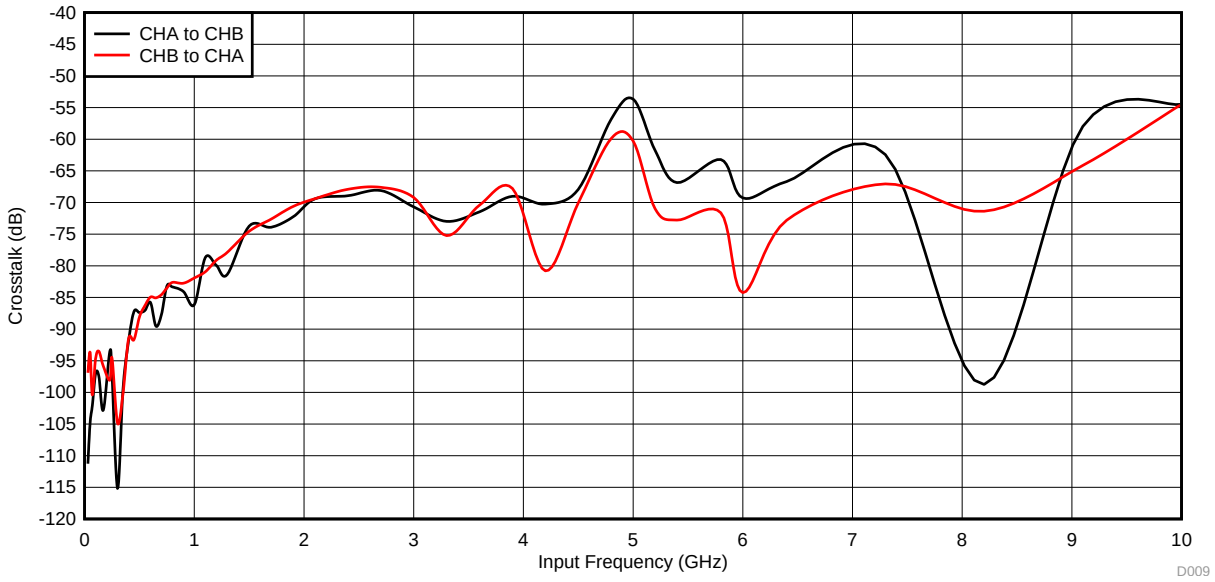

图 15. Crosstalk Performance in Dual-Channel Mode for Channel A and Channel B

The board was modified by replacing both the input baluns with BALH-0009SMG. This balun has a better performance at higher frequencies.

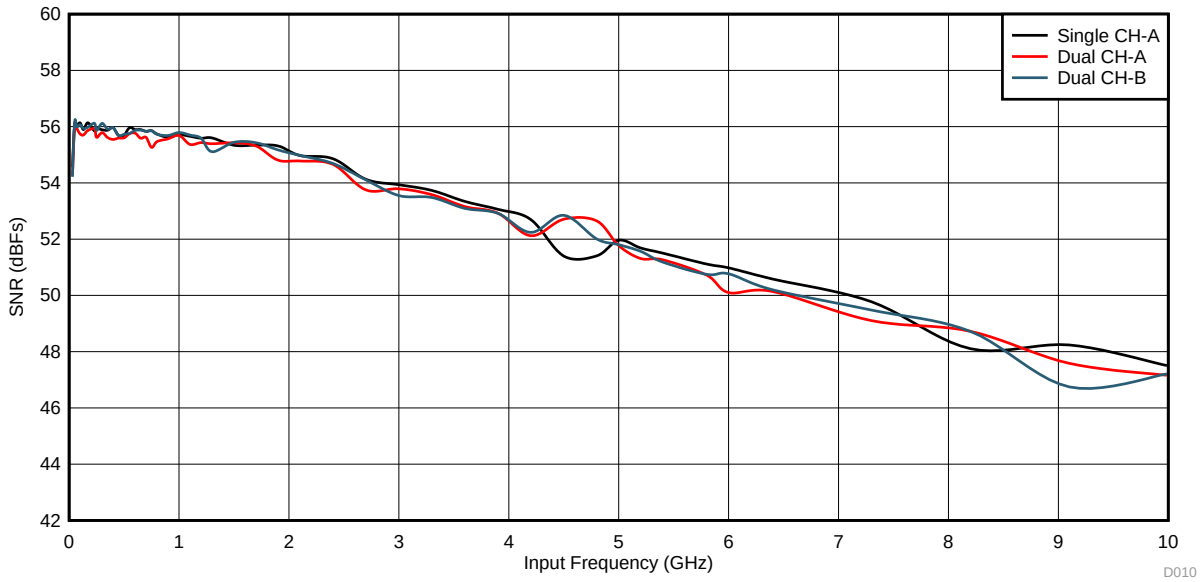

图 16. SNR for Interleaved Single-Channel and Dual-Channel Mode

图 17 shows the THD for both single-channel interleaved mode and dual-channel mode.

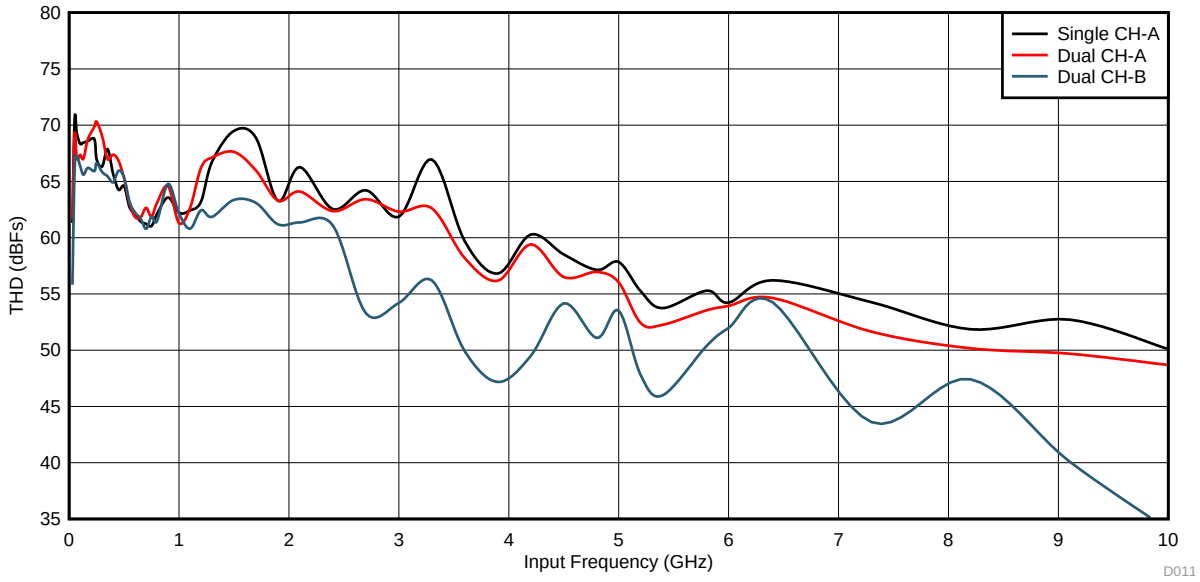

图 17. THD Performance for Single-Channel Interleaved Mode and Dual-Channel Mode

图 18 and 图 19 show the HD2 and HD3 performance for both single-channel interleaved mode and dual-channel mode.

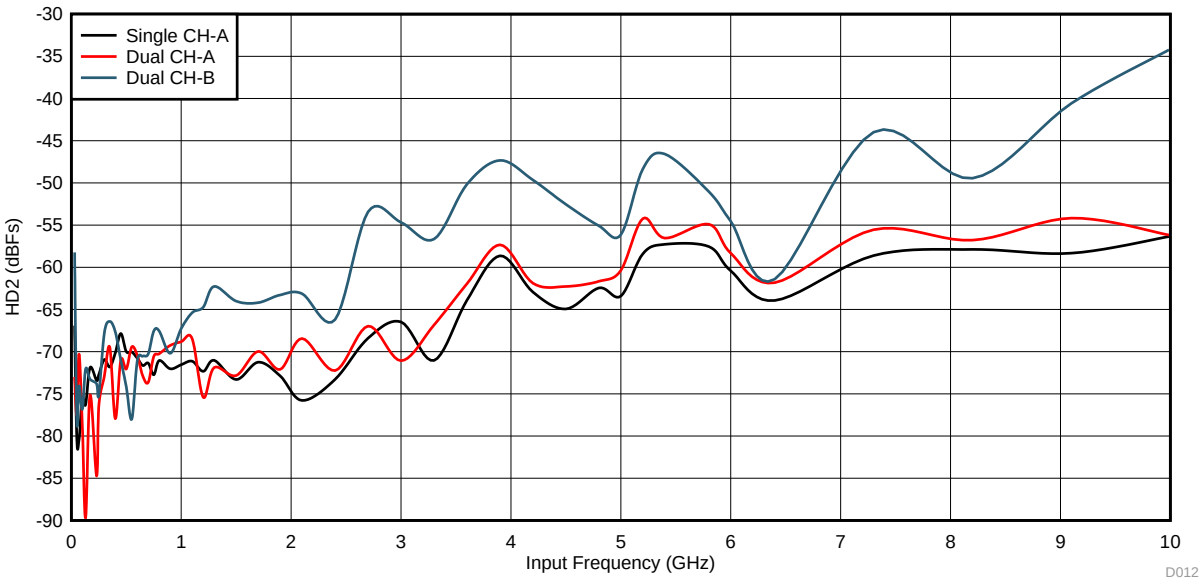

图 18. HD2 Performance for Single-Channel Interleaved Mode and Dual-Channel Mode

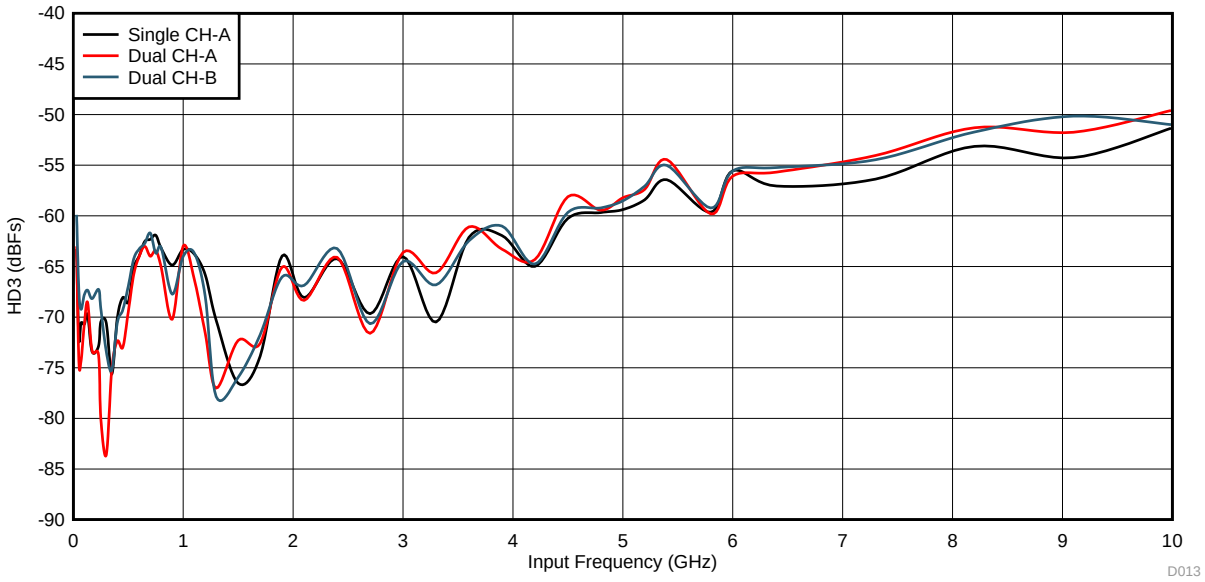

图 19. HD3 Performance for Single-Channel Interleaved Mode and Dual-Channel Mode

图 20 and 图 21 show the SFDR and SINAD performance for both single-channel interleaved mode and dual-channel mode.

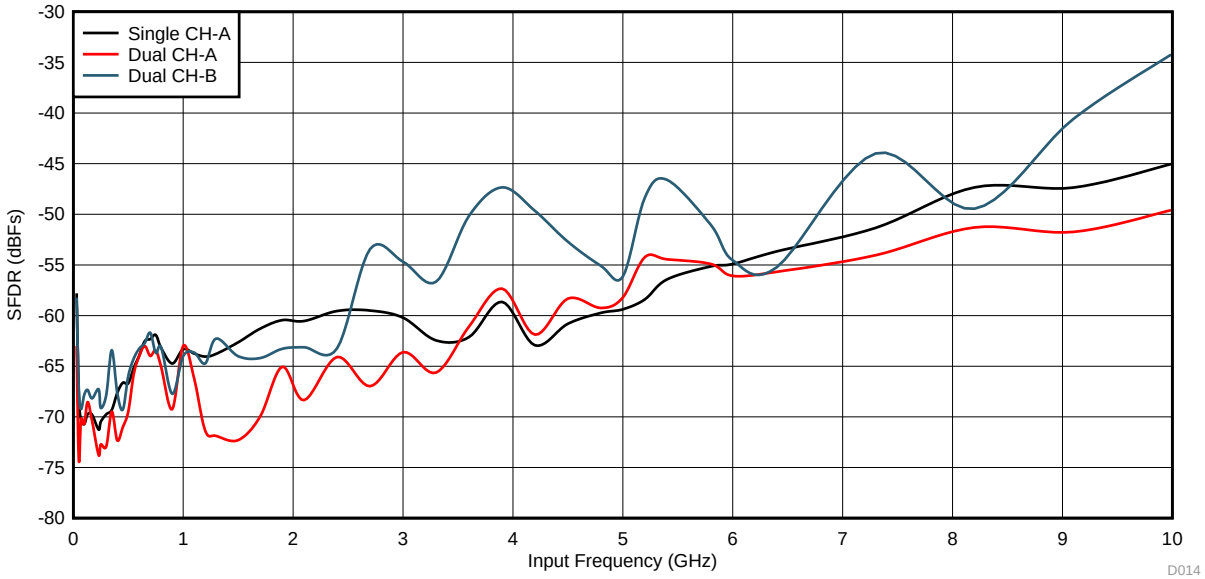

图 20. SFDR Performance for Single-Channel Interleaved Mode and Dual-Channel Mode

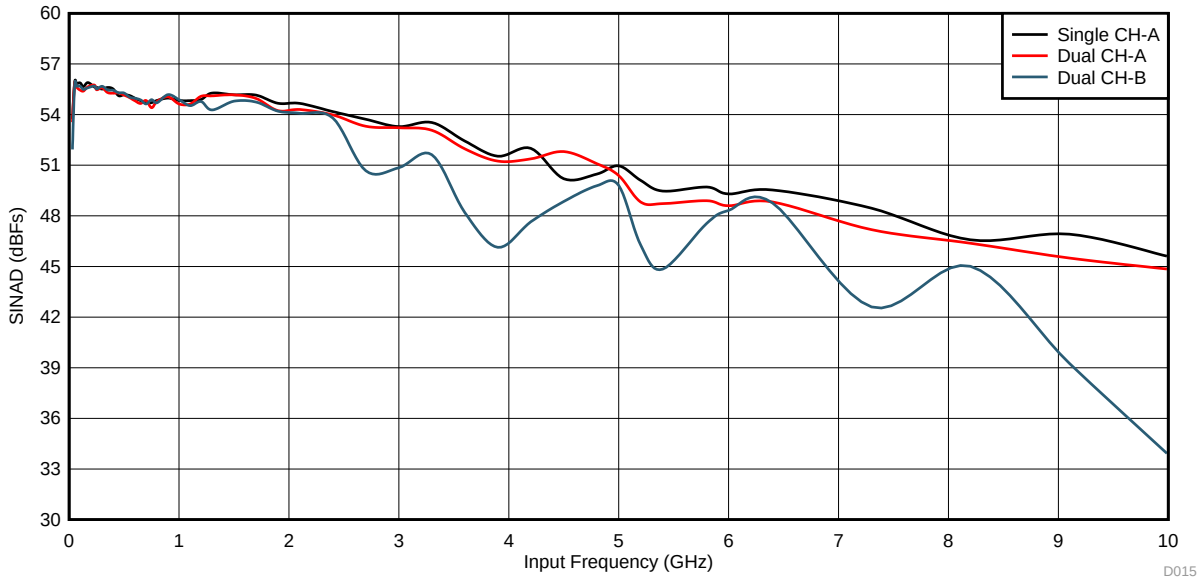

图 21. SINAD Performance for Single-Channel Interleaved Mode and Dual-Channel Mode

图 22 and 图 23 show the S11 and frequency response performance for both single-channel interleaved mode and dual-channel mode.

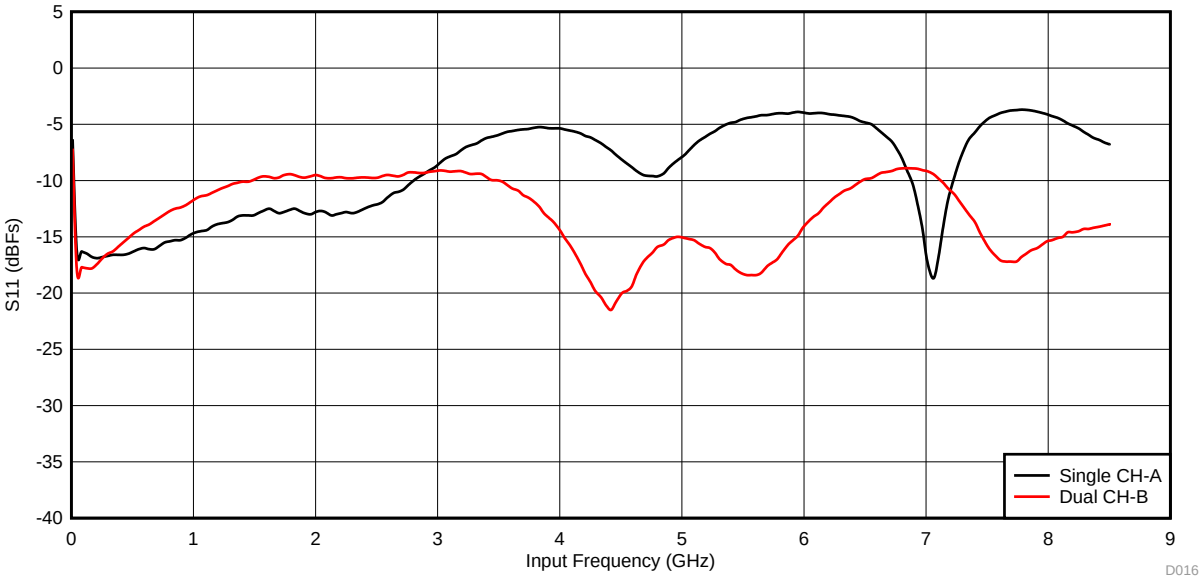

图 22. S11 Performance for Single-Channel Interleaved Mode and Dual-Channel Mode

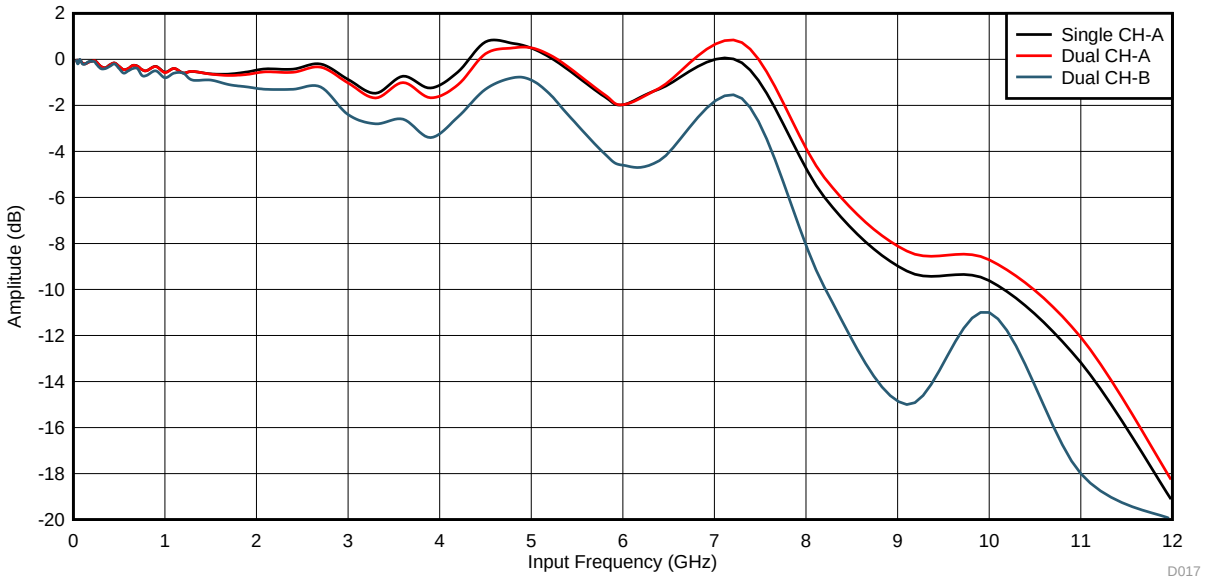

图 **23. Frequency Response for Single-Channel Interleaved Mode and Dual-Channel Mode**

图 24 shows the channel-to-channel isolation performance for dual-channel mode.

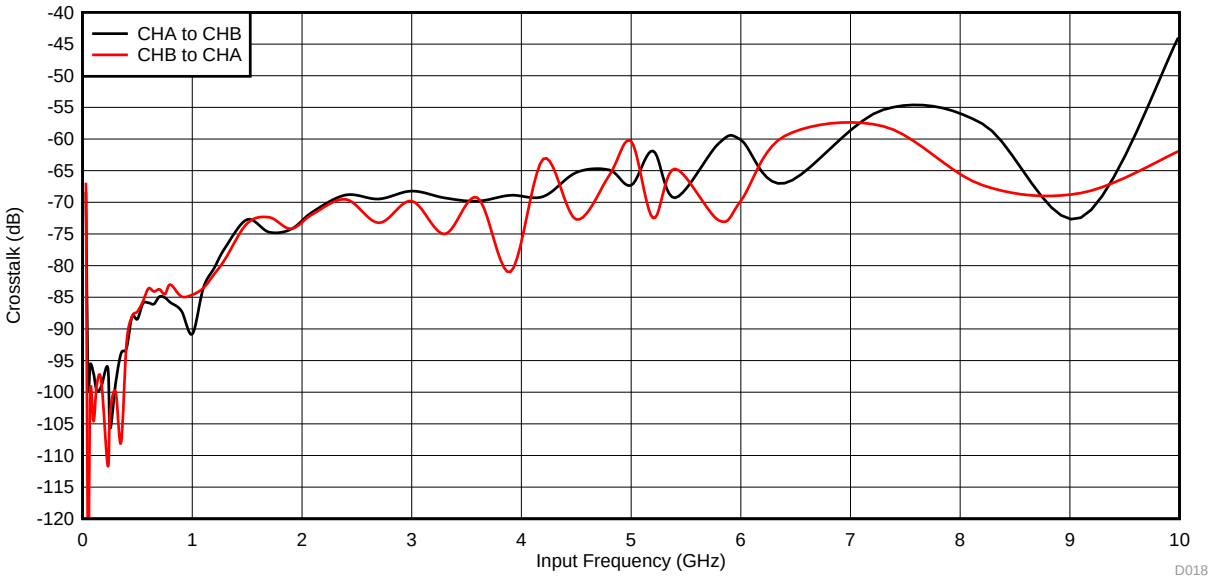

图 **24. Crosstalk Performance in Dual-Channel Mode for Channel A and Channel B**

6 Design Files

6.1 Schematics

To download the schematics, see the design files at TIDA-01442.

6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01442.

6.3 PCB Layout Recommendations

6.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01442.

6.4 PCB Project

To download the Altium project files, see the design files at TIDA-01442.

6.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01442.

6.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01442.

7 Software Files

To download the software files, see the design files at TIDA-01442.

8 商标

9 About the Author

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