# *TI Designs：TIDA-01003*

# *采用 YUV422、FPD-Link III 和 4V 至 36V 同轴电缆供电技术的汽车 100 万像素摄像头模块参考设计*

## 说明

此参考设计是一款宽输入电压摄像头模块，它使用 100 万像素 ON Semiconductor®AS0140AT CMOS 成像仪通过 FPD-Link III 提供多种未压缩的视频格式。支持的视频格式为 8 位和 10 位 YUV422。凭借 TI 的 FPD-Link III SerDes 技术，可以通过一条同轴电缆同时传输视频数据双向控制信号和电力。该设计的输入电压范围为 4V 至 36V，具有“电池短路”保护，可用于高级驾驶员辅助和信息娱乐系统（如环视系统、后视摄像头、驾驶员监控、智能后视镜），并且可以用作模拟或以太网摄像头的替代产品。

## 资源

| | |
|---|---|
| TIDA-01003 | 设计文件夹 |
| DS90UB913A-Q1 | 产品文件夹 |
| LM53600-Q1 | 产品文件夹 |
| TPS62261-Q1 | 产品文件夹 |
| LP5907-Q1 | 产品文件夹 |
| TIDA-01002 | 工具文件夹 |

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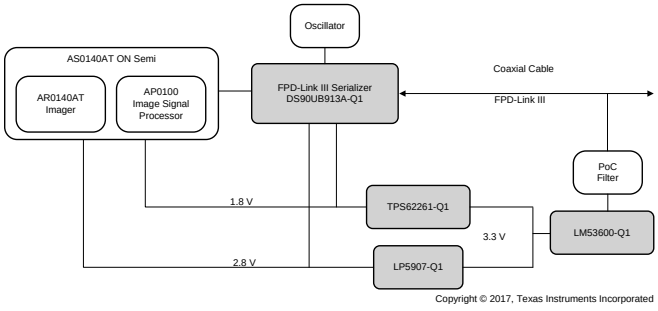
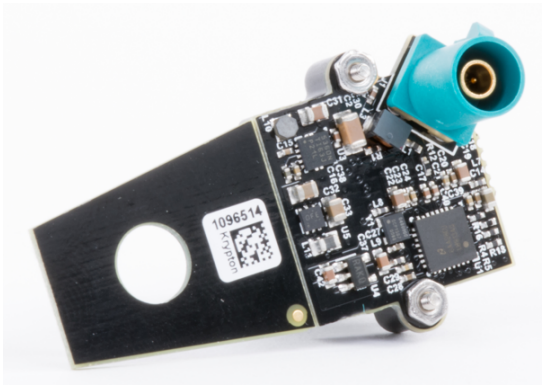
## 特性

- 设计经过空间优化，可安装在 20 x 20mm 的单块 PCB 上
- 电源使用宽输入电压开关转换器，可承受电池短路情况
- 模块输出 YUV422 720p 高达 30fps
- 配备适用于数字视频、电源、控制和诊断的单个 Rosenberger Fakra 同轴电缆连接器
- 包含设计注意事项和 BOM 分析

## 应用

- 环视系统
- ADAS 视觉系统
- 后视摄像头
- 智能后视镜



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# 1 System Description

Many automotive safety systems require small camera modules that provide low-latency, uncompressed video. This TI Design addresses this need by combining a 1-megapixel (MP) imager with an integrated image signal processor (ISP), a 1.4 Gbit/s serializer, and a necessary power supply for the two parts to provide uncompressed, displayable 720p resolution at up to 30fps video data. All of this functionality is contained on a 20-mm×20-mm circuit card. The system power supply and power over coax (PoC) filter have a wide input voltage range and can withstand a short to battery condition. The only connection required by the system is a single 50-Ω coaxial cable.

This camera module is intended to be used as either a rear view camera, a camera in a surround view system, or as a replacement for an analog camera module. The output is an uncompressed, readily displayed video feed, which lowers the processing load for the processor because the video feed does not require any further processing. Analog and Ethernet cameras cannot provide uncompressed, low-latency, displayable video without extra processing.

The video output of the ISP is connected to the serializer through a parallel video interface. This video data is then converted to a high-speed serial stream that is transmitted over a single LVDS pair to the deserializer located on the other end of the coax cable. The high-speed signal is connected to the serializer through an AC coupling capacitor to block out any DC. This is the path that the video data and control backchannel will take between the serializer and deserializer. The backchannel is a low-latency, bidirectional control channel that transmits control information from an $I^2C$ port. This control channel is independent of video blanking period and is used by the system microprocessor to configure and control the serializer and ISP. Power comes from across the channel through the PoC filter, which serves to protect the datalink and provide clean power.

## *1.1 Key System Specifications*

表 **1. Key System Specifications**

| PARAMETER | SPECIFICATIONS | DETAILS |
|---|---|---|
| Input voltage | 4 to 36 V, 9 V nominal | 节 2.4.2.1 |
| Total power consumption | < 0.8 W, 9 V nominal | 节 3.2.4.1.3 |
| Switching frequencies | > 1.8 MHz | 节 3.2.4.1.2 |
| Pixel clock frequency | 72 MHz | 节 3.2.4.2 |

# 2 System Overview

## 2.1 Block Diagram

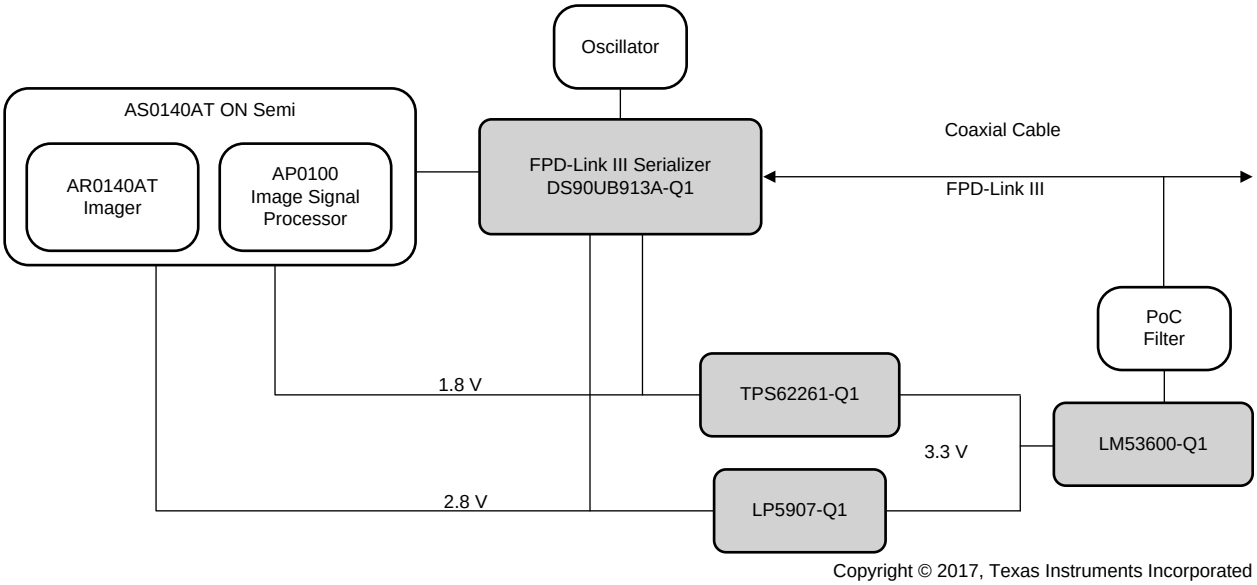



图 **1. TIDA-01003 Block Diagram**

## 2.2 Highlighted Products

### 2.2.1 DS90UB913A-Q1

The DS90UB913A-Q1 is the serializer portion of a chipset that offers an FPD-Link III interface with a high-speed forward channel and a bidirectional control channel for data transmission over a single coaxial cable or differential pair. This chipset incorporates differential signaling on both the high-speed forward channel and bidirectional control channel data paths. The serializer-deserializer pair is targeted for connections between imagers and video processors in an electronic control unit (ECU), respectively.

### 2.2.2 LM53600-Q1

The LM53600-Q1 is a 650-mA wide input voltage, synchronous 2.1-MHz step-down converter. The device provides the 3.3-V-rail for the system. This 3.3-V-rail feeds the two system rails and provides the sequencing signal to meet the power sequence requirements.

### 2.2.3 TPS62261-Q1

The TPS622261-Q1 is a 600-mA, 1.8-V fixed-output buck converter, which has fixed switching frequency operation at 2.25 MHz.

### 2.2.4 LP5907-Q1

The LP5907-Q1 is a 250-mA, fixed-output, ultra-low noise and low-$I_Q$ low-dropout regulator used as the 2.8-V supply. This device provides high PSRR, excellent transient response, and very low output noise voltage without the need for a noise bypass capacitor. If necessary, this regulator can also support remote output capacitor placement.

### 2.2.5 AS0140AT Imager + ISP

Available from ON Semiconductor, this device has both the AR0140AT imager and AP0100AT image signal processor, conveniently available in one single package. It contains a ¼-inch 1-MP, CMOS imager with high dynamic range (HDR) and 8- or 10-bit YUV422, and 10 to 12-bit tone-mapped Bayer output data formats. There is also a fully programmable spatial transform engine (STE) that can perform spatial transforms and eliminate the need for an expensive DSP for lens distortion correction. This sensor-processor combo package is suitable for automotive viewing systems. Some additional features of the imager are:

- Supports image sizes: 1280 × 800 and 720p
- 45 fps at 1 MP, 60 fps at 720p
- 50- or 60-Hz auto flicker detection and avoidance
- Superior low-light performance
- Configured using $I^2C$

## *2.3 Design Considerations*

This section highlights selected device features and briefly discusses how they are used to meet the system requirements of this TI Design. To quickly reiterate, this system must have a small and efficient power solution that does not interfere with the AM band and provide high-quality video while withstanding a short-to-battery condition.

### 2.3.1 Serializer

Using a serializer to combine video data with a bidirectional control signal onto one coax or twisted pair greatly simplifies system complexity and minimizes solution size, cost, and cabling requirements. The parallel video input of the DS90UB913A-Q1 mates with the parallel output of the AS0140AT. When combined with the PoC filter, the formatted video stream, $I^2C$ control, diagnostics, and power can all be transmitted up to 15 meters on a single inexpensive coax cable. For more information on the cable itself, see the cable requirements application note [2].

### 2.3.2 Wide Input Voltage DC-DC Step-Down Converter With Fixed 3.3-V Output

In rear camera or satellite camera systems, form factor is a major driver of design constraints. Because camera sensor circuits usually are sensitive to noise at frequencies below 1 MHz, and AM interference must be avoided for all automotive applications, keeping switching frequencies above 1.8 MHz is necessary. These modules also need to be power efficient without adding measurable noise to the video coming from the imager. For this system, the supply must also withstand the wide input voltage range of a direct battery connection. The ISP and serializer also have power sequencing requirements.

The LM53600-Q1 is a strong candidate due to its wide input voltage range, high efficiency, fixed switching frequency operating mode, and reset signal. The /RESET output of the device behaves like a delayed Power Good (PG) signal. This can be used to meet power-up sequence requirements. In this system, the LM53600-Q1 steps the incoming PoC voltage down to 3.3 V to supply power to the other two supplies in the system.

### 2.3.3 Output DC-DC Step-Down Converter With Fixed 1.8-V Output

This device is a 1.8-V fixed-output DC-DC step-down converter. Because it is fixed output, there is no resistor feedback network. In this TI Design, the external component count is reduced to three, and the total solution size is impressively small, which is desirable with such tight board size requirements. This device can also operate with a fixed switching frequency. This switching frequency is 2.25 MHz, which minimizes the possibility of interference in the AM band. With an input voltage of 3.3 V, an output of 1.8 V, and relatively high loading on the 1.8-V rail, this device will operate at a high efficiency.

### 2.3.4 Low-Dropout Regulator With Fixed 2.8-V Output

Because there is a 3.3-V system voltage and a sensitive and dynamic 2.8-V rail with light loading, a low-dropout regulator would be an efficient way to provide 2.8 V from the 3.3-V rail. The 2.8-V rail max current draw is 130 mA, but typical is 70 mA. The LP5907-Q1 is a perfect match here because it is rated for 250 mA, has a fixed 2.8-V output, very low-noise output voltage that does not disturb video quality, high PSRR to reject upstream switching noise, and transient response to respond to the dynamic loading on the 2.8-V rail. The fixed-output option reduces our total solution size as well, especially compared with a switching converter or adjustable output LDO. Therefore, this device meets all requirements.

## 2.4 System Design Theory

This section discusses the considerations behind the design of each subsection of the system. This section also provides necessary calculations for external components for each device and device modes to meet the system requirements of this TI Design.

### 2.4.1 PCB Form Factor

This TI Design is not intended to fit any particular form factor. The only goal of the TIDA-01003 with regards to the PCB was to make as compact a solution as possible. The square portion of the board is 20 mm × 20 mm. The area near the board is used for attaching the optics housing that holds the lens with screws. 图 2 shows the front of the board:

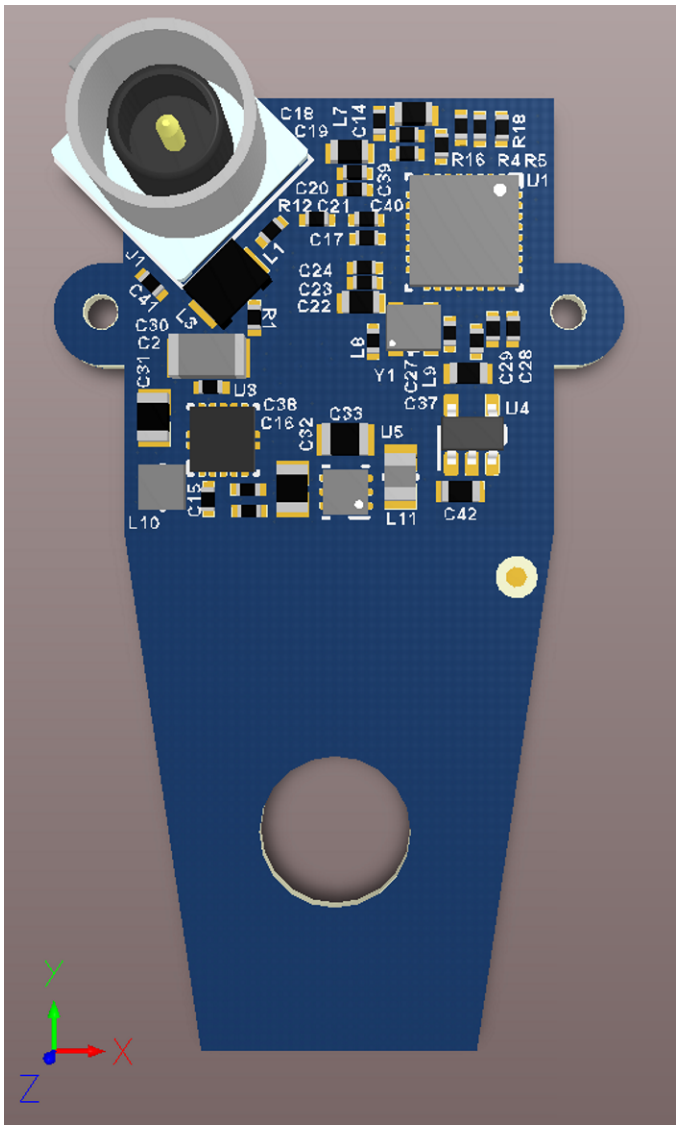



图 2. Front of Board

The mounting tab on the bottom of the board allows for easy mounting to tripods through the ¼-inch screw hole. This tab has no circuitry and is only intended to be used for mounting. It can be removed if desired. In 图 3, the mounting of the board to a tripod is shown:

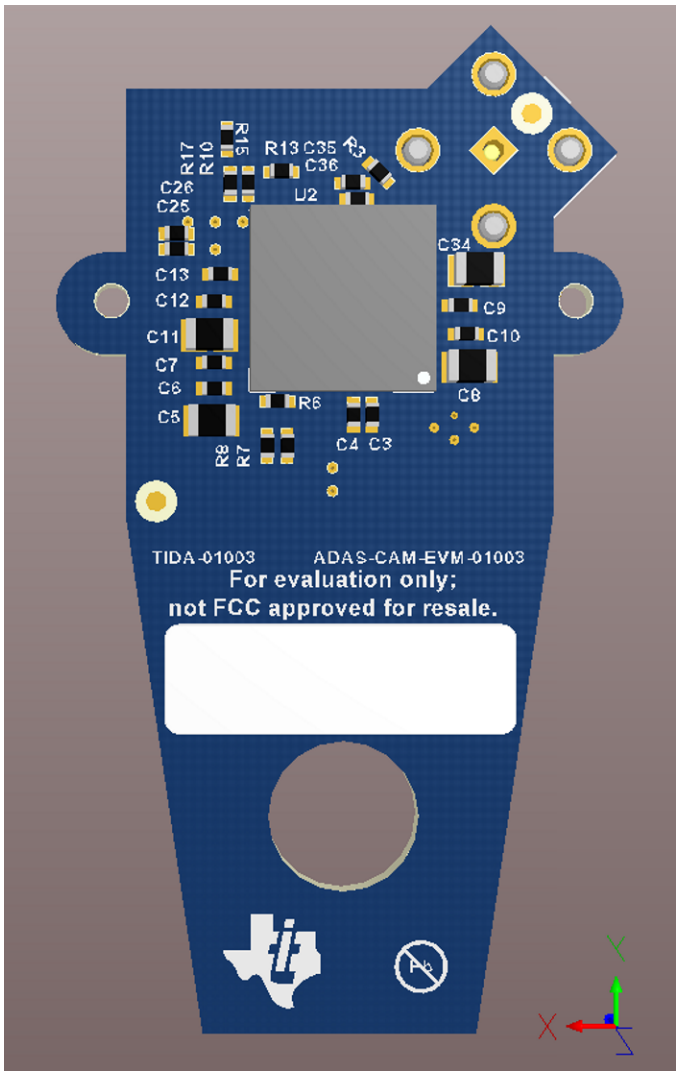



**图 3. Back of Board**

### 2.4.2 Power Supply Design

Because this TI Design is targeted at automotive applications, there are few considerations that constrict design choices. In addition, there are system-level specifications that shaped the TIDA-01003 design:

- The total solution size needs to be minimized to meet the size requirement, which is less than 20 mm × 20 mm
- The input voltage range is 4 to 36 V, 9 V nominal
- The total power dissipation of the system should not be more than 1 W
- The switching frequencies of the DC-DC converters in our system must be above 1.8 MHz
- The 2.8-V rail must come up before the 1.8-V rail
- All devices need to be AEC-Q100 (-Q1) rated

Ultimately, this TI Design uses the LM53600-Q1, TPS62261-Q1, and LP5907-Q1 in a cascaded-parallel topology where the LM53600-Q1 provides the system voltage of 3.3 V. The following sections examine how and why these parts were selected. See 图 4 for the power supply schematic:

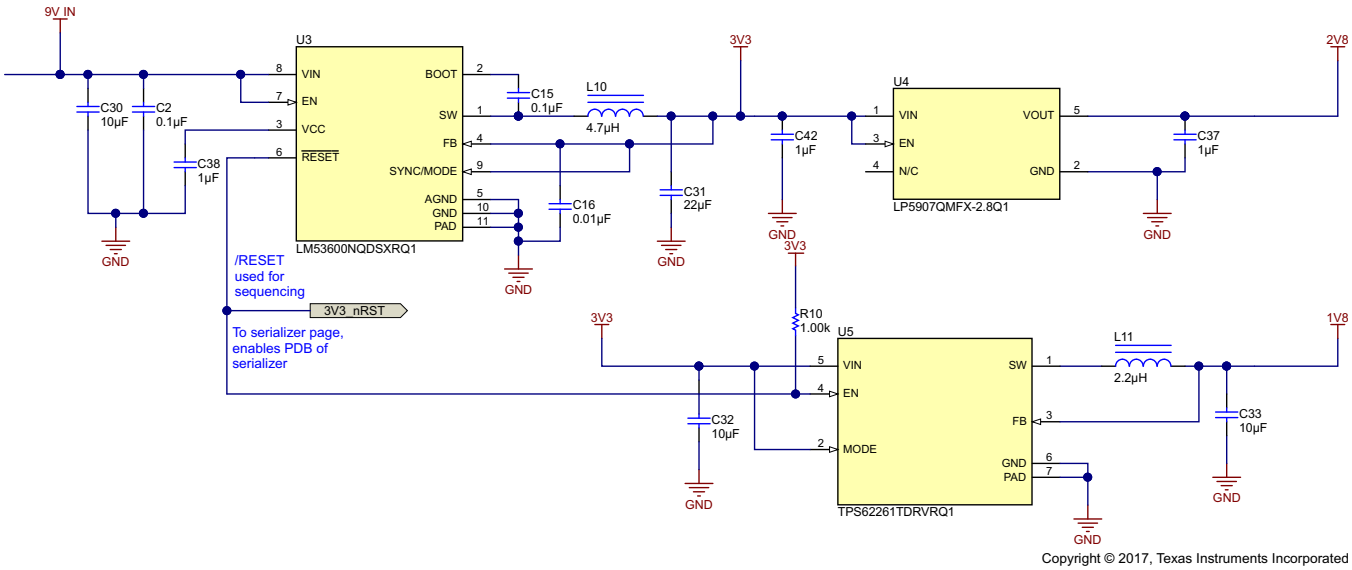



**图 4. Power Supply Schematic**

The small solution size and wide input voltage range requirements are in opposition to one another. Combining all of these requirements together can make for a very difficult layout as ICs and components become larger to satisfy the wide input voltage requirement, and prioritizing one over the other must be done on a case-by-case basis.

The capacitors that will see the high-input voltage selected should have an X7R temperature coefficient and be rated for at least twice the voltage they will see. However, the TIDA-01003 design has input capacitors that are rated for 50 V despite that it is not double the maximum voltage to minimize the package size.

表 2 describes the power budget of the TIDA-01003 design, which were taken from the device data sheets:

**表 2. Power Budget**

| DS90UB913A-Q1 | VOLTAGE (V) | CURRENT (TYP) (A) | CURRENT (MAX) (A) | POWER (TYP) (W) | POWER (MAX) (W) |
|---|---|---|---|---|---|
| VDDT | 1.8 | 0.0610 | 0.0800 | 0.10980 | 0.14400 |
| VDDIO | 2.8 | 0.0050 | 0.0080 | 0.00270 | 0.00540 |
| **ON AS0140AT** | | | | | |
| VDD_1V8 | 1.8 | 0.2313 | 0.4600 | 0.41634 | 0.82800 |
| VDDA_DAC | 2.8 | 0.0001 | 0.0003 | 0.00028 | 0.00084 |
| VDDIO_2V8 | 2.8 | 0.0329 | 0.0600 | 0.09212 | 0.16800 |
| VAA_2V8 | 2.8 | 0.0405 | 0.0700 | 0.11340 | 0.19600 |
| **RAIL TOTAL** | | | | | |
| | 1.8 | 0.2923 | 0.5480 | 0.52884 | 0.98640 |
| | 2.8 | 0.0785 | 0.1383 | 0.20850 | 0.38724 |
| **TOTAL POWER** | | | | | |
| | | | | 0.73734 | 1.37364 |

Summing these values, the 1.8-V rail requires around 290 mA and the 2.8-V rail requires about 78 mA. These estimates do not take into account the power dissipation of passives, but are a good ballpark number for a typical operating current. The system will either be off, in standby, or streaming video.

As previously mentioned, the parts in the power supply need to be -Q100 rated, switch outside the AM band, and satisfy the wide input voltage range and current requirements listed in 表 2. Because the input voltage is known to be a regulated voltage that will always be greater than any of the power rail needs, only step-down converters and LDOs are considered. However, keep in mind that in some situations a designer may sacrifice efficiency in order to avoid the inherent noise and EMI issues associated with switching power supplies.

Many buck regulators integrate everything into very small packages except the input capacitors, output capacitors, and the inductor. With high integration, efficiency is lost across different operating points. However, for this TI Design efficiency can be sacrificed for size and simplicity. The device families from which to choose all have high integration of external circuitry and high efficiency.

First look at the wide input voltage DC-DC converter and 3.3-V system supply, the LM53600-Q1. The key features and operating points of the LM53600-Q1 that directly affect whether the system requirements are met are the wide input voltage range, switching frequency, power sequencing, and total solution size.

The switching frequency of the LM53600-Q1 is specified to be above 1.85 MHz as long as there is a roughly 2-V differential between the input and output voltage. Application curves from the data sheet show that the switching frequency will be around 2.1 MHz for the operating conditions of this TI Design. It also has a factory enabled spread spectrum option. This feature is used in the TIDA-01003 design as well to mitigate EMI as much as possible. Spread spectrum eliminates the peak emissions at specific frequencies by spreading emissions across a wider range of frequencies than a device with fixed frequency operation. Typically, low-frequency conducted emissions from the first few harmonics can be easily filtered. However, reducing emissions at higher harmonics that fall in the FM band can be more difficult. With spread spectrum, peak emissions at the device's switching frequency are only reduced by 1 dB, but peaks in the FM band are reduced by more than 6 dB with the spread of energy across the FM band.

As mentioned earlier, the open drain /RESET pin of the LM53600-Q1 can be used for sequencing. This can sometimes replace supervisory ICs because it offers similar functionality. The /RESET pin is pulled low internally until 6 ms after the output voltage is reached. In this TI Design, it is used to delay the turnon of the 1.8-V supply and serializer. The total solution of the LM53600-Q1 requires seven external components, including the inductor.

The 1.8-V supply chosen was the TPS62261-Q1 buck converter. Ths TPS62261-Q1 is very efficient at our operating conditions and has a very small solution size. It is also automotive grade, has a fixed switching frequency above the AM band, and a fixed-output option.

The low-noise and fast-transient LP5907-Q1 LDO was selected for the 2.8-V supply. This was chosen because the 2.8-V rail powers both the dynamic load of the ISP and the sensitive analog rails for the imager. Ideally, this rail should be as quiet as possible for best video quality. Because there is a 3.3-V rail present, one can efficiently use an LDO to provide the 2.8 V.

The next section discusses the details and calculations behind the design with these devices.

#### 2.4.2.1 LM53600-Q1

Find more details on component selection and design theory, see *0.65A/1A, 36V Synchronous, 2.1MHz, Automotive Step Down DC-DC Converter*.

Because the device is internally compensated, it is stable within a range of values for L and C. It is recommended the inductance be between 4 and 10 µH. For most applications, 4.7 µH should be used with fixed 5-V and 3.3-V versions.

This inductor must be sized to not be in saturation and have as small as a footprint as possible. With the device efficiencies and the rail current values outlined in the power budget, the output current is calculated to be about 265 mA. This means the ripple current for the 9-V input, 4.7-µH inductor, and 2.1-MHz switching frequency is 201 mA, using 公式 1:

$$\Delta I_L = V_{OUT} + \frac{1 - \frac{V_{OUT}}{V_{IN}}}{2} \quad (1)$$

With the ripple current, the maximum current through the inductor is calculated using 公式 2:

$$I_{Lmax} = I_{OUTmax} + \frac{\Delta I_L}{2} \quad (2)$$

As shown in 公式 2, the maximum current is calculated to be 460 mA. This TI Design ultimately uses the NRV2010T4R7MGF from Taiyo-Yuden, as this inductor saturates at 760 mA, providing reasonable headroom. The package size is 2 × 2 mm, which is quite small given the current and saturation specs. This inductor has an AEC-Q200 rating.

Selecting the output capacitance is a bit simpler than the inductor. As recommended in the data sheet, a 22-µF capacitor ensures stability and handle the transients of switching between standby to streaming data and dynamic loading of the ISP.

The LM53600-Q1 switcher has a forced PWM (FPWM) mode of operation, which keeps the switching frequency around 2.1 MHz as long as the difference between input and output voltage is more than 2 V and there is no large negative current in the inductor. In this case, the loading will be roughly 300 mA continuously while the ISP streams data. To set the device in FPWM mode, the SYNC/MODE pin of the device must be pulled up to at least 1.5 V and not exceed 42 V.

The spread spectrum option is a factory enabled option. To minimize interference in the AM band, spread spectrum mode should be enabled while operating in FPWM mode. Fortunately, in this case, spread spectrum is active even without load in FPWM mode (for example, when the ISP is not streaming data). The only way spread spectrum would be disabled is if the input voltage is too low and the device is in dropout.

The /RESET pin of this device will be used to achieve proper sequencing of the serializer and ISP. As discussed in previous sections, the /RESET pin of the device has similar functionality to a typical PG signal. The difference here is that the /RESET signal goes high 6 ms after the device output voltage level is reached. The /RESET signal is not controlled until the input voltage reaches 1.5 V. Once this 1.5-V input voltage threshold is reached, the /RESET signal is grounded until the correct output voltage level is reached. In this TI Design, the /RESET signal is connected to both the 1.8-V Enable and the PDB pin of the serializer. The delayed /RESET output ensures the critical devices wake up only after all rails have stabilized and internal ADCs have settled.

#### 2.4.2.2 TPS62261-Q1

Find more details on component selection and design theory, see *2.25-MHz 600-mA STEP-DOWN CONVERTERS*.

Similar to the inductor calculations for the LM53600-Q1 switcher, the ripple current and maximum inductor current are calculated before selecting the inductor. Using the same steps used in 节 2.4.2.1, the ripple current is found to be around 165 mA, and the maximum is found to be 373 mA. Because the smallest inductor is preferred, the 2.2-µH MLZ2012M2R2HTD25 from TDK is selected. It comes in an extremely small 2-mm×1.5-mm package. It is also important to note that this device is optimized for operation with a 2.2-µH inductor and 10-µF output capacitor.

#### 2.4.2.3 LP5907-Q1

For the LDO, 1-µF capacitors are used for both the input and output capacitors.

### 2.4.3 FPD-Link III Interface

The FPD-Link III interface allows for proper power and high-throughput data transmission, and is made up of a PoC filter and the DS90UB913A-Q1. This section discusses the PoC filter, followed by a discussion of key parameters when designing with the serializer.

### 2.4.3.1 Power Over Coax (PoC) Filter

One of the most critical portions of a design with PoC is the filter circuitry. The goal of the PoC filter is twofold:

1. Deliver a clean DC supply to the input of the switching regulators.
2. Protect the FPD-Link communication channels from noise coupled backwards from the rest of the system.

The DS90UB913A/DS90UB914 SerDes devices used in this system communicate over two carrier frequencies: 700 MHz at full speed ("forward channel") and 2.5 MHz ("backchannel") determined by the deserializer device. The filter should attenuate this rather large band spanning both carriers, only passing DC. This DC portion is connected to the input of the LM53600-Q1 buck converter to output 3.3 V. By filtering out the backchannel frequency, the PoC filter can also filter the switching frequencies from the upstream power supplies. In 图 5, L2 represents the full PoC filter in this reference design:

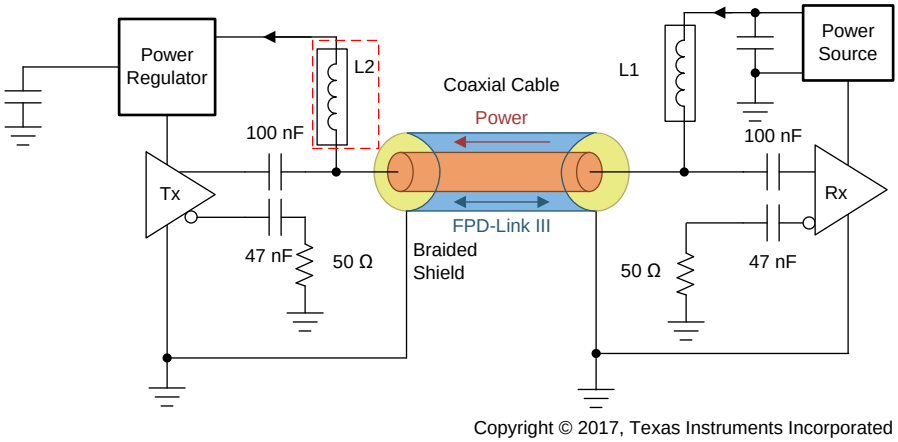





图 5. Power Over Coax

The nominal backchannel speed is 2.5 MHz but can vary from 1 MHz to 4 MHz when taking into account process variation, temperature, and power supply. To achieve the 1-kΩ impedance for the POC network across the full frequency range of 1 MHz to 700 MHz, it is recommended to use two inductors: a 4.7-µH inductor for high frequency forward channel filtering, and a 100-µH inductor for low-frequency backchannel filtering. See the PoC application note for more details[1].

图 6 shows the schematic of the PoC filter for this system:

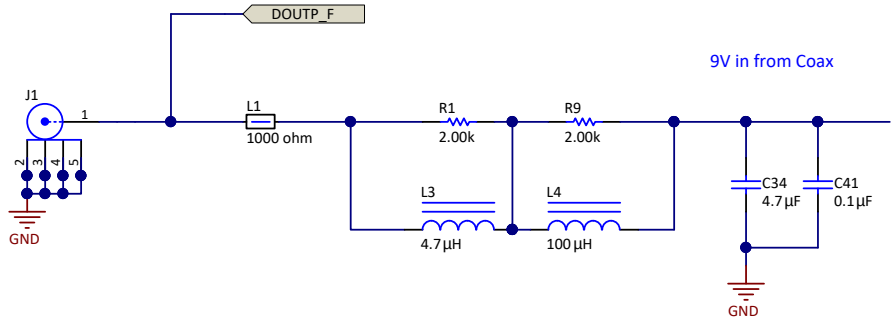



图 6. Power Over Coax Schematic

Ferrite bead L1 increases conducted immunity tested in bulk current injection (BCI) tests. The resistor parallel to the inductors prevents the impedance from spiking above 2-kΩ across the band of interest.

### 2.4.3.2 DS90UB913A-Q1

图 7 closely resembles the FPD-Link III interface of this TI Design and is shown to demonstrate important components and sub-blocks of this system.

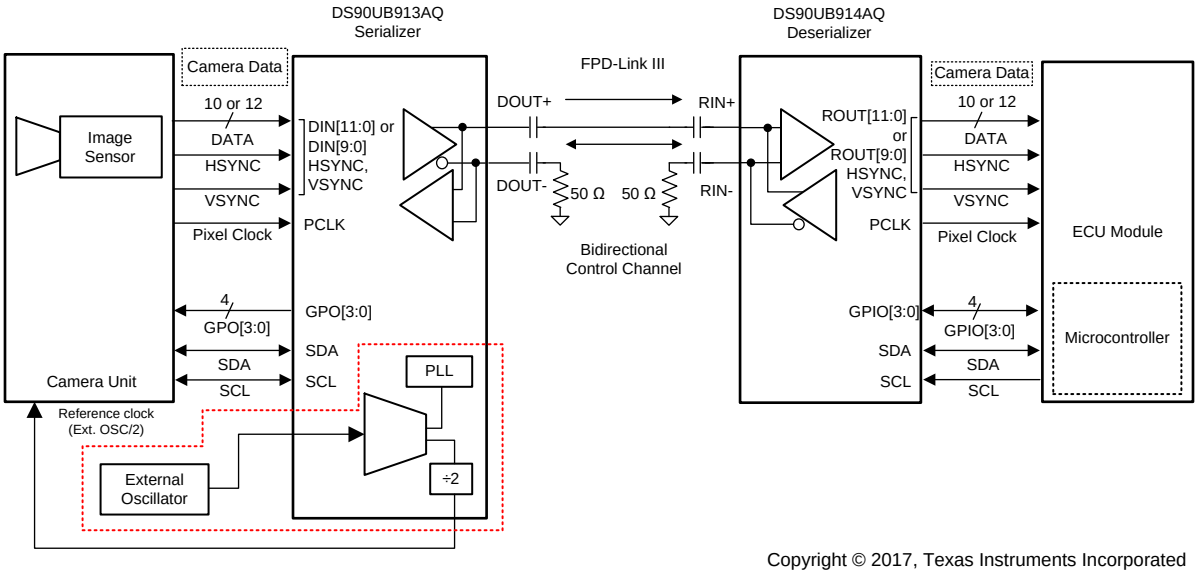





**图 7. Typical Operation in External Oscillator Mode**

Besides the passives used in this configuration circuitry, an oscillator must be selected. The TIDA-01003 uses a non-automotive grade 48-MHz oscillator for the serializer to operate in external oscillator mode and 12-bit high frequency mode to achieve 720p at 30 fps (see 节 2.4.3.2.1 for more details on why this was selected). This camera module supports outputs from the ISP in 8- and 10-bit YUV422. Note that the data output of the AS0140AT is LSB aligned. The recent camera module designs that use the AS0140AT have gone through two different iterations of bit alignments. LSB aligned was ultimately selected for compatibility across multiple test platforms that use a parallel or CSI-2 interface.

The following critical design parameters are covered in the following subsections:

- Modes of Operation
- PCLK Frequency
- Synchronizing Multiple Cameras
- GPIO Pins
- Power-up and PDB Pin
- ID[X] Pin

Find more details on component selection and design theory, see *25-MHz to 100-MHz 10/12-Bit FPD-Link III Serializer*.

#### 2.4.3.2.1 Modes of Operation

As mentioned in 节 2.4.3.2, this TI Design uses the serializer in a 12-bit high-frequency mode with an external 48-MHz oscillator as the reference clock. There is an important distinction to note between these two types of modes: the 10- or 12-bit mode relates to the number of data bits input to the serializer, and the other relates to the way the serializer-deserializer pair gets its reference clock. These modes are set in hardware, but can be overridden over $I^2C$. For the oscillator mode, this is set in hardware on the serializer side of the channel. For the bit mode, this is set in hardware on the deserializer side of the channel.

Some systems may require using the pixel clock (PCLK) as the reference clock source for the system. This can be done to achieve higher frame rates or simply for flexibility of the timing signals, such as PCLK and VSYNC. However, the PCLK from an imager can have jitter that exceeds the serializer jitter tolerance in the PCLK mode compared to when the serializer is in external oscillator mode. It is recommended to use an external clock source for the reference clock of the serializer. In this mode, the serializer has a higher jitter tolerance than when operating with pixel clock from imager as the reference clock. This TI Design follows this recommendation.

When the serializer operates in external oscillator mode, the clock signal that is fed to the ISP from the serializer will be half the external oscillator frequency. The output from the external oscillator goes into the serializer through GPO pin 3, and through a divide-by-2 circuit before being outputted at GPO pin 2. The frame rate requirement drives the resonant frequency requirement of our external oscillator to be higher within 48 to 60 MHz, because the frequency of this signal is halved and the ISP is specified to receive an incoming clock with a frequency between 6 to 30 MHz.

The following values were derived from the data sheets of both serializer and imager. Here are the requirements for the external oscillator:

- Resonant frequency of 48 to 60 MHz
- Supply voltage rated for $V_{DDIO}$, or 2.8 V
- Small footprint

The TIDA-01003 design uses a 48-MHz crystal oscillator from Pericom. It has a small footprint (2.5 mm × 2.0 mm), has a jitter of ±10 ppm over temperatures of –40°C to 105°C, and supports a supply voltage range of 1.8 to 3.3 V.

See the device data sheet for details on the required circuitry to implement the clocking scheme described in this section.

#### 2.4.3.2.2 Pixel Clock (PCLK) Frequency

Because the serializer will be operating in 12-bit high frequency mode using an external oscillator as its reference clock, PCLK and external oscillator ratio must be fixed. In 12-bit high frequency mode, the device divides the incoming pixel clock internally by 1.5. Therefore, the pixel clock frequency must be 1.5 times the external oscillator frequency. In this TI Design, the external oscillator frequency is 48 MHz. This means the PCLK frequency from the AS0140AT to the serializer must be 72 MHz.

#### 2.4.3.2.3 Synchronizing Multiple Cameras

Surround view systems require synchronizing multiple cameras. To achieve this with this serializer, this TI Design uses the general-purpose input/output (GPIO) pins to transmit the control signals for syncing multiple cameras. The system controller must provide a field sync output, such as a vertical sync or frame sync signal, and the imager must be set to accept this auxiliary sync input. 图 8 shows an example of this:

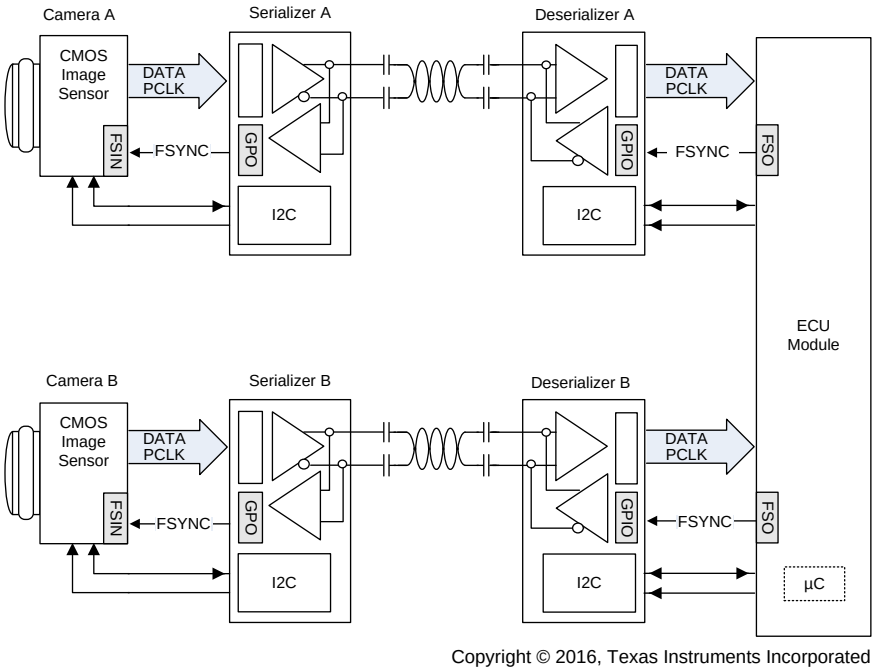





**图 8. Synchronizing Multiple Cameras**

When control data is reconstructed from the bidirectional control channel, there is a time variation of GPIO signals arriving at different target devices between the parallel links (Camera A and B). For synchronization, the maximum latency delta, t1, of the GPIO data transmitted across multiple links is 25 µs. This time spans between the rising edge of GPIO and the time the signal arrives at the camera from the GPIO output of the serializer. Note the timing variations between the different links must always be verified to system and timing specifications. 图 9 shows SER A GPIO output as an example of what exceeding the maximum latency looks like, while SER B falls within the specified time:

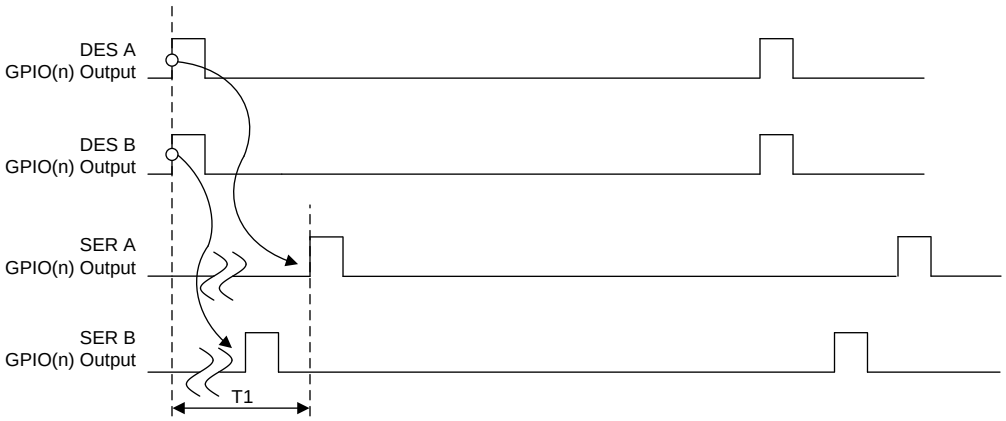



**图 9. GPIO Maximum Latency**

#### 2.4.3.2.4 GPO Pins

There are four GPO pins available on the serializer. However, because this TI Design is running in External Oscillator mode, GPO3 is automatically configured to be the input for the external clock, and GPO2 is configured to be the output of the divide-by-2 clock, which is fed to the imager as its reference clock. This leaves 2 GPO pins for use.

Because this TI Design also needs to be able to use this camera in a synchronized multi-camera system, one of these GPO pins will be used as the frame sync signal transmitter, and the last GPO pin serves as the reset for the imager.

#### 2.4.3.2.5 Power-up and PDB Pin

The Power Down Bar input pin, or PDB pin, enables or disables the serializer. The purpose of PDB is to ensure the serializer turns on when system voltages have stabilized. When PDB is low and it is powered down, the internal PLL is shut off and current draw is minimized. The PDB pin must be ramped after the VDDIO and VDD_n supplies have reach their final voltage levels. In this case, 2.8 V must come up before 1.8 V, then finally PDB. 图 10 shows how the sequence should look:

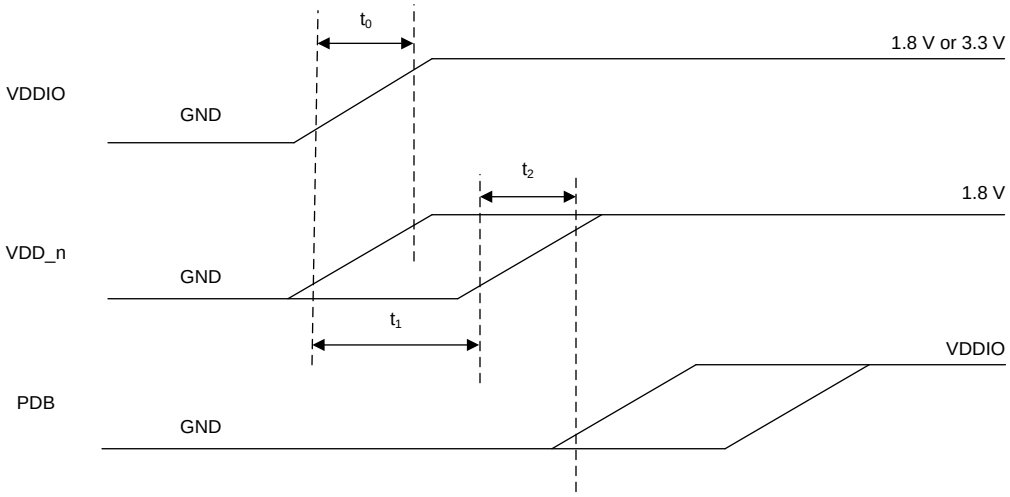



**图 10. Target Power-up Sequence**

In this TI Design, the /RESET output from the 3.3-V switcher enables the serializer through an RC network. As previously discussed, this /RESET signal has a 6-ms delay before asserting high. The RC has a time constant of 5 ms. Note that PDB must be pulled up to $V_{DDIO}$.

#### 2.4.3.2.6 ID[X]

The ID[x] pin is used to assign the device $I^2C$ address. It is used to decode and set the physical slave address of the serializer to allow up to five devices on the bus connected to the serializer. There are six possible addresses for each serializer device.

In this TI Design, device address 0x58 is desired. This requires using a 0-Ω resistor for the bottom resistor, RID, of the ID[X] resistor divider network. See the data sheet for more details about using this ID[X] pin.

# 3 Hardware, Software, Testing Requirements, and Test Results

## 3.1 Required Hardware and Software

The TIDA-01003 needs only one connection to a system with a compatible deserializer over the FAKRA connector.


图 **11. TIDA-01003 Completed Assembly**

注: Screwing the lens in too tight will damage the sensor.

### 3.1.1 Hardware

When the TIDA-01003 is connected to a deserializer board, the LOCK signal on the deserializer should be high. This signifies that the PLL is locked and forward channel communication is possible. The deserializers have a LOCK and PASS pin to monitor the state of the link. On some EVMs, the LOCK status is reported by turning on an LED. Whenever the forward channel link is lost, LOCK will go low. Whenever there is an error detected in the transmission of data, the PASS pin goes low. These two pins used in conjunction are a way to determine the reliability of the link. Triggering on an event such as a loss of LOCK while monitoring other signals, such as the pixel clock or other $I^2C$ commands, can yield very useful information about the system and the link quality. For more details on troubleshooting and diagnostic features of the deserializer, see the corresponding device data sheet.

### 3.1.2 I²C FPD-Link III Initialization

In order to stream video from the imager, the serializer-deserializer pair needs to be properly initialized. This is done in a few simple steps over the backchannel using I²C. As discussed in previous sections, the default addresses of both the serializer and deserializer are selected by voltage dividers on the ID[x] pins. In this TI Design, the default addresses are 0xB0 (0x58 7-bit) for the serializer, and 0xC0 (0x60 in 7-bit) for the '914A-Q1 deserializer and 0x60 (0x30 in 7-bit) for the '934-Q1.

The deserializer must be initialized first as it is the first "stop" in the communication chain. The first step is to write the serializer address to the serializer ID register of the deserializer. This is not always mandatory because ser-des is designed to do this automatically once the pair is locked; this step is included for thoroughness. The second step is to write the ISP address to the slave ID register and the slave alias ID register of the deserializer. Now the deserializer and serializer are initialized. To bring the imager out of reset, the serializer GPO that controls the imager reset must be set high. Once it is set, the TIDA-01003 design is ready to talk to the ISP. The last thing to ensure is that the deserializer is in 12-bit high frequency mode.

The writes to initialize the 913-914 pair are as follows:

- Deserializer I²C address 0xC0 (8-bit) or 0x60 (7-bit):
  - Register 0x07 with 0xB0: Sets serializer ID to 0xB0
  - Register 0x08 with 0x90: Sets slave ID for imager to 0x90
  - Register 0x10 with 0x90: Sets slave alias for imager to 0x90
  - Register 0x1F with 0x12: Overrides mode set by pin, enables 12-bit HF mode
- Serializer I²C address 0xB0 (8-bit) or 0x58 (7-bit):
  - Register 0x0D with 0x99: Sets GPO0 and 1 on serializer, disables remote deserializer GPO control

For the 913-934 pair, see the following writes:

- Deserializer I²C address 0x60 (8-bit) or 0x30 (7-bit):
  - Register 0x4c with 0x01: Enables register writes for Port 0
  - Register 0x58 with 0x58: I²C passthrough enabled
  - Register 0x5C with 0xB0: Sets serializer alias to 0xB0
  - Register 0x65 with 0x90: Sets slave ID for imager to 0x90
  - Register 0x6D with 0x7E: Configures port to coax mode and FPD III to RAW 12 HF mode
- Serializer I²C address 0xB0 (8-bit) or 0x58 (7-bit):
  - Register 0x0D with 0x99: Sets GPO0 and 1 on serializer, disables remote deserializer GPO control

### 3.1.3 Software

The software used to verify and display video is DevWareX, from ON Semiconductor.

## 3.2 Testing and Results

For the following tests, the camera was connected to a single camera system. The DS90UB914A-Q1 or DS90UB934-Q1 EVM was used to connect to the camera module, and a Demo3 was connected to the EVM through two adapter boards.

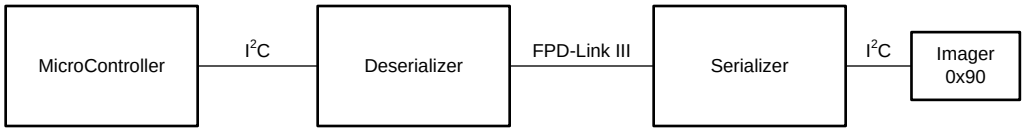



图 12. Simplified Block Diagram

### 3.2.1 Setup for Verifying Power Supply Requirements

The following sections go over the test set up for verification of this TI Design. The power-up sequence, switching frequencies of the DC-DC converters, and system efficiency will be tested. For the switching frequencies and efficiency tests, the camera will be transmitting video.

#### 3.2.1.1 Power-up Sequence

The sequencing requirement is that 2.8-V rail turns on before the 1.8-V rail, and finally PDB is released from reset.

1. 2.8-V ON
2. 1.8-V ON
3. PDB ON

图 13 shows where the test leads are connected.

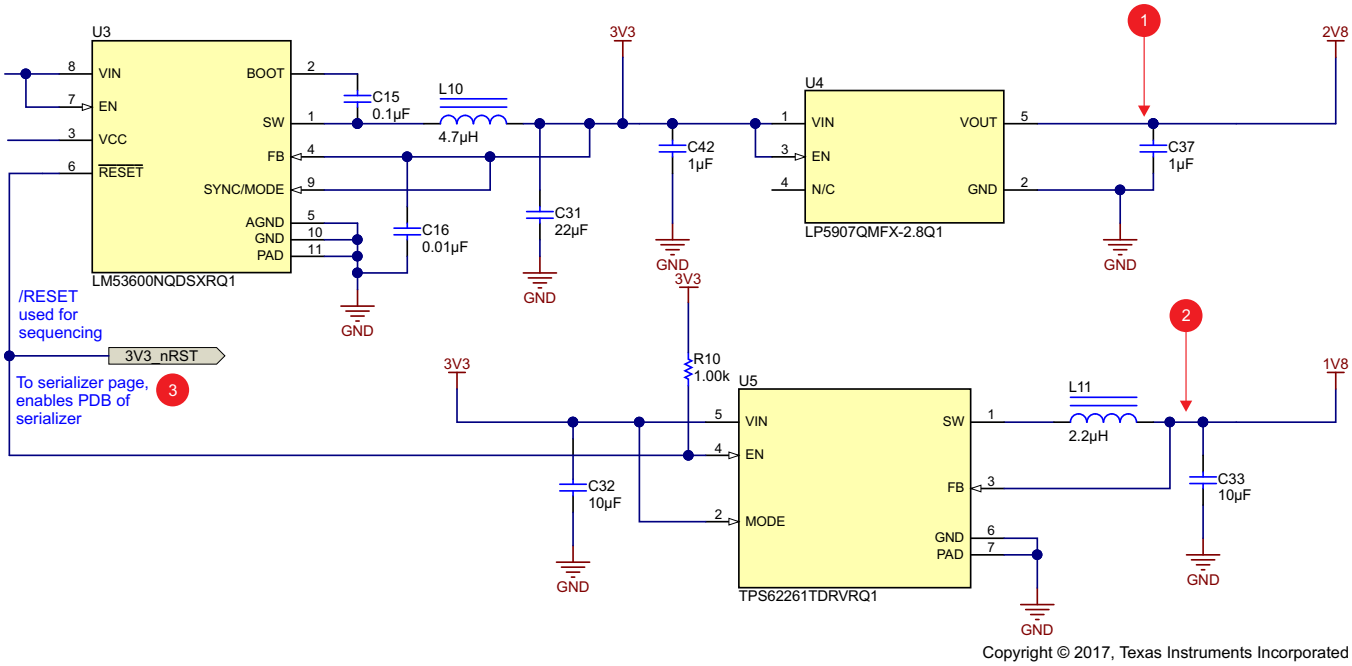



图 13. Power-up Sequence for Test Lead Connections

#### 3.2.1.2 Switching Frequencies

To make sure the switching frequencies are above the AM band (530 kHz to 1.8 MHz), the switched-node side of the inductor for each buck converter is probed with a very small loop. The data shown will be taken while the imager is streaming video.

#### 3.2.1.3 System Power Consumption

The system power consumption is measured for a 9-V PoC input voltage. To measure the power consumption, the current through the PoC inductor that feeds the main 3.3-V system supply is measured through a digital multimeter, and voltage at the input decoupling capacitors for the main 3.3-V system supply is measured. Four states are measured:

1. Pre-initialization (power on)
2. Imager on (serializer-deserializer initialized)
3. Imager initialized
4. Streaming video

#### 3.2.1.4 System Operating Temperature

Using an IR camera, a photo of the board is taken after ten minutes of video transmission. The photo is shown and discussed in 节 3.2.4.1.4.

### 3.2.2 Setup for Verifying Video

The main requirement of this system is of course a clear video feed. The video feed will be tested by showing a screenshot of the video transmission from the software tool DevwareX. The following output formats are demonstrated:

- 8-bit YUV422
- 10-bit YUV422

Results are shown in 节 3.2.4.2.

### 3.2.3 Setup for Verifying I²C Communications

For this test, a Salae logic analyzer with I²C decode is used to monitor the I²C traffic on the buses. The two buses of interest are:

1. I²C connection from serializer to imager
2. I²C connection from microprocessor to deserializer

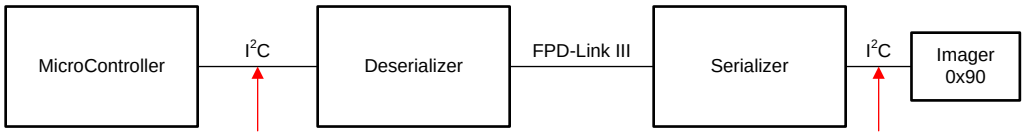



图 **14. Setup for Monitoring I²C Transactions**

When I²C communication is working properly, transactions meant for addresses on the remote end of the FPD-Link III can be detected.

### 3.2.4 Test Data

This section contains the test data to verify the design of the TIDA-01003.

#### 3.2.4.1 Power Supply Requirements Testing and Modification

The power supply is examined to ensure it meets the requirements outlined in 节 3.2.1.

##### 3.2.4.1.1 Power-up Sequence

图 15 shows the target waveform:

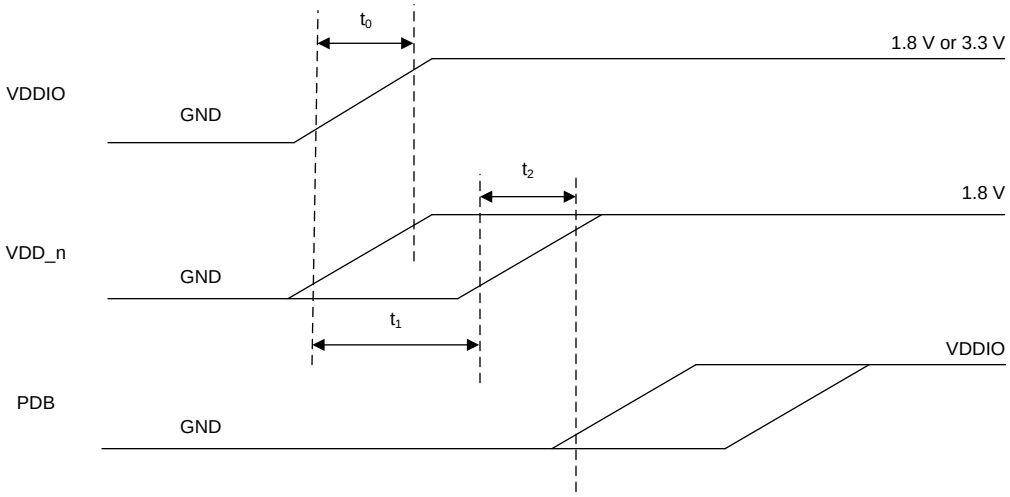



图 15. Target Power-up Sequence

图 16 is the screenshot of the actual power-up sequence.

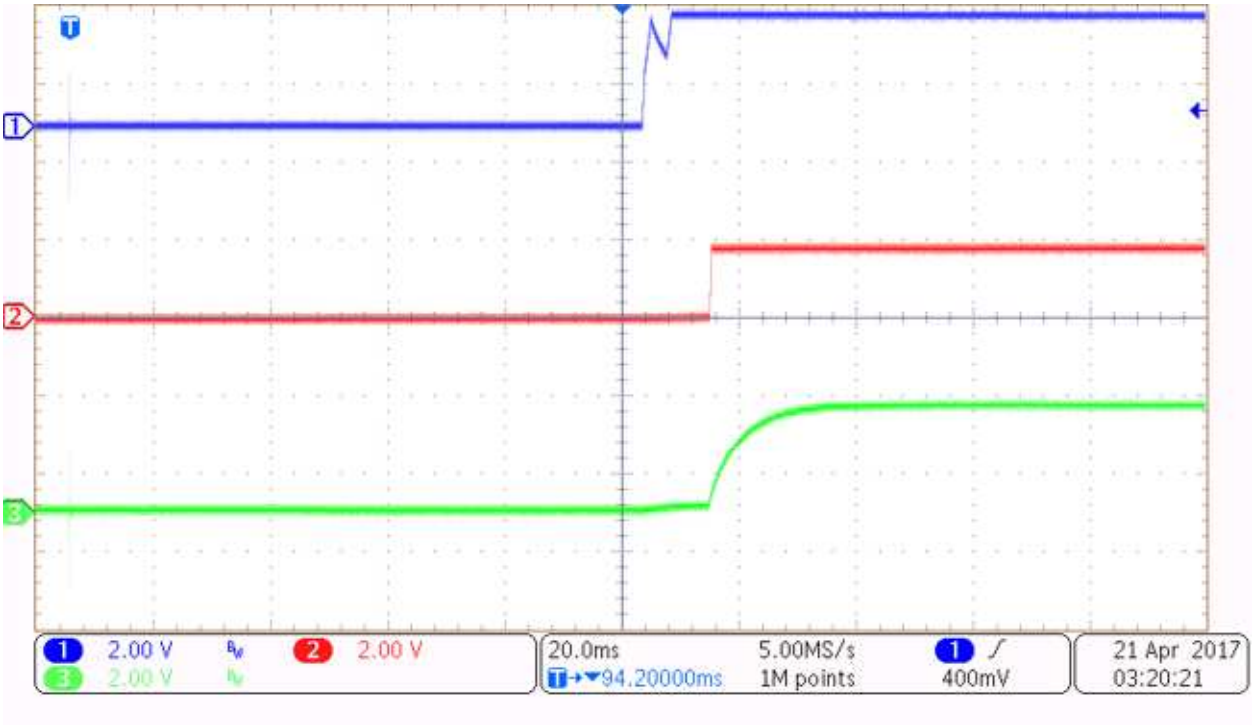



图 16. Power-up Sequence Waveform

As shown in 图 16, 2.8 V is high before 1.8 V, and PDB reaches the high threshold well after the required power sequence due to the delayed /RESET output. This sequence meets our power sequence requirement.

#### 3.2.4.1.2 Switching Frequencies

The switching frequencies of both DC-DC converters are both around 2.1 MHz, a good margin from the AM band. Because both switchers used in this TI Design have a forced fixed-frequency operation (FPWM mode), there is no concern that the switching frequency will dip into the AM band. For the LM53600-Q1, the spread spectrum operation is verified by closely examining the jitter introduced by spread spectrum. The screenshots in 图 17 and 图 18 show the oscilloscope images of the waveforms at the switching node of each DC-DC converter.

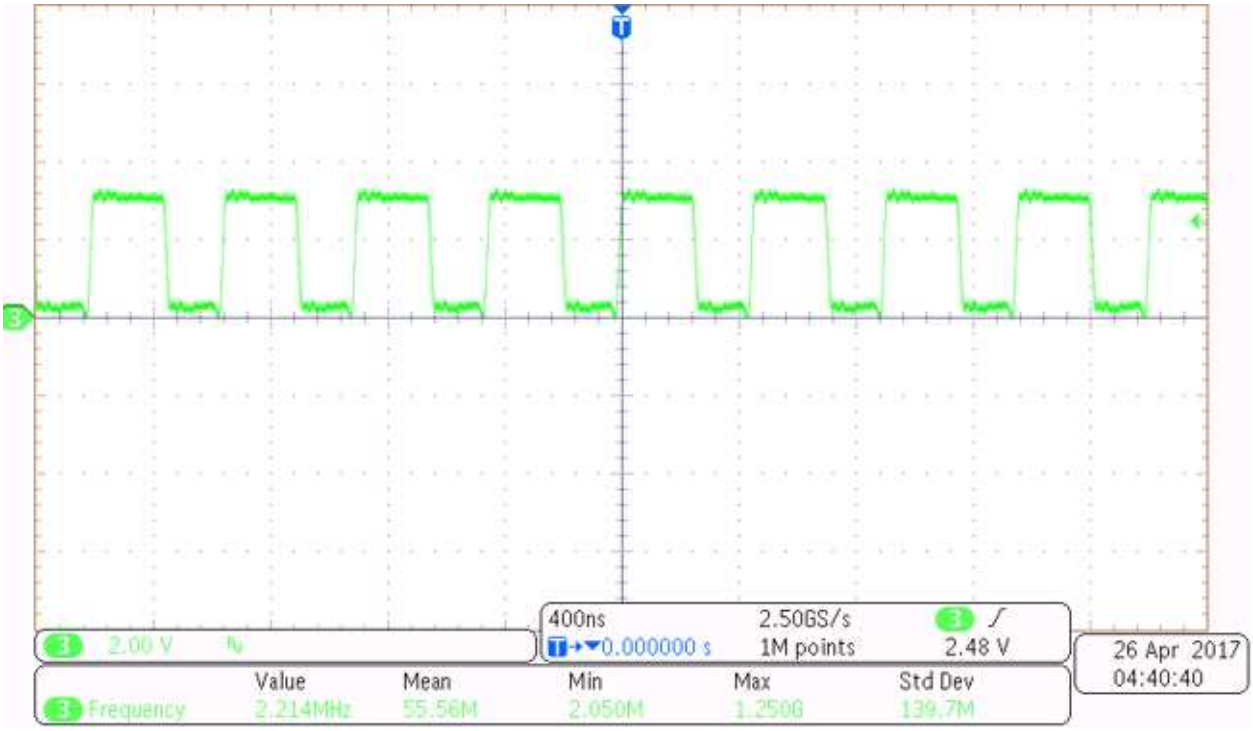



图 **17. 1.8-V Switching Waveform**

As previously described, the 1.8-V switching waveform has a frequency well above the AM band.

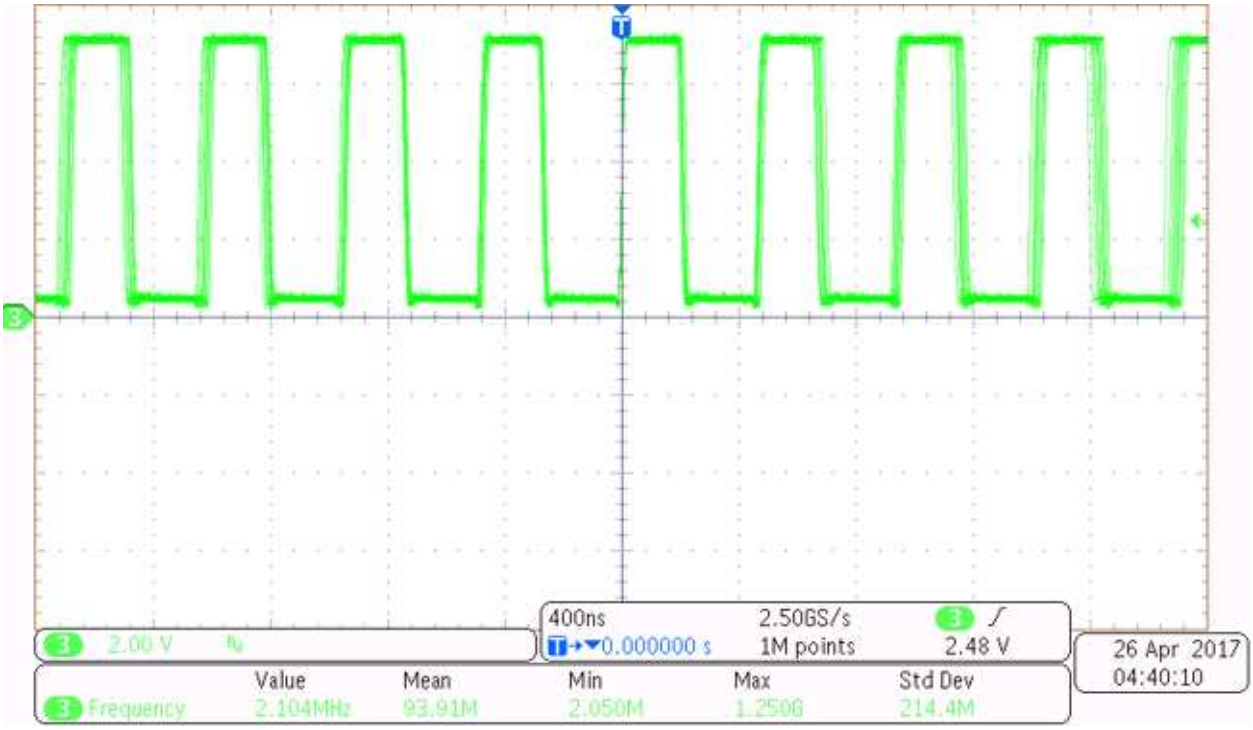



图 **18. 3.3-V Switching Waveform**

For the 3.3-V switch node, notice the jitter in the waveform compared to the 1.8-V switching waveform. This frequency dithering is the action of spread spectrum. As discussed in 节 2.4.2, the spread of energy due to this frequency dithering reduces peaks in the FM band by 6 dB. In 图 19, this jitter is examined more closely:

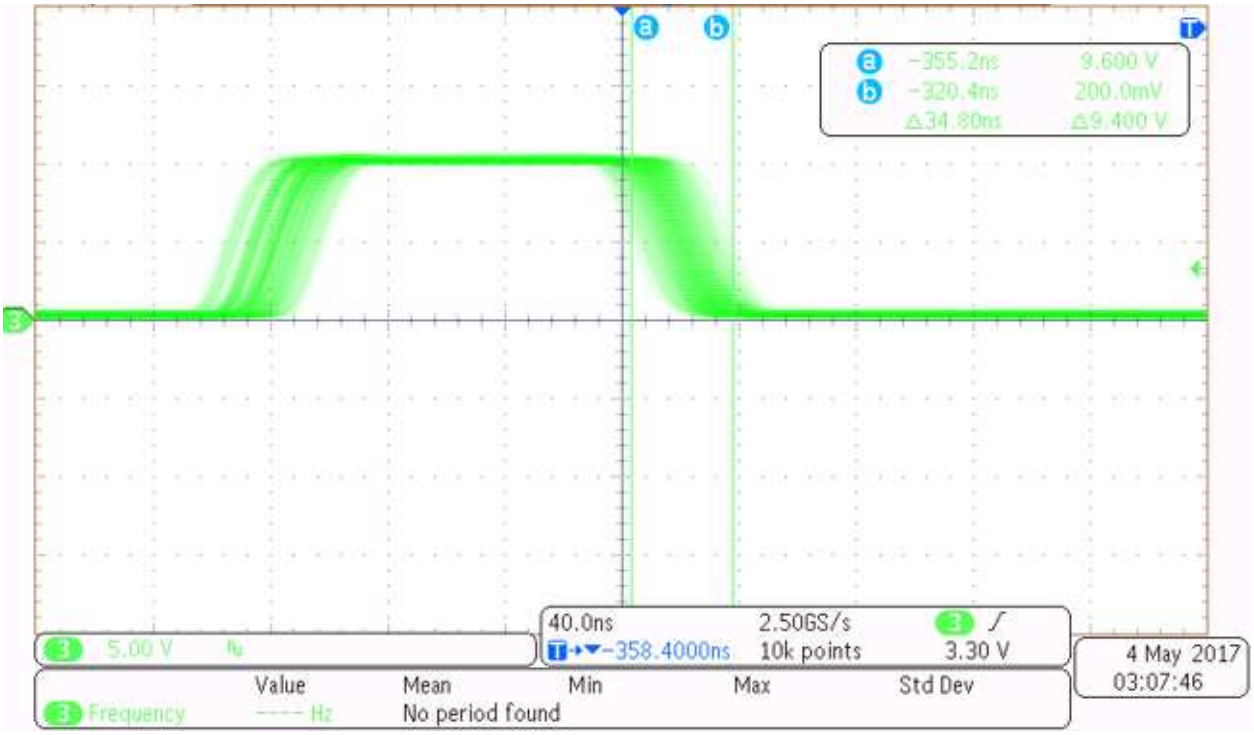



**图 19. Spread Spectrum Operation**

Because the 3.3-V supply is in forced PWM mode to ensure the switching frequency is constant, the switching frequency is expected be around 2.1 MHz. Keeping in mind that the AM band must be avoided, the width of the jitter is estimated by looking at one switching period with the persistence function of the oscilloscope enabled. The deviation in period from the expected switching frequency due to the inherent spread spectrum jitter should not increase the switching period to that of the 1.8-MHz AM band upper limit. The periods of the switching frequency and the upper limit of the AM band are calculated in 公式 3 and 公式 4:

$$T_{SW} = \frac{1}{F_{SW}} = 476 \text{ ns} \quad (3)$$

$$T_{AM_{min}} = \frac{1}{F_{AM_{max}}} = 555 \text{ ns} \quad (4)$$

The difference of period calculated above is 79 ns. To truly fall into the AM band, the period of the switching frequency must not only be increased by 79 ns, but must also persist for multiple switching actions. As shown in 图 19, the cursors estimate the maximum deviation to be ±17 ns for both rising and falling edges. Therefore, it is virtually impossible to switch in the AM band while in FPWM mode with spread spectrum because the inherent jitter does not increase the period more than 17 ns. Further confirmation of AM band avoidance is that the measured frequency of the switching waveform is still 2.1 MHz as shown in 图 18. This jitter does not alter the switching frequency nearly enough to be pushed down into the AM band.

#### *3.2.4.1.3 System Power Consumption*

The system power consumption for the four system states is shown in 表 3:

表 **3. System State Power Consumption**

| STATE | CURRENT DRAW (mA) | VOLTAGE (V) | POWER DRAW (mW) |
|---|---|---|---|
| Pre-initialization | 30 | 8.53 | 256 |
| Imager on | 33 | 8.53 | 281 |
| Imager initialized | 39 | 8.50 | 331 |
| Streaming video | 81 | 8.32 | 672 |

#### 3.2.4.1.4 System Operating Temperature

The screenshot in 图 20 was taken using an IR camera and shows the board temperature after ten minutes of operation.

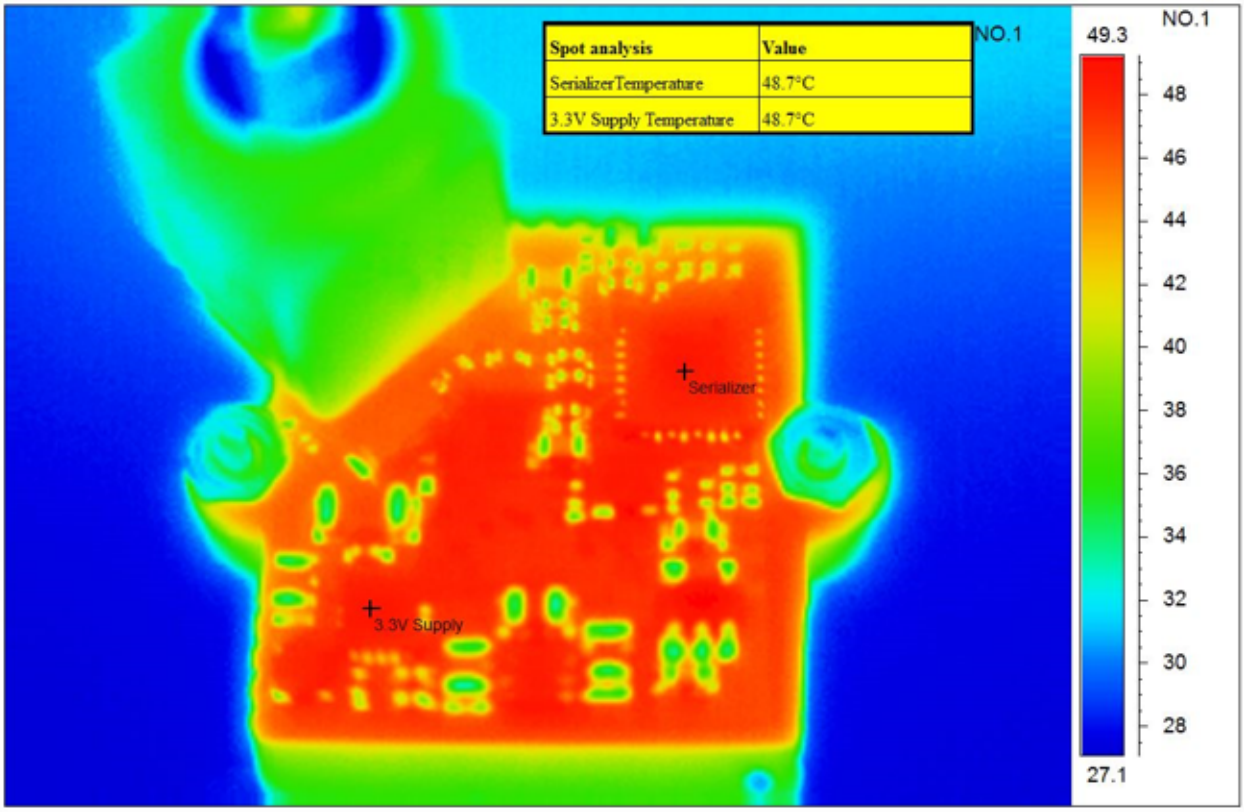



**图 20. Thermal Measurement**

图 21 is the output of the imager while the thermal measurement was being taken. The top right corner displays ISP registers containing operation information such as total frames received, operating mode, device operating temperature, and maximum recorded device temperature.

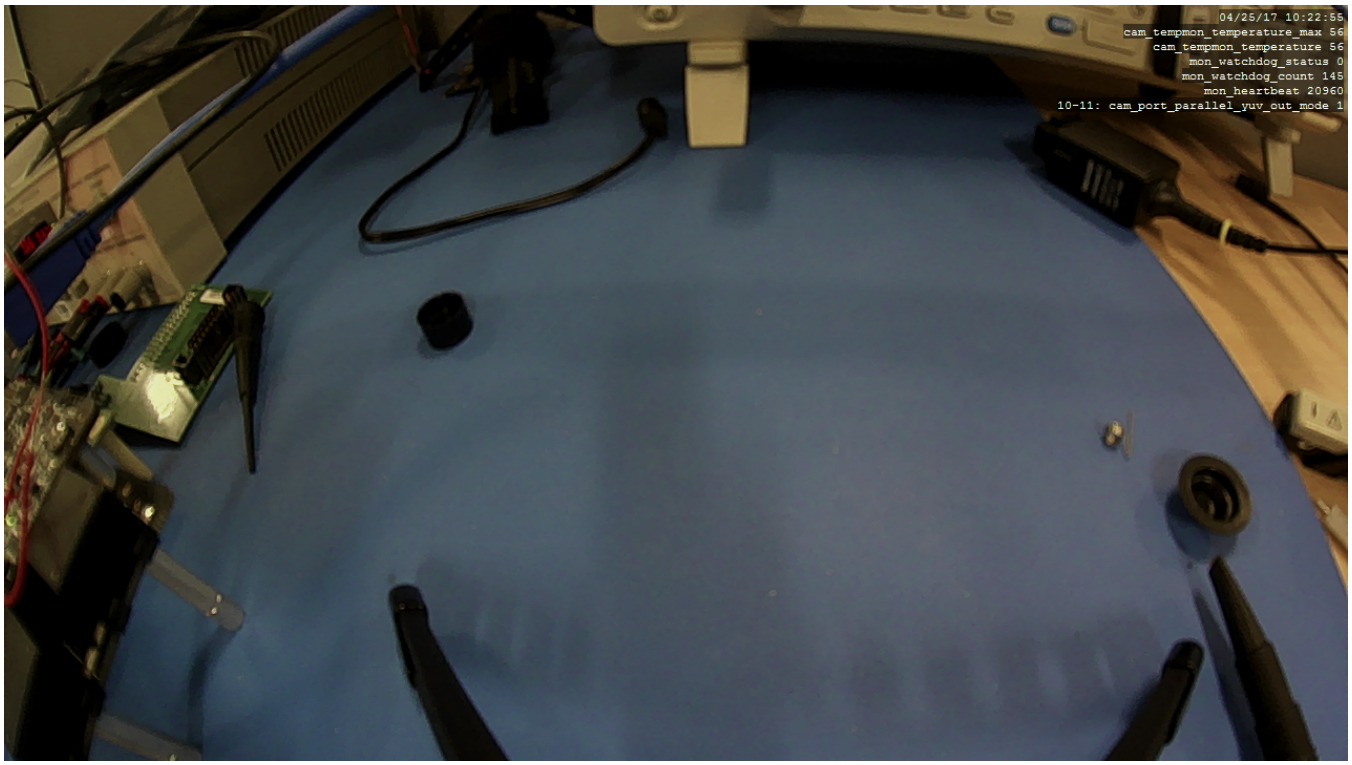



**图 21. Imager Output During Thermal Measurement**

#### 3.2.4.2 Video Verification

图 22 was taken of the live video feed and system info seen on DevWareX, running 720p at 30 fps. The output format is 8-bit YUV422.

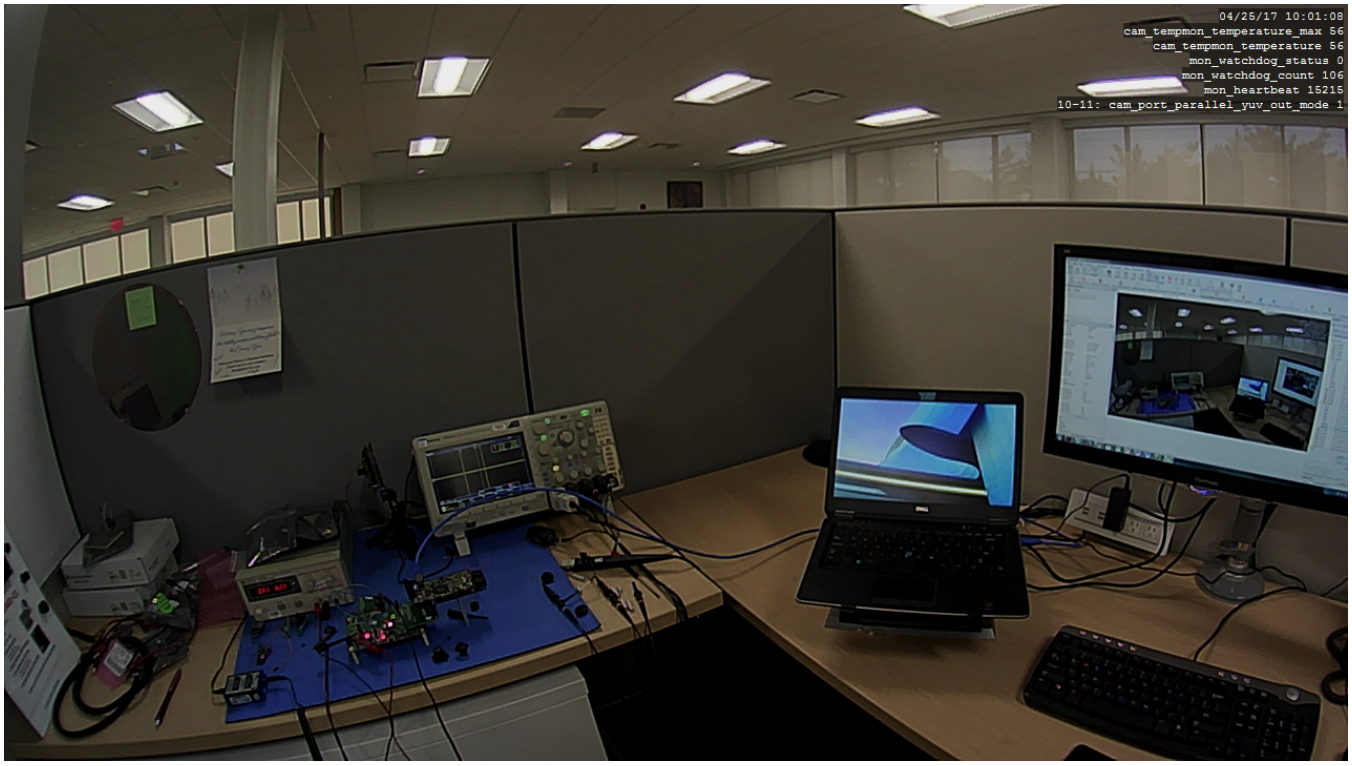



图 **22. 720p at 30 fps**

图 23 shows the 10-bit YUV422.

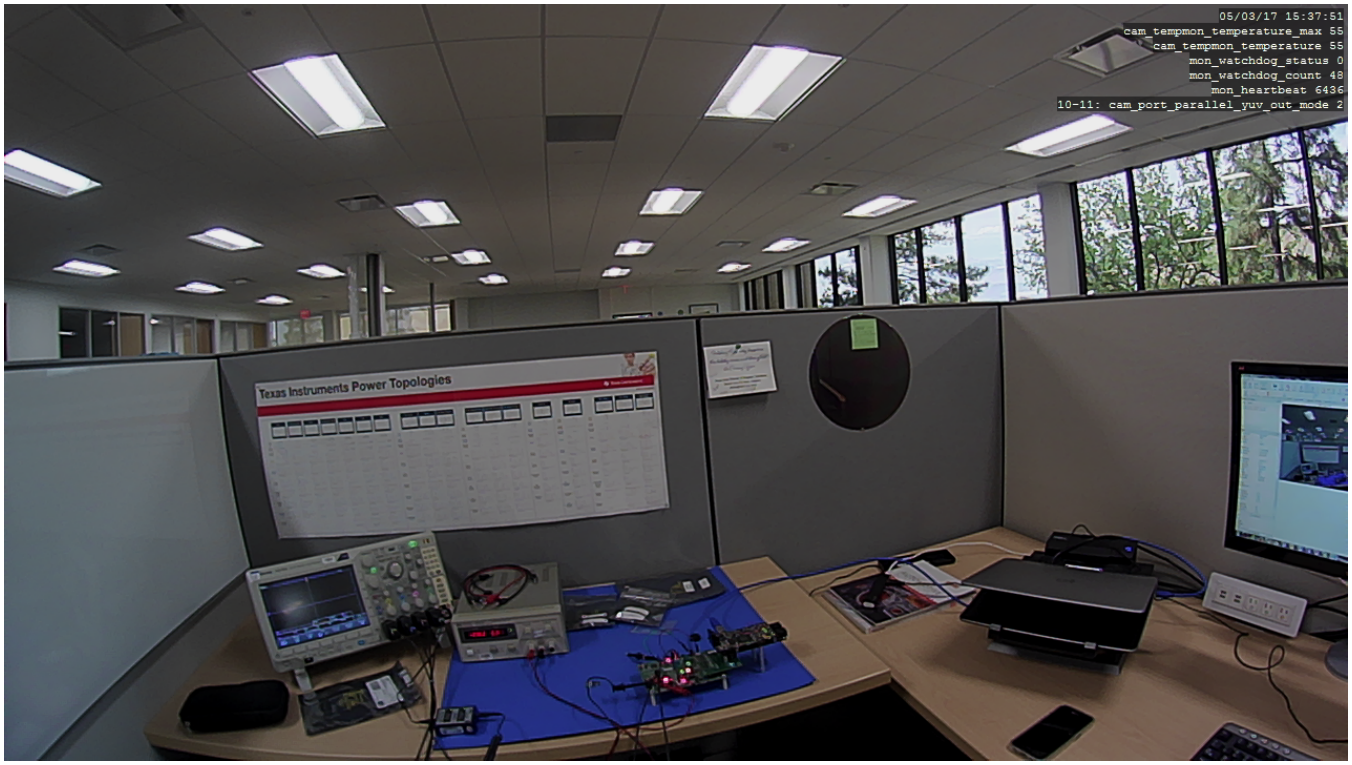



图 **23. 10-bit YUV422**

### *3.2.4.3 I²C Communications*

图 24 shows that the I²C communication through the FPD-Link III is working. The I²C master on the deserializer end successfully reading a register in the ISP is demonstrated in 图 24.

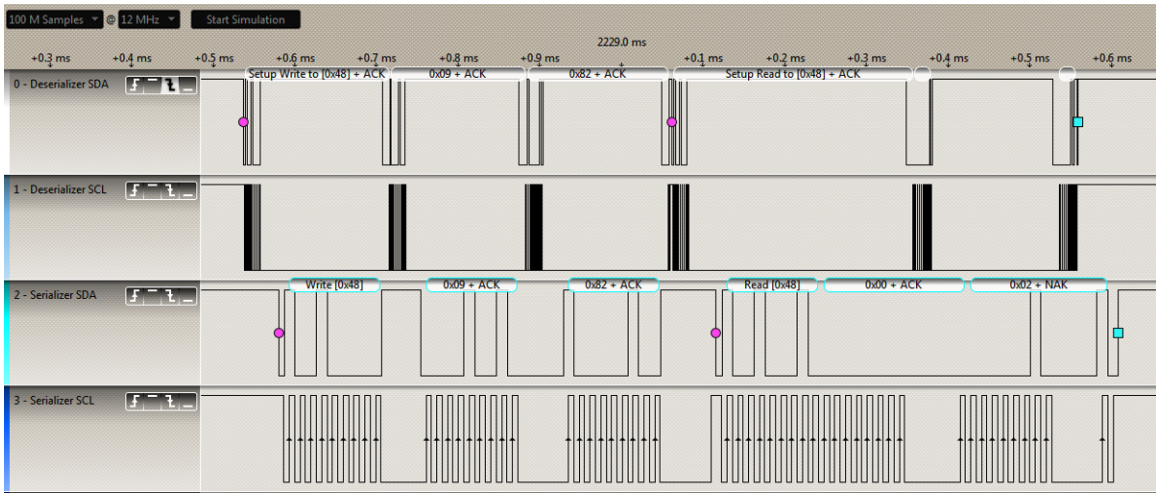



图 **24. I²C ISP Transaction**

This transaction only occurs if the deserializer is properly initialized, as described in 节 3.1.2. By acknowledging the $I^2C$ write, the ISP has confirmed that it is present and active. Reading the status registers can confirm the status of the imager as well as verify that the correct imager was installed during assembly.

# 4 Design Files

## 4.1 Schematics

To download the schematics, see the design files at TIDA-01003.

## 4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01003.

## 4.3 PCB Layout Recommendations

### 4.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-01003.

### 4.3.2 PoC Filter and Power Supplies

During part placement and routing, it is critical to consider all current paths in the circuit, especially fast-changing currents. Careful placement is especially important for this case where both a sensor and ISP are loading each rail. Proper and strategic use of power planes and vias enable maximum performance of the power supplies to respond to dynamic loading and sensitivity of the imager and ISP rails to avoid video defects and FPD-Link communication disruption.

For this TI Design, the top priority is the placement and orientation of the sensor. After the imager placement is locked in, the placement of the PoC filter and power supplies are designed to minimize noise. The distance between the rails of the ISP and the supplies are kept short, and the high di/dt current paths are kept as far away as possible from sensitive circuitry and high-speed video signals. After mapping out critical power paths, the required escaped vias were spaced to minimize voids in the power and ground planes. There are many different ways to prioritize component placement, but for this type of system, prioritizing power paths was the most critical for a high quality system output: clear video.

This layout discussion will begin by following current flowing from the input to the supplies. First, current coming in from the coax connector flows through the first ferrite bead, L1, then through the PoC filter inductors L3 and L4 to charge the 3.3-V supply input capacitors C30 and C2. Capacitor C41 filters out any high-frequency noise not blocked by the two inductors. Ideally, the PoC filter hugs the coax connector as tightly as possible to minimize the area of the high-frequency current loop. However, there are several escape vias from the imager and ISP that could not be moved. The inductors are turned parallel to the high-speed trace to the serializer to allow space for these vias. In 图 25, the red arrow shows DC flow, and the green arrow shows the return path for high-frequency current:

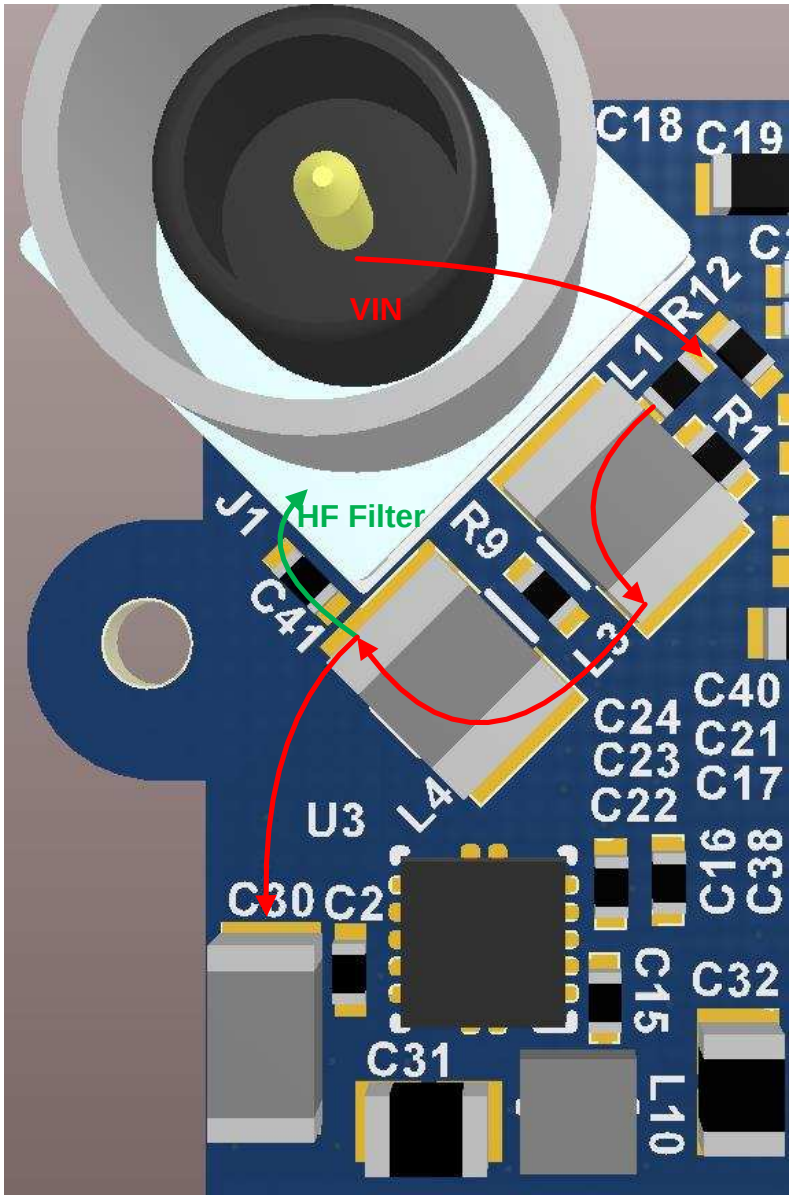



**图 25. PoC Current Path**

Note that bypass capacitor C2 is placed as close to the input of U3 as possible. Because smaller capacitors have low impedance at high frequencies, this placement provides a short, low impedance path to minimize the area of the high di/dt current loop of the 3.3-V supply.

The 3.3-V supply is shown in 图 26:

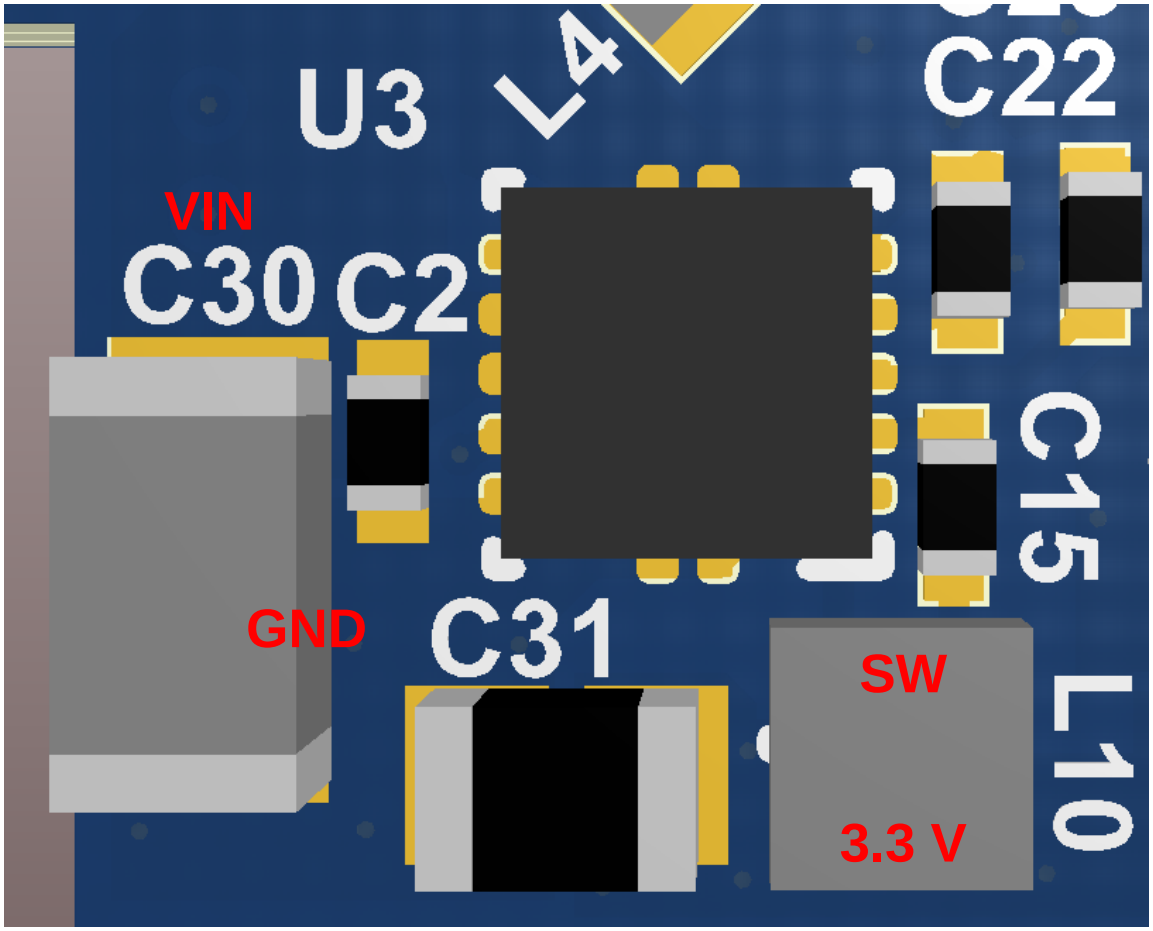



图 **26. 3.3-V Supply**

The layout for the 3.3-V supply is nearly an exact copy of the recommended layout in the device data sheet. As previously mentioned, the input bypass capacitors are close to the input, with the higher-frequency bypass capacitor closest to the input. The ground plane labeled with red text follows the requirements of a large area connecting the grounds of the input capacitors C30 and C2, output capacitor C31, and thermal pad of the device U3. Any return currents from the input capacitor C30 and C2 or the output capacitor C31 are joined together at the bottom left of U3 before they are connected to the ground plane. This setup reduces the amount of return currents and, thereby, voltage gradients in the ground plane. It may not be noticeable in the performance of the converter, but it reduces noise coupling into other devices.

图 27 shows the 3.3-V plane.

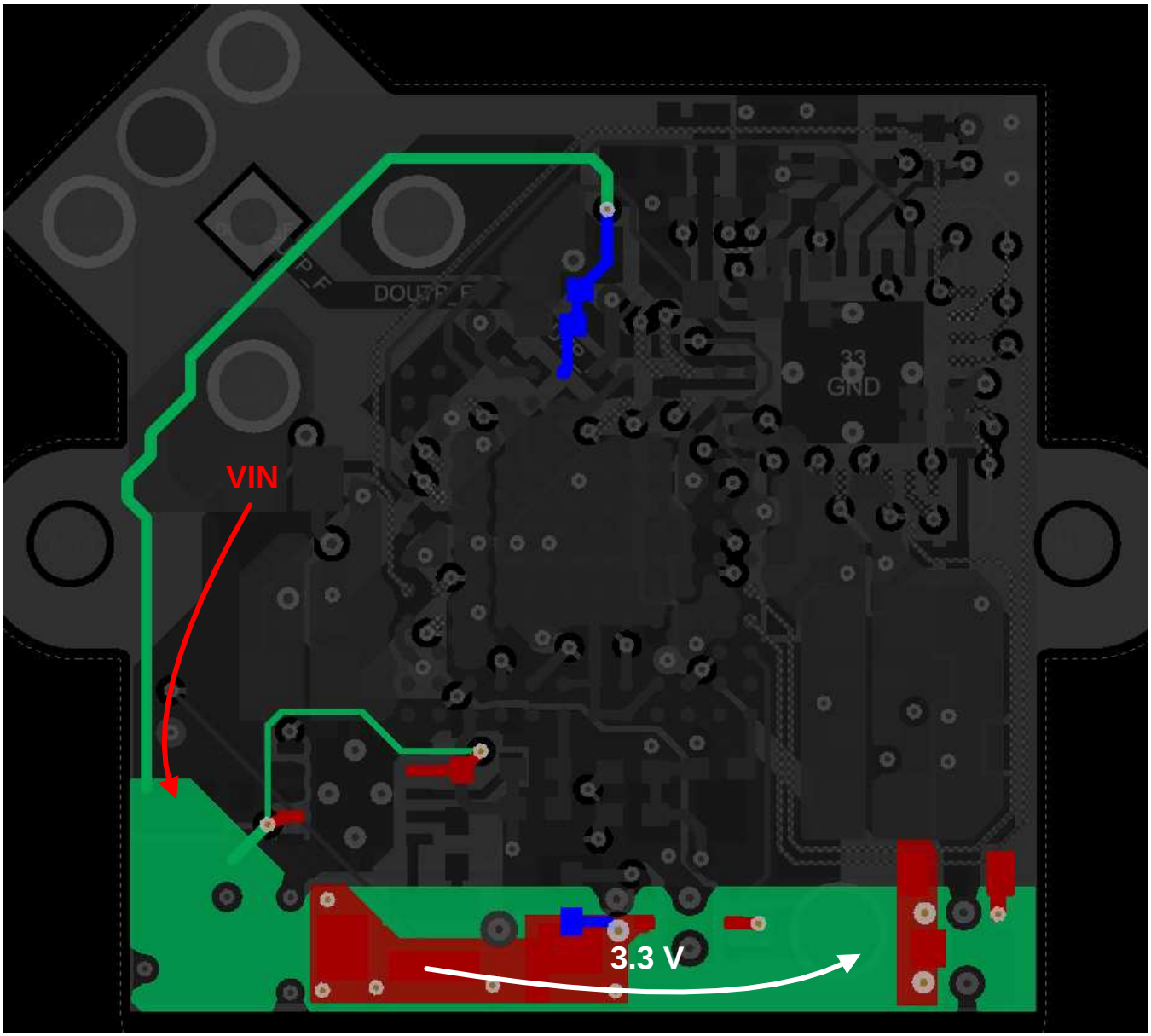



图 **27. 3.3-V Plane**

The red layer is the top layer of the board, the green layer is the fourth layer, and the blue is the bottom layer. The input to the 3.3-V supply runs along the side edge of the board on the top layer, and the 3.3-V plane runs along the bottom edge of the board, feeding the both 1.8- and 2.8-V supplies whose inputs are also near the bottom edge. This isolates any power supply noise to the bottom edge of the board, between the supplies and away from the sensitive devices and circuitry. There is a thin, long trace to the top of the board, but this trace is simply to provide 3.3 V to the DAC voltage for the ISPs analog video output, which is not used in this design, and draws virtually no current. Next is the 1.8-V switcher and 1.8-V plane.

For the 1.8-V switcher, U5, the same switcher layout concepts discussed before apply in 图 28:

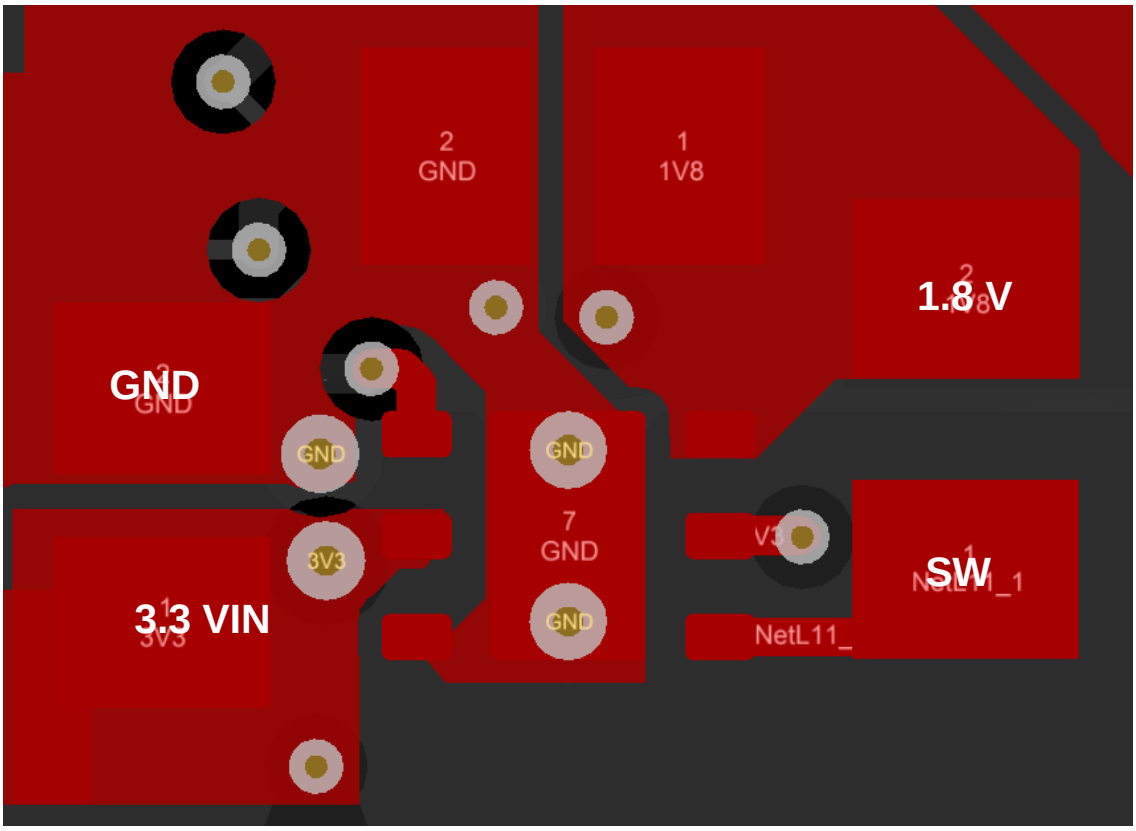



图 **28. 1.8-V Supply**

The input capacitor, C32, is as close to the input as possible, and the ground of C32 as close as possible to the ground of the output capacitor, C33. These grounds are tied together with a wide polygon pour and connected to the device ground. The large shared ground plane for the device thermal pad, input, and output capacitors, are desired because these short and large traces minimize any series parasitic inductances that could potentially cause ringing at the switching node or create additional voltage drops. See the 1.8-V plane in 图 29:

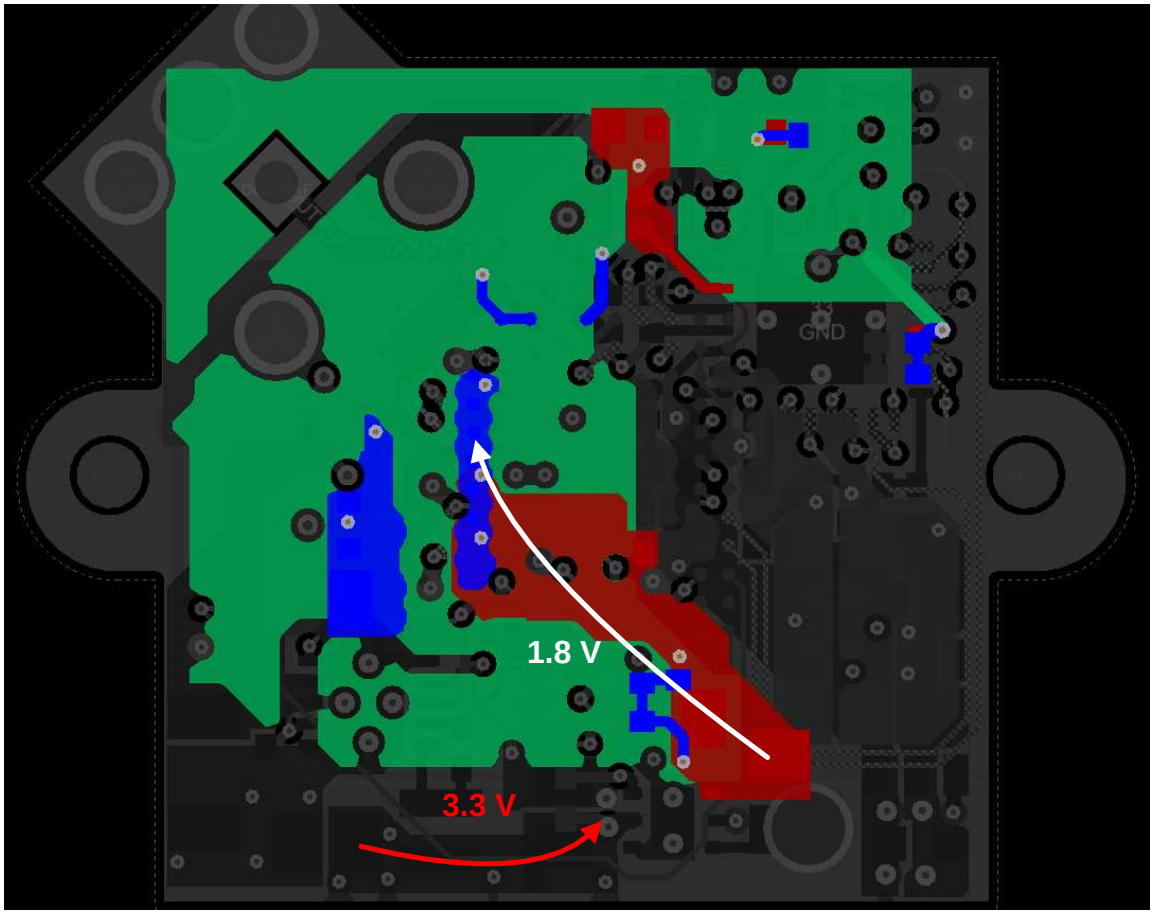



图 **29. 1.8-V Plane**

Because the supply is on the top layer, the 1.8-V output connects to the plane on the top layer and extends on the top layer directly over the pins of the ISP on the bottom layer to minimize the number of layer transitions. Wherever there is a via for power, there is a nearby ground via to keep the high-frequency current loops to the ISP as tight as possible. This via minimizes noise coupling into surrounding circuitry and minimizes the loop inductance of high-frequency current flowing to the ISP. At least three vias per layer are used to minimize any parasitic resistance and inductances due to the vias themselves. Next is the 2.8-V supply and 2.8-V plane.

Because the 2.8-V supply is an LDO, the layout is extremely straightforward. Ideally, this supply is on the same layer as the imager and ISP to minimize distance between the supply and load and reduce any potential high di/dt loops. However, due to size limitations, this supply could only fit on the top layer. Both input and output capacitors are close to the input and output of the LDO, respectively, and the grounds of the capacitors are tied together on the top layer along with the LDO ground. The complications arise when placing vias to minimize current loops as done for the 1.8- and 3.3-V planes. The 2.8-V rail for the ISP resides on the "right" side of the ISP, which is partially underneath the serializer. Both ISP and serializer have necessary escape vias that make placing power-ground via pairs more difficult. Nonetheless, the effort is taken to find optimal placement of the via pairs:

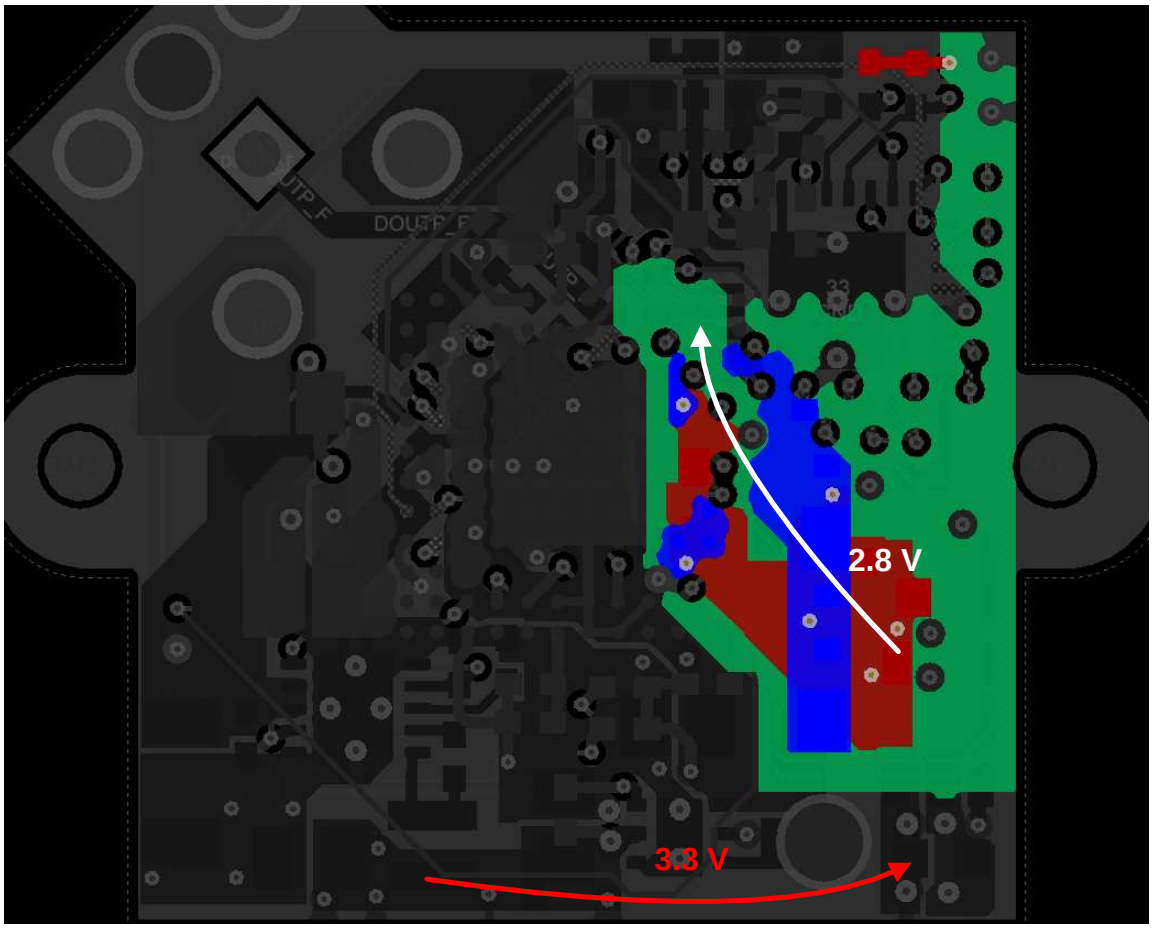



图 **30. 2.8-V Plane**

One final point regarding the layout in terms of power is that the power planes are on the fourth layer, or as close to the bottom layer as possible. Because the ISP consumes the most current and is placed on the bottom layer, keep the power plane close to the layer that sees the most current draw. This placement further minimizes the current loop area to the ISP so it only needs to go through at most two layers instead of three or more.

### 4.3.3 Serializer Layout Recommendations

Decoupling capacitors need to be as close to the supply pins of the serializer as possible. Just like before, this requires that considering the path of the supply current and the return current. Keeping the loop area of this connection small reduces the parasitic inductance associated with the connection of the capacitor and minimizes EMI. Smaller value capacitors that provide higher frequency decoupling should be placed closest to the device. Due to the space constraints of this design, ideal placement may not always be possible.

For this application, a single-ended controlled impedance of 50 Ω is required for the coax interconnect. The calculated trace width to achieve this is 23 mils. Whenever possible, this trace should be kept short to reduce system susceptibility to noise and minimize EMI. The routing of the high-speed serial line is shown in 图 31 with trace measurements overlaying each segment of the trace. The total length of the trace from signal pin on the coax connecter to the AC coupling capacitor is just 9.1 mm (358 mils or 0.358 inches). The stackup is discussed in the next section.

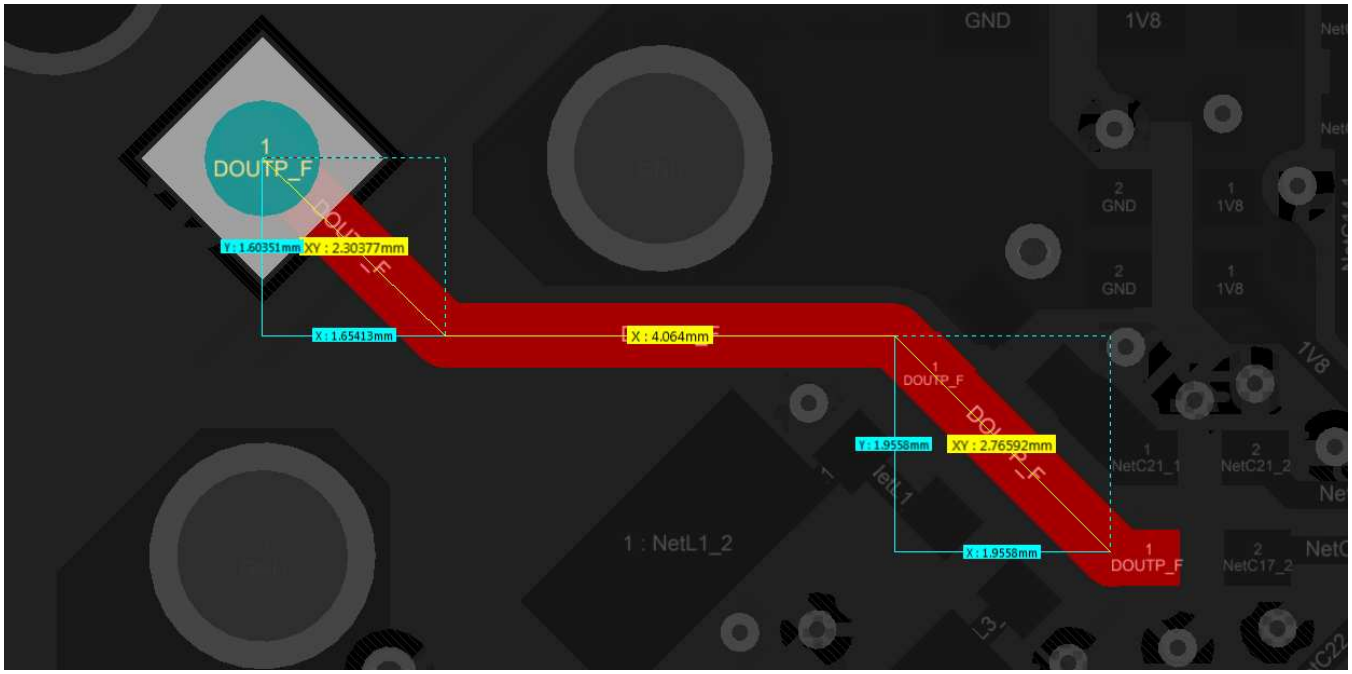
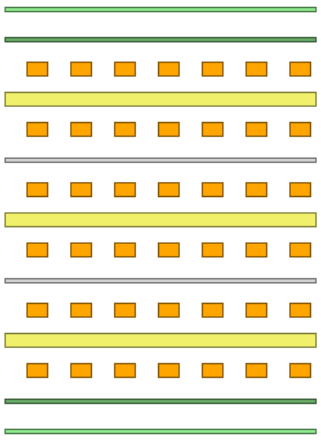



图 **31. High-Speed Data Line Trace**

### 4.3.4 PCB Layer Stackup Recommendations

The following recommendations are for the PCB layer stackup. Because automotive is the target space, there are a few extra measures and considerations to take when dealing with high-speed signals and small PCBs.

- Use at least a four-layer board with a power and ground plane. Locate LVCMOS signals away from the differential lines to prevent coupling from the LVCMOS lines to the differential lines.
- If using a four-layer board, layer two should be a ground plane. Because most of the components and switching currents are on the top layer, this middle ground layer reduces the inductive effect of the vias when currents are returned through the plane.
- An additional two layers were used in this board to simplify BGA and serializer fan out and routing. 图 32 shows the stack up used in this board.



| Layer Name | Type | Material | Thickness (mil) | Dielectric Material | Dielectric Constant |
|---|---|---|---|---|---|
| Top Overlay | Overlay | | | | |
| Top Solder | Solder Mask/Co... | Surface Material | 0.4 | Solder Resist | 3.5 |
| Layer 1 - Top Lay... | Signal | Copper | 1.4 | | |
| Dielectric 1 | Dielectric | Core | 12.6 | 370HR | 4.2 |
| Layer 2 - GND | Signal | Copper | 1.417 | | |
| Dielectric 2 | Dielectric | Prepreg | 8 | 370HR | 4.2 |
| Layer 3 - Signal | Signal | Copper | 1.417 | | |
| Dielectric 3 | Dielectric | Core | 11.6 | 370HR | 4.2 |
| Layer 4 - Power | Signal | Copper | 1.417 | | |
| Dielectric 4 | Dielectric | Prepreg | 8 | 370HR | 4.2 |
| Layer 5 - GND | Signal | Copper | 1.42 | | |
| Dielectric 5 | Dielectric | Core | 12.6 | 370HR | 4.2 |
| Layer 6 - Bottom... | Signal | Copper | 1.4 | | |
| Bottom Solder | Solder Mask/Co... | Surface Material | 0.4 | Solder Resist | 3.5 |
| Bottom Overlay | Overlay | | | | |

**图 32. Layer Stackup**

### 4.4 Altium Project

To download the Altium project files, see the design files at TIDA-01003.

### 4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01003.

### 4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01003.

## 5 Software Files

To download the software files, see the design files at TIDA-01003.

## 6 Related Documentation

1. Texas Instruments, *Sending Power Over Coax in DS90UB913A Designs Application Report*
2. Texas Instruments, *Cable Requirements for the DS90UB913A & DS90UB914A Application Report*
3. Texas Instruments, *Low-Noise CMOS Camera Supply Application Report*

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# 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

**Changes from Original (May 2017) to A Revision** **Page**

- 已更改 Figure 2: *Front of Board* ..... 6
- 已更改 Figure 3: *Back of Board* ..... 7
- 已更改 Figure 6: *Power Over Coax Schematic* ..... 12
- Combined hardware, software, and testing sections to follow current template ..... 17
- Updated layout guidelines in Section 4.3.2: *PoC Filter and Power Supplies* ..... 31
- 已更改 Figure 25: *PoC Current Path* ..... 32
- 已更改 Figure 26: *3.3-V Supply* ..... 33
- 已添加 Figure 27: *3.3-V Plane* ..... 34
- 已更改 Figure 28: *1.8-V Supply* ..... 35
- 已更改 Figure 29: *1.8-V Plane* ..... 36
- 已更改 Figure 30: *2.8-V Plane* ..... 37
- layout guidelines in Section 4.3.3: *Serializer Layout Recommendations* ..... 38
- 已删除 Figure 30: $V_{DDPLL}$ *and* $V_{DDIO}$ *Decoupling Capacitors Loop* ..... 38
- 已更改 Figure 31: *High-Speed Data Line Trace* ..... 38
- 已更改 Figure 32: *Layer Stackup* ..... 39

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