

TPS736 具有反向电流保护功能的无电容 NMOS、400mA 低压降稳压器

1 特性

- 不借助输出电容器或者任何电容值或类型的电容器即可实现稳定
- 输入电压范围为 1.7V 至 5.5V
- 超低压降电压：75mV (典型值)
- 无论是否使用可选输出电容器，均可实现出色的负载瞬态响应
- NMOS 拓扑可提供低反向漏电流
- 低噪声：30 μ V_{RMS} 典型值 (10Hz 至 100kHz)
- 初始精度为 0.5%
- 整个线路、负载和温度范围内的精度达 1%
- 关断模式下 I_Q 最大值小于 1 μ A
- 热关断和指定最小/最大电流限制保护
- 提供了多个输出电压版本：
 - 1.20V 至 5.0V 固定输出
 - 1.20V 至 5.5V 的可调输出
 - 可提供定制输出

2 应用

- 便携式、电池供电类设备
- 适用于开关电源的后置稳压
- 噪声敏感电路 (如 VCO)
- 适用于 DSP、FPGA、ASIC 和微处理器的负载点调节

3 说明

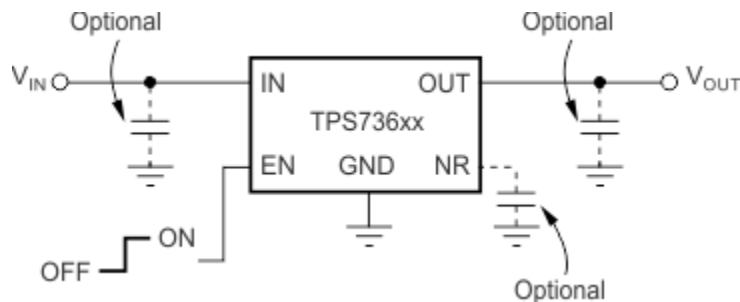
TPS736 低压降 (LDO) 线性稳压器采用全新的拓扑结构：在电压跟随器配置中使用 NMOS 导通晶体管。这个拓扑结构在使用具有低等效串联电阻 (ESR) 的输出电容器时保持稳定，甚至可实现无电容器运行。该器件还提供高反向阻断 (低反向电流) 和接地引脚电流 (在所有输出电流值范围内几乎保持恒定)。

TPS736 利用先进的 BiCMOS 工艺实现高精度，同时提供超低压降电压和低接地引脚电流。未启用时，电流消耗低于 1 μ A，非常适合于便携式应用。极低的输出噪声 (0.1 μ F C_{NR} 时为 30 μ V_{RMS}) 使得此器件非常适合为 VCO 供电。该器件受到热关断和折返电流限制的保护。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 ⁽²⁾
TPS736	DBV (SOT-23, 5)	2.9mm × 2.8mm
	DCQ (SOT-223, 6)	6.5mm × 7.06mm
	DRB (VSON, 8)	3mm × 3mm

- (1) 如需更多信息，请参阅 [机械、封装和可订购信息](#)。
 (2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。



针对固定电压版本的典型应用电路



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4 Pin Configuration and Functions

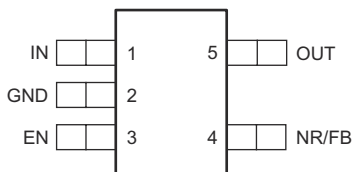


图 4-1. DBV Package, 5-Pin SOT-23 (Top View)

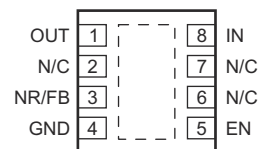


图 4-2. DRB Package, 8-Pin VSON (Top View)

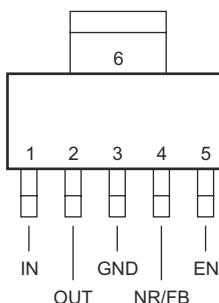


图 4-3. DCQ Package, 6-Pin SOT-223 (Top View)

表 4-1. Pin Functions

PIN				TYPE	DESCRIPTION
NAME	NO.				
	SOT-23	SOT-223	VSON		
EN	3	5	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See the <i>Enable Pin and Shutdown</i> section for more details. EN can be connected to IN if not used.
FB	4	4	3	I	Adjustable-voltage version only. This pin is the input to the control loop error amplifier, and sets the output voltage of the device.
GND	2	3, 6	4, Pad	—	Ground.
IN	1	1	8	I	Input supply.
NR	4	4	3	—	Fixed-voltage versions only. Connecting an external capacitor to this noise reduction pin bypasses noise generated by the internal band gap, reducing output noise to very low levels.
OUT	5	2	1	O	Output of the regulator. There are no output capacitor requirements for stability.

5 Specifications

5.1 绝对最大额定值

在工作结温范围内测得（除非另有说明）⁽¹⁾

		最小值	最大值	单位
电压	输入, V_{IN}	-0.3	6	V
	使能, V_{EN}	-0.3	6	
	输出, V_{OUT}	-0.3	5.5	
	V_{NR} 、 V_{FB}	-0.3	6	
电流	最大输出, I_{OUT}	受内部限制		
输出短路持续时间		未确定		
持续总功率耗散	P_{DISS}	请参阅热性能信息		
温度	工作结温, T_J	-55	150	°C
	贮存温度, T_{stg}	-65	150	

- (1) 超出绝对最大额定值运行可能会对器件造成永久损坏。绝对最大额定值并不表示器件能够在该等条件下或在任何超出建议运行条件的其他条件下正常运行。如果在建议运行条件以外,但在绝对最大额定值范围以内使用,器件可能无法完全正常运行,这可能会影响器件的可靠性、功能与性能,并且可能缩短器件寿命。

5.2 ESD 等级

			值	单位
$V_{(ESD)}$	静电放电	人体放电模型 (HBM), 符合 ANSI/ESDA/JEDEC JS-001 标准, 所有引脚 ⁽¹⁾	±2000	V
		充电器件模型 (CDM), 符合 JEDEC 规范 JESD22-C101, 所有引脚 ⁽²⁾	±500	

- (1) JEDEC 文档 JEP155 指出: 500V HBM 时能够在标准 ESD 控制流程下安全生产。

- (2) JEDEC 文档 JEP157 指出: 250V CDM 时能够在标准 ESD 控制流程下安全生产。

5.3 建议运行条件

在工作结温范围内测得（除非另有说明）

		最小值	标称值	最大值	单位
V_{IN}	输入电源电压	1.7		5.5	V
I_{OUT}	输出电流	0		400	mA
T_J	工作结温	-40		125	°C

5.4 热性能信息

热指标 ⁽¹⁾		TPS736 新器件			单位
		DRB (VSON)	DCQ (SOT-223)	DBV (SOT-23)	
		8 引脚	6 引脚	5 引脚	
$R_{\theta JA}$	结至环境热阻	49.4	76	185.2	°C/W
$R_{\theta JC(top)}$	结至外壳 (顶部) 热阻	76.6	46.6	82.9	°C/W
$R_{\theta JB}$	结至电路板热阻	22.0	18.1	53.1	°C/W
ψ_{JT}	结至顶部特征参数	3.8	8.6	21.1	°C/W
ψ_{JB}	结至电路板特征参数	22.0	17.6	52.7	°C/W
$R_{\theta JC(bot)}$	结至外壳 (底部) 热阻	3.8	不适用	不适用	°C/W

- (1) 有关新旧热指标的更多信息, 请参阅半导体和 IC 封装热指标应用手册。

5.5 热性能信息

热指标 ^{(1) (2)}		TPS736 传统器件 ⁽³⁾			单位
		DRB (VSON)	DCQ (SOT-223)	DBV (SOT-23)	
		8 引脚	6 引脚	5 引脚	
$R_{\theta JA}$	结至环境热阻 ⁽⁴⁾	52.8	118.7	221.9	°C/W
$R_{\theta JC(top)}$	结至外壳 (顶部) 热阻 ⁽⁵⁾	60.4	64.9	74.9	°C/W
$R_{\theta JB}$	结到电路板热阻 ⁽⁶⁾	28.4	65.0	51.9	°C/W
ψ_{JT}	结到顶部的表征参数 ⁽⁷⁾	2.1	14.0	2.8	°C/W
ψ_{JB}	结到电路板的表征参数 ⁽⁸⁾	28.6	63.8	51.1	°C/W
$R_{\theta JC(bot)}$	结到芯片外壳 (底部) 热阻 ⁽⁹⁾	12.0	不适用	不适用	°C/W

- (1) 有关新旧热指标的更多信息, 请参阅 [半导体和 IC 封装热指标](#) 应用手册。
- (2) 如需根据 PCB 覆铜区对该器件进行热量估算, 请参阅 [TI PCB 热量计算器](#)。
- (3) DRB、DCQ 和 DBV 封装的热数据是根据 JESD51 系列中指定的 JEDEC 标准方法进行热仿真得出的。仿真时使用了以下假设：
 - (a) i. DRB：外露焊盘通过 2x2 散热过孔阵列连接到 PCB 接地层。
 - ii. DCQ：外露焊盘通过 3x2 散热过孔阵列连接到 PCB 接地层。
 - iii. DBV：DBV 封装没有外露焊盘。
 - (b) i. DRB：假设顶部和底部铜层的导热率为铜的 20%，表示铜覆盖率为 20%。
 - ii. DCQ：每个顶部和底部铜层都有一个专用图案，可实现 20% 的铜覆盖。
 - iii. DBV：假设顶部和底部铜层的导热率为铜的 20%，表示铜覆盖率为 20%。
 - (c) 这些数据生成时只有一个器件位于 JEDEC 高 K (2s2p) 电路板的中心，覆铜区为 3 英寸 × 3 英寸。要了解覆铜区对热性能的影响，请参阅本数据表的“功率耗散”部分。
- (4) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的规定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻。
- (5) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳 (顶部) 的热阻。不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。
- (6) 结至板热阻，可按照 JESD51-8 中的说明在使用环形冷板夹具来控制 PCB 温度的环境中进行仿真来获得。
- (7) 结至顶部特征参数 ψ_{JT} 估算器件在实际系统中的结温，可通过 JESD51-2a (第 6 节和第 7 节) 介绍的步骤从获得 $R_{\theta JA}$ 的仿真数据中获取该温度。
- (8) 结至电路板特征参数 ψ_{JB} 估算器件在实际系统中的结温，可通过 JESD51-2a (第 6 节和第 7 节) 介绍的步骤从获得 $R_{\theta JA}$ 的仿真数据中获取该温度。
- (9) 通过在外露 (电源) 焊盘上进行冷板测试仿真来获得结至芯片外壳 (底部) 热阻。不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。

5.6 电气特性

在工作温度范围 ($T_J = -40^{\circ}\text{C}$ 至 125°C)、 $V_{IN} = V_{OUT(nom)} + 0.5V^{(1)}$ 、 $I_{OUT} = 10\text{mA}$ 、 $V_{EN} = 1.7V$ 且 $C_{OUT} = 0.1\mu\text{F}$ 条件下 (除非另有说明)。典型值为 $T_J = 25^{\circ}\text{C}$ 条件下的值。

参数		测试条件		最小值	典型值	最大值	单位
V_{IN}	输入电压范围 ^{(1) (2)}			1.7		5.5	V
V_{FB}	内部基准 (TPS73601)	$T_J = 25^{\circ}\text{C}$		1.198	1.204	1.210	V
V_{OUT}	输出电压范围 (TPS73601) ⁽³⁾			V_{FB}		5.5 - V_{DO}	V
	准确度 ^{(1) (4)}	标称值	$T_J = 25^{\circ}\text{C}$	-0.5		0.5	%
		在 V_{IN} 、 I_{OUT} 且 T 条件下		-1	± 0.5	1	
$\Delta V_{OUT(\Delta V_{IN})}$	线性调整率 ⁽¹⁾	$V_{OUT(nom)} + 0.5V \leq V_{IN} \leq 5.5V$			0.01		%/V
$\Delta V_{OUT(\Delta I_{OUT})}$	负载调整率	$1\text{mA} \leq I_{OUT} \leq 400\text{mA}$			0.002		%/mA
		$10\text{mA} \leq I_{OUT} \leq 400\text{mA}$			0.0005		
V_{DO}	压降电压 ⁽⁵⁾ ($V_{IN} = V_{OUT(nom)} - 0.1V$)	$I_{OUT} = 400\text{mA}$			75	200	mV
$Z_{O(DO)}$	压降中的输出阻抗	$1.7V \leq V_{IN} \leq V_{OUT} + V_{DO}$			0.25		Ω
I_{CL}	输出电流限制	$V_{OUT} = 0.9 \times V_{OUT(nom)}$	传统器件	400	650	800	mA
		$3.6V \leq V_{IN} \leq 4.2V$, $0^{\circ}\text{C} \leq T_J \leq 70^{\circ}\text{C}$		500		800	
		$V_{OUT} = 0.9 \times V_{OUT(nom)}$	新器件	500		800	
I_{SC}	短路电流	$V_{OUT} = 0V$			450		mA
I_{REV}	反向漏电流 ⁽⁶⁾ ($-I_{IN}$)	$V_{EN} \leq 0.5V$, $0V \leq V_{IN} \leq V_{OUT}$			0.1	10	μA
I_{GND}	接地引脚电流	$I_{OUT} = 10\text{mA}$ (I_Q)			400	550	μA
I_{GND}	接地引脚电流	$I_{OUT} = 400\text{mA}$			800	1000	μA
I_{SHDN}	关断电流 (I_{GND})	$V_{EN} \leq 0.5V$, $V_{OUT} \leq V_{IN} \leq 5.5V$, $-40^{\circ}\text{C} \leq T_J \leq 100^{\circ}\text{C}$, 传统器件			0.02	1	μA
		$V_{EN} \leq 0.5V$, $V_{OUT} \leq V_{IN} \leq 5.5V$, 新器件			0.02	1	
I_{FB}	反馈引脚电流 (TPS73601)				0.1	0.3	μA
PSRR	电源抑制比 (纹波抑制)	$f = 100\text{Hz}$, $I_{OUT} = 400\text{mA}$			58		dB
		$f = 10\text{kHz}$, $I_{OUT} = 400\text{mA}$			37		
V_N	输出噪声电压, BW = 10Hz 至 100kHz	$C_{OUT} = 10\mu\text{F}$, 无 C_{NR}			27 x V_{OUT}		μV_{RMS}
		$C_{OUT} = 10\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$			8.5 x V_{OUT}		
t_{STR}	启动时间	$V_{OUT} = 3V$, $R_L = 30\Omega$, $C_{OUT} = 1\mu\text{F}$, $C_{NR} = 0.01\mu\text{F}$			600		μs
$V_{EN(high)}$	EN 引脚高电平 (已使能)			1.7		V_{IN}	V
$V_{EN(low)}$	EN 引脚低电平 (关断)			0		0.5	V
$I_{EN(high)}$	使能引脚电流 (已使能)	$V_{EN} = 5.5V$			0.02	0.1	μA
T_{SD}	热关断温度	关断, 温度升高			160		$^{\circ}\text{C}$
		复位, 温度降低			140		
T_J	工作结温			-40		125	$^{\circ}\text{C}$

(1) 最小 $V_{IN} = V_{OUT} + V_{DO}$ 或者 $1.7V$, 以较大者为准。

(2) 对于 $V_{OUT(nom)} < 1.6V$, 当 $V_{IN} \leq 1.6V$ 时, 输出锁定到 V_{IN} 并可能导致输出上出现破坏性过压情况。为避免这种情况, 请先禁用器件, 然后再将 V_{IN} 关断。(仅限传统器件)

(3) TPS73601 在 $V_{OUT} = 2.5V$ 条件下进行测试。

(4) 外部电阻器的耐受电压不包括在这个技术规范中。

(5) 针对输出版本, 不在 $V_{OUT(nom)} < 1.8V$ 时测量 V_{DO} ; 这是因为最小 $V_{IN} = 1.7V$ 。

(6) 只适用于固定电压版本; 更多信息请参考应用信息部分。

5.7 Typical Characteristics

For all voltage versions, at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\ \mu\text{F}$, unless otherwise noted.

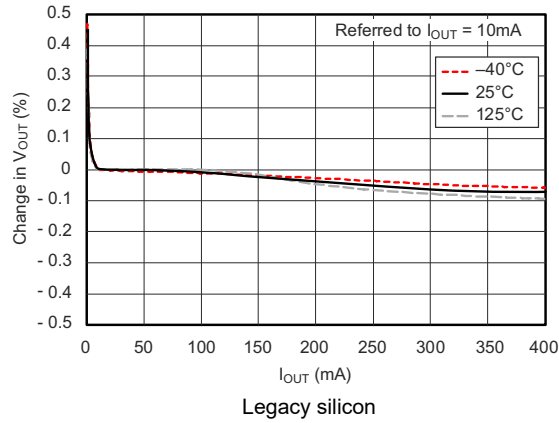


图 5-1. Load Regulation

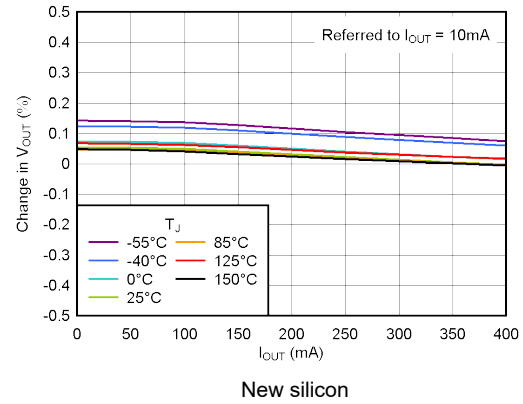


图 5-2. Load Regulation

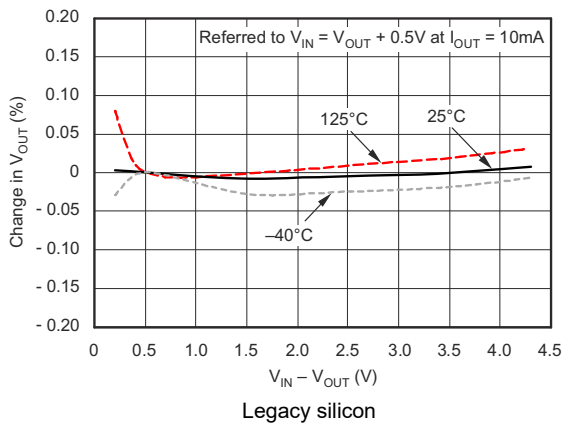


图 5-3. Line Regulation

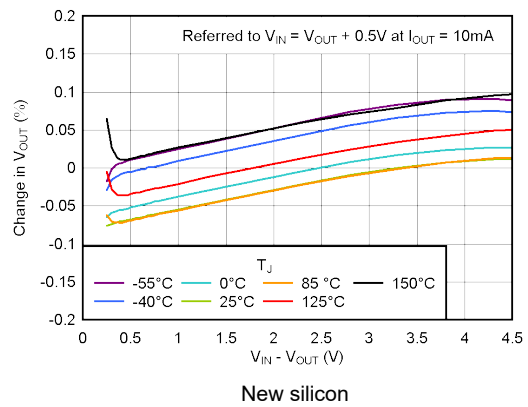


图 5-4. Line Regulation

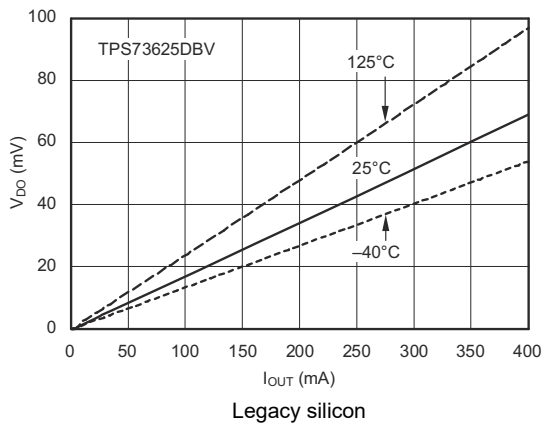


图 5-5. Dropout Voltage vs Output Current

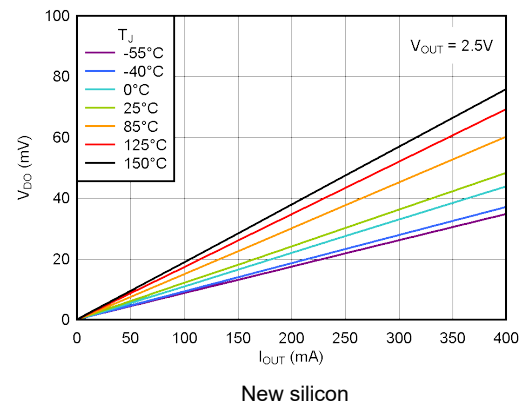


图 5-6. Dropout Voltage vs Output Current

5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\ \mu\text{F}$, unless otherwise noted.

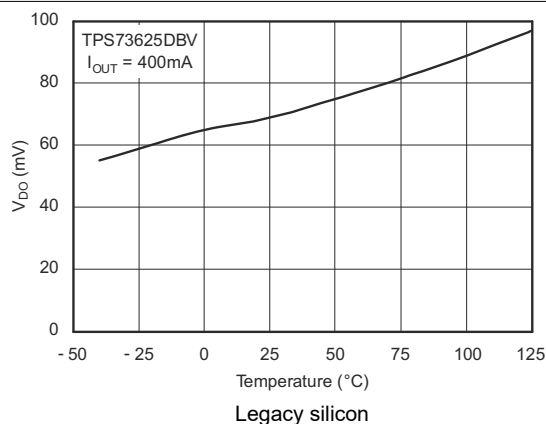


图 5-7. Dropout Voltage vs Temperature

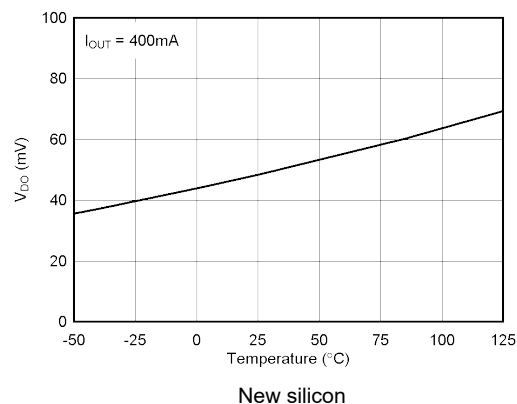


图 5-8. Dropout Voltage vs Temperature

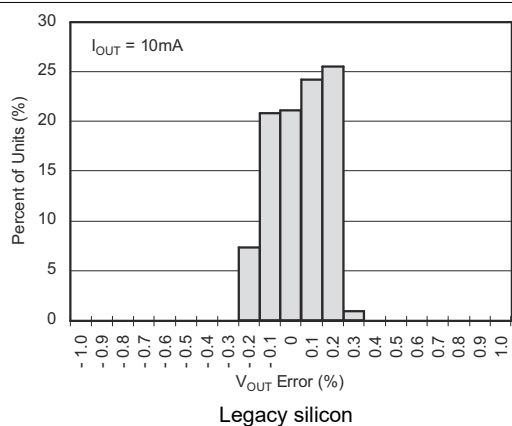


图 5-9. Output Voltage Accuracy Histogram

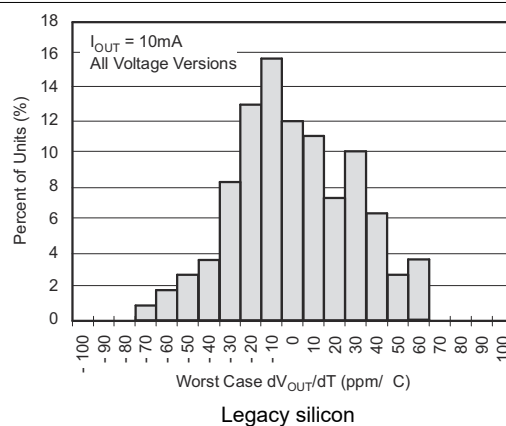


图 5-10. Output Voltage Drift Histogram

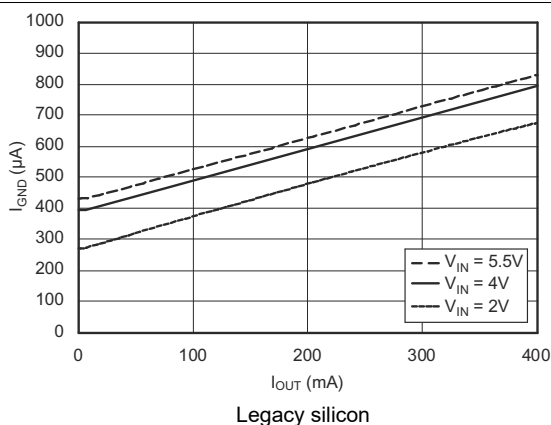


图 5-11. Ground Pin Current vs Output Current

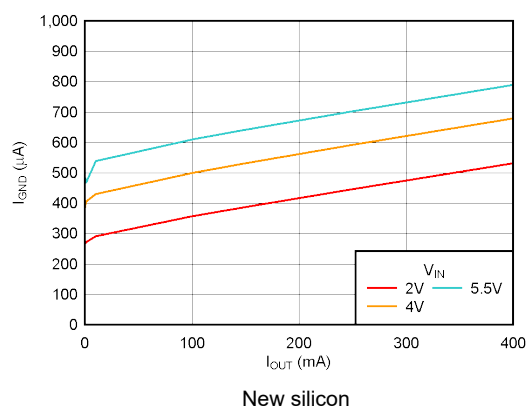


图 5-12. Ground Pin Current vs Output Current

5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\ \mu\text{F}$, unless otherwise noted.

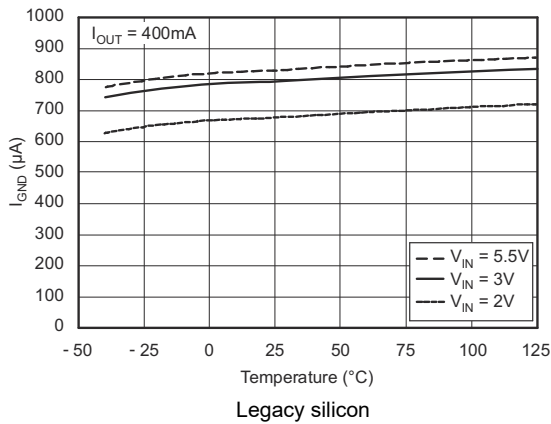


图 5-13. Ground Pin Current vs Temperature

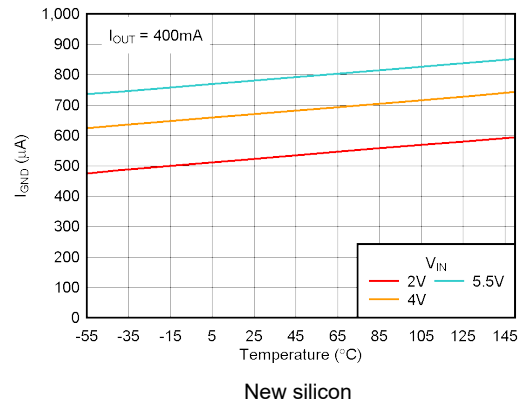


图 5-14. Ground Pin Current vs Temperature

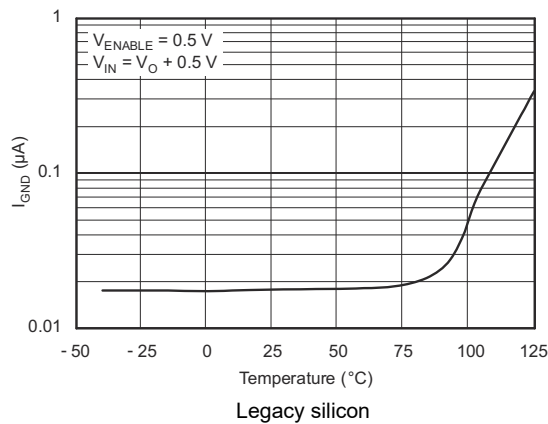


图 5-15. Ground Pin Current in Shutdown vs Temperature

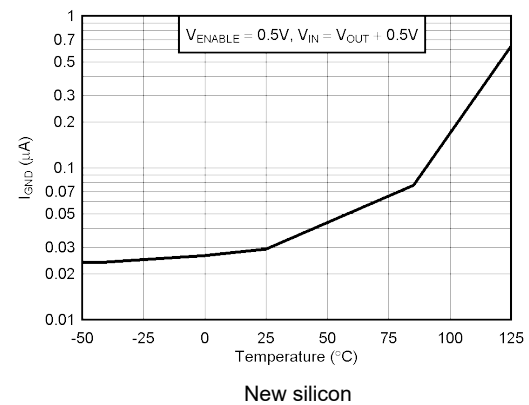


图 5-16. Ground Pin Current in Shutdown vs Temperature

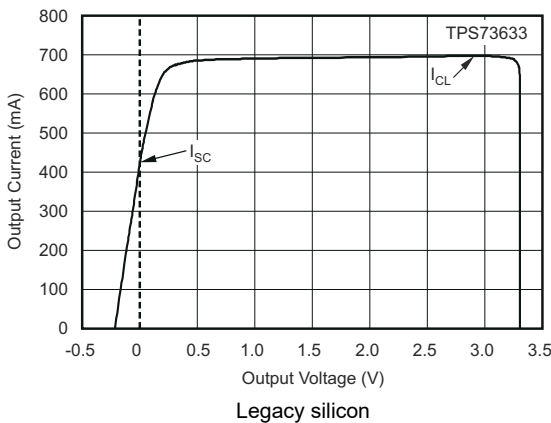


图 5-17. Current Limit vs V_{OUT} (Foldback)

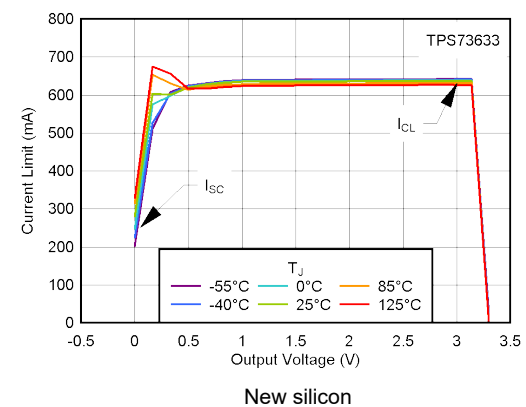


图 5-18. Current Limit vs V_{OUT} (Foldback)

5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\ \mu\text{F}$, unless otherwise noted.

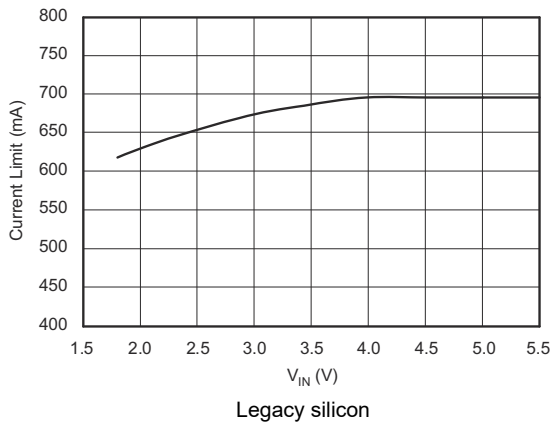


图 5-19. Current Limit vs V_{IN}

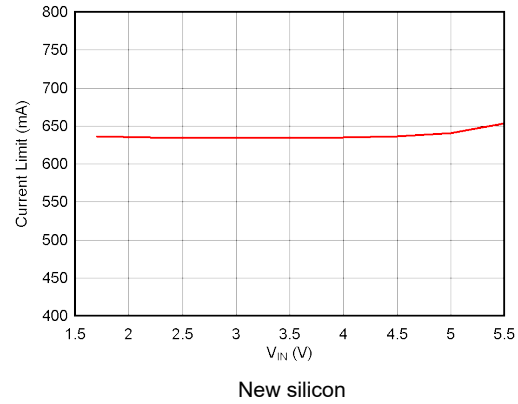


图 5-20. Current Limit vs V_{IN}

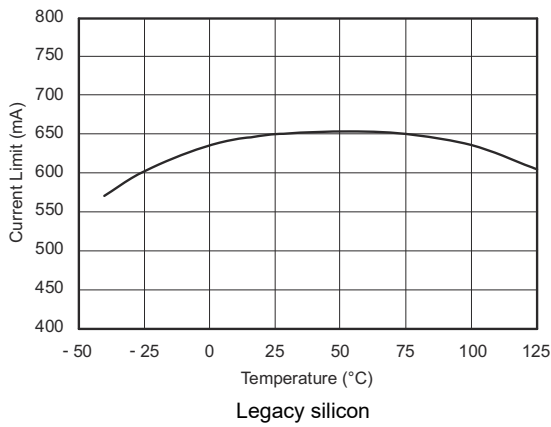


图 5-21. Current Limit vs Temperature

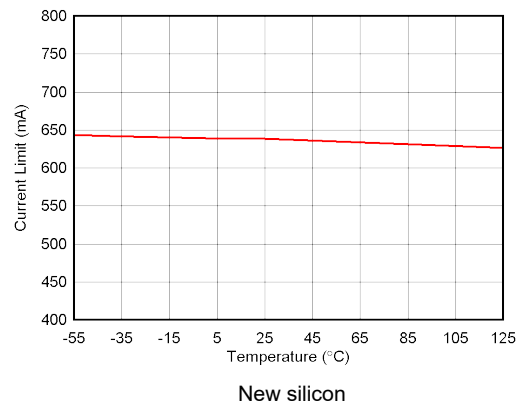


图 5-22. Current Limit vs Temperature

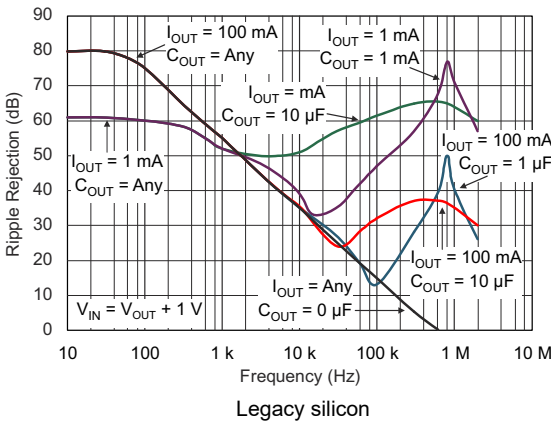


图 5-23. PSRR (Ripple Rejection) vs Frequency

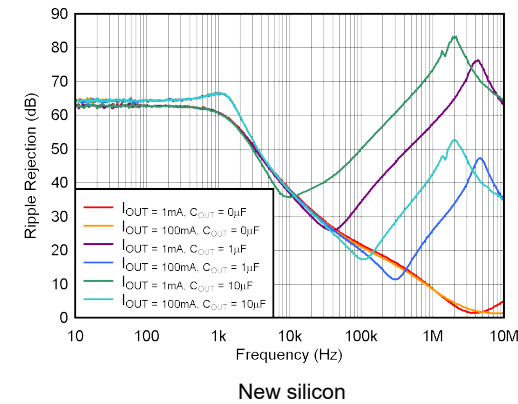


图 5-24. PSRR (Ripple Rejection) vs Frequency

5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$, unless otherwise noted.

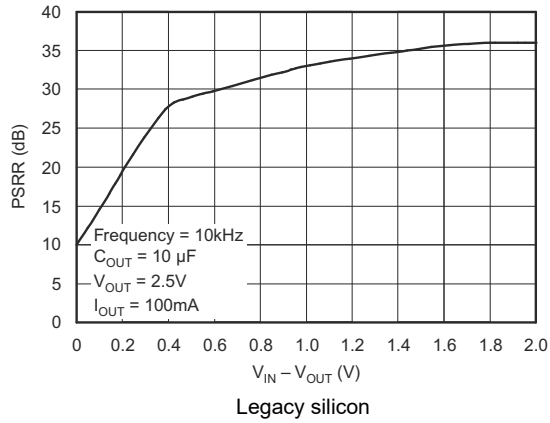


图 5-25. PSRR (Ripple Rejection) vs $V_{IN} - V_{OUT}$

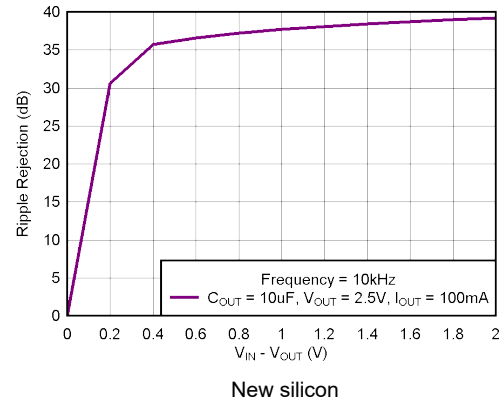


图 5-26. PSRR (Ripple Rejection) vs $V_{IN} - V_{OUT}$

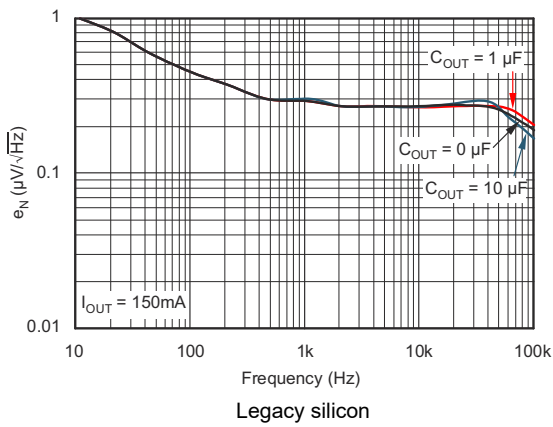


图 5-27. Noise Spectral Density $C_{NR} = 0\text{ }\mu\text{F}$

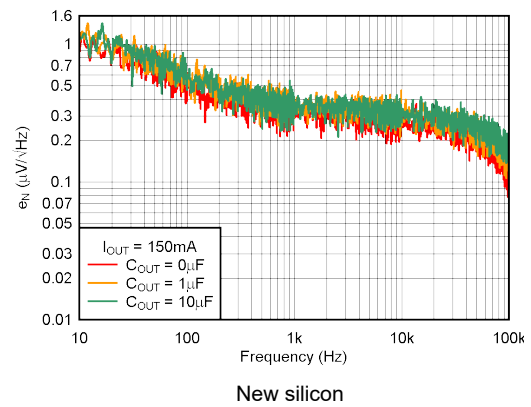


图 5-28. Noise Spectral Density $C_{NR} = 0\text{ }\mu\text{F}$

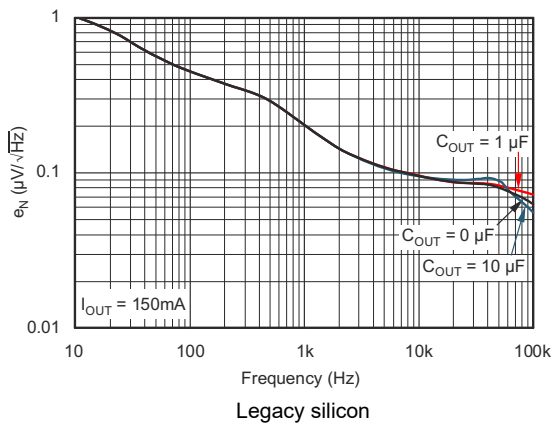


图 5-29. Noise Spectral Density $C_{NR} = 0.01\text{ }\mu\text{F}$

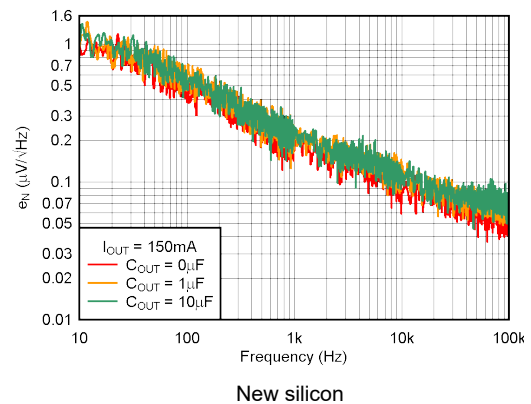


图 5-30. Noise Spectral Density $C_{NR} = 0.01\text{ }\mu\text{F}$

5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\ \mu\text{F}$, unless otherwise noted.

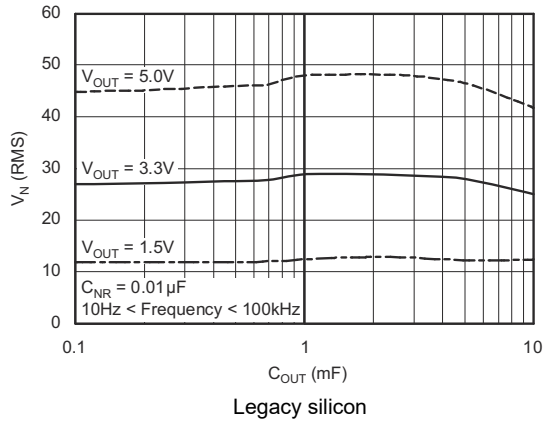
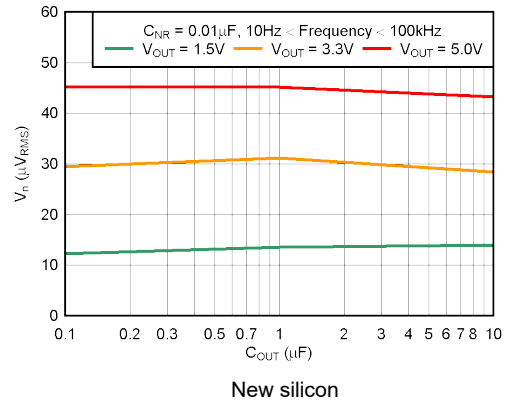
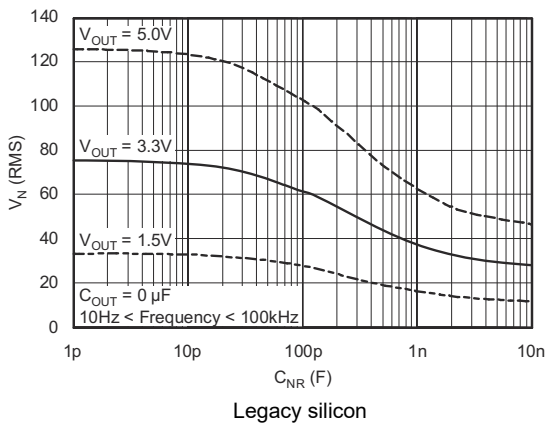
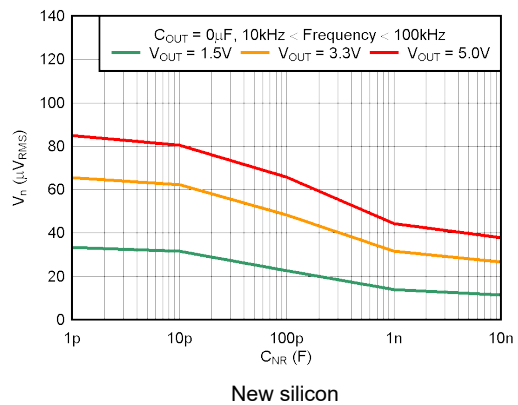
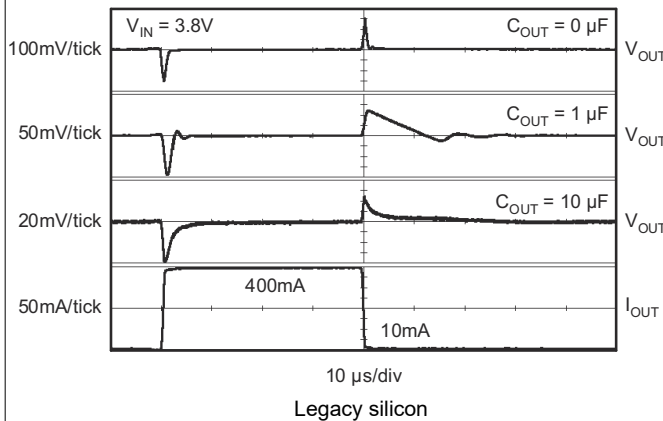
图 5-31. RMS Noise Voltage vs C_{OUT} 图 5-32. RMS Noise Voltage vs C_{OUT} 图 5-33. RMS Noise Voltage vs C_{NR} 图 5-34. RMS Noise Voltage vs C_{NR} 

图 5-35. TPS73633 Load Transient Response

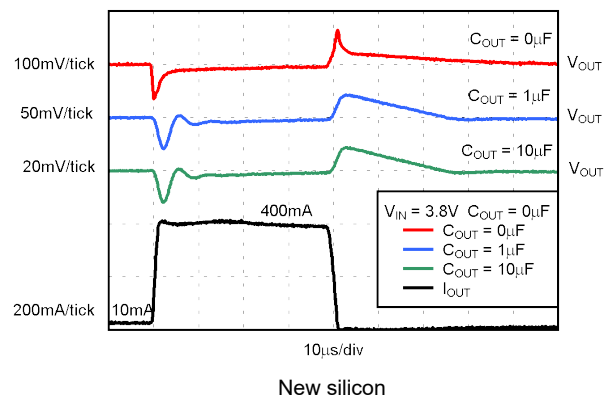


图 5-36. TPS73633 Load Transient Response

5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$, unless otherwise noted.

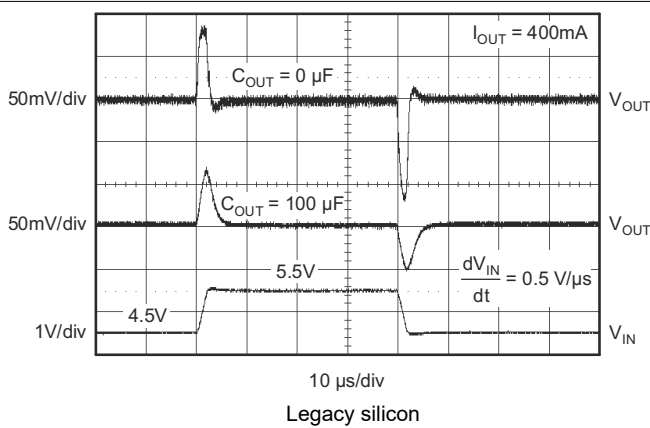


图 5-37. TPS73633 Line Transient Response

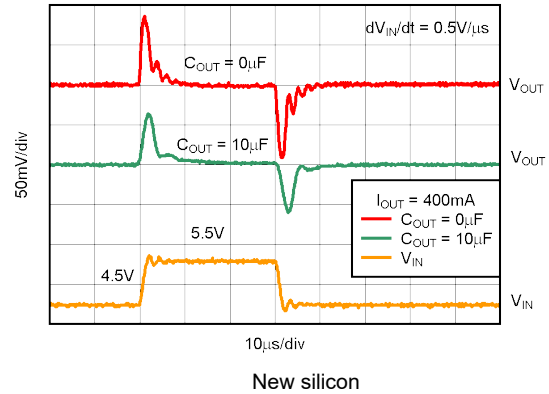


图 5-38. TPS73633 Line Transient Response

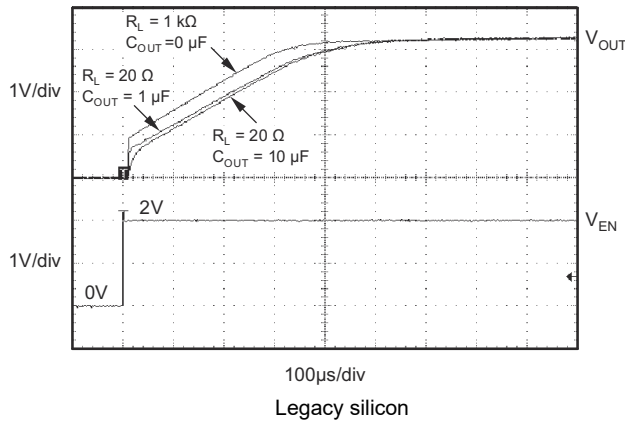


图 5-39. TPS73633 Turn-On Response

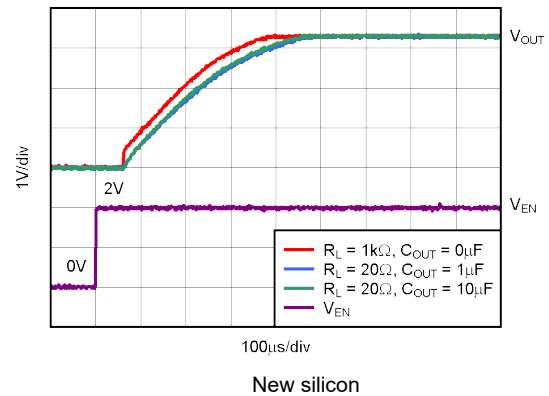


图 5-40. TPS73633 Turn-On Response

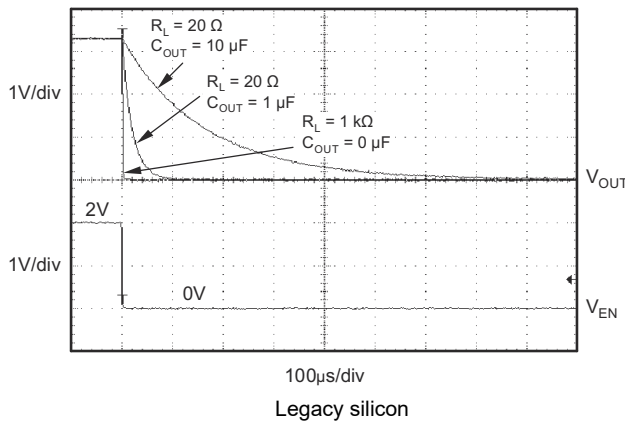


图 5-41. TPS73633 Turn-Off Response

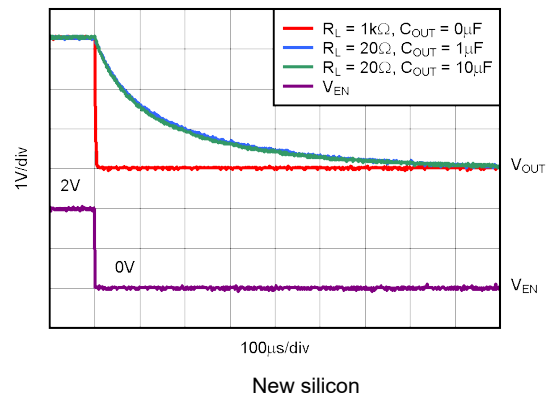


图 5-42. TPS73633 Turn-Off Response

5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\ \mu\text{F}$, unless otherwise noted.

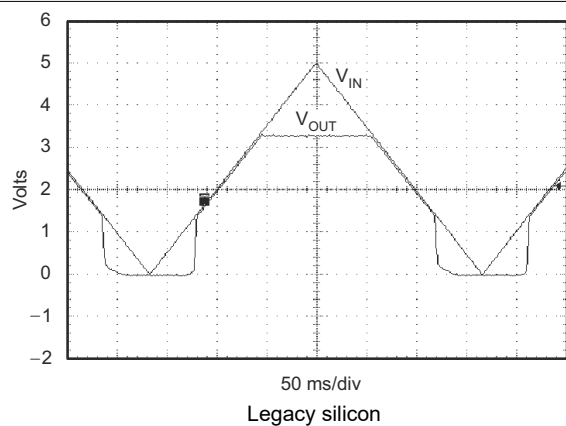


图 5-43. TPS73633 Power-Up, Power-Down

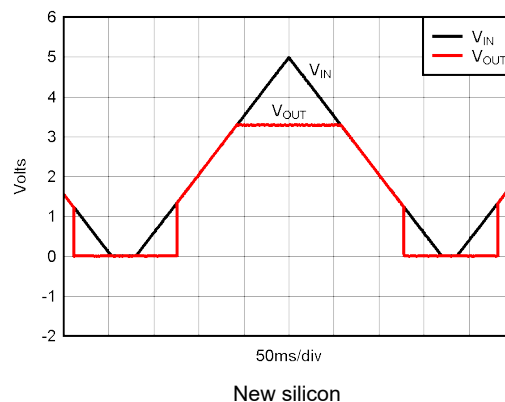


图 5-44. TPS73633 Power-Up, Power-Down

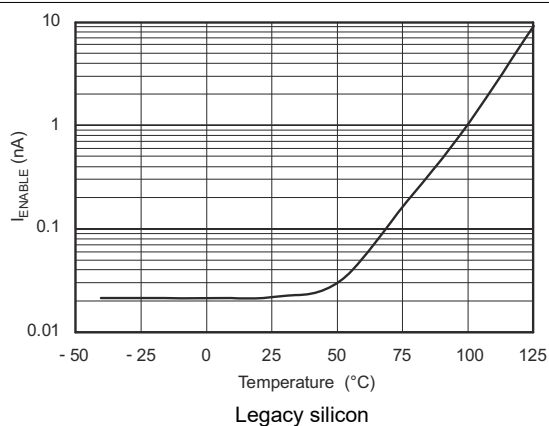


图 5-45. I_{ENABLE} vs Temperature

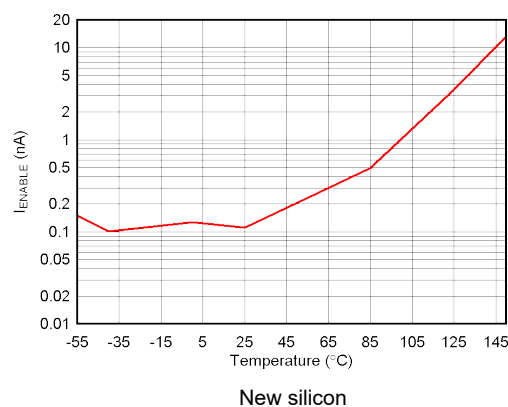


图 5-46. I_{ENABLE} vs Temperature

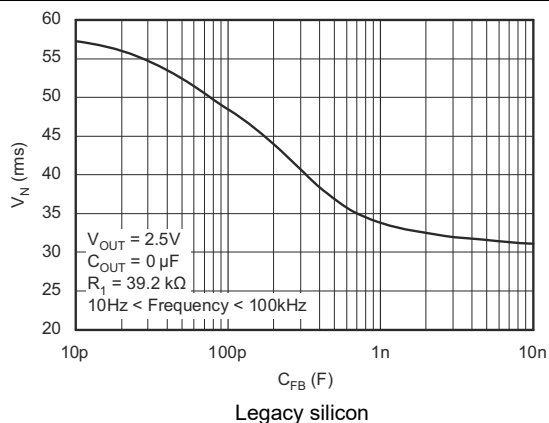


图 5-47. TPS73601 RMS Noise Voltage vs C_{FB}

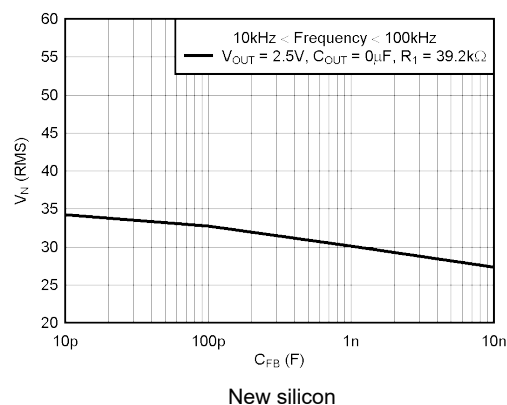


图 5-48. TPS73601 RMS Noise Voltage vs C_{FB}

5.7 Typical Characteristics (continued)

For all voltage versions, at $T_J = 25^\circ\text{C}$, $V_{IN} = V_{OUT(nom)} + 0.5\text{V}$, $I_{OUT} = 10\text{mA}$, $V_{EN} = 1.7\text{V}$, and $C_{OUT} = 0.1\text{ }\mu\text{F}$, unless otherwise noted.

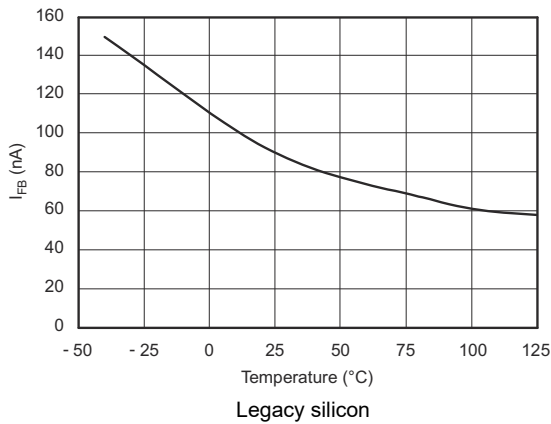


图 5-49. TPS73601 I_{FB} vs Temperature

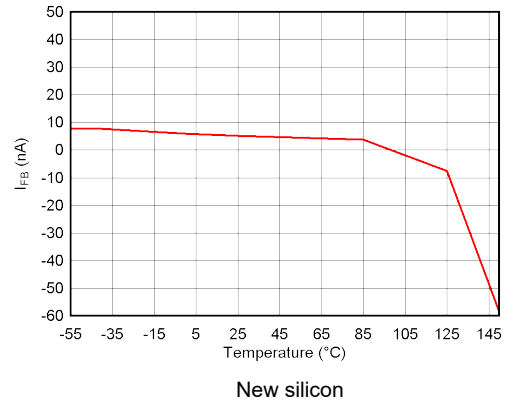


图 5-50. TPS73601 I_{FB} vs Temperature

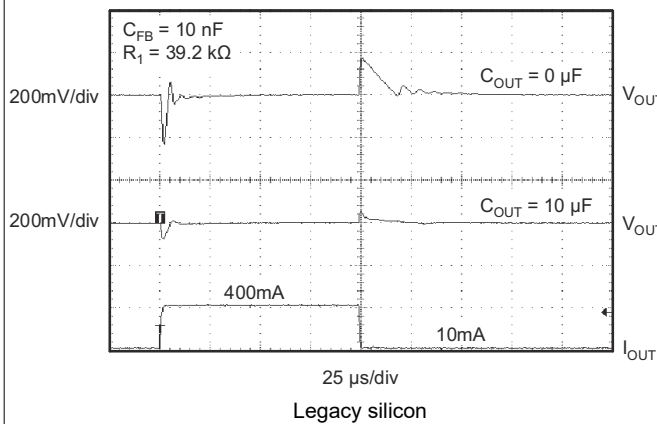


图 5-51. TPS73601 Load Transient, Adjustable Version

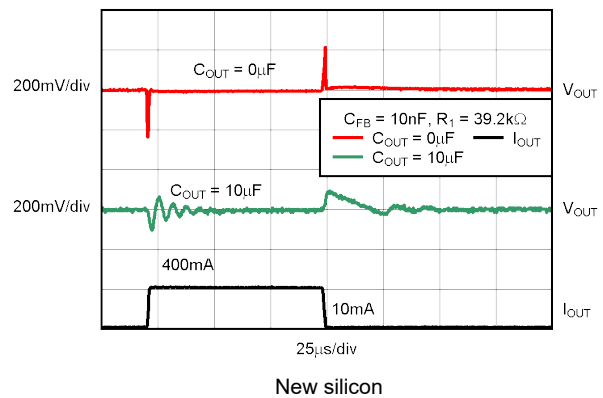


图 5-52. TPS73601 Load Transient, Adjustable Version

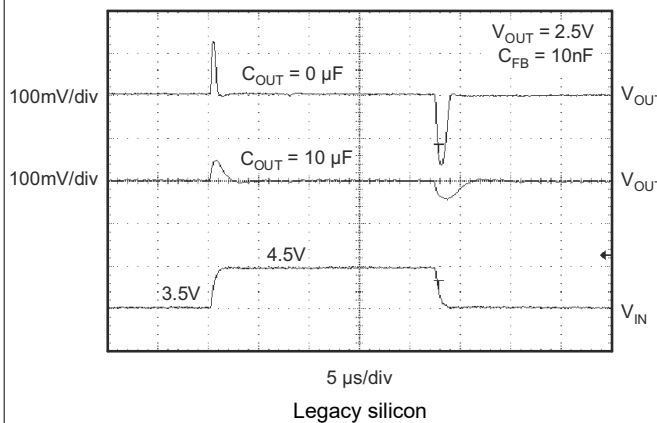


图 5-53. TPS73601 Line Transient, Adjustable Version

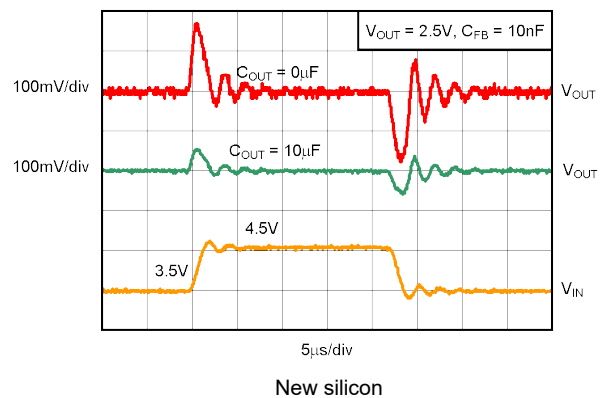


图 5-54. TPS73601 Line Transient, Adjustable Version

6 Detailed Description

6.1 Overview

The TPS736 low-dropout linear regulator operates down to an input voltage of 1.7 V and supports output voltages down to 1.2 V while sourcing up to 400 mA of load current. This linear regulator uses an NMOS pass transistor with an integrated 4-MHz charge pump to provide a dropout voltage of less than 200 mV at full load current. This unique architecture also permits stable regulation over a wide range of output capacitors. In fact, the TPS736 device does not require any output capacitor for stability. The increased insensitivity to the output capacitor value and type makes this linear regulator an ideal choice when powering a load where the effective capacitance is unknown.

The TPS736 also features a noise reduction (NR) pin that allows for additional reduction of the output noise. With a noise reduction capacitor of 0.01 μF connected from the NR pin to GND, the TPS73615 output noise can be as low as 12.75 μV_{RMS} . The low noise output featured by the TPS736 makes the device well-suited for powering VCOs or any other noise sensitive load.

6.2 Functional Block Diagrams

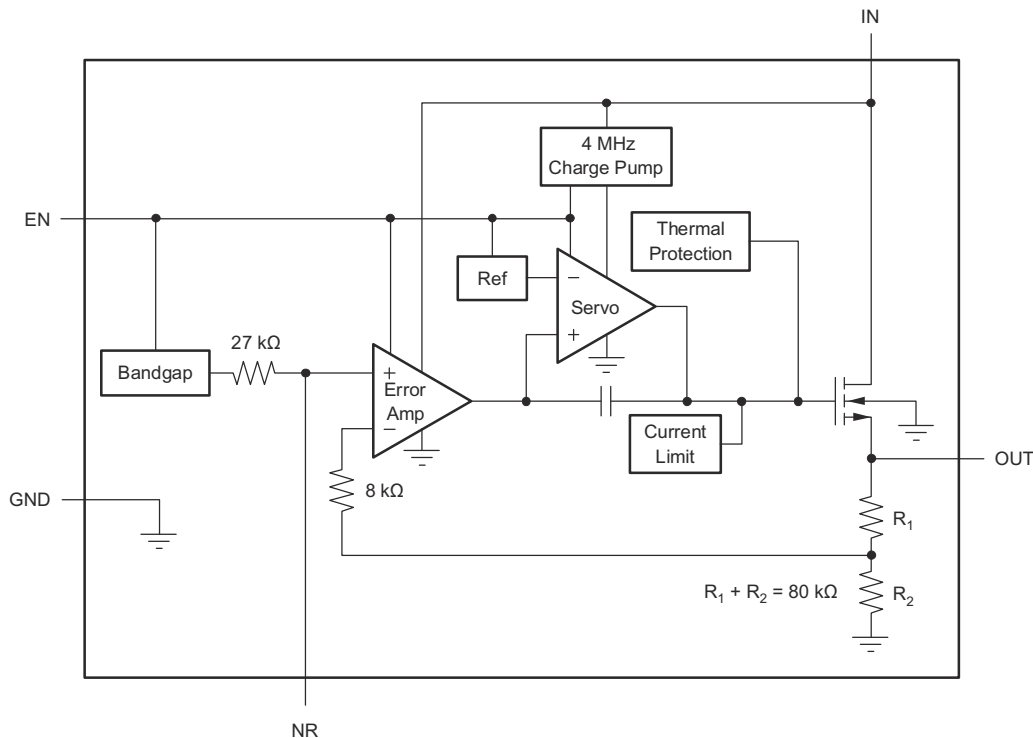
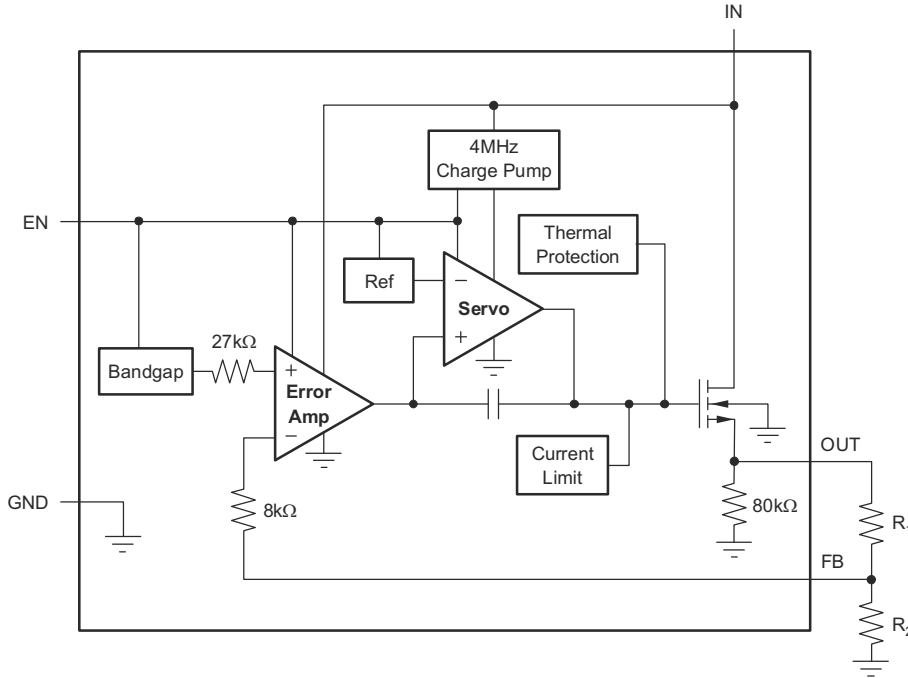


图 6-1. Fixed-Voltage Version



**Standard 1%
Resistor Values for
Common Output Voltages**

V _O	R ₁	R ₂
1.2V	Short	Open
1.5V	23.2kΩ	95.3kΩ
1.8V	28.0kΩ	56.2kΩ
2.5V	39.2kΩ	36.5kΩ
2.8V	44.2kΩ	33.2kΩ
3.0V	46.4kΩ	30.9kΩ
3.3V	52.3kΩ	30.1kΩ

NOTE: $V_{OUT} = (R_1 + R_2)/R_2 \times 1.204$;
 $R_1 || R_2 \cong 19k\Omega$ for best
accuracy.

图 6-2. Adjustable-Voltage Version

6.3 Feature Description

6.3.1 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF} . This reference is the dominant noise source within the TPS736 and generates approximately $32 \mu V_{RMS}$ (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Since the value of V_{REF} is 1.2 V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT}(V) \quad (2)$$

for the case of no C_{NR} .

An internal 27-kΩ resistor in series with the noise-reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise-reduction capacitor, C_{NR} , is connected from NR to ground. For $C_{NR} = 10$ nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT}(V) \quad (3)$$

for $C_{NR} = 10$ nF.

This noise reduction effect is shown as *RMS Noise Voltage vs C_{NR}* in the [Typical Characteristics](#) section.

The TPS73601 adjustable version does not have the NR pin available. However, connecting a feedback capacitor, C_{FB} , from the output to the feedback pin (FB) reduces output noise and improves load transient performance.

The TPS736 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass transistor above V_{OUT} . The charge pump generates approximately 250 μ V of switching noise at approximately 4 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT} .

6.3.2 Internal Current Limit

The TPS736 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See [图 5-17](#) in the [Typical Characteristics](#) section.

Note from [图 5-17](#) that approximately -0.2 V of V_{OUT} results in a current limit of 0 mA. Therefore, if OUT is forced below -0.2 V before EN goes high, the device may not start up. In applications that work with both a positive and negative voltage supply, the TPS736 should be enabled first.

6.3.3 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. V_{EN} below 0.5V (max) turns the regulator off and drops the GND pin current to approximately 10nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate. A V_{EN} above 1.7V (minimum) turns the regulator on and the output ramps back up to a regulated V_{OUT} (see [图 5-40](#)).

When shutdown capability is not required, connect EN to V_{IN} . However, the pass transistor may not be discharged using this configuration, and the pass transistor may be left on (enhanced) for a significant time after V_{IN} has been removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power-up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output may overshoot upon power-up.

Current limit foldback can prevent device start-up under some conditions. See the [Internal Current Limit](#) section for more information.

6.3.4 Reverse Current

The NMOS pass transistor of the TPS736 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass transistor is pulled low. To ensure that all charge is removed from the gate of the pass transistor, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass transistor may be left on due to stored charge on the gate.

After the EN pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There is additional current flowing into the OUT pin due to the 80-k Ω internal resistor divider to ground (see [图 6-1](#) and [图 6-2](#)).

For the TPS73601, reverse current may flow when V_{FB} is more than 1.0 V above V_{IN} .

6.4 Device Functional Modes

6.4.1 Normal Operation with $1.7\text{ V} \leq V_{IN} \leq 5.5\text{ V}$ and $V_{EN} \geq 1.7\text{ V}$

The TPS736 requires an input voltage of at least 1.7 V to function properly and attempt to maintain regulation. If the device output voltage is greater than 1.5 V when the input voltage is at 1.7 V, the device is operating in dropout and regulation cannot be maintained. Because of the NMOS architecture used in the TPS736, the dropout voltage is not a strong function of the input voltage.

When operating the device near 5.5 V, take care to suppress any transient spikes that may exceed the 6.0-V absolute maximum voltage rating. The device should never operate at a dc voltage greater than 5.5 V.

7 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

7.1 Application Information

The TPS736 is an LDO regulator that uses an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS736 ideal for portable applications. This regulator offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

7.2 Typical Application

图 7-1 shows the basic circuit connections for the fixed voltage models. 图 7-2 gives the connections for the adjustable output version (TPS73601).

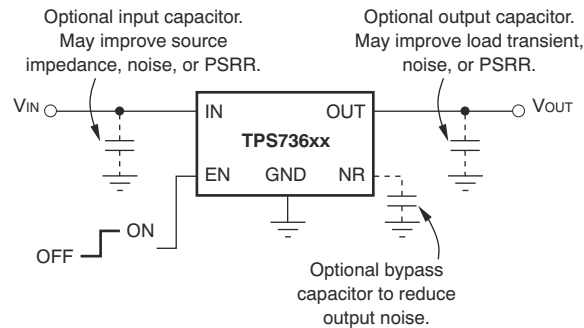


图 7-1. Typical Application Circuit for Fixed-Voltage Versions

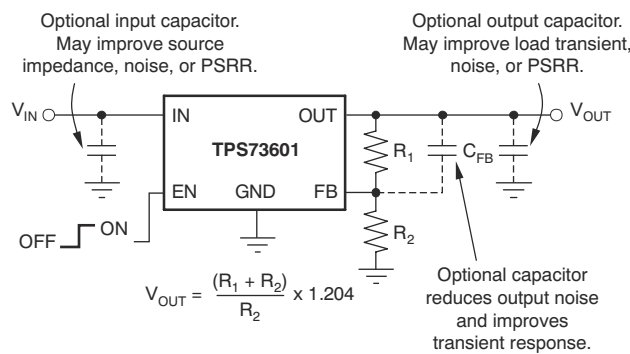


图 7-2. Typical Application Circuit for Adjustable-Voltage Version

7.2.1 Design Requirements

For this design example, use the parameters listed below as the input parameters.

表 7-1. Design Parameters (Fixed-Voltage Version)

PARAMETER	DESIGN REQUIREMENT
Input voltage	5 V, $\pm 3\%$
Output voltage	3.3 V, $\pm 1\%$
Output current	400 mA (maximum), 20 mA (minimum)
RMS noise, 10 Hz to 100 kHz	$< 30 \mu V_{RMS}$
Ambient temperature	55°C (maximum)

表 7-2. Design Parameters (Adjustable-Voltage Version)

PARAMETER	DESIGN REQUIREMENT
Input voltage	5 V, $\pm 3\%$, provided by the dc/dc converter switching at 1 MHz
Output voltage	2.5 V, $\pm 1\%$
Output current	0.4 A (maximum), 10 mA (minimum)
RMS noise, 10 Hz to 100 kHz	$< 35 \mu V_{RMS}$
Ambient temperature	55°C (maximum)

7.2.2 Detailed Design Procedure

The first step when designing with a linear regulator is to examine the maximum load current along with the input and output voltage requirements to determine if the device thermal and dropout voltage requirements can be met. At 0.4 A, the dropout voltage of the TPS73633 is a maximum of 200 mV over temperature; thus, the dropout headroom is sufficient for operation over both input and output voltage accuracy.

The maximum power dissipated in the linear regulator is the maximum voltage dropped across the pass transistor from the input to the output times the maximum load current. In this example, the maximum voltage drop across in the pass transistor is 5 V + 3% (5.15 V) minus 3.3 V – 1% (3.267 V) or 1.883 V. The power dissipated in the pass transistor is calculated by taking this voltage drop multiplied by the maximum load current. For this example, the maximum power dissipated in the linear regulator is 942 mW. Once the power dissipated in the linear regulator is known, the corresponding junction temperature rise can be calculated. To calculate the junction temperature rise above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. For thermal resistance information see the [Thermal Protection](#) section. For this example, using the DRB package, the maximum junction temperature rise is calculated to be 45°C. The maximum junction temperature rise is calculated by adding junction temperature rise to the maximum ambient temperature. In this example, the maximum junction temperature is 100°C. Keep in mind the maximum junction temperature must be below 125°C for reliable operation. Addition ground planes, added thermal vias, and air flow all help to lower the maximum junction temperature. Using the DCQ or DBV packages are not recommended for this application due to the excessive junction temperature rise that would be incurred.

To get the noise level below 30 μV_{RMS} , a noise reduction capacitance (C_{NR}) of 10 nF is selected along with an output capacitance of 10 μF . Referencing the [Output Noise](#) section, the RMS noise can be calculated to be 28 μV_{RMS} .

Use of an input capacitor is optional. However, in systems where the input supply is located several inches away from the LDO, a small 0.1- μF input capacitor is recommended to negate the adverse effects that input supply inductance has on stability and ac performance.

In the same way as with designing with a fixed output voltage, the first step is to examine the maximum load current along with the input and output voltage requirements to determine if the device thermal and dropout voltage requirements are met. At 0.4 A, the maximum dropout voltage is 200 mV. Since the input voltage is 5 V and the output voltage is 2.5 V, there is more than sufficient voltage headroom to avoid dropout and maintain good PSRR.

The maximum power dissipated in the linear regulator is the maximum voltage dropped across the pass transistor from the input to the output times the maximum load current. In this example, the maximum voltage drop across in the pass transistor is $5\text{ V} + 3\%$ (5.15 V) minus $2.5\text{ V} - 1\%$ (2.475 V) or 2.675 V. The power dissipated in the pass transistor is calculated by taking this voltage drop multiplied by the maximum load current. For this example, the maximum power dissipated in the linear regulator is 1.07 W. Once the power dissipated in the linear regulator is known, the corresponding junction temperature rise can be calculated. To calculate the junction temperature rise above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. For thermal resistance information, see the [热性能信息](#) table. For this example, using the DRB package, the maximum junction temperature rise is calculated to be 51°C. The maximum junction temperature rise is calculated by adding junction temperature rise to the maximum ambient temperature. In this example, the maximum junction temperature is 106°C. Keep in mind the maximum junction temperature must be below 125°C for reliable operation. Addition ground planes, added thermal vias, and air flow all help to lower the maximum junction temperature. Using the DCQ or DBV packages are not recommended for this application due to the excessive junction temperature rise that would be incurred.

R_1 and R_2 can be calculated for any output voltage using the formula shown in [图 7-2](#). Sample resistor values for common output voltages are shown in [图 6-2](#).

For best accuracy, make the parallel combination of R_1 and R_2 approximately equal to 19 k Ω . This 19 k Ω , in addition to the internal 8-k Ω resistor, presents the same impedance to the error amp as the 27-k Ω bandgap reference output. This impedance helps compensate for leakages into the error amp terminals.

Using the values in [图 6-2](#) for a 2.5-V output results in a value of 39.2 k Ω for R_1 and 36.5 k Ω for R_2 .

To get the noise level below 35 μV_{RMS} , a noise reduction capacitance (C_{FF}) of 10 nF is selected. [图 5-47](#) should be used as a reference when selecting optimal value for C_{FF} .

A 10- μF , low equivalent series resistance (ESR) ceramic X5R capacitor was used on the output of this design to minimize the output voltage droop during a low transient. Use of an input capacitor is optional. However, in systems where the input supply is located several inches away from the LDO, a small 0.1- μF input capacitor is recommended to negate the adverse effects that input supply inductance has on stability and ac performance. See the [Input and Output Capacitor Requirements](#) section for additional information about input and output capacitor selection.

7.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1- μF to 1- μF , low ESR capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS736 does not require an output capacitor for stability and has maximum phase margin with no capacitor. The device is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50 n ΩF . Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

7.2.2.2 Dropout Voltage

The TPS736 uses an NMOS pass transistor to achieve extremely low dropout. When $(V_{IN} - V_{OUT})$ is less than the dropout voltage (V_{DO}), the NMOS pass transistor is in the linear region of operation and the input-to-output resistance is the $R_{DS(on)}$ of the NMOS pass transistor.

For large step changes in load current, the TPS736 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of $V_{IN} - V_{OUT}$ above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with $(V_{IN} - V_{OUT})$ close to dc dropout levels], the TPS736 can take a couple of hundred microseconds to return to the specified regulation accuracy.

7.2.2.3 Transient Response

The low open-loop output impedance provided by the NMOS pass transistor in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1 μ F) from the OUT pin to ground reduces undershoot magnitude but increases the duration. In the adjustable version, the addition of a capacitor, C_{FB} , from the OUT pin to the FB pin also improves the transient response.

The TPS736 does not have active pull-down when the output is over-voltage. This feature allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This feature also results in an output overshoot of several percent if load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal/external load resistance. The rate of decay is given by:

Fixed voltage version

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80 \text{ k}\Omega \parallel R_{LOAD}} \quad (4)$$

Adjustable voltage version

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80 \text{ k}\Omega \parallel (R_1 + R_2) \parallel R_{LOAD}} \quad (5)$$

7.2.3 Application Curves

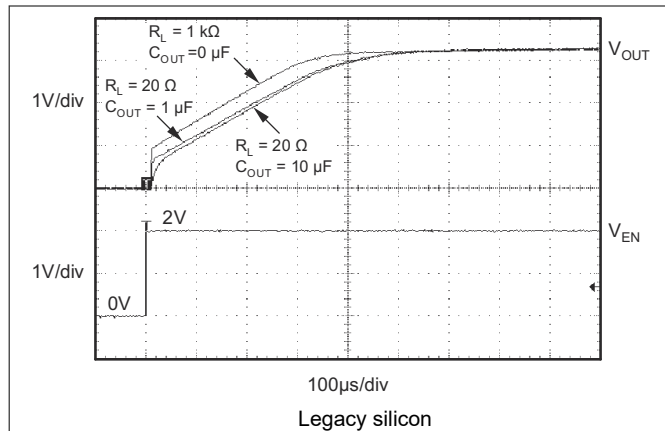


图 7-3. TPS73633 Turn-On Response

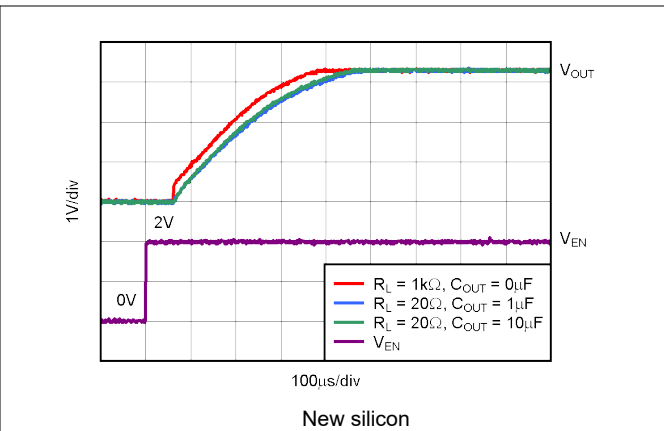


图 7-4. TPS73633 Turn-On Response

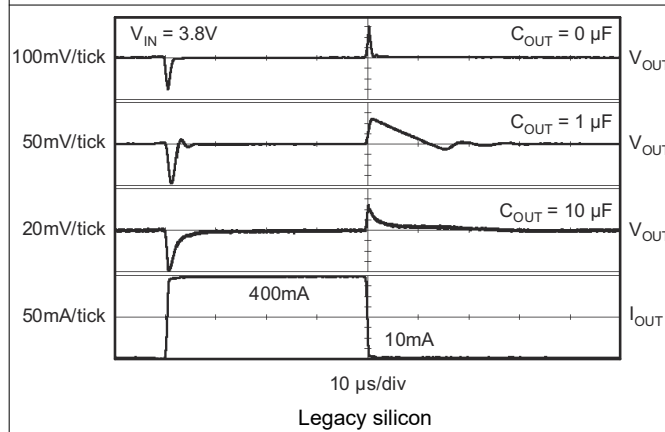


图 7-5. TPS73633 Load Transient Response

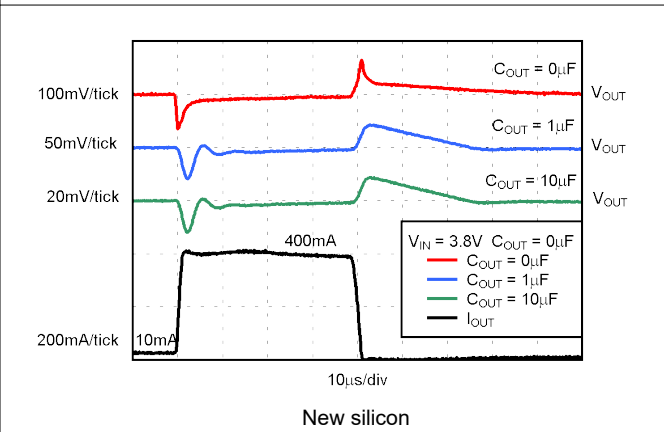


图 7-6. TPS73633 Load Transient Response

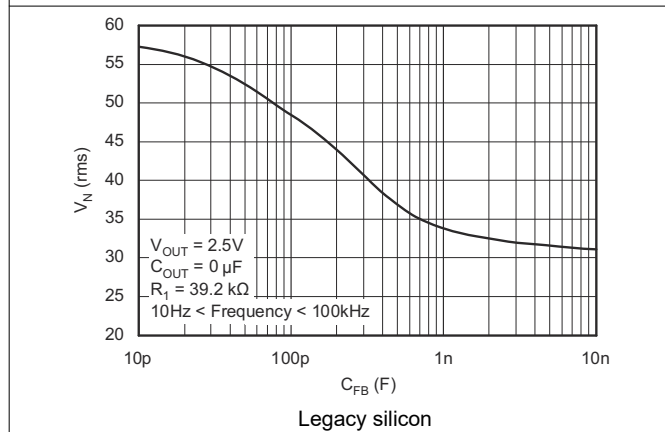


图 7-7. TPS73601 RMS Noise Voltage vs CFB

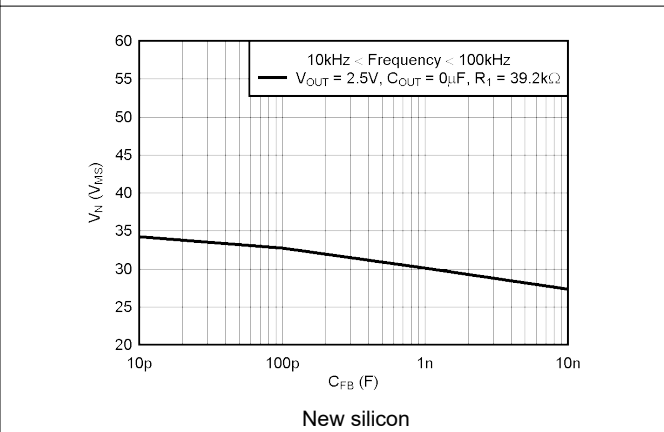
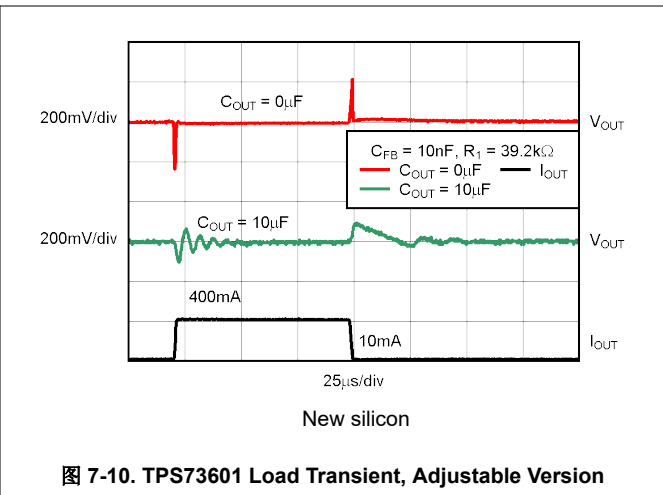
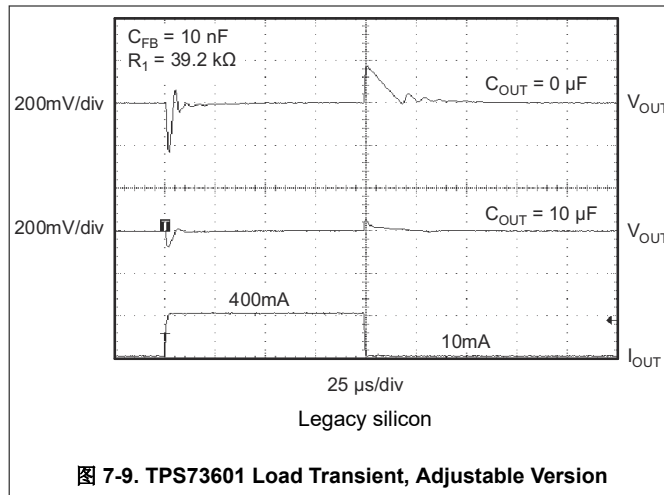


图 7-8. TPS73601 RMS Noise Voltage vs CFB

7.2.3 Application Curves (continued)



7.3 Power Supply Recommendations

This device is designed to operate with an input supply range of 1.7V to 5.5V. If the input supply is noisy, additional input capacitors with low ESR help improve output noise performance.

7.4 Layout

7.4.1 Layout Guidelines

To improve ac performance such as PSRR, output noise, and transient response, design the board with ground plane connections for V_{IN} and V_{OUT} capacitors, and the ground plane connected at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

7.4.1.1 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are shown in the [热性能信息](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass transistor (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

7.4.1.2 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS736 has been designed to protect against overload conditions. This circuitry is not intended to replace proper heat sinking. Continuously running the TPS736 into thermal shutdown degrades device reliability.

7.4.2 Layout Examples

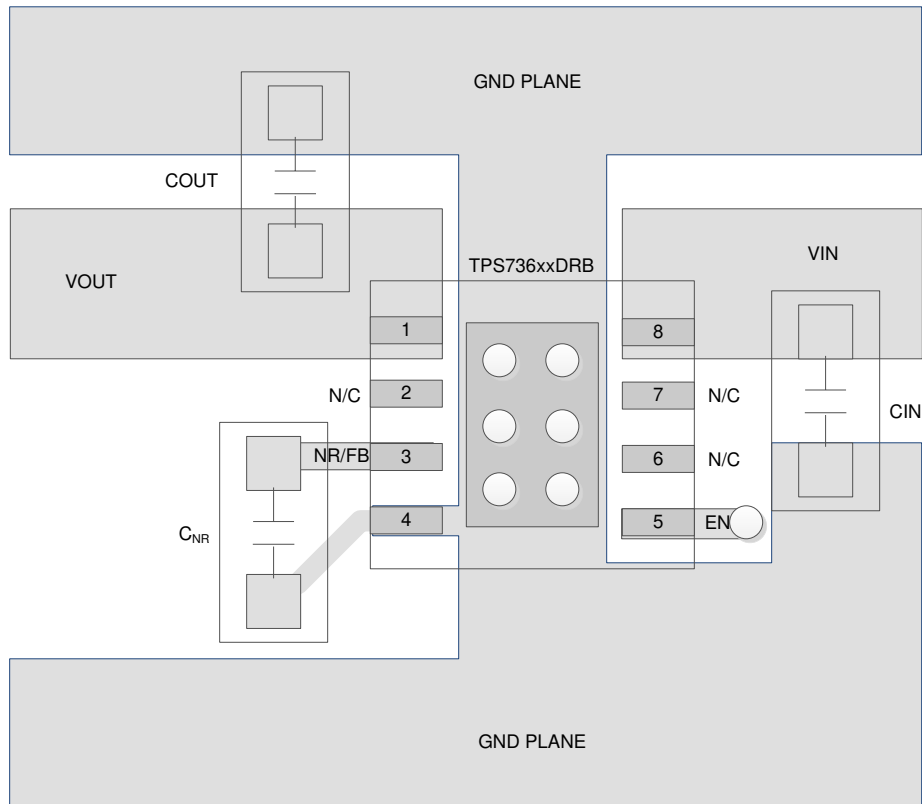


图 7-11. Fixed Output Voltage Option Layout (DRB Package)

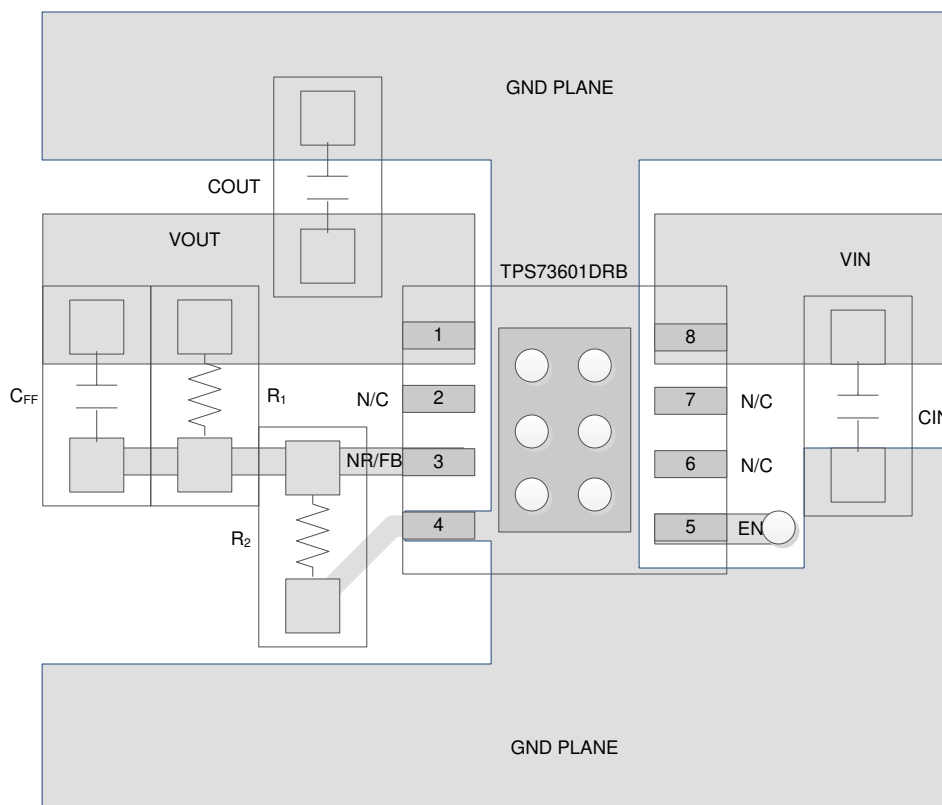


图 7-12. Adjustable Output Voltage Option Layout (DRB Package)

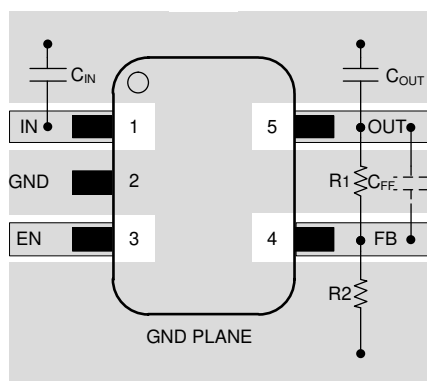


图 7-13. Layout Example for the DBV Package Adjustable Version

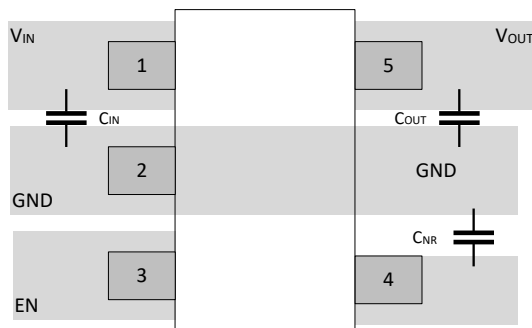


图 7-14. Layout Example for the DBV Package Fixed Version

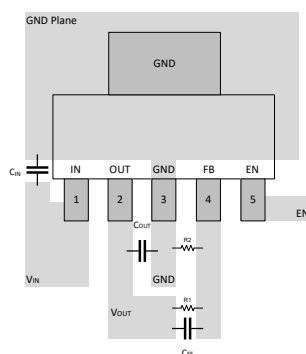


图 7-15. Layout Example for the DCQ Package Adjustable Version

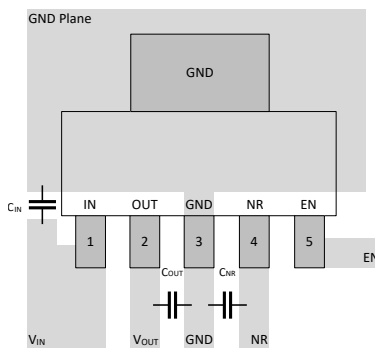


图 7-16. Layout Example for the DCQ Package Fixed Version

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Support

8.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS736. The [TPS73601DRBEVM-518 evaluation module](#) (and [related user guide](#)) can be requested at the Texas Instruments website through the product folders or purchased directly from the [TI eStore](#).

8.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS736 is available through the product folders under *Simulation Models*.

8.1.2 Device Nomenclature

表 8-1. Device Nomenclature

PRODUCT ⁽¹⁾	DESCRIPTION
TPS736xxyyy z(M3)	xx is the nominal output voltage (for example, 25 = 2.5V; 01 = Adjustable). yyy is the package designator. z is the package quantity. M3 is a suffix designator for devices that only use the latest manufacturing flow (CSO: RFB). Devices without this suffix ship with the <i>legacy silicon</i> (CSO: DLN) or the <i>new silicon</i> (CSO: RFB). The reel packaging label provides CSO information to distinguish which silicon is being used. Device performance for new and legacy silicon is denoted throughout the document.

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

8.2 Documentation Support

8.2.1 Related Documentation

For related documentation see the following:

- Texas Instruments, [Regulating \$V_{OUT}\$ Below 1.2 V Using an External Reference application note](#)
- Texas Instruments, [TPS73x01DRBEVM-518 user's guide](#)

8.3 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.4 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的[使用条款](#)。

8.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

8.6 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.7 术语表

TI 术语表 本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision V (September 2024) to Revision W (May 2025)	Page
• 更新了 DRB0008A 封装外形图的 DRB (VSON).....	4
• 添加了新的硅基 DBV 热性能信息.....	4
• Changed discussion of EN and added information about EN turning the regulator on in <i>Enable Pin and Shutdown</i> section.....	18
• Deleted <i>Package Mounting</i> section.....	25
• Changed <i>legacy chip</i> to <i>legacy silicon</i> in <i>Device Nomenclature</i> table.....	28

Changes from Revision U (January 2015) to Revision V (September 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 向文档中添加了 M3 器件并添加了 M3 新器件热性能信息表.....	1
• 更改了最大输出电流.....	4
• 更改了 VFB 典型值.....	6
• 添加了新器件电流限值.....	6
• Added new silicon plots to <i>Typical Characteristics</i> section.....	7
• Changed <i>Output current</i> value from 500 mA to 400 mA in <i>Design Parameters (Fixed-Voltage Version)</i> table.....	20
• Changed <i>Detailed Design Procedure</i> section: Changed dropout voltage value from 0.5 A to 0.4 A, changed maximum dropout voltage from an estimation to 200 mV	20
• Added new silicon plots to <i>Application Curves</i> section.....	23
• Added <i>Layout Example for the DBV Package Adjustable Version</i> through <i>Layout Example for the DCQ Package Fixed Version</i> figures to <i>Layout Examples</i> section.....	25
• Added M3 information to <i>Device Nomenclature</i> section.....	28

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73601DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJFQ
TPS73601DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJFQ
TPS73601DBVR1G4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJFQ
TPS73601DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJFQ
TPS73601DBVT.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJFQ
TPS73601DBVTG4.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJFQ
TPS73601DCQ	Obsolete	Production	SOT-223 (DCQ) 6	-	-	Call TI	Call TI	-40 to 125	PS73601
TPS73601DCQG4	Obsolete	Production	SOT-223 (DCQ) 6	-	-	Call TI	Call TI	-40 to 125	PS73601
TPS73601DCQR	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS73601
TPS73601DCQR.A	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS73601
TPS73601DRBR	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJFQ
TPS73601DRBR.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJFQ
TPS73601DRBRG4	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJFQ
TPS73601DRBRM3	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJFQ
TPS73601DRBRM3.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJFQ
TPS73601DRBT	Active	Production	SON (DRB) 8	250 SMALL T&R	Yes	NIPDAU NIPDAUAG NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJFQ
TPS73601DRBT.A	Active	Production	SON (DRB) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJFQ
TPS73601DRBTG4	Active	Production	SON (DRB) 8	250 SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PJFQ
TPS736125DRBR	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T49
TPS736125DRBR.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T49
TPS73615DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T44
TPS73615DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T44
TPS73615DBVT	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 125	T44
TPS73615DCQ	Obsolete	Production	SOT-223 (DCQ) 6	-	-	Call TI	Call TI	-40 to 125	PS73615
TPS73615DCQR	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS73615
TPS73615DCQR.A	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS73615
TPS73615DCQRG4	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73615
TPS73615DCQRG4.A	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73615

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73615DRBR	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T44
TPS73615DRBR.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T44
TPS73616DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCQ
TPS73616DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	OCQ
TPS73616DBVT	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 125	OCQ
TPS73618DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T43
TPS73618DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T43
TPS73618DBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T43
TPS73618DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T43
TPS73618DBVT.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T43
TPS73618DBVTG4.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T43
TPS73618DCQR	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS73618
TPS73618DCQR.A	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS73618
TPS73619DRBR	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BYY
TPS73619DRBR.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	BYY
TPS73619DRBT	Obsolete	Production	SON (DRB) 8	-	-	Call TI	Call TI	-40 to 125	BYY
TPS73625DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42
TPS73625DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42
TPS73625DBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42
TPS73625DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42
TPS73625DBVT.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42
TPS73625DBVTG4.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T42
TPS73625DCQ	Obsolete	Production	SOT-223 (DCQ) 6	-	-	Call TI	Call TI	-40 to 125	PS73625
TPS73625DCQR	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS73625
TPS73625DCQR.A	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	SN	Level-2-260C-1 YEAR	-40 to 125	PS73625
TPS73630DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T45
TPS73630DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T45
TPS73630DBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T45
TPS73630DBVT	Obsolete	Production	SOT-23 (DBV) 5	-	-	Call TI	Call TI	-40 to 125	T45
TPS73630DCQ	Obsolete	Production	SOT-223 (DCQ) 6	-	-	Call TI	Call TI	-40 to 125	PS73630
TPS73630DCQR	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73630

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS73630DCQR.A	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73630
TPS73632DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T53
TPS73632DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T53
TPS73632DBVRG4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T53
TPS73633DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T46
TPS73633DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T46
TPS73633DBVR1G4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T46
TPS73633DBVR1G4.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T46
TPS73633DBVT	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T46
TPS73633DBVT.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T46
TPS73633DBVTG4.A	Active	Production	SOT-23 (DBV) 5	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T46
TPS73633DCQ	Obsolete	Production	SOT-223 (DCQ) 6	-	-	Call TI	Call TI	-40 to 125	PS73633
TPS73633DCQR	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73633
TPS73633DCQR.A	Active	Production	SOT-223 (DCQ) 6	2500 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PS73633
TPS73633DRBR	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T46
TPS73633DRBR.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	T46
TPS73633DRBRM3	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T46
TPS73633DRBRM3.A	Active	Production	SON (DRB) 8	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T46
TPS73633DRBT	Active	Production	SON (DRB) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T46
TPS73633DRBT.A	Active	Production	SON (DRB) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T46
TPS73633DRBTG4	Active	Production	SON (DRB) 8	250 SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T46
TPS73643DBVR	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T54
TPS73643DBVR.A	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T54
TPS73643DBVRG4	Active	Production	SOT-23 (DBV) 5	3000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T54

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

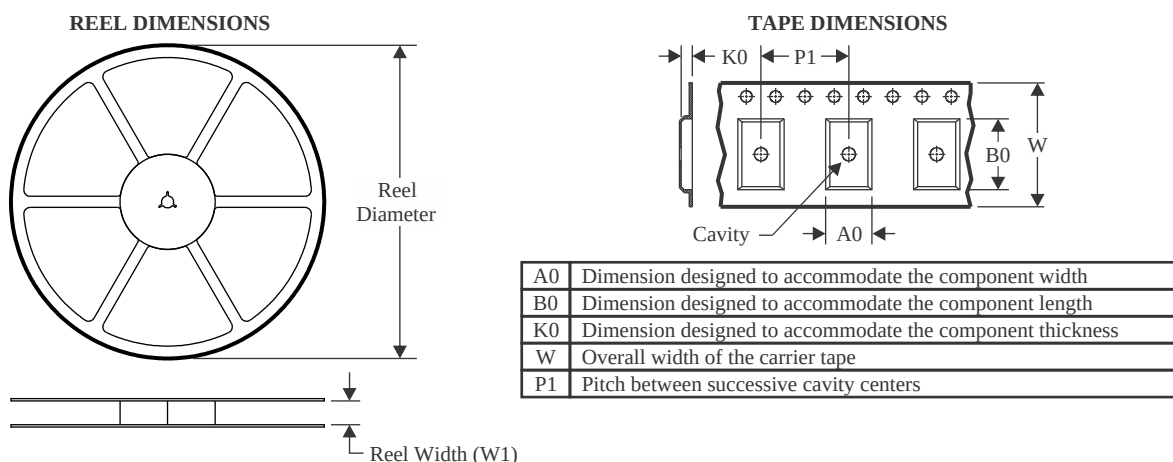
OTHER QUALIFIED VERSIONS OF TPS736 :

- Automotive : [TPS736-Q1](#)

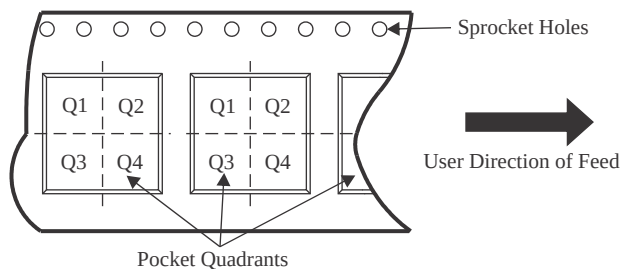
NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

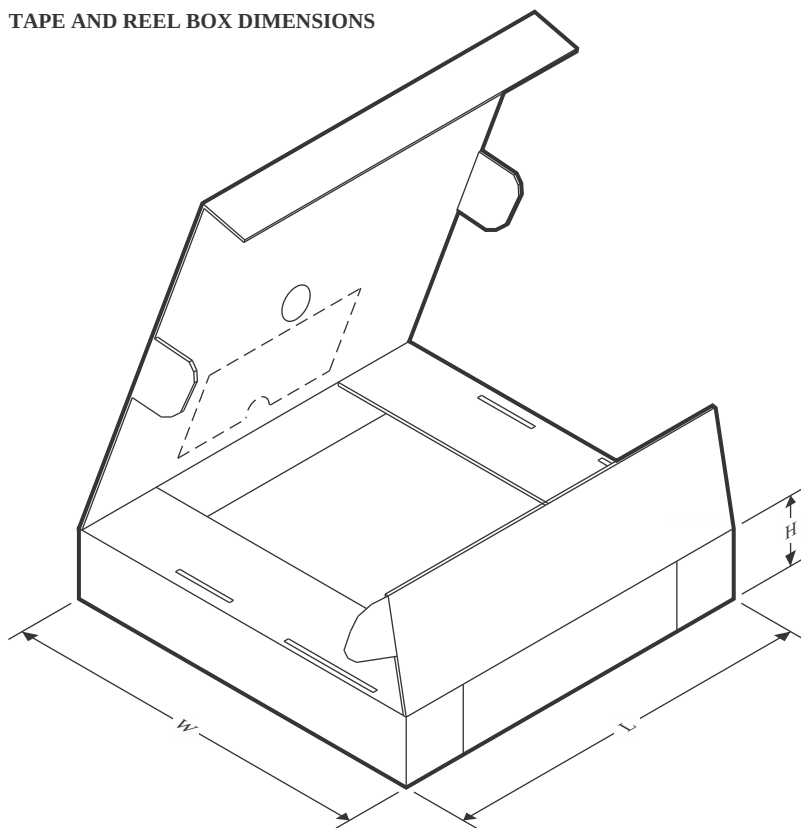


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73601DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73601DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS73601DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS73601DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73601DRBRM3	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73601DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS736125DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73615DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS73615DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS73615DCQRG4	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73615DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73616DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73618DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73618DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73618DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS73619DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.0	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73625DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73625DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73625DBVT	SOT-23	DBV	5	250	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73625DCQR	SOT-223	DCQ	6	2500	330.0	12.4	6.85	7.3	1.88	8.0	12.0	Q3
TPS73630DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73630DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73632DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73633DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73633DBVR1G4	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73633DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS73633DCQR	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73633DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73633DRBRM3	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73633DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73643DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73601DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73601DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73601DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS73601DRBR	SON	DRB	8	3000	356.0	356.0	35.0
TPS73601DRBRM3	SON	DRB	8	3000	367.0	367.0	35.0
TPS73601DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS736125DRBR	SON	DRB	8	3000	356.0	356.0	35.0
TPS73615DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73615DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS73615DCQRG4	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS73615DRBR	SON	DRB	8	3000	356.0	356.0	35.0
TPS73616DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73618DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73618DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73618DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS73619DRBR	SON	DRB	8	3000	367.0	367.0	38.0
TPS73625DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73625DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

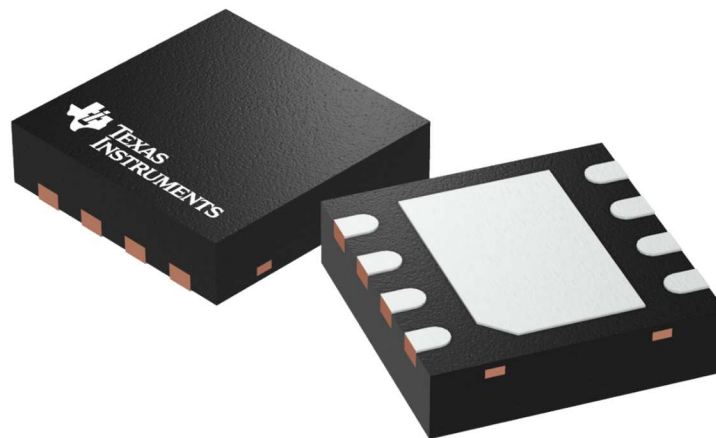
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73625DBVT	SOT-23	DBV	5	250	200.0	183.0	25.0
TPS73625DCQR	SOT-223	DCQ	6	2500	356.0	356.0	36.0
TPS73630DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73630DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73632DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73633DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73633DBVR1G4	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS73633DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS73633DCQR	SOT-223	DCQ	6	2500	346.0	346.0	41.0
TPS73633DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPS73633DRBRM3	SON	DRB	8	3000	367.0	367.0	35.0
TPS73633DRBT	SON	DRB	8	250	210.0	185.0	35.0
TPS73643DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0

DRB 8

GENERIC PACKAGE VIEW

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



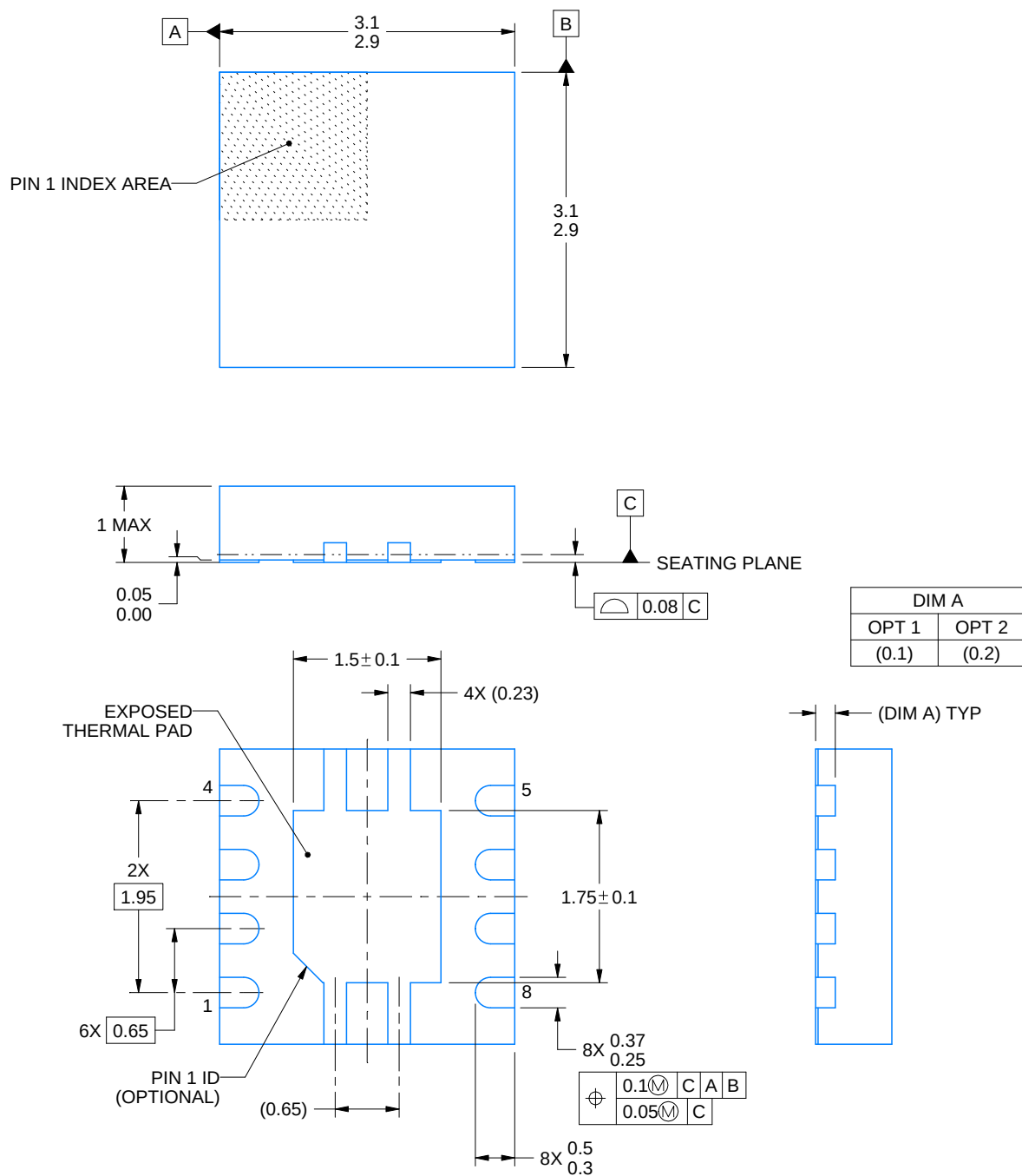
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L



VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



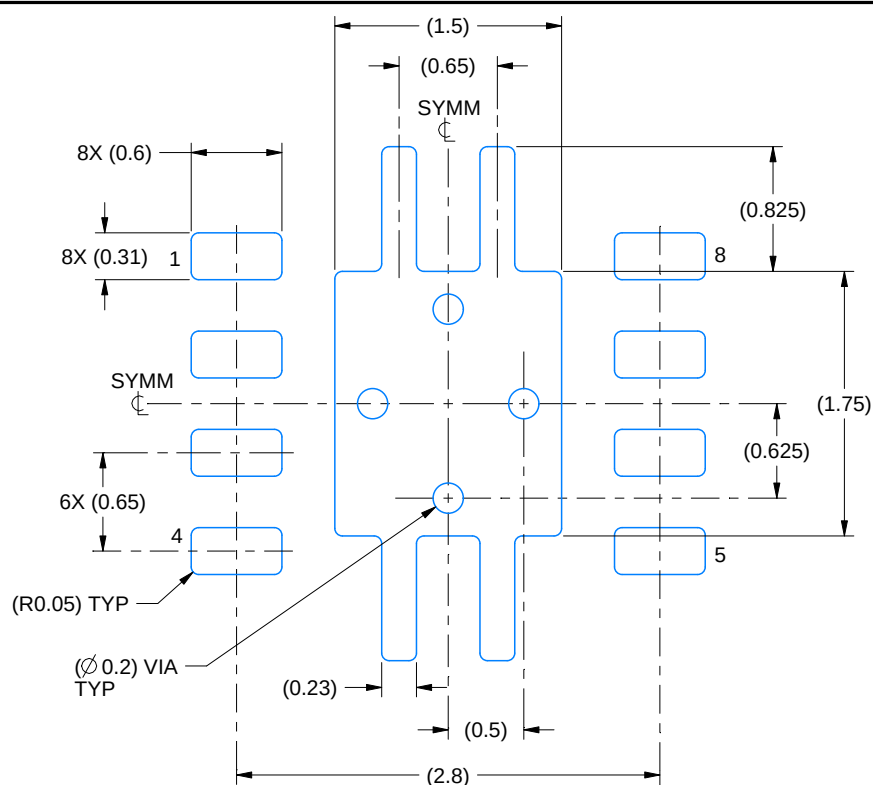
4218875/A 01/2018

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

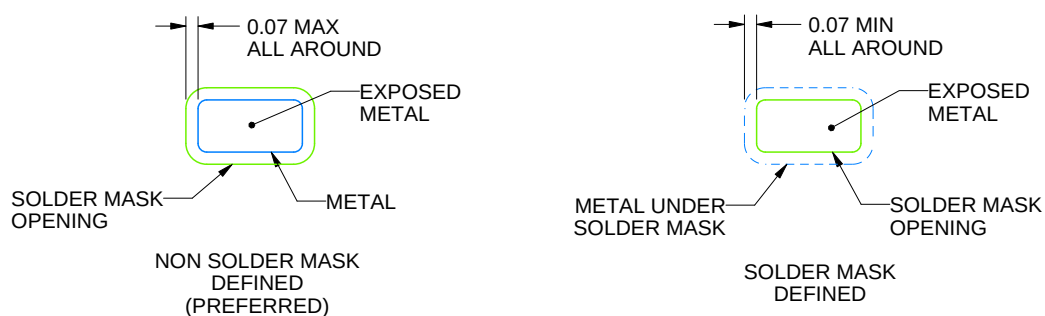
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

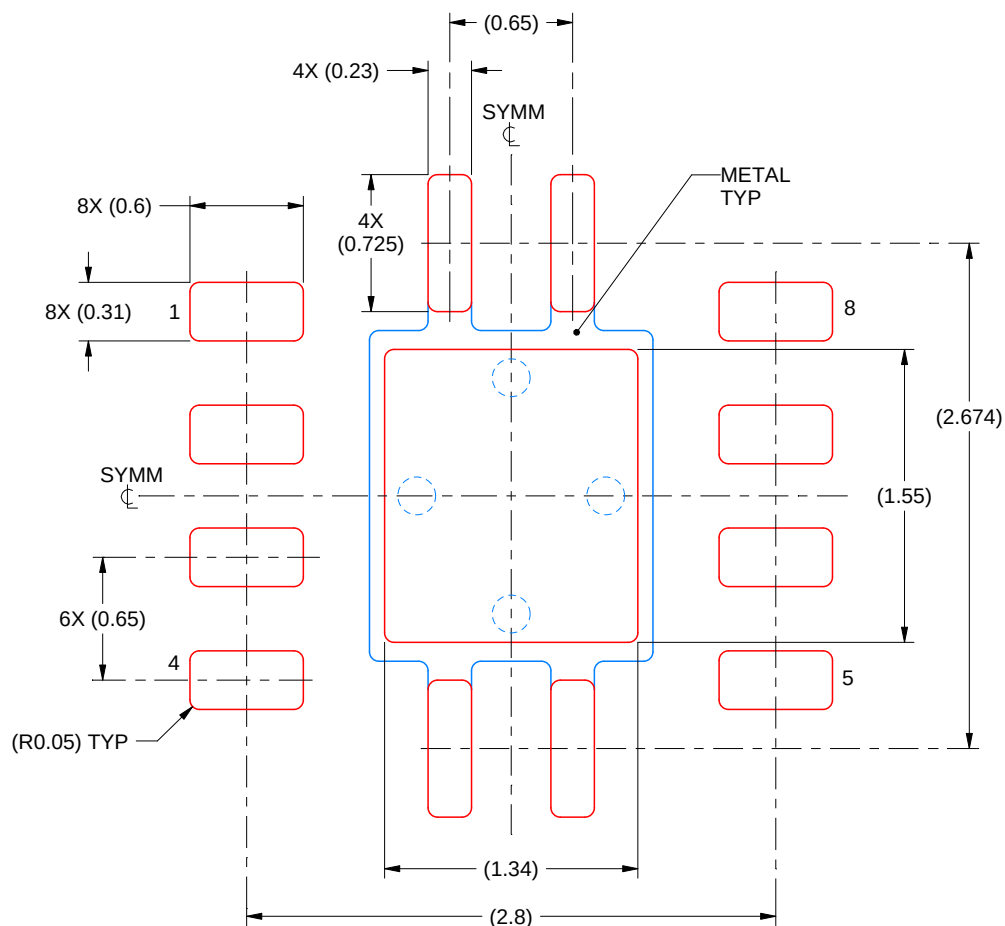
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

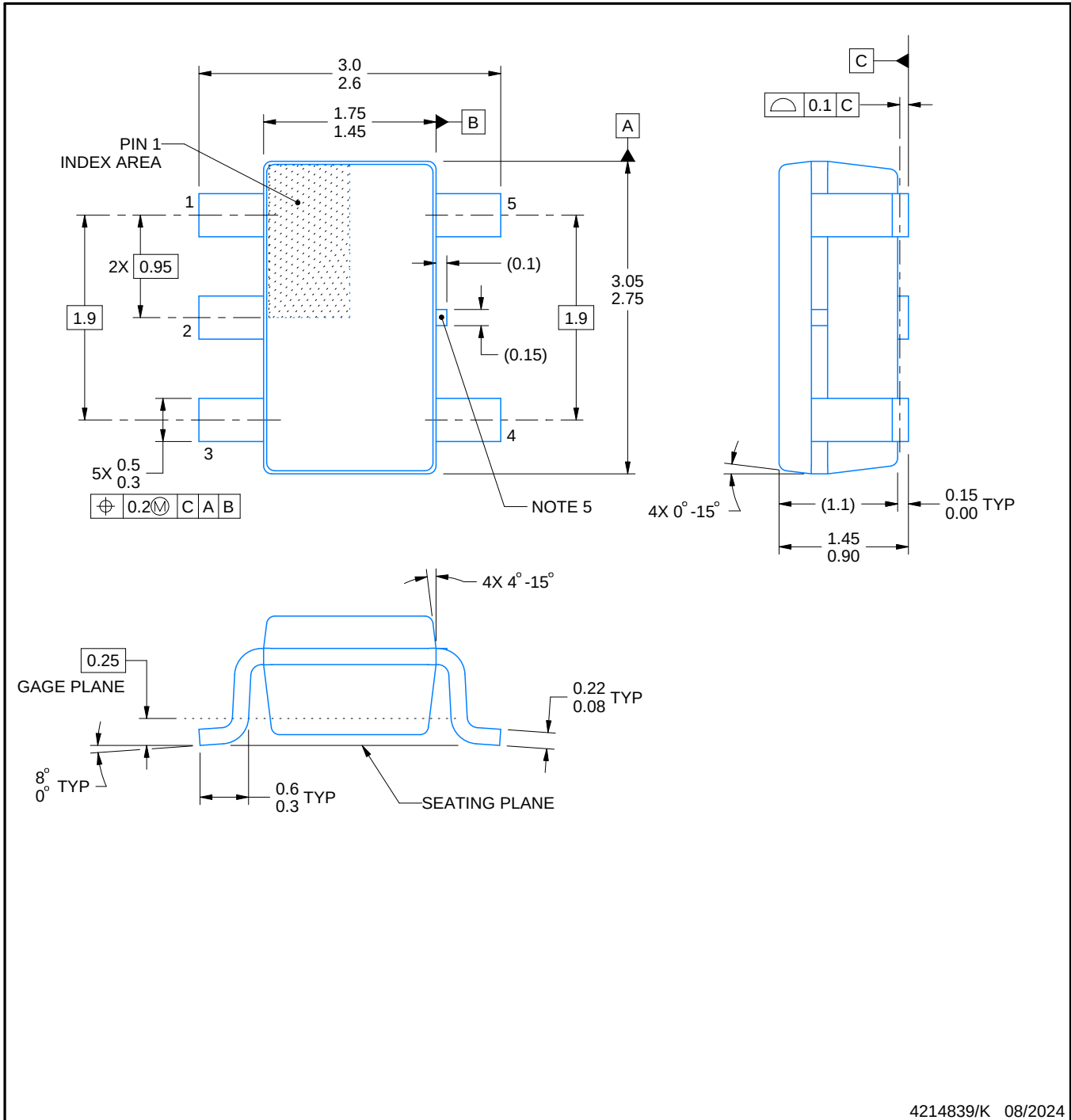


DBV0005A

PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/K 08/2024

NOTES:

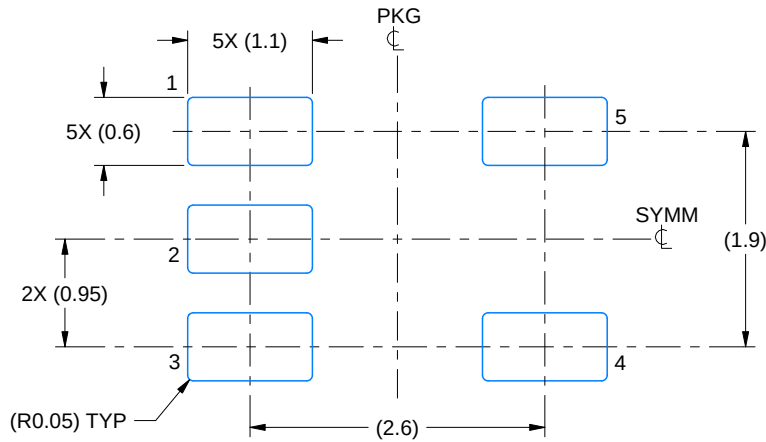
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

EXAMPLE BOARD LAYOUT

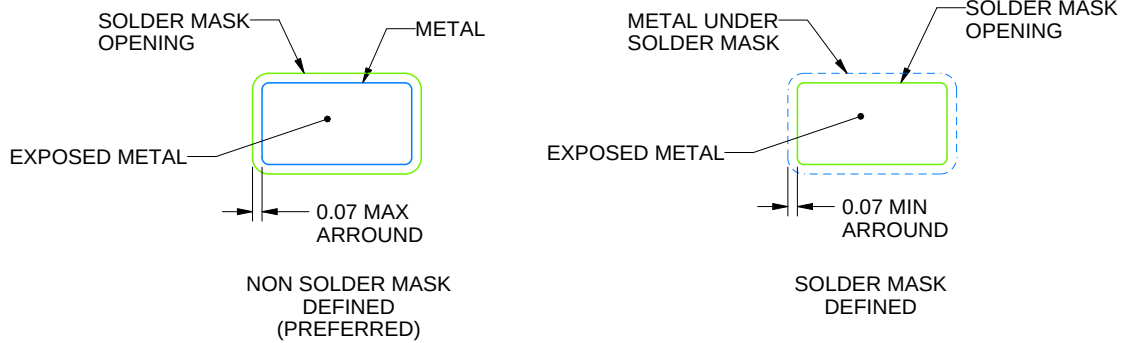
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4214839/K 08/2024

NOTES: (continued)

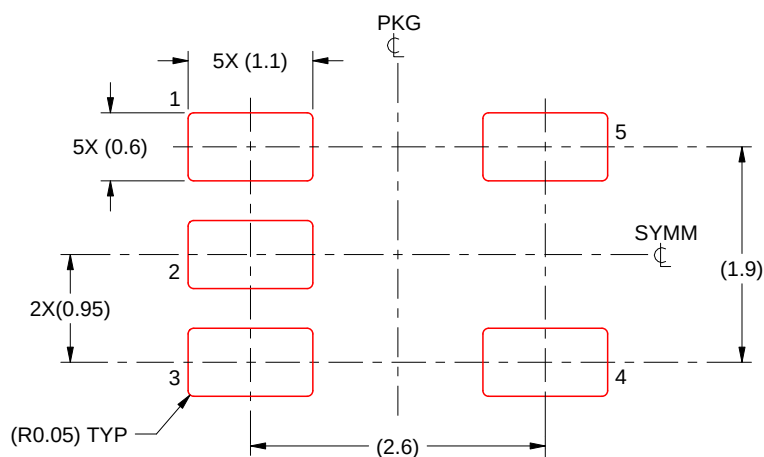
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

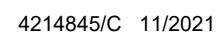
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.

2. This drawing is subject to change without notice.

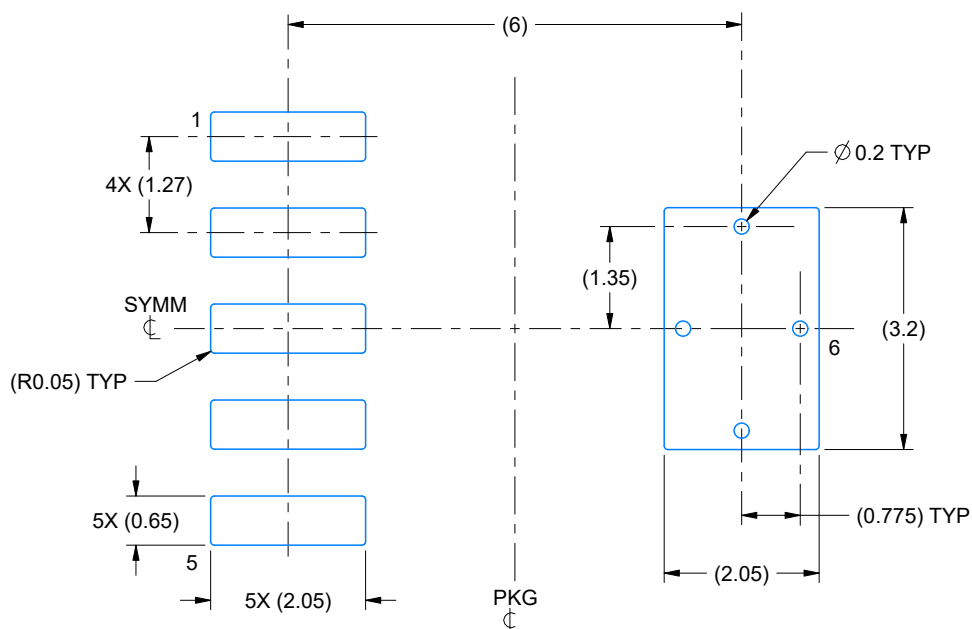
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

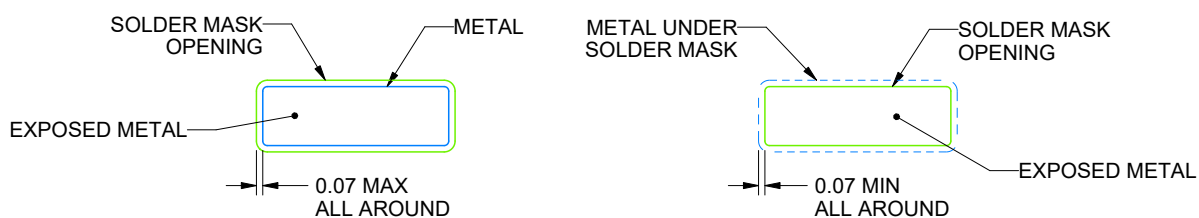
DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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NOTES: (continued)

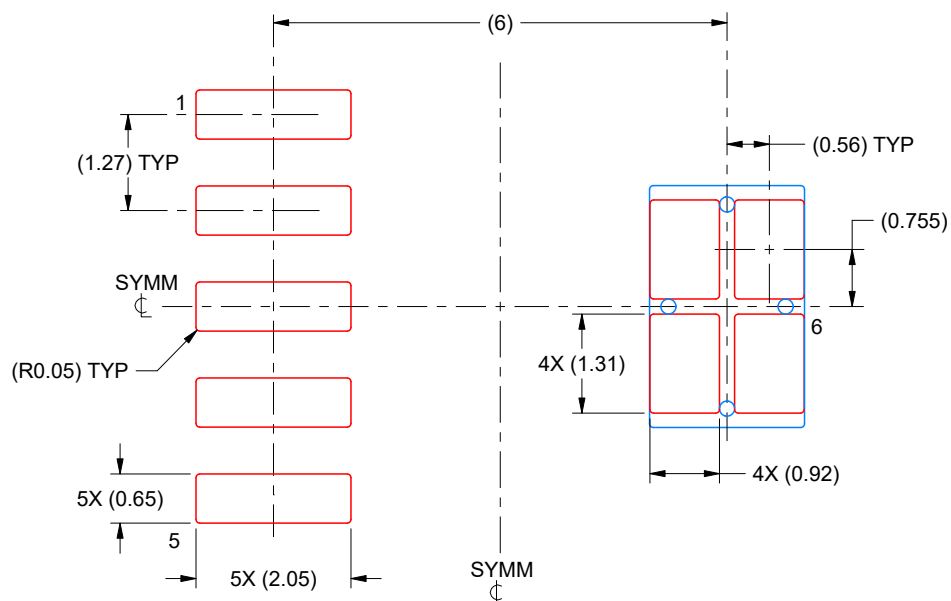
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DCQ0006A

SOT - 1.8 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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