具有自适应电源管理功能的 DAC8771 单通道 16 位电压或电流输出数模转换器

1 特性

- 输出电流：
  - 0mA - 24mA；3.5mA - 23.5mA；0mA - 20mA；4mA - 20mA；±24mA
- 输出电压（可配置或不配置 20% 的超量程）：
  - 0V - 5V；0V - 10V；±5V；±10V
  - 0V - 6V；0V - 12V；±6V；±12V
- 自适应电源管理
- 单宽电源引脚
  - 12V - 36V（使用降压/升压转换器）
  - 12V - 33V（不使用降压/升压转换器）
- ±0.1% 满量程范围 (FSR) 总未调节误差 (TUE)
- 微分非线性 (DNL)：±1 最低有效位 (LSB) 最大值
- 5V 内部基准（10ppm/°C 最大值）
- 5V 内部数字电源输出
- CRC/帧错误检查，看门狗定时器
- 过热报警、开路/短路
- 报警条件下的安全操作
- 自动学习功能
- 宽温度范围：-40°C 至 +125°C

2 应用

- 4mA 至 20mA 电流环路
- 模拟输出模块
- 可编程逻辑控制器 (PLC)
- 楼宇自动化

3 说明

DAC8771 是一款单通道的精密全集成 16 位数模转换器 (DAC)，具有自适应电源管理功能，适用于工业控制 应用中，低功耗是一个关键问题。自适应电源管理电路在使能后能够最大程度降低芯片功耗。通过编程设定为电流输出后，电流输出驱动器上的电源电压根据电流输出引脚处电压的连续反馈，通过降压/升压转换器在 4V 至 32V 范围内进行调节。通过编程设定为电压输出后，该电路为电压输出级 (±15V) 生成可编程电源电压。DAC8771 包含一个 LDO，用于从单电源引脚生成数字电源 (5V)，特别适合用于支持隔离式 应用中，低功耗是一个关键问题。

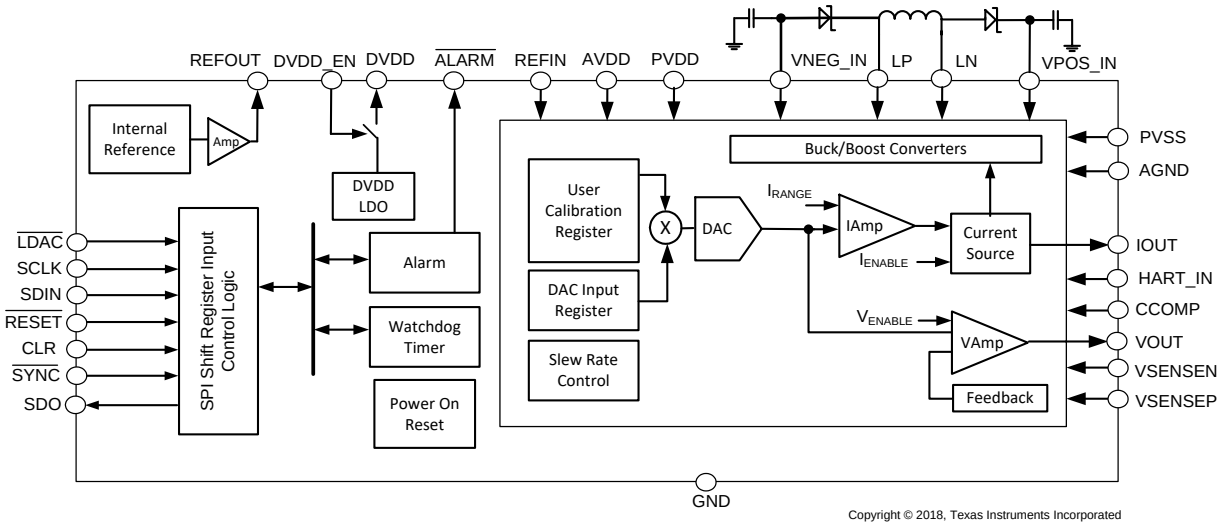
DAC8771 还采用一种 HART 信号接口，支持在电流输出中叠加外部 HART 信号。电流输出 DAC 压摆率由寄存器通过编程设定。该器件可在使用集成降压/升压转换器的情况下由 +12V 至 +36V 的单个外部电源供电，或在禁用降压/升压转换器的情况下由多个外部电源供电。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DAC8771	VQFN (48)	7.00mm x 7.00mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

DAC8771 框图



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4 修订历史记录

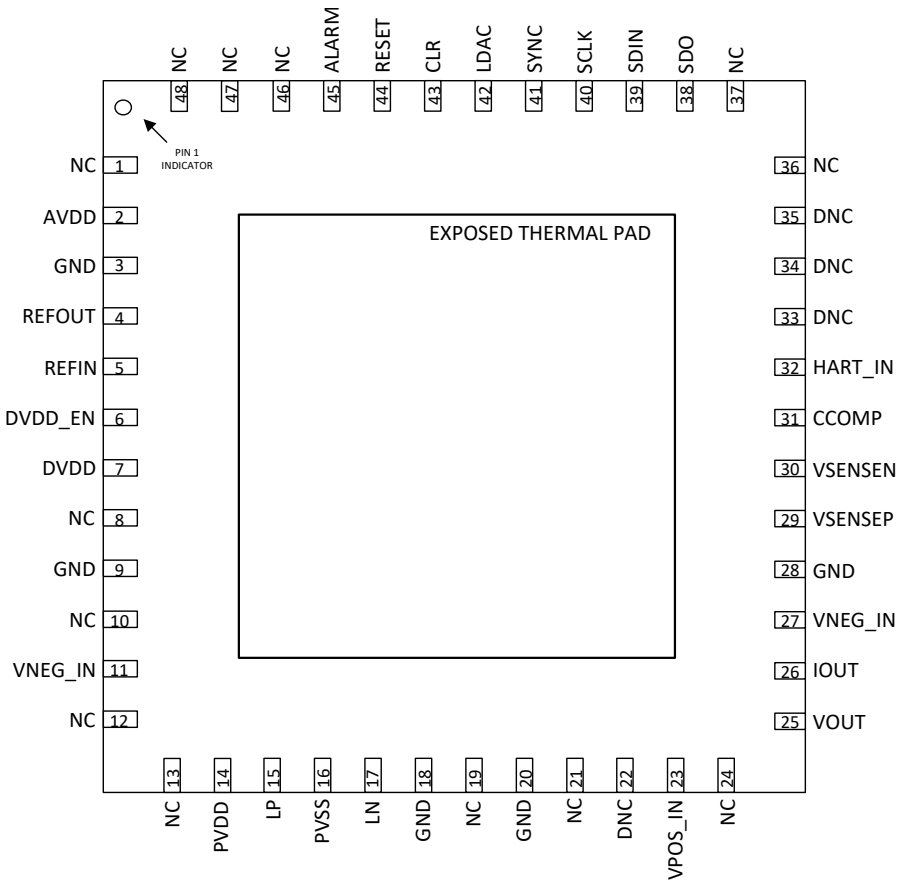
日期	修订版本	说明
2017 年 2018	*	第一版.

5 Device Comparison Table

PRODUCT	RESOLUTION	DIFFERENTIAL NONLINEARITY (LSB)	SPECIFIED TEMPERATURE RANGE
DAC8771	16	±1	–40°C to +125°C

6 Pin Configuration and Functions

RGZ Package
48 Pin VQFN
Top View



Thermal pad connected to ground.

Pin Functions

NAME	NUMBER	TYPE	DESCRIPTION
AVDD	2	Supply	Power supply for all analog circuitry of the device except buck-boost converter and output amplifiers.
GND	3, 9, 18, 20, 28	Supply	Ground.
REFOUT	4	Analog Output	Internal reference output. Connects to REFIN when using internal reference.
REFIN	5	Analog Input	Reference input. Connects to REFOUT when using internal reference.
DVDD_EN	6	Digital Input	Internal power-supply enable pin. Connect this pin to GND to disable the internal DVDD, or leave this pin unconnected to enable the internal DVDD. When this pin is connected to GND an external supply must be connected to the DVDD pin.

Pin Functions (continued)

NAME	NUMBER	TYPE	DESCRIPTION
DVDD	7	Supply	Digital supply pin (Input/Output). Internal DVDD enabled when DVDD_EN is floating, External DVDD must be supplied when DVDD_EN is connected to GND.
VNEG_IN	11, 27	Supply	Negative power supply for output stage. Connected internally, however both external connections are required.
PVDD	14	Supply	Buck-Boost converter power supply.
LP	15	Analog Output	External inductor positive terminal.
PVSS	16	Supply	Switch ground for Buck-Boost converter.
LN	17	Analog Output	External inductor negative terminal.
VPOS_IN	23	Supply	Positive power supply for output stage.
VOUT	25	Analog Output	Voltage output pin.
IOUT	26	Analog Output	Current output pin.
VSENSEP	29	Analog Input	Positive sense pin for voltage output.
VSENSEN	30	Analog Input	Negative sense pin for voltage output.
CCOMP	31	Analog Output	External compensation capacitor connection pin for voltage output. Addition of the external capacitor improves stability for high capacitive loads at the VOUT pin by reducing the bandwidth of the output amplifier at the expense of settling time.
HART_IN	32	Analog Input	Input pin for HART modulation. If this pin is used it must be AC coupled to the HART input sinusoidal waveforms via a capacitor. If this feature is not used TI recommends to AC couple this pin to ground via a capacitor, though it may also be left floating.
SDO	38	Digital Output	Serial data output. Data is valid on the falling edge of SCLK.
SDIN	39	Digital Input	Serial data input. Data is clocked into the 24-bit input shift register on the falling edge of the serial clock input. Schmitt-Trigger logic input.
SCLK	40	Digital Input	Serial clock input of serial peripheral interface (SPI™). Data can be transferred at rates up to 25 MHz. Schmitt-Trigger logic input.
$\overline{\text{SYNC}}$	41	Digital Input	SPI™ bus chip select input (active low). Data bits are not clocked into the serial shift register unless $\overline{\text{SYNC}}$ is low. When SYNC is high SDO is in a high-impedance state.
$\overline{\text{LDAC}}$	42	Digital Input	Load DAC latch control input. A logic low on this pin loads the input shift register data into the DAC register and updates the DAC output.
CLR	43	Digital Input	Level triggered clear pin (active high). Clears DAC output to zero code or mid code (see DAC Clear section).
$\overline{\text{RESET}}$	44	Digital Input	Reset input (active low). Logic low on this pin causes the device to perform a reset.
$\overline{\text{ALARM}}$	45	Digital Output	$\overline{\text{ALARM}}$ pin. Open drain output. External pull-up resistor required (10 kΩ). The pin goes low (active) when any ALARM condition is detected (open-circuit, over-temperature, watchdog timeout, and others).
NC	1, 8, 10, 12, 13, 19, 21, 24, 36, 37, 46, 47, 48	N/A	No connection is required on these pins.
DNC	22,33, 34, 35	N/A	Do not connect these pins.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage	PVDD/AVDD to PBKG	-0.3	40	V
	PVSS to GND	-0.3	0.3	
	VPOS_IN to VNEG_IN	-0.3	40	
	VPOS_IN to GND	-0.3	33	
	VNEG_IN to GND	-20	0.3	
	VSENSEN to GND	VNEG_IN	VPOS_IN	
	VSENSEP to GND	VNEG_IN	VPOS_IN	
	CCOMP to VNEG_IN	-0.3	6	
	DVDD to GND	-0.3	6	
	REFOUT/REFIN to GND	-0.3	6	
	Digital input voltage to GND	-0.3	DVDD+0.3	
Output voltage	VOUT to GND	VNEG_IN	VPOS_IN	V
	IOUT to GND	VNEG_IN	VPOS_IN	
	SDO, ALARM to GND	-0.3	DVDD+0.3	
Input Current	Current into any pin	-10	10	mA
Power dissipation			(TJmax – TA)/ThetaJA	W
Operating junction temperature, T_J		-40	150	°C
Junction temperature range (TJ max)			150	
Storage temperature, T_{stg}		-65	150	

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	NOM	MAX	UNIT
POWER SUPPLY					
PVDD/AVDD/ to GND	Positive supply voltage to ground	12		36	V
VPOS_IN to GND	Positive supply voltage to ground for all modes	-0.3		33	
VNEG_IN to GND	Negative supply voltage to substrate for current output mode	-18		0	V
	Negative supply voltage to substrate for voltage output mode	-18		-5	V
VPOS_IN to VNEG_IN		12		36	V
VSENSEN to GND	The minimum headroom spec for voltage output stage must be met	-7		7	V
DVDD to GND	Digital supply voltage to substrate	2.7		5.5	V
DIGITAL INPUTS					
VIH, input high voltage		2			V
VIL, input low voltage	3.6 V < DVDD < 5.5 V			0.8	V
	2.7 V < DVDD < 3.6 V			0.6	V
REFERENCE INPUT					
REFIN to GND	Reference input to substrate	4.95		5.05	V
TEMPERATURE RANGE					
TA	Operating temperature	-40		125	°C

(1) The minimum headroom spec for voltage output stage and the compliance voltage for current output stage should be met. When Buck-Boost converter is enabled VPOS_IN_x/VNEG_IN_x are generated internally to meet headroom and compliance specs. When Buck-Boost converter is disabled VPOS_IN_x, AVDD, and PVDD must be tied together.

7.4 Thermal Information

THERMAL METRIC(1)		DAC8771 RGZ 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	21.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	9.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	5.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.3	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953

7.5 Electrical Characteristics

AVDD/PVDD/VPOS_IN = +15V, VNEG_IN = -15V, VSENSEN = GND = PVSS = 0 V, External DVDD = 2.7 V. VOUT : RL = 1 kΩ, CL = 200 pF, IOUT : RL = 250Ω; all specifications -40C to +125C, unless otherwise noted. REFIN= +5 V external, REFOUT = +5V internal, Buck-Boost Converter disabled unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT OUTPUT						
IOUT	Output Current Ranges		0		24	mA
			0		20	mA
			3.5		23.5	mA
			-24		24	mA
			4		20	mA
ACCURACY						
	Resolution		16			Bits
INL	Relative accuracy(1)	All ranges except bipolar range	-10		10	LSB
		Bipolar range only	-12		12	LSB
DNL	Differential Nonlinearity(1)	Ensured monotonic	-1		1	LSB
TUE	Total Unadjusted Error(1)	-40°C to 125°C	-0.1		0.1	%FSR
		TA = +25°C	-0.08		0.08	
		-40°C to 125°C (4-20mA)	-0.130		0.130	
		TA = +25°C (4-20mA)	-0.08		0.08	
OE	Offset Error(1)	-40°C to 125°C	-0.06		0.06	%FSR
		TA = +25°C	-0.05		0.05	
		-40°C to -125°C (4-20mA)	-0.085		0.085	
		TA = +25°C (4-20mA)	-0.04		0.04	
OE-TC	Offset Error Temperature Coefficient	-40°C to -125°C		1.5		ppm FSR / ºC
ZCE	Zero Code Error	DAC data set to 0x0000	-13		13	uA
		DAC data set to 0x0000 (4-20mA)	-13		13	uA
ZCE-TC	Zero Code Error Temperature Coefficient	DAC data set to 0x0000, -40°C to -125°C		1.5		ppm/ ºC
GE	Gain Error(1)	-40°C to -125°C	-0.1		0.1	%FSR
		TA = +25°C	-0.075		0.075	
		-40°C to -125°C (4-20mA)	-0.110		0.110	
		TA = +25°C (4-20mA)	-0.08		0.08	
GE-TC	Gain Error Temperature Coefficient	-40C to -125C		3		ppm FSR / ºC
FSE	Full Scale Error	DAC data set to 0xFFFF, -40°C to -125°C	-0.1		0.1	%FSR
		DAC data set to 0xFFFF, -40°C to -125°C (4-20mA)	-0.130		0.130	%FSR
NFSE	Negative Full Scale Error	DAC data set to 0x0000, bipolar range only, -40°C to -125°C	-0.05		0.05	%FSR
FSE-TC	Full Scale Error Temperature Coefficient			3		ppm FSR / ºC
BPZE	Bipolar Zero Error	bipolar range only, DAC data set to 0x8000, -40°C to -125°C	-0.05		0.05	%FSR
		bipolar range only, DAC data set to 0x8000, TA = +25°C	-0.02		0.02	
BPZE-TC	Bipolar Zero Error Temperature Coefficient	0x8000h into DAC,-40°C to -125°C		4		ppm/ ºC

(1) For current output all ranges except ±24 mA, low code of 256d and a high code of 65280d are used, for ±24 mA range low code of 0d and a high code of 65280d. For voltage output, low code of 256d and a high code of 65280d are used

Electrical Characteristics (continued)

AVDD/PVDD/VPOS_IN = +15V, VNEG_IN = -15V, VSENSEN = GND = PVSS = 0 V, External DVDD = 2.7 V. VOUT : RL = 1 kΩ, CL = 200 pF, IOUT : RL = 250Ω; all specifications -40C to +125C, unless otherwise noted. REFIN= +5 V external, REFOUT = +5V internal, Buck-Boost Converter disabled unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCL	Loop Compliance Voltage	Output=24mA			VPOS_IN-3	V
		Output=±24mA	|VNEG_IN|-3		VPOS_IN-3	
RL	Resistive Load	All except ±24 mA range			1.2K	Ω
		±24 mA range			0.625K	
DC-PSRR	DC Power Supply Rejection Ratio	DAC data set to 0x8000, 20mA range		0.1		µA/V
Zo	Output Impedance	DAC data set to 0x8000		10		MΩ
IOLEAK	Output Current Leakage	Iout is disabled or in power-down		1		nA
HART INTERFACE						
VHART-IN	HART Input		400	500	600	mVpp
	Corresponding Output	HART In = 500mVpp 1.2KHz		1		mApp
VOLTAGE OUTPUT						
VOUT	Voltage Output Ranges (normal mode)		0		5	
			0		10	
			-5		5	
			-10		10	
	Voltage Output Ranges (Overrange mode)		0		6	
			0		12	
			-6		6	
			-12		12	
ACCURACY						
	Resolution		16			Bits
INL	Relative Accuracy, INL(1)		-12		12	LSB
DNL	Differential Nonlinearity, DNL(1)	Ensured monotonic	-1		1	LSB
TUE	Total Unadjusted Error, TUE(1)	-40°C to 125°C, VOUT unloaded	-0.1	±0.05	0.1	%FSR
		TA = +25°C, VOUT unloaded	-0.75		0.75	
BPZE	Bipolar Zero Error	bipolar range only, DAC data set to 0x8000, -40°C to 125°C, VOUT unloaded	-0.05		0.05	%FSR
		bipolar range only, DAC data set to 0x8000, TA = +25°C, VOUT unloaded	-0.03		0.03	
BPZE-TC	Bipolar Zero Error Temperature Coefficient	bipolar range only, DAC data set to 0x8000, -40°C to 125°C, (VOUT unloaded)		1		ppm FSR / ºC
OE	Offset Error	Unipolar ranges only, (Vout unloaded), -40°C to 125°C	-5		5	mV
OE	Offset Error	Unipolar ranges only, (Vout unloaded), TA = 25°C		0.65		mV
OE-TC	Offset Error Temperature Coefficient	Unipolar ranges only, -40°C to 125°C		1.5		ppm FSR/ ºC
GE	Gain Error(1)	-40°C to 125°C, VOUT unloaded	-0.1		0.1	%FSR
		TA = +25°C, VOUT unloaded	-0.07		0.07	
GE-TC	Gain Error Temperature Coefficient			3		ppm FSR / ºC
FSE	Full Scale Error	DAC data set to 0xFFFF, -40° to 125°C, (Vout unloaded)	-0.1		0.1	%FSR
		DAC data set to 0xFFFF, 25°C, (Vout unloaded)		0.03		%FSR

Electrical Characteristics (continued)

AVDD/PVDD/VPOS_IN = +15V, VNEG_IN = -15V, VSENSEN = GND = PVSS = 0 V, External DVDD = 2.7 V. VOUT : RL = 1 kΩ, CL = 200 pF, IOUT : RL = 250Ω; all specifications -40C to +125C, unless otherwise noted. REFIN= +5 V external, REFOUT = +5V internal, Buck-Boost Converter disabled unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
NFSE	Negative Full Scale Error	Bipolar ranges only, DAC data set to 0x0000, -40°C to 125°C, (Vout unloaded)	-0.07		0.07	%FSR
		Bipolar ranges only, DAC data set to 0x0000, -40°C to 125°C, (Vout unloaded)		0.002		%FSR
FSE-TC	Full Scale Error Temperature Coefficient	(Vout unloaded)		2		ppm FSR / ºC
	Headroom	Output unloaded, VPOS_IN with respect to VOUT, DAC data set to 0xFFFF, specified by design	0.5			V
		1kΩ output load, VPOS_IN with respect to VOUT, DAC data set to 0xFFFF, specified by design	3			V
	Footroom	Bipolar, ranges only, VNEG_IN with respect to VOUT, DAC data set to 0x0000, specified by design	-3			V
		Unipolar ranges only, VNEG_IN with respect to VOUT, DAC data set to 0x0000, specified by design	-5			V
	Short-Circuit Current	SCLIM[1:0] = "00" (see register map)	17		27	mA
		SCLIM[1:0] = "01" (see register map)	8		12	mA
		SCLIM[1:0] = "10" (see register map)	22		30	mA
		SCLIM[1:0] = "11" (see register map)	26		36	mA
RL	Load		1			kΩ
CL	Capacitive Load Stability	RL = Open			20	nF
		RL = 1 kΩ			20	nF
		RL = 1 kΩ with External compensation capacitor (150pF) connected.			1	µF
ZO	DC Output Impedance	Voltage output enabled, Vout = Mid-Scale, 0-10V range		0.01		Ω
		Voltage output disabled		50		MΩ
		Voltage output disabled (POC = '0')		30		kΩ
DC-PSRR	DC Power Supply Rejection Ratio	No Output Load		10		µV/V
	VSENSEP Impedance	VOUT Enabled, Vout = Mid-Scale, 0-10V Range, specified by design		120		kΩ
	VSENSEN Impedance	VOUT Enabled, Vout = Mid-Scale, 0-10V Range, specified by design		240		kΩ
EXTERNAL REFERENCE INPUT						
IREF	External reference current	Vout = Negative Full-Scale, ±12V range		350		µA
	Reference Input Capacitance			100		pF
INTERNAL REFERENCE OUTPUT						
VREF	Reference Output	TA = 25°C	4.99		5.01	V
VREF-TC	Reference TC	TA = -40°C to 125°C	-10		10	ppm/°C
TUE	DAC Voltage Output Total unadjusted error(1)	-40°C to 125°C, VOUT unloaded, Internal reference enabled		0.2		%FSR
	DAC Current Output Total unadjusted error(1)	-40°C to +125°C, Internal reference enabled		0.2		%FSR
	Output Noise (0.1 Hz to 10 Hz)	TA = 25°C		13		µV p-p
	Noise Spectral Density	At 10 kHz, 25°C		200		nV/sqrtHz

Electrical Characteristics (continued)

AVDD/PVDD/VPOS_IN = +15V, VNEG_IN = -15V, VSENSEN = GND = PVSS = 0 V, External DVDD = 2.7 V. VOUT : RL = 1 kΩ, CL = 200 pF, IOUT : RL = 250Ω; all specifications -40C to +125C, unless otherwise noted. REFIN= +5 V external, REFOUT = +5V internal, Buck-Boost Converter disabled unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CL	Capacitive Load				600	nF
IL	Load Current			±5		mA
	Short Circuit Current	Reference output shorted to GND		20		mA
	Load Regulation	Sourcing and Sinking, TA = +25°C		5		µV/mA
	Line regulation	TA = +25°C		1		uV/V
BUCK BOOST CONVERTER						
RON	Switch On Resistanvce	TA = +25°C		3		Ω
ILEAK	Switch Leakage Current	TA = +25°C		20		nA
L	Inductor	between LP and LN		100		µH
ILMAX	Peak Inductor Current	TA = +25°C, maximum specified by design		0.35	0.5	A
VO	Output Voltage	VPOS_IN	4		32	V
		VNEG_IN	-18		-5	V
CL	Load Capacitor	VPOS_IN and VNEG_IN	10			µF
	Start up time	After enabling VPOS_IN and VNEG_IN with 10µF load capacitor on these pins		3		ms
DVDD LDO						
VO	Output Voltage			5		V
ILOAD	Load Current				10	mA
CL	Load Capacitor				0.2	µF
THERMAL ALARM						
	Trip point			150		°C
	Hysteresis			15		°C
DIGITAL INPUTS						
	Hysteresis voltage			0.4		V
	Input Current		-5		5	µA
	Pin Capacitance	Per pin		10		pF
DIGITAL OUTPUTS						
SDO						
VOL	Output Low Voltage	Sinking 200 µA			0.4	V
VOH	Output High Voltage	Sourcing 200 µA	DVDD-0.5			V
ILEAK	High Impedance Leakage		-5		5	µA
	High Impedance Output Capacitance			10		pF
ALARM						
VOL	Output Low Voltage	At 10 mA		0.4		V
ILEAK	High Impedance Leakage			50		µA
	High Impedance Output Capacitance			10		pF
POWER REQUIREMENTS						
IAVDD	Current Flowing into AVDD	Buck-Boost converter enabled, All IOUT Active, 0mA, 0-20mA range		3		mA
		IOUT Active, 0 mA, 0-20mA range, VNEG_IN = 0V		1.3		mA
IPVDD	Current Flowing into PVDD	Buck-Boost converter enabled, Peak Current, specified by design			0.5	A
		Buck-Boost converter disabled		0.1		mA

Electrical Characteristics (continued)

AVDD/PVDD/VPOS_IN = +15V, VNEG_IN = -15V, VSENSEN = GND = PVSS = 0 V, External DVDD = 2.7 V. VOUT : RL = 1 kΩ, CL = 200 pF, IOUT : RL = 250Ω; all specifications -40C to +125C, unless otherwise noted. REFIN= +5 V external, REFOUT = +5V internal, Buck-Boost Converter disabled unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDVDD	Current Flowing into DVDD	All digital pins at DVDD, DVDD 2.7V to 5.5V		1.8		mA
IVPOS_IN	Current Flowing into VPOS_IN	IOUT Active, 0mA, 0-20mA range			1.2	mA
		VOUT Active, no load, 0-10V range, mid scale code			3	mA
IVNEG_IN	Current Flowing into VNEG_IN	IOUT Active, 0mA, ±24mA range			1.2	mA
		VOUT Active, no load, 0-10V range, mid scale code			3	mA
PDISS	Power dissipation (PVDD+AVDD)	Buck-Boost converter positive output enabled, IOUT mode operation, All IOUT channels enabled, Rload = 1Ω, 24mA, PVDD = AVDD = 12V		0.226	0.275	W
IVSENSEP	Current Flowing into VSENSEP	VOUT Disabled, specified by design			40	nA
IVSENSEN	Current Flowing into VSENSEN	VOUT Disabled, specified by design			20	nA
DYNAMIC PERFORMANCE						
VOLTAGE OUTPUT						
T_{sett}	Output Voltage Settling Time	0 to 10V, to ±0.03% FSR RL = 1kΩ || CL = 200pF		15		µs
		0 to 5V, to ±0.03% FSR RL = 1kΩ || CL = 200pF		10		µs
		-5 to 5V, to ±0.03% FSR RL = 1kΩ || CL = 200pF		20		µs
		-10 to 10V, to ±0.03% FSR RL = 1kΩ || CL = 200pF		30		µs
	Output voltage ripple	Buck-Boost converter enabled, 50 KHz 20dB/decade low-pass filter on VPOS_IN		2		mVpp
SR	Slew Rate	RL = 1kΩ || CL = 200pF		1		V/µs
	Power-On Glitch Energy(2)	Specified by design			0.1	V
	Power-off Glitch Energy(3)	Specified by design			0.8	V
	Code-Code Glitch			0.15		µV-sec
	Digital Feedthrough			1		nV-sec
	Output Noise (0.1 Hz to 10 Hz Bandwidth)	0-10V range, Mid-Scale		0.1		LSB p-p
	Output Noise (100 kHz Bandwidth)	0-10V range, Mid-Scale		200		µVrms
	Output Noise Spectral Density	±10V Measured at 10 kHz, Mid-Scale		200		nV/sqrtHz
AC-PSRR	AC Power Supply Rejection Ratio	200mV 50/60Hz sinusoid superimposed on power supply voltage (AC analysis).		-75		dB
CURRENT OUTPUT						
Tsett	Output Current Settling Time	24 mA Step, to 0.1% FSR, no L		10		µs
		24 mA Step, to 0.1% FSR , L = 1mH, CL = 22nF		50		µs
	Output current ripple	Buck-boost converter enabled, 50 KHz 20dB/decade low-pass filter on VPOS_IN		2		µApp
L	Inductive Load(4)				50	mH

(2) No load, DVDD supply ramps up before VPOS_IN, and VNEG_IN, ramp rate of VPOS_IN,and VNEG_IN limited to 18V/msec
(3) Vout disabled, no load, ramp rate of VPOS_IN, and VNEG_IN limited to 18V/msec
(4) 680nF is required at IOUT pin for 50mH pure inductor load

Electrical Characteristics (continued)

AVDD/PVDD/VPOS_IN = +15V, VNEG_IN = -15V, VSENSEN = GND = PVSS = 0 V, External DVDD = 2.7 V. VOUT : RL = 1 kΩ, CL = 200 pF, IOUT : RL = 250Ω; all specifications -40C to +125C, unless otherwise noted. REFIN= +5 V external, REFOUT = +5V internal, Buck-Boost Converter disabled unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC-PSRR	AC Power Supply Rejection Ratio	200mV 50/60Hz Sine wave superimposed on power supply voltage		-75		dB

7.6 Timing Requirements: Write and Readback Mode

At T_A = –40°C to +125°C and DVDD = +2.7 V to +5.5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{SCLK}	Max clock frequency			25	MHz
t_1	SCLK cycle time		40		ns
t_2	SCLK high time		18		ns
t_3	SCLK low time		18		ns
t_4	$\overline{SYNC}$ falling edge to SCLK falling edge setup time		15		ns
t_5	24th/32nd SCLK falling edge to $\overline{SYNC}$ rising edge		13		ns
t_6	$\overline{SYNC}$ high time	Digital slew rate control disabled	40		ns
t_7	Data setup time		8		ns
t_8	Data hold time		5		ns
t_9	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge		33		ns
t_{10}	$\overline{LDAC}$ pulse width low		10		ns
t_{11}	$\overline{LDAC}$ falling edge to DAC output response time			50	ns
t_{12}	DAC output settling time		See section 5.3		µs
t_{13}	CLR high time		10		ns
t_{14}	CLR activation time			50	ns
t_{15}	SCLK rising edge to SDO valid			14	ns
t_{16}	$\overline{SYNC}$ rising edge to DAC output response time			50	ns
t_{17}	$\overline{LDAC}$ falling edge to $\overline{SYNC}$ rising edge		100		ns
t_{18}	$\overline{RESET}$ pulse width		10		ns
t_{19}	$\overline{SYNC}$ rising edge to CLR falling/rising edge		60		ns

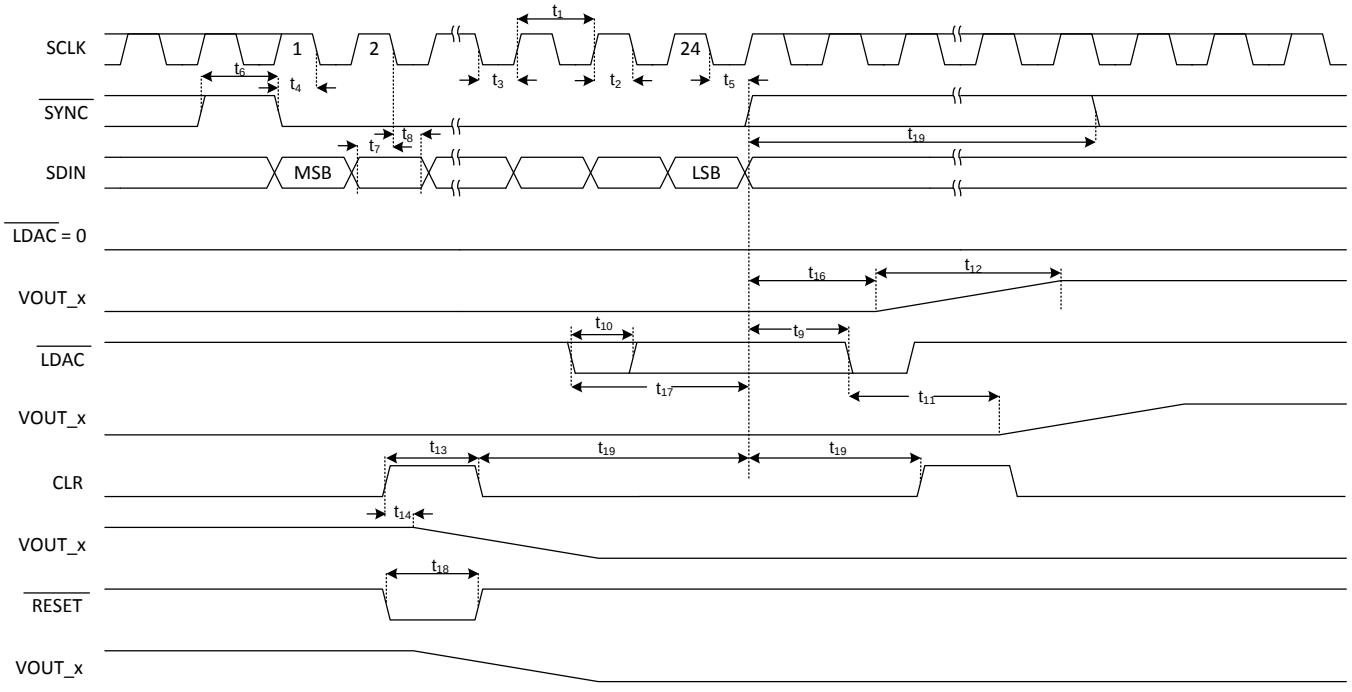


图 1. Write Mode Timing

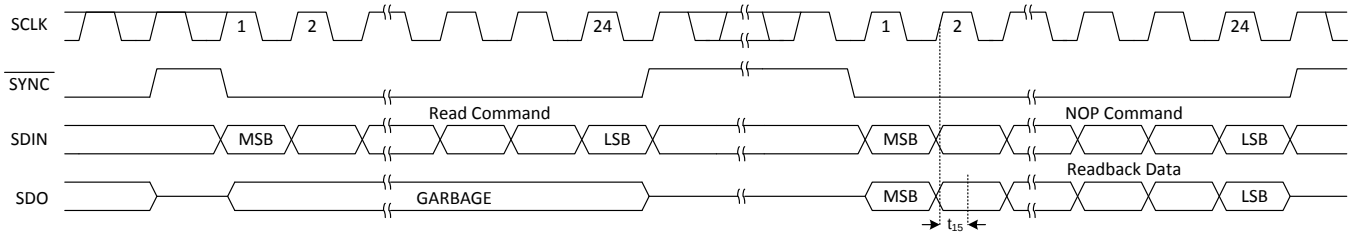


图 2. Readback Mode Timing

7.7 Typical Characteristics

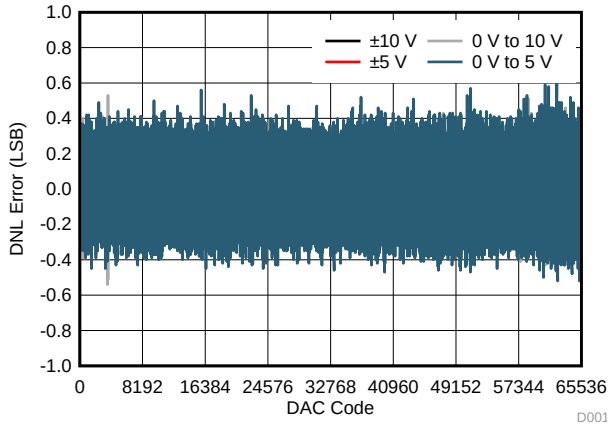


图 3. VOUT DNL vs Code (DC/DC Enabled)

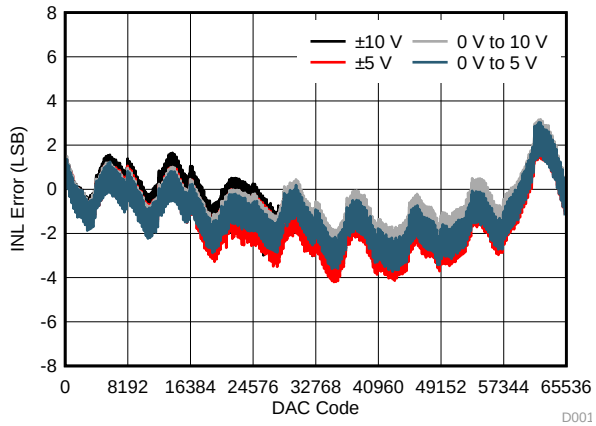


图 4. VOUT INL vs Code (DC/DC Enabled)

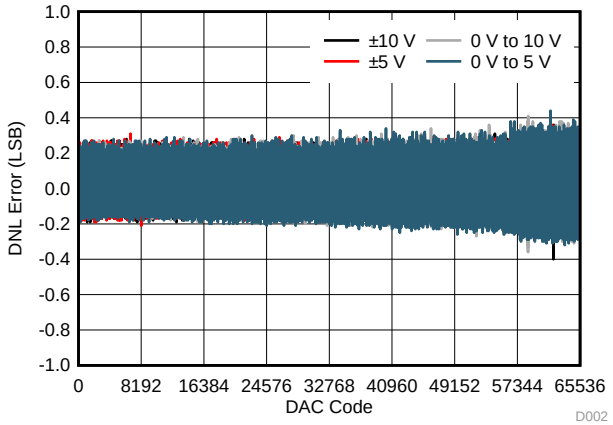


图 5. VOUT DNL vs Code (DC/DC Disabled)

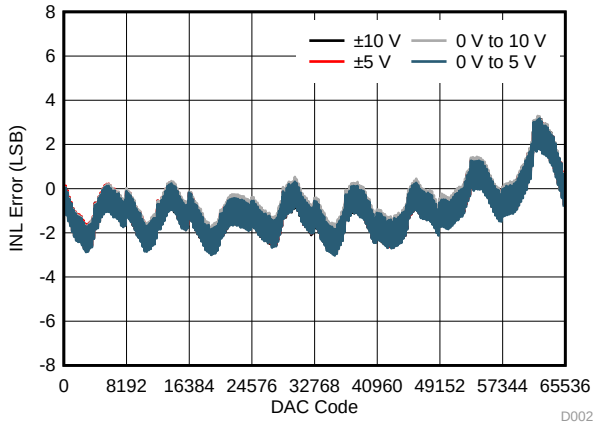


图 6. VOUT INL vs Code (DC/DC Disabled)

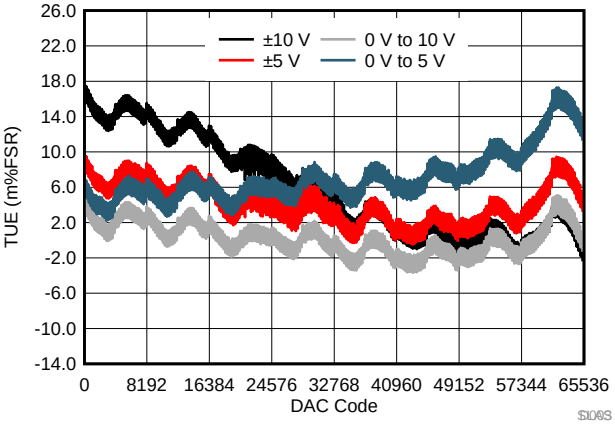


图 7. VOUT TUE vs Code (DC/DC Enabled)

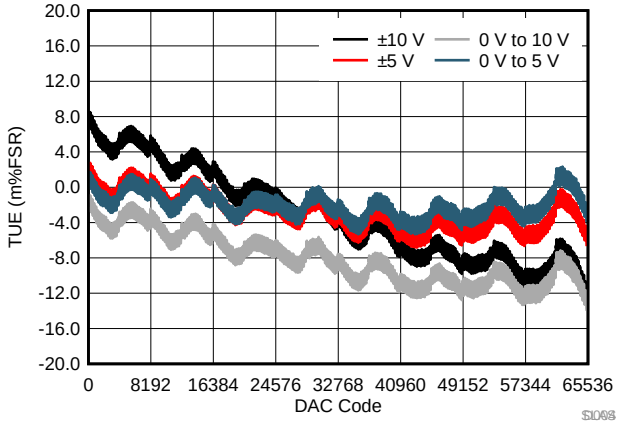


图 8. VOUT TUE vs Code (DC/DC Disabled)

Typical Characteristics (接下页)

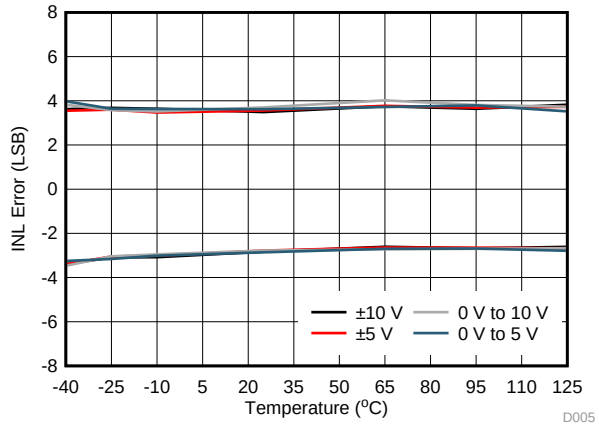


图 9. VOUT INL vs Temperature

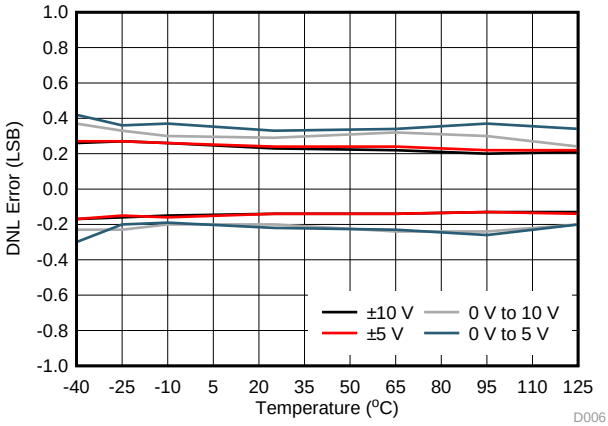


图 10. VOUT DNL vs Temperature

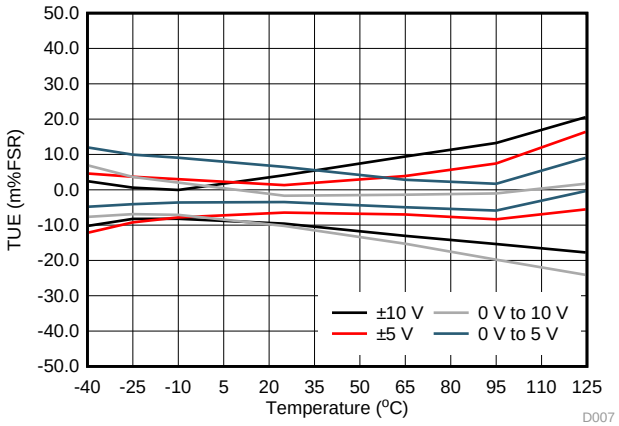


图 11. VOUT TUE vs Temperature

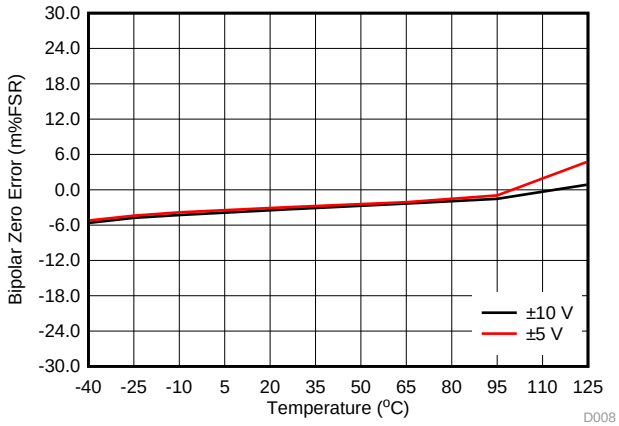


图 12. VOUT Bipolar Zero Error vs Temperature

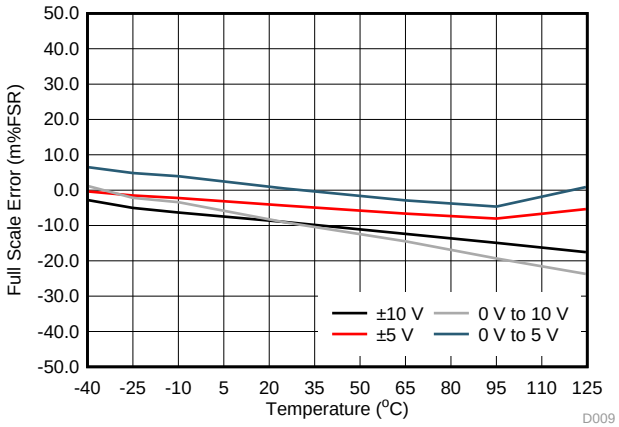


图 13. VOUT Full-Scale Error vs Temperature

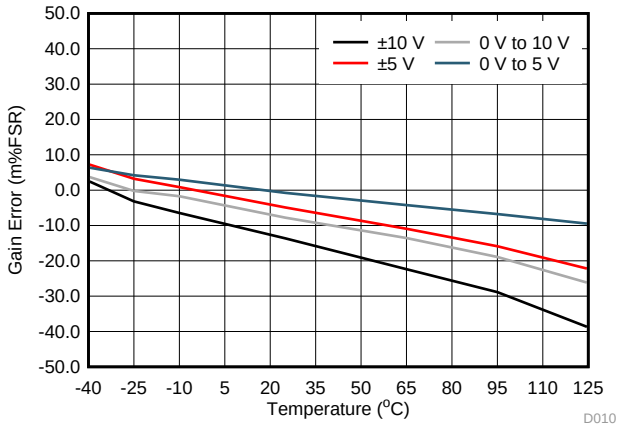


图 14. VOUT Gain Error vs Temperature

Typical Characteristics (接下页)

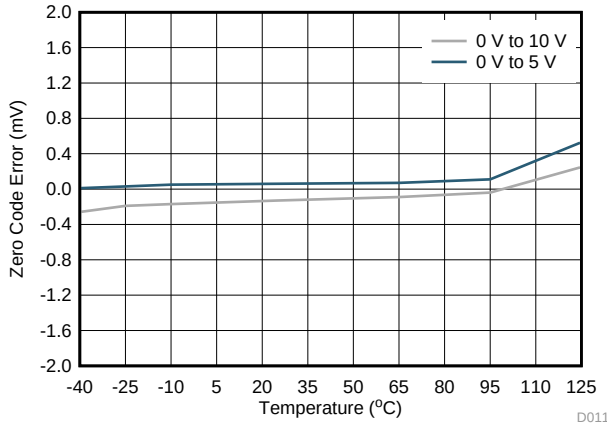


图 15. VOUT Zero-Code Error vs Temperature

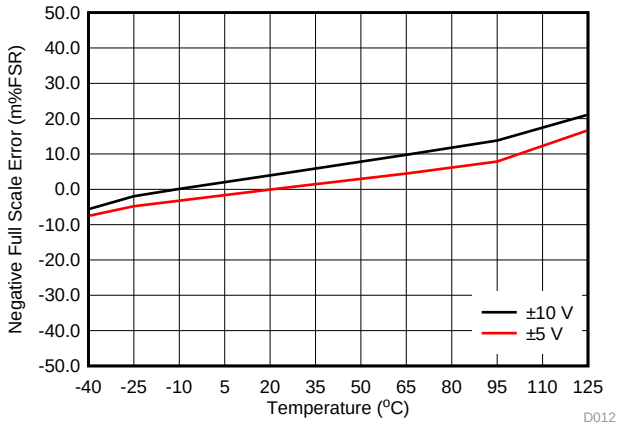


图 16. VOUT Negative Full-Scale Error vs Temperature

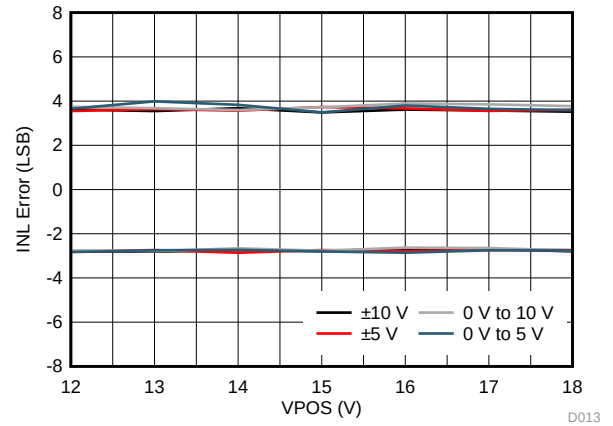


图 17. VOUT INL vs VPOS

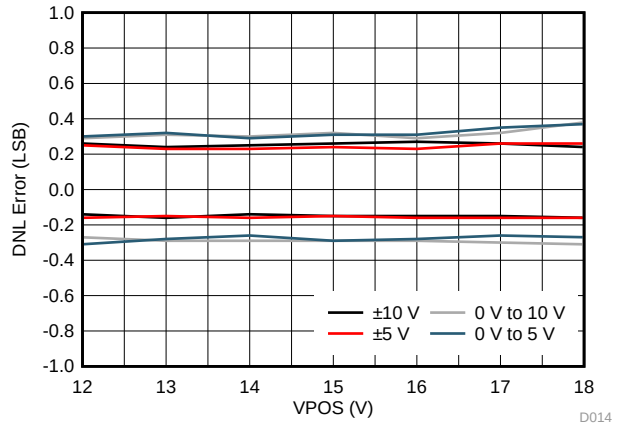


图 18. VOUT DNL vs VPOS

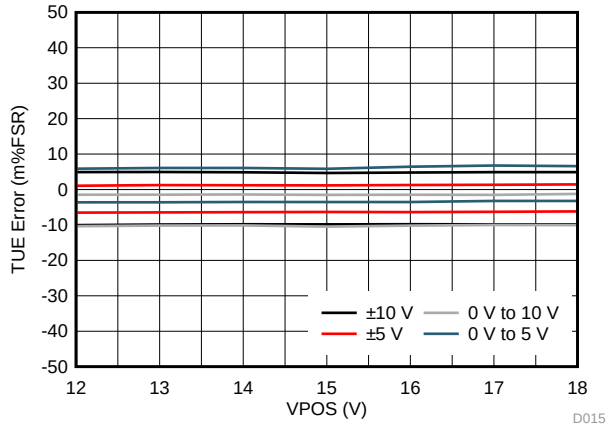


图 19. VOUT TUE vs VPOS

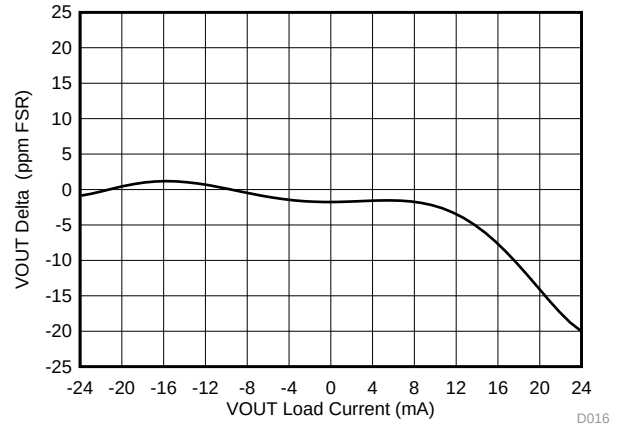


图 20. VOUT Load Regulation (SCLM = 11)

Typical Characteristics (接下页)

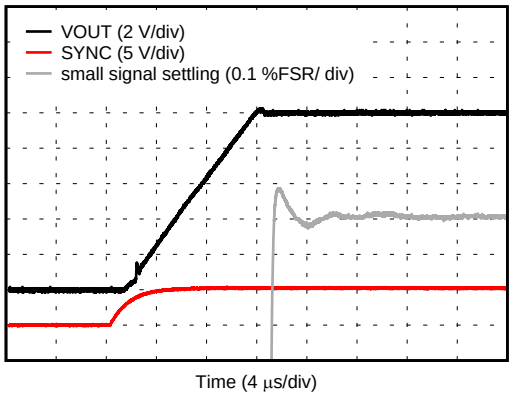


图 21. VOUT Settling Time, Rising Signal

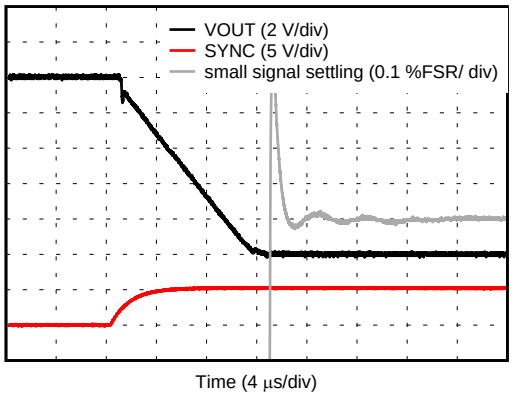


图 22. VOUT Settling Time, Falling Signal

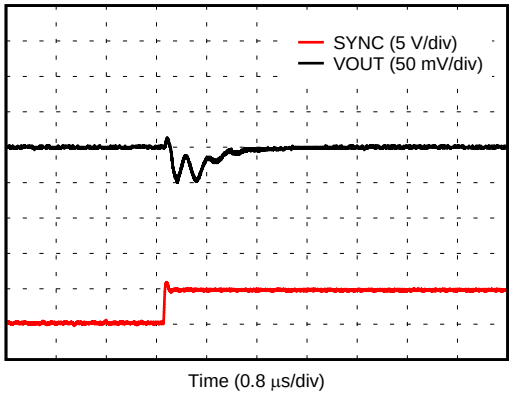


图 23. VOUT Major-Carry Glitch, Positive

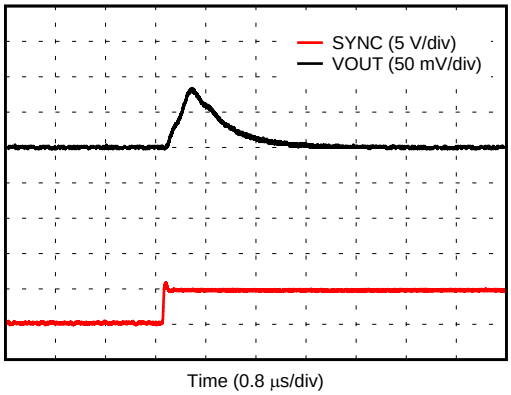


图 24. VOUT Major-Carry Glitch, Negative

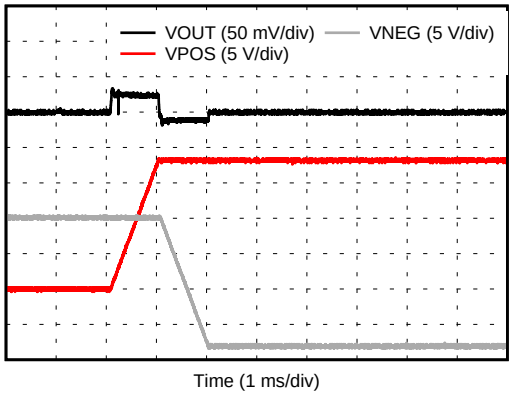


图 25. VOUT Power-On Glitch

Typical Characteristics (接下页)

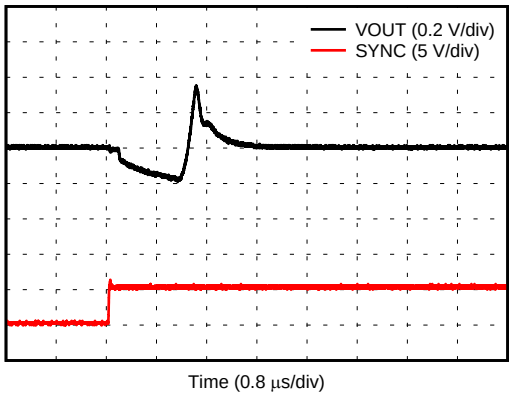


图 26. VOUT Output-Enable Glitch

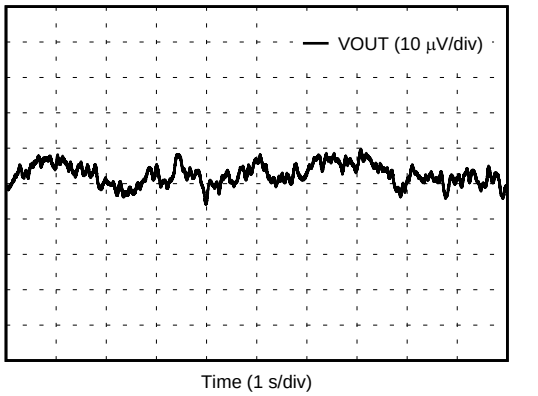


图 27. VOUT Noise (DC/DC Disabled)

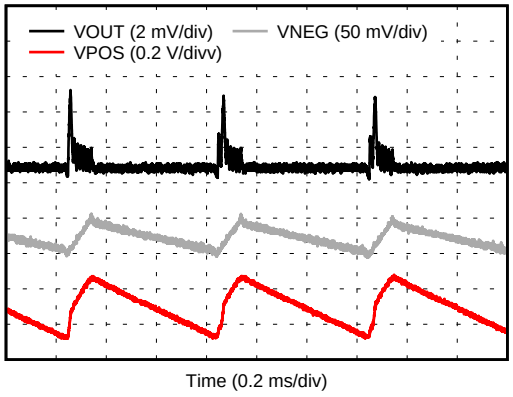


图 28. VOUT DC/DC Ripple (50kHz First-Order Low-Pass Filter)

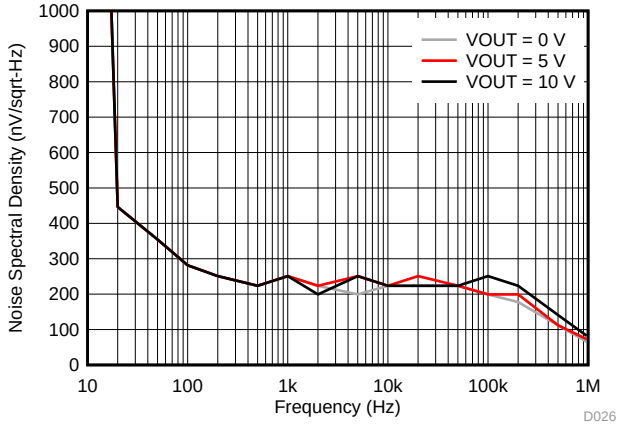


图 29. VOUT Noise Spectral Density (DC/DC Disabled)

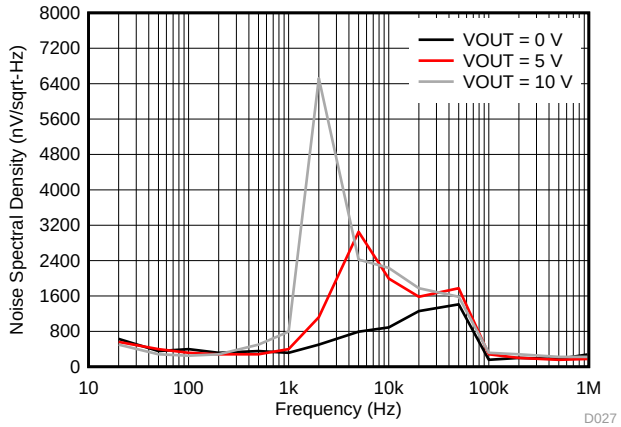


图 30. VOUT Noise Spectral Density (DC/DC Enabled)

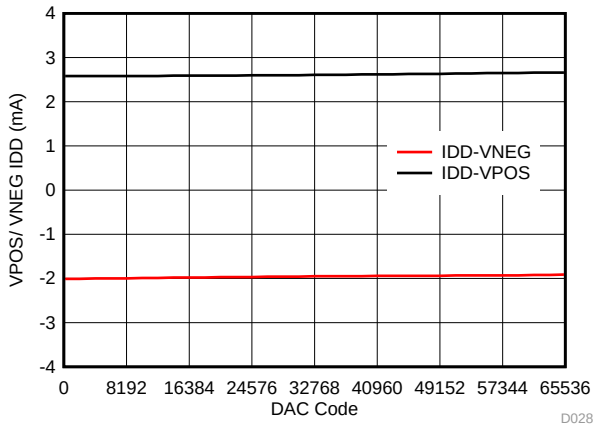


图 31. VOUT Quiescent Current vs Code (No Load)

Typical Characteristics (接下页)

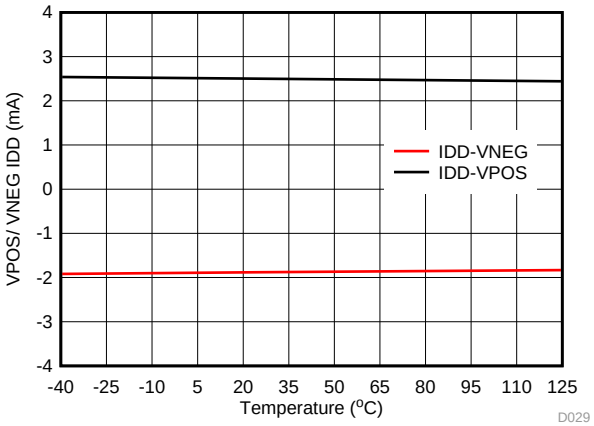


图 32. VOUT Quiescent Current vs Temperature (No Load)

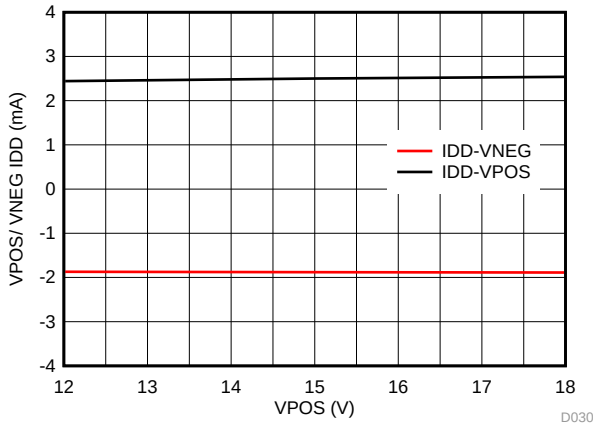


图 33. VOUT Quiescent Current vs VPOS (No Load)

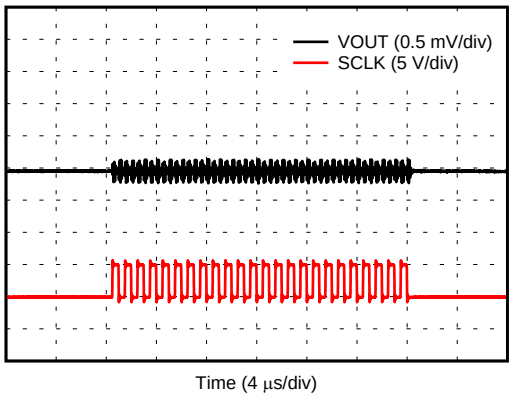


图 34. VOUT Digital Feedthrough

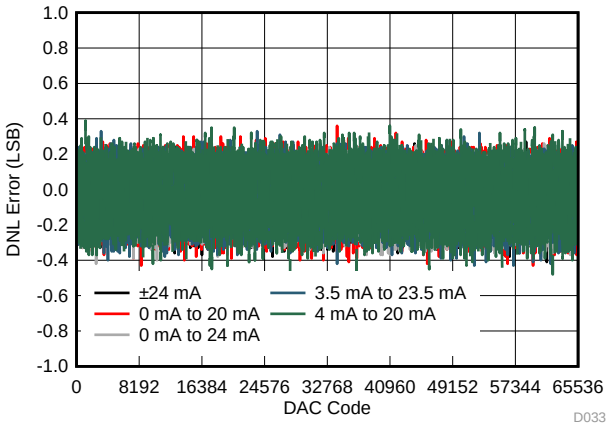


图 35. IOUT DNL vs Code (DC/DC Enabled)

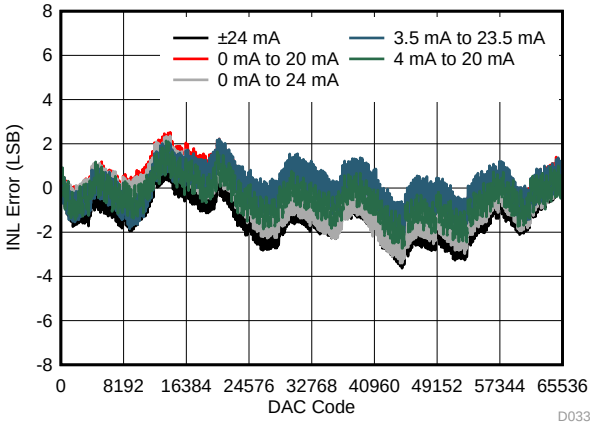


图 36. IOUT INL vs Code (DC/DC Enabled)

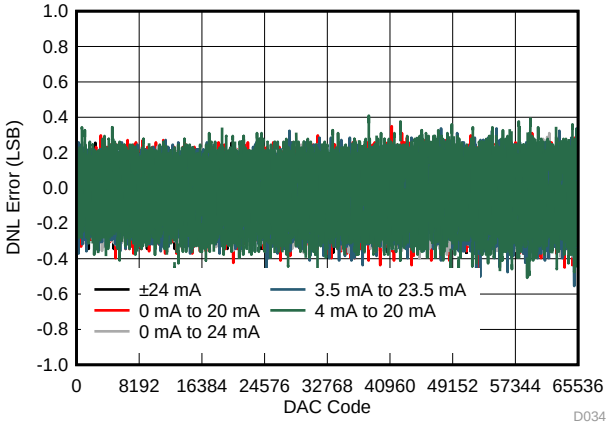


图 37. IOUT DNL vs Code (DC/DC Disabled)

Typical Characteristics (接下页)

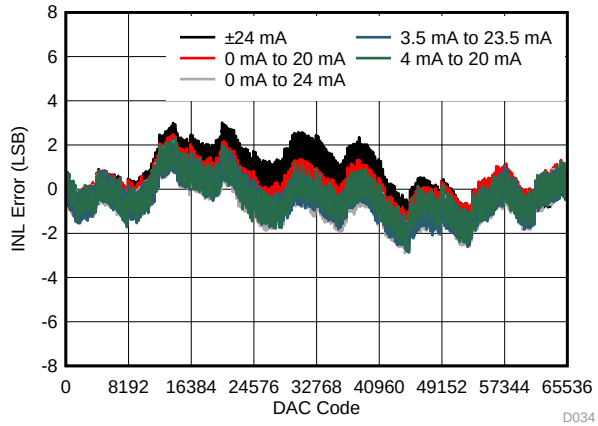


图 38. IOUT INL vs Code (DC/DC Disabled)

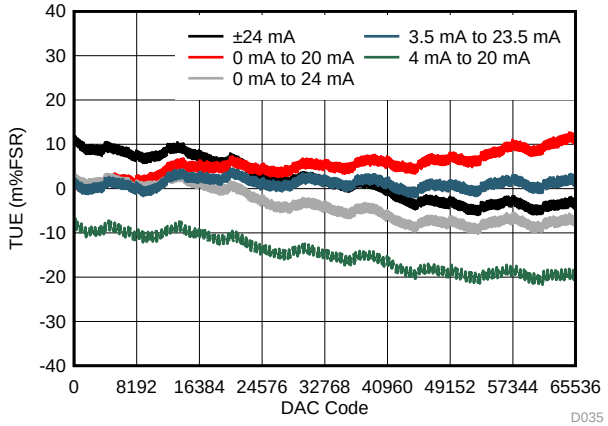


图 39. IOUT TUE vs Code (DC/DC Enabled)

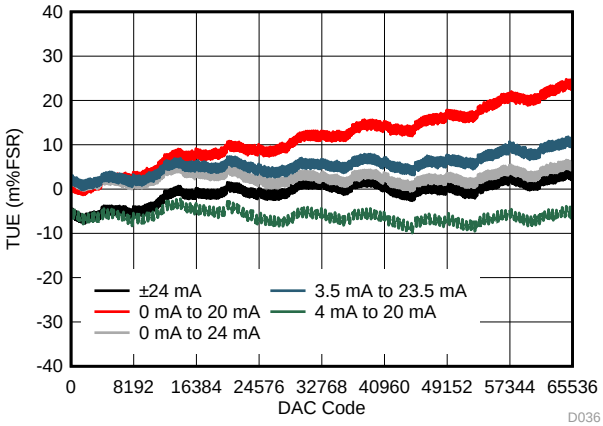


图 40. IOUT TUE vs Code (DC/DC Enabled)

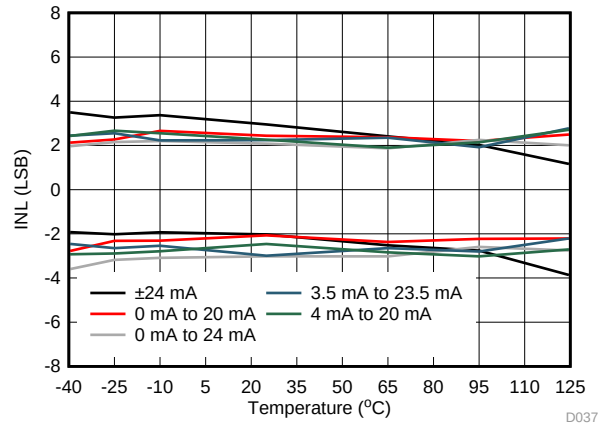


图 41. IOUT INL vs Temperature

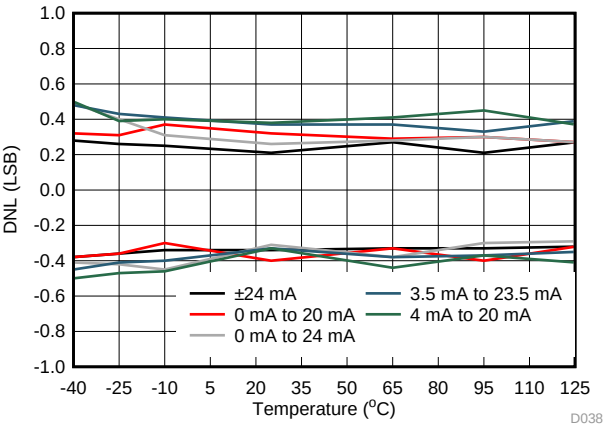


图 42. IOUT DNL vs Temperature

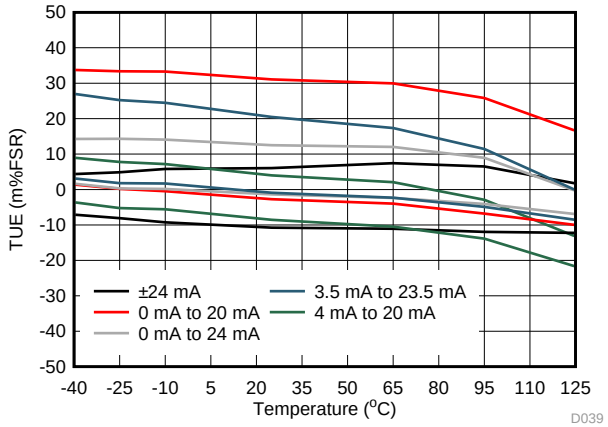


图 43. IOUT TUE vs Temperature

Typical Characteristics (接下页)

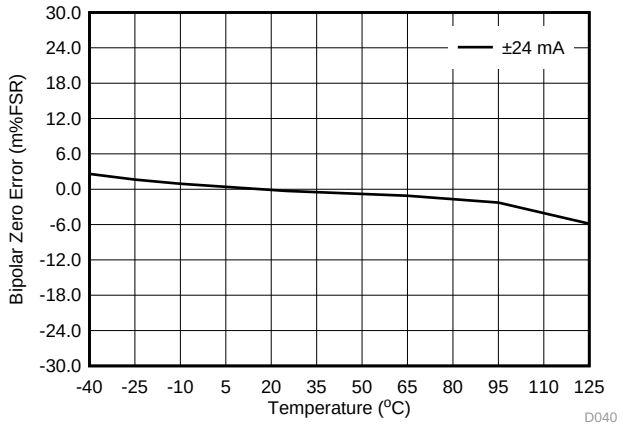


图 44. IOUT Bipolar Zero Error vs Temperature

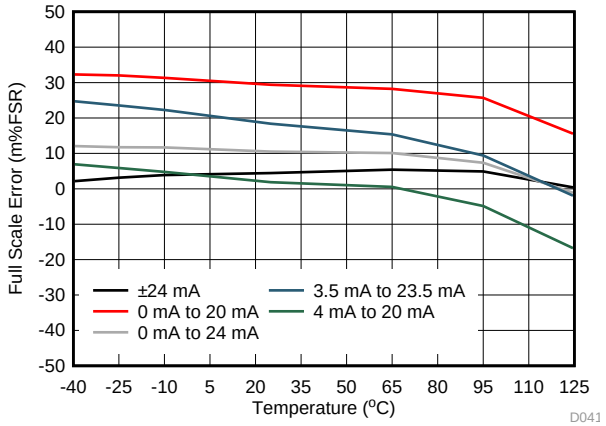


图 45. IOUT Full-Scale Error vs Temperature

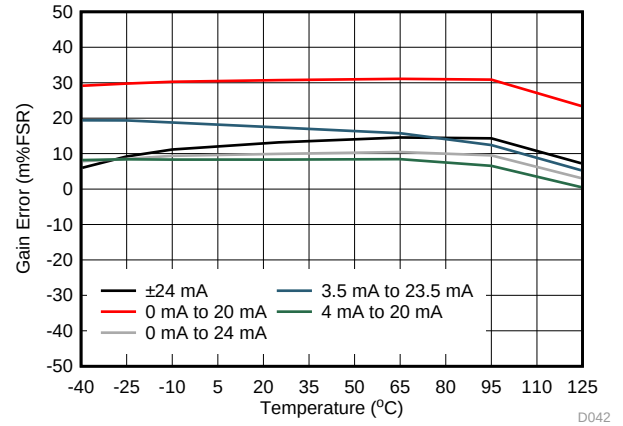


图 46. IOUT Gain Error vs Temperature

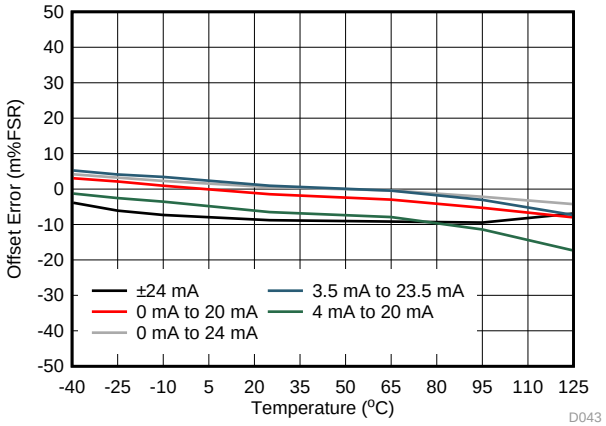


图 47. IOUT Offset Error vs Temperature

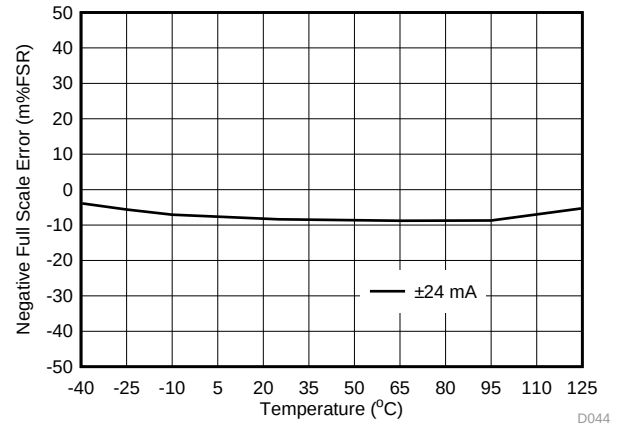


图 48. IOUT Negative Full-Scale Error vs Temperature

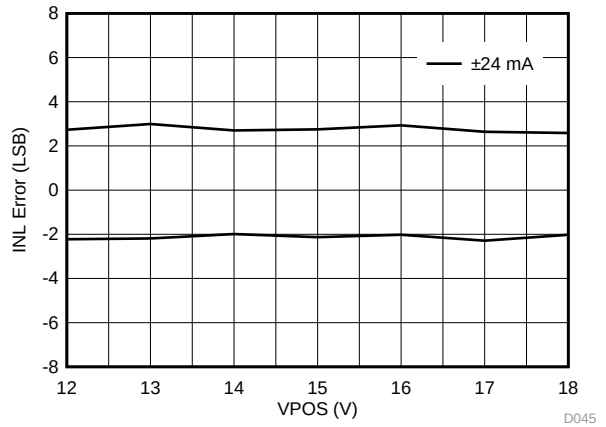


图 49. IOUT Bipolar Range INL vs VPOS

Typical Characteristics (接下页)

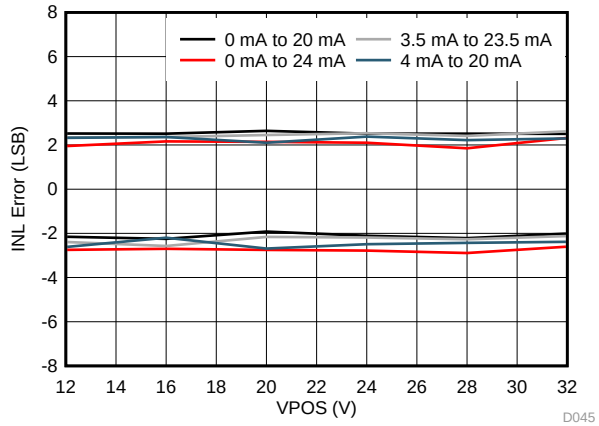


图 50. IOUT Unipolar Ranges INL vs VPOS

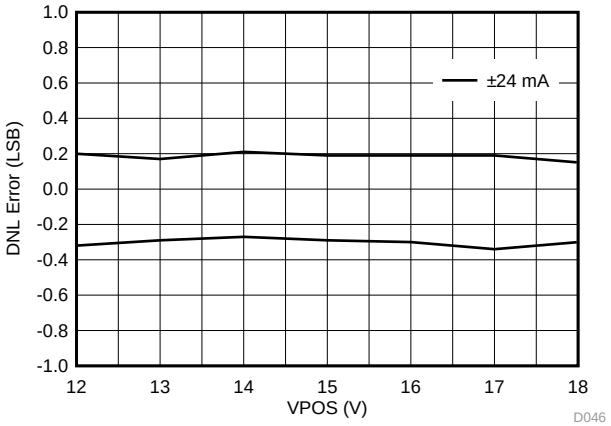


图 51. IOUT Bipolar Range DNL vs VPOS

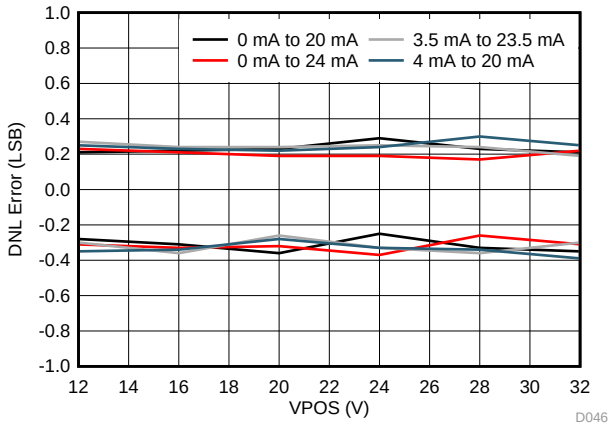


图 52. IOUT Unipolar Ranges DNL vs VPOS

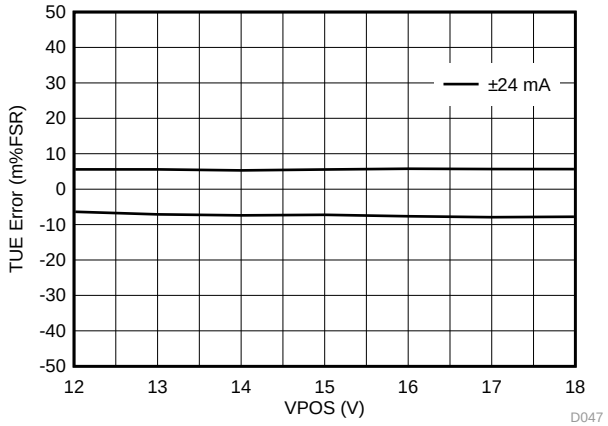


图 53. IOUT Bipolar Range TUE vs VPOS

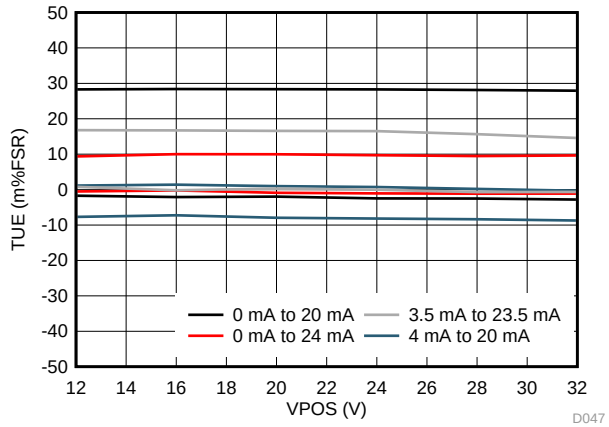


图 54. IOUT Unipolar Ranges TUE vs VPOS

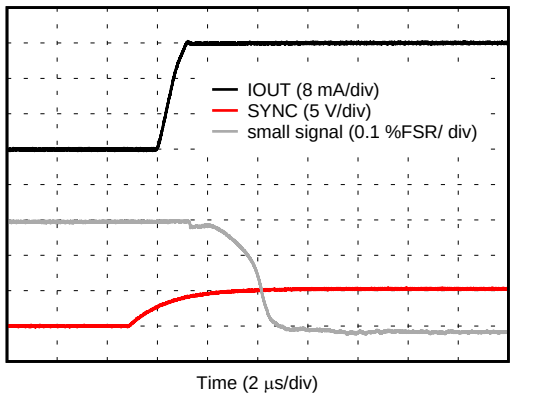


图 55. IOUT Settling Time, Rising Signal

Typical Characteristics (接下页)

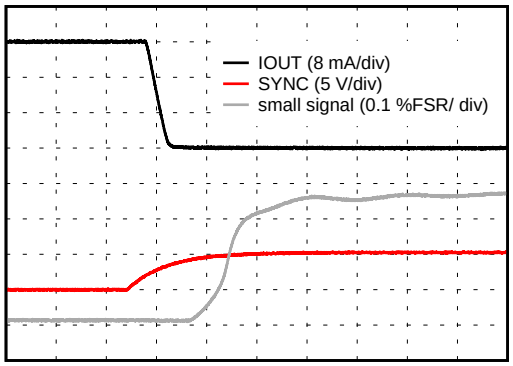


图 56. IOUT Settling Time, Falling Signal

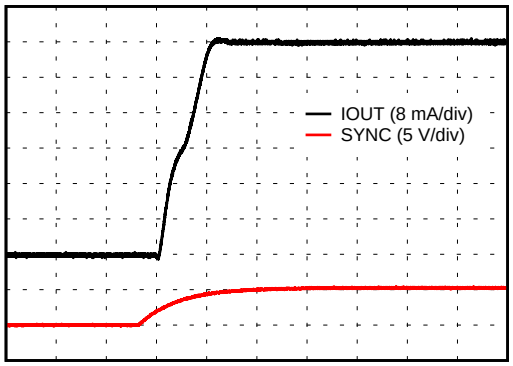


图 57. IOUT Settling Time, Bipolar Range, Rising Signal

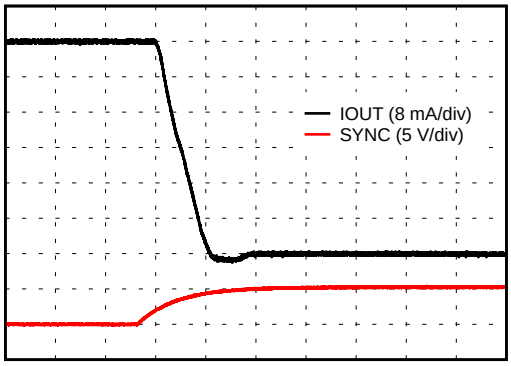


图 58. IOUT Settling Time, Bipolar Range, Falling Signal

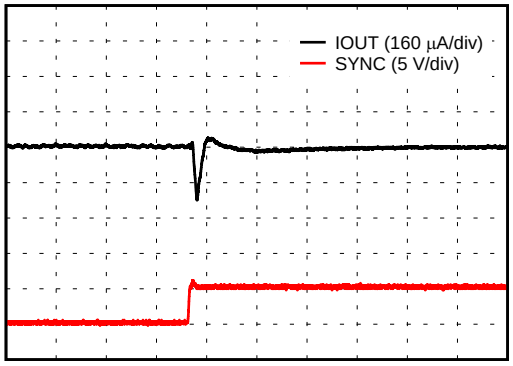


图 59. IOUT Major Carry Glitch, Positive

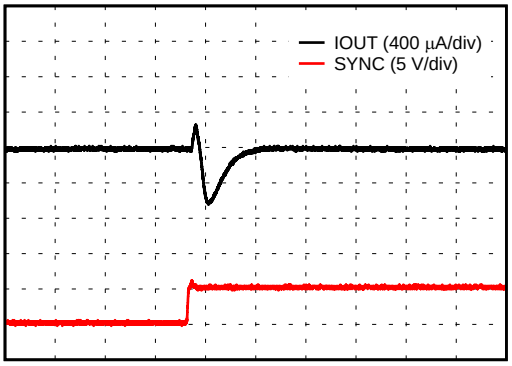


图 60. IOUT Major Carry Glitch, Negative

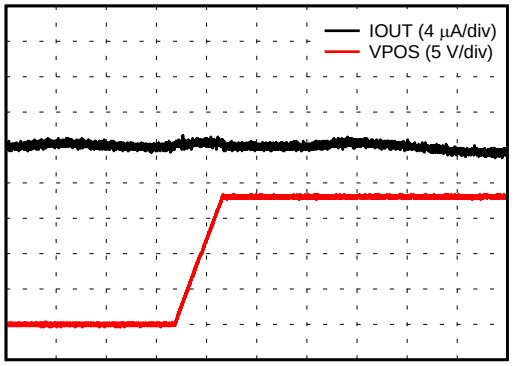


图 61. IOUT Power On Glitch

Typical Characteristics (接下页)

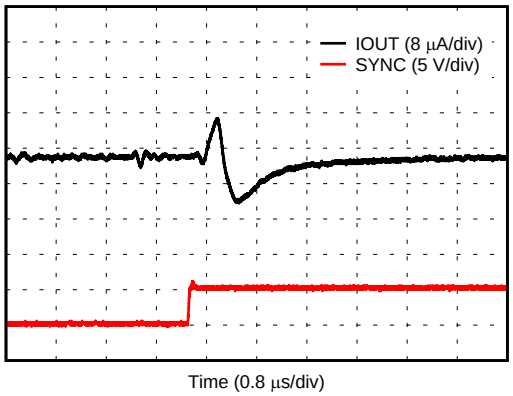


图 62. IOUT Output Enable Glitch

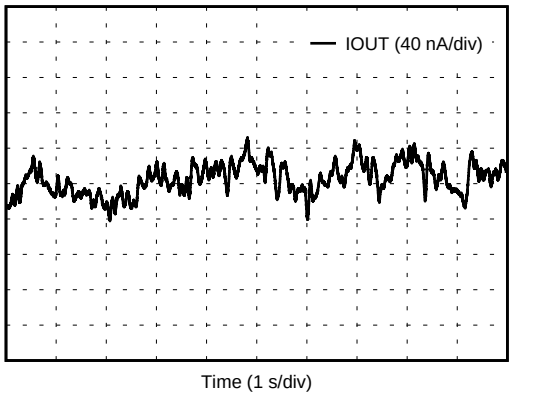


图 63. IOUT Noise (DC/DC Disabled)

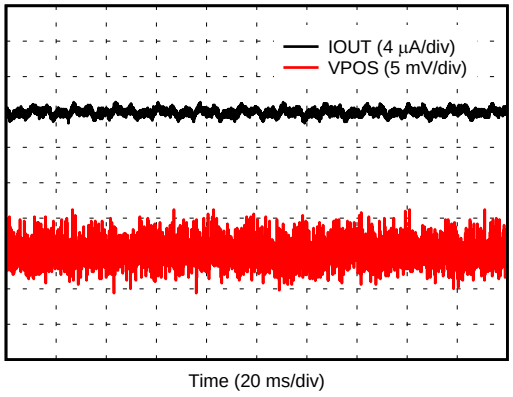


图 64. IOUT DC/DC Ripple (50kHz First-Order Low-Pass Filter)

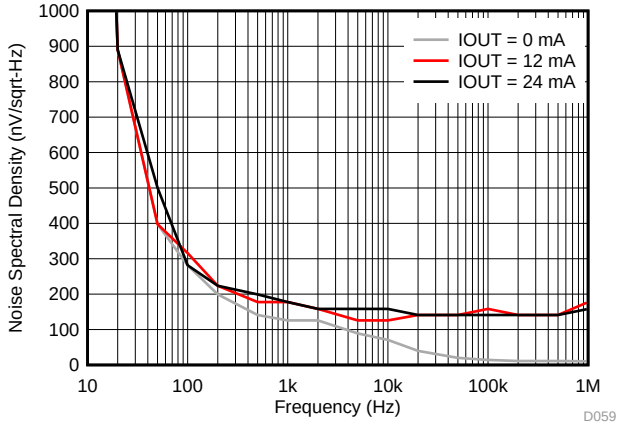


图 65. IOUT Noise Spectral Density (DC/DC Disabled)

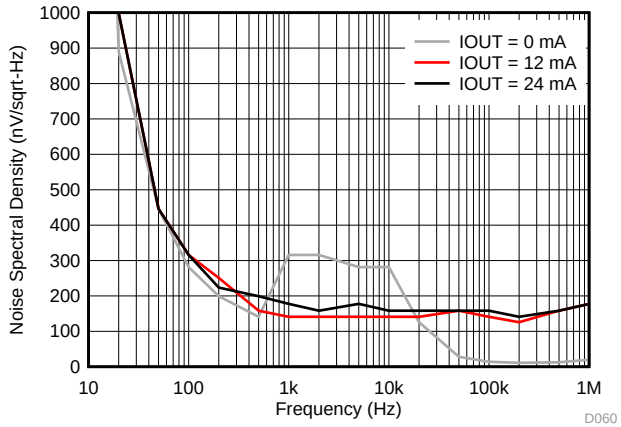


图 66. IOUT Noise Spectral Density (DC/DC Enabled)

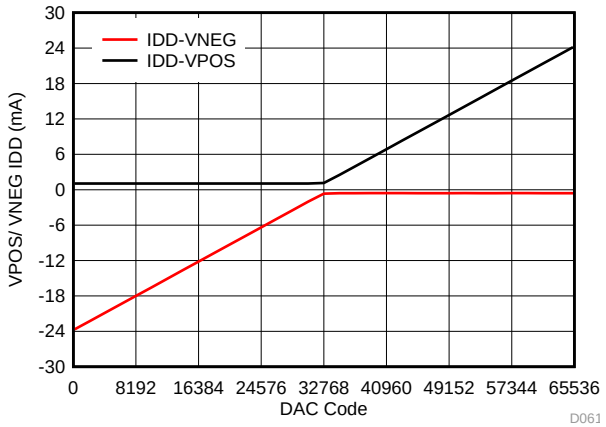


图 67. IOUT Quiescent Current vs Code, Bipolar Range

Typical Characteristics (接下页)

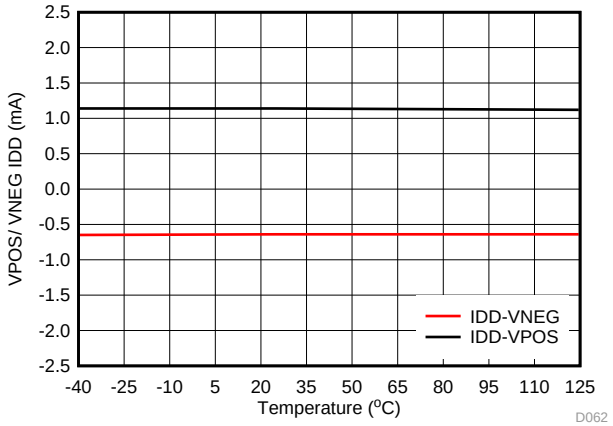


图 68. IOUT Quiescent Current vs Temperature

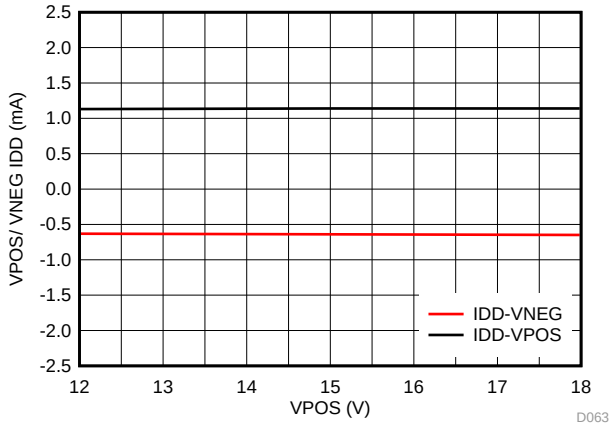


图 69. IOUT Quiescent Current vs VPOS

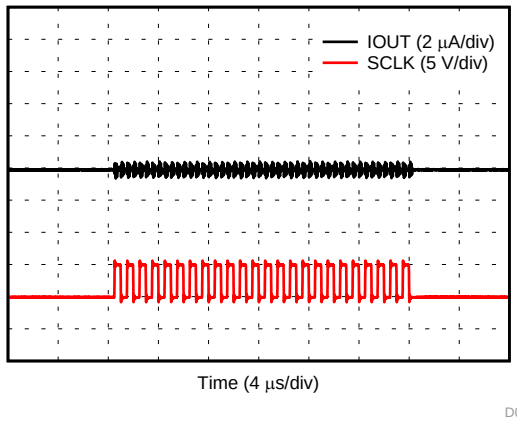


图 70. IOUT Digital Feed-Through

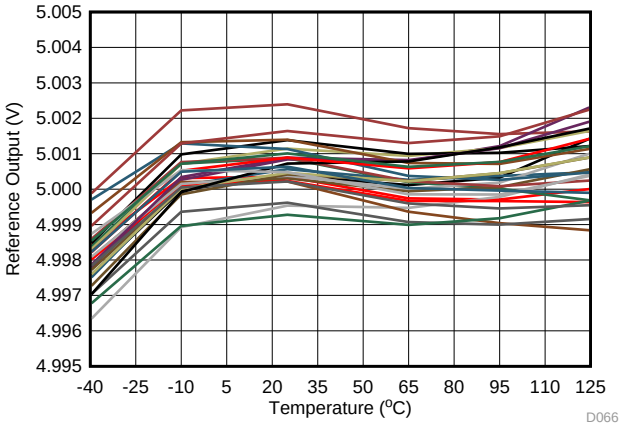


图 71. Internal Reference Voltage vs Temperature

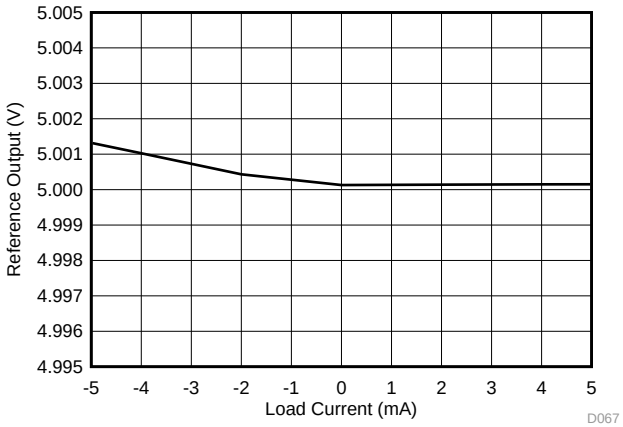


图 72. Internal Reference Voltage vs Load

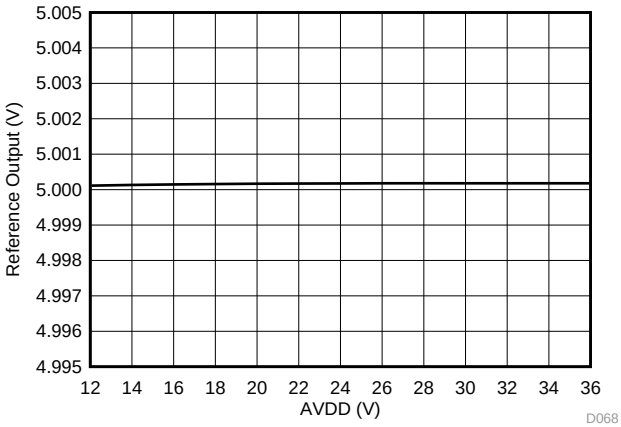


图 73. Internal Reference Voltage vs AVDD

Typical Characteristics (接下页)

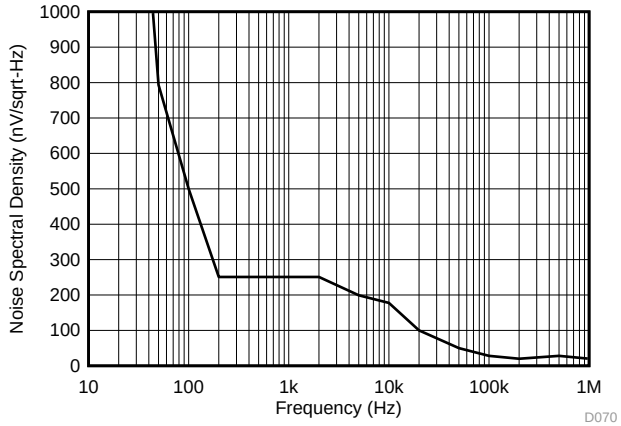


图 74. Internal Reference Voltage Noise Spectral Density (DC/DC Disabled)

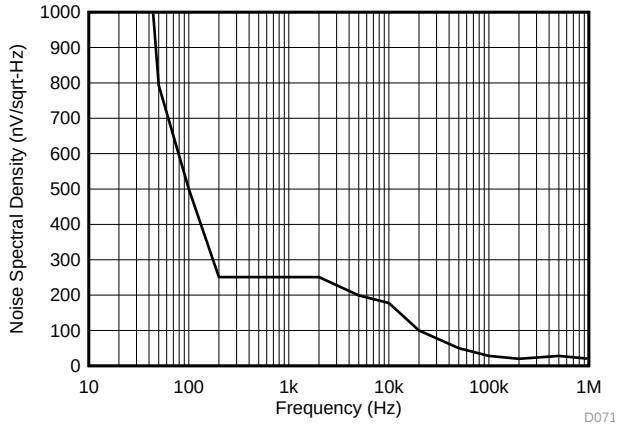


图 75. Internal Reference Voltage Noise Spectral Density (DC/DC Enabled)

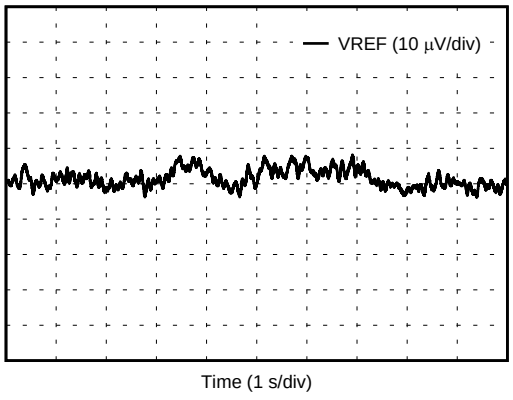


图 76. Internal Reference Voltage Noise (DC/DC Disabled)

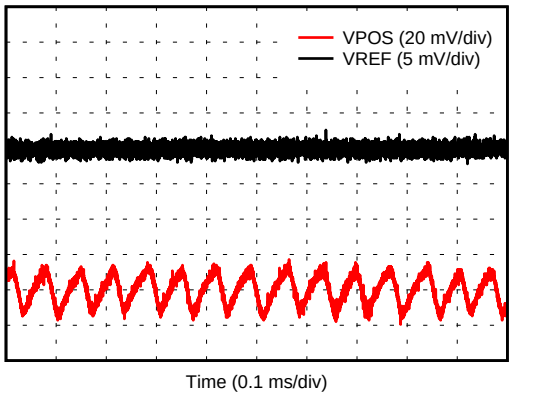


图 77. Internal Reference Voltage DC/DC Ripple

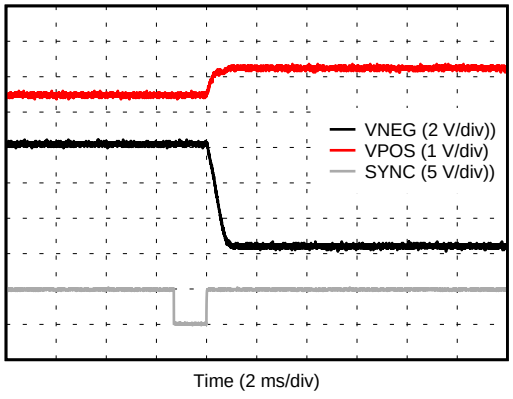


图 78. VPOS & VNEG Enable Settling Time

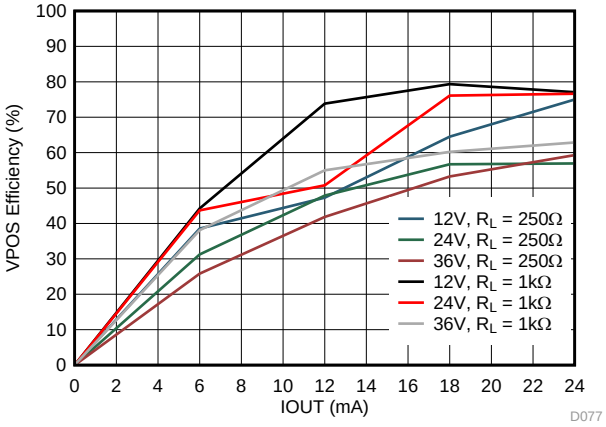


图 79. IOUT VPOS Efficiency

Typical Characteristics (接下页)

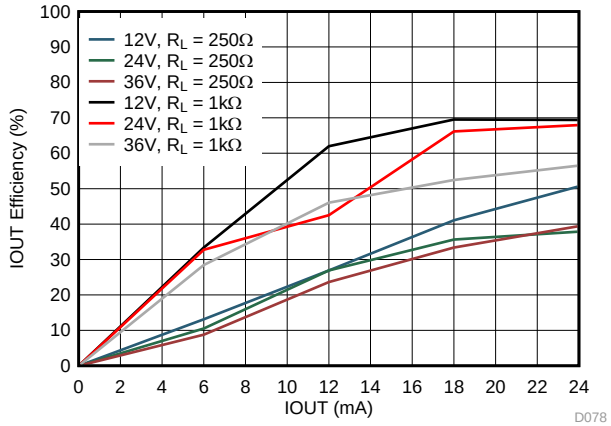


图 80. IOUT DC/DC Efficiency

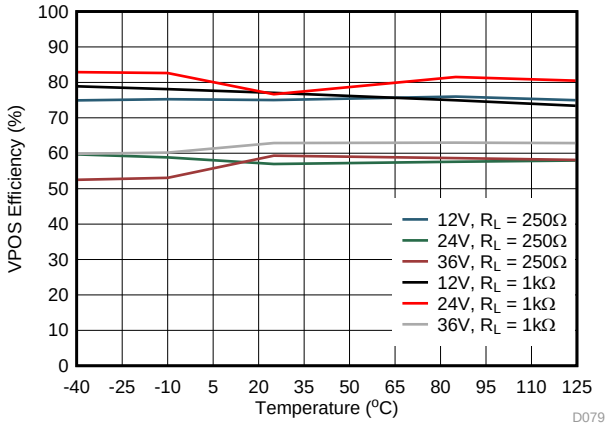


图 81. VPOS Efficiency vs Temperature

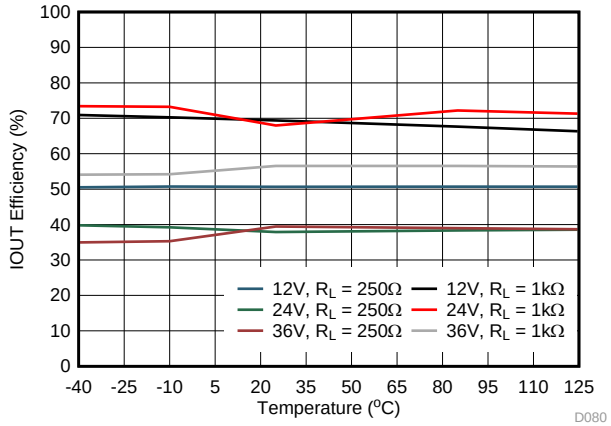


图 82. IOUT DC/DC Efficiency vs Temperature

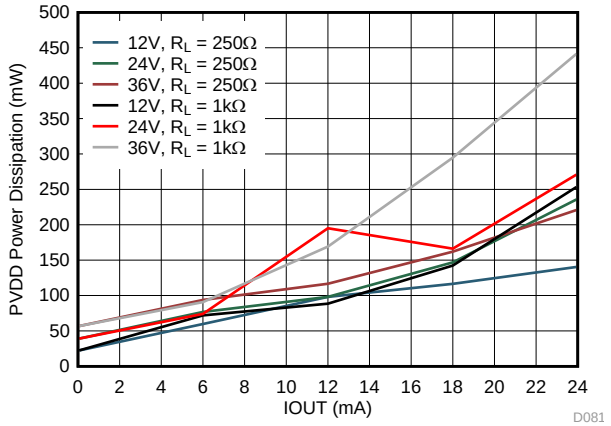


图 83. IOUT Power Dissipation vs Load

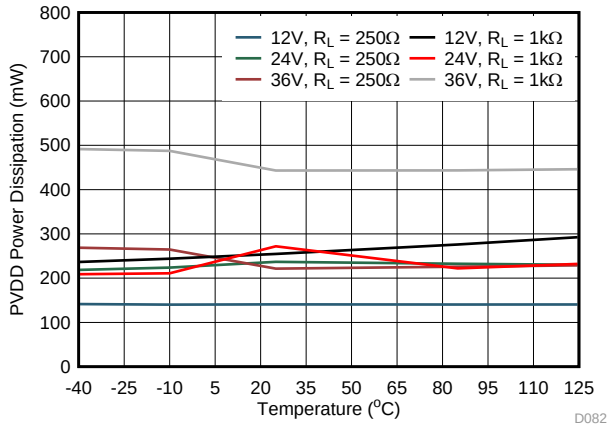


图 84. IOUT Power Dissipation vs Temperature

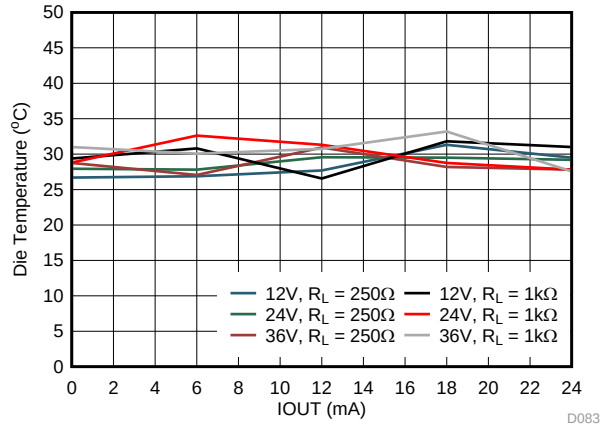


图 85. IOUT Die Temperature vs Load

Typical Characteristics (接下页)

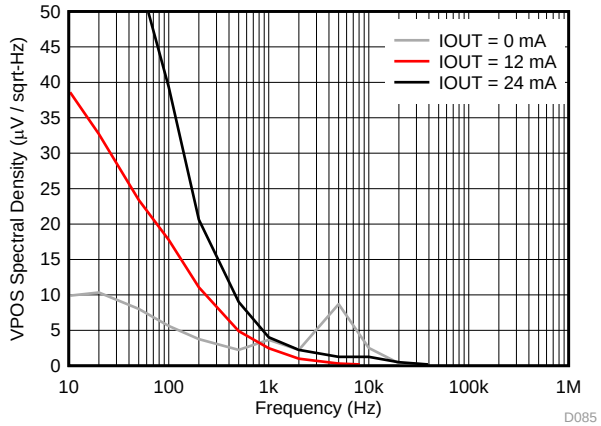


图 86. IOUT VPOS Noise Spectral Density

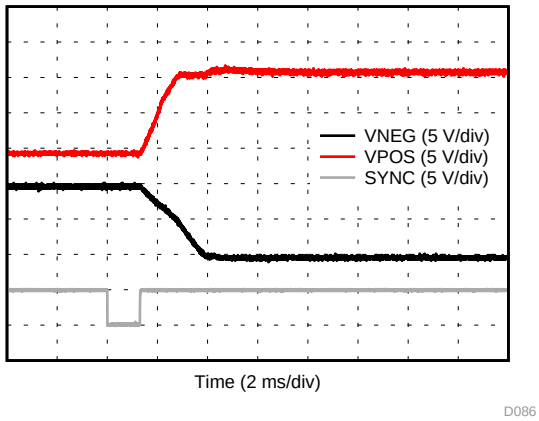


图 87. VOUT Enable VPOS and VNEG Settling Time

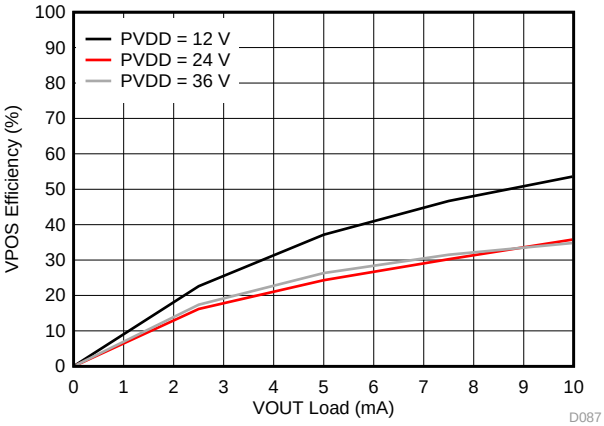


图 88. VOUT VPOS Efficiency vs Load

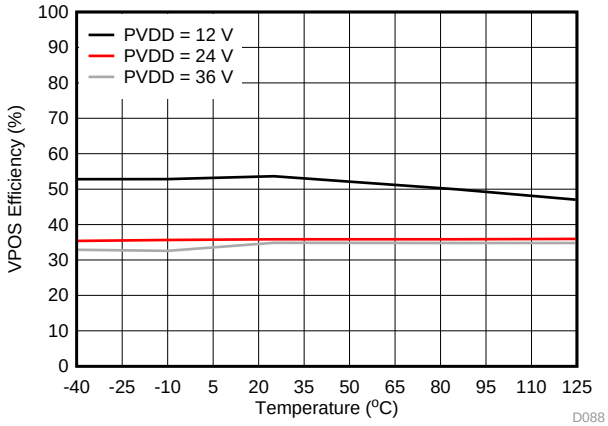


图 89. VOUT VPOS Efficiency vs Temperature

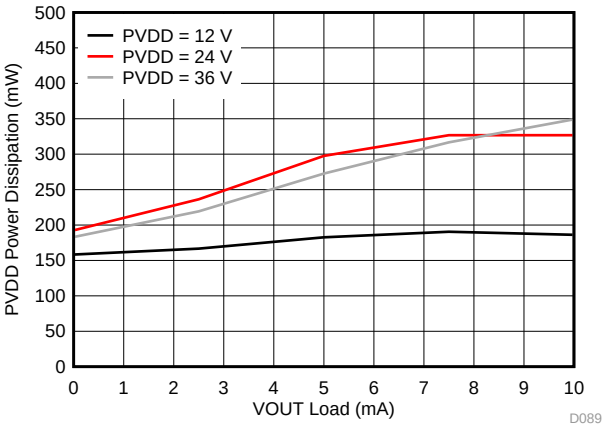


图 90. VOUT Power Dissipation vs Load

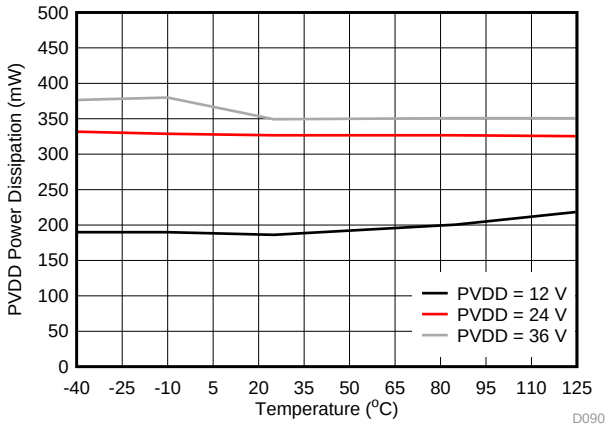


图 91. VOUT Power Dissipation vs Temperature

Typical Characteristics (接下页)

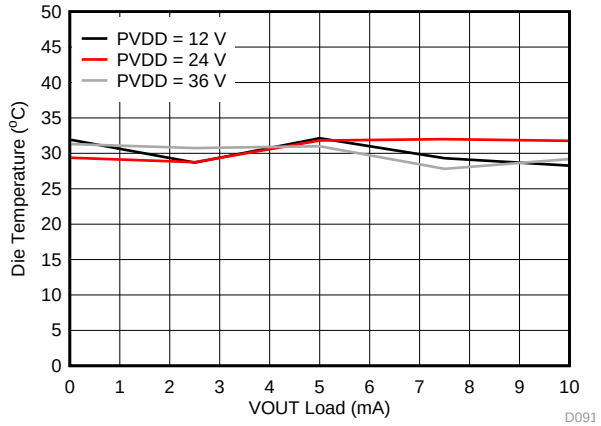


图 92. VOUT Die Temperature vs Load

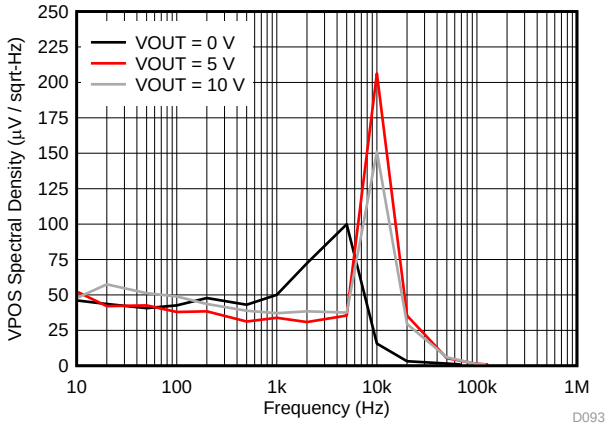


图 93. VOUT VPOS Noise Spectral Density

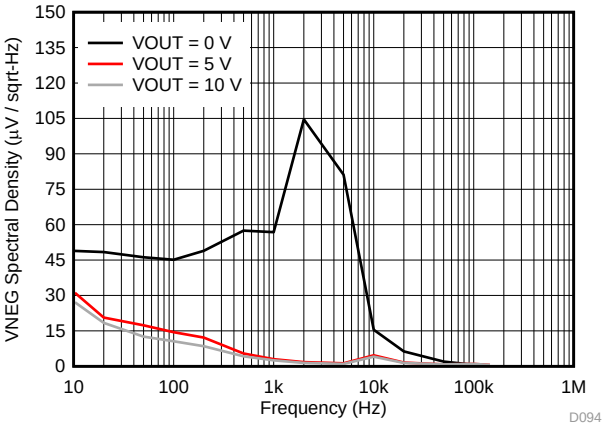


图 94. VPOS VNEG Noise Spectral Density

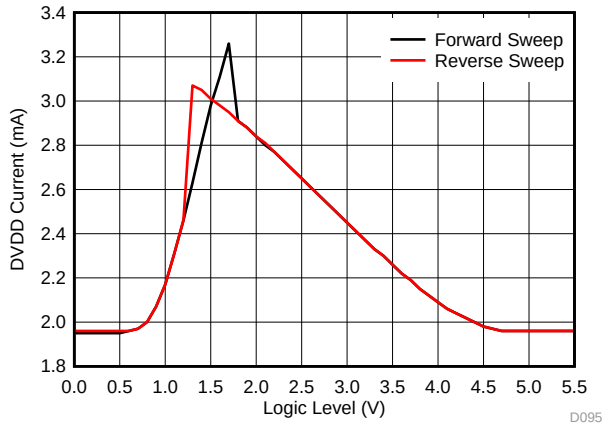


图 95. DVDD Iq vs Logic Level

8 Detailed Description

8.1 Overview

The DAC8771 consists of a resistor-string digital-to-analog converter (DAC) followed by buffer amplifiers. The output of the buffer drives the current output stage and the voltage output amplifier. The resistor-string section is simply a string of resistors, each of value R, from REFIN to GND, as Functional Block Diagram illustrates. This type of architecture ensures DAC monotonicity. The 16-bit binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed into the output amplifier. The current output stage converts the output from the string to current using a precision current source. The voltage output provides a voltage output to the external load. When the current output stage is disabled the IOUT pin is Hi-Z. When the voltage output stage is disabled, the output impedance is controlled by the POC bit, by default set to 30 kΩ. After power-on, both output stages are disabled. The DAC8771 also contains a Buck-Boost converter which can be used to generate the power supply for the current output stage and voltage output amplifier.

8.2 Functional Block Diagram

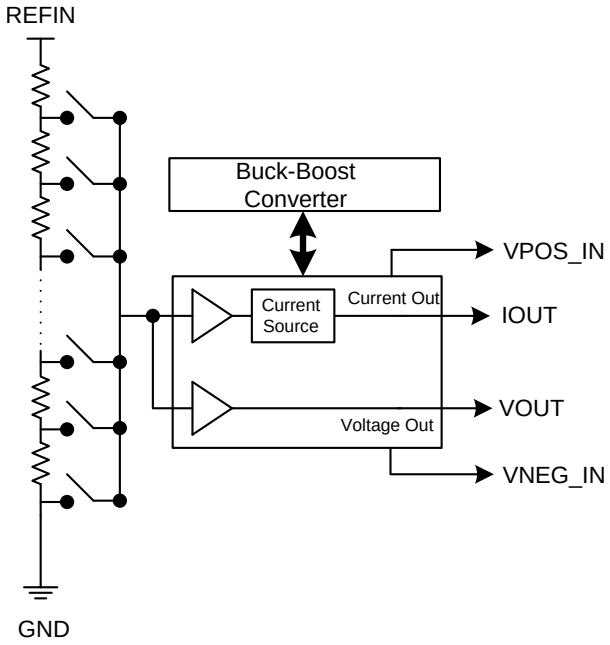


图 96. General Architecture

8.3 Feature Description

8.3.1 Current Output Stage

The current output stage consists of a pre-conditioner and a precision current source as shown in 图 97. This stage provides a current output according to the DAC code. The output range can be programmed as 0 mA - 20 mA, 0 mA - 24 mA, 4 mA - 20 mA, 3.5 mA - 23.5 mA, or ±24 mA. In the current output mode, the maximum compliance voltage on pin IOUT is between (-|VNEG_IN| + 3 V) ≤ $|V_{IOUT}|$ ≤ (VPOS_IN – 3 V). When in unipolar current output modes the low-side of the compliance voltage limit is replaced by GND. This compliance voltage is automatically maintained when the Buck-Boost converter is used to generate these supplies (see Buck-Boost Converter section). However, when using an external supply for VPOS_IN pin (Buck-Boost converter disabled), the VPOS_IN and VNEG_IN supplies should be chosen such that this compliance voltage is maintained.

Feature Description (接下页)

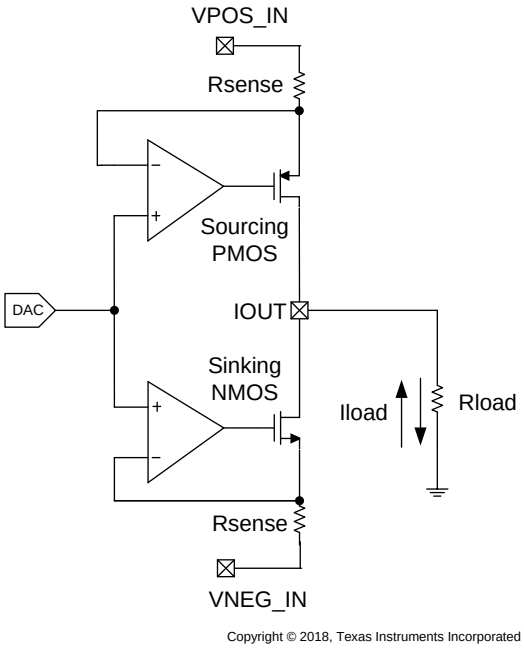


图 97. Current Output

The 16 bit data can be written to DAC8771 using address 0x05 (DAC data register, 表 4 and 表 5).

For a 0-mA to 20-mA output range:

$$IOUT = 20mA\ x \left[\frac{CODE}{2^N}\right] \quad (1)$$

For a 0-mA to 24-mA output range:

$$IOUT = 24mA\ x \left[\frac{CODE}{2^N}\right] \quad (2)$$

For a 3.5-mA to 23.5-mA output range:

$$IOUT = 20mA\ x \left[\frac{CODE}{2^N}\right] + 3.5mA \quad (3)$$

For a 4-mA to 20-mA output range:

$$IOUT = 16mA\ x \left[\frac{CODE}{2^N}\right] + 4mA \quad (4)$$

For a -24-mA to 24-mA output range:

$$IOUT = 40mA\ x \left[\frac{CODE}{2^N}\right] - 20mA \quad (5)$$

Where:

- *CODE* is the decimal equivalent of the code loaded to the DAC.
- *N* is the bits of resolution; 16

Feature Description (接下页)

8.3.2 Voltage Output Stage

The voltage output stage as conceptualized in 图 98 provides the voltage output according to the DAC code and the output range setting. The output range can be programmed as 0 V to +5 V or 0 V to +10 V for unipolar output mode, and ±5 V or ±10V for bipolar output mode. In addition, an option is available to increase the output voltage range by 20%. The output current drive can be up to 34 mA. The output stage has short-circuit current protection that limits the output current to 16 mA, this limit can be changed to 8 mA, 20 mA or 24 mA via writing bits 15 and 14 of address 0x04. The minimum headroom and foot-room for the voltage output stage is automatically maintained when the Buck-Boost converter is used to generate these supplies. However, when using an external supply for VPOS_IN and VNEG_IN pin (Buck-Boost converter disabled) the minimum headroom and foot-room as per must be maintained. In this case, the *Recommended Operating Conditions* shows the maximum allowable difference between VPOS_IN and VNEG_IN.

The voltage output is designed to drive capacitive loads of up to 1 μF. For loads greater than 20 nF, an external compensation capacitor must be connected between CCOMP and VOUT to keep the output voltage stable at the expense of reduced bandwidth and increased settling time. Note that, a step response (due to input code change) on the voltage output pin loaded with large capacitive load (> 20 nF) triggers the short circuit limit circuit of the output stage. This results in setting the short circuit alarm status bits. Therefore, it is recommended to use slew rate control for large step change, when the voltage output pin is loaded with high capacitive loads.

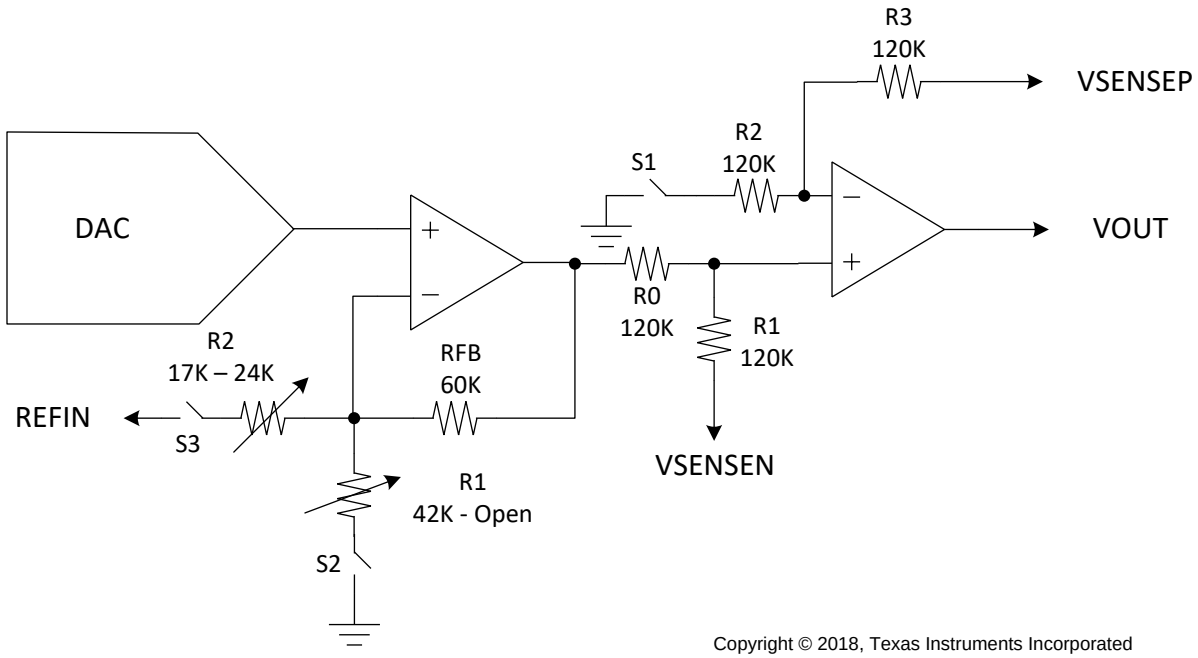


图 98. Voltage Output

The VSENSEP pin is provided to enable sensing of the load. Ideally, it is connected to VOUT at the terminals. Additionally, it can also be used to connect remotely to points electrically "nearer" to the load. This allows the internal output amplifier to ensure that the correct voltage is applied across the load as long as headroom is available on the power supply. However, if this line is cut, the amplifier loop would be broken. Therefore, an optional resistor can be used between VOUT and VSENSEP to prevent this.

The VSENSEN pin can be used to sense the remote ground and offset the VOUT pin accordingly. The VSENSEN pin can sense a maximum of ±7 V difference from the GND pin of the DAC8771.

The 16 bit data can be written to DAC8771 as shown in DAC data registers,表 4 and 表 5.

For unipolar output mode:

$$VOUT = VREFIN\ x\ GAIN\ x\ \left[\frac{CODE}{2^N}\right] \quad (6)$$

Feature Description (接下页)

For bipolar output mode:

$$VOUT = VREFIN\ x\ GAIN\ x\ \left[\frac{CODE}{2^N}\right] - \frac{GAIN\ x\ VREFIN}{2} \quad (7)$$

Where:

- *CODE* is the decimal equivalent of the code loaded to the DAC.
- *N* is the bits of resolution; 16
- VREFIN is the reference voltage; for internal reference, VREFIN = +5 V.
- *GAIN* is automatically selected for a desired voltage output range as shown in

8.3.3 Buck-Boost Converter

The DAC8771 includes a Buck-Boost Converter to minimize the power dissipation of the chip and provides significant system integration. This Buck-Boost converter is based on a Single Inductor Multiple Output (SIMO) architecture and requires a single inductor to simultaneously generate all the analog power supplies required by the chip. The Buck-Boost converter uses three on-chip switches (shown in 图 99) which are synchronously controlled via current mode control logic. The DC/DC converter is designed to work in discontinuous conduction mode (DCM) with an external inductor of value 100 µH connected between LN and LP pins (see *Buck-Boost Converter External Component Selection* section). The peak inductor current inductor is limited to a value of 0.5 A internally.

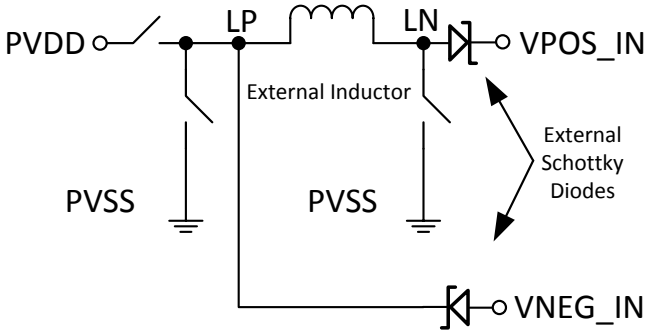


图 99. Buck-Boost Converter

The Buck-Boost converter employs a variable switching frequency technique. This technique increases the converter efficiency at all loads by automatically reducing the switching frequency at light loads and increasing it at heavy loads. At no load condition, the converter stops switching completely until the load capacitor discharges by a preset voltage. At this point, the converter automatically starts switching and recharges the load capacitor(s). In addition to saving power at all loads, this technique ensures low switching noise on the converter outputs at light loads. The minimum load capacitor for the Buck-Boost converter is 10 µF. This capacitor must be connected between the Schottky diode(s) and ground (0 V) for each arm of the Buck-Boost converter. The Buck-Boost converter, when enabled, generates ripples on the supply pins (VPOS_IN and VNEG_IN). This ripple is typically attenuated by the power supply rejection ratio of the output amplifiers (IOUT or VOUT) and appears as noise on the output pin of the amplifiers (IOUT and VOUT). A larger load capacitor in combination with additional filter (see application section) reduces the output ripple at the expense of increasing settling time of the converter output.

The input voltage to the Buck-Boost converter (pin PVDD) can vary from +12 V to +36 V. These outputs can be individually enabled or disabled via the user SPI interface (See Commands in 表 4 and 表 5).

8.3.3.1 Buck-Boost Converter Outputs

The Buck-Boost converter can be used to provide power to the current output stage or the voltage output stage by enabling the Buck-Boost converter and connecting the power supplies as shown in 图 100. Additional passive filters can optionally be added between the Schottky diode and input supply pins (VPOS_IN and VNEG_IN) to attenuate the ripple feeding into the VPOS_IN and VNEG_IN pin.

Feature Description (接下页)

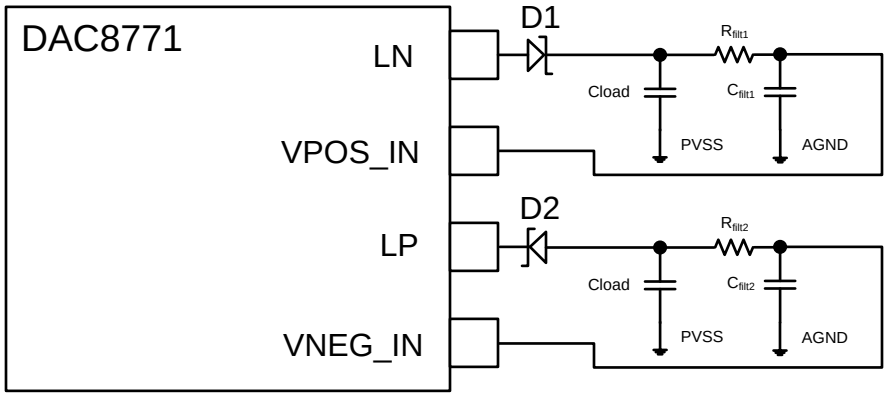


图 100. Buck-Boost Converter Positive and Negative Outputs

8.3.3.2 Selecting and Enabling Buck-Boost Converter

The analog outputs of the Buck-Boost converter can be enabled in two different ways: Current Output Mode or Voltage Output Mode. The positive/negative arm of the selected Buck-Boost converter can be enabled via writing to address 0x07 (*Configuration Buck-Boost Register (address = 0x07) [reset = 0x0000]*). Note that, VNEG_IN is internally shorted to GND when the negative arm of Buck-Boost converter is not enabled.

When used in voltage output mode, the Buck-Boost converter generates a constant ±15.0 V for the positive and negative power supplies.

When used in current output mode the Buck-Boost converter generates the positive and negative power supply based on the RANGE setting, for example the negative power supply is only generated for ±24 mA range.

The minimum voltage that the Buck-Boost converter can generate on the VPOS_IN pin in 4.96 V with a typical efficiency of 75% at PVDD = 12 V and a load current of 24 mA, thus significantly minimizing power dissipation on chip. The maximum voltage that the Buck-Boost converter can generate on the VPOS_IN pin is 32 V. Similarly, the minimum voltage that the Buck-Boost converter can generate on the VNEG_IN pin in -15.0 V. The maximum voltage that the Buck-Boost converter can generate on the VNEG_IN pin in -5.0 V

8.3.3.3 Configurable Clamp Feature and Current Output Settling Time

A large signal step on the output pin IOUT (for example 0 mA to 24 mA) with a load of 1 KΩ would require that the respective Buck-Boost converter change the output voltage on the VPOS_IN pin from 4.0 V to 27 V. Thus, the current output settling time will be dominated by the settling time of the VPOS_IN voltage. A trade off can be made to reduce the settling time at the expense of power saving by increasing the minimum voltage that the respective Buck-Boost converter generates on the positive output.

The DAC8771 implements a configurable clamp feature. This feature allows multiple modes of operation based on CCLP[1:0] and HSCLMP bits (*Configuration Buck-Boost Register (address = 0x07) [reset = 0x0000]*).

8.3.3.3.1 Default Mode - CCLP[1:0] = "00"

This is the default mode of operation, CCLP[1:0] = "00" for Buck-Boost converter is to be in full tracking mode. The minimum voltage generated on VPOS_IN in this case is 4 V. The Buck-Boost converter varies the positive and negative outputs adaptively such that the voltage across these outputs and IOUT pins is ≤ 3 V. This is accomplished by internally feeding back the voltage across the current output PMOS and NMOS to the respective Buck-Boost converter control circuit. For example, for a load current of 24 mA flowing through a load resistance of 1 KΩ, the generated voltage at the VPOS_IN pin will be around 27V.

8.3.3.3.2 Fixed Clamp Mode - CCLP[1:0] = "01"

In this mode of operation, the user can over-rides the default operation by writing "01" to CCLP[1:0]. The minimum voltage generated on VPOS_IN and VNEG_IN can be adjusted by writing to PCLMP[3:0] / NCLMP[3:0] (address 0x07).

Feature Description (接下页)

8.3.3.3.3 Auto Learn Mode - CCLP[1:0] = "10"

In this mode ,the device automatically senses the load on the current output terminal and sets the minimum voltage generated on VPOS_IN terminals to a fixed value. The value is calculated such that for any code change, the settling time is dependent only on the DAC settling time. For example, with a load of 250 Ω and a maximum current of 24 mA, the Buck-Boost output voltage is set as 9 - 12 V. This achieves the maximum power saving without sacrificing settling time because the Buck-Boost output is fixed.

In order to ensure the correct operation of auto-learn mode, following steps below must be followed.

1. The device must be enabled in full tracking mode, CCLP[1:0] = "00".
2. Current output is enabled and a code greater then 4000h should be written to the DAC.
3. Write CCLP[1:0] = "10" to enable auto learn mode.

At this point, the clamp register (PCLMP - address 0x07) is populated with the appropriate settings. The clamp status bit CLST (address 0x0B) is set once the clamp register is populated indicating the completion of this process. In this mode the PCLMP bits are read only. Typically, this process of sensing the load is done only once after power up. In order to re initiate this process, the CCLP bits must be rewritten with "10".

8.3.3.3.4 High Side Clamp (HSCLMP)

The default maximum positive voltage that the Buck-Boost converter can generate is 32 V. However, this voltage can be reduced to 26 V by writing '1' to HSCLMP bit (address 0x0E 表 5). Note that this feature can be enabled or disabled per channel by selecting the corresponding channel (address 0x03)

8.3.4 Analog Power Supply

The DAC8771 is designed to operate with a single power supply (12 V to 36 V) using integrated Buck-Boost converter. In this mode, pins PVDD and AVDD must be tied together and driven by the same power supply. VPOS_IN and VNEG_IN will be enabled as programmed by the device registers. It is recommended that DVDD is applied first to reduce output transients.

The DAC8771 can also be operated without using the integrated Buck-Boost converter. In this mode, pins PVDD, AVDD, and VPOS_IN must be tied together and driven by the same power supply (12 V to 33 V). In this mode in order to reduce output transients it is recommended that DVDD is applied first, followed by VPOS_IN / PVDD / AVDD and finally REFIN.Note that in this mode, the minimum required head room and foot room for the output amplifiers must be met.

Recommended Operating Conditions shows the maximum and minimum allowable limits for all the power supplies when DAC8771 is powered using external power supplies.

8.3.5 Digital Power Supply

The digital power supply to DAC8771 can be internally generated or externally supplied. This is determined by the status of DVDD_EN pin.

When the DVDD_EN pin is left floating, the voltage on DVDD pin is generated via an internal LDO. The typical value of the voltage generated on DVDD pin is 5 V. In this mode, the DVDD pin can also be used to power other digital components on the board. The maximum drive capability of this pin is 10mA. Please note that to ensure stability the minimum load capacitance on this pin is limited to 100 pF, where as the maximum load capacitance is limited to 0.2 µF.

When the DVDD_EN pin is tied to 0V, the internal LDO is disabled and the DVDD pin must be powered via an external digital supply.

8.3.6 Internal Reference

The DAC8771 includes an integrated 5V reference with an initial accuracy of ±10 mV maximum and a temperature drift coefficient of 10 ppm/°C maximum. A buffered output capable of driving up to 5 mA is available on REFOUT. The internal reference for DAC8771 is disabled by default. To enable the internal reference, REF_EN bit on address 0x02h must be set to '1' (表 5).

Feature Description (接下页)

It is recommended to follow JEDEC standardized solder reflow parameters for surface mount devices, as is typically provided by most contract PCB assembly services. Failure to adhere to suggested JEDEC standards can result in excessively high temperatures in the solder process or excessive time exposed to high temperatures, which can induce mechanical stress on thin-packages, such as QFNs, resulting in parametric degradation in many band-gap reference topologies.

8.3.7 Power-On-Reset

The DAC8771 contain power on reset circuits which is based on AVDD and DVDD power supplies. After power-on, the power-on-reset circuit ensures that all registers are at their default values (表 4). The current, voltage output DAC, and the Buck-Boost converter are disabled. The current output pin is in high impedance state.

The voltage output pin is in a 30kΩ-to-GND state; however, the VSENSEP pin is an open circuit. If the VOUT and VSENSEP pins are connected together, the VOUT pin would also be connected to GND through the same resistor. The VOUT pin connection to GND can be reconfigured to high-impedance through the POC bit. This resistor is disconnected when the voltage output is enabled. The Buck-Boost converter for each channel are powered off at power-on reset.

8.3.8 $\overline{\text{ALARM}}$ Pin

The DAC8771 contains an $\overline{\text{ALARM}}$ pin. When one or more of following events occur, the $\overline{\text{ALARM}}$ pin is pulled low:

1. The load on the IOUT pin is in open circuit (>500µsec); or
2. The voltage at IOUT, when enabled, reaches a level where the accuracy of the output current would be compromised (>500µsec). This condition is detected by monitoring internal voltage levels of the IOUT circuitry and will typically be below the specified compliance voltage minimum of 3V; or
3. The die temperature has exceeded +150°C; or
4. The SPI watchdog timer exceeded the timeout period (if enabled); or
5. The SPI frame error check (CRC) encountered an error (if enabled)
6. A short circuit current limit is reached (>500µsec) on any VOUT when enabled in voltage output mode
7. The Buck-Boost converter has reached the maximum output voltage (set by bit HSCLMP 表 5 address 0x0E)

When connecting the $\overline{\text{ALARM}}$ pins of multiple DAC8771 devices together, forming a wired-AND function, the host processor should read the status register of each device to know all the fault conditions that are present.

The $\overline{\text{ALARM}}$ pin continuously monitors the above mentioned conditions and returns to open drain condition if the alarm condition is removed (non-latched behavior - default). For condition (1) mentioned above and Buck-Boost converter used to power the DAC, the $\overline{\text{ALARM}}$ pin if pulled low due to the alarm condition will remain pulled low even after the alarm condition is removed (latched behavior). In this condition the alarm pin can be reset by

1. Resetting the corresponding fault bits in the status register (address 0x0B 表 5); or
2. Performing software reset (write to address 0x01 表 5); or
3. Toggling hardware reset pin; or
4. Performing power on reset

Note that if the alarm action bits are programmed to "10" (AC_IOC[1:0], the Buck-Boost converter and the current output amplifier are automatically disabled upon the event of open circuit on current output. In this case, the $\overline{\text{ALARM}}$ automatically resets to the default behavior (non-latched behavior).

8.3.9 Power GOOD bit

The Buck-Boost converter in DAC8771 has a read only bit called power good (PG) (address 0x0B 表 5). This bit is set to logic '1' when both of the following conditions are met

1. The VPOS_IN > 4V (if enabled) and
2. The VNEG_IN < -3V (if enabled)

Feature Description (接下页)

The PG bit indicates the status of the outputs of the enabled Buck-Boost converter. For example, if the positive and negative outputs of the Buck-Boost converter are enabled, then the PGA bit is set to a logic '1' only after the positive output pins of the Buck-Boost converter are ≥ 4 V and the negative output pin of Buck-boost converter is ≤ -3 V.

8.3.10 Status Register

Since, DAC8771 contains one $\overline{\text{ALARM}}$ pin for the entire chip, the status of individual fault condition can be checked using the status register. This register (see) consists of five types of $\overline{\text{ALARM}}$ status bits (Faults on current and voltage outputs , Over temperature condition, CRC errors, Watchdog timeout and Buck-Boost converter power good) and two status bit (User toggle, Auto Learn status). The device continuously monitors these conditions. When an alarm occurs, the $\overline{\text{ALARM}}$ pin is pulled low and the corresponding status bit is set ('1'). Whenever one of these status bits is set, it remains set until the user clears it by writing '1' to corresponding bit on address 0x0B. The status bit can also be cleared by performing a hardware reset, software reset, or power-on reset, note that it takes a minimum of 8 µsec for the status register to get reset. These bits are reasserted if the ALARM condition continues to exist in the next monitoring cycle.

8.3.11 Status Mask

The $\overline{\text{ALARM}}$ pin for DAC8771 is triggered by any of the alarm condition $\overline{\text{ALARM}}$ Pin . However, these different alarm conditions can be masked from creating the alarm signal at the pin by using the status mask register. The status mask register (address 0x0C) has the same bit order as the status register except that it can be set to mask any or all status bits that create the alarm signal.

8.3.12 Alarm Action

The DAC8771 implements an alarm action register (address 0x0D,). By writing to this register, the user can select the action that the device takes automatically in case of a specific alarm condition. If different setting are chosen for different alarm conditions, the following priority (high to low) is considered when taking action:

1. Over temperature alarm
2. Output fault alarm
3. CRC error/Watchdog timer fault alarm

This device also contains a 6 bit alarm code register (address 0x0E 表 5) which can be loaded to the DAC if the alarm action register is set to "01". Note that the alarm code, once set, remains set even if the alarm condition is removed. Also note that the alarm action change to the programmed code is a step function even if slew rate control is enabled.

8.3.13 Watchdog Timer

This feature is useful to ensure that communication between the host processor and the DAC8771 has not been lost. It can be enabled by setting the WEN (address 0x03) bit to '1', see . The watchdog timeout period can be set using the WPD[1:0] address 0x03) bits. The timer period is based off an internal oscillator with a typical value of 8 MHz

If enabled, the chip must have an SPI frame with 0x10 as the write address byte written to the device within the programmed timeout period. Otherwise, the $\overline{\text{ALARM}}$ pin asserts low and the WDT bit (address 0x0B) of the status register is set to '1'. The WDT bit is set to '0' with a software/hardware reset, or by disabling the watchdog timer (WEN = '0'), or powering down the device.

When using multiple DAC8771 devices in a daisy-chain configuration, the open-drain $\overline{\text{ALARM}}$ pins of all devices can be connected together to form a wired-AND network. The watchdog timer can be enabled in any number of the devices in the chain although enabling it in one device in the chain should be sufficient. The wired-AND $\overline{\text{ALARM}}$ pin may get pulled low because of the simultaneous presence of different trigger conditions in the devices in the daisy-chain. The host processor should read the status register of each device to know all the fault conditions present in the chain.

Feature Description (接下页)

8.3.14 Programmable Slew Rate

The slew rate control feature allows the user to control the rate at which the output voltage or current changes. This feature is disabled by default and can be enabled for the selected channel by writing logic '1' to the SREN bit at address 0x04 (see). With the slew rate control feature disabled, the output changes smoothly at a rate limited by the output drive circuitry and the attached load.

With this feature enabled, the output does not slew directly between the two values. Instead, the output steps digitally at a rate defined by bits [2:0] (SR_STEP) and bits [3:0] (SRCLK_RATE) on address 0x04 (see). SR_RATE defines the rate at which the digital slew updates; SRCLK_STEP defines the amount by which the output value changes at each update. shows different settings for SRCLK_STEP and SR_RATE.

The time required for the output to slew over a given range can be expressed as 公式 8:

$$Slew\ Time = \frac{Output\ Change}{Step\ Size\ x\ Update\ Clock\ Frequency\ x\ LSB\ Size} \quad (8)$$

Where:

- *Slew Time* is expressed in seconds
- *Output Change* is expressed in amps (A) for current output mode or volts (V) for voltage output mode

When the slew rate control feature is enabled, the output changes happen at the programmed slew rate. This configuration results in a staircase formation at the output. If the CLR pin is asserted, the output slews to the zero-scale value at the programmed slew rate. When a new DAC data is written, the output starts slewing to the new value at the slew rate determined by the current DAC code and the new DAC data. The update clock frequency for any given value is the same for all output ranges. The step size, however, varies across output ranges for a given value of step size because the LSB size is different for each output range.

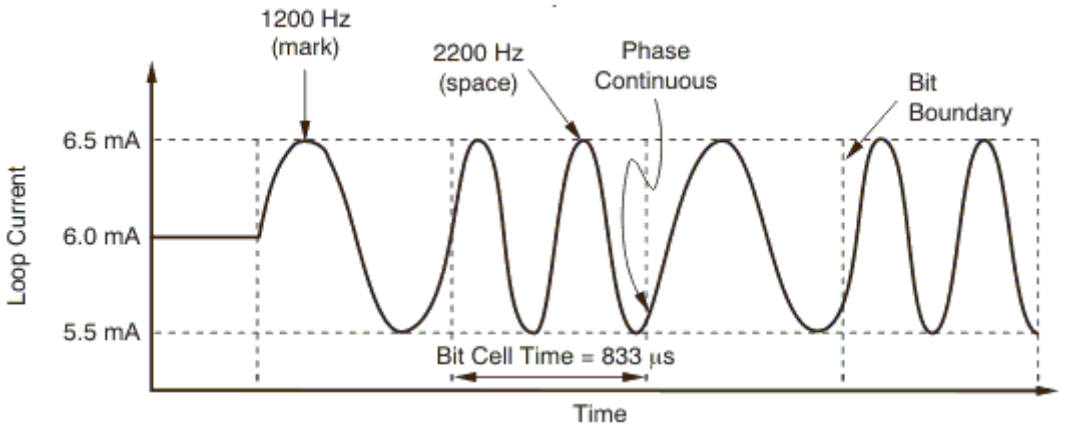
Note that disabling the slew rate feature while the DAC is executing the slew rate command will abort the slew rate operation and the DAC output will stay at the last code after which the slew rate disable command was acknowledged.

8.3.15 HART Interface

On the DAC8771, digital communication such as HART can be modulated onto the current output signal.

If the RANGE (address 0x04) bits are programmed such that the IOUT is enabled, the external HART signal (ac voltage; 500 mV_{PP}, 1200 Hz and 2200 Hz) can be capacitively coupled in through the HARTIN pin and transferred to a current that is superimposed on the current output. The HARTIN pin has a typical input impedance of 20 kΩ to 30 kΩ, depending on the selected current output range, which together with the input capacitor used to couple the external HART signal into the HARTIN pin can be used to form a high-pass filter to attenuate frequencies below the HART bandpass region. In addition to this filter, an external passive filter is recommended to complete the filtering requirements of the HART specifications. 图 101 illustrates the output current vs time operation for a typical HART interface.

Feature Description (接下页)



Note: DC current = 6 mA.

图 101. Output Current vs Time

The HART pin for the selected channel can be enabled by writing logic '1' to the HTEN bit at address 0x04 (表 4 and 表 5).

8.4 Device Functional Modes

8.4.1 Serial Peripheral Interface (SPI)

The device is controlled over a versatile four-wire serial interface (SDIN, SDO, SCLK, and $\overline{\text{SYNC}}$) that operates at clock rates of up to 25 MHz and is compatible with SPI, QSPI™, Microwire™, and digital signal processing (DSP) standards. The SPI communication command consists of a write address byte and a data word for a total of 24 bits (when CRC is disabled). The timing for the digital interface is shown in the timing section.

8.4.1.1 Stand-Alone Operation

The serial clock SCLK can be a continuous or a gated clock. When $\overline{\text{SYNC}}$ is high, the SCLK and SDIN signals are blocked and the SDO pin is in a HiZ state. Exactly 24 falling clock edges must be applied before $\overline{\text{SYNC}}$ is brought high. If $\overline{\text{SYNC}}$ is brought high before the 24th falling SCLK edge, then the data written are not transferred into the internal registers. If more than 24 falling SCLK edges are applied before $\overline{\text{SYNC}}$ is brought high, then the last 24 bits are used. The device internal registers are updated from the Shift Register on the rising edge of $\overline{\text{SYNC}}$. In order for another serial transfer to take place, $\overline{\text{SYNC}}$ must be brought low again.

8.4.1.2 Daisy-Chain Operation

For systems that contain more than one device, the SDO pin can be used to daisy-chain multiple devices together. Daisy-chain operation can be useful for system diagnostics and in reducing the number of serial interface lines. The daisy chain feature can be enabled by writing logic '0' to DSDO bit address 0x03 (), the SDO pin is set to HiZ when DSDO bit is set to 1. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multiple-device interface is constructed, as 图 102 illustrates.

Device Functional Modes (接下页)

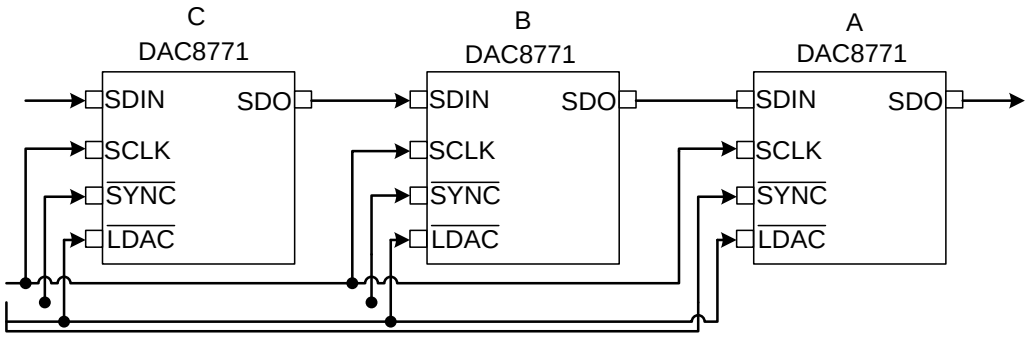


图 102. Three DAC8771s in Daisy-Chain Mode

The DAC8771 provides two modes for daisy-chain operation: normal and transparent. The TRN bit in the Reset config register determines which mode is used. In Normal mode (TRN bit = '0'), the data clocked into the SDIN pin are transferred into the shift register. The first falling edge of SYNC starts the operating cycle. SCLK is continuously applied to the SPI Shift Register when SYNC is low. If more than 24 clock pulses are applied, the data ripple out of the shift register and appear on the SDO line. These data are clocked out on the rising edge of SCLK and are valid on the falling edge. By connecting the SDO pin of the first device to the SDIN input of the next device in the chain, a multiple-device interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × N, where N is the total number of DAC8771s in the chain. When the serial transfer to all devices is complete, SYNC is taken high. This action latches the data from the SPI Shift registers to the device internal registers synchronously for each device in the daisy-chain, and prevents any further data from being clocked in. Note that a continuous SCLK source can only be used if SYNC is held low for the correct number of clock cycles. For gated clock mode, a burst clock containing the exact number of clock cycles must be used and SYNC must be taken high after the final clock in order to latch the data.

In Transparent mode (address 0x02h, TRN bit = '1' 表 5), the data clocked into SDIN are routed to the SDO pin directly; the Shift Register is bypassed. When SCLK is continuously applied with SYNC low, the data clocked into the SDIN pin appear on the SDO pin almost immediately (with approximately a 12 ns delay); there is no 24 clock delay, as there is in normal operating mode. While in Transparent mode, no data bits are clocked into the Shift Register, and the device does not receive any new data or commands. Putting the device into transparent mode eliminates the 24 clock delay from SDIN to SDO caused by the Shift Register, thus greatly speeding up the data transfer. For example, consider three DAC8771s (C, B, and A) in a daisy-chain configuration (图 102). The data from the SPI controller are transferred first to C, then to B, and finally to A. In normal daisy-chain operation, a total of 72 clocks are needed to transfer one word to A. However, if C and B are placed into Sleep mode, the first 24 data bits are directly transferred to A (through C and B); therefore, only 24 clocks are needed.

To wake the device up from transparent mode and return to normal operation, the hardware RESET pin must be toggled.

8.4.2 SPI Shift Register

The SPI Shift Register is 24 bits wide (refer to the *Frame Error Checking* section for 32-bit frame mode). The default 24-bit input frame consists of an 8-bit address byte followed by a 16-bit data word as shown in 表 1.

表 1. Default SPI Frame

BIT 23:BIT 16	BIT 15:BIT 0
Address byte	Data word

8.4.3 Write Operation

A typical write to program a channel of the DAC8771 consists of writing to the following registers in the sequence shown in Figure 12.

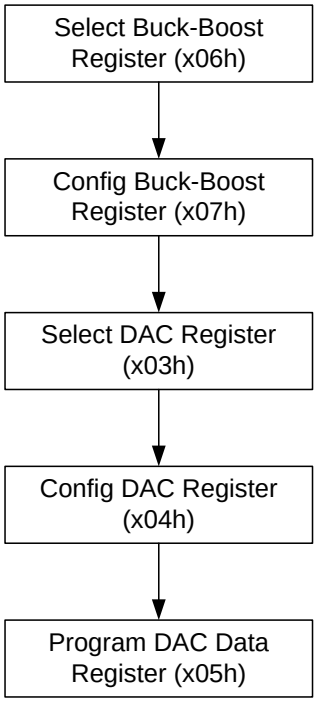


图 103. Typical Write to DAC8771

8.4.4 Read Operation

A read operation is accomplished when DB 23 is '1' (see 表 2). A no-operation (NOP) command should follow the read operation in order to clock out an addressed register. The read register value is output MSB first on SDO on successive falling edges of SCLK.

表 2. Register Read Address Functions(1)

ADDRESS BYTE	
DB23	DB 22: DB 16
Read/Write Bit	Register Addresses

(1) 'X' denotes *don't care* bits.

8.4.5 Updating the DAC Outputs and $\overline{\text{LDAC}}$ Pin

Depending on the status of both $\overline{\text{SYNC}}$ and $\overline{\text{LDAC}}$, and after data have been transferred into the DAC Data registers, the DAC outputs can be updated either in asynchronous mode or synchronous mode.

8.4.5.1 Asynchronous Mode

In this mode, the $\overline{\text{LDAC}}$ pin is set low before the rising edge of $\overline{\text{SYNC}}$. This action places the DAC8771 into Asynchronous mode, and the $\overline{\text{LDAC}}$ signal is ignored. The DAC latches are updated immediately when $\overline{\text{SYNC}}$ goes high.

8.4.5.2 Synchronous Mode

To use this mode, set $\overline{\text{LDAC}}$ high before the rising edge of $\overline{\text{SYNC}}$, and then take $\overline{\text{LDAC}}$ low after $\overline{\text{SYNC}}$ goes high. In this mode, when $\overline{\text{LDAC}}$ stays high, the DAC latch is not updated; therefore, the DAC output does not change. The DAC latch is updated by taking $\overline{\text{LDAC}}$ low any time after a certain delay from the rising edge of $\overline{\text{SYNC}}$ (see 图 1). If this delay requirement is not satisfied, invalid data are loaded. Refer to the Timing Diagrams for details.

8.4.6 Hardware $\overline{\text{RESET}}$ Pin

When the $\overline{\text{RESET}}$ pin is low, the device is in hardware reset. All the analog outputs (VOUT_A to VOUT_D and IOUT_A to IOUT_D), all the registers except the POC register, and the DAC latches are set to the default reset values. In addition, the Gain and Zero Registers are loaded with default values, communication is disabled, and the signals on $\overline{\text{SYNC}}$ and SDIN are ignored (note that SDO is in a high-impedance state). When the $\overline{\text{RESET}}$ pin is high, the serial interface returns to normal operation and all the analog outputs (VOUT_A to VOUT_D and IOUT_A to IOUT_D) maintain the reset value until a new value is programmed.

8.4.7 Hardware CLR Pin

The CLR pin is an active high input that should be low for normal operation. When this pin is a logic '1', all the outputs are cleared to either zero-scale code or midscale code depending on the status of the CLSLx bit (see reset register). While CLR is high, all $\overline{\text{LDAC}}$ pulses are ignored. When CLR is taken low again, the DAC outputs remain cleared until new data is written to the DAC. The contents of the offset Registers, Gain Registers and DAC input registers are not affected by taking CLR high. Note that the clear action will result in the outputs clearing to the default value instantaneously even if slew rate control is enabled.

8.4.8 Frame Error Checking

If the DAC8771 is used in a noisy environment, error checking can be used to check the integrity of SPI data communication between the device and the host processor. This feature can be enabled by setting the CREN bit address 0x03 .

The frame error checking scheme is based on the CRC-8-ATM (HEC) polynomial $x^8 + x^2 + x + 1$ (that is, *100000111*). When error checking is enabled, the SPI frame width is 32 bits, as shown in 表 3 . The normal 24-bit SPI data are appended with an 8-bit CRC polynomial by the host processor before feeding it to the device. For a register readback, the CRC polynomial is output on the SDO pins by the device as part of the 32 bit frame.

Note that the user has to start with the default 24 bit frame and enable frame error checking through the CREN bit and switch to the 32 bit frame. Alternatively, the user can use a 32 bit frame from the beginning and pad the 8 MSB bits as the device will only use the last 24 bits until the CRCEN bit is set. The frame length has to be carefully managed, especially when using daisy-chaining in combination with CRC checking to ensure correct operation.

表 3. SPI Frame with Frame Error Checking Enabled

BIT 31:BIT 8	BIT 7:BIT 0
Normal SPI frame data	8-bit CRC polynomial

The DAC8771 decodes the 32-bit input frame data to compute the CRC remainder. If no error exists in the frame, the CRC remainder is zero. When the remainder is non-zero (that is, the input frame has single- or multiple-bit errors), the $\overline{\text{ALARM}}$ pin asserts low and the CRE bit of the status register (address 0x0B) is also set to '1'. Note that the $\overline{\text{ALARM}}$ pin can be asserted low for any of the different conditions as explained in the *$\overline{\text{ALARM}}$ Pin* section. The CRE bit is set to '0' with a software or hardware reset, or by disabling the frame error checking, or by powering down the device. In the case of a CRC error, the specific SPI frame is blocked from writing to the device.

Frame error checking can be enabled for any number of DAC8771 devices connected in a daisy-chain configuration. However, it is recommended to enable error checking for none or all devices in the chain. When connecting the $\overline{\text{ALARM}}$ pins of all combined devices, forming a wired-AND function, the host processor should read the status register of each device to know all the fault conditions present in the chain. For proper operation, the host processor must provide the correct number of SCLK cycles in each frame, taking care to identify whether or not error checking is enabled in each device in the daisy-chain.

8.4.9 DAC Data Calibration

The DAC8771 contains a dedicated user calibration register set. This feature allows the user to trim the system gain and offset errors. Both the voltage output and the current output have common user calibration registers available. The user calibration feature is disabled by default. To enable this feature, the CLEN bit (DB0) on address 0x08 must be set to logic '1 (see).

8.4.9.1 DAC Data Gain and Offset Calibration Registers

The DAC calibration register set includes one gain calibration and one offset calibration register (16 bits for DAC8771). The range of gain adjustment is typically ±50% of full-scale with 1 LSB per step. The power-on value of the gain register is 0x8000 which is equivalent to a gain of 1.0. The offset code adjustment is typically ±32,768 LSBs with 1 LSB per step. The input data format of the gain register is unsigned straight binary, and the input data format of the offset register is twos complement. The gain and offset calibration is described by 公式 9.

$$CODE\_OUT = \left[CODE\ x \left(\frac{User\_Gain + 2^{15}}{2^{16}} \right) + User\_Zero \right] \quad (9)$$

Where:

- *CODE* is the decimal equivalent of the code loaded to the DAC.
- VREFIN is the reference voltage; for internal reference, VREFIN = +5.0 V.
- *GAIN* is automatically selected for a desired voltage output range as shown in
- *User_Offset* is the signed 16-bit code in the offset register.
- *User_GAIN* is the unsigned 16-bit code in the gain register.

It is important to note that this is a purely digital implementation and the output is still limited by the programmed value at both ends of the voltage or current output range. Therefore, the user must remember that the correction only makes sense for endpoints inside of the true device end points. If the user desires to correct more than just the actual device error, for example a system offset, the valid range for the adjustment would change accordingly and must be taken into account. This range is set by the RANGE bits as described in Configuration DAC Register (address = 0x04) [reset = 0x0000].

8.5 Register Maps

8.5.1 Register Maps

8.5.1.1 DAC8771 Commands

表 4. Address Functions

ADDRESS BYTE	FUNCTION	READ/WRITE	PER CHANNEL	POWER-ON RESET VALUE
0x00	No operation (NOP)	Write	No	0x0000
0x01	Reset register	Read+Write	No	0x0000
0x02	Reset config register	Read+Write	No	0x0000
0x03	Select DAC register	Read+Write	No	0x0000
0x04	Configuration DAC register	Read+Write	Yes	0x0000
0x05	DAC data register	Read+Write	Yes	0x0000
0x06	Select Buck-Boost converter register	Read+Write	No	0x0000
0x07	Configuration Buck-Boost converter register	Read+Write	Yes	0x0000
0x08	DAC channel calibration enable register	Read+Write	Yes	0x0000
0x09	DAC channel gain calibration register	Read+Write	Yes	0x0000
0x0A	DAC channel offset calibration register	Read+Write	Yes	0x0000
0x0B	Status register	Read+Write	No	0x1000
0x0C	Status mask register	Read+Write	No	0x0000
0x0D	Alarm action register	Read+Write	No	0x0000
0x0E	User alarm code register	Read+Write	Yes	0x0000
0x0F	Reserved	N/A	N/A	N/A
0x10	Write watchdog timer reset	Write	No	0x0000
0x11	Device ID	Read	No	0x0000
0x12 - 0xFF	Reserved	N/A	N/A	N/A

Note that, in order to write to (or read from) a per channel address, corresponding Buck-Boost converter and DAC channel must be selected using commands 0x06 and 0x03.

8.5.1.2 Register Maps and Bit Functions

表 5. Register Map

ADDRESS	BITS															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x01	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	RST
0x02	x	x	x	IDA	IDB	IDC	CLREN	x	x	x	x	REF_EN	TRN	CLR	POC	UBT
0x03	x	x	x	Reserved	Reserved	Reserved	CLSL	Reserved	Reserved	Reserved	CH	DSDO	CREN	WPD[1:0]		WEN
0x04	SCLIM[1:0]		HTEN	OTEN	SRCLK_RATE[3:0]				SR_STEP[2:0]			SREN	RANGE[3:0]			
0x05	DAC_DATA[15:0]															
0x06	x	x	x	x	x	x	x	x	x	x	x	x	Reserved	Reserved	Reserved	DC
0x07	x	x	x	x	CCLP[1:0]		PCLMP[3:0]				NCLMP[3:0]				PNSEL[1:0]	
0x08	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CLEN
0x09	UGAIN[15:0]															
0x0A	UOFF[15:0]															
0x0B	x	x	x	CLST	WDT	DIDA	DIDB	DIDC	PG	UTGL	CRE	TMP	Reserved	Reserved	Reserved	F
0x0C	x	x	x	x	MWT	x	x	x	x	x	MCRE	MTMP	Reserved	Reserved	Reserved	MF
0x0D	x	x	x	x	x	x	x	x	AC_CRE_WDT[1:0]		AC_IOC[1:0]		AC_VSC[1:0]		AC_TMP[1:0]	
0x0E	ACODE[15:10]						HSCLMP	0	x	x	x	x	x	x	x	x
0x10	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	RWD
0x11	x	x	x	x	x	x	x	x	x	x	x	x	x	DID[2:0]		

8.5.1.2.1 No Operation Register (address = 0x00) [reset = 0x0000]

图 104. No Operation Register

15	14	13	12	11	10	9	8
Reserved							
W							
7	6	5	4	3	2	1	0
Reserved							
W							

LEGEND: R/W = Read/Write; R = Read only; W = Write Only; -n = value after reset

表 6. No Operation Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	W	00000000 00000000	Reserved

8.5.1.2.2 Reset Register (address = 0x01) [reset = 0x0000]

图 105. Reset Register

15	14	13	12	11	10	9	8
Reserved							
R/W							
7	6	5	4	3	2	1	0
Reserved							RST
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 7. Reset Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	Reserved	R/W	00000000 0000000	Reserved
0	RST	R/W	0	Reset. When set, it resets all registers except POC register bit to the respective power-on reset default value. After reset completes the RST bit clears

8.5.1.2.3 Reset Config Register (address = 0x02) [reset = 0x0000]

图 106. Reset Config Register

15	14	13	12	11	10	9	8
Reserved			IDA	IDB	IDC	CLRENA	Reserved
R/W			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved			REF_EN	TRN	CLR	POC	UBT
R/W			R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8. Reset Config Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R/W	000	Reserved
12	IDA	R/W	0	User Bit 0 - Sets this user bit low. 1 - Sets this user bit high.
11	IDB	R/W	0	User Bit 0 - Sets this user bit low. 1 - Sets this user bit high.
10	IDC	R/W	0	User Bit 0 - Sets this user bit low. 1 - Sets this user bit high.
9	CLREN	R/W	0	Clear Enable 0 - DAC hardware and software clear is disabled 1 - DAC hardware and software clear is enabled
8:5	Reserved	R/W	0000	Reserved
4	REF_EN	R/W	0	Internal reference enable/disable 0 - Internal reference disabled (default) 1 - Internal reference enabled
3	TRN	R/W	0	Enable transparent mode (see section "daisy chain operation")
2	CLR	R/W	0	Active high, clears all DAC registers to either zero or full scale based on CLSL bit. After clear completes the CLR bit resets.
1	POC	R/W	0	Power-Off-Condition 0 - IOUT to HIZ, VOUT to 30K-to-PBKG at power up, hardware or software reset (default) 1 - IOUT and VOUT to HIZ at power up, hardware and software reset
0	UBT	R/W	0	User Bit - This bit can be used to check if the communication to the chip is working correctly by writing a known value to this bit and reading that value from the status register toggle bit. The toggle resister bit UTGL (address 0x0B) is set to the same value as the UBT bit.

8.5.1.2.4 Select DAC Register (address = 0x03) [reset = 0x0000]

图 107. Select DAC Register

15	14	13	12	11	10	9	8
Reserved			Reserved	Reserved	Reserved	CLSLA	Reserved
R/W			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
Reserved	Reserved	CHA	DSDO	CREN	WPD[1:0]		WEN
R/W	R/W	R/W	R/W	R/W	R/W		R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 9. Select DAC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	Reserved	R/W	000	Reserved
9	CLSLA	R/W	0	Clear Select 0 - DAC registers cleared to zero scale upon hardware or software clear (default) 1 - DAC registers cleared to mid scale upon hardware or software clear
8:6	Reserved	R/W	0	Reserved
5	CHA	R/W	0	Channel A selected
4	DSDO	R/W	0	Disable SDO - When set, this bit disables daisy chain operation and SDO pin is set to HiZ, enabled by default
3	CREN	R/W	0	Enable CRC - When set, this bit enables frame error checking, disabled by default
2:1	WPD[1:0]	R/W	00	Watchdog Timer Period 00 - 10 ms (typical) 01 - 51 ms (typical) 10 - 102 ms (typical) 11 - 204 ms (typical)
0	WEN	R/W	0	Enable Watchdog Timer - When set, this bit enables watchdog timer, disabled by default

8.5.1.2.5 Configuration DAC Register (address = 0x04) [reset = 0x0000]

图 108. Configuration DAC Register

15	14	13	12	11	10	9	8
SCLIM[1:0]		HTEN	OTEN	SRCLK_RATE[3:0]			
R/W		R/W	R/W	R/W			
7	6	5	4	3	2	1	0
SR_STEP[2:0]			SREN	RANGE[3:0]			
R/W			R/W	R/W			

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 10. Configuration DAC Register Field Descriptions

Bit	Field	Type	Reset	Description
15:14	SCLIM[1:0]	R/W	00	Voltage output short circuit limit 00 - 22 mA (default). Actual value will be between the minimum and maximum values specified in *Electrical Characteristics*. 01 - 10 mA. Actual value will be between the minimum and maximum values specified in *Electrical Characteristics*. 10 - 26 mA. Actual value will be between the minimum and maximum values specified in *Electrical Characteristics*. 11 - 31 mA. Actual value will be between the minimum and maximum values specified in *Electrical Characteristics*.
13	HTEN	R/W	0	Enable HART - When set, this bit enables HART, disabled by default
12	OTEN	R/W	0	Output Enabled - When set, this bit enables DAC (Voltage or Current) outputs, disabled by default
11:8	SRCLK_RATE[3:0]	R/W	0000	Slew Clock Rate 0000 - DAC updates at 258,065 Hz (default) 0001 - DAC updates at 200,000 Hz 0010 - DAC updates at 153,845 Hz 0011 - DAC updates at 131,145 Hz 0100 - DAC updates at 115,940 Hz 0101 - DAC updates at 69,565 Hz 0110 - DAC updates at 37,560 Hz 0111 - DAC updates at 25,805 Hz 1000 - DAC updates at 20,150 Hz 1001 - DAC updates at 16,030 Hz 1010 - DAC updates at 10,295 Hz 1011 - DAC updates at 8,280 Hz 1100 - DAC updates at 6,900 Hz 1101 - DAC updates at 5,530 Hz 1110 - DAC updates at 4,240 Hz 1111 - DAC updates at 3,300 Hz
7:5	SR_STEP[2:0]	R/W	000	Slew Rate Step Size 000 - 1 LSB (default) 001 - 2 LSB 010 - 4 LSB 011 - 8 LSB 100 - 16 LSB 101 - 32 LSB 110 - 64 LSB 111 - 128 LSB
4	SREN	R/W	0	Slew Rate Enabled - When set, this bit enables slew rate feature, disabled by default

表 10. Configuration DAC Register Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
3:0	RANGE[3:0]	R/W	0000	Range, Please note that upon changing the range, the DAC output changes based on CLSLA (Address 0x03) 0000 - Voltage output 0 to +5 V (default) 0001 - Voltage output 0 to +10 V 0010 - Voltage output ±5 V 0011 - Voltage output ±10 V 0100 - Current output 3.5 mA to 23.5 mA 0101 - Current output 0 to 20 mA 0110 - Current output 0 to 24 mA 0111 - Current output ±24 mA 1000 - Voltage output 0 to +6 V 1001 - Voltage output 0 to +12 V 1010 - Voltage output ±6 V 1011 - Voltage output ±12 V 11xx - Current output 4 mA to 20 mA

8.5.1.2.6 DAC Data Register (address = 0x05) [reset = 0x0000]

图 109. DAC Data Register

15	14	13	12	11	10	9	8
DAC_DATA[15:8]							
R/W							
7	6	5	4	3	2	1	0
DAC_DATA[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 11. DAC Data Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	DAC_DATA[15:0]	R/W		16-bit DAC data

8.5.1.2.7 Select Buck-Boost Converter Register (address = 0x06) [reset = 0x0000]

图 110. Select Buck-Boost Converter Register

15	14	13	12	11	10	9	8
Reserved							
R/W							
7	6	5	4	3	2	1	0
Reserved				Reserved	Reserved	Reserved	DC
R/W				R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 12. Select Buck-Boost Converter Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	Reserved	R/W	0000000000000	Reserved
0	DCA	R/W	0	Buck-Boost converter A selected

8.5.1.2.8 Configuration Buck-Boost Register (address = 0x07) [reset = 0x0000]

图 111. Configuration Buck-Boost Register

15	14	13	12	11	10	9	8
Reserved				CCLP[1:0]		PCLMP[3:2]	
R/W				R/W		R/W	
7	6	5	4	3	2	1	0
PCLMP[1:0]		NCLMP[3:0]				PNSEL[1:0]	
R/W		R/W				R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 13. Configuration Buck-Boost Register Field Descriptions

Bit	Field	Type	Reset	Description		
15:12	Reserved	R/W	0000	Reserved		
11:10	CCLP[1:0]	R/W	00	Buck-Boost converter configurable clamp setting 00 - Buck-Boost converter in full tracking mode (default) 01 - User can write to PCLMP and NCLMP bits 10 - PCLMP bits are populated automatically to optimum value - "Auto Learn mode", User cannot write to PCLMP bits 11 - Invalid		
9:6	PCLMP[3:0]	R/W	0000	Buck-Boost converter positive clamp setting, DAC output unloaded - Buck-Boost converter positive arm low side clamp		
					Current Output Mode	Voltage Output Mode
				0000	4.0 V (default)	Invalid
				0001	5.0 V	Invalid
				0010	6.0 V	Invalid
				0011	9.0 V	9.0 V
				0100	11.0 V	Invalid
				0101	12.0 V	Invalid
				0110	13.0 V	Invalid
				0111	14.0 V	Invalid
				1000	15.0 V	15.0 V
				1001	18.0 V	18.0 V
				1010	20.0 V	Invalid
				1011	23.0 V	Invalid
				1100	25.0 V	Invalid
				1101	27.0 V	Invalid
				1110	30.0 V	Invalid
				1111	32.0 V	Invalid

表 13. Configuration Buck-Boost Register Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
5:2	NCLMP[3:0]	R/W	0000	Buck-Boost converter negative clamp setting, DAC output unloaded - Buck-Boost converter negative arm low side clamp
				0000 – Current Output Mode: –5.0 V; Voltage Output Mode: Invalid
				0001 – Current Output Mode: –6.0 V; Voltage Output Mode: Invalid
				0010 – Current Output Mode: –9.0 V; Voltage Output Mode: –9.0 V
				0011 – Current Output Mode: –11.0 V; Voltage Output Mode: Invalid
				0100 – Current Output Mode: –12.0 V; Voltage Output Mode: Invalid
				0101 – Current Output Mode: –13.0 V; Voltage Output Mode: Invalid
				0110 – Current Output Mode: –14.0 V; Voltage Output Mode: Invalid
				0111 – Current Output Mode: –15.0 V; Voltage Output Mode: –15.0 V (default)
				1000 – Current Output Mode: –18.0 V; Voltage Output Mode: Invalid
				1001 – Current Output Mode: –18.0 V; Voltage Output Mode: –18.0 V
				101x – Current Output Mode: Invalid; Voltage Output Mode: Invalid
				11xx – Current Output Mode: Invalid; Voltage Output Mode: Invalid
1:0	PNSEL[1:0]	R/W	00	Enable Buck-Boost converter positive and negative arm 00 - Buck-Boost converter positive and negative arm disabled (default) 01 - Buck-Boost converter positive arm enabled and negative arm disabled 10 - Buck-Boost converter positive arm disabled and negative arm enabled 11 - Buck-Boost converter positive arm and negative arm enabled

8.5.1.2.9 DAC Channel Calibration Enable Register (address = 0x08) [reset = 0x0000]

图 112. DAC Channel Calibration Enable Register

15	14	13	12	11	10	9	8
Reserved							
R/W							
7	6	5	4	3	2	1	0
Reserved							CLEN
R/W							R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 14. DAC Channel Calibration Enable Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	Reserved	R/W	0000000000000000	Reserved
0	CLEN	R/W	0	Enable DAC calibration - When set, this bit enables DAC data calibration, disabled by default

8.5.1.2.10 DAC Channel Gain Calibration Register (address = 0x09) [reset = 0x0000]

图 113. DAC Channel Gain Calibration Register

15	14	13	12	11	10	9	8
UGAIN[15:8]							
R/W							
7	6	5	4	3	2	1	0
UGAIN[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 15. DAC Channel Gain Calibration Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UGAIN[15:0]	R/W	00000000 00000000	16-bit user gain data

8.5.1.2.11 DAC Channel Offset Calibration Register (address = 0x0A) [reset = 0x0000]

图 114. DAC Channel Offset Calibration Register

15	14	13	12	11	10	9	8
UOFF[15:8]							
R/W							
7	6	5	4	3	2	1	0
UOFF[7:0]							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 16. DAC Channel Offset Calibration Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	UOFF[15:0]	R/W	00000000 00000000	16-bit user offset data

8.5.1.2.12 Status Register (address = 0x0B) [reset = 0x1000]

图 115. Status Register

15	14	13	12	11	10	9	8
Reserved			CLST	WDT	DIDA	DIDB	DIDC
R/W			R/W	R/W	R/W	R/W	R/W
7	6	5	4	3	2	1	0
PG	UTGL	CRE	TMP	Reserved	Reserved	Reserved	F
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 17. Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15:13	Reserved	R/W	000	Reserved
12	CLST	R/W	1	Auto Learn status - Indicates that Auto Learn operation is finished
11	WDT	R/W	0	Watchdog timer fault - Indicates that watchdog timer fault has occurred
10	DIDA	R	0	Fixed at logical 1
9	DIDB	R	0	Fixed at logical 1
8	DIDC	R	0	Fixed at logical 1
7	PG	R/W	0	Buck-Boost power good - Indicates the power good condition on the Buck-Boost converter
6	UTGL	R/W	0	User toggle - Copy of user bit (UBT)
5	CRE	R/W	0	CRC error - Indicates CRC error condition
4	TMP	R/W	0	Over temperature - Indicates over temperature condition
3:1	Reserved	R/W	0	Reserved
0	F	R/W	0	DAC Fault - Indicates DAC fault condition

8.5.1.2.13 Status Mask Register (address = 0x0C) [reset = 0x0000]

图 116. Status Mask Register

15	14	13	12	11	10	9	8
Reserved				MWT	Reserved		
R/W				R/W	R/W		
7	6	5	4	3	2	1	0
Reserved		MCRE	MTMP	Reserved	Reserved	Reserved	MF
R/W		R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 18. Status Mask Register Field Descriptions

Bit	Field	Type	Reset	Description
15:12	Reserved	R/W	0000	Reserved
11	MWT	R/W	0	Mask WDT - When set, it masks the alarm pin from watchdog timer fault condition
10:6	Reserved	R/W	00000	Reserved
5	MCRE	R/W	0	CRC error - When set, it masks the alarm pin from CRC error condition
4	MTMP	R/W	0	Mask TMP - When set, it masks the alarm pin from over temperature condition
3:1	Reserved	R/W	0	Reserved
0	MFA	R/W	0	Mask F - When set, it masks the alarm pin from fault condition for the DAC output channel

8.5.1.2.14 Alarm Action Register (address = 0x0D) [reset = 0x0000]

图 117. Alarm Action Register

15	14	13	12	11	10	9	8
Reserved							
R/W							
7	6	5	4	3	2	1	0
AC_CRE_WDT[1:0]		AC_IOC[1:0]		AC_VSC[1:0]		AC_TMP[1:0]	
R/W		R/W		R/W		R/W	

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 19. Alarm Action Register Field Descriptions

Bit	Field	Type	Reset	Description
15:8	Reserved	R/W	00000000	Reserved
7:6	AC_CRE_WDT[1:0]	R/W	00	Action CRC error and Watchdog timer fault circuit condition 00 - No action on Buck-Boost converter, no action on DAC (default) 01 - No action on Buck-Boost converter, respective user alarm code on all DAC 10 - All Buck-Boost converter and DAC disabled and remain disabled even after the alarm condition is removed. 11 - Invalid
5:4	AC_IOC[1:0]	R/W	00	Action current output open circuit condition 00 - No action on Buck-Boost converter, no action on DAC (default) 01 - No action on Buck-Boost converter, respective user alarm code on DAC(s) initiating the alarm 10 - All Buck-Boost converter and DAC disabled and remain disabled even after the alarm condition is removed. 11 - Invalid
3:2	AC_VSC[1:0]	R/W	00	Action voltage output short circuit condition 00 - No action on Buck-Boost converter, no action on DAC (default) 01 - No action on Buck-Boost converter, respective user alarm code on DAC(s) initiating the alarm 10 - All Buck-Boost converter and DAC disabled and remain disabled even after the alarm condition is removed. 11 - Invalid
1:0	AC_TMP[1:0]	R/W	00	Action over temperature condition 00 - No action on Buck-Boost converter, no action on DAC (default) 01 - No action on Buck-Boost converter, respective user alarm code on all DAC 10 - All Buck-Boost converter and DAC disabled and remain disabled even after the alarm condition is removed. 11 - Invalid

8.5.1.2.15 User Alarm Code Register (address = 0x0E) [reset = 0x0000]

图 118. User Alarm Code Register

15	14	13	12	11	10	9	8
ACODE[15:10]						HSCLMP	0
R/W						R/W	R/W
7	6	5	4	3	2	1	0
Reserved							
R/W							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 20. User Alarm Code Register Field Descriptions

Bit	Field	Type	Reset	Description
15:10	ACODE[15:10]	R/W	000000	6 bit alarm code data
9	HSCLMP	R/W	0	Buck-Boost positive output high side clamp 0 - Buck-Boost converter positive output high side clamp set to 32 V (default) 1 - Buck-Boost converter positive output high side clamp set to 26 V (default)
8	0	R/W	0	0
7:0	Reserved	R/W	00000000	Reserved

8.5.1.2.16 Reserved Register (address = 0x0F) [reset = N/A]

图 119. Reserved Register

15	14	13	12	11	10	9	8
Reserved							
R							
7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 21. Reserved Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Reserved	R	N/A	Reserved

8.5.1.2.17 Write Watchdog Timer Register (address = 0x10) [reset = 0x0000]

图 120. Write Watchdog Timer Register

15	14	13	12	11	10	9	8
Reserved							
R							
7	6	5	4	3	2	1	0
Reserved							RWD
R							W

LEGEND: R/W = Read/Write; R = Read only; W = Write only; -n = value after reset

表 22. Write Watchdog Timer Register Field Descriptions

Bit	Field	Type	Reset	Description
15:1	Reserved	R	00000000 0000000	Reserved

表 22. Write Watchdog Timer Register Field Descriptions (接下页)

Bit	Field	Type	Reset	Description
0	RWD	W	0	Reset watchdog timer, this bit clears itself after resetting watch dog timer

8.5.1.2.18 Reserved Register (address 0x12 - 0xFF) [reset = N/A]

图 121. Reserved Register

15	14	13	12	11	10	9	8
Reserved							
R							
7	6	5	4	3	2	1	0
Reserved							
R							

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 23. Reserved Register Field Descriptions

Bit	Field	Type	Reset	Description
15:0	Reserved	R	N/A	Reserved

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Buck-Boost Converter External Component Selection

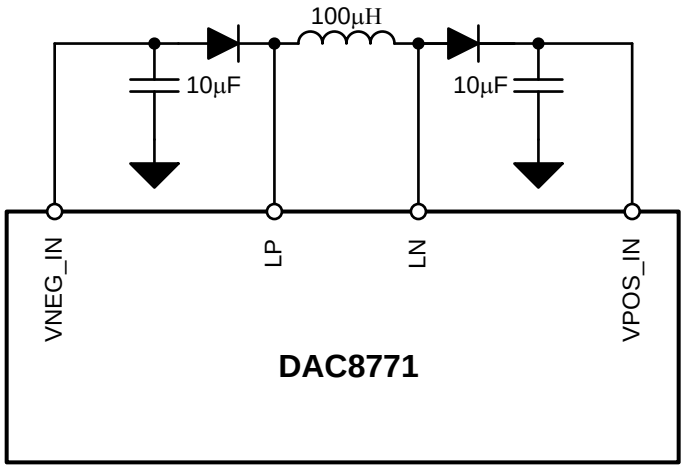


图 122. DAC8771 External Buck-Boost Components with Recommended Values

The buck-boost converter integrated in the DAC8771 requires three external passive components for operation: a single inductor along with two storage capacitors and two switching diodes, one for each VPOS_IN and VNEG_IN when active. If only one output is used, either VPOS_IN or VNEG_IN, the inactive output components may be removed and the respective inputs tied to ground. In order to meet the parametric performance outlined in the section for the voltage output, 500 mV of footroom is required on VNEG_IN.

The recommended value for the external inductor is 100 µH with at least 500 mA peak inductor current. Reducing the inductor value to as low as 80 µH is possible, though this will limit the buck-boost converter maximum input voltage to output voltage ratio, reduce efficiency, and increase ripple. Reducing the inductor below 80 µH will result in device damage. Peak inductor current should be rated at 500 mA or greater with 20% inductance tolerance at peak current. If peak inductor current for an inductor is violated the effective inductance is reduced, which will impact maximum input to output voltage ratio, efficiency, and ripple.

An output, or storage, X7R capacitor with value of 10 µF and voltage rating of 50 V is recommended though other values and dielectric materials may be used without damaging the DAC8771. Reducing capacitor value will increase buck-boost converter output ripple and reduced voltage rating will reduce effective capacitance at full-scale buck-boost converter outputs. X7R capacitors are rated for –55°C to 125°C operation with 15% maximum capacitance variance over temperature. Designs operating over reduced temperature spans and with loose efficiency requirements may use different dielectric material. C0G capacitor typically offer tighter capacitance variance but come in larger packages, but may be beneficial substitutes.

The external diode switches illustrated on the left and right side of the 100 µH inductor shown in 图 122 should be selected based on reverse voltage rating, reverse recovery time, leakage or parasitic capacitance, and current or power ratings. Breakdown voltage rating of at least 60 V is recommended to accommodate for the maximum voltage that may be across the diode when both VPOS and VNEG are both active during switching of the DC/DC. Minimal reverse recovery time and parasitic capacitance is recommended in order to preserve efficiency of the DC/DC. The external diode should be rated for at least 500 mA average forward current.

Application Information (接下页)

9.1.2 Voltage and Current Outputs on a Shared Terminal

图 123 illustrates a simplified block diagram of the voltage output stages of the DAC8771.

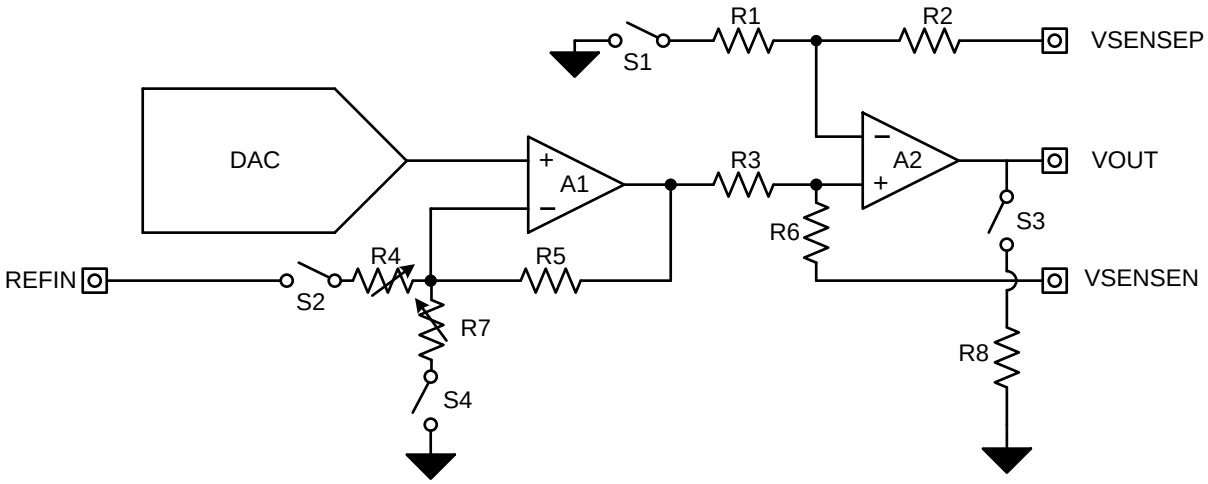


图 123. Simplified Block Diagram of Voltage Output Architecture

When designing for a shared voltage and current output terminal it is important to consider leakage paths that may corrupt the voltage or current output stages.

When the voltage output is active and the current output is inactive the IOUT pin becomes a high-impedance node and therefore does not significantly load the voltage output in a way that would degrade VOUT performance. When the voltage output is inactive and the current output is active switches S1, S2, and S4 all become open while switch S3 is controlled by the POC bit in the Reset Config Register. When the POC bit is set to a 0, the default value, switch S3 is closed when VOUT is disabled. This creates a leakage path with respect to the current output when the terminals are shared which will create a load dependent error. In order to reduce this error the POC bit can be set to a 1 which opens switch S3, effectively making the VOUT pin high-impedance and reducing the magnitude of leakage current.

9.1.3 Optimizing Current Output Settling Time with Auto-Learn Mode

When the buck-boost converter is active, power and heat dissipation of the device are at a minimum, however settling time of the current output is dominated by the slew rate of the buck-boost converter, which is significantly slower that the current output signal chain alone. When the buck-boost converter is bypassed settling time of the current output is minimized while power and heat dissipation are significant.

Auto-learn mode offers an alternative mode which allows the buck-boost converter to learn the size of the load and choose a clamped output value that does not change over the full range of the selected current output. This allows a balance between settling time and power dissipation. There are two options for entering auto-learn mode:

- Enable the buck-boost converter in full-tracking mode followed by enabling the current output. Until the DAC code 0x4000 is passed, settling time will be dominated by the buck-boost converter. After code 0x4000 is surpassed the buck-boost converter detects the load and sets the clamp value appropriately.
- Enable the buck-boost converter in clamp-mode with clamp value set to a greater voltage than required by the largest load the current output will be expected to drive, followed by enabling the current output. Enter full-tracking mode. In this case the clamp value of maintained without the buck-boost converter output changing, therefore settling time is set by the IOUT signal chain. After code 0x4000 is surpassed the buck-boost converter detects the load and adjusts the clamp value appropriately. At all times using this initialization procedure the settling time is defined by the IOUT signal chain.

Application Information (接下页)

9.1.4 Protection for Industrial Transients

In order to successfully protect the DAC8771, or any integrated circuit, against industrial transient testing the internal structures and how they may behave when exposed to said signals must be understood. 图 124 depicts a simplified representation of internal structures present on the device output pins which are represented as a pair of clamp-to-rail diodes connected to the VPOS_IN and VNEG_IN supply rails

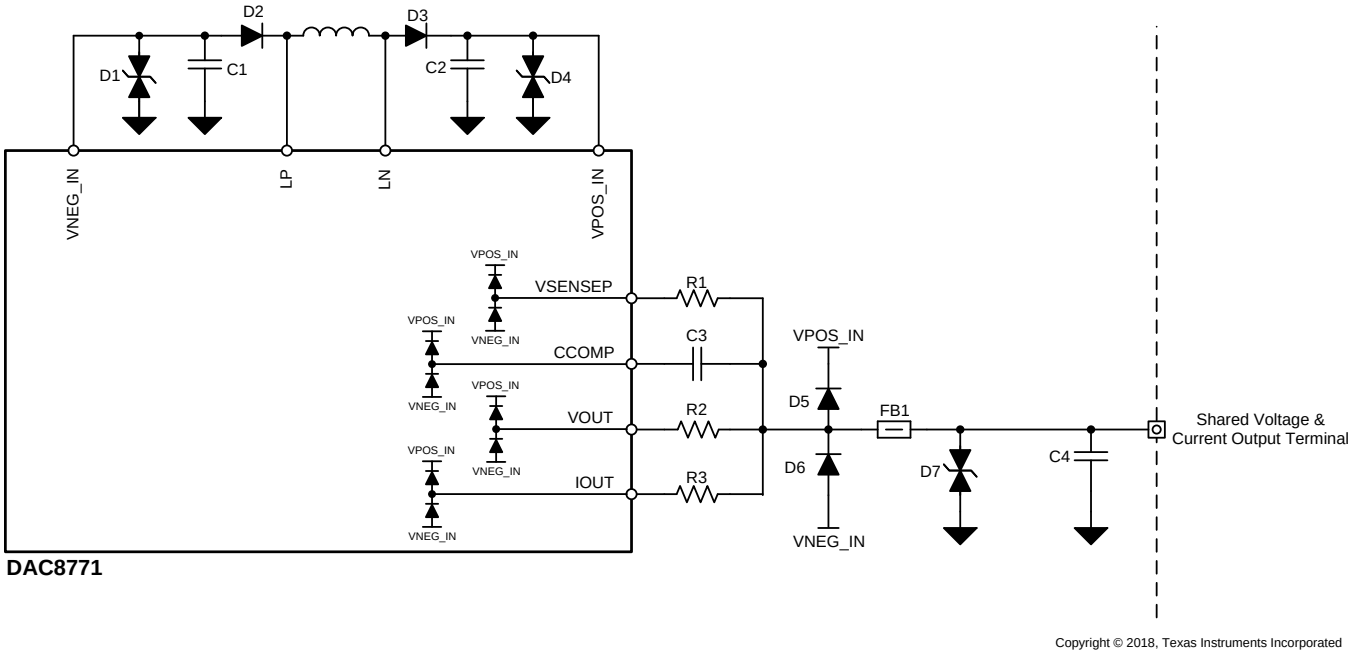


图 124. Simplified Block Diagram of Internal Structures and External Protection

When these internal structures are exposed to industrial transient testing, without the external protection components, the diode structures will become forward biased and conduct current. If the conducted current is too large, which is often true for high-voltage industrial transient tests, the structures will become permanently damaged and impact device functionality.

Both attenuation and diversion strategies are implemented to protect the internal structures as well as the device itself. Attenuation is realized by capacitor C4 which forms an R/C low-pass filter when interacting with the source impedance of the transient generator, ferrite bead FB1 also helps attenuate high-frequency current, along with both AC and DC current limiters realized by series pass elements R1, R2, and R3. Diversion is achieved by transient voltage suppressor (TVS) diode D7 and clamp-to-rail diodes D5 and D6. The combined effects of both strategies effectively limit the current flowing into the device and through the internal diode structures such that the device is not damaged and remains functional.

It is important to also include TVS diodes D1 and D4 at the VPOS_IN and VNEG_IN nodes in order to provide a discharge path for the energy that is going to be sent to these nodes through diodes D5, D6, and the internal diode structures. Without these diodes when current is diverted to these nodes, the DC/DC converter storage capacitors C1 and C2 will charge, and slowly increasing the voltage at these nodes.

9.1.5 Implementing HART with DAC8771

The DAC8771 features an internal resistor to convert a 500-mVpp HART FSK signal sourced by an external HART modem. These resistors are ratiometrically matched to the gain-setting resistors for the current output signal chain to ensure that a 500-mVpp input at the HART_IN pin is delivered as a 1-mApp signal at the IOUT pin regardless of which gain mode is selected.

An external capacitor, placed in series between the HART_IN pin and HART FSK source, is required to AC couple the HART FSK signal to the HART_IN pin. The recommended capacitance for this external capacitor is from 10 nF to 22 nF.

9.2 Typical Application

9.2.1 Single-Channel, Isolated, EMC and EMI Protected Analog Output Module with Adaptive Power Management

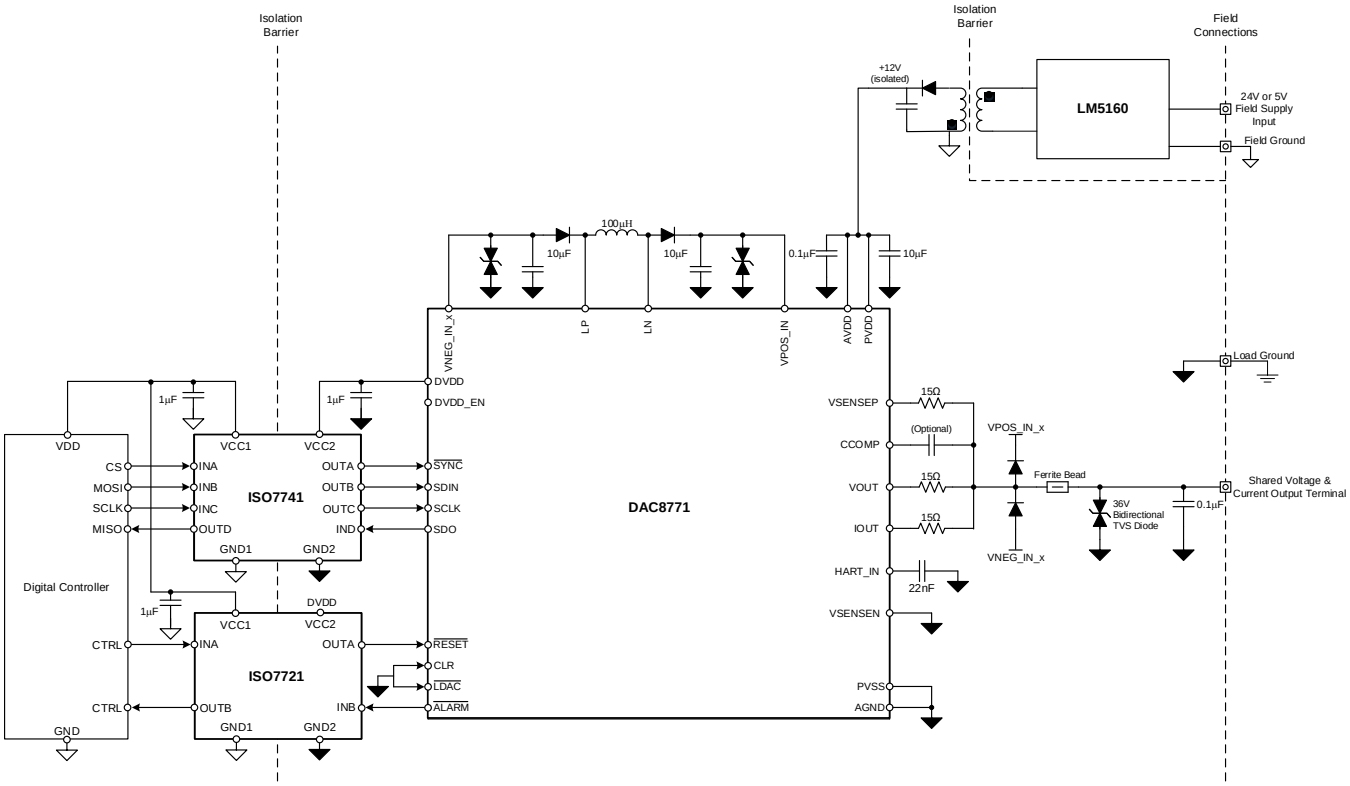


图 125. DAC8771 in Isolated Single-Channel PLC AO Module

9.2.2 Design Requirements

Analog I/O modules are used by programmable logic controllers (PLCs) to interface sensors, actuators, and other field instruments. These modules must meet stringent electrical specifications for both accuracy and robust protection. These outputs are typically current outputs based on the 4-mA to 20-mA range and derivatives or voltage outputs ranging from 0 V to 5 V, 0 V to 10 V, ±5 V, and ±10 V. Common error budgets accommodate 0.1% full-scale range total unadjusted error (% FSR TUE) at room temperature. Designs that desire stronger accuracy over temperature frequently implement calibration. Often the PLC back-plane provides access to a 12-V to 36-V analog supply from which a majority of analog supply voltages are derived.

Analog output modules are frequently multi-channel modules featuring either channel-to-channel isolation between each channel or group isolation where several channels share a common ground connection. As channel count increases it is desirable to maintain small form-factor requiring high levels of integration and reduced power dissipation in order to control heat inside of the PLC enclosure. This design example illustrates a single-channel with isolation, which could be extended for multiple channels to create a channel-to-channel isolated PLC AO module.

Therefore the design requirements are:

- Support of standard industrial automation voltage and current output spans
- Operation with standard industrial automation supply voltages from 12 V to 36 V
- Current and voltage outputs with TUE less than 0.1% at 25°C
- At minimum criteria B IEC61000-4 ESD, EFT, CI, and Surge immunity

Typical Application (接下页)

9.2.3 Detailed Design Procedure

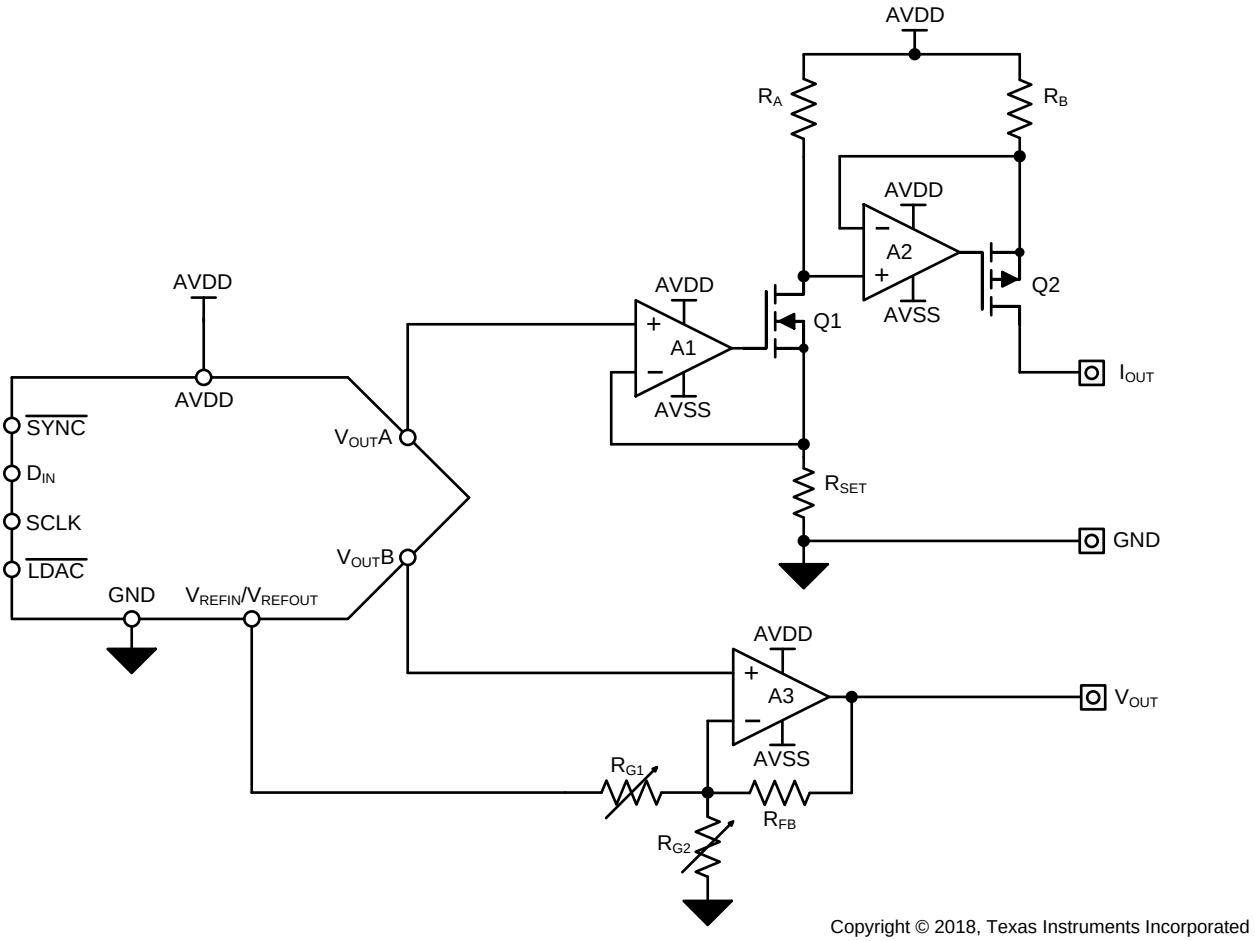


图 126. Generic Design for Typical PLC Current and Voltage Outputs

图 126 illustrates a common generic solution for realizing the desired voltage and current output spans for industrial automation applications.

The current output circuit is comprised of amplifiers A1 and A2, MOSFETs Q1 and Q2, and the three resistors RSET, RA, and RB. This two-stage current source enables the ground-referenced DAC output voltage to drive the high-side amplifier required for the current-source.

The voltage output circuit is composed of amplifier A3 and the resistor network consisting of RFB, RG1, and RG2. A3 operates as a modified summing amplifier, where the DAC controls the non-inverting input and inverting input has one path to GND and a second to VREF. This configuration allows the single-ended DAC to create both the unipolar 0-V to 5-V and 0-V to 10-V outputs and the bipolar ±5-V and ±10-V outputs by modifying the values of RG1 and RG2.

Though this generic circuit realizes the desired spans, both the voltage and current outputs have short-comings. The current output high-side supply voltage is typically 24 V, when driving low impedance loads with this supply voltage a considerable amount of power is dissipated on RB and Q2. This power dissipation results in increased heat which leads to drift errors for amplifiers A1 and A2 as well as the DAC, resistors, and the reference voltage. In order to reduce the power dissipation in the high-side voltage to current converter circuit a feedback system which monitors the voltage drop across Q2 and adaptively adjusts the high-side supply voltage can be implemented. This feedback system adjusts the high side supply voltage to the minimum supply required to keep Q2 in the linear region of operation, avoiding compliance voltage saturation, reducing power dissipation and heat to a minimum which helps maintain accuracy.

Typical Application (接下页)

The generic voltage output circuit performs well but does not compensate for errors associated with excessive output impedance or differences in ground potential from the local PLC ground and the load ground. A modified circuit can be implemented which provides connections to sense errors associated with both output impedance voltage drops and differences in ground potentials, this circuit is shown in 图 123.

图 125 illustrates the DAC8771 along with the LM5160 in a single-channel PLC analog output module. The DAC8771 includes the generic voltage and current output circuits along with buck-boost converter and feedback circuits for the current output and positive and negative sense connections for the voltage output circuit. The DAC8771 also includes an internal reference and internal LDO for supplying the field-side of a digital isolator along with the buck-boost converter generating the single or dual high voltage supplies required for the output circuits, all powered from a single supply.

The DAC8771 buck-boost converter operates at peak efficiency with 12-V input voltage with peak power consumption of approximately 250mW. The LM5160 circuit accepts a wide range of input voltages from just above 12 V to 30 V, providing coverage for most standard PLC supply voltages, and buck-converts this supply voltage to the optimal 12-V supply for the DAC8771. Cumulative power dissipation for the DAC8771 and LM5160 is under 550 mW.

Two ISO7641 devices implement galvanic isolation for all of the digital communication lines, though only a single ISO7641 is required for basic communication with the DAC8771 SPI compatible interface. An output protection circuit is included which is designed to provide immunity to the IEC61000-4 industrial transient and radiation test suite. The protection circuit includes transient voltage suppressor (TVS) diodes, clamp-to-rail steering diodes, and pass elements in the form of resistors and ferrite beads.

9.2.4 Application Curves

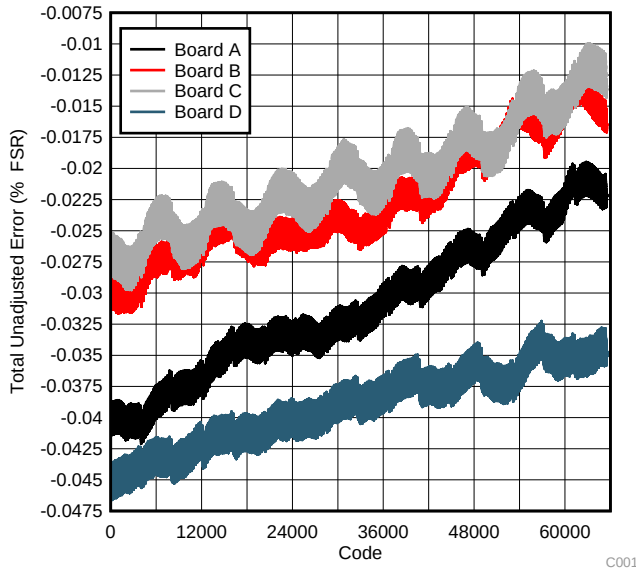


图 127. Voltage Output TUE

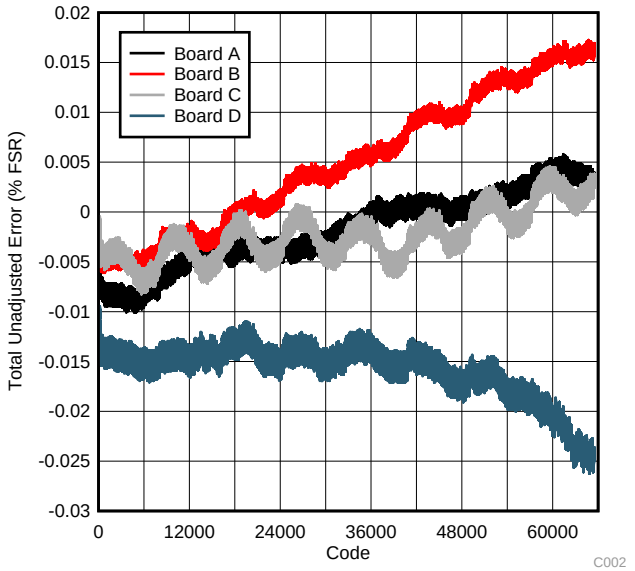


图 128. Current Output TUE

10 Power Supply Recommendations

There are three possible hardware power supply configurations for the DAC8771: the internal DC/DC provides both positive and negative supply voltages, the internal DC/DC provides only one of the supply voltages with an external supply provided on the other, or the internal DC/DC is not used at all and external supply voltages are provided for both positive and negative supply voltages. Simple illustrations for each case are as follows.

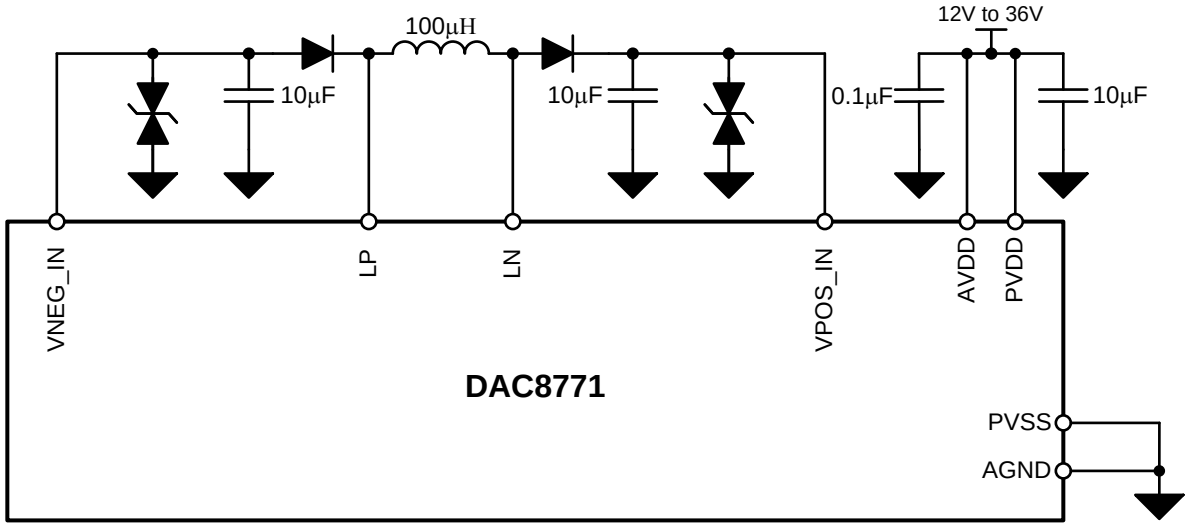


图 129. DAC8771 With Dual Supplies from Internal DC/DC

图 130 illustrates using a single supply from the DAC8771 internal DC/DC and the other supply from an external source. In this example the VNEG_IN supply is the input being supplied by an external supply, or ground for unipolar output spans. A similar scheme could be used if VPOS_IN was supplied by an external supply and VNEG_IN was supplied by the internal DC/DC.

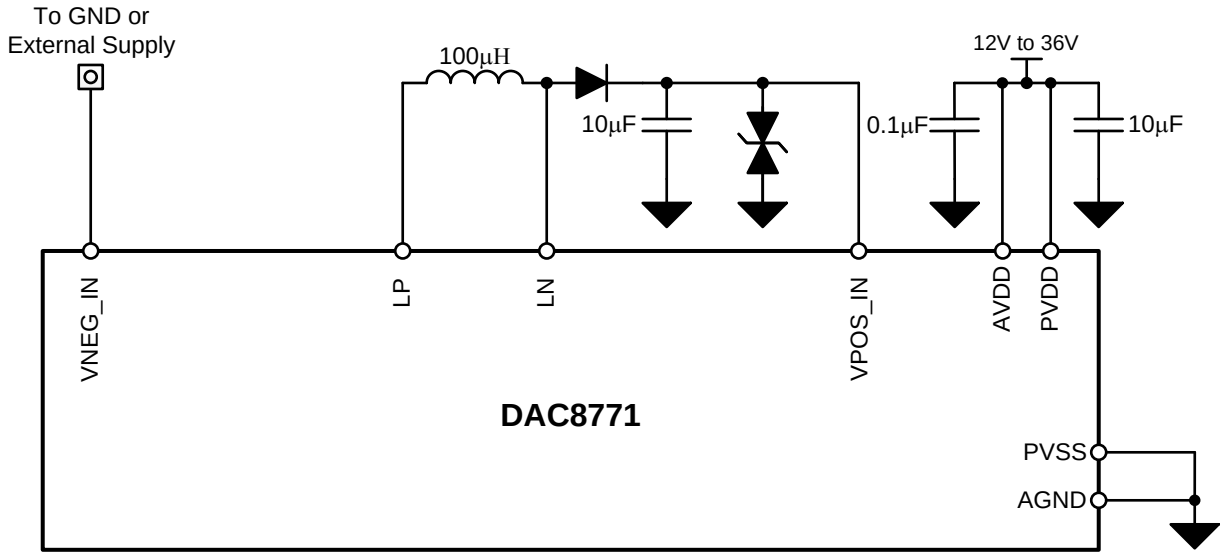


图 130. DAC8771 With Single Supply from Internal DC/DC

The scheme in 图 131 should be used if the internal DC/DC is not used at all and external supplies are selected for VPOS_IN and VNEG_IN. When using external supplies for VPOS_IN it is important that VPOS_IN, PVDD, and AVDD nodes are tied to the same voltage potential with the same ramp-rate

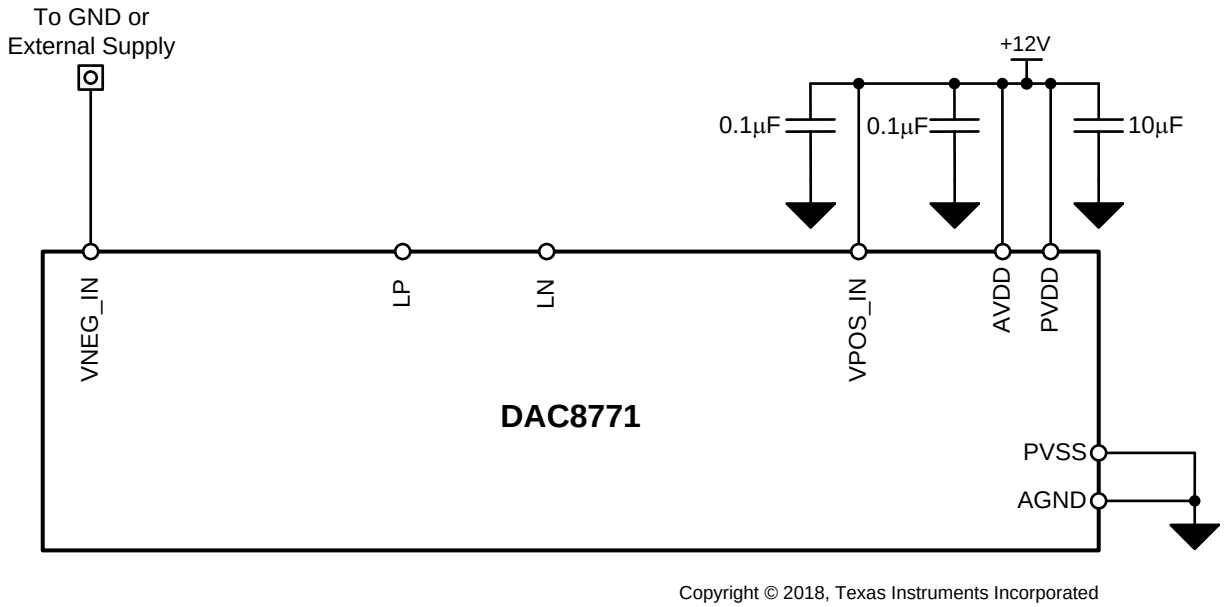


图 131. DAC8771 With External Supplies

11 Layout

11.1 Layout Guidelines

An example layout based on the design discussed in the Typical Application section is shown in the Layout Example section. 图 132 shows the top-layer of the design which illustrates all component placement as no components are placed on the bottom layer. 图 133 shows the internal power-layers for the internal buck-boost converter outputs.

The layer stack-up for this 4-layer example layout is shown below. A 4-layer design is not required, however provides optimal conditions for ground and power-supply planes. The solid ground plane beneath the majority of the signal traces, which are placed on the top layer, allows for a clean return path for sensitive analog traces and keeps them isolated from the internal power supply nets which will exhibit ripple from the DC/DC converter.

表 24. Example Layout Layer Stack-Up

Signal Traces and Ground Fill
SOLID Ground Plane
Split Power Supply Plane for VPOS, VNEG, and DVDD
Signal Traces and Ground Fill

Traces for the DC/DC external components should be as low impedance, low inductance, and low capacitance as possible in order to maintain optimum performance. As such wide traces should be used to minimize inductance with minimal use of vias as vias contribute large inductance and capacitance to the trace. For this reason, it is recommended that all DC/DC components placed on the top layer.

The industrial transient protection circuit should be placed as close to the output connectors as possible to ensure that the return currents from these transients have a controlled path to exit the PCB which does not impact the analog circuitry.

Split ground planes for the DC/DC, digital, and analog grounds are not required but may be helpful to isolated ground return currents from cross-talk. If split ground planes are used, care should be taken to ensure that signal traces are only placed above or below the locations where their respective grounds are placed in order to mitigate unexpected return paths or coupling to the other ground planes. If a single ground plane is used, it is advisable to follow similar practices implementing a star-ground where the respective return currents interact with one another minimally. The example layout uses a single ground plane, based on measured results, performs similarly to an identical version with split ground planes.

The perimeter of the board is stitched with vias in order to enhance design performance against environments which may include radiated emissions. Additional vias are placed in critical areas nearby the design in order to place ground pours in between nodes to reduce cross-talk between adjacent traces.

Standard best-practices should be applied to the remaining components, including but not limited to, placing decoupling capacitors close to their respective pins and using wide traces or copper pours where possible, particularly for power traces where high current may flow.

11.2 Layout Example

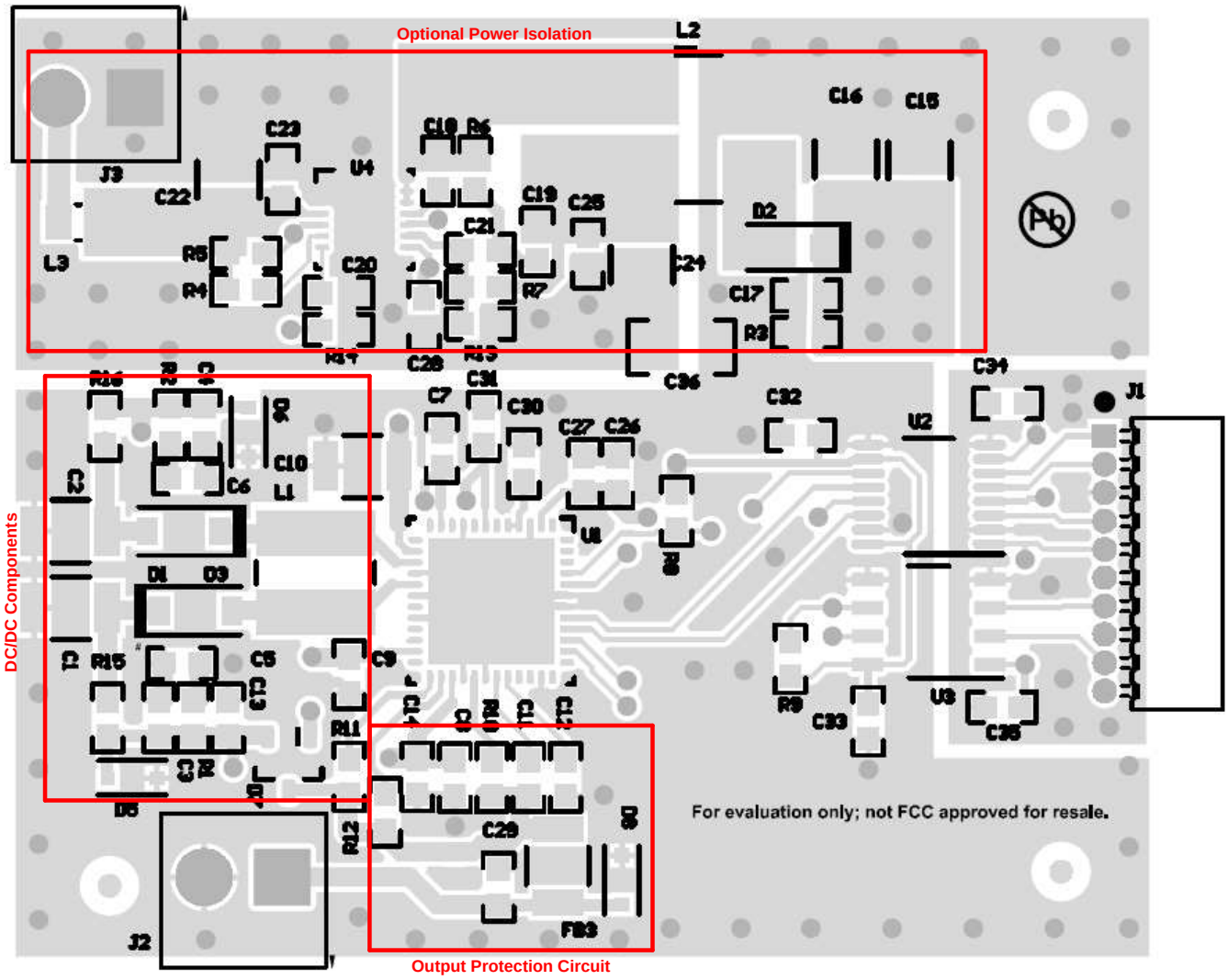


图 132. Application Example Layout

Layout Example (接下页)

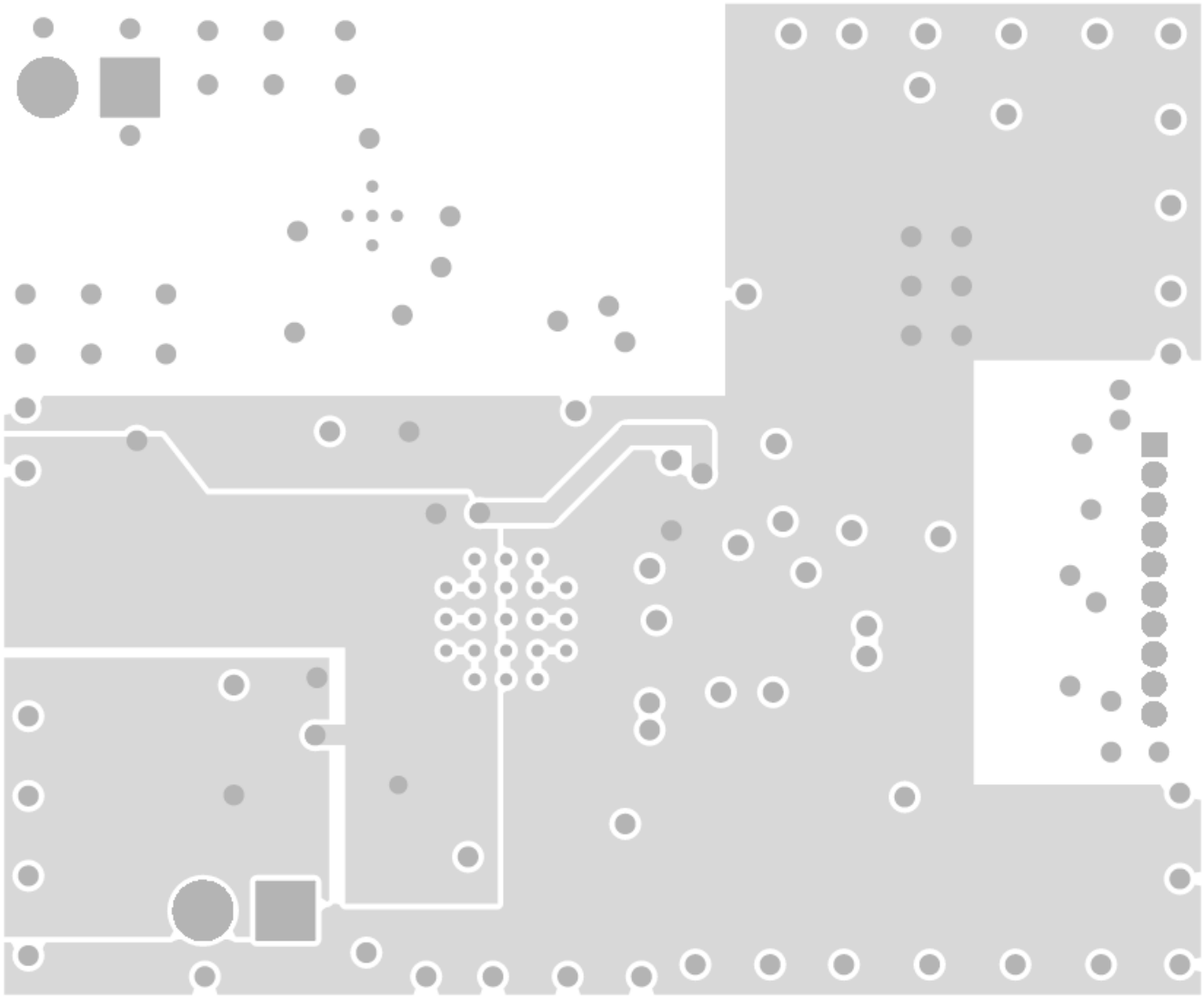


图 133. Example Design Internal Copper Pours

Layout Example (接下页)

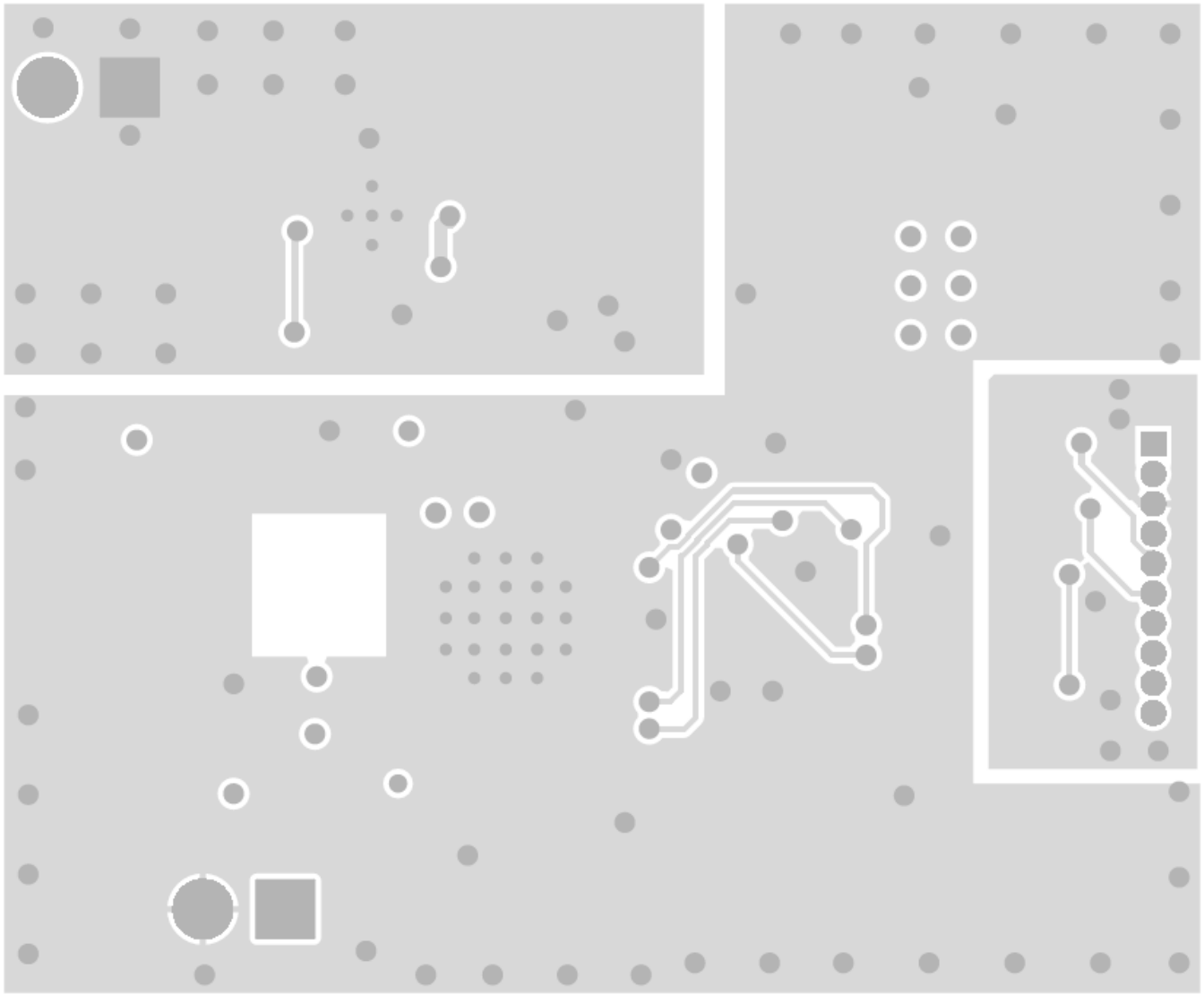


图 134. Example Design Bottom Layer

12 器件和文档支持

12.1 器件支持

12.1.1 Third-Party Products Disclaimer

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12.2 文档支持

12.2.1 相关文档

如需相关文档，请参阅：

- *《半导体和 IC 封装热指标》*应用报告，SPRA953

12.3 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。请单击右上角的*提醒我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.4 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** **可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。**

12.5 商标

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12.6 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DAC8771RGZR	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 125	DAC8771
DAC8771RGZR.A	Active	Production	VQFN (RGZ) | 48	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	DAC8771
DAC8771RGZT	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	Call TI | Nipdau	Level-3-260C-168 HR	-40 to 125	DAC8771
DAC8771RGZT.A	Active	Production	VQFN (RGZ) | 48	250 | SMALL T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 125	DAC8771

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

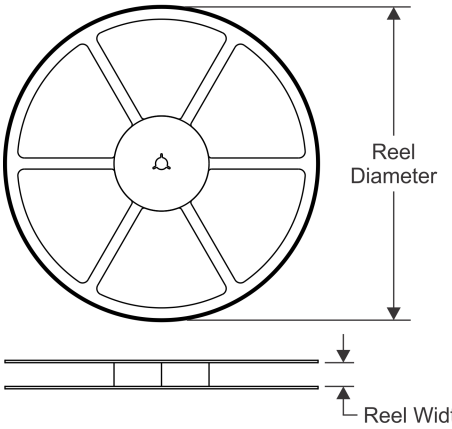
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

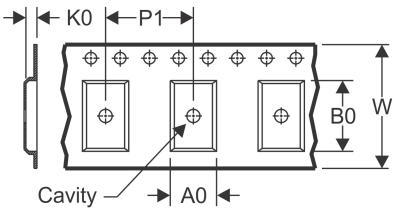
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

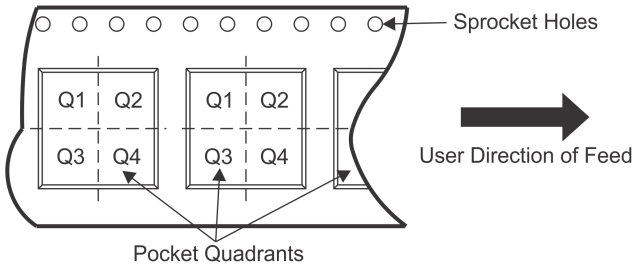


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

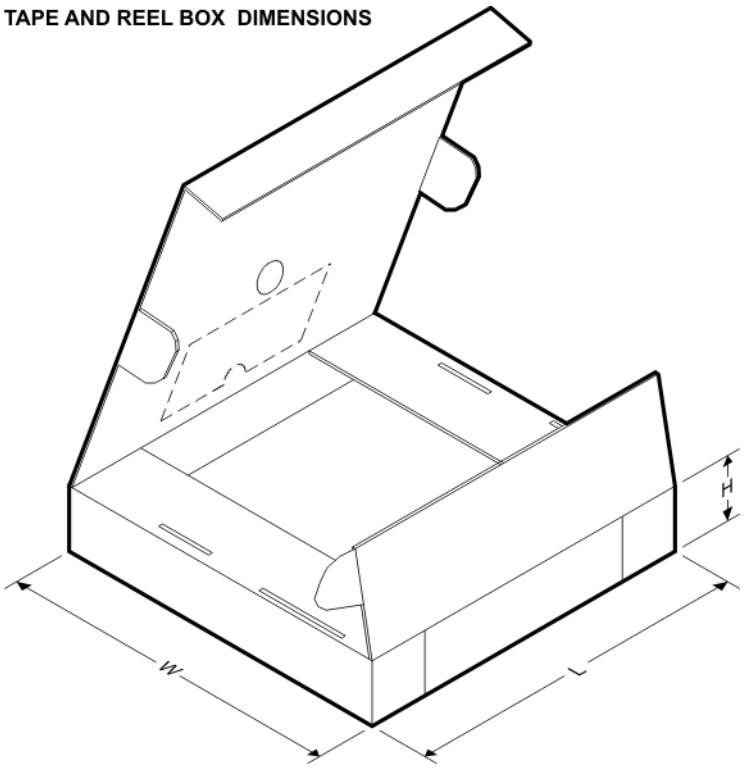
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC8771RGZR	VQFN	RGZ	48	2500	330.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2
DAC8771RGZT	VQFN	RGZ	48	250	180.0	16.4	7.3	7.3	1.1	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC8771RGZR	VQFN	RGZ	48	2500	367.0	367.0	38.0
DAC8771RGZT	VQFN	RGZ	48	250	210.0	185.0	35.0

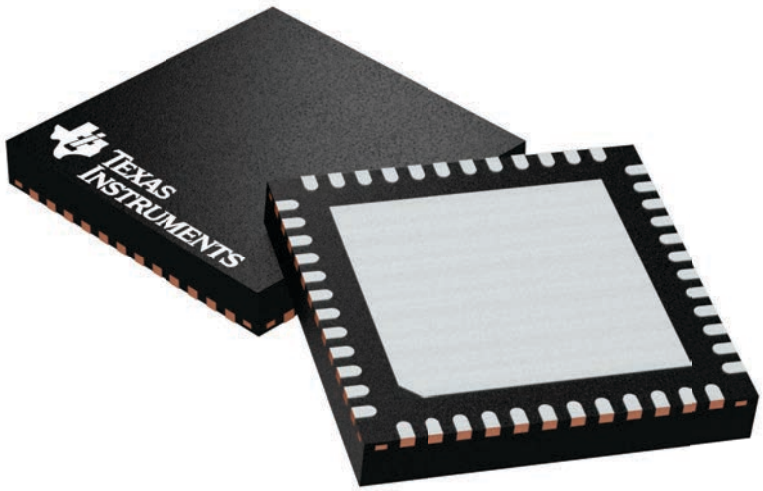
GENERIC PACKAGE VIEW

RGZ 48

VQFN - 1 mm max height

7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

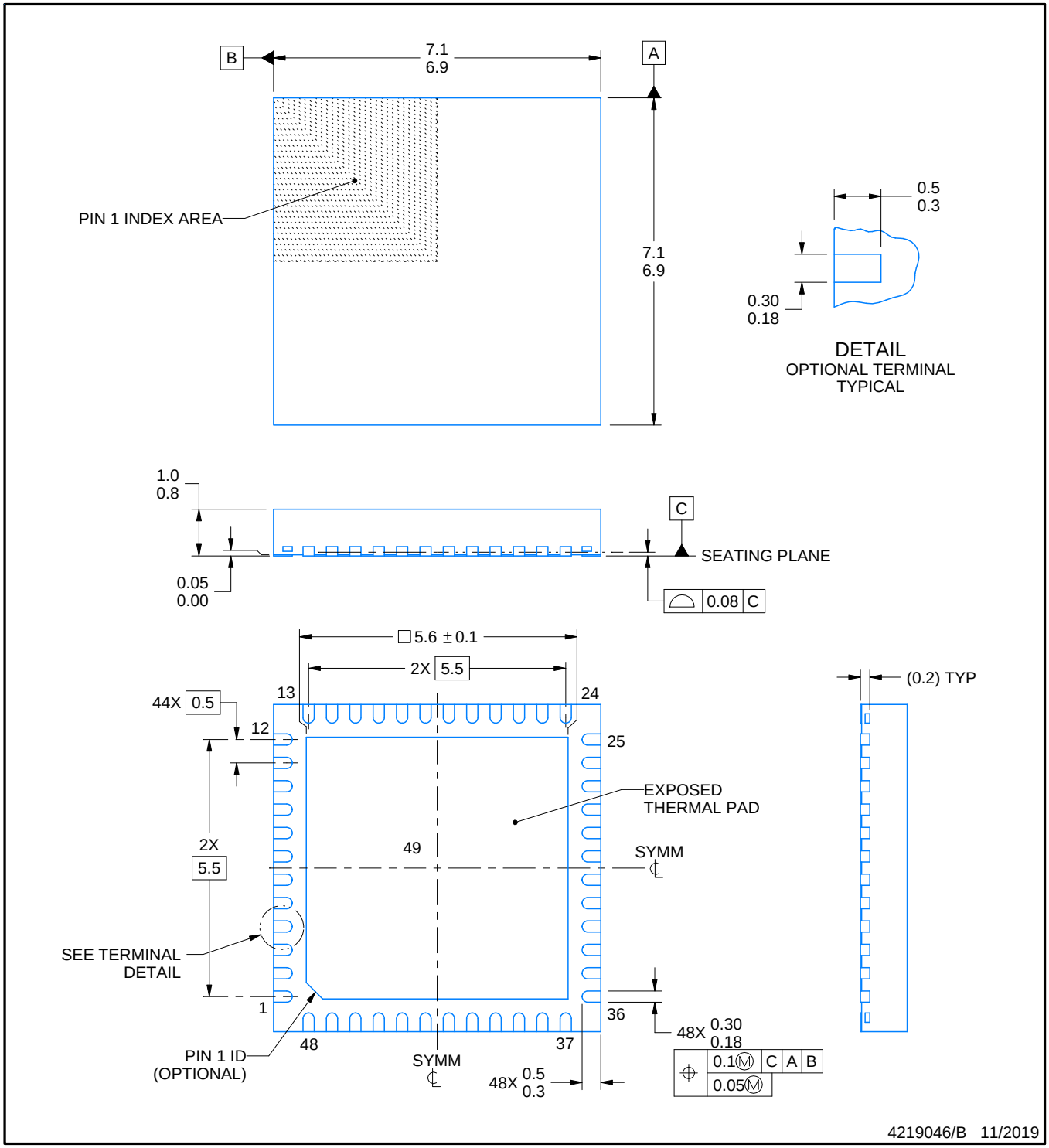
4224671/A

PACKAGE OUTLINE

RGZ0048D

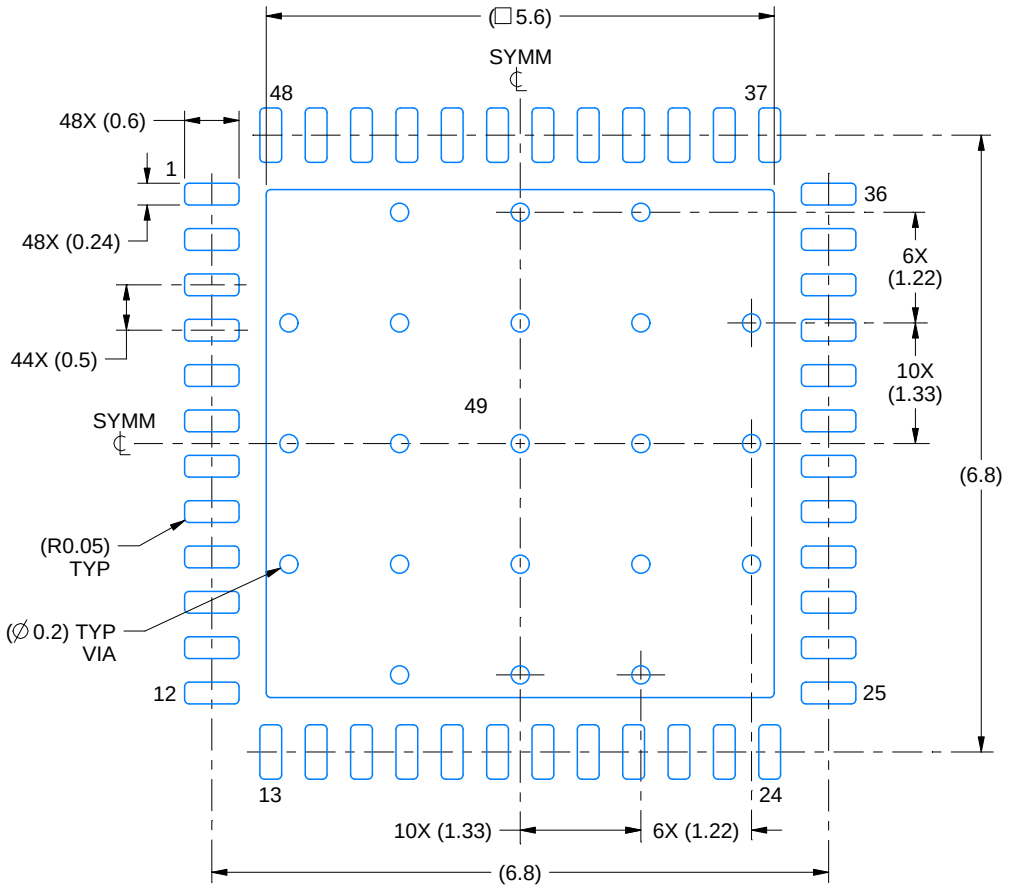
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

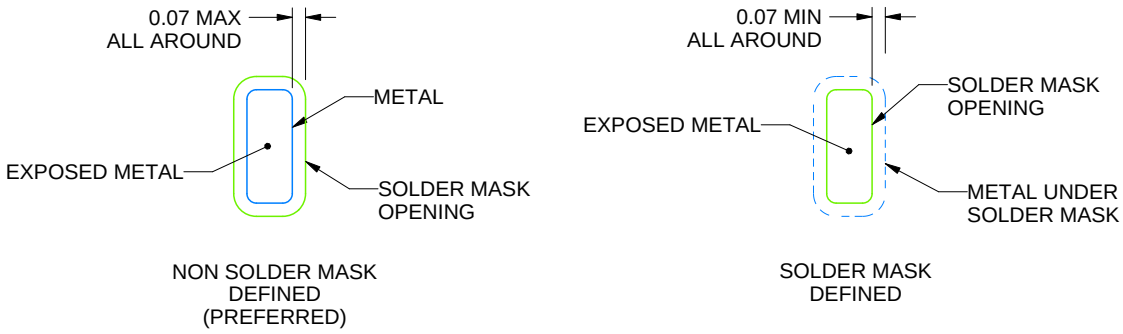


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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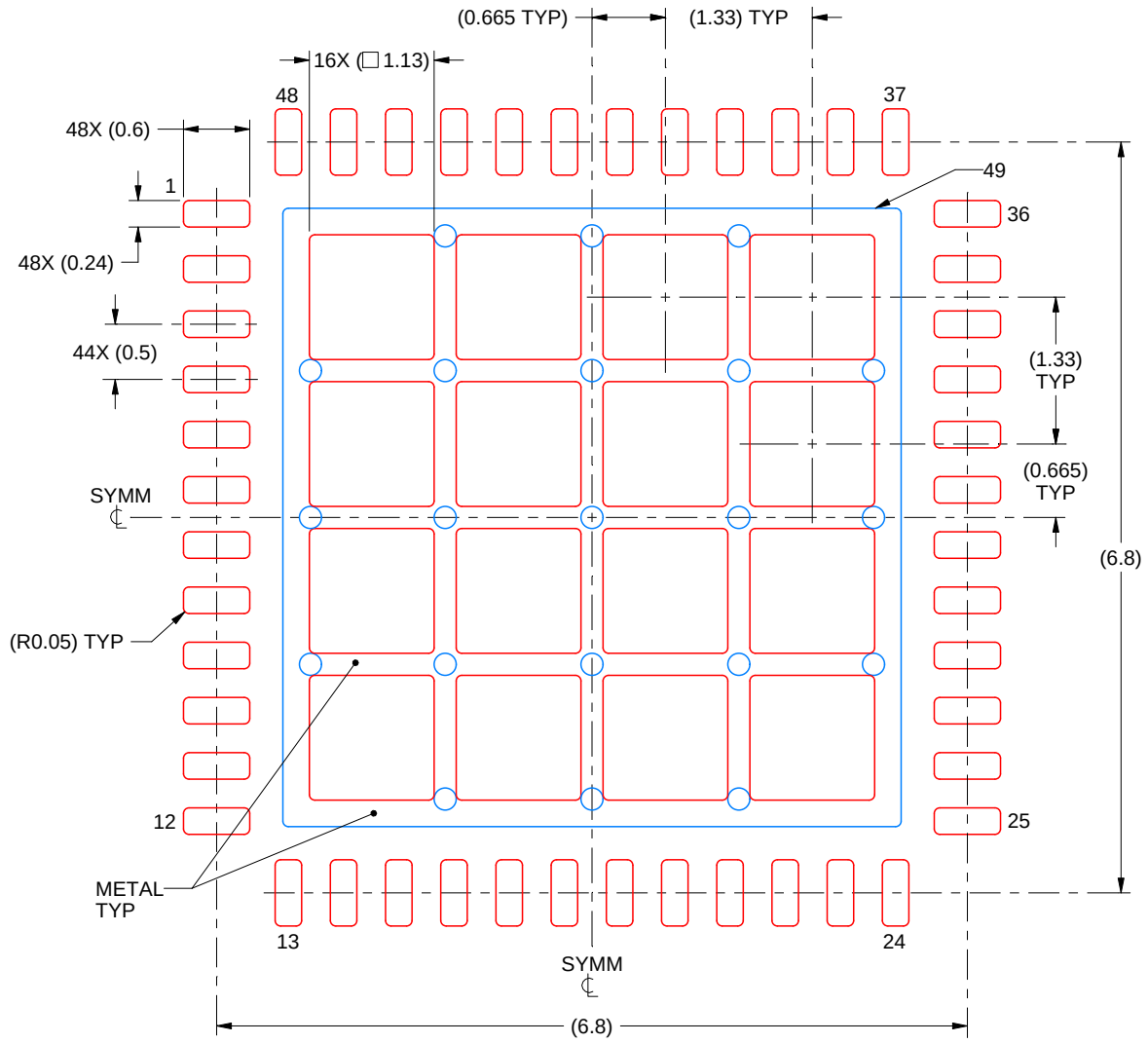
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
66% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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