具有宽占空比范围的 LM25145 6V 至 42V 同步降压直流/直流控制器

1 特性

- 多功能同步降压直流/直流控制器
  - 宽输入电压范围为 6V 至 42V
  - 可调节输出电压范围为 0.8V 至 40V
- 符合 EN55022/CISPR 22 EMI 标准
- 无损 $R_{DS(on)}$ 或分流电流感应
- 开关频率范围为 100kHz 至 1MHz
  - 同步输入和同步输出能力
- 40ns 最短导通时间，可实现高 V_{IN}/V_{OUT} 比率
- 140ns 最短关闭时间，以实现低压差
- 具有 ±1% 反馈精度的 0.8V 基准
- 适用于标准 V_{TH} MOSFET 的 7.5V 栅极驱动器
  - 14ns 自适应死区时间控制
  - 2.3A 拉电流和 3.5A 灌电流能力
  - 针对预偏置启动的低侧软启动
- 可调软启动或可选电压跟踪
- 快速线路和负载瞬态响应
  - 具有线路前馈的电压模式控制
  - 高增益带宽误差放大器
- 精密使能端输入和漏极开路电源正常指示器（用于排序和控制）
- 固有保护 特性 可实现稳健设计
  - 间断模式过流保护
  - 具有迟滞的输入 UVLO
  - VCC 和栅极驱动 UVLO 保护
  - 具有迟滞的热关断保护
- 具有可湿性侧面的 VQFN-20 封装
- 使用 LM25145 并借助 WEBENCH® 电源设计器创建定制设计

2 应用

- 电信基础设施
- 工厂自动化
- 测试与测量
- 工业电机驱动

3 说明

LM25145 42V 同步降压控制器旨在对会发生高压瞬变的高输入电压源或输入电源轨的电压进行调节，从而最大限度地减少对外部浪涌抑制组件的需求。40ns 的高侧开关最短导通时间有助于获得较大的降压比，支持从 24V 标称输入到低电压轨的直接降压转换，从而降低系统的复杂性并减少解决方案成本。LM25145 在输入电压突降至 6V 时，仍能根据需要以接近 100% 的占空比继续工作，因此非常适用于高性能工业控制、机器人、数据通信和射频功率放大器 应用。

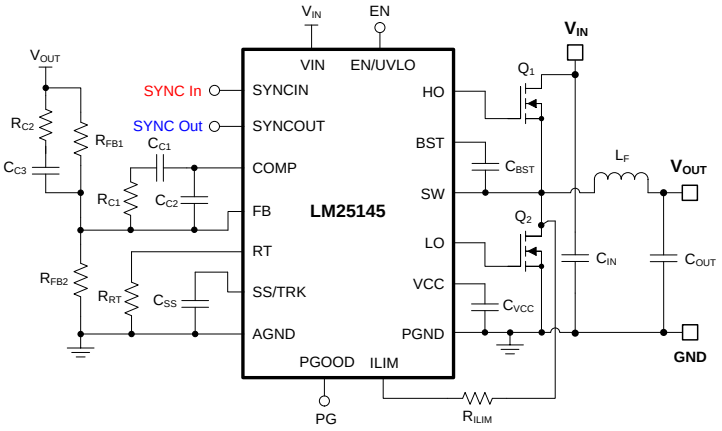
强制 PWM (FPWM) 模式运行可以消除频率变化以最大程度地降低 EMI，而用户可选的二极管仿真功能则可以降低轻负载条件下的电流消耗。逐周期过流保护可通过测量低侧 MOSFET 上的压降或使用可选电流感应电阻器来实现。高达 1MHz 的可调开关频率可同步至外部时钟源，以消除噪声敏感应用中的 拍频。

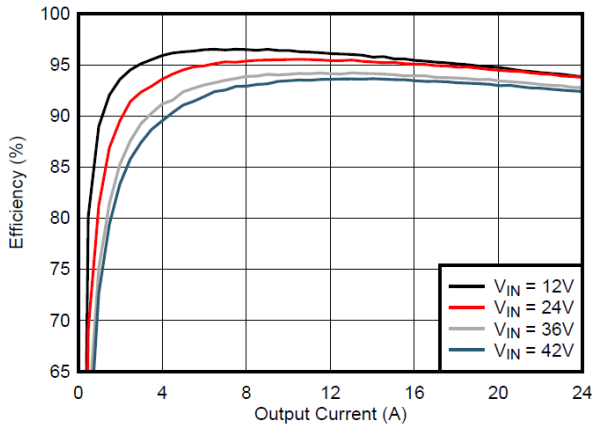
器件信息(1)

器件型号	封装	封装尺寸（标称值）
LM25145	VQFN (20)	3.50mm × 4.50mm

(1) 要了解所有可用封装，请参阅数据表末尾的可订购产品附录。

典型应用电路和效率性能，V_{OUT} = 5V，F_{SW} = 225kHz





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4 修订历史记录

日期	修订版本	注释
2017 年 6 月	*	最初发布版本

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5 说明（续）

LM25145 电压模式控制器使用适用于标准阈值 MOSFET 的可靠的 7.5V 栅极驱动器驱动外部高侧和低侧 N 通道电源开关。具有 2.3A 拉电流和 3.5A 灌电流能力的自适应定时栅极驱动器可在开关切换期间最大限度地减少体二极管导通，从而降低在以高输入电压和高频率驱动 MOSFET 时的开关损耗并提高热性能。LM25145 可从开关稳压器的输出或其他可用的源供电，从而进一步提高效率。

180° 异相时钟输出（相对于内部振荡器的同步输出）非常适用于级联或多通道电源，可降低输入电容器纹波电流和 EMI 滤波器尺寸。其他 的 LM25145 功能还包括可配置软启动、用于故障报告和输出监控的漏极开路电源正常监控、单调启动至预偏置负载、集成 VCC 偏置电源稳压器和自举二极管、外部电源跟踪、针对可调线路欠压锁定 (UVLO) 且具有迟滞的精密使能端输入、间断模式过载保护和带自动恢复的热关断保护。

LM25145 控制器采用 3.5mm × 4.5mm 热增强型 20 引脚 VQFN 封装，并为高电压引脚和可湿性侧面留出额外间距，以便对焊锡接点填角焊缝进行光学检测。

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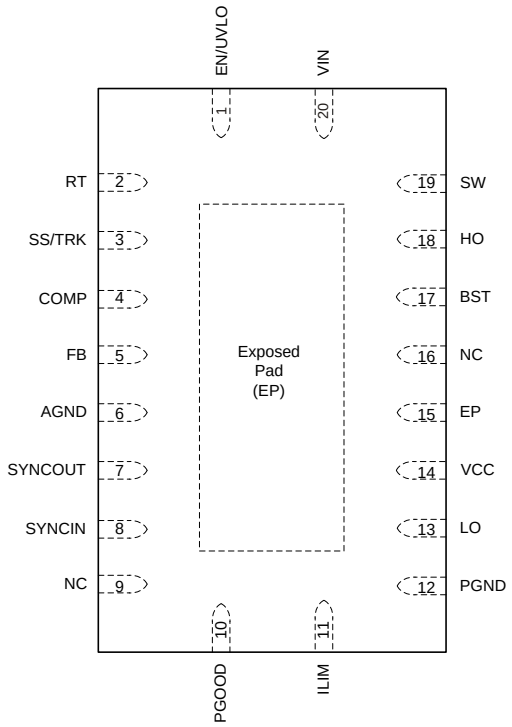
6 Pin Configuration and Functions

RGY Package
20-Pin VQFN With Wettable Flanks
Top View



Connect Exposed Pad on bottom to AGND and PGND on the PCB.

Pin Functions

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
1	EN/UVLO	I	Enable input and undervoltage lockout programming pin. If the EN/UVLO voltage is below 0.4 V, the controller is in the shutdown mode with all functions disabled. If the EN/UVLO voltage is greater than 0.4 V and less than 1.2 V, the regulator is in standby mode with the VCC regulator operational, the SS pin grounded, and no switching at the HO and LO outputs. If the EN/UVLO voltage is above 1.2 V, the SS/TRK pin is allowed to ramp and pulse-width modulated gate drive signals are delivered to the HO and LO pins. A 10-μA current source is enabled when EN/UVLO exceeds 1.2 V and flows through the external UVLO resistor divider to provide hysteresis. Hysteresis can be adjusted by varying the resistance of the external divider.
2	RT	I	Oscillator frequency adjust pin. The internal oscillator is programmed with a single resistor between RT and the AGND. The recommended maximum oscillator frequency is 1 MHz. An RT pin resistor is required even when using the SYNCIN pin to synchronize to an external clock.
3	SS/TRK	I	Soft-start and voltage tracking pin. An external capacitor and an internal 10-μA current source set the ramp rate of the error amplifier reference during start-up. When the SS/TRK pin voltage is less than 0.8 V, the SS/TRK voltage controls the noninverting input of the error amp. When the SS/TRK voltage exceeds 0.8 V, the amplifier is controlled by the internal 0.8-V reference. SS/TRK is discharged to ground during standby and fault conditions. After start-up, the SS/TRK voltage is clamped 115 mV above the FB pin voltage. If FB falls due to a load fault, SS/TRK is discharged to a level 115 mV above FB to provide a controlled recovery when the fault is removed. Voltage tracking can be implemented by connecting a low impedance reference between 0 V and 0.8 V to the SS/TRK pin. The 10-μA SS/TRK charging current flows into the reference and produces a voltage error if the impedance is not low. Connect a minimum capacitance from SS/TRK to AGND of 2.2 nF.
4	COMP	O	Low impedance output of the internal error amplifier. The loop compensation network should be connected between the COMP pin and the FB pin.
5	FB	I	Feedback connection to the inverting input of the internal error amplifier. A resistor divider from the output to this pin sets the output voltage level. The regulation threshold at the FB pin is nominally 0.8 V.

(1) P = Power, G = Ground, I = Input, O = Output.

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Pin Functions (continued)

PIN		TYPE (1)	DESCRIPTION
NO.	NAME		
6	AGND	P	Analog ground. Return for the internal 0.8-V voltage reference and analog circuits.
7	SYNCOUT	O	Synchronization output. Logic output that provides a clock signal that is 180° out-of-phase with the high-side FET gate drive. Connect SYNCOUT of the master LM25145 to the SYNCIN pin of a second LM25145 to operate two controllers at the same frequency with 180° interleaved high-side FET switch turnon transitions. Note that the SYNCOUT pin does not provide 180° interleaving when the controller is operating from an external clock that is different from the free-running frequency set by the RT resistor.
8	SYNCIN	I	Dual function pin for providing an optional clock input and for enabling diode emulation by the low-side MOSFET. Connecting a clock signal to the SYNCIN pin synchronizes switching to the external clock. Diode emulation by the low-side MOSFET is disabled when the controller is synchronized to an external clock, and negative inductor current can flow in the low-side MOSFET with light loads. A continuous logic low state at the SYNCIN pin enables diode emulation to prevent reverse current flow in the inductor. Diode emulation results in DCM operation at light loads, which improves efficiency. A logic high state at the SYNCIN pin disables diode emulation producing forced-PWM (FPWM) operation. During soft-start when SYNCIN is high or a clock signal is present, the LM25145 operates in diode emulation mode until the output is in regulation, then gradually increases the SW zero-cross threshold, resulting in a gradual transition from DCM to FPWM.
9	NC	—	No electrical connection.
10	PGOOD	O	Power Good indicator. This pin is an open-drain output. A high state indicates that the voltage at the FB pin is within a specified tolerance window centered at 0.8 V.
11	ILIM	I	Current limit adjust and current sense comparator input. A current sourced from the ILIM pin through an external resistor programs the threshold voltage for valley current limiting. The opposite end of the threshold adjust resistor can be connected to either the drain of the low-side MOSFET for $R_{DS(on)}$ sensing or to a current sense resistor connected to the source of the low-side FET.
12	PGND	P	Power ground return pin for the low-side MOSFET gate driver. Connect directly to the source of the low-side MOSFET or the ground side of a shunt resistor.
13	LO	P	Low-side MOSFET gate drive output. Connect to the gate of the low-side synchronous rectifier FET through a short, low inductance path.
14	VCC	O	Output of the 7.5-V bias regulator. Locally decouple to PGND using a low ESR/ESL capacitor located as close to the controller as possible. Controller bias can be supplied from an external supply that is greater than the internal VCC regulation voltage. Use caution when applying external bias to ensure that the applied voltage is not greater than the minimum VIN voltage and does not exceed the VCC pin maximum operating rating, see *Recommended Operating Conditions*.
15	EP	—	Pin internally connected to exposed pad of the package. Electrically isolated.
16	NC	—	No electrical connection.
17	BST	O	Bootstrap supply for the high-side gate driver. Connect to the bootstrap capacitor. The bootstrap capacitor supplies current to the high-side FET gate and should be placed as close to controller as possible. If an external bootstrap diode is used to reduce the time required to charge the bootstrap capacitor, connect the cathode of the diode to the BST pin and anode to VCC.
18	HO	P	High-side MOSFET gate drive output. Connect to the gate of the high-side MOSFET through a short, low inductance path.
19	SW	P	Switching node of the buck controller. Connect to the bootstrap capacitor, the source terminal of the high-side MOSFET and the drain terminal of the low-side MOSFET using short, low inductance paths.
20	VIN	P	Supply voltage input for the VCC LDO regulator.
—	EP	—	Exposed pad of the package. Electrically isolated. Solder to the system ground plane to reduce thermal resistance.

6.1 Wettable Flanks

100% automated visual inspection (AVI) post-assembly is typically required to meet requirements for high reliability and robustness. Standard quad-flat no-lead (VQFN) packages do not have solderable or exposed pins and terminals that are easily viewed. It is therefore difficult to determine visually whether or not the package is successfully soldered onto the printed-circuit board (PCB). The wettable-flank process was developed to resolve the issue of side-lead wetting of leadless packaging. The LM25145 is assembled using a 20-pin VQFN package with wettable flanks to provide a visual indicator of solderability, which reduces the inspection time and manufacturing costs.

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7 Specifications

7.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted).(1)

		MIN	MAX	UNIT
Input voltages	VIN	–0.3	45	V
	SW	–1	45	
	SW (20-ns transient)	–5	45	
	ILIM	–1	45	
	EN/UVLO	–0.3	45	
	VCC	–0.3	14	
	FB, COMP, SS/TRK, RT	–0.3	6	
	SYNCIN	–0.3	14	
Output voltages	BST	–0.3	60	V
	BST to VCC		45	
	BST to SW	–0.3	14	
	VCC to BST (20-ns transient)		7	
	LO (20-ns transient)	–3		
	PGOOD	–0.3	14	
Operating junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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7.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted).(1)

			MIN	NOM	MAX	UNIT
V_I	Input voltages	VIN	6		42	V
		SW	–1		42	
		ILIM	–1		42	
		External VCC bias rail	8		13	
		EN/UVLO	0		42	
V_O	Output voltages	BST	–0.3		55	V
		BST to VCC			42	
		BST to SW	5		13	
		PGOOD			13	
I_{SINK}, I_{SRC}	Sink/source currents	SYNCOUT	–1		1	mA
		PGOOD			2	
T_J	Operating junction temperature		–40		125	°C

(1) *Recommended Operating Conditions* are conditions under which the device is intended to be functional. For specifications and test conditions, see *Electrical Characteristics*.

7.4 Thermal Information

THERMAL METRIC(1)		LM25145 RGY (VQFN) 20 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	11.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 24 V, $V_{EN/UVLO}$ = 1.5 V, R_{RT} = 25 kΩ unless otherwise stated.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT SUPPLY						
V_{IN}	Operating input voltage range		6		42	V
I_{Q-RUN}	Operating input current, not switching	$V_{EN/UVLO}$ = 1.5 V, $V_{SS/TRK}$ = 0 V		1.8	2.1	mA
I_{Q-STBY}	Standby input current	$V_{EN/UVLO}$ = 1 V		1.75	2	mA
I_{Q-SDN}	Shutdown input current	$V_{EN/UVLO}$ = 0 V, V_{VCC} < 1 V		13.5	16	µA
VCC REGULATOR						
V_{VCC}	VCC regulation voltage	$V_{SS/TRK}$ = 0 V, 9 V ≤ V_{VIN} ≤ 42 V, 0 mA < I_{VCC} ≤ 20 mA	7.3	7.5	7.7	V
$V_{VCC-LDO}$	VIN to VCC dropout voltage	V_{VIN} = 6 V, $V_{SS/TRK}$ = 0 V, I_{VCC} = 20 mA		0.25	0.63	V
I_{SC-LDO}	VCC short-circuit current	$V_{SS/TRK}$ = 0 V, V_{VCC} = 0 V	40	50	70	mA
V_{VCC-UV}	VCC undervoltage threshold	V_{VCC} rising	4.8	4.93	5.2	V
$V_{VCC-UVH}$	VCC undervoltage hysteresis	Rising threshold – falling threshold		0.26		V

(1) All minimum and maximum limits are specified by correlating the electrical characteristics to process and temperature variations and applying statistical process control.
(2) The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (P_D in Watts) as follows: $T_J = T_A + (P_D \bullet R_{\theta JA})$ where $R_{\theta JA}$ (in °C/W) is the package thermal impedance provided in *Thermal Information*.

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Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 24 V, $V_{EN/UVLO}$ = 1.5 V, R_{RT} = 25 kΩ unless otherwise stated.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{VCC-EXT}$	Minimum external bias supply voltage	Voltage required to disable VCC regulator	8			V
I_{VCC}	External VCC input current, not switching	$V_{SS/TRK}$ = 0 V, V_{VCC} = 13 V			2.1	mA
ENABLE AND INPUT UVLO						
V_{SDN}	Shutdown to standby threshold	$V_{EN/UVLO}$ rising		0.42		V
$V_{SDN-HYS}$	Shutdown threshold hysteresis	EN/UVLO rising – falling threshold		50		mV
V_{EN}	Standby to operating threshold	$V_{EN/UVLO}$ rising	1.164	1.2	1.236	V
I_{EN-HYS}	Standby to operating hysteresis current	$V_{EN/UVLO}$ = 1.5 V	9	10	11	µA
ERROR AMPLIFIER						
V_{REF}	FB reference voltage	FB connected to COMP	792	800	808	mV
$I_{FB-BIAS}$	FB input bias current	V_{FB} = 0.8 V	–0.1		0.1	µA
$V_{COMP-OH}$	COMP output high voltage	V_{FB} = 0 V, COMP sourcing 1 mA		5		V
$V_{COMP-OL}$	COMP output low voltage	COMP sinking 1 mA			0.3	V
AVOL	DC gain			94		dB
GBW	Unity gain bandwidth			6.5		MHz
SOFT-START AND VOLTAGE TRACKING						
I_{SS}	SS/TRK capacitor charging current	$V_{SS/TRK}$ = 0 V	8.5	10	12	µA
R_{SS}	SS/TRK discharge FET resistance	$V_{EN/UVLO}$ = 1 V, $V_{SS/TRK}$ = 0.1 V		11		Ω
V_{SS-FB}	SS/TRK to FB offset		–15		15	mV
$V_{SS-CLAMP}$	SS/TRK clamp voltage	$V_{SS/TRK}$ – V_{FB}, V_{FB} = 0.8 V		115		mV
POWER GOOD INDICATOR						
PG_{UTH}	FB upper threshold for PGOOD high to low	% of V_{REF}, V_{FB} rising	106%	108%	110%	
PG_{LTH}	FB lower threshold for PGOOD high to low	% of V_{REF}, V_{FB} falling	90%	92%	94%	
PG_{HYS_U}	PGOOD upper threshold hysteresis	% of V_{REF}		3%		
PG_{HYS_L}	PGOOD lower threshold hysteresis	% of V_{REF}		2%		
$T_{PG-RISE}$	PGOOD rising filter	FB to PGOOD rising edge		25		µs
$T_{PG-FALL}$	PGOOD falling filter	FB to PGOOD falling edge		25		µs
V_{PG-OL}	PGOOD low state output voltage	V_{FB} = 0.9 V, I_{PGOOD} = 2 mA			150	mV
I_{PG-OH}	PGOOD high state leakage current	V_{FB} = 0.8 V, V_{PGOOD} = 13 V			100	nA
OSCILLATOR						
F_{SW1}	Oscillator Frequency – 1	R_{RT} = 100 kΩ		100		kHz
F_{SW2}	Oscillator Frequency – 2	R_{RT} = 25 kΩ	380	400	420	kHz
F_{SW3}	Oscillator Frequency – 3	R_{RT} = 12.5 kΩ		780		kHz
SYNCHRONIZATION INPUT AND OUTPUT						
F_{SYNC}	SYNCIN external clock frequency range	% of nominal frequency set by R_{RT}	–20%		+50%	
$V_{SYNC-IH}$	Minimum SYNCIN input logic high		2			V
$V_{SYNC-IL}$	Maximum SYNCIN input logic low				0.8	V
R_{SYNCIN}	SYNCIN input resistance	V_{SYNCIN} = 3 V		20		kΩ
$T_{SYNCI-PW}$	SYNCIN input minimum pulsewidth	Minimum high state or low state duration	50			ns
$V_{SYNCO-OH}$	SYNCOUT high state output voltage	$I_{SYNCOUT}$ = –1 mA (sourcing)	3			V
$V_{SYNCO-OL}$	SYNCOUT low state output voltage	$I_{SYNCOUT}$ = 1 mA (sinking)			0.4	V
$T_{SYNCOUT}$	Delay from HO rising to SYNCOUT leading edge	V_{SYNCIN} = 0 V, T_S = 1/F_{SW}, F_{SW} set by R_{RT}		T_S/2 – 140		ns

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Electrical Characteristics (continued)

Typical values correspond to T_J = 25°C. Minimum and maximum limits apply over the –40°C to 125°C junction temperature range unless otherwise stated. V_{IN} = 24 V, $V_{EN/UVLO}$ = 1.5 V, R_{RT} = 25 kΩ unless otherwise stated.(1)(2)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SYNCIN}	Delay from SYNCIN leading edge to HO rising	50% to 50%		150		ns
BOOTSTRAP DIODE AND UNDERVOLTAGE THRESHOLD						
$V_{BST-FWD}$	Diode forward voltage, VCC to BST	VCC to BST, BST pin sourcing 20 mA		0.75	0.9	V
I_{Q-BST}	BST to SW quiescent current, not switching	$V_{SS/TRK}$ = 0 V, V_{SW} = 24 V, V_{BST} = 30 V		80		µA
V_{BST-UV}	BST to SW undervoltage detection	V_{BST} – V_{SW} falling		3.4		V
$V_{BST-HYS}$	BST to SW undervoltage hysteresis	V_{BST} – V_{SW} rising		0.42		V
PWM CONTROL						
$T_{ON(MIN)}$	Minimum controllable on-time	V_{BST} – V_{SW} = 7 V, HO 50% to 50%		40	60	ns
$T_{OFF(MIN)}$	Minimum off-time	V_{BST} – V_{SW} = 7 V, HO 50% to 50%		140	200	ns
DC_{100kHz}	Maximum duty cycle	F_{SW} = 100 kHz, 6 V ≤ V_{VIN} ≤ 42 V	98%	99%		
DC_{400kHz}		F_{SW} = 400 kHz, 6 V ≤ V_{VIN} ≤ 42 V	90%	94%		
$V_{RAMP(min)}$	Ramp valley voltage (COMP at 0% duty cycle)			300		mV
k_{FF}	PWM feedforward gain (V_{IN} / V_{RAMP})	6 V ≤ V_{VIN} ≤ 42 V		15		V/V
OVERCURRENT PROTECT (OCP) – VALLEY CURRENT LIMITING						
I_{RS}	ILIM source current, R_{SENSE} mode	Low voltage detected at ILIM	90	100	110	µA
I_{RDSON}	ILIM source current, $R_{DS(on)}$ mode	SW voltage detected at ILIM, T_J = 25°C	180	200	220	µA
I_{RSTC}	ILIM current tempco	R_{DS-ON} mode		4500		ppm/°C
$I_{RDSONTC}$	ILIM current tempco	R_{SENSE} mode		0		ppm/°C
$V_{ILIM-TH}$	ILIM comparator threshold at ILIM		–8	–2	3.5	mV
SHORT-CIRCUIT PROTECT (SCP) – DUTY CYCLE CLAMP						
$V_{CLAMP-OS}$	Clamp offset voltage – no current limiting	CLAMP to COMP steady state offset voltage		0.2 + V_{VIN}/75		V
$V_{CLAMP-MIN}$	Minimum clamp voltage	CLAMP voltage with continuous current limiting		0.3 + V_{VIN}/150		V
HICCUP MODE FAULT PROTECTION						
$C_{HICC-DEL}$	Hiccup mode activation delay	Clock cycles with current limiting before hiccup off-time activated		128		cycles
C_{HICCUP}	Hiccup mode off-time after activation	Clock cycles with no switching followed by SS/TRK release		8192		cycles
DIODE EMULATION						
V_{ZCD-SS}	Zero-cross detect (ZCD) soft-start ramp	ZCD threshold measured at SW pin 50 clock cycles after first HO pulse		0		mV
$V_{ZCD-DIS}$	Zero-cross detect disable threshold (CCM)	ZCD threshold measured at SW pin 1000 clock cycles after first HO pulse		200		mV
V_{DEM-TH}	Diode emulation zero-cross threshold	Measured at SW with V_{SW} rising	–5	0	5	mV
GATE DRIVERS						
R_{HO-UP}	HO high-state resistance, HO to BST	V_{BST} – V_{SW} = 7 V, I_{HO} = –100 mA		1.5		Ω
$R_{HO-DOWN}$	HO low-state resistance, HO to SW	V_{BST} – V_{SW} = 7 V, I_{HO} = 100 mA		0.9		Ω
R_{LO-UP}	LO high-state resistance, LO to VCC	V_{BST} – V_{SW} = 7 V, I_{LO} = –100 mA		1.5		Ω
$R_{LO-DOWN}$	LO low-state resistance, LO to PGND	V_{BST} – V_{SW} = 7 V, I_{LO} = 100 mA		0.9		Ω
I_{HOH}, I_{LOH}	HO, LO source current	V_{BST} – V_{SW} = 7 V, HO = SW, LO = AGND		2.3		A
I_{HOL}, I_{LOL}	HO, LO sink current	V_{BST} – V_{SW} = 7 V, HO = BST, LO = VCC		3.5		A
THERMAL SHUTDOWN						
T_{SD}	Thermal shutdown threshold	T_J rising		175		°C
T_{SD-HYS}	Thermal shutdown hysteresis			20		°C

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7.6 Switching Characteristics

Over operating free-air temperature range (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{HO-TR} T_{LO-TR}	HO, LO rise times	$V_{BST} – V_{SW}$ = 7 V, C_{LOAD} = 1 nF, 20% to 80%		7		ns
T_{HO-TF} T_{LO-TF}	HO, LO fall times	$V_{BST} – V_{SW}$ = 7 V, C_{LOAD} = 1 nF, 80% to 20%		4		ns
T_{HO-DT}	HO turnon dead time	$V_{BST} – V_{SW}$ = 7 V, LO off to HO on, 50% to 50%		14		ns
T_{LO-DT}	LO turnon dead time	$V_{BST} – V_{SW}$ = 7 V, HO off to LO on, 50% to 50%		14		ns

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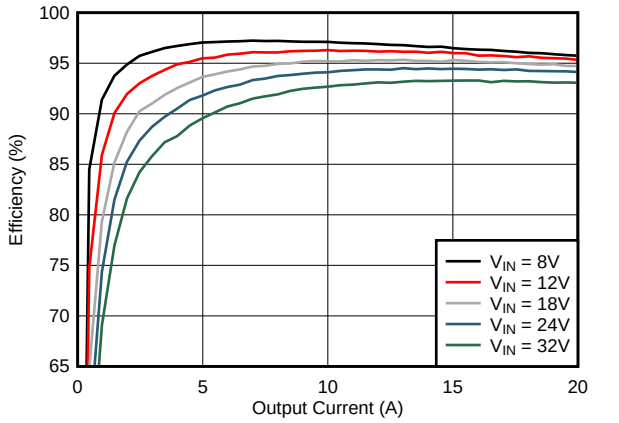
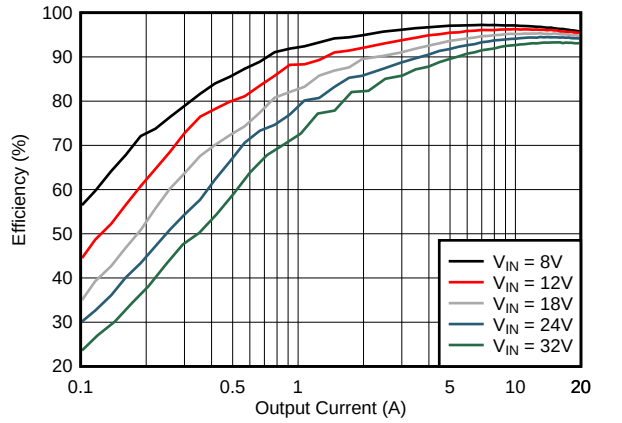
7.7 Typical Characteristics

V_{VIN} = 24 V, R_{RT} = 25 kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN (unless otherwise noted).



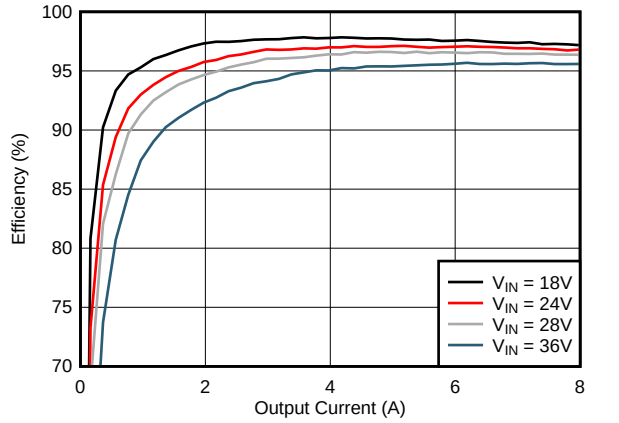
V_{OUT} = 5 V
See Figure 46
V_{SYNCIN} = V_{VCC}
F_{SW} = 500 kHz
R_{RT} = 20 kΩ

Figure 1. Efficiency vs Load, CCM



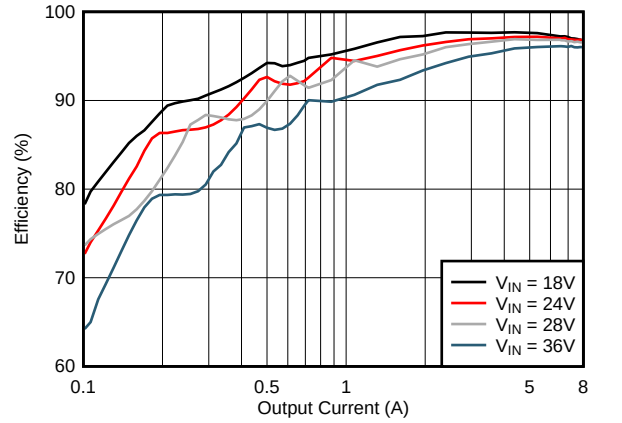
V_{OUT} = 5 V
See Figure 46
V_{SYNCIN} = 0 V
F_{SW} = 500 kHz
R_{RT} = 20 kΩ

Figure 2. Efficiency vs Load, DCM



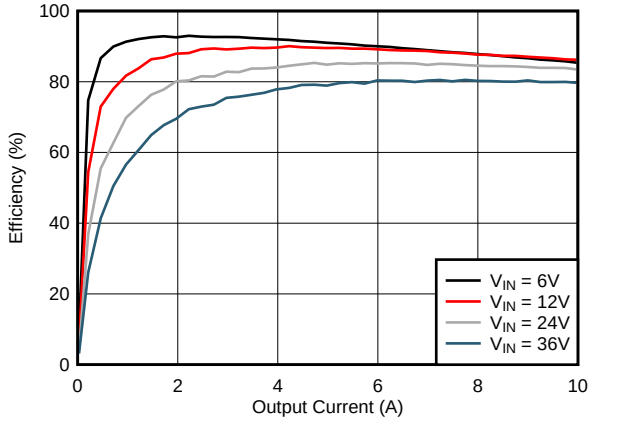
V_{OUT} = 12 V
See Figure 57
V_{SYNCIN} = V_{VCC}
F_{SW} = 425 kHz
R_{RT} = 23.7 kΩ

Figure 3. Efficiency vs Load, CCM



V_{OUT} = 12 V
See Figure 57
V_{SYNCIN} = 0 V
F_{SW} = 425 kHz
R_{RT} = 23.7 kΩ

Figure 4. Efficiency vs Load, DCM (V_{OUT} Supplies Bias Power to VCC)



V_{OUT} = 1.1 V
See Figure 70
F_{SW} = 300 kHz
R_{RT} = 33.2 kΩ

Figure 5. Efficiency vs Load, CCM

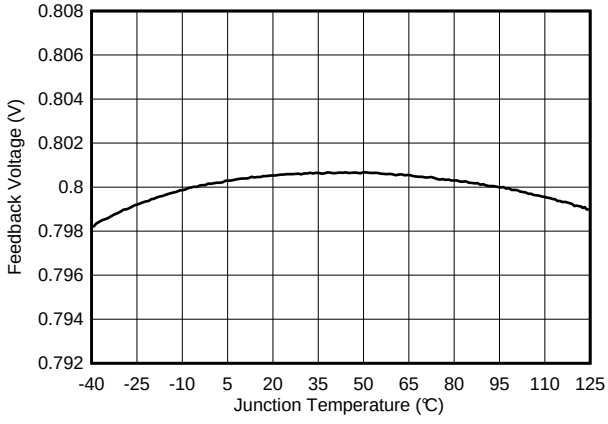


Figure 6. FB Voltage vs Junction Temperature

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Typical Characteristics (continued)

V_{VIN} = 24 V, R_{RT} = 25 kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN (unless otherwise noted).

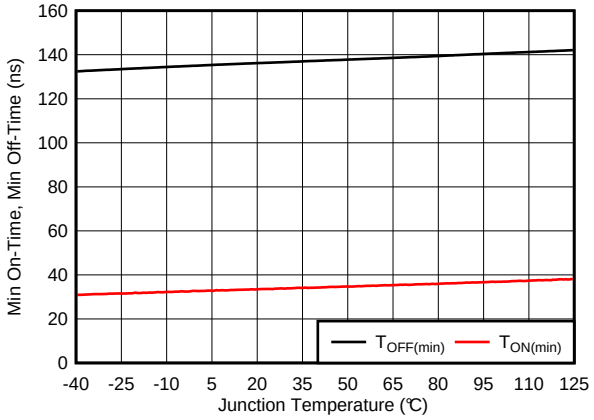
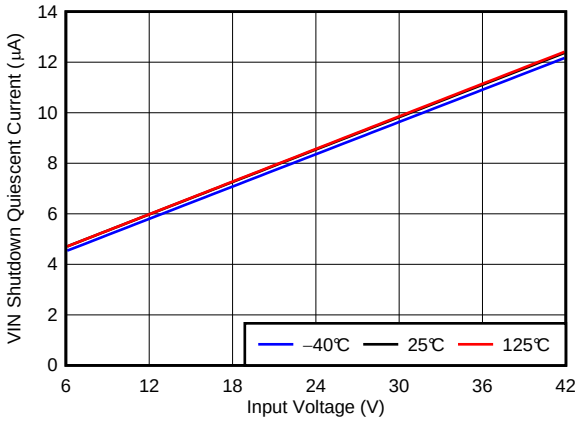
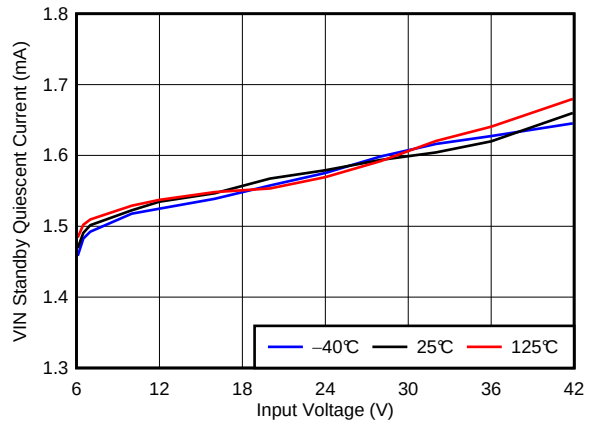


Figure 7. $T_{ON(min)}$ and $T_{OFF(min)}$ vs Junction Temperature



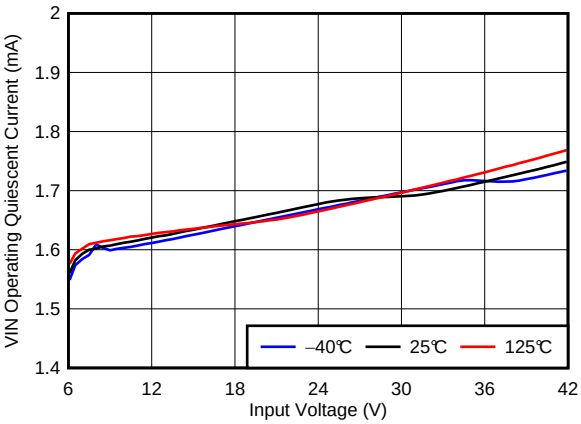
V_{SW} = 0 V $V_{EN/UVLO}$ = 0 V

Figure 8. I_{Q-SHD} vs Input Voltage



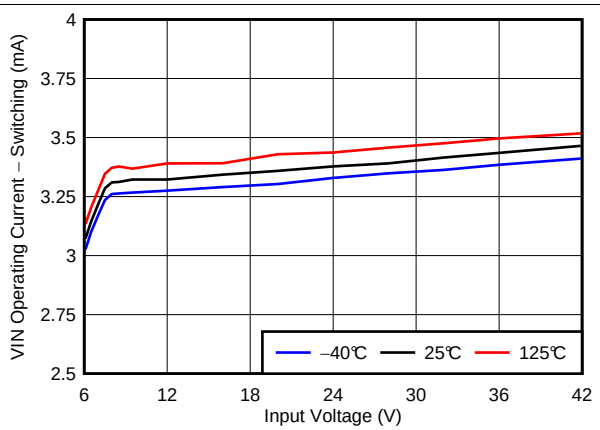
V_{SW} = 0 V $V_{EN/UVLO}$ = 1 V

Figure 9. $I_{Q-STANDBY}$ vs Input Voltage



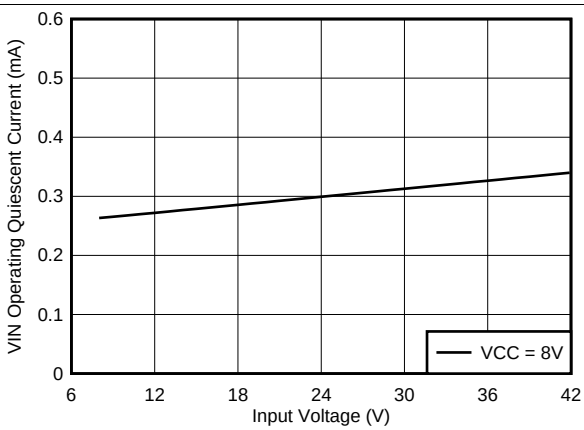
V_{SW} = 0 V $V_{EN/UVLO}$ = V_{VIN} $V_{SS/TRK}$ = 0 V

Figure 10. $I_{Q-OPERATING}$ (Nonswitching) vs Input Voltage



V_{SW} = 0 V HO, LO Open

Figure 11. $I_{Q-OPERATING}$ (Switching) vs Input Voltage



V_{SW} = 0 V V_{VCC} = V_{BST} = V_{ILIM} V_{FB} = 0 V

Figure 12. VIN Quiescent Current With External VCC Applied

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Typical Characteristics (continued)

V_{VIN} = 24 V, R_{RT} = 25 kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN (unless otherwise noted).

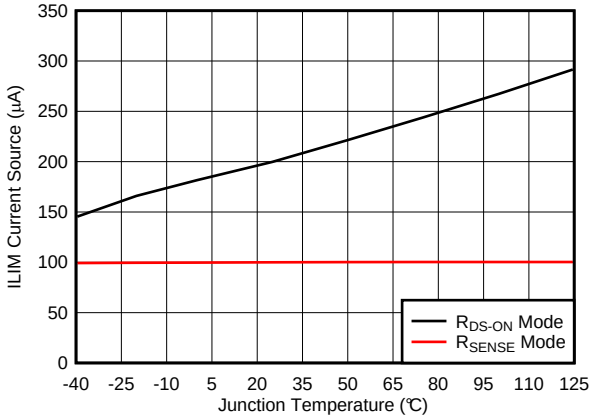
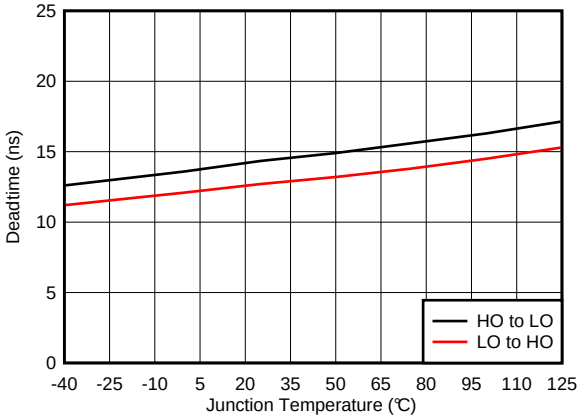


Figure 13. ILIM Current Source vs Junction Temperature



V_{SW} = 0 V

Figure 14. Dead Time vs Junction Temperature

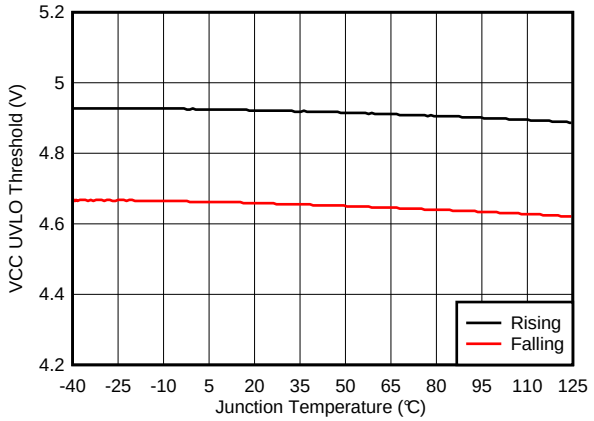


Figure 15. VCC UVLO Thresholds vs Junction Temperature

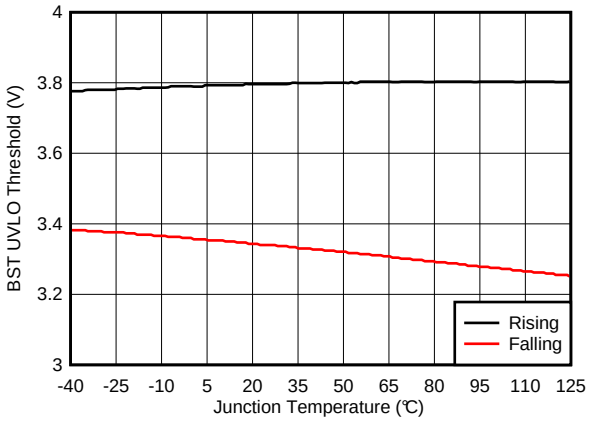


Figure 16. BST UVLO Thresholds vs Junction Temperature

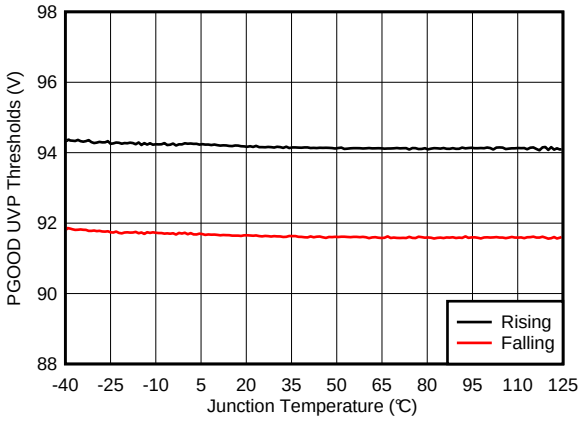


Figure 17. PGOOD UVP Thresholds vs Junction Temperature

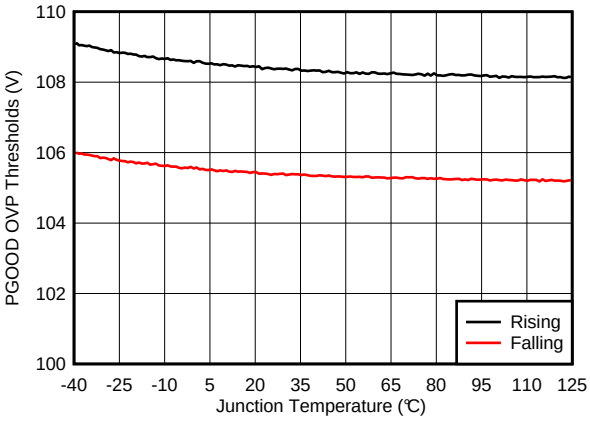


Figure 18. PGOOD OVP Thresholds vs Junction Temperature

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Typical Characteristics (continued)

V_{VIN} = 24 V, R_{RT} = 25 kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN (unless otherwise noted).

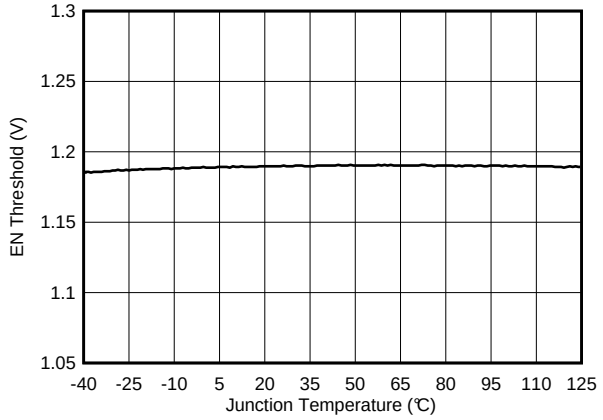


Figure 19. EN/UVLO Threshold vs Junction Temperature

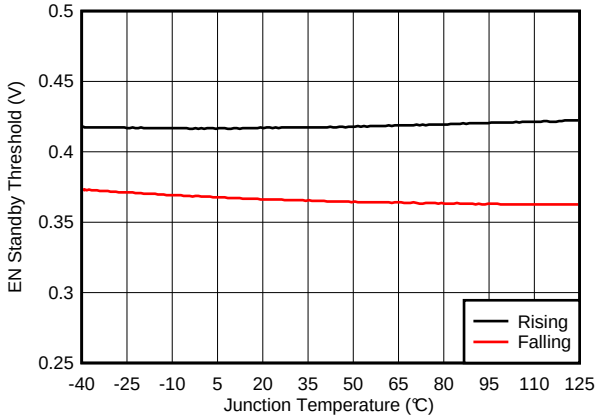
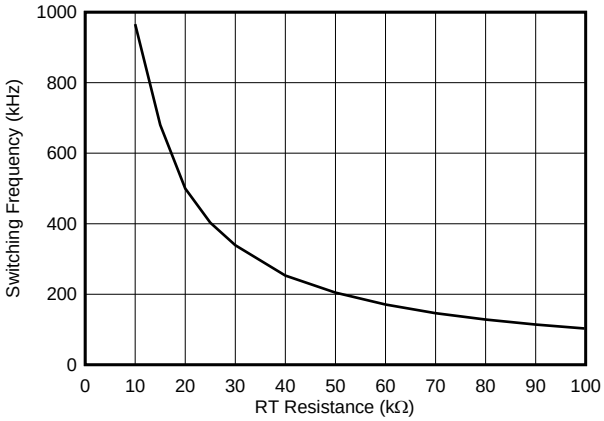


Figure 20. EN Standby Thresholds vs Junction Temperature



V_{SW} = 0 V

Figure 21. Oscillator Frequency vs RT Resistance

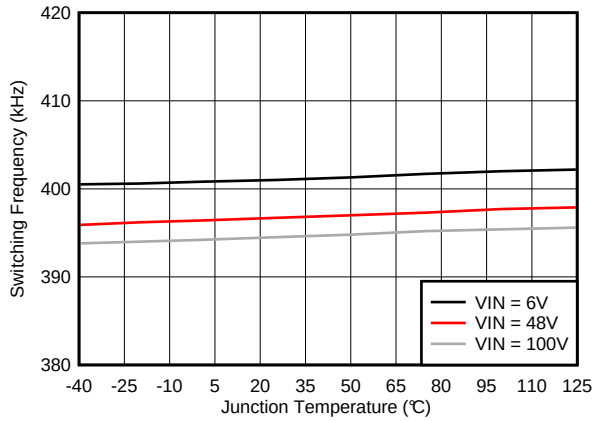


Figure 22. Oscillator Frequency vs Junction Temperature

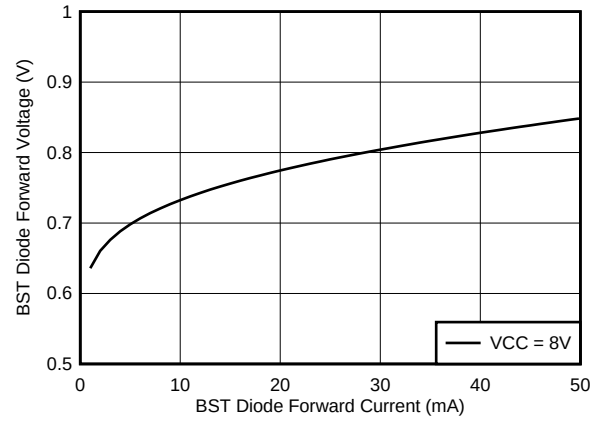


Figure 23. BST Diode Forward Voltage vs Current

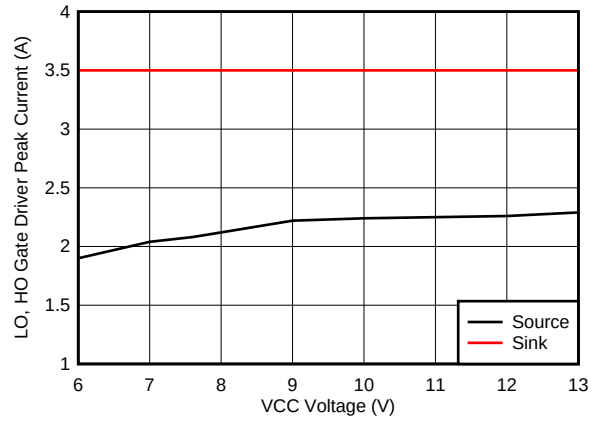


Figure 24. Gate Driver Peak Current vs VCC Voltage

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Typical Characteristics (continued)

V_{VIN} = 24 V, R_{RT} = 25 kΩ, SYNCIN tied to VCC, EN/UVLO tied to VIN (unless otherwise noted).

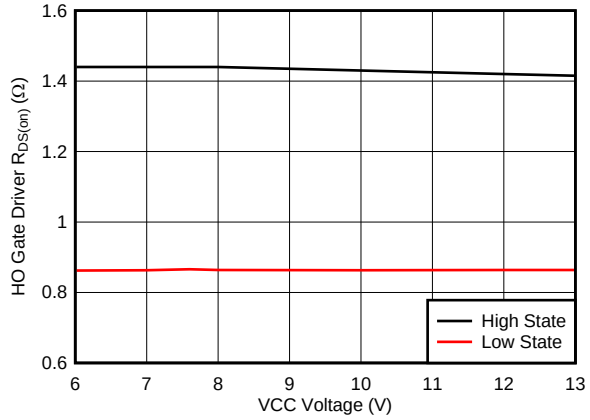


Figure 25. HO Driver Resistance vs VCC Voltage

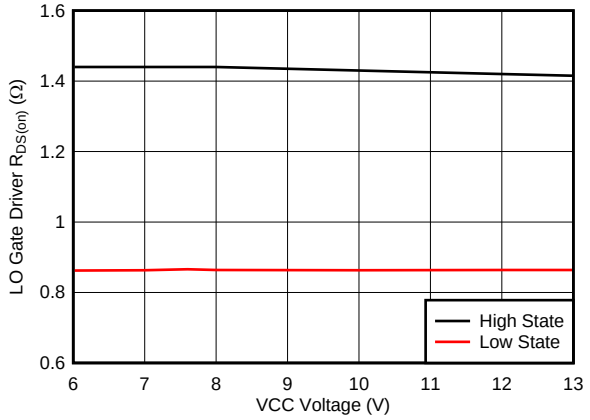
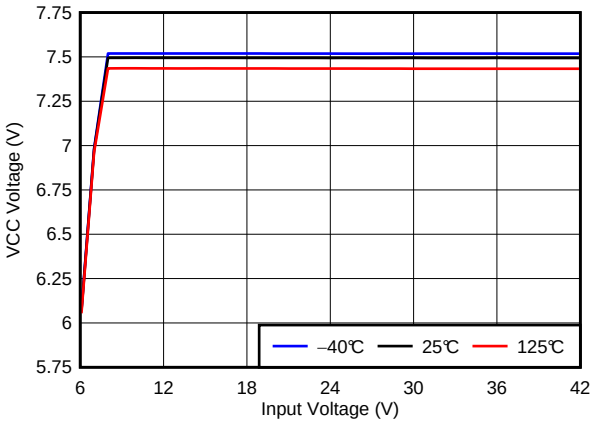
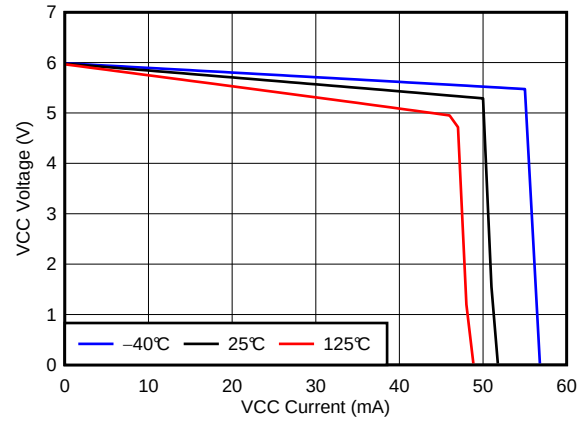


Figure 26. LO Driver Resistance vs VCC Voltage



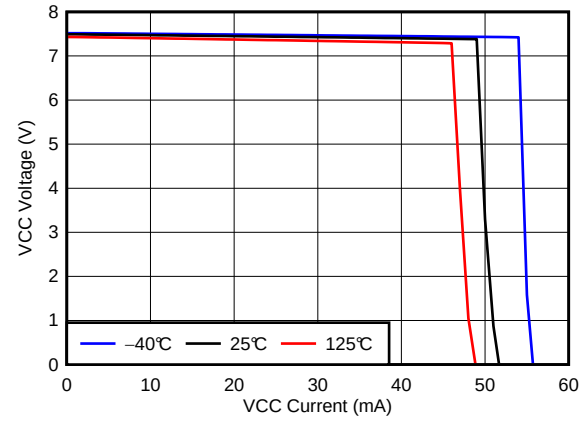
$V_{SS/TRK}$ = 0 V

Figure 27. VCC Voltage vs Input Voltage



V_{IN} = 6 V

Figure 28. VCC vs ICC Characteristic



V_{IN} = 12 V

Figure 29. VCC vs ICC Characteristic

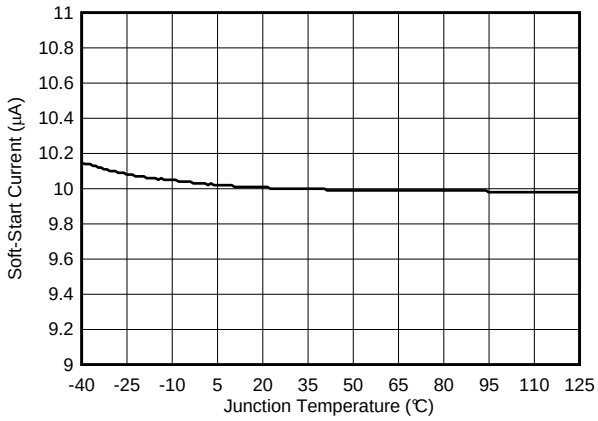


Figure 30. SS/TRK Current Source vs Junction Temperature

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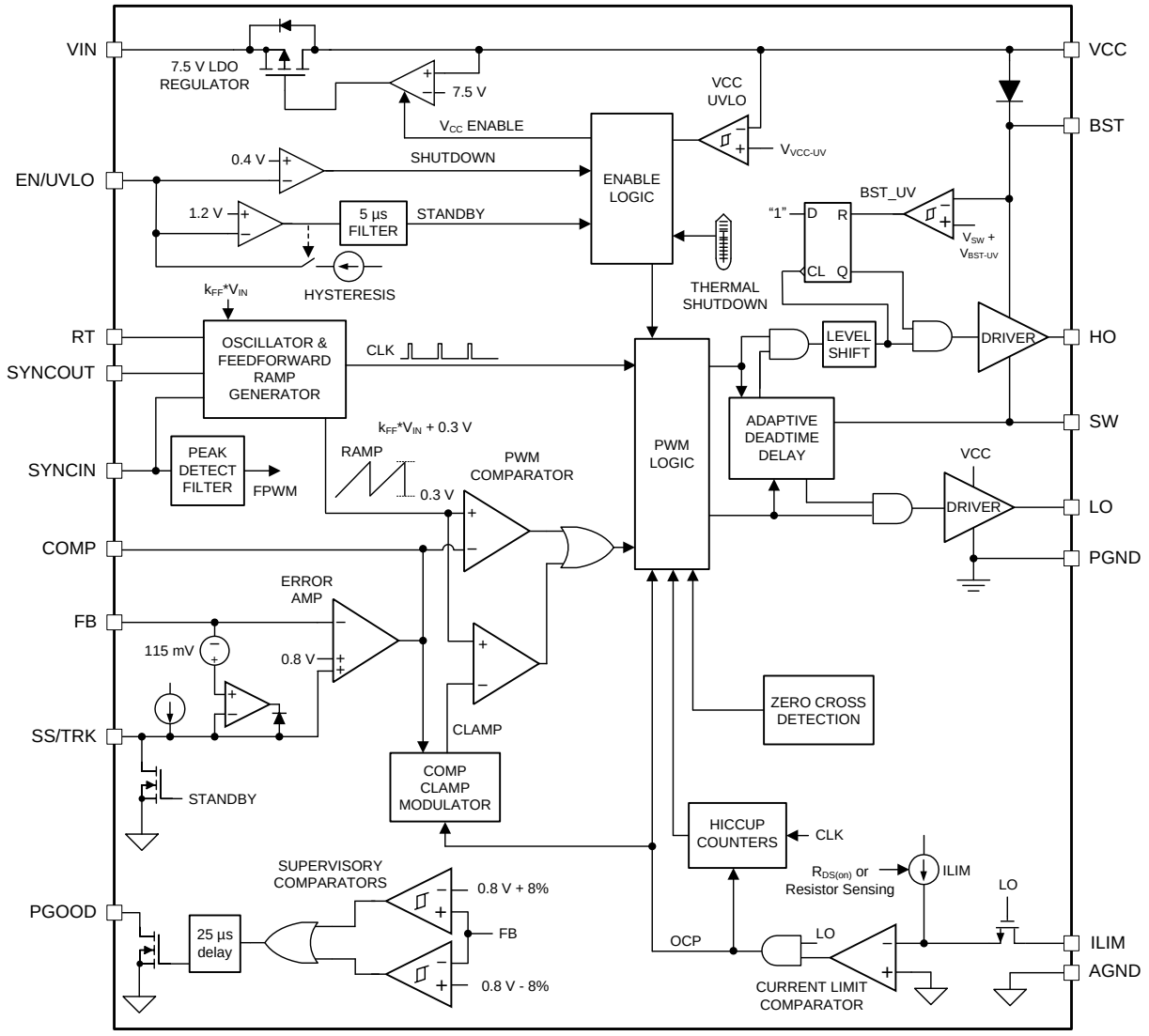
8 Detailed Description

8.1 Overview

The LM25145 is a 42-V synchronous buck controller that features all of the functions necessary to implement a high efficiency step-down power supply with output voltage ranging from 0.8 V to 40 V. The voltage-mode control architecture uses input feedforward for excellent line transient response over a wide V_{IN} range. Voltage-mode control supports the wide duty cycle range for high input voltage and low dropout applications as well as when a high voltage conversion ratio (for example, 10-to-1) is required. Current sensing for cycle-by-cycle current limit can be implemented with either the low-side FET $R_{DS(on)}$ or a current sense resistor. The operating frequency is programmable from 100 kHz to 1 MHz. The LM25145 drives external high-side and low-side NMOS power switches with robust 7.5-V gate drivers suitable for standard threshold MOSFETs. Adaptive dead-time control between the high-side and low-side drivers is designed to minimize body diode conduction during switching transitions. An external bias supply can be connected to the VCC pin to improve efficiency in high-voltage applications. A user-selectable diode emulation feature enables discontinuous conduction mode operation for improved efficiency and lower dissipation at light-load conditions.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Input Range (VIN)

The LM25145 operational input voltage range is from 6 V to 42 V. The device is intended for step-down conversions from 12-V, 24-V, 28-V and 36-V unregulated, semiregulated, and fully-regulated supply rails. The application circuit of Figure 31 shows all the necessary components to implement an LM25145-based wide-V_{IN} step-down regulator using a single supply. The LM25145 uses an internal LDO subregulator to provide a 7.5-V VCC bias rail for the gate drive and control circuits (assuming the input voltage is higher than 7.5 V plus the necessary subregulator dropout specification).

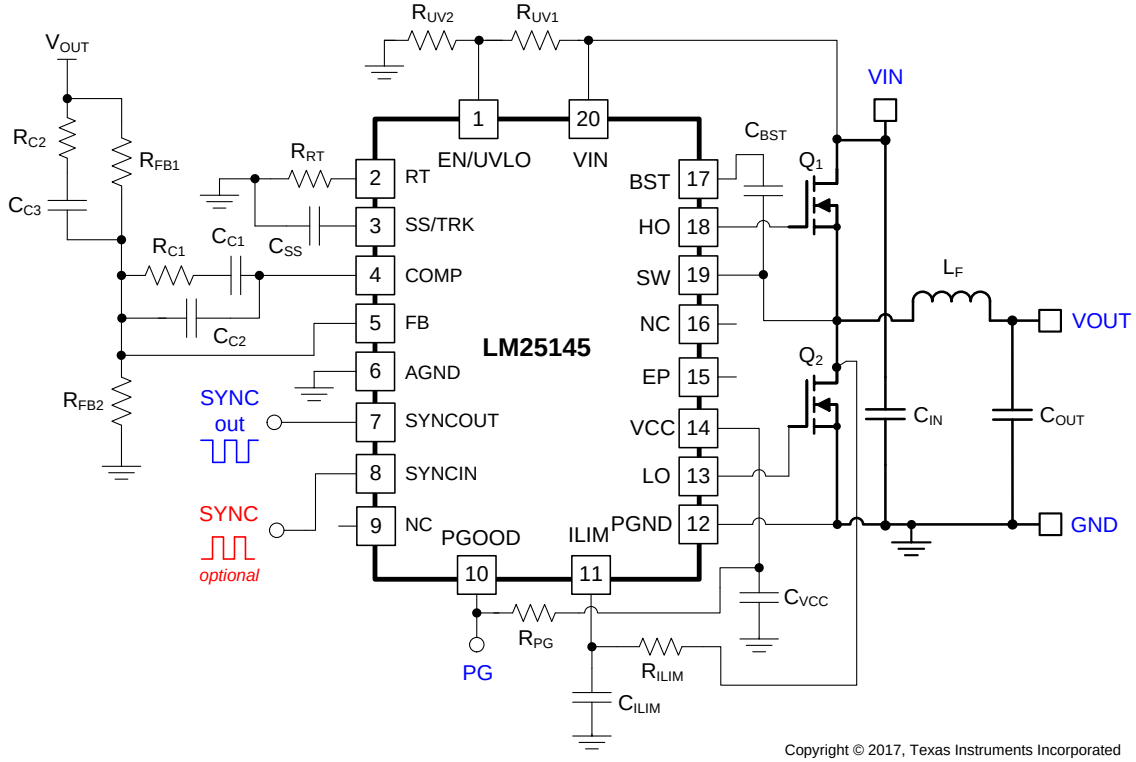

Figure 31. Schematic Diagram for VIN Operating Range of 6 V to 42 V

In high voltage applications, take extra care to ensure the VIN pin does not exceed the absolute maximum voltage rating of 55 V during line or load transient events. Voltage ringing on the VIN pin that exceeds the *Absolute Maximum Ratings* can damage the IC. Use high-quality ceramic input capacitors to minimize ringing. An RC filter from the input rail to the VIN pin (for example, 4.7 Ω and 0.1 µF) provides supplementary filtering at the VIN pin.

8.3.2 Output Voltage Setpoint and Accuracy (FB)

The reference voltage at the FB pin is set at 0.8 V with a feedback system accuracy over the full junction temperature range of ±1%. Junction temperature range for the device is –40°C to +125°C. While dependent on switching frequency and load current levels, the LM25145 is generally capable of providing output voltages in the range of 0.8 V to a maximum of slightly less than VIN. The DC output voltage setpoint during normal operation is set by the feedback resistor network, R_{FB1} and R_{FB2}, connected to the output.

8.3.3 High-Voltage Bias Supply Regulator (VCC)

The LM25145 contains an internal high-voltage VCC regulator that provides a bias supply for the PWM controller and its gate drivers for the external MOSFETs. The input pin (VIN) can be connected directly to an input voltage source up to 42 V. The output of the VCC regulator is set to 7.5 V. However, when the input voltage is below the VCC setpoint level, the VCC output tracks V_{IN} with a small voltage drop. Connect a ceramic decoupling capacitor between 1 µF and 5 µF from VCC to AGND for stability.

Feature Description (continued)

The VCC regulator output has a current limit of 40 mA (minimum). At power up, the regulator sources current into the capacitor connected to the VCC pin. When the VCC voltage exceeds its rising UVLO threshold of 4.93 V, the output is enabled (if EN/UVLO is above 1.2 V) and the soft-start sequence begins. The output remain active until the VCC voltage falls below its falling UVLO threshold of 4.67 V (typical) or if EN/UVLO goes to a standby or shutdown state.

Internal power dissipation of the VCC regulator can be minimized by connecting the output voltage or an auxiliary bias supply rail (up to 13 V) to VCC using a diode D_{VCC} as shown in Figure 32. A diode in series with the input prevents reverse current flow from VCC to VIN if the input voltage falls below the external VCC rail.

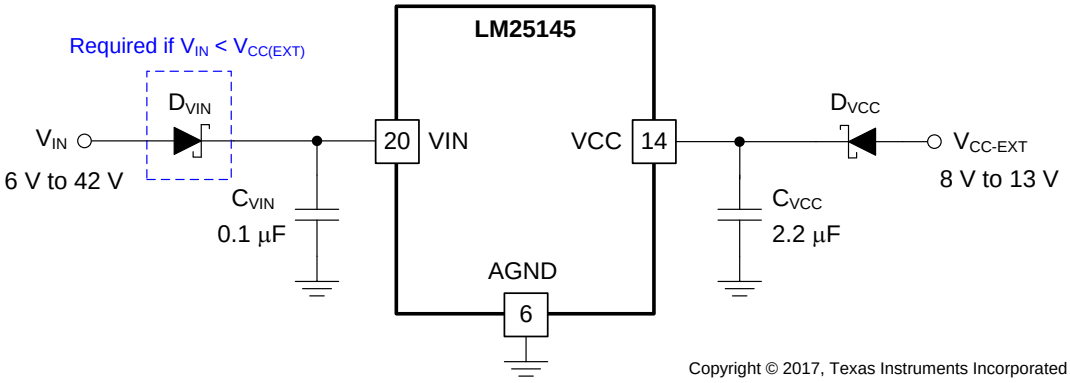

Figure 32. VCC Bias Supply Connection From VOUT or Auxiliary Supply

Note that a finite bias supply regulator dropout voltage exists and is manifested to a larger extent when driving high gate charge (Q_G) power MOSFETs at elevated switching frequencies. For example, at V_{VIN} = 6 V, the VCC voltage is 5.8 V with a DC operating current, I_{VCC}, of 20 mA. Such a low gate drive voltage may be insufficient to fully enhance the power MOSFETs. At the very least, MOSFET on-state resistance, $R_{DS(ON)}$, may increase at such low gate drive voltage.

Here are the main considerations when operating at input voltages below 7.5 V:

- Increased MOSFET $R_{DS(on)}$ at lower V_{GS}, leading to Increased conduction losses and reduced OCP setpoint.
- Increased switching losses given the slower switching times when operating at lower gate voltages.
- Restricted range of suitable power MOSFETs to choose from (MOSFETs with $R_{DS(on)}$ rated at V_{GS} = 4.5 V become mandatory).

8.3.4 Precision Enable (EN/UVLO)

The EN/UVLO input supports adjustable input undervoltage lockout (UVLO) with hysteresis programmed by the resistor values for application specific power-up and power-down requirements. EN/UVLO connects to a comparator-based input referenced to a 1.2-V bandgap voltage. An external logic signal can be used to drive the EN/UVLO input to toggle the output ON and OFF and for system sequencing or protection. The simplest way to enable the operation of the LM25145 is to connect EN/UVLO directly to VIN. This allows self start-up of the LM25145 when V_{CC} is within its valid operating range. However, many applications benefit from using a resistor divider R_{UV1} and R_{UV2} as shown in Figure 33 to establish a precision UVLO level.

Use Equation 1 and Equation 2 to calculate the UVLO resistors given the required input turnon and turnoff voltages.

$$R_{UV1} = \frac{V_{IN(on)} - V_{IN(off)}}{I_{HYS}} \quad (1)$$

$$R_{UV2} = R_{UV1} \cdot \frac{V_{EN}}{V_{IN(on)} - V_{EN}} \quad (2)$$

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Feature Description (continued)

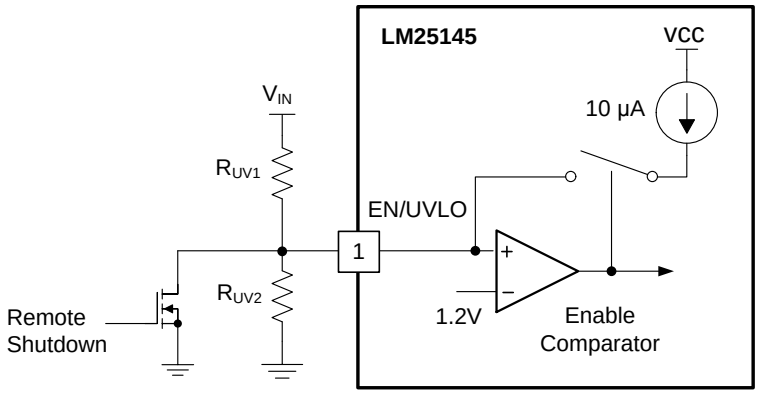

Figure 33. Programmable Input Voltage UVLO Turnon and Turnoff

The LM25145 enters a low I_Q shutdown mode when EN/UVLO is pulled below approximately 0.4 V. The internal LDO regulator powers off and the internal bias supply rail collapses, shutting down the bias currents of the LM25145. The LM25145 operates in standby mode when the EN/UVLO voltage is between the hard shutdown and precision enable (standby) thresholds.

8.3.5 Power Good Monitor (PGOOD)

The LM25145 provides a PGOOD flag pin to indicate when the output voltage is within a regulation window. Use the PGOOD signal as shown in Figure 34 for start-up sequencing of downstream converters, fault protection, and output monitoring. PGOOD is an open-drain output that requires a pullup resistor to a DC supply not greater than 13 V. The typical range of pullup resistance is 10 kΩ to 100 kΩ. If necessary, use a resistor divider to decrease the voltage from a higher voltage pullup rail.

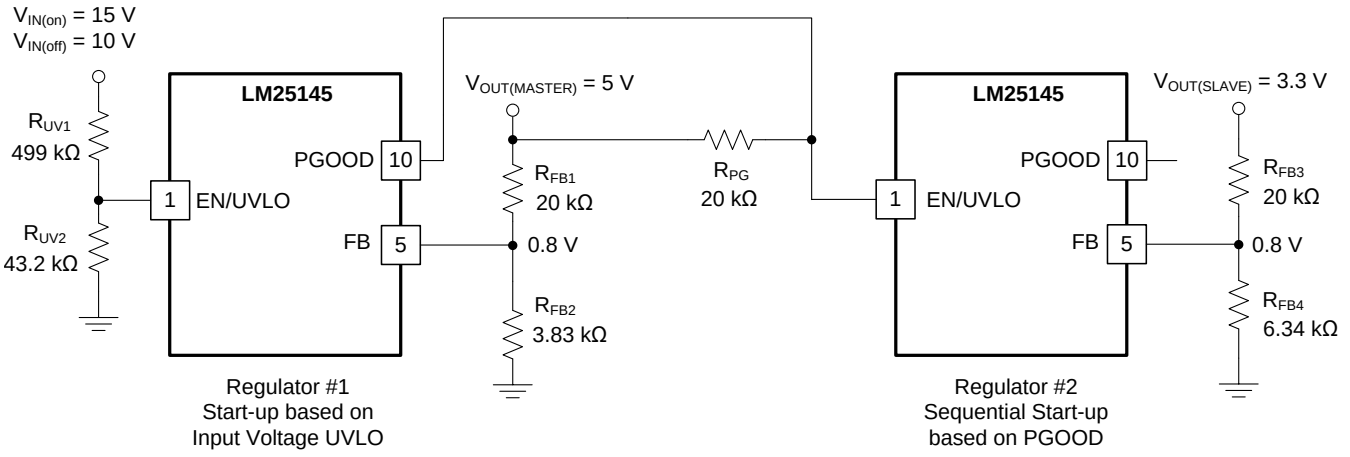

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Figure 34. Master-Slave Sequencing Implementation Using PGOOD and EN/UVLO

When the FB voltage exceeds 94% of the internal reference V_{REF}, the internal PGOOD switch turns off and PGOOD can be pulled high by the external pullup. If the FB voltage falls below 92% of V_{REF}, the internal PGOOD switch turns on, and PGOOD is pulled low to indicate that the output voltage is out of regulation. Similarly, when the FB voltage exceeds 108% of V_{REF}, the internal PGOOD switch turns on, pulling PGOOD low. If the FB voltage subsequently falls below 105% of V_{REF}, the PGOOD switch is turned off and PGOOD is pulled high. PGOOD has a built-in deglitch delay of 25 µs.

Feature Description (continued)

8.3.6 Switching Frequency (RT, SYNCIN)

There are two options for setting the switching frequency, F_{SW}, of the LM25145, thus providing a power supply designer with a level of flexibility when choosing external components for various applications. To adjust the frequency, use a resistor from the RT pin to AGND, or synchronize the LM25145 to an external clock signal through the SYNCIN pin.

8.3.6.1 Frequency Adjust

Adjust the LM25145 free-running switching frequency by using a resistor from the RT pin to AGND. The switching frequency range is from 100 kHz to 1 MHz. The frequency set resistance, R_{RT}, is governed by Equation 3. E96 standard-value resistors for common switching frequencies are given in Table 1.

$$R_{RT}\left[k\Omega\right] = \frac{10^4}{F_{SW}\left[kHz\right]} \quad (3)$$

Table 1. Frequency Set Resistors

SWITCHING FREQUENCY (kHz)	FREQUENCY SET RESISTANCE (kΩ)
100	100
200	49.9
250	40.2
300	33.2
400	24.9
500	20
750	13.3
1000	10

8.3.6.2 Clock Synchronization

Apply an external clock synchronization signal to the LM25145 to synchronize switching in both frequency and phase. Requirements for the external clock SYNC signal are:

- Clock frequency range: 100 kHz to 1 MHz
- Clock frequency: –20% to +50% of the free-running frequency set by R_{RT}
- Clock maximum voltage amplitude: 13 V
- Clock minimum pulse width: 50 ns

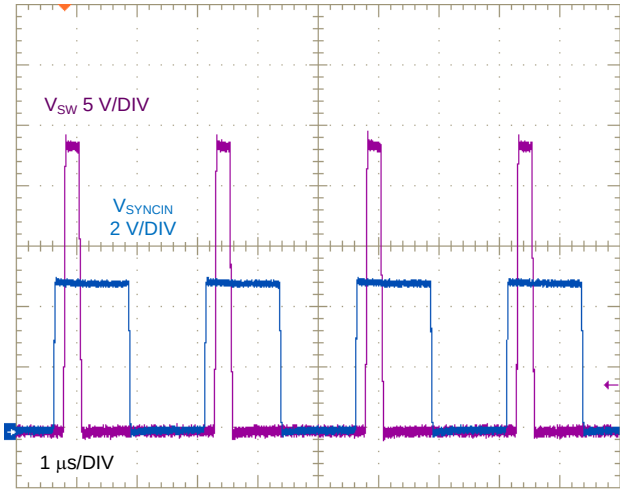

Figure 35. Typical 400-kHz SYNCIN and SW Voltage Waveforms

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Figure 35 shows a clock signal at 400 kHz and the corresponding SW node waveform (V_{IN} = 24 V, V_{OUT} = 5 V, free-running frequency = 280 kHz). The SW voltage waveform is synchronized with respect to the rising edge of SYNCIN. The rising edge of the SW voltage is phase delayed relative to SYNCIN by approximately 100 ns.

8.3.7 Configurable Soft-Start (SS/TRK)

After the EN/UVLO pin exceeds its rising threshold of 1.2 V, the LM25145 begins charging the output to the DC level dictated by the feedback resistor network. The LM25145 features an adjustable soft-start (set by a capacitor from the SS/TRK pin to GND) that determines the charging time of the output. A 10-µA current source charges this soft-start capacitor. Soft-start limits inrush current as a result of high output capacitance to avoid an overcurrent condition. Stress on the input supply rail is also reduced. The soft-start time, t_{SS}, for the output voltage to ramp to its nominal level is set by Equation 4.

$$t_{SS} = \frac{C_{SS} \cdot V_{REF}}{I_{SS}} \quad (4)$$

where

- C_{SS} is the soft-start capacitance
- V_{REF} is the 0.8-V reference
- I_{SS} is the 10-µA current sourced from the SS/TRK pin.

More simply, calculate C_{SS} using Equation 5.

$$C_{SS}\left[nF\right] = 12.5 \cdot t_{SS}\left[ms\right] \quad (5)$$

The SS/TRK pin is internally clamped to V_{FB} + 115 mV to allow a soft-start recovery from an overload event. The clamp circuit requires a soft-start capacitance greater than 2 nF for stability and has a current limit of approximately 2 mA.

8.3.7.1 Tracking

The SS/TRK pin also doubles as a tracking pin when master-slave power-supply tracking is required. This tracking is achieved by simply dividing down the output voltage of the master with a simple resistor network. Coincident, ratiometric, and offset tracking modes are possible.

If an external voltage source is connected to the SS/TRK pin, the external soft-start capability of the LM25145 is effectively disabled. The regulated output voltage level is reached when the SS/TRACK pin reaches the 0.8-V reference voltage level. It is the responsibility of the system designer to determine if an external soft-start capacitor is required to keep the device from entering current limit during a start-up event. Likewise, the system designer must also be aware of how fast the input supply ramps if the tracking feature is enabled.

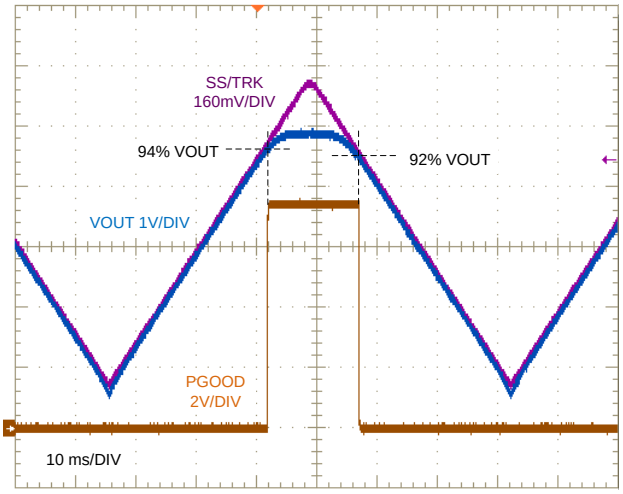

Figure 36. Typical Output Voltage Tracking and PGOOD Waveforms

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Figure 36 shows a triangular voltage signal directly driving SS/TRK and the corresponding output voltage tracking response. Nominal output voltage here is 5 V, with oscilloscope channel scaling chosen such that the waveforms overlap during tracking. As expected, the PGOOD flag transitions at thresholds of 94% (rising) and 92% (falling) of the nominal output voltage setpoint.

Two practical tracking configurations, ratiometric and coincident, are shown in Figure 37. The most common application is coincident tracking, used in core versus I/O voltage tracking in DSP and FPGA implementations. Coincident tracking forces the master and slave channels to have the same output voltage ramp rate until the slave output reaches its regulated setpoint. Conversely, ratiometric tracking sets the output voltage of the slave to a fraction of the output voltage of the master during start-up.

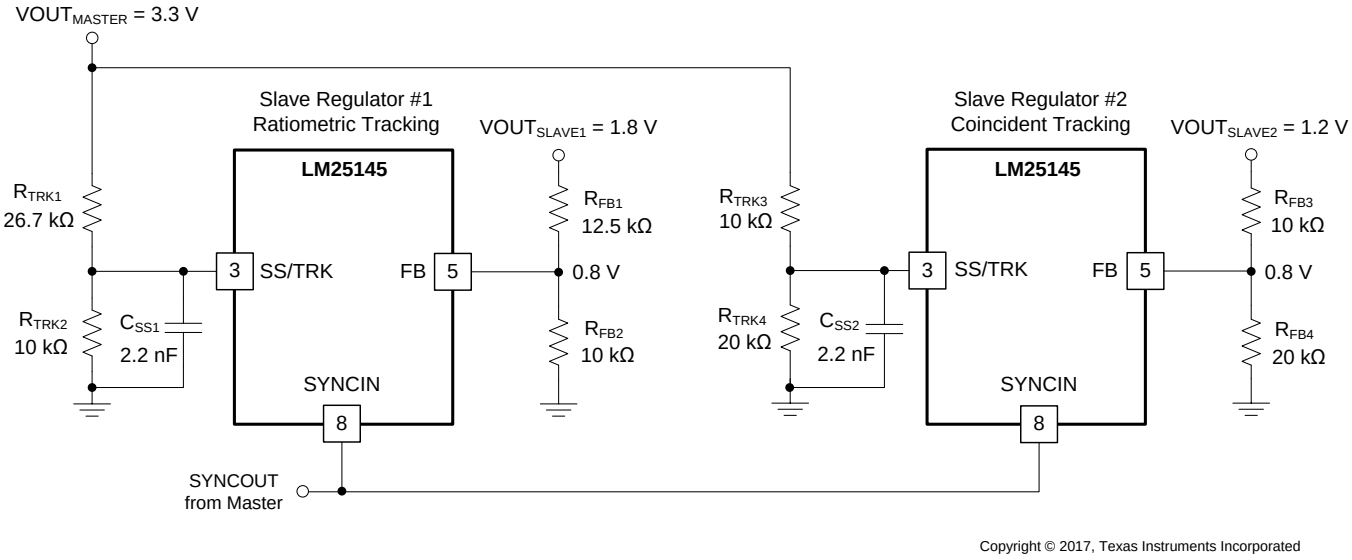

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Figure 37. Tracking Implementation With Master, Ratiometric Slave, and Coincident Slave Rails

For coincident tracking, connect the SS/TRK input of the slave regulator to a resistor divider from the output voltage of the master that is the same as the divider used on the FB pin of the slave. In other words, simply select $R_{TRK3} = R_{FB3}$ and $R_{TRK4} = R_{FB4}$ as shown in . As the master voltage rises, the slave voltage rises identically (aside from the 80-mV offset from SS/TRK to FB when V_{FB} is below 0.8 V). Eventually, the slave voltage reaches its regulation voltage, at which point the internal reference takes over the regulation while the SS/TRK input continues to 115 mV above FB, and no longer controls the output voltage.

In all cases, to ensure that the output voltage accuracy is not compromised by the SS/TRK voltage being too close to the 0.8-V reference voltage, the final value of the SS/TRK voltage of the slave should be at least 100 mV above FB.

8.3.8 Voltage-Mode Control (COMP)

The LM25145 incorporates a voltage-mode control loop implementation with input voltage feedforward to eliminate the input voltage dependence of the PWM modulator gain. This configuration allows the controller to maintain stability throughout the entire input voltage operating range and provides for optimal response to input voltage transient disturbances. The constant gain provided by the controller greatly simplifies loop compensation design because the loop characteristics remain constant as the input voltage changes, unlike a buck converter without voltage feedforward. An increase in input voltage is matched by a concomitant increase in ramp voltage amplitude to maintain constant modulator gain. The input voltage feedforward gain, k_{FF}, is 15, equivalent to the input voltage divided by the ramp amplitude, V_{IN}/V_{RAMP}. See *Control Loop Compensation* for more detail.

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8.3.9 Gate Drivers (LO, HO)

The LM25145 gate driver impedances are low enough to perform effectively in high output current applications where large die-size or paralleled MOSFETs with correspondingly large gate charge, Q_G, are used. Measured at V_{VCC} = 7.5 V, the low-side driver of the LM25145 has a low impedance pulldown path of 0.9 Ω to minimize the effect of dv/dt induced turnon, particularly with low gate-threshold voltage MOSFETs. Similarly, the high-side driver has 1.5-Ω and 0.9-Ω pullup and pulldown impedances, respectively, for faster switching transition times, lower switching loss, and greater efficiency.

The high-side gate driver works in conjunction with an integrated bootstrap diode and external bootstrap capacitor, C_{BST}. When the low-side MOSFET conducts, the SW voltage is approximately at 0 V and C_{BST} is charged from VCC through the integrated boot diode. Connect a 0.1-µF or larger ceramic capacitor close to the BST and SW pins.

Furthermore, there is a proprietary adaptive dead-time control on both switching edges to prevent shoot-through and cross-conduction, minimize body diode conduction time, and reduce body diode reverse recovery losses.

8.3.10 Current Sensing and Overcurrent Protection (ILIM)

The LM25145 implements a lossless current sense scheme designed to limit the inductor current during an overload or short-circuit condition. Figure 38 portrays the popular current sense method using the on-state resistance of the low-side MOSFET. Meanwhile, Figure 39 shows an alternative implementation with current shunt resistor, R_S. The LM25145 senses the inductor current during the PWM off-time (when LO is high).

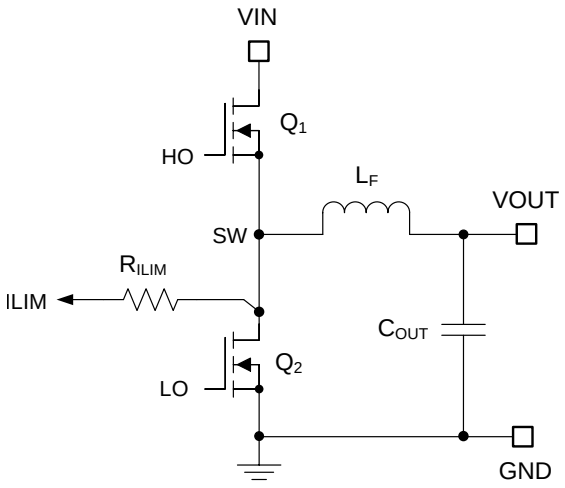

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Figure 38. MOSFET $R_{DS(on)}$ Current Sensing

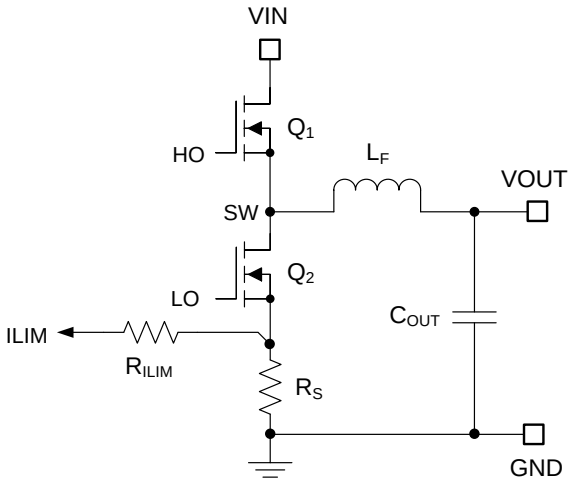

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Figure 39. Shunt Resistor Current Sensing

The ILIM pin of the LM25145 sources a reference current that flows in an external resistor, designated R_{ILIM}, to program of the current limit threshold. A current limit comparator on the ILIM pin prevents further SW pulses if the ILIM pin voltage goes below GND. Figure 40 shows the implementation.

Resistor R_{ILIM} is tied to SW to use the $R_{DS(on)}$ of the low-side MOSFET as a sensing element (termed R_{DS-ON} mode). Alternatively, R_{ILIM} is tied to a shunt resistor connected at the source of the low-side MOSFET (termed R_{SENSE} mode). The LM25145 detects the appropriate mode at start-up and sets the source current amplitude and temperature coefficient (TC) accordingly.

The ILIM current with R_{DS-ON} sensing is 200 µA at 27°C junction temperature and incorporates a TC of +4500 ppm/°C to generally track the $R_{DS(on)}$ temperature variation of the low-side MOSFET. Conversely, the ILIM current is a constant 100 µA in R_{SENSE} mode. This controls the valley of the inductor current during a steady-state overload at the output. Depending on the chosen mode, select the resistance of R_{ILIM} using Equation 6.

$$R_{ILIM} = \begin{cases} \dfrac{I_{OUT} - \Delta I_L/2}{I_{RDSON}} \cdot R_{DS(on)Q2}, & R_{DS(on)} \text{ sensing} \\ \dfrac{I_{OUT} - \Delta I_L/2}{I_{RS}} \cdot R_S, & \text{shunt sensing} \end{cases}$$

where

- ΔI_L is the peak-to-peak inductor ripple current
- $R_{DS(on)Q2}$ is the on-state resistance of the low-side MOSFET
- I_{RDSON} is the ILIM pin current in R_{DS-ON} mode
- R_S is the resistance of the current-sensing shunt element, and
- I_{RS} is the ILIM pin current in R_{SENSE} mode. (6)

Given the large voltage swings of ILIM in R_{DS-ON} mode, a capacitor designated C_{ILIM} connected from ILIM to PGND is essential to the operation of the valley current limit circuit. Choose this capacitance such that the time constant $R_{ILIM} \cdot C_{ILIM}$ is approximately 6 ns.

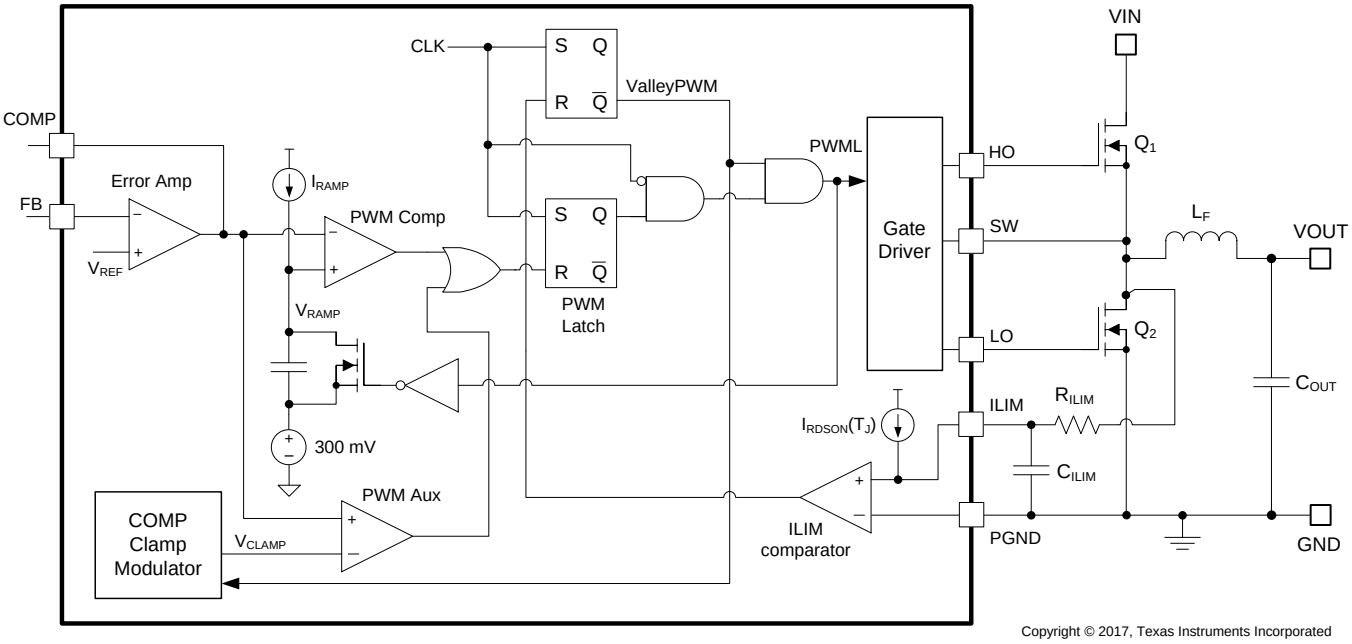

Figure 40. OCP Setpoint Defined by Current Source I_{RDSON} and Resistor R_{ILIM} in R_{DS-ON} Mode

Note that current sensing with a shunt component is typically implemented at lower output current levels to provide accurate overcurrent protection. Burdened by the unavoidable efficiency penalty, PCB layout, and additional cost implications, this configuration is not usually implemented in high-current applications (except where OCP setpoint accuracy and stability over the operating temperature range are critical specifications).

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8.3.11 OCP Duty Cycle Limiter

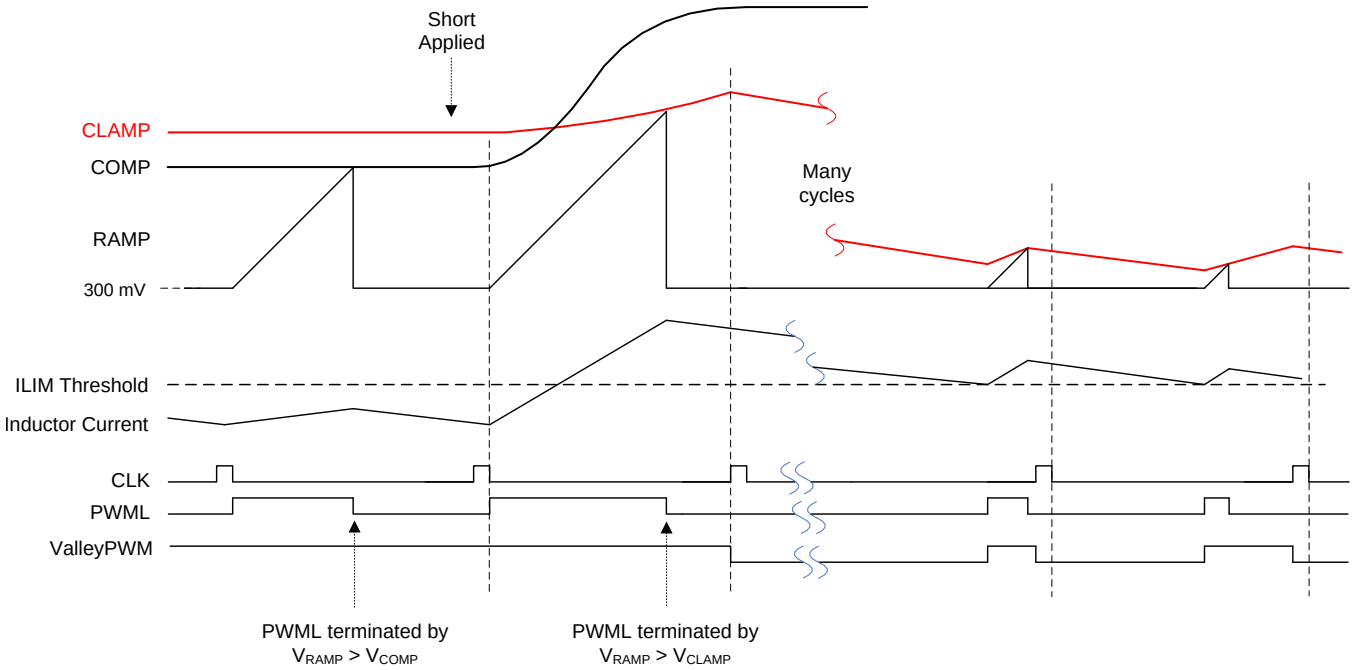

Figure 41. OCP Duty Cycle Limiting Waveforms

In addition to valley current limiting, the LM25145 uses a proprietary duty-cycle limiter circuit to reduce the PWM on-time during an overcurrent condition. As shown in Figure 40, an auxiliary PWM comparator along with a modulated CLAMP voltage limits how quickly the on-time increases in response to a large step in the COMP voltage that typically occurs with a voltage-mode control loop architecture.

As depicted in Figure 41, the CLAMP voltage, V_{CLAMP}, is normally regulated above the COMP voltage to provide adequate headroom during a response to a load-on transient. If the COMP voltage rises quickly during an overloaded or shorted output condition, the on-time pulse terminates thereby limiting the on-time and peak inductor current. Moreover, the CLAMP voltage is reduced if additional valley current limit events occur, further reducing the average output current.

If the overcurrent condition exists for 128 continuous clock cycles, a hiccup event is triggered and SS is pulled low for 8192 clock cycles before a soft-start sequence is initiated.

8.4 Device Functional Modes

8.4.1 Shutdown Mode

The EN/UVLO pin provides ON / OFF control for the LM25145. When the EN/UVLO voltage is below 0.37 V (typical), the device is in shutdown mode. Both the internal bias supply LDO and the switching regulator are off. The quiescent current in shutdown mode drops to 13.5 μA (typical) at V_{IN} = 24 V. The LM25145 also includes undervoltage protection of the internal bias LDO. If the internal bias supply voltage is below its UVLO threshold level, the switching regulator remains off.

8.4.2 Standby Mode

The internal bias supply LDO has a lower enable threshold than the switching regulator. When the EN/UVLO voltage exceeds 0.42 V (typical) and is below the precision enable threshold (1.2 V typically), the internal LDO is on and regulating. Switching action and output voltage regulation are disabled in standby mode.

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Device Functional Modes (continued)

8.4.3 Active Mode

The LM25145 is in active mode when the VCC voltage is above its rising UVLO threshold of 5 V and the EN/UVLO voltage is above the precision EN threshold of 1.2 V. The simplest way to enable the LM25145 is to tie EN/UVLO to VIN. This allows self start-up of the LM25145 when the input voltage exceeds the VCC threshold plus the LDO dropout voltage from VIN to VCC.

8.4.4 Diode Emulation Mode

The LM25145 provides a diode emulation feature that can be enabled to prevent reverse (drain-to-source) current flow in the low-side MOSFET. When configured for diode emulation, the low-side MOSFET is switched off when reverse current flow is detected by sensing of the SW voltage using a zero-cross comparator. The benefit of this configuration is lower power loss at no-load and light-load conditions, the disadvantage being slower light-load transient response.

The diode emulation feature is configured with the SYNCIN pin. To enable diode emulation and thus achieve discontinuous conduction mode (DCM) operation at light loads, connect the SYNCIN pin to AGND or leave SYNCIN floating. If forced PWM (FPWM) continuous conduction mode (CCM) operation is desired, tie SYNCIN to VCC either directly or using a pullup resistor. Note that diode emulation mode is automatically engaged to prevent reverse current flow during a prebias start-up. A gradual change from DCM to CCM operation provides monotonic start-up performance.

8.4.5 Thermal Shutdown

The LM25145 includes an internal junction temperature monitor. If the temperature exceeds 175°C (typical), thermal shutdown occurs.

When entering thermal shutdown, the device:

1. Turns off the low-side and high-side MOSFETs;
2. Pulls SS/TRK and PGOOD low;
3. Initiates a soft-start sequence when the die temperature decreases by the thermal shutdown hysteresis of 20°C (typical).

This is a non-latching protection, and, as such, the device will cycle into and out of thermal shutdown if the fault persists.

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Design and Implementation

To expedite the process of designing of a LM25145-based regulator for a given application, please use the LM25145 Quickstart Calculator available as a free download, as well as numerous LM25145 reference designs populated in TI Designs™ reference design library, or the designs provided in *Typical Applications*. The LM25145 is also WEBENCH® Designer enabled.

9.1.2 Power Train Components

Comprehensive knowledge and understanding of the power train components are key to successfully completing a synchronous buck regulator design.

9.1.2.1 Inductor

For most applications, choose an inductance such that the inductor ripple current, ΔI_L, is between 30% and 40% of the maximum DC output current at nominal input voltage. Choose the inductance using Equation 7 based on a peak inductor current given by Equation 8.

$$L_F = \frac{V_{OUT}}{V_{IN}} \cdot \left(\frac{V_{IN} - V_{OUT}}{\Delta I_L \cdot F_{SW}} \right) \tag{7}$$

$$I_{L(peak)} = I_{OUT} + \frac{\Delta I_L}{2} \tag{8}$$

Check the inductor datasheet to ensure that the saturation current of the inductor is well above the peak inductor current of a particular design. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can then concentrate on copper loss and preventing saturation. Low inductor core loss is evidenced by reduced no-load input current and higher light-load efficiency. However, ferrite core materials exhibit a hard saturation characteristic and the inductance collapses abruptly when the saturation current is exceeded. This results in an abrupt increase in inductor ripple current, higher output voltage ripple, not to mention reduced efficiency and compromised reliability. Note that the saturation current of an inductor generally deceases as its core temperature increases. Of course, accurate overcurrent protection is key to avoiding inductor saturation.

9.1.2.2 Output Capacitors

Ordinarily, the output capacitor energy store of the regulator combined with the control loop response are prescribed to maintain the integrity of the output voltage within the dynamic (transient) tolerance specifications. The usual boundaries restricting the output capacitor in power management applications are driven by finite available PCB area, component footprint and profile, and cost. The capacitor parasitics—equivalent series resistance (ESR) and equivalent series inductance (ESL)—take greater precedence in shaping the load transient response of the regulator as the load step amplitude and slew rate increase.

The output capacitor, C_{OUT}, filters the inductor ripple current and provides a reservoir of charge for step-load transient events. Typically, ceramic capacitors provide extremely low ESR to reduce the output voltage ripple and noise spikes, while tantalum and electrolytic capacitors provide a large bulk capacitance in a relatively compact footprint for transient loading events.

Based on the static specification of peak-to-peak output voltage ripple denoted by ΔV_{OUT}, choose an output capacitance that is larger than that given by Equation 9.

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Application Information (continued)

$$C_{OUT} \geq \frac{\Delta I_L}{8 \cdot F_{SW} \sqrt{\Delta V_{OUT}^2 - \left(R_{ESR} \cdot \Delta I_L\right)^2}} \quad (9)$$

Figure 42 conceptually illustrates the relevant current waveforms during both load step-up and step-down transitions. As shown, the large-signal slew rate of the inductor current is limited as the inductor current ramps to match the new load-current level following a load transient. This slew-rate limiting exacerbates the deficit of charge in the output capacitor, which must be replenished as rapidly as possible during and after the load step-up transient. Similarly, during and after a load step-down transient, the slew rate limiting of the inductor current adds to the surplus of charge in the output capacitor that must be depleted as quickly as possible.

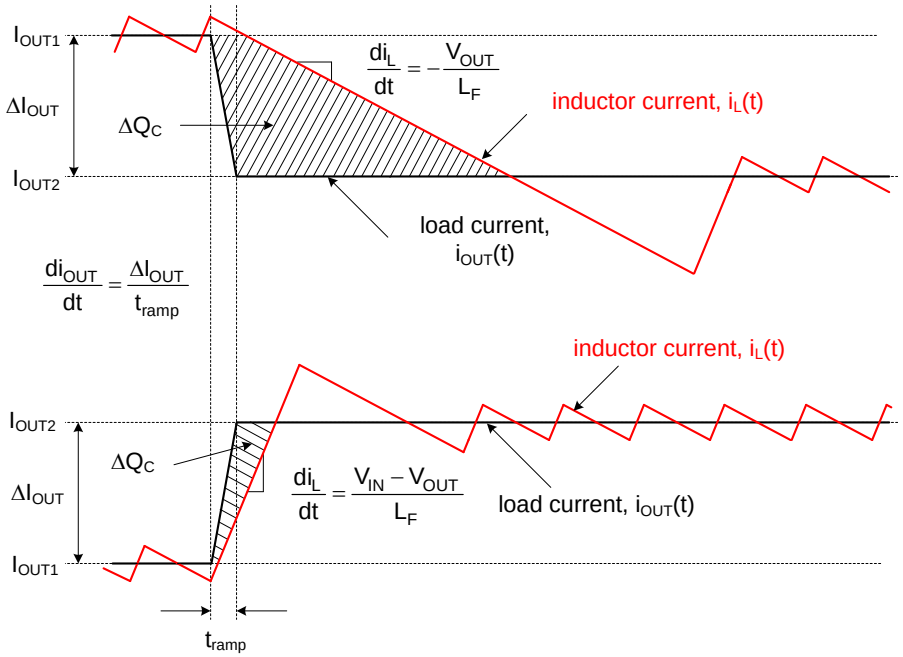

Figure 42. Load Transient Response Representation Showing C_{OUT} Charge Surplus or Deficit

In a typical regulator application of 24-V input to low output voltage (for example, 5 V), it should be recognized that the load-off transient represents worst-case. In that case, the steady-state duty cycle is approximately 10% and the large-signal inductor current slew rate when the duty cycle collapses to zero is approximately $-V_{OUT}/L$. Compared to a load-on transient, the inductor current takes much longer to transition to the required level. The surplus of charge in the output capacitor causes the output voltage to significantly overshoot. In fact, to deplete this excess charge from the output capacitor as quickly as possible, the inductor current must ramp below its nominal level following the load step. In this scenario, a large output capacitance can be advantageously employed to absorb the excess charge and limit the voltage overshoot.

To meet the dynamic specification of output voltage overshoot during such a load-off transient (denoted as $\Delta V_{OVERSHOOT}$ with step reduction in output current given by ΔI_{OUT}), the output capacitance should be larger than

$$C_{OUT} \geq \frac{L_F \cdot \Delta I_{OUT}^2}{\left(V_{OUT} + \Delta V_{OVERSHOOT}\right)^2 - V_{OUT}^2} \quad (10)$$

The ESR of a capacitor is provided in the manufacturer's data sheet either explicitly as a specification or implicitly in the impedance vs. frequency curve. Depending on type, size and construction, electrolytic capacitors have significant ESR, 5 mΩ and above, and relatively large ESL, 5 nH to 20 nH. PCB traces contribute some parasitic resistance and inductance as well. Ceramic output capacitors, on the other hand, have low ESR and ESL contributions at the switching frequency, and the capacitive impedance component dominates. However, depending on package and voltage rating of the ceramic capacitor, the effective capacitance can drop quite significantly with applied DC voltage and operating temperature.

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Application Information (continued)

Ignoring the ESR term in Equation 9 gives a quick estimation of the minimum ceramic capacitance necessary to meet the output ripple specification. One to four 47-µF, 10-V, X7R capacitors in 1206 or 1210 footprint is a common choice. Use Equation 10 to determine if additional capacitance is necessary to meet the load-off transient overshoot specification.

A composite implementation of ceramic and electrolytic capacitors highlights the rationale for paralleling capacitors of dissimilar chemistries yet complementary performance. The frequency response of each capacitor is accretive in that each capacitor provides desirable performance over a certain portion of the frequency range. While the ceramic provides excellent mid- and high-frequency decoupling characteristics with its low ESR and ESL to minimize the switching frequency output ripple, the electrolytic device with its large bulk capacitance provides low-frequency energy storage to cope with load transient demands.

9.1.2.3 Input Capacitors

Input capacitors are necessary to limit the input ripple voltage to the buck power stage due to switching-frequency AC currents. TI recommends using X5R or X7R dielectric ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. To minimize the parasitic inductance in the switching loop, position the input capacitors as close as possible to the drain of the high-side MOSFET and the source of the low-side MOSFET. The input capacitor RMS current is given by Equation 11.

$$I_{CIN,rms} = \sqrt{D \cdot \left({I_{OUT}}^2 \cdot (1-D) + \frac{\Delta I_L^2}{12} \right)} \tag{11}$$

The highest input capacitor RMS current occurs at D = 0.5, at which point the RMS current rating of the capacitors should be greater than half the output current.

Ideally, the DC component of input current is provided by the input voltage source and the AC component by the input filter capacitors. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} − I_{IN}) during the D interval and sinks I_{IN} during the 1−D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. It follows that the resultant capacitive component of AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, the peak-to-peak ripple voltage amplitude is given by Equation 12.

$$\Delta V_{IN} = \frac{I_{OUT} \cdot D \cdot (1-D)}{F_{SW} \cdot C_{IN}} + I_{OUT} \cdot R_{ESR} \tag{12}$$

The input capacitance required for a particular load current, based on an input voltage ripple specification of ΔV_{IN}, is given by Equation 13.

$$C_{IN} \geq \frac{D \cdot (1-D) \cdot I_{OUT}}{F_{SW} \cdot (\Delta V_{IN} - R_{ESR} \cdot I_{OUT})} \tag{13}$$

Low-ESR ceramic capacitors can be placed in parallel with higher valued bulk capacitance to provide optimized input filtering for the regulator and damping to mitigate the effects of input parasitic inductance resonating with high-Q ceramics. One bulk capacitor of sufficiently high current rating and two or three 2.2-µF 100-V X7R ceramic decoupling capacitors are usually sufficient. Select the input bulk capacitor based on its ripple current rating and operating temperature.

9.1.2.4 Power MOSFETs

The choice of power MOSFETs has significant impact on DC-DC regulator performance. A MOSFET with low on-state resistance, $R_{DS(on)}$, reduces conduction loss, whereas low parasitic capacitances enable faster transition times and reduced switching loss. Normally, the lower the $R_{DS(on)}$ of a MOSFET, the higher the gate charge and output charge (Q_G and Q_{OSS} respectively), and vice versa. As a result, the product $R_{DS(on)}$ × Q_G is commonly specified as a MOSFET figure-of-merit. Low thermal resistance ensures that the MOSFET power dissipation does not result in excessive MOSFET die temperature.

The main parameters affecting power MOSFET selection in an LM25145 application are as follows:

- $R_{DS(on)}$ at V_{GS} = 7.5 V;
- Drain-source voltage rating, BV_{DSS}, typically 30 V, 40 V or 60 V, depending on maximum input voltage;

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Application Information (continued)

- Gate charge parameters at V_{GS} = 7.5 V;
- Output charge, Q_{OSS}, at the relevant input voltage;
- Body diode reverse recovery charge, Q_{RR};
- Gate threshold voltage, $V_{GS(th)}$, derived from the plateau in the Q_G vs. V_{GS} plot in the MOSFET data sheet. With a MOSFET Miller plateau voltage typically in the range of 3 V to 5 V, the 7.5-V gate drive amplitude of the LM25145 provides an adequately-enhanced MOSFET when on and a margin against Cdv/dt shoot-through when off.

The MOSFET-related power losses are summarized by the equations presented in Table 2, where suffixes 1 and 2 represent high-side and low-side MOSFET parameters, respectively. While the influence of inductor ripple current is considered, second-order loss modes, such as those related to parasitic inductances and SW node ringing, are not included. Consult the LM25145 Quickstart Calculator to assist with power loss calculations.

Table 2. Buck Regulator MOSFET Power Losses

POWER LOSS MODE	HIGH-SIDE MOSFET	LOW-SIDE MOSFET
MOSFET Conduction(1)(2)	$P_{cond1} = D \cdot \left({I_{OUT}}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)1}$	$P_{cond2} = D' \cdot \left({I_{OUT}}^2 + \frac{\Delta I_L^2}{12} \right) \cdot R_{DS(on)2}$
MOSFET Switching	$P_{sw1} = V_{IN} \cdot F_{SW} \left[\left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_R + \left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_F \right]$	Negligible
MOSFET Gate Drive(3)	$P_{Gate1} = V_{CC} \cdot F_{SW} \cdot Q_{G1}$	$P_{Gate2} = V_{CC} \cdot F_{SW} \cdot Q_{G2}$
MOSFET Output Charge(4)	$P_{Coss} = F_{SW} \cdot \left(V_{IN} \cdot Q_{oss2} + E_{oss1} - E_{oss2} \right)$	
Body Diode Conduction	N/A	$P_{cond_{BD}} = V_F \cdot F_{SW} \left[\left(I_{OUT} + \frac{\Delta I_L}{2} \right) \cdot t_{dt1} + \left(I_{OUT} - \frac{\Delta I_L}{2} \right) \cdot t_{dt2} \right]$
Body Diode Reverse Recovery(5)	$P_{RR} = V_{IN} \cdot F_{SW} \cdot Q_{RR2}$	

(1) MOSFET $R_{DS(on)}$ has a positive temperature coefficient of approximately 4500 ppm/°C. The MOSFET junction temperature, T_J, and its rise over ambient temperature is dependent upon the device total power dissipation and its thermal impedance.
(2) D' = 1–D is the duty cycle complement.
(3) Gate drive loss is apportioned based on the internal gate resistance of the MOSFET, externally-added series gate resistance and the relevant driver resistance of the LM25145.
(4) MOSFET output capacitances, C_{oss1} and C_{oss2}, are highly non-linear with voltage. These capacitances are charged losslessly by the inductor current at high-side MOSFET turn-off. During turn-on, however, a current flows from the input to charge the output capacitance of the low-side MOSFET. E_{oss1}, the energy of C_{oss1}, is dissipated at turn-on, but this is offset by the stored energy E_{oss2} on C_{oss2}.
(5) MOSFET body diode reverse recovery charge, Q_{RR}, depends on many parameters, particularly forward current, current transition speed and temperature.

The high-side (control) MOSFET carries the inductor current during the PWM on-time (or D interval) and typically incurs most of the switching losses. It is therefore imperative to choose a high-side MOSFET that balances conduction and switching loss contributions. The total power dissipation in the high-side MOSFET is the sum of the losses due to conduction, switching (voltage-current overlap), output charge, and typically two-thirds of the net loss attributed to body diode reverse recovery.

The low-side (synchronous) MOSFET carries the inductor current when the high-side MOSFET is off (or 1–D interval). The low-side MOSFET switching loss is negligible as it is switched at zero voltage – current just commutates from the channel to the body diode or vice versa during the transition dead-times. The LM25145, with its adaptive gate drive timing, minimizes body diode conduction losses when both MOSFETs are off. Such losses scale directly with switching frequency.

In high step-down ratio applications, the low-side MOSFET carries the current for a large portion of the switching period. Therefore, to attain high efficiency, it is critical to optimize the low-side MOSFET for low $R_{DS(on)}$. In cases where the conduction loss is too high or the target $R_{DS(on)}$ is lower than available in a single MOSFET, connect two low-side MOSFETs in parallel. The total power dissipation of the low-side MOSFET is the sum of the losses due to channel conduction, body diode conduction, and typically one-third of the net loss attributed to body diode reverse recovery. The LM25145 is well suited to drive TI's comprehensive portfolio of NexFET™ power MOSFETs.

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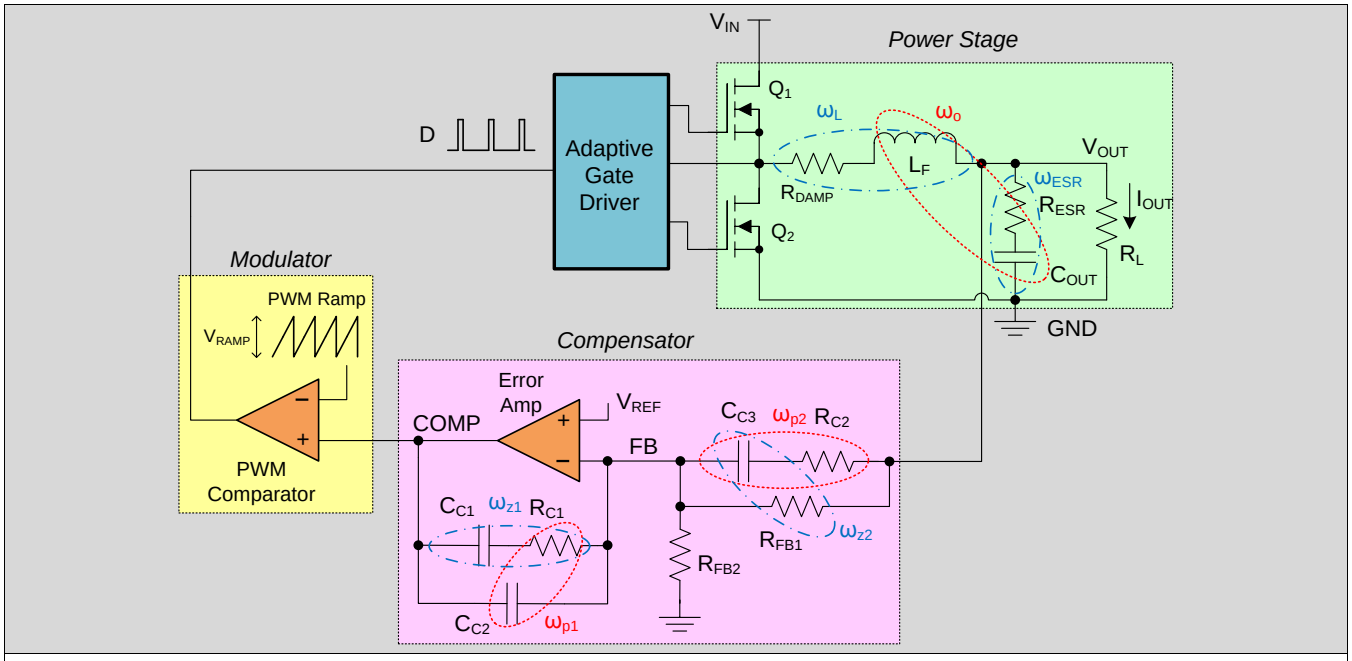
9.1.3 Control Loop Compensation

The poles and zeros inherent to the power stage and compensator are respectively illustrated by red and blue dashed rings in the schematic embedded in Table 3.

The compensation network typically employed with voltage-mode control is a Type-III circuit with three poles and two zeros. One compensator pole is located at the origin to realize high DC gain. The normal compensation strategy uses two compensator zeros to counteract the LC double pole, one compensator pole located to nullify the output capacitor ESR zero, with the remaining compensator pole located at one-half switching frequency to attenuate high frequency noise. The resistor divider network to FB determines the desired output voltage. Note that the lower feedback resistor, R_{FB2}, has no impact on the control loop from an AC standpoint because the FB node is the input to an error amplifier and is effectively at AC ground. Hence, the control loop is designed irrespective of output voltage level. The proviso here is the necessary output capacitance derating with bias voltage and temperature.

Table 3. Buck Regulator Poles and Zeros(1)(2)



POWER STAGE POLES	POWER STAGE ZEROS	COMPENSATOR POLES	COMPENSATOR ZEROS
$\omega_0 = \frac{1}{\sqrt{L_F \cdot C_{OUT}\left(\frac{1+R_{ESR}/R_L}{1+R_{ESR}/R_{DAMP}}\right)}} \cong \frac{1}{\sqrt{L_F \cdot C_{OUT}}}$	$\omega_{ESR} = \frac{1}{R_{ESR} \cdot C_{OUT}}$	$\omega_{p1} = \frac{1}{R_{C2} \cdot C_{C3}}$	$\omega_{z1} = \frac{1}{R_{C1} \cdot C_{C1}}$
	$\omega_L = \frac{L_F}{R_{DAMP}}$	$\omega_{p2} = \frac{1}{R_{C1} \cdot (C_{C1} \parallel C_{C2})} \cong \frac{1}{R_{C1} \cdot C_{C2}}$	$\omega_{z2} = \frac{1}{(R_{FB2} + R_{C2}) \cdot C_{C3}}$

(1) R_{ESR} represents the ESR of the output capacitor C_{OUT}.
(2) $R_{DAMP} = D \cdot R_{DS(on)high\text{-}side} + (1–D) \cdot R_{DS(on)\ low\text{-}side} + R_{DCR}$, shown as a lumped element in the schematic, represents the effective series damping resistance.

The small-signal open-loop response of a buck regulator is the product of modulator, power train and compensator transfer functions. The power stage transfer function can be represented as a complex pole pair associated with the output LC filter and a zero related to the ESR of the output capacitor. The DC (and low frequency) gain of the modulator and power stage is V_{IN}/V_{RAMP}. The gain from COMP to the average voltage at the input of the LC filter is held essentially constant by the PWM line feedforward feature of the LM25145 (15 V/V or 23.5 dB).

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Complete expressions for small-signal frequency analysis are presented in Table 4. The transfer functions are denoted in normalized form. While the loop gain is of primary importance, a regulator is not specified directly by its loop gain but by its performance related characteristics, namely closed-loop output impedance and audio susceptibility.

Table 4. Buck Regulator Small-Signal Analysis

TRANSFER FUNCTION	EXPRESSION
Open-loop transfer function	$T_v(s) = \frac{\hat{v}_{comp}(s)}{\hat{v}_o(s)} \cdot \frac{\hat{v}_o(s)}{\hat{d}(s)} \cdot \frac{\hat{d}(s)}{\hat{v}_{comp}(s)} = G_c(s) \cdot G_{vd}(s) \cdot F_M$
Duty-cycle-to-output transfer function	$G_{vd}(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)}\Big\|_{\substack{\hat{v}_{in}(s)=0 \\ \hat{i}_o(s)=0}} = V_{IN} \frac{1+\frac{s}{\omega_{ESR}}}{1+\frac{s}{Q_o\omega_o}+\frac{s^2}{\omega_o^2}}$
Compensator transfer function(1)	$G_c(s) = \frac{\hat{v}_{comp}(s)}{\hat{v}_o(s)} = K_{mid} \frac{\left(1+\frac{\omega_{z1}}{s}\right)\left(1+\frac{s}{\omega_{z2}}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)}$
Modulator transfer function	$F_M = \frac{\hat{d}(s)}{\hat{v}_{comp}(s)} = \frac{1}{V_{RAMP}}$

(1) $K_{mid} = R_{C1}/R_{FB1}$ is the mid-band gain of the compensator. By expressing one of the compensator zeros in inverted zero format, the mid-band gain is denoted explicitly.

An illustration of the open-loop response gain and phase is given in Figure 43. The poles and zeros of the system are marked with x and o symbols, respectively, and a + symbol indicates the crossover frequency. When plotted on a log (dB) scale, the open-loop gain is effectively the sum of the individual gain components from the modulator, power stage, and compensator (see Figure 44). The open-loop response of the system is measured experimentally by breaking the loop, injecting a variable-frequency oscillator signal and recording the ensuing frequency response using a network analyzer setup.

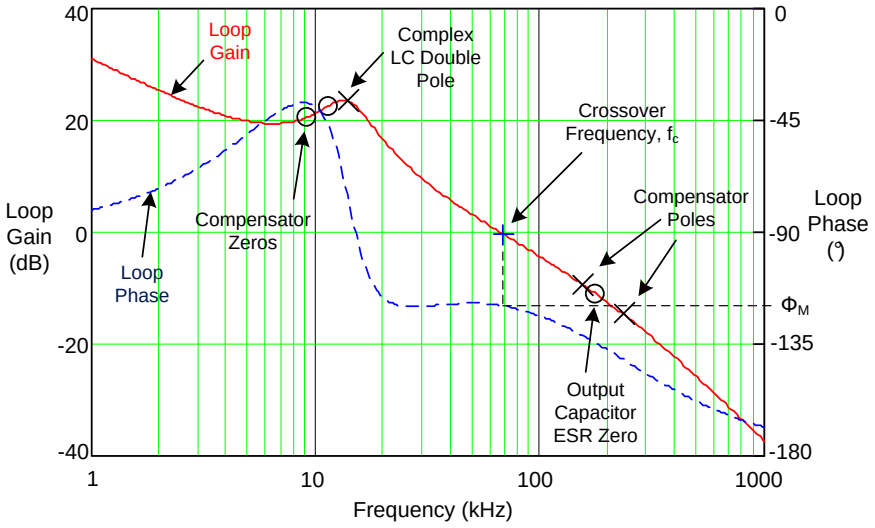

Figure 43. Typical Buck Regulator Loop Gain and Phase With Voltage-Mode Control

If the pole located at ω_{p1} cancels the zero located at ω_{ESR} and the pole at ω_{p2} is located well above crossover, the expression for the loop gain, $T_v(s)$ in Table 4, can be manipulated to yield the simplified expression given in Equation 14.

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$$T_v(s) = R_{C1} \cdot C_{C3} \cdot \frac{V_{IN}}{V_{RAMP}} \cdot \frac{\omega_o^2}{s} \quad (14)$$

Essentially, a multi-order system is reduced to a single-order approximation by judicious choice of compensator components. A simple solution for the crossover frequency, denoted as f_c in Figure 43, with Type-III voltage-mode compensation is derived as shown in Equation 15 and Equation 16.

$$\omega_c = 2\pi \cdot f_c = \omega_o \cdot K_{mid} \cdot \frac{V_{IN}}{V_{RAMP}} \quad (15)$$

$$K_{mid} = \frac{f_c}{f_o} \cdot \frac{1}{k_{FF}} = \frac{R_{C1}}{R_{FB1}} \quad (16)$$

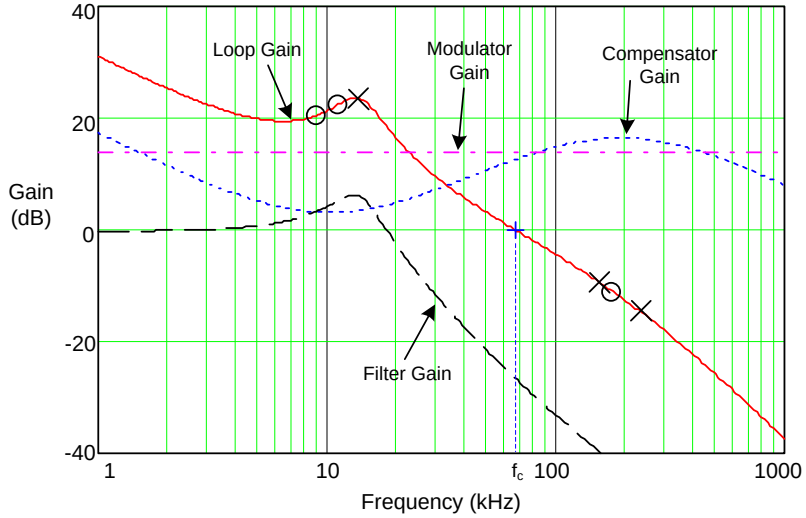

Figure 44. Buck Regulator Constituent Gain Components

The loop crossover frequency is usually selected between one-tenth to one-fifth of switching frequency. Inserting an appropriate crossover frequency into Equation 15 gives a target for the mid-band gain of the compensator, K_{mid}. Given an initial value for R_{FB1}, R_{FB2} is then selected based on the desired output voltage. Values for R_{C1}, R_{C2}, C_{C1}, C_{C2} and C_{C3} are calculated from the design expressions listed in Table 5, with the premise that the compensator poles and zeros are set as follows: $\omega_{z1} = 0.5 \cdot \omega_o$, $\omega_{z2} = \omega_o$, $\omega_{p1} = \omega_{ESR}$, $\omega_{p2} = \omega_{SW}/2$.

Table 5. Compensation Component Selection

RESISTORS	CAPACITORS
$R_{FB2} = \frac{R_{FB1}}{(V_{OUT}/V_{REF}) - 1}$	$C_{C1} = \frac{2}{\omega_{z1} \cdot R_{C1}}$
$R_{C1} = K_{mid} \cdot R_{FB1}$	$C_{C2} = \frac{1}{\omega_{p2} \cdot R_{C1}}$
$R_{C2} = \frac{1}{\omega_{p1} \cdot C_{C3}}$	$C_{C3} = \frac{1}{\omega_{z2} \cdot R_{FB1}}$

Referring to the bode plot in Figure 43, the phase margin, indicated as φ_M, is the difference between the loop phase and –180° at crossover. A target of 50° to 70° for this parameter is considered ideal. Additional phase boost is dialed in by locating the compensator zeros at a frequency lower than the LC double pole (hence why C_{C1} is scaled by a factor of 2 above). This helps mitigate the phase dip associated with the LC filter, particularly at light loads when the Q-factor is higher and the phase dip becomes especially prominent. The ramification of low phase in the frequency domain is an under-damped transient response in the time domain.

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The power supply designer now has all the necessary expressions to optimally position the loop crossover frequency while maintaining adequate phase margin over the required line, load and temperature operating ranges. The LM25145 *Quickstart Calculator* is available to expedite these calculations and to adjust the bode plot as needed.

9.1.4 EMI Filter Design

Switching regulators exhibit negative input impedance, which is lowest at the minimum input voltage. An underdamped LC filter exhibits a high output impedance at the resonant frequency of the filter. For stability, the filter output impedance must be less than the absolute value of the converter input impedance.

$$Z_{IN} = \left| -\frac{V_{IN(min)}^{2}}{P_{IN}} \right| \tag{17}$$

The EMI filter design steps are as follows:

- Calculate the required attenuation of the EMI filter at the switching frequency, where C_{IN} represents the existing capacitance at the input of the switching converter;
- Input filter inductor L_{IN} is usually selected between 1 µH and 10 µH, but it can be lower to reduce losses in a high current design;
- Calculate input filter capacitor C_F.

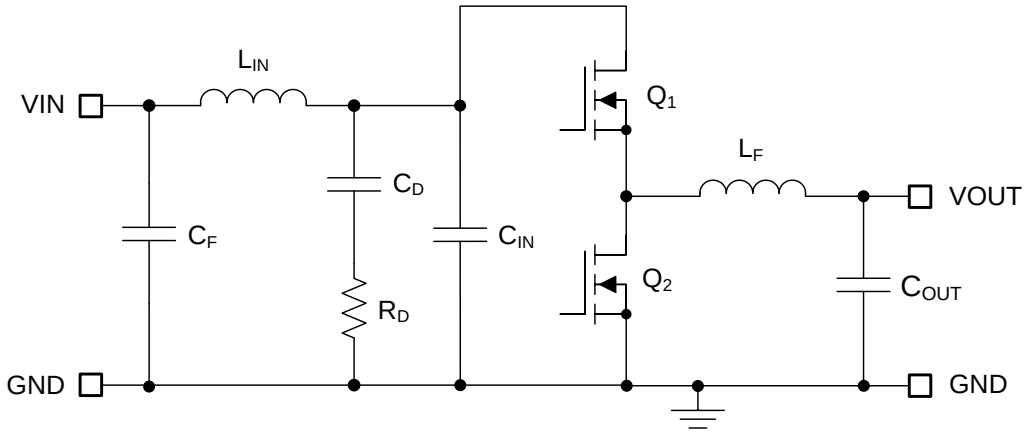

Figure 45. Buck Regulator With π-Stage EMI Filter

By calculating the first harmonic current from the Fourier series of the input current waveform and multiplying it by the input impedance (the impedance is defined by the existing input capacitor C_{IN}), a formula is derived to obtain the required attenuation as shown by Equation 18.

$$Attn = 20\log\left(\frac{I_{PEAK}}{\pi^{2} \cdot F_{SW} \cdot C_{IN}} \cdot 1\,\mu V\right) \cdot \sin\left(\pi \cdot D_{MAX}\right) - V_{MAX} \tag{18}$$

V_{MAX} is the allowed dBµV noise level for the applicable EMI standard, for example EN55022 Class B. C_{IN} is the existing input capacitance of the buck regulator, D_{MAX} is the maximum duty cycle, and I_{PEAK} is the peak inductor current. For filter design purposes, the current at the input can be modeled as a square-wave. Determine the EMI filter capacitance C_F from Equation 19.

$$C_F = \frac{1}{L_{IN}} \left(\frac{10^{\frac{|Attn|}{40}}}{2\pi \cdot F_{SW}} \right)^{2} \tag{19}$$

Adding an input filter to a switching regulator modifies the control-to-output transfer function. The output impedance of the filter must be sufficiently small such that the input filter does not significantly affect the loop gain of the buck converter. The impedance peaks at the filter resonant frequency. The resonant frequency of the filter is given by Equation 20.

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$$f_{res} = \frac{1}{2\pi \cdot \sqrt{L_{IN} \cdot C_F}} \quad (20)$$

The purpose of R_D is to reduce the peak output impedance of the filter at the resonant frequency. Capacitor C_D blocks the DC component of the input voltage to avoid excessive power dissipation in R_D. Capacitor C_D should have lower impedance than R_D at the resonant frequency with a capacitance value greater than that of the input capacitor C_{IN}. This prevents C_{IN} from interfering with the cutoff frequency of the main filter. Added damping is needed when the output impedance of the filter is high at the resonant frequency (Q of filter formed by L_{IN} and C_{IN} is too high). An electrolytic capacitor C_D can be used for damping with a value given by Equation 21.

$$C_D \geq 4 \cdot C_{IN} \quad (21)$$

Select the damping resistor R_D using Equation 22.

$$R_D = \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (22)$$

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9.2 Typical Applications

For step-by-step design procedure, circuit schematics, bill of materials, PCB files, simulation and test results of an LM25145-powered implementation, please refer to *TI Designs* reference design library.

9.2.1 Design 1 – 20-A High-Efficiency Synchronous Buck Regulator for Telecom Power Applications

Figure 46 shows the schematic diagram of a 5-V, 20-A buck regulator with a switching frequency of 500 kHz. In this example, the target full-load efficiency is 94% at a nominal input voltage of 24 V that ranges from 6.5 V to as high as 32 V. The switching frequency is set by means of a synchronization input signal at 500 kHz, and the free-running switching frequency (in the event that the synchronization signal is removed) is set at 450 kHz by resistor R_{RT}. In terms of control loop performance, the target loop crossover frequency is 70 kHz with a phase margin greater than 50°. The output voltage soft-start time is 4 ms.

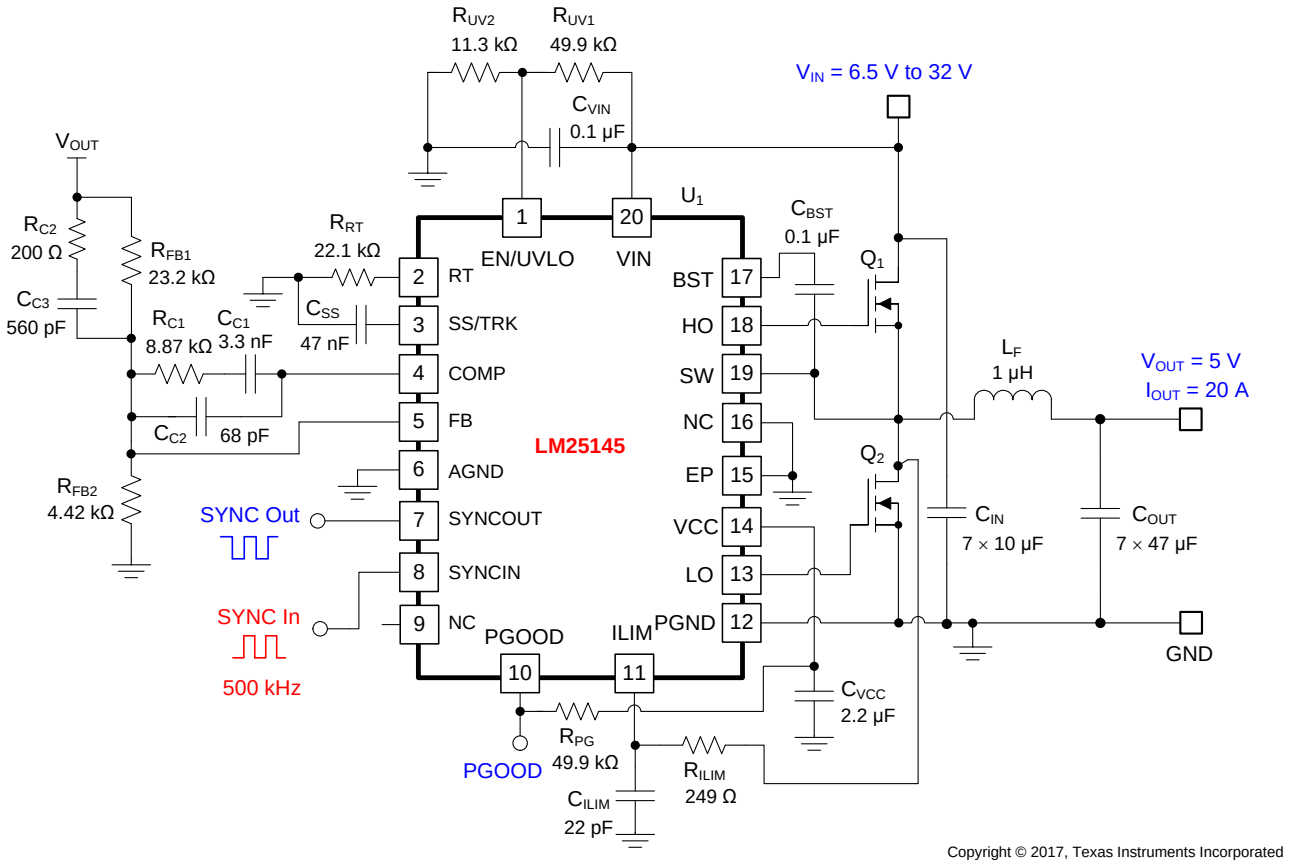

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Figure 46. Application Circuit #1 With LM25145 24-V to 5-V, 20-A Buck Regulator at 500 kHz

NOTE

This and subsequent design examples are provided herein to showcase the LM25145 controller in several different applications. Depending on the source impedance of the input supply bus, an electrolytic capacitor may be required at the input to ensure stability, particularly at low input voltage and high output current operating conditions. See Power Supply Recommendations for more detail.

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9.2.1.1 Design Requirements

The intended input, output, and performance-related parameters pertinent to this design example are shown in Table 6.

Table 6. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	6.5 V to 32 V
Input transient voltage (peak)	42 V
Output voltage and current	5 V, 20 A
Input voltage UVLO thresholds	6.5 V on, 6 V off
Switching frequency (SYNC in)	500 kHz
Output voltage regulation	±1%
Load transient peak voltage deviation	< 100 mV

9.2.1.2 Detailed Design Procedure

The design procedure for an LM25145-based regulator for a given application is streamlined by using the *LM25145 Quickstart Calculator* available as a free download, or by availing of TI's WEBENCH® Power Designer.

The selected buck converter powertrain components are cited in Table 7, and many of the components are available from multiple vendors. The MOSFETs in particular are chosen for both lowest conduction and switching power loss, as discussed in detail in *Power MOSFETs*.

The current limit setpoint in this design is set at 26 A based on the resistor R_{ILIM} and the 2-mΩ $R_{DS(on)}$ of the low-side MOSFET (typical at T_J = 25°C and V_{GS} = 7.5 V). This design uses a low-DCR, metal-powder inductor and an all-ceramic output capacitor implementation.

Table 7. List of Materials for Design 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	7	10 µF, 50 V, X7R, 1210, ceramic	TDK	C3225X7R1H106M
			Murata	GRM32ER71H106KA12L
			AVX	12105C106KAT2A
			Kemet	C1210C106K5RACTU
			Taiyo Yuden	UMK325AB7106MM-T
C_{OUT}	7	47 µF, 10 V, X7R, 1210, ceramic	Murata	GRM32ER71A476KE15L
			Taiyo Yuden	LMK325B7476MM-TR
			AVX	1210ZC476KAT2A
			Kemet	C1210C476M8RAC7800
L_F	1	1 µH, 2.3 mΩ, 40 A, 11.15 × 10 × 3.8 mm	Cyntec	CMLE104T-1R0MS2R307
		1.2 µH, 1.8 mΩ, 25 A, 10.2 × 10.2 × 4.7 mm	Würth Electronik	WE HCI 744325120
		1 µH, 2.3 mΩ, 38 A, 10.9 × 10 × 5.0 mm	Panasonic	ETQP5M1R0YLC
		1 µH, 2.2 mΩ, 36 A, 10.5 × 10 × 6.5 mm	TDK	SPM10065VT-D
Q_1	1	40 V, 3.7 mΩ, high-side MOSFET, SON 5 × 6	Texas Instruments	CSD18503Q5A
Q_2	1	40 V, 2 mΩ, low-side MOSFET, SON 5 × 6	Texas Instruments	CSD18511Q5A
U_1	1	Wide V_{IN} synchronous buck controller	Texas Instruments	LM25145RGYR

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9.2.1.3 Custom Design With WEBENCH® Tools

Click here to create a custom design using the LM25145 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

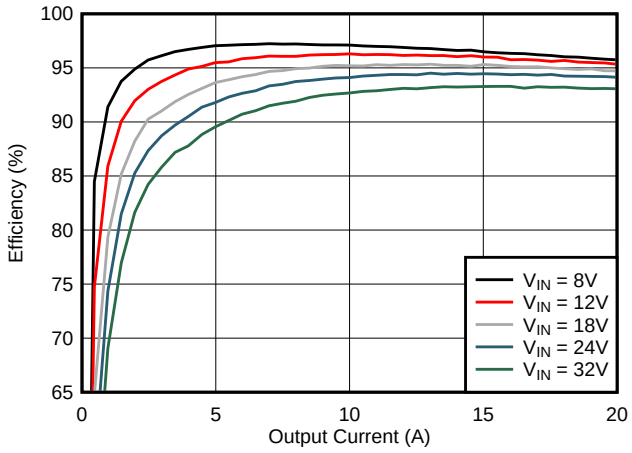
The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

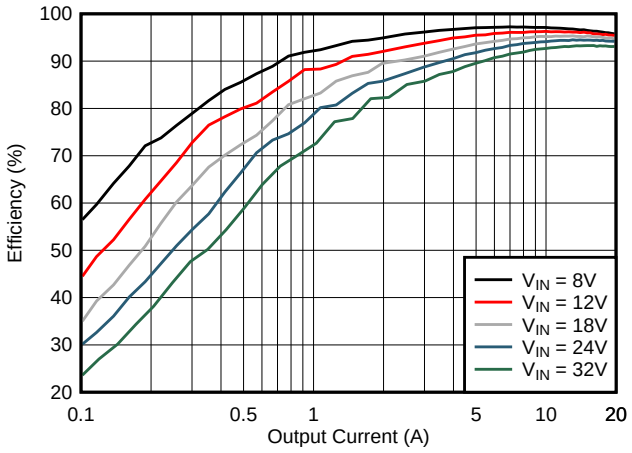
Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.1.4 Application Curves



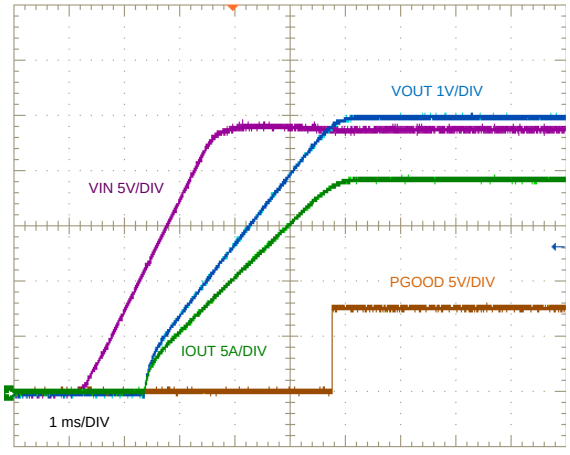
SYNCIN tied to VCC

Figure 47. Efficiency and Power Loss vs I_{OUT} and V_{IN}, CCM



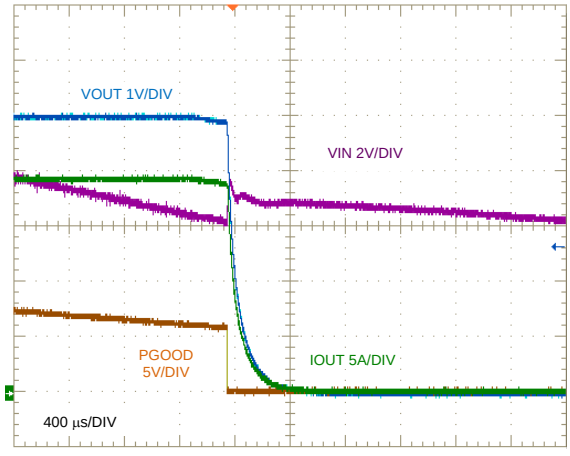
SYNCIN tied to GND

Figure 48. Efficiency and Power Loss vs I_{OUT} and V_{IN}, DCM



V_{IN} step to 24 V 0.25-Ω Load

Figure 49. Start-Up, 20-A Resistive Load



V_{IN} 24 V to 6 V 0.25-Ω Load

Figure 50. Shutdown Through Input UVLO, 20-A Resistive Load

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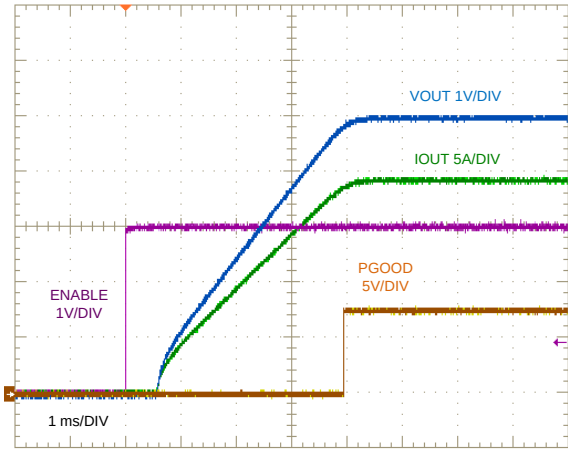
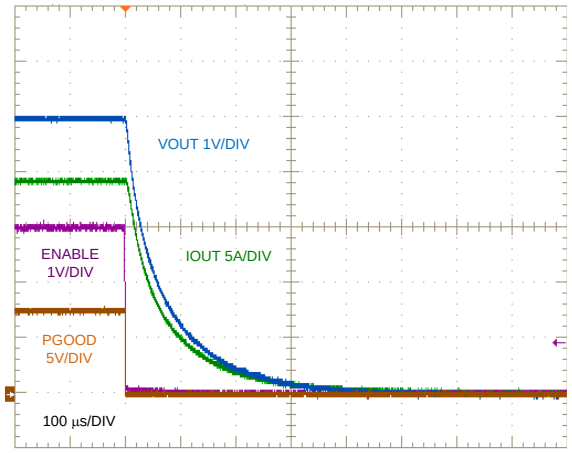


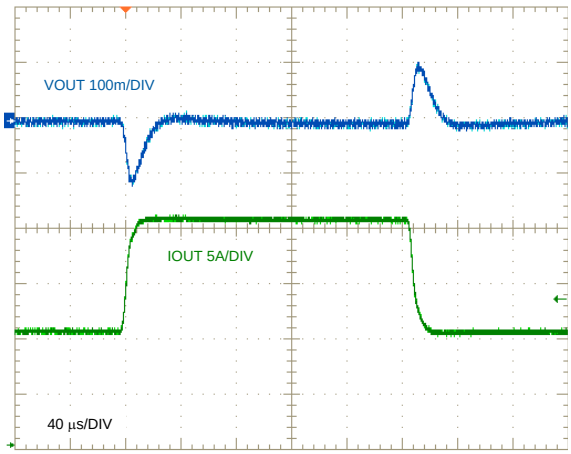
V_{IN} = 24 V 0.25-Ω Load

Figure 51. ENABLE ON, 20-A Resistive Load



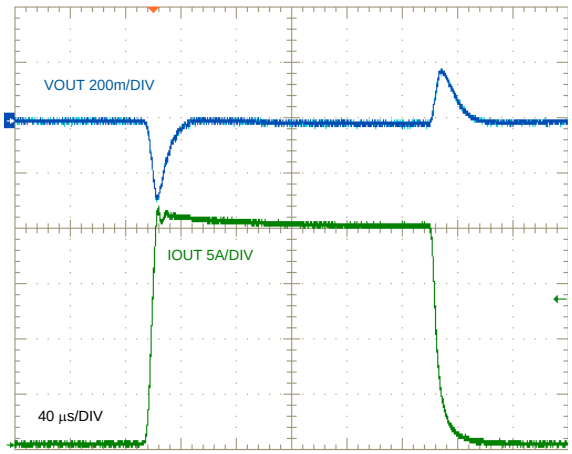
V_{IN} = 24 V 0.25-Ω Load

Figure 52. ENABLE OFF, 20-A Resistive Load



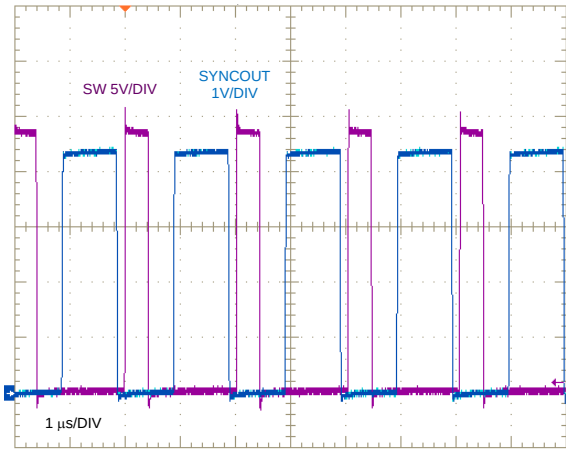
V_{IN} = 24 V

Figure 53. Load Transient Response, 10 A to 20 A to 10 A



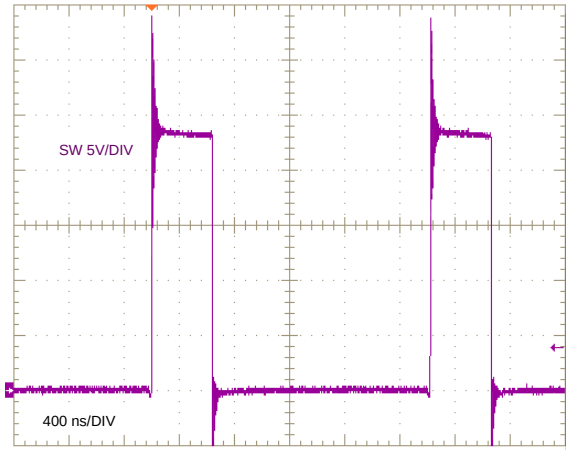
V_{IN} = 24 V

Figure 54. Load Transient Response, 0 A to 20 A to 0 A



V_{IN} = 24 V I_{OUT} = 0 A

Figure 55. SYNCOUT and SW Node Voltages



V_{IN} = 24 V I_{OUT} = 20 A

Figure 56. SW Node Voltage

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9.2.2 Design 2 – High Density, 12-V, 8-A Rail With LDO Low-Noise Auxiliary Output for Industrial Applications

Figure 57 shows the schematic diagram of a 425-kHz, 12-V output, 8-A synchronous buck regulator intended for RF power applications.

An auxiliary 10-V, 800-mA rail to power noise-sensitive circuits is available using the LP38798 ultra-low noise LDO as a post-regulator. The internal pullup of the EN pin of the LP38798 facilitates direct connection to the PGOOD of the LM25145 for sequential start-up control.

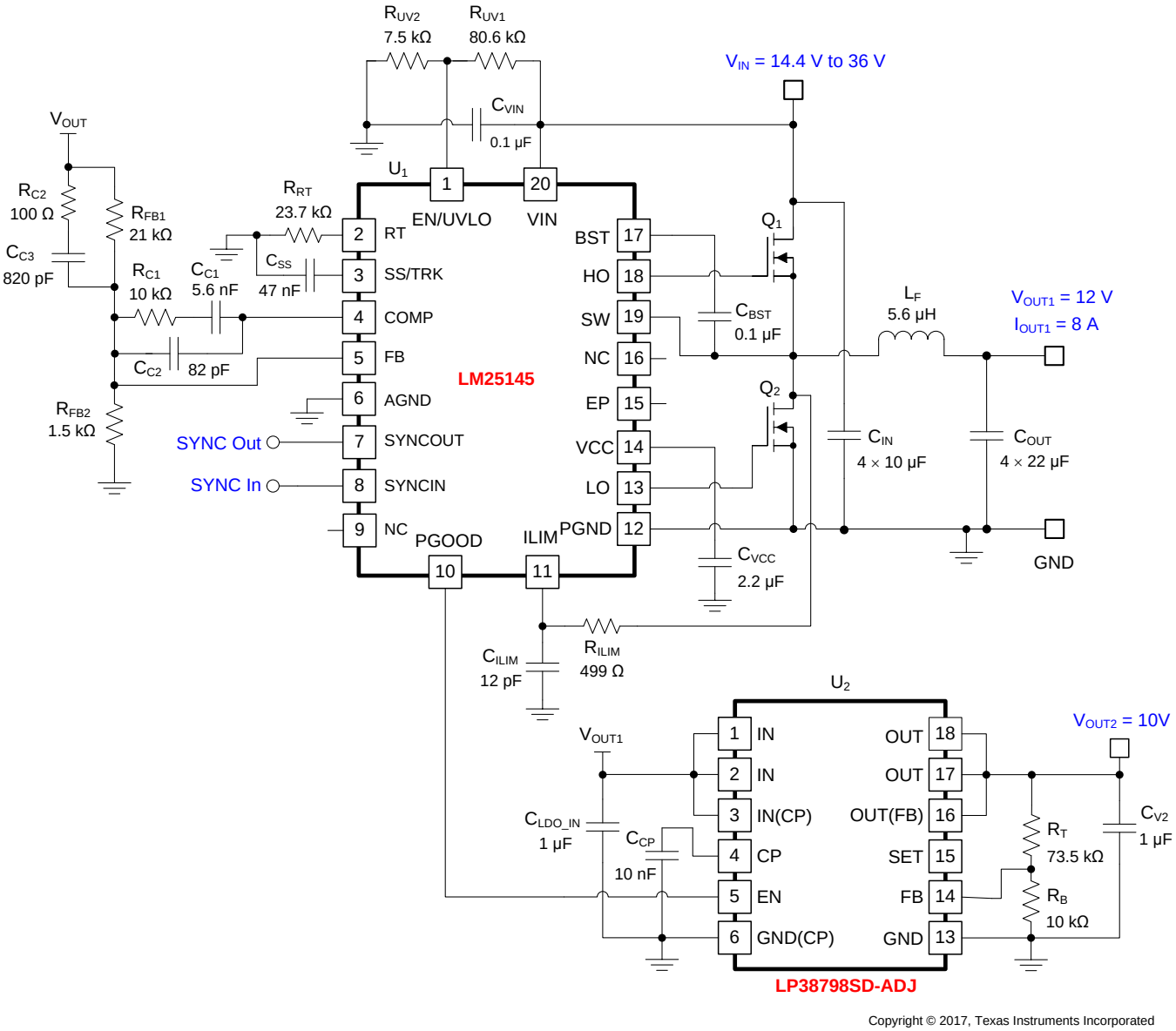

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Figure 57. Application Circuit #2 With LM25145 24-V to 12-V Synchronous Buck Regulator at 425 kHz

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9.2.2.1 Design Requirements

The required input, output, and performance parameters for this application example are shown in Table 8.

Table 8. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	14.4 V to 36 V
Input transient voltage (peak)	42 V
Output voltage and current	12 V, 8 A
Input UVLO thresholds	14 V on, 13.2 V off
Switching frequency	425 kHz
Output voltage regulation	±1%
Load transient peak voltage deviation, 4-A load step, 1 A/µs	< 150 mV

9.2.2.2 Detailed Design Procedure

A high power density, high-efficiency regulator solution is realized by using TI NexFET™ Power MOSFETs, such as CSD18543Q3A (60-V, 8.5-mΩ MOSFET in a SON 3.3-mm × 3.3-mm package), together with a low-DCR inductor and all-ceramic capacitor design. The design occupies 15 mm × 15 mm on a single-sided PCB. The overcurrent (OC) setpoint in this design is set at 11 A based on the resistor R_{ILIM} and the 8.5-mΩ $R_{DS(on)}$ of the low-side MOSFET (typical at T_J = 25°C and V_{GS} = 7.5 V). Connecting VCC to either V_{OUT1} or V_{OUT2} using a series diode reduces bias power dissipation and improves efficiency, especially at light loads.

The selected buck converter powertrain components are cited in Table 9, including power MOSFETs, buck inductor, input and output capacitors, and ICs. Using the *LM25145 Quickstart Calculator*, compensation components are selected based on a target loop crossover frequency of 70 kHz and phase margin greater than 55°. The output voltage soft-start time is 4 ms based on the selected soft-start capacitance, C_{SS}, of 47 nF.

Table 9. List of Materials for Design 2

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	4	10 µF, 50 V, X7R, 1210, ceramic	TDK	C3225X7R1H106M
			Murata	GRM32ER71H106KA12L
			AVX	12105C106KAT2A
C_{OUT}	4	22 µF, 25 V, X7R, 1210, ceramic	Murata	GRM32ER71E226KE15L
			Taiyo Yuden	TMK325B7226MM-TR
			TDK	C3225X7R1E226M
L_F	1	5.6 µH, 17 mΩ, 18 A, 10.85 × 10 × 3.8 mm	Cyntec	CMLS104T-5R6MS
		5.6 µH, 20 mΩ, 14 A, 10.85 × 10 × 3.8 mm	Delta	MPT1040-5R6H1
		5.6 µH, 16 mΩ, 12 A, 10.7 × 10 × 4 mm	Bourns	SRP1040-5R6M
		5.6 µH, 19.3 mΩ, 16 A, 11 × 10 × 4 mm	Laird	MGV10045R6M-10
		6.8 µH, 17.5 mΩ, 14 A, 11 × 10 × 3.8 mm	Würth Electronik	WE-LHMI 74437368068
		6.8 µH, 17.9 mΩ, 25 A, 10.5 × 10 × 4 mm	TDK	SPM10040VT-6R8M-D
		6.8 µH, 18.3 mΩ, 12.1 A, 10.7 × 10 × 4 mm	Panasonic	ETQP4M6R8KVC
Q_1, Q_2	2	60 V, 8 mΩ, MOSFET, SON 3 × 3	Texas Instruments	CSD18543Q3A
U_1	1	Wide V_{IN} synchronous buck controller	Texas Instruments	LM25145RGYR
U_2	1	Ultra-low noise and high-PSRR LDO for RF and analog circuits, 4-mm × 4-mm 12-pin WSON	Texas Instruments	LP38798SD-ADJ

If needed, a 2.2-Ω resistor can be added in series with C_{BST} is used to slow the turn-on transition of the high-side MOSFET, reducing the spike amplitude and ringing of the SW node voltage and minimizing the possibility of Cdv/dt-induced shoot-through of the low-side MOSFET. If needed, place an RC snubber (for example, 2.2 Ω and 100 pF) close to the drain (SW node) and source (PGND) terminals of the low-side MOSFET to further attenuate any SW node voltage overshoot and/or ringing. Please refer to the application note *Reduce Buck Converter EMI and Voltage Stress by Minimizing Inductive Parasitics* for more detail.

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9.2.2.2.1 Application Curves

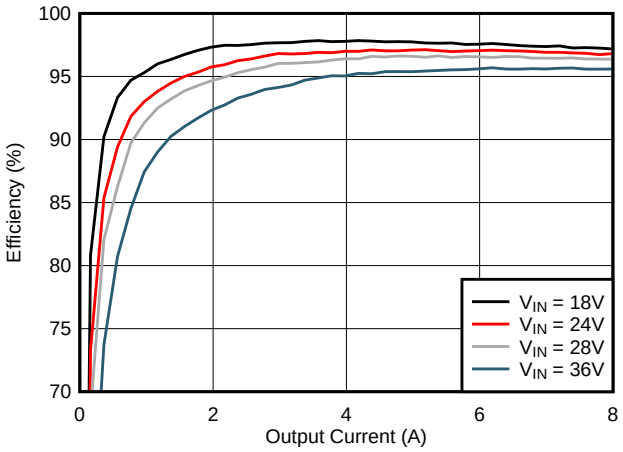

Figure 58. Efficiency vs I_{OUT} and V_{IN}

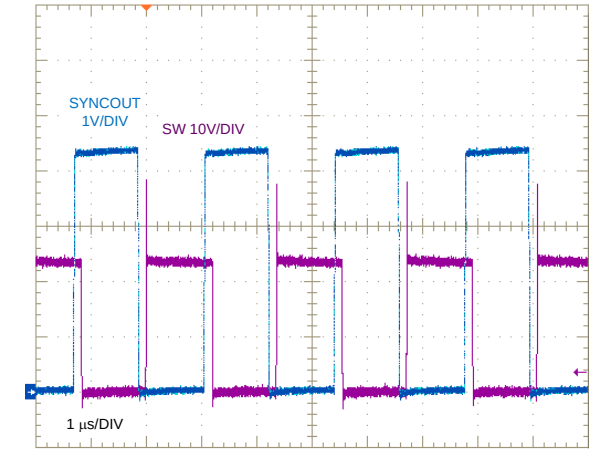

Figure 59. SYNCOUT and SW Node Voltages

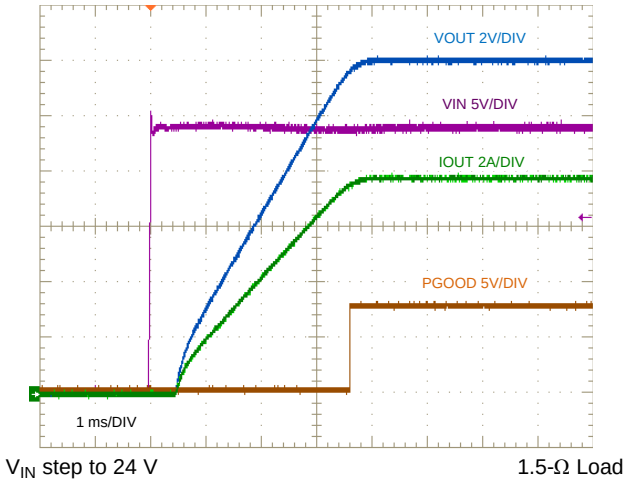

Figure 60. Start-Up, 8-A Resistive Load

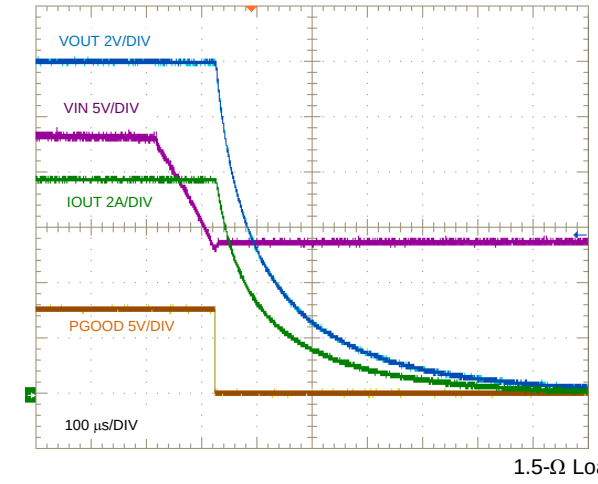

Figure 61. Shutdown Through Input UVLO, 8-A Resistive Load

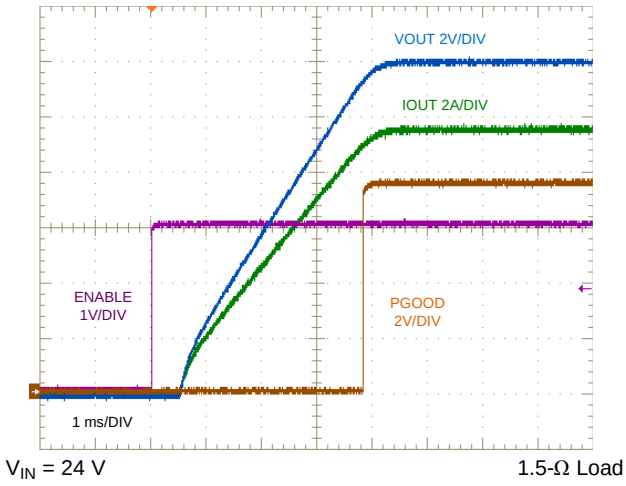

Figure 62. ENABLE ON, 8-A Resistive Load

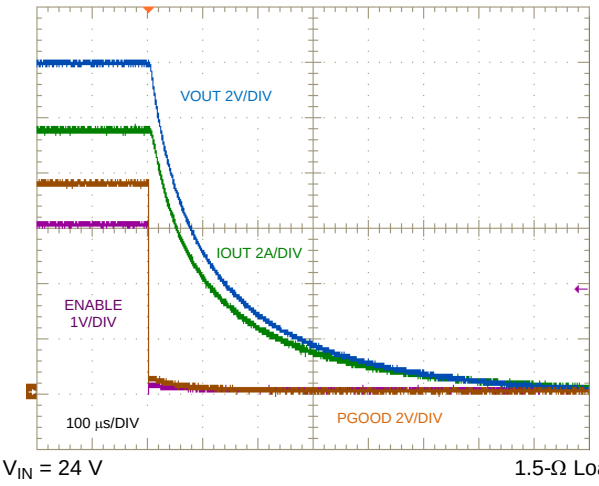

Figure 63. ENABLE OFF, 8-A Resistive Load

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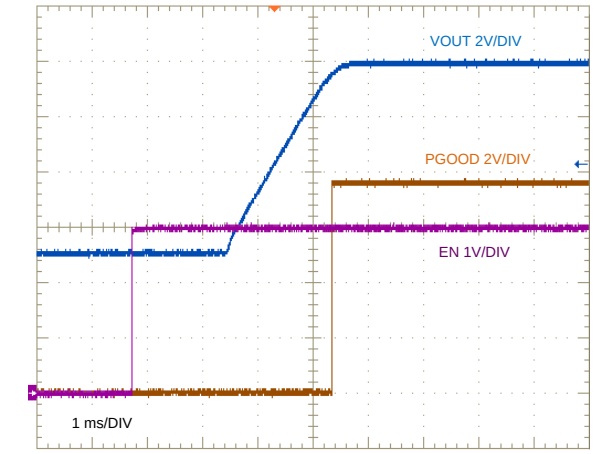
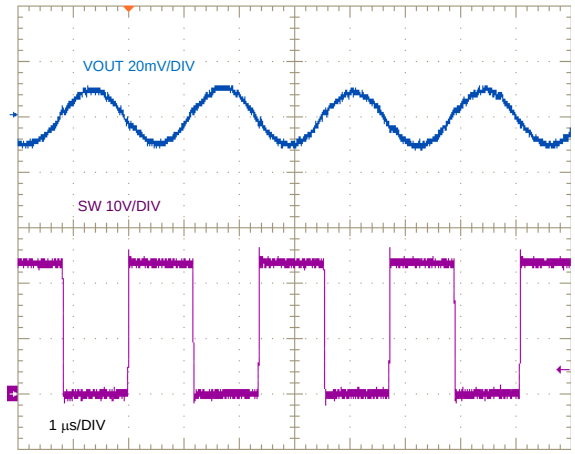


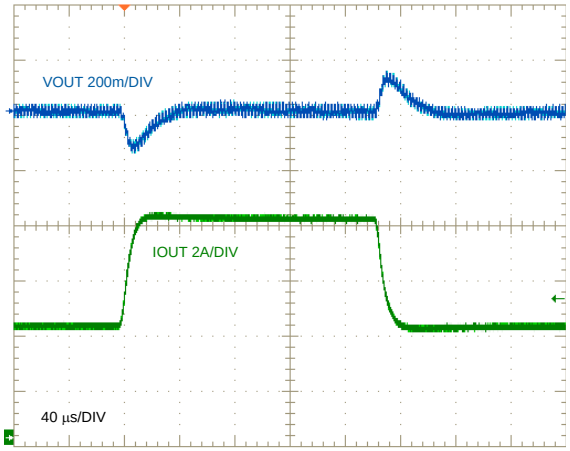
V_{IN} = 24 V I_{OUT} = 0 A

Figure 64. Pre-Biased Start-Up



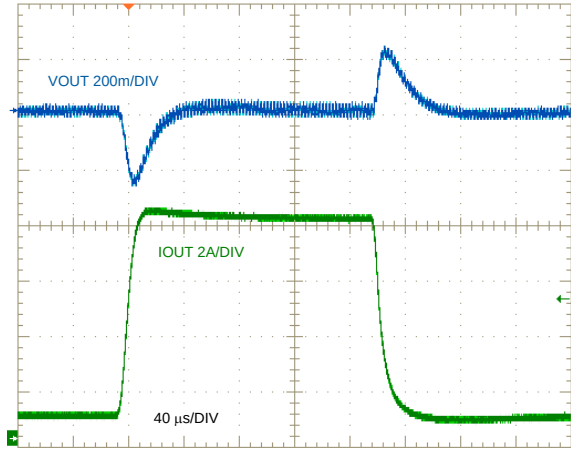
V_{IN} = 24 V I_{OUT} = 0 A

Figure 65. SW Node and VOUT Ripple



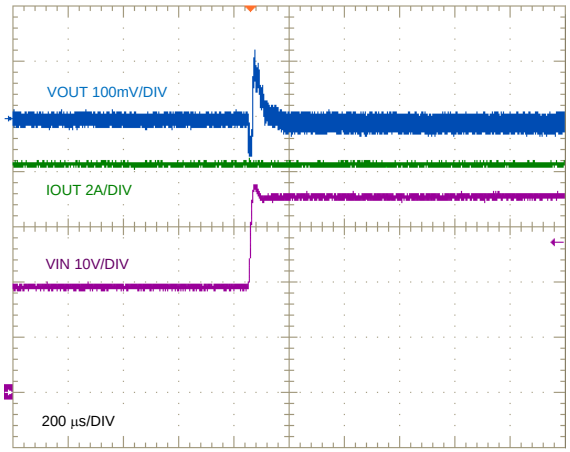
V_{IN} = 24 V

Figure 66. Load Transient Response, 4 A to 8 A to 4 A



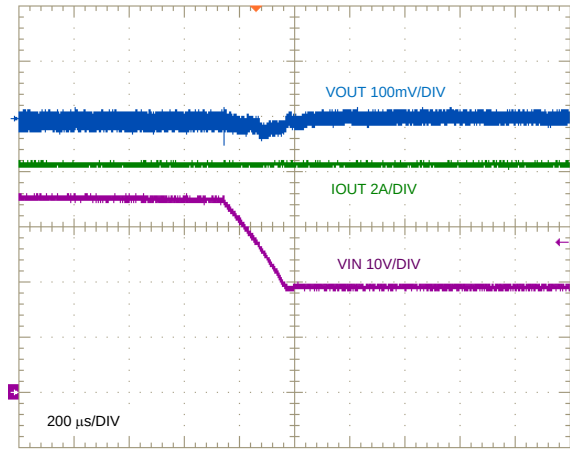
V_{IN} = 24 V

Figure 67. Load Transient Response, 0.8 A to 8 A to 0.8 A



I_{OUT} = 8 A

Figure 68. Line Transient Response, 18 V to 36 V



I_{OUT} = 8 A

Figure 69. Line Transient Response, 36 V to 18 V

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9.2.3 Design 3 – Powering a Multicore DSP From a 24-V Rail

For technical solutions, industry trends, and insights for designing and managing power supplies, please refer to TI's *Power House* blog series.

Figure 70 shows the schematic diagram of a 10-A synchronous buck regulator for a DSP core voltage supply.

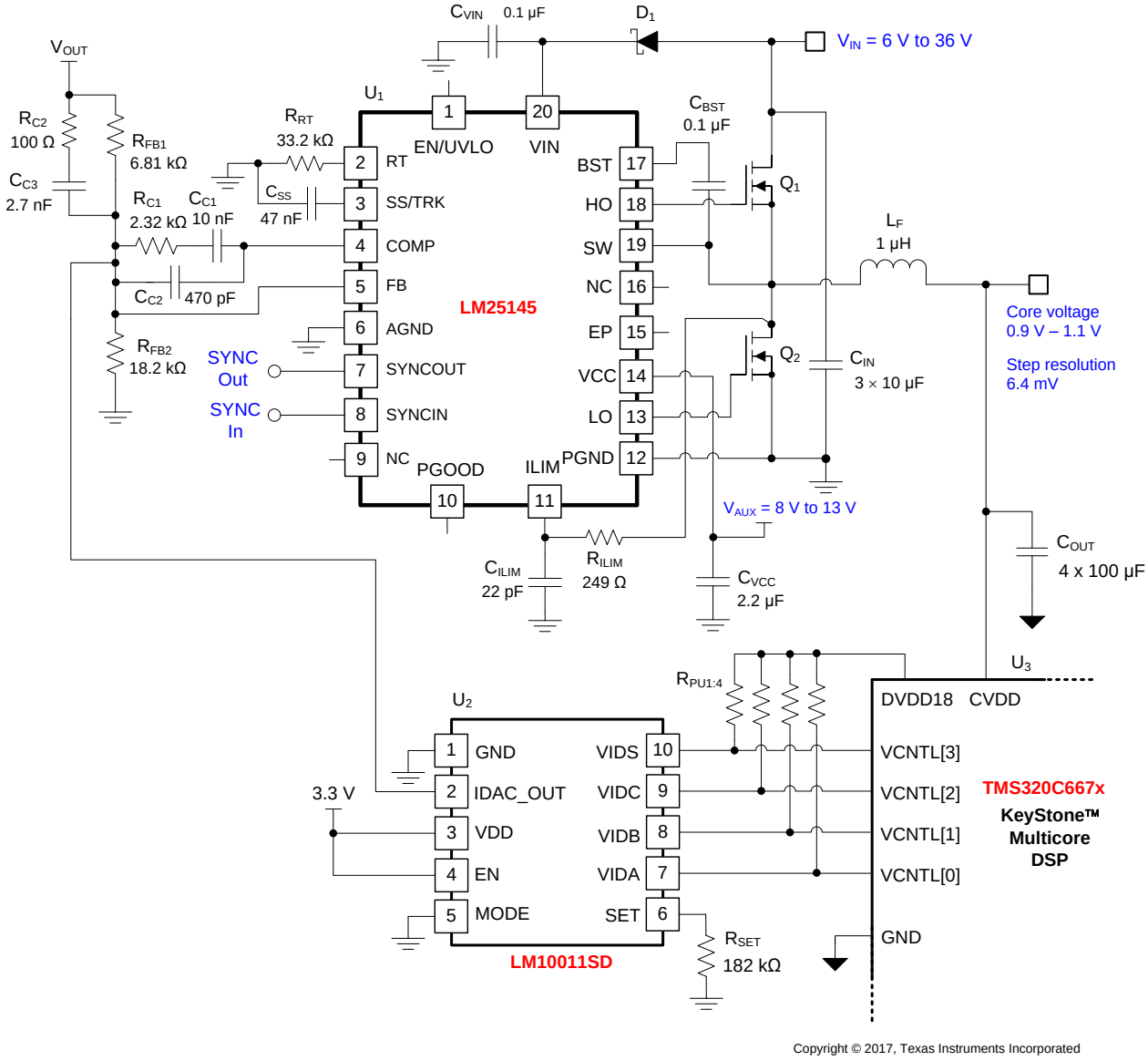

Figure 70. Application Circuit #3 With LM25145 DSP Core Voltage Supply

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9.2.3.1 Design Requirements

For this application example, the intended input, output, and performance parameters are listed in Table 10.

Table 10. Design Parameters

DESIGN PARAMETER	VALUE
Input voltage range (steady-state)	6 V to 36 V
Input transient voltage (peak)	42 V
Output voltage and current	0.9 V to 1.1 V, 10 A
Output voltage regulation	±1%
Load transient peak voltage deviation, 10-A step	< 120 mV
Switching frequency	300 kHz

9.2.3.2 Detailed Design Procedure

The schematic diagram of a 300-kHz, 24-V nominal input, 10-A regulator powering a KeyStone™ DSP is given in Figure 70. This high step-down ratio design leverages the low 40-ns minimum controllable on-time of the LM25145 controller to achieve stable, efficient operation at very low duty cycles. 60-V power MOSFETs, such as TI's CSD18543Q3A and CSD18531Q5A NexFET devices, are used together with a low-DCR, metal-powder inductor, and ceramic output capacitor implementation. An external rail between 8 V and 13 V powers VCC to minimize bias power dissipation, and a blocking diode connected to the VIN pin is used as recommended in Figure 32.

The important components for this design are listed in Table 11.

Table 11. List of Materials for Design 3

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER	PART NUMBER
C_{IN}	3	10 µF, 50 V, X7R, 1210, ceramic	TDK	C3225X7R1H106M
			Murata	GRM32ER71H106KA12L
			AVX	12105C106KAT2A
C_{OUT}	4	100 µF, 6.3V, X7S, 1210, ceramic	Murata	GRM32EC70J107ME15L
			Taiyo Yuden	JMK325AC7107MM-P
		100 µF, 6.3V, X5R, 1206, ceramic	Murata	GRM31CR60J107ME39K
			TDK	C3216X5R0J107M
			Würth Electronik	885012108005
L_F	1	1 µH, 5.6 mΩ, 16 A, 6.95 × 6.6 × 2.8 mm	Cyntec	CMLE063T-1R0MS
		1 µH, 5.5 mΩ, 12 A, 6.65 × 6.45 × 3.0 mm	Würth Electronik	WE XHMI 74439344010
		1 µH, 7.9 mΩ, 16 A, 6.5 × 6.0 × 3.0 mm	Panasonic	ETQP3M1R0YFN
		1 µH, 6.95 mΩ, 18 A, 6.76 × 6.56 × 3.1 mm	Coilcraft	XEL6030-102ME
Q_1	1	60 V, 8.5 mΩ, high-side MOSFET, SON 3 × 3	Texas Instruments	CSD18543Q3A
Q_2	1	60 V, 4 mΩ, low-side MOSFET, SON 5 × 6	Texas Instruments	CSD18531Q5A
U_1	1	Wide V_{IN} synchronous buck controller	Texas Instruments	LM25145RGYR
U_2	1	6- or 4-bit VID voltage programmer, WSON-10	Texas Instruments	LM10011SD
U_3	1	KeyStone™ DSP	Texas Instruments	TMS320C667x

The regulator output current requirements are dependent upon the baseline and activity power consumption of the DSP in a real-use case. While baseline power is highly dependent on voltage, temperature and DSP frequency, activity power relates to dynamic core utilization, DDR3 memory access, peripherals, and so on. To this end, the IDAC_OUT pin of the LM10011 connects to the LM25145 FB pin to allow continuous optimization of the core voltage. The SmartReflex-enabled DSP provides 6-bit information using the VCNTL open-drain I/Os to command the output voltage setpoint with 6.4-mV step resolution.(1)

(1) Refer to *Hardware Design Guide for Keystone I Devices* (SPRAB12) and *How to Optimize Your DSP Power Budget* for further detail.

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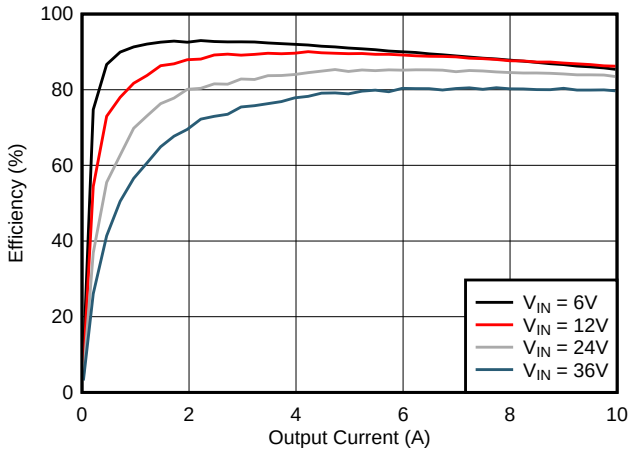
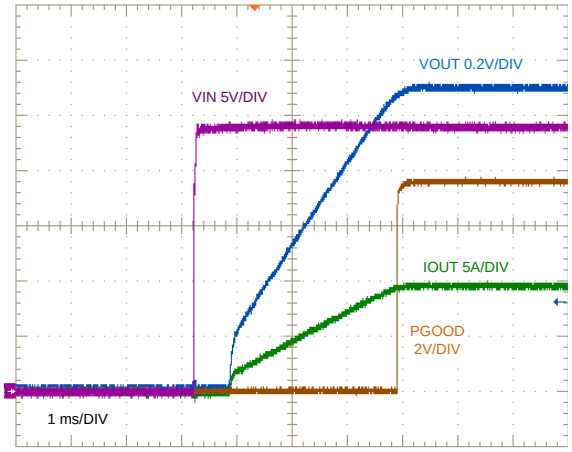
9.2.3.3 Application Curves



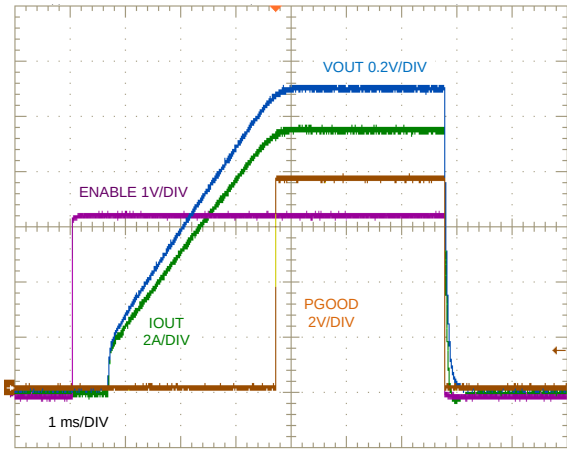
V_{OUT} = 1.1 V V_{AUX} = 8 V

Figure 71. Efficiency vs I_{OUT} and V_{IN}



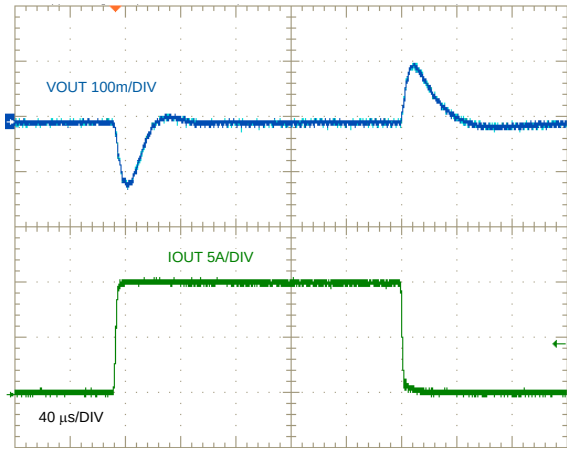
V_{IN} step to 24 V 0.11-Ω Load

Figure 72. Start-Up, 10-A Resistive Load



V_{IN} = 24 V 0.11-Ω Load

Figure 73. ENABLE ON and OFF, 10-A Resistive Load



V_{IN} = 24 V

Figure 74. Load Transient Response, 0 A to 10 A to 0 A

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10 Power Supply Recommendations

The LM25145 buck controller is designed to operate from a wide input voltage range from 6 V to 42 V. The characteristics of the input supply must be compatible with the Absolute Maximum Ratings and Recommended Operating Conditions tables. In addition, the input supply must be capable of delivering the required input current to the fully-loaded regulator. Estimate the average input current with Equation 23.

$$I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} \quad (23)$$

where

- η is the efficiency

If the converter is connected to an input supply through long wires or PCB traces with a large impedance, special care is required to achieve stable performance. The parasitic inductance and resistance of the input cables may have an adverse affect on converter operation. The parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit. This circuit can cause overvoltage transients at VIN each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the regulator is operating close to the minimum input voltage, this dip can cause false UVLO fault triggering and a system reset. The best way to solve such issues is to reduce the distance from the input supply to the regulator and use an aluminum or tantalum input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitors helps to damp the input resonant circuit and reduce any voltage overshoots. A capacitance in the range of 10 µF to 47 µF is usually sufficient to provide input damping and helps to hold the input voltage steady during large load transients.

An EMI input filter is often used in front of the regulator that, unless carefully designed, can lead to instability as well as some of the effects mentioned above. The application report *Simple Success with Conducted EMI for DC-DC Converters* (SNVA489) provides helpful suggestions when designing an input filter for any switching regulator.

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11 Layout

11.1 Layout Guidelines

Proper PCB design and layout is important in a high current, fast switching circuit (with high current and voltage slew rates) to assure appropriate device operation and design robustness. As expected, certain issues must be considered before designing a PCB layout using the LM25145. The high-frequency power loop of the buck converter power stage is denoted by #1 in the shaded area of Figure 75. The topological architecture of a buck converter means that particularly high di/dt current flows in the components of loop #1, and it becomes mandatory to reduce the parasitic inductance of this loop by minimizing its effective loop area. Also important are the gate drive loops of the low-side and high-side MOSFETs, denoted by #2 and #3, respectively, in Figure 75.

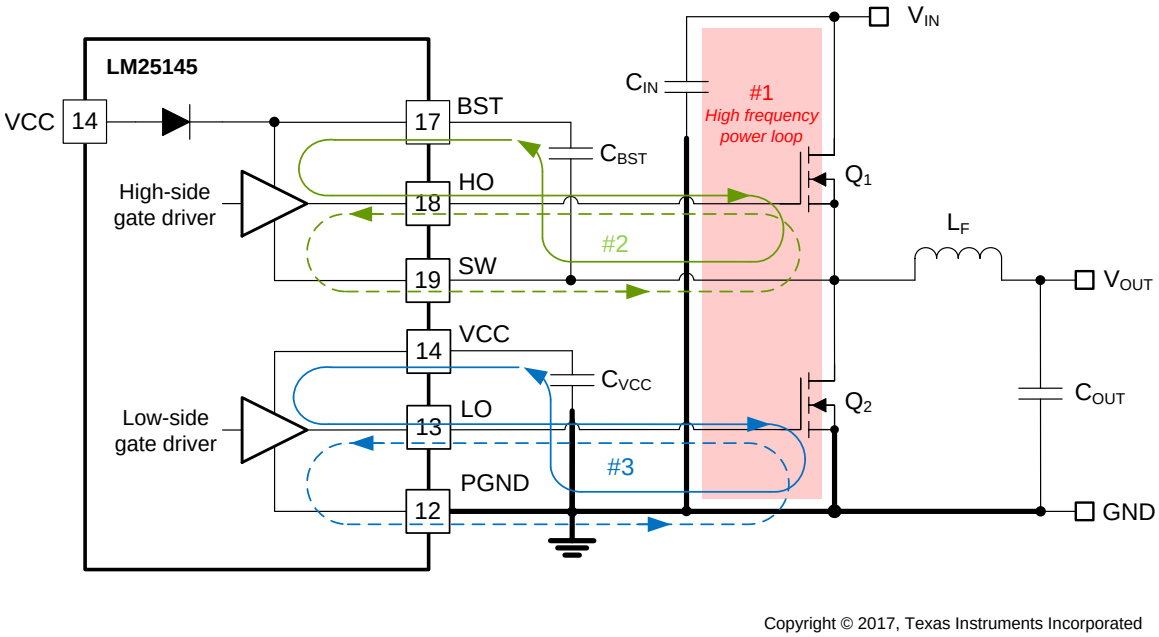

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Figure 75. DC-DC Regulator Ground System With Power Stage and Gate Drive Circuit Switching Loops

11.1.1 Power Stage Layout

1. Input capacitors, output capacitors, and MOSFETs are the constituent components in the power stage of a buck regulator and are typically placed on the top side of the PCB (solder side). The benefits of convective heat transfer are maximized because of leveraging any system-level airflow. In a two-sided PCB layout, small-signal components are typically placed on the bottom side (component side). At least one inner plane should be inserted, connected to ground, to shield and isolate the small-signal traces from noisy power traces and lines.
2. The DC-DC converter has several high-current loops. Minimize the area of these loops in order to suppress generated switching noise and parasitic loop inductance and optimize switching performance.
   - Loop #1: The most important loop to minimize the area of is the path from the input capacitor(s) through the high- and low-side MOSFETs, and back to the capacitor(s) through the ground connection. Connect the input capacitor(s) negative terminal close to the source of the low-side MOSFET (at ground). Similarly, connect the input capacitor(s) positive terminal close to the drain of the high-side MOSFET (at VIN). Refer to loop #1 of Figure 75.
   - Another loop, not as critical though as loop #1, is the path from the low-side MOSFET through the inductor and output capacitor(s), and back to source of the low-side MOSFET through ground. Connect the source of the low-side MOSFET and negative terminal of the output capacitor(s) at ground as close as possible.
3. The PCB trace defined as SW node, which connects to the source of the high-side (control) MOSFET, the drain of the low-side (synchronous) MOSFET and the high-voltage side of the inductor, should be short and wide. However, the SW connection is a source of injected EMI and thus should not be too large.

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Layout Guidelines (continued)

4. Follow any layout considerations of the MOSFETs as recommended by the MOSFET manufacturer, including pad geometry and solder paste stencil design.
5. The SW pin connects to the switch node of the power conversion stage, and it acts as the return path for the high-side gate driver. The parasitic inductance inherent to loop #1 in Figure 75 and the output capacitance (C_{OSS}) of both power MOSFETs form a resonant circuit that induces high frequency (>100 MHz) ringing on the SW node. The voltage peak of this ringing, if not controlled, can be significantly higher than the input voltage. Ensure that the peak ringing amplitude does not exceed the absolute maximum rating limit for the SW pin. In many cases, a series resistor and capacitor snubber network connected from the SW node to GND damps the ringing and decreases the peak amplitude. Provide provisions for snubber network components in the PCB layout. If testing reveals that the ringing amplitude at the SW pin is excessive, then include snubber components as needed.

11.1.2 Gate Drive Layout

The LM25145 high-side and low-side gate drivers incorporate short propagation delays, adaptive dead-time control and low-impedance output stages capable of delivering large peak currents with very fast rise and fall times to facilitate rapid turnon and turnoff transitions of the power MOSFETs. Very high di/dt can cause unacceptable ringing if the trace lengths and impedances are not well controlled.

Minimization of stray or parasitic gate loop inductance is key to optimizing gate drive switching performance, whether it be series gate inductance that resonates with MOSFET gate capacitance or common source inductance (common to gate and power loops) that provides a negative feedback component opposing the gate drive command, thereby increasing MOSFET switching times. The following loops are important:

- Loop #2: high-side MOSFET, Q_1. During the high-side MOSFET turn on, high current flows from the boot capacitor through the gate driver and high-side MOSFET, and back to the negative terminal of the boot capacitor through the SW connection. Conversely, to turn off the high-side MOSFET, high current flows from the gate of the high-side MOSFET through the gate driver and SW, and back to the source of the high-side MOSFET through the SW trace. Refer to loop #2 of Figure 75.
- Loop #3: low-side MOSFET, Q_2. During the low-side MOSFET turnon, high current flows from the VCC decoupling capacitor through the gate driver and low-side MOSFET, and back to the negative terminal of the capacitor through ground. Conversely, to turn off the low-side MOSFET, high current flows from the gate of the low-side MOSFET through the gate driver and GND, and back to the source of the low-side MOSFET through ground. Refer to loop #3 of Figure 75.

The following circuit layout guidelines are strongly recommended when designing with high-speed MOSFET gate drive circuits.

1. Connections from gate driver outputs, HO and LO, to the respective gate of the high-side or low-side MOSFET should be as short as possible to reduce series parasitic inductance. Use 0.65 mm (25 mils) or wider traces. Use via(s), if necessary, of at least 0.5 mm (20 mils) diameter along these traces. Route HO and SW gate traces as a differential pair from the LM25145 to the high-side MOSFET, taking advantage of flux cancellation.
2. Minimize the current loop path from the VCC and BST pins through their respective capacitors as these provide the high instantaneous current, up to 3.5 A, to charge the MOSFET gate capacitances. Specifically, locate the bootstrap capacitor, C_{BST}, close to the BST and SW pins of the LM25145 to minimize the area of loop #2 associated with the high-side driver. Similarly, locate the VCC capacitor, C_{VCC}, close to the VCC and PGND pins of the LM25145 to minimize the area of loop #3 associated with the low-side driver.
3. Placing a 2-Ω to 10-Ω resistor in series with the BST capacitor slows down the high-side MOSFET turnon transition, serving to reduce the voltage ringing and peak amplitude at the SW node at the expense of increased MOSFET turnon power loss.

11.1.3 PWM Controller Layout

With the proviso to locate the controller as close as possible to the MOSFETs to minimize gate driver trace runs, the components related to the analog and feedback signals, current limit setting and temperature sense are considered in the following:

1. Separate power and signal traces, and use a ground plane to provide noise shielding.
2. Place all sensitive analog traces and components such as COMP, FB, RT, ILIM and SS/TRK away from high-voltage switching nodes such as SW, HO, LO or BST to avoid mutual coupling. Use internal layer(s) as

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Layout Guidelines (continued)

ground plane(s). Pay particular attention to shielding the feedback (FB) trace from power traces and components.

3. The upper feedback resistor can be connected directly to the output voltage sense point at the load device or the bulk capacitor at the converter side.
4. Connect the ILIM setting resistor from the drain of the low-side MOSFET to ILIM and make the connections as close as possible to the LM25145. The trace from the ILIM pin to the resistor should avoid coupling to a high-voltage switching net.
5. Minimize the loop area from the VCC and VIN pins through their respective decoupling capacitors to the GND pin. Locate these capacitors as close as possible to the LM25145.

11.1.4 Thermal Design and Layout

The useful operating temperature range of a PWM controller with integrated gate drivers and bias supply LDO regulator is greatly affected by:

- average gate drive current requirements of the power MOSFETs;
- switching frequency;
- operating input voltage (affecting bias regulator LDO voltage drop and hence its power dissipation);
- thermal characteristics of the package and operating environment.

For a PWM controller to be useful over a particular temperature range, the package must allow for the efficient removal of the heat produced while keeping the junction temperature within rated limits. The LM25145 controller is available in a small 3.5-mm × 4.5-mm 20-pin VQFN (RGY) PowerPAD™ package to cover a range of application requirements. The thermal metrics of this package are summarized in Thermal Information. The application report *IC Package Thermal Metrics* (SPRA953) provides detailed information regarding the thermal information table.

The 20-pin VQFN package offers a means of removing heat from the semiconductor die through the exposed thermal pad at the base of the package. While the exposed pad of the package is not directly connected to any leads of the package, it is thermally connected to the substrate of the LM25145 device (ground). This allows a significant improvement in heat sinking, and it becomes imperative that the PCB is designed with thermal lands, thermal vias, and a ground plane to complete the heat removal subsystem. The exposed pad of the LM25145 is soldered to the ground-connected copper land on the PCB directly underneath the device package, reducing the thermal resistance to a very low value. Wide traces of the copper tying in the no-connect pins of the LM25145 (pins 9 and 16) and connection to this thermal land helps to dissipate heat.

Numerous vias with a 0.3-mm diameter connected from the thermal land to the internal and solder-side ground plane(s) are vital to help dissipation. In a multi-layer PCB design, a solid ground plane is typically placed on the PCB layer below the power components. Not only does this provide a plane for the power stage currents to flow but it also represents a thermally conductive path away from the heat generating devices.

The thermal characteristics of the MOSFETs also are significant. The drain pad of the high-side MOSFET is normally connected to a VIN plane for heat sinking. The drain pad of the low-side MOSFET is tied to the SW plane, but the SW plane area is purposely kept relatively small to mitigate EMI concerns.

11.1.5 Ground Plane Design

As mentioned previously, using one or more of the inner PCB layers as a solid ground plane is recommended. A ground plane offers shielding for sensitive circuits and traces and also provides a quiet reference potential for the control circuitry. Connect the PGND pin to the system ground plane using an array of vias under the exposed pad. Also connect the PGND directly to the return terminals of the input and output capacitors. The PGND net contains noise at the switching frequency and can bounce because of load current variations. The power traces for PGND, VIN and SW can be restricted to one side of the ground plane. The other side of the ground plane contains much less noise and is ideal for sensitive analog trace routes.

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11.2 Layout Example

Figure 76 shows an example PCB layout based on the *LM5145EVM-HD-20A* 20-A design. The power component connections are made on the top layer with wide, copper-filled areas. A power ground plane is placed on layer 2 with 6 mil (0.15 mm) spacing to the top layer. The small area of buck regulator hot loop is denoted by the white border in Figure 76.

The LM25145 is located on the bottom side with a surrounding analog ground plane for sensitive analog components as shown in Figure 77. The analog ground plane (AGND) and power ground plane (PGND) are connected at a single point directly under the IC (at the die attach pad or DAP). Refer to the *LM5145 EVM User's Guide* (SNVU545) for more detail.

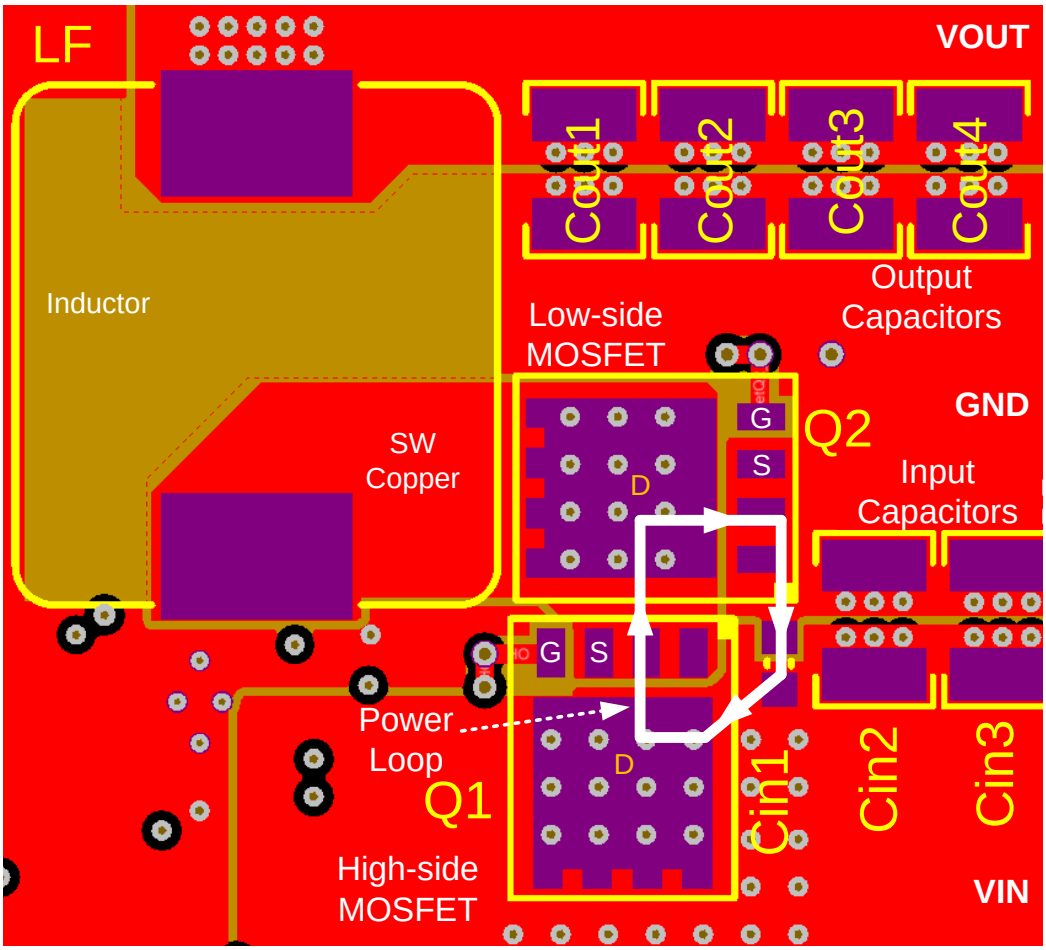

Figure 76. LM25145 Power Stage PCB Layout

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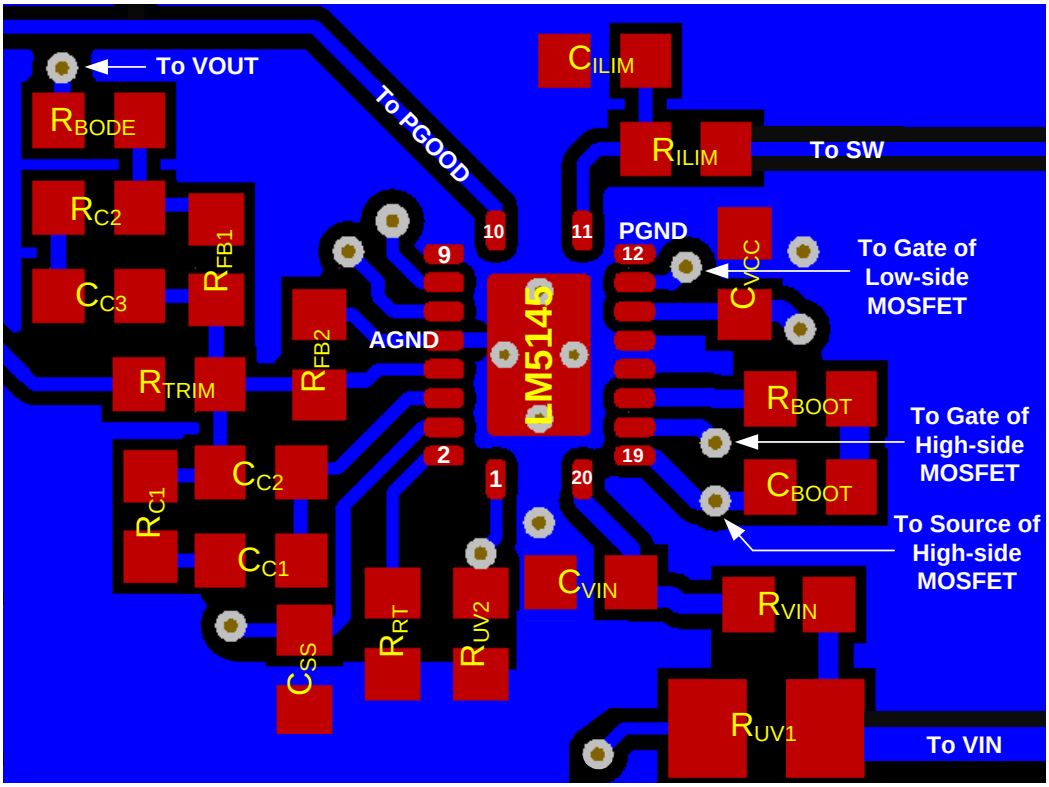
Layout Example (continued)



Legend

Bottom Layer Copper Layer 3 GND Plane Bottom Solder

Figure 77. LM25145 Controller PCB Layout (Viewed From Top)

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12 器件和文档支持

12.1 器件支持

12.1.1 第三方产品免责声明

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12.1.2 开发支持

相关开发支持请参阅以下文档：

- LM25145 快速入门计算器
- LM25145 仿真模型
- 有关 TI 的参考设计库，请访问 TI Designs
- 有关 TI WEBENCH 设计环境，请访问 WEBENCH® 设计中心

12.1.3 使用 WEBENCH® 工具定制设计方案

请单击此处，使用 LM25145 器件并借助 WEBENCH® 电源设计器创建定制设计。

1. 在开始阶段键入输出电压 (V_{IN})、输出电压 (V_{OUT}) 和输出电流 (I_{OUT}) 要求。
2. 使用优化器拨盘优化关键设计参数，如效率、封装和成本。
3. 将生成的设计与德州仪器 (TI) 的其他解决方案进行比较。

WEBENCH Power Designer 提供一份定制原理图以及罗列实时价格和组件可用性的物料清单。

在多数情况下，可执行以下操作：

- 运行电气仿真，观察重要波形以及电路性能
- 运行热性能仿真，了解电路板热性能
- 将定制原理图和布局方案导出至常用 CAD 格式
- 打印设计方案的 PDF 报告并与同事共享

有关 WEBENCH 工具的详细信息，请访问 www.ti.com/WEBENCH。

12.2 文档支持

12.2.1 相关文档

请参阅如下相关文档：

- *《LM5145 同步降压控制器高密度 EVM》*(SNVU545)
- *《通过将电感寄生效应降至最低来降低降压转换器 EMI 和电压应力》*(SLYT682)
- *《直流/直流转换器的传导 EMI 的 AN-2162 简单成功案例》*(SNVA489)
- 白皮书：
  - *《评估适用于具有成本效益的严苛应用的宽 V_{IN}、低 EMI 同步降压 电路》*(SLYY104)
- Power House 博客：
  - *同步降压控制器解决方案支持提供宽 V_{IN} 性能和灵活性*

12.2.1.1 PCB 布局资源

- *《AN-1149 开关电源布局指南》*(SNVA021)
- *《AN-1229 Simple Switcher PCB 布局指南》*(SNVA054)
- *构建电源 - 布局注意事项* (SLUP230)
- *《使用 LM4360x 与 LM4600x 简化低辐射 EMI 布局》*(SNVA721)
- *直流/直流转换器的高密度 PCB 布局*

12.2.1.2 热设计资源

- *《富于洞见而非后知后觉的 AN-2020 热设计》*(SNVA419)
- *《确保外露焊盘封装的最佳热阻性的 AN-1520 电路板布局指南》*(SNVA183)

文档支持 (接下页)

- 《半导体和 IC 封装热指标》（文献编号：SPRA953）
- 《使用 LM43603 和 LM43602 简化热设计》(SNVA719)
- 《PowerPAD™ 热增强型封装》(SLMA002)
- 《PowerPAD 速成》（文献编号：SLMA004）
- 《使用新的热指标》(SBVA025)

12.3 相关链接

下面的表格列出了快速访问链接。类别包括技术文档、支持与社区资源、工具和软件，以及申请样片或购买产品的快速链接。

表 12. 相关链接

器件	产品文件夹	样片与购买	技术文档	工具和软件	支持和社区
LM25145	请单击此处	请单击此处	请单击此处	请单击此处	请单击此处

12.4 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。请单击右上角的*通知我*进行注册，即可收到任意产品信息更改每周摘要。有关更改的详细信息，请查看任意已修订文档中包含的修订历史记录。

12.5 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

12.6 商标

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WEBENCH is a registered trademark of Texas Instruments.
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12.7 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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13 机械、封装和可订购信息

以下页面包括机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据发生变化时，我们可能不会另行通知或修订此文档。如欲获取此产品说明书的浏览器版本，请参见左侧的导航栏。

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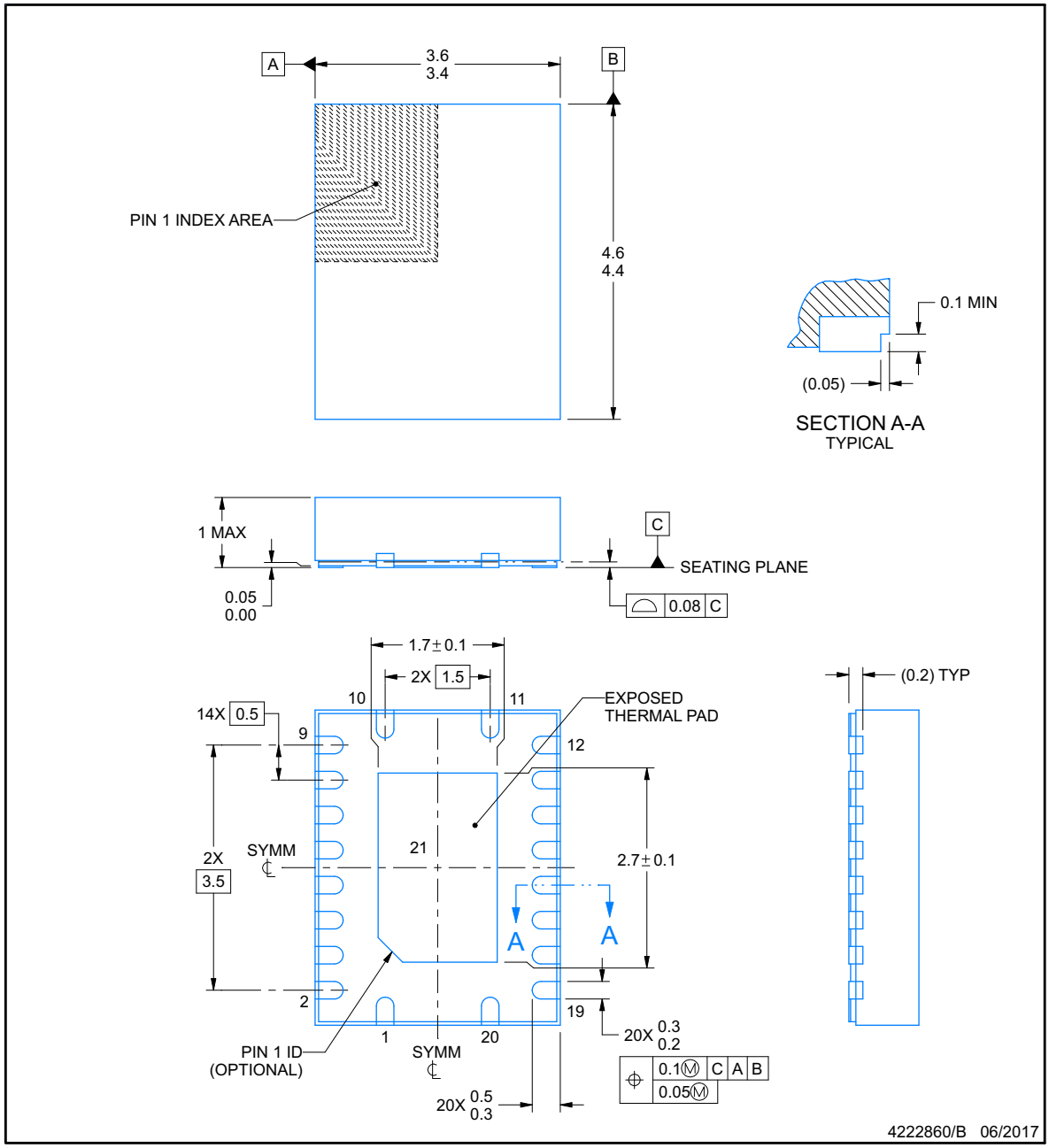
RGY0020B

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

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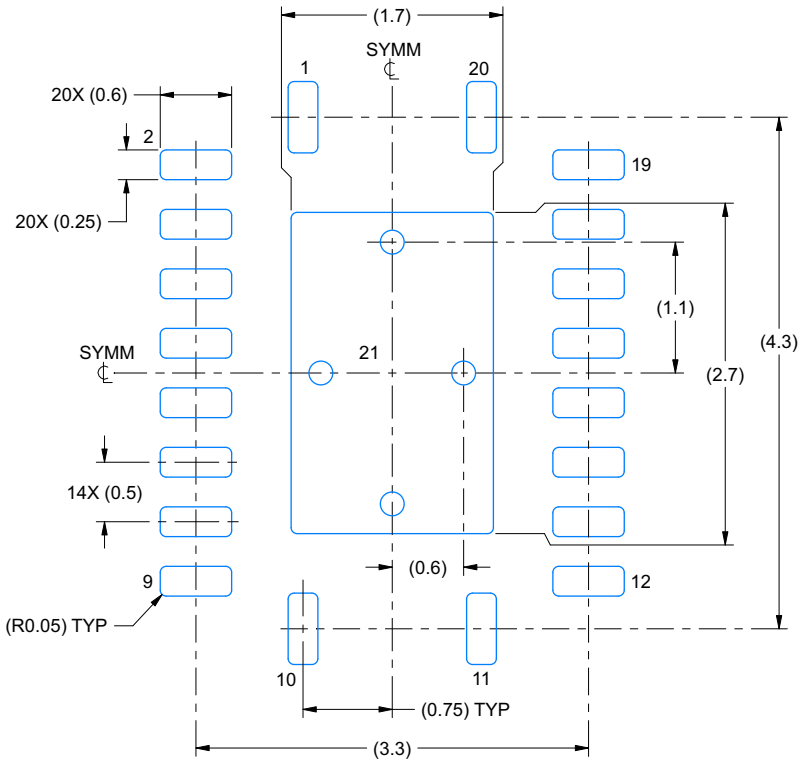
EXAMPLE BOARD LAYOUT

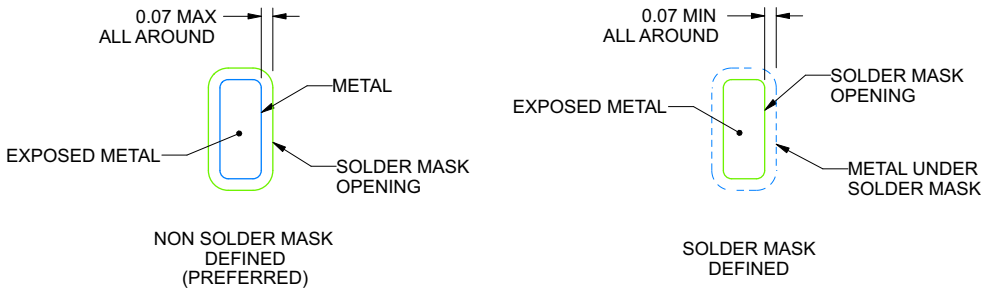
RGY0020B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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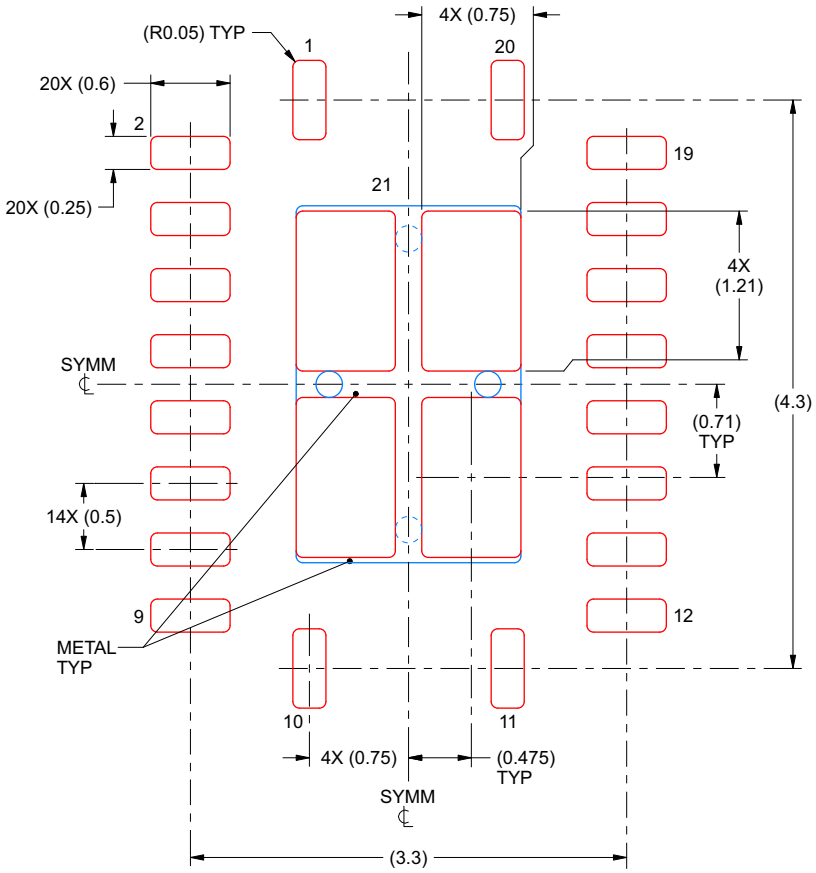
EXAMPLE STENCIL DESIGN

RGY0020B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 21
80% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
LM25145RGYR	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LM 25145
LM25145RGYR.A	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM 25145
LM25145RGYRG4.A	Active	Production	VQFN (RGY) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM 25145
LM25145RGYT	Active	Production	VQFN (RGY) | 20	250 | SMALL T&R	Yes	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	LM 25145
LM25145RGYT.A	Active	Production	VQFN (RGY) | 20	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM 25145

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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