DS90UH928Q-Q1 5MHz 至 85MHz 24 位彩色 FPD-Link III 至 FPD-Link 解串器，具有 HDCP 功能

1 特性

- 支持片载密钥存储的集成型 HDCP 密码引擎
- 支持 HDCP 中继器应用
- 双向控制通道接口，可连接到 I^2C 兼容串行控制总线
- 低电磁干扰 (EMI) FPD-Link 视频输出
- 支持高清 (720p) 数字视频
- 支持 RGB888 + VS，HS，DE 和 I2S 音频
- 支持 5MHz、85MHz 像素时钟
- 多达 4 个针对环绕立体声应用的 I2S 数字音频输出
- 4 条具有 2 个专用引脚的双向通用输入输出 (GPIO) 通道
- 通过 1.8V 或 3.3V 兼容 LVCMOS I/O 接口实现 3.3V 单电源运行
- 长达 10 米的交流耦合屏蔽双绞线 (STP) 互连
- 具有嵌入式时钟的直流均衡和扰频数据
- 自适应电缆均衡
- 图像增强（白平衡和抖动）和内部图案生成
- 汽车应用级产品：符合 AEC-Q100 2 级要求
- >8kV 的人体模型 (HBM) 和 ISO 10605 静电放电 (ESD) 额定值
- 向后兼容模式

2 应用范围

- 汽车导航显示屏
- 后座娱乐系统

3 说明

DS90UH928Q-Q1 解串器与 DS90UH925Q-Q1 或 DS90UH927Q-Q1 串行器配套使用，可针对汽车信息娱乐系统内的内容受保护数字视频的安全分发提供一套解决方案。。 该解串器借助嵌入式时钟（由单信号对 (FPD-Link III) 提供）将高速串行化接口数据转换为四个低压差分信令 (LVDS) 数据/控制流、一个 LVDS 时钟对 (FPD-Link) 以及 I2S 音频数据。 数字视频和音频数据采用业界标准的 HDCP 复制保护方案加以保护。FPD-Link III 串行总线方案支持通过单个差分链路实现高速正向通道数据传输和低速全双工反向通道通信。 通过单个差分对整合音频、视频和和控制数据可减小互连线尺寸和重量，同时还消除了偏差问题并简化了系统设计。

通过对串行输入数据流使用自适应输入均衡功能，可对传输介质损耗和确定性抖动进行补偿。 通过使用低压差分信令可最大限度减少电磁干扰 (EMI)。

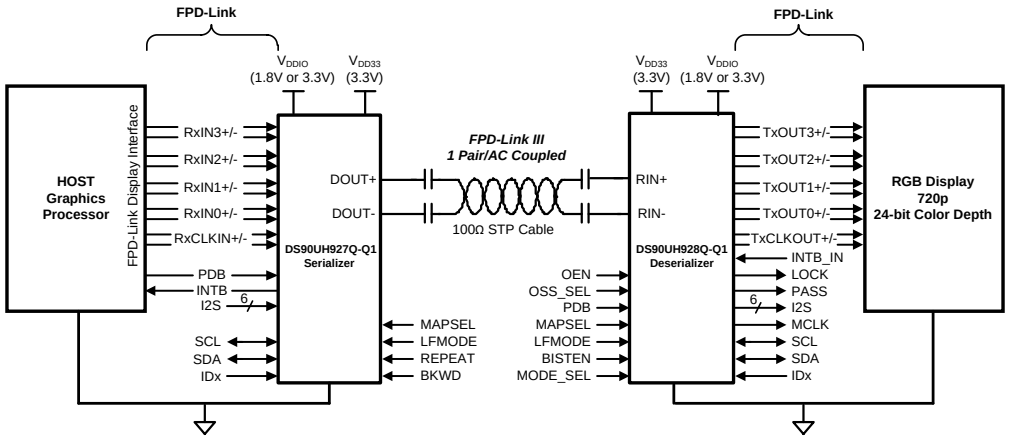
串化器和解串器上都执行 HDCP 密钥引擎。 HDCP 密钥被存储在片载存储器中。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DS90UH928Q-Q1	WQFN (48)	7.00mm x 7.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

4 应用图



目录

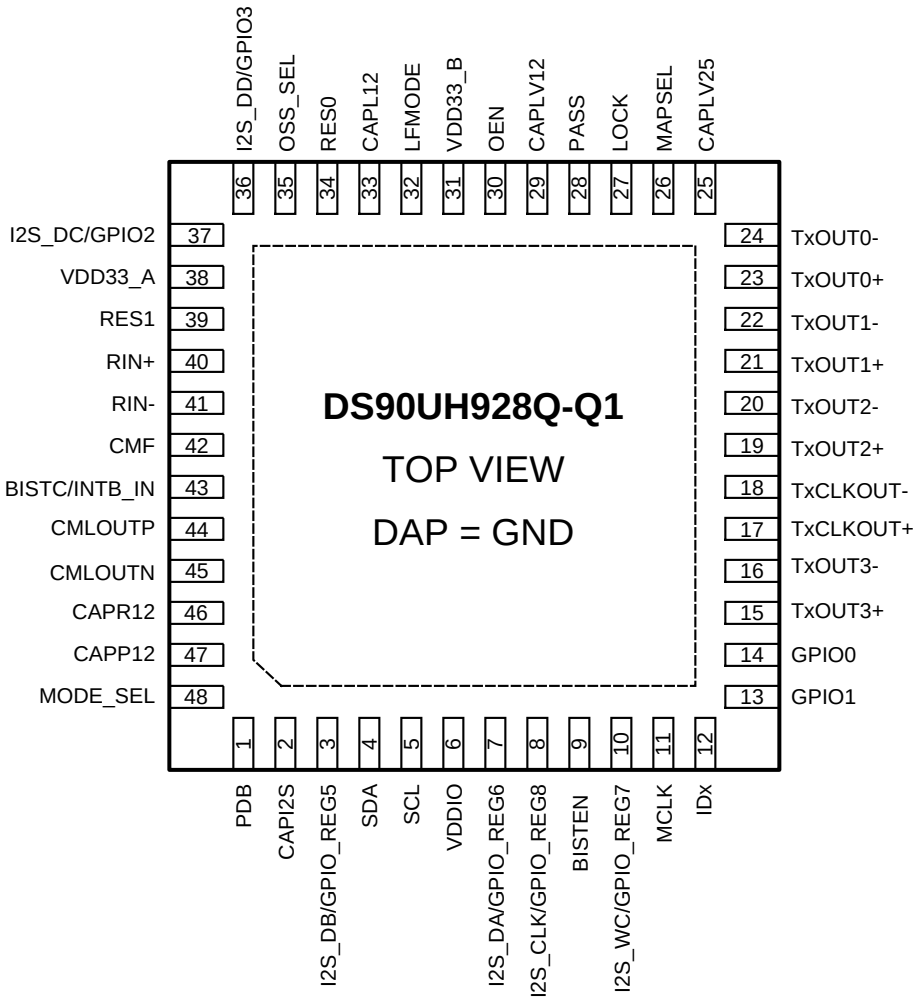
5 修订历史记录

Changes from Revision A (April 2013) to Revision B **Page**

- 已添加 *ESD 额定值表*，*特性描述*部分，*器件功能模式*，*应用和实施*部分，*电源相关建议*部分，*布局*部分，*器件和文档支持*部分以及*机械、封装和可订购信息*部分 ... 1

6 Pin Configuration and Functions

RHS Package
48-Pin WQFN
Top View



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
FPD-LINK OUTPUT INTERFACE			
TxCLKOUT-	18	O, LVDS	Inverting LVDS Clock Output The pair requires external 100Ω differential termination for standard LVDS levels
TxCLKOUT+	17	O, LVDS	True LVDS Clock Output The pair requires external 100Ω differential termination for standard LVDS levels
TxOUT[3:0]-	16, 20, 22, 24	O, LVDS	Inverting LVDS Data Outputs Each pair requires external 100Ω differential termination for standard LVDS levels
TxOUT[3:0]+	15, 19, 21, 23	O, LVDS	True LVDS Data Outputs Each pair requires external 100Ω differential termination for standard LVDS levels
LVCMOS INTERFACE			
GPIO[1:0]	13, 14	I/O, LVCMOS with pulldown	General Purpose IO
GPIO[3:2]	36, 37	I/O, LVCMOS with pulldown	General Purpose I/O Shared with I2S_DD, I2S_DC

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
GPIO_REG[8:5]	8, 10, 7, 3	I/O, LVCMOS with pulldown	General Purpose I/O, register access only Shared with I2S_CLK, I2S_WC, I2S_DA, I2S_DB
I2S_DA I2S_DB I2S_DC I2S_DD	7 3 37 36	O, LVCMOS	Digital Audio Interface I2S Data Outputs Shared with GPIO_REG6, GPIO_REG5, GPIO2, GPIO3
INTB_IN	43	I, LVCMOS with pulldown	HDCP Interrupt Input Shared with BISTC
MCLK I2S_WC I2S_CLK	11 10 8	O, LVCMOS	Digital Audio Interface I2S Master Clock, Word Clock and I2S Bit Clock Outputs I2S_WC and I2S_CLK are shared with GPIO_REG7 and GPIO_REG8
CONTROL AND CONFIGURATION			
BISTC	43	I, LVCMOS with pulldown	BIST Clock Select Shared with INTB_IN Requires a 10-kΩ pullup if set HIGH
BISTEN	9	I, LVCMOS with pulldown	BIST Enable Requires a 10-kΩ pullup if set HIGH
IDx	12	I, Analog	I2C Address Select External pullup to V_{DD33} is required under all conditions. **DO NOT FLOAT.** Connect to external pullup to V_{DD33} and pulldown to GND to create a voltage divider. See Table 6
LFMODE	32	I, LVCMOS with pulldown	Low Frequency Mode Select LFMODE = 0, 15 MHz ≤ TxCLKOUT ≤ 85 MHz (Default) LFMODE = 1, 5 MHz ≤ TxCLKOUT < 15 MHz Requires a 10-kΩ pullup if set HIGH
MAPSEL	26	I, LVCMOS with pulldown	FPD-Link Output Map Select MAPSEL = 0, LSBs on TxOUT3± (Default) MAPSEL = 1, MSBs on TxOUT3± Requires a 10-kΩ pullup if set HIGH
MODE_SEL	48	I, Analog	Device Configuration Select Configures Backwards Compatibility (BKWD), Repeater (REPEAT), I2S 4-channel (I2S_B), and Long Cable (LCBL) modes Connect to external pullup to V_{DD33} and pulldown to GND resistors to create a voltage divider. **DO NOT FLOAT** See Table 5
OEN	30	I, LVCMOS with pulldown	Output Enable Requires a 10-kΩ pullup if set HIGH See Table 4
OSS_SEL	35	I, LVCMOS with pulldown	Output Sleep State Select Requires a 10-kΩ pullup if set HIGH See Table 4
PDB	1	I, LVCMOS	Power-down Mode Input Pin Must be driven or pulled up to V_{DD33}. Refer to “Power Up Requirements and PDB Pin" in the Applications Information Section. PDB = H, device is enabled (normal operation) PDB = L, device is powered down When the device is in the powered down state, the LVDS and LVCMOS outputs are tri-state, the PLL is shutdown, and I_{DD} is minimized. Control Registers are **RESET**.
SCL	5	I/O, Open Drain	I^2C Clock Input/Output Interface Must have an external pullup to V_{DD33}. **DO NOT FLOAT** Recommended pullup: 4.7 kΩ
SDA	4	I/O, Open Drain	I2C Data Input/Output Interface Must have an external pullup to V_{DD33}. **DO NOT FLOAT** Recommended pullup: 4.7 kΩ
STATUS			
LOCK	27	O, LVCMOS	LOCK Status Output 0: PLL is unlocked, I2S, GPIO, TxOUT[3:0]±, and TxCLKOUT± are idle with output states controlled by OEN and OSS_SEL. May be used to indicate Link Status or Display Enable. 1: PLL is locked, outputs are active with output states controlled by OEN and OSS_SEL Route to test point or pad (Recommended). Float if unused.

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
PASS	28	O, LVCMOS	PASS Status Output 0: One or more errors were detected in the received BIST payload (BIST Mode) 1: Error-free transmission (BIST Mode) Route to test point or pad (Recommended). Float if unused.
FPD-LINK III SERIAL INTERFACE			
CMF	42	Analog	Common Mode Filter Requires a 0.1-µF capacitor to GND
CMLOUTN	45	O, LVDS	Inverting Loop-through Driver Output Monitor point for equalized forward channel differential signal
CMLOUTP	44	O, LVDS	True Loop-through Driver Output Monitor point for equalized forward channel differential signal
RIN-	41	I/O, LVDS	FPD-Link III Inverting Input The output must be AC-coupled with a 0.1-µF capacitor
RIN+	40	I/O, LVDS	FPD-Link III True Input The output must be AC-coupled with a 0.1-µF capacitor
POWER AND GROUND (1)			
GND	DAP	Ground	Large metal contact at the bottom center of the device package **Connect to the ground plane (GND) with at least 9 vias**
VDD33_A VDD33_B	38 31	Power	3.3-V Power to on-chip regulator Each pin requires a 4.7-µF capacitor to GND
VDDIO	6	Power	1.8 V/3.3 V LVCMOS I/O Power Requires a 4.7-µF capacitor to GND
REGULATOR CAPACITOR			
CAPI2S CAPLV25 CAPLV12 CAPR12 CAPP12	2 25 29 46 47	CAP	Decoupling capacitor connection for on-chip regulator Each requires a 4.7-µF decoupling capacitor to GND
CAPL12	33	CAP	Decoupling capacitor connection for on-chip regulator Requires two 4.7-µF decoupling capacitors to GND
OTHER			
RES[1:0]	39, 34	GND	Reserved Connect to GND

(1) The V_{DD} (V_{DD33} and V_{DDIO}) supply ramp should be faster than 1.5 ms with a monotonic rise.

7 Specifications

7.1 Absolute Maximum Ratings (1) (2)

	MIN	MAX	UNIT
Supply Voltage – V_{DD33} (3)	−0.3	4.0	V
Supply Voltage – V_{DDIO} (3)	−0.3	4.0	V
LVCMOS I/O Voltage	−0.3	(V_{DDIO} + 0.3)	V
Deserializer Input Voltage	−0.3	2.75	V
Junction Temperature		150	°C
48 LLP Package Maximum Power Dissipation Capacity at 25°C			
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications, see product folder at www.ti.com and SNOA549.
(3) The DS90UH928Q-Q1V_{DD33} and V_{DDIO} voltages require a specific ramp rate during power up. The power supply ramp time must be less than 1.5 ms with a monotonic rise.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002, all pins[1]		±8000	V
		Charged device model (CDM), per AEC Q100-011, all pins		±1250	
		Machine model (MM)		±250	
		(IEC, powered-up only) R_D = 330 Ω, C_S = 150 pF	Air Discharge (Pins 40, 41, 44, and 45)	±15000	
			Contact Discharge (Pins 40, 41, 44, and 45)	±8000	
		(ISO10605) R_D = 330 Ω, C_S = 150 pF	Air Discharge (Pins 40, 41, 44, and 45)	±15000	
			Contact Discharge (Pins 40, 41, 44, and 45)	±8000	
		(ISO10605) R_D = 2 kΩ, C_S = 150 pF or 330 pF	Air Discharge (Pins 40, 41, 44, and 45)	±15000	
			Contact Discharge (Pins 40, 41, 44, and 45)	±8000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply Voltage (V_{DD33})[1]		3.0	3.3	3.6	V
LVCMOS Supply Voltage (V_{DDIO})[1] [2]	Connect V_{DDIO} to 3.3 V and use 3.3-V IOs	3.0	3.3	3.6	V
	Connect V_{DDIO} to 1.8 V and use 1.8-V IOs	1.71	1.8	1.89	V
Operating Free Air Temperature (T_A)		−40	+25	+105	°C
PCLK Frequency (out of TxCLKOUT±)		5		85	MHz
Supply Noise[3]				100	mV_{P-P}

(1) The DS90UH928Q-Q1V_{DD33} and V_{DDIO} voltages require a specific ramp rate during power up. The power supply ramp time must be less than 1.5 ms with a monotonic rise.
(2) V_{DDIO} should not exceed V_{DD33} by more than 300 mV (V_{DDIO} < V_{DD33} + 0.3 V).
(3) Supply noise testing was done with minimum capacitors on the PCB. A sinusoidal signal is AC-coupled to the V_{DD33} and V_{DDIO} supplies with amplitude >100 mVp-p measured at the device VDD33 and VDDIO pins. Bit error rate testing of input to the Ser and output of the Des with 10 meter cable shows no error when the noise frequency on the Ser is less than 50 MHz. The Des on the other hand shows no error when the noise frequency is less than 50 MHz.

7.4 Thermal Information

THERMAL METRIC[1]		DS90UH928Q-Q1 RHS (WQFN) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	26.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	4.4	
$R_{\theta JB}$	Junction-to-board thermal resistance	4.3	
ψ_{JT}	Junction-to-top characterization parameter	0.1	
ψ_{JB}	Junction-to-board characterization parameter	4.3	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

7.5 DC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
3.3 V LVCMOS I/O							
V_{IH}	High Level Input Voltage	V_{DDIO} = 3.0 V to 3.6 V	GPIO[3:0], REG_GPIO[8:5], LFMODE, MAPSEL, BISTEN, BISTC, INTB_IN, OEN, OSS_SEL	2.0		V_{DDIO}	V
V_{IL}	Low Level Input Voltage			GND		0.8	V
I_{IN}	Input Current	V_{IN} = 0 V or V_{IN} = 3.0 V to 3.6 V		−10	±1	+10	µA
V_{IH}	High Level Input Voltage		(4)PDB	2.0		V_{DDIO}	V
V_{IL}	Low Level Input Voltage			GND		0.7	V
I_{IN}	Input Current	V_{IN} = 0 V or V_{IN} = 3.0 V to 3.6 V (4)		−10	±1	+10	µA
V_{OH}	HIGH Level Output Voltage	I_{OH} = -4 mA	GPIO[3:0], REG_GPIO[8:5], MCLK, I2S_WC, I2S_CLK, I2S_D[A:D], LOCK, PASS	2.4		V_{DDIO}	V
V_{OL}	LOW Level Output Voltage	I_{OL} = +4 mA		0		0.4	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V (5)			−55		mA
I_{OZ}	Tri-state Output Current	V_{OUT} = 0 V or V_{DDIO}, PDB = L		−20		+20	µA

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* conditions and/or notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD33} = 3.3 V, V_{DDIO} = 1.8 V or 3.3 V, Ta = +25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages.
(4) PDB is specified to 3.3 V LVCMOS only and must be driven or pulled up to V_{DD33} or to $V_{DDIO} \geq$ 3.0 V.
(5) I_{OS} is not specified for an indefinite period of time. Do not hold in short circuit for more than 500 ms or part damage may result.

DC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
1.8 V LVCMOS I/O							
V_{IH}	High Level Input Voltage	V_{DDIO} = 1.71 V to 1.89 V	GPIO[3:0], REG_GPIO[8:5], LFMODE, MAPSEL, BISTEN, BISTC, INTB_IN, OEN, OSS_SEL	0.65 * V_{DDIO}		V_{DDIO}	V
V_{IL}	Low Level Input Voltage			0		0.35 * V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0 V or V_{IN} = 1.71 V to 1.89 V		-10		10	µA
V_{OH}	HIGH Level Output Voltage	I_{OH} = -4 mA	GPIO[3:0], REG_GPIO[8:5], MCLK, I2S_WC, I2S_CLK, I2S_D[A:D], LOCK, PASS	V_{DDIO} - 0.45		V_{DDIO}	V
V_{OL}	LOW Level Output Voltage	I_{OL} = +4 mA		0		0.45	V
I_{OS}	Output Short Circuit Current	V_{OUT} = 0 V (5)			-35		mA
I_{OZ}	TRI-STATE® Output Current	V_{OUT} = 0 V or V_{DDIO}, PDB = L,		-20		20	µA
FPD-LINK LVDS OUTPUT							
V_{OD}	Output Voltage Swing (single-ended)	R_L = 100 Ω	TxCLK±, TxOUT[3:0]±	350	450	600	mV
V_{ODp-p}	Differential Output Voltage				900		mV
ΔV_{OD}	Output Voltage Unbalance				1	50	mV
V_{OS}	Common Mode Voltage			1.0	1.2	1.5	V
ΔV_{OS}	Offset Voltage Unbalance				1	50	mV
I_{OS}	Output Short Circuit Current	V_{OUT} = GND			-5		mA
I_{OZ}	Output TRI-STATE® Current	OEN = GND, V_{OUT} = V_{DDIO} or GND, 0.8 V≤V_{IN}≤1.6 V		-500		500	µA
FPD-LINK III RECEIVER							
V_{TH}	Input Threshold High	V_{CM} = 2.1 V (Internal V_{BIAS})	RIN±			50	mV
V_{TL}	Input Threshold Low			-50			mV
V_{ID}	Input Differential Threshold					100	mV
V_{CM}	Common-mode Voltage				2.1		V
R_T	Internal Termination Resistance (Differential)			80	100	120	Ω
LOOP-THROUGH MONITOR OUTPUT							
V_{ODp-p}	Differential Output Voltage	R_L = 100 Ω	CMLOUTP, CMLOUTN		360		mV
SUPPLY CURRENT							
I_{DD1}	Supply Current R_L = 100Ω, PCLK = 85MHz	Checkerboard Pattern	V_{DD33}= 3.6 V		190	250	mA
I_{DDIO1}			V_{DDIO} = 3.6 V		0.1	1	mA
			V_{DDIO} = 1.89 V		0.1	1	mA
I_{DD2}		Random Pattern	V_{DD33}= 3.6 V		185		mA
I_{DDIO2}			V_{DDIO} = 3.6 V		0.1		mA
			V_{DDIO} = 1.89 V		0.1		mA
I_{DDZ}	Supply Current — Power Down	PDB = 0 V, All other LVCMOS inputs = 0 V	V_{DD33} = 3.6 V		3	8	mA
I_{DDIOZ}			V_{DDIO} = 3.6 V		100	500	µA
			V_{DDIO} = 1.89 V		50	250	µA

7.6 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
GPIO							
$t_{GPIO,FC}$	GPIO Pulse Width, Forward Channel	See (4)	GPIO[3:0], PCLK = 5MHz to 85MHz	>2/PCLK			s
$t_{GPIO,BC}$	GPIO Pulse Width, Back Channel	See (4)	GPIO[3:0]	20			µs
RESET							
t_{LRST}	PDB Reset Low Pulse	See (4)	PDB	2			ms
LOOP-THROUGH MONITOR OUTPUT							
E_W	Differential Output Eye Opening Width	R_L = 100 Ω, Jitter freq > f/40	RIN±		>0.4		UI
E_H	Differential Output Eye Height				>300		mV
FPD-LINK LVDS OUTPUT							
t_{TLHT}	Low to High Transition Time	R_L = 100 Ω	TxCLK±, TxOUT[3:0]±		0.25	0.5	ns
t_{THLT}	High to Low Transition Time				0.25	0.5	ns
t_{DCCJ}	Cycle-to-Cycle Output Jitter	PCLK = 5 MHz	TxCLK±		170	275	ps
		PCLK = 85 MHz			35	55	
t_{TTPn}	Transmitter Pulse Position	5 MHz≤PCLK≤85 MHz n=[6:0] for bits [6:0] See Figure 13	TxOUT[3:0]±		0.5 + n		UI
Δt_{TTP}	Offset Transmitter Pulse Position (bit 6 - bit 0)	PCLK = 85 MHz			<0.1		UI
t_{DD}	Delay Latency				147*T		T
t_{TPDD}	Power Down Delay Active to OFF				900		µs
t_{TXZR}	Enable Delay OFF to Active				6		ns
FPD-LINK III INPUT							
t_{DDLT}	Lock Time (4)	5 MHz≤PCLK≤85 MHz	RIN±, LOCK		6	40	ms
LVCMOS OUTPUTS							
t_{CLH}	Low to High Transition Time	C_L = 8 pF	LOCK, PASS		3	7	ns
t_{CHL}	High to Low Transition Time				2	5	ns
BIST MODE							
t_{PASS}	BIST PASS Valid Time		PASS		800		ns
I2S TRANSMITTER							
t_J	Clock Output Jitter		MCLK		2		ns
T_{I2S}	I2S Clock Period Figure 10, (4) (5)	PCLK=5 MHz to 85 MHz	I2S_CLK, PCLK = 5MHz to 85MHz		>2/PCLK or >77		ns
T_{HC}	I2S Clock High Time Figure 10, (5)		I2S_CLK	0.35			T_{I2S}
T_{LC}	I2S Clock Low Time Figure 10, (5)		I2S_CLK	0.35			T_{I2S}

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* conditions and/or notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD33} = 3.3 V, V_{DDIO} = 1.8 V or 3.3 V, Ta = +25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages.
(4) Specification is ensured by design and is not tested in production.
(5) I2S specifications for t_{LC} and t_{HC} pulses must each be greater than 1 PCLK period to ensure sampling and supersedes the 0.35*T_{I2S_CLK} requirement. t_{LC} and t_{HC} must be longer than the greater of either 0.35*T_{I2S_CLK} or 2*PCLK.

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified. (1) (2) (3)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
t_{sr}	I2S Set-up Time		I2S_WC I2S_D[A:D]	0.2			T_{I2S}
t_{hr}	I2S Hold Time		I2S_WC I2S_D[A:D]	0.2			T_{I2S}

7.7 Timing Requirements for the Serial Control Bus

Over 3.3-V supply and temperature ranges unless otherwise specified. (1) (2)

			MIN	TYP	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard Mode	0		100	kHz
		Fast Mode	0		400	kHz
t_{LOW}	SCL Low Period	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_{HIGH}	SCL High Period	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition (3)	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
$t_{SU:STA}$	Set Up time for a start or a repeated start condition (3)	Standard Mode	4.7			µs
		Fast Mode	0.6			µs
$t_{HD;DAT}$	Data Hold Time (3)	Standard Mode	0		3.45	µs
		Fast Mode	0		0.9	µs
$t_{SU;DAT}$	Data Set Up Time (3)	Standard Mode	250			ns
		Fast Mode	100			ns
$t_{SU;STO}$	Set Up Time for STOP Condition (3)	Standard Mode	4.0			µs
		Fast Mode	0.6			µs
t_{BUF}	Bus Free Time Between STOP and START (3)	Standard Mode	4.7			µs
		Fast Mode	1.3			µs
t_r	SCL & SDA Rise Time, (3)	Standard Mode			1000	ns
		Fast Mode			300	ns
t_f	SCL & SDA Fall Time, (3)	Standard Mode			300	ns
		Fast mode			300	ns

(1) The *Electrical Characteristics* tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* conditions and/or notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD33} = 3.3 V, V_{DDIO} = 1.8 V or 3.3 V, T_A = +25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Specification is ensured by design and is not tested in production.

7.8 Timing Requirements

			MIN	NOM	MAX	UNIT
t_R	SDA RiseTime – READ	SDA, RPU = 10 kΩ, Cb ≤ 400 pF, Figure 9		430		ns
t_F	SDA Fall Time – READ			20		ns
$t_{SU;DAT}$	Set Up Time — READ	Figure 9		560		ns
$t_{HD;DAT}$	Hold Up Time — READ	Figure 9		615		ns

7.9 DC and AC Serial Control Bus Characteristics

Over 3.3-V supply and temperature ranges unless otherwise specified. (1) (2) (3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	Input High Level	SDA and SCL	0.7* V_{DDIO}		V_{DD33}	V
V_{IL}	Input Low Level Voltage	SDA and SCL	GND		0.3* V_{DD33}	V
V_{HY}	Input Hysteresis			>50		mV
V_{OL}		SDA or SCL, IOL = 1.25 mA	0		0.36	V
I_{in}		SDA or SCL, Vin = V_{DDIO} or GND	-10		+10	µA
t_{SP}	Input Filter			50		ns
C_{in}	Input Capacitance	SDA or SCL		<5		pF

(1) The *Electrical Characteristics* tables list specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics* conditions and/or notes. Typical specifications are estimations only and are not ensured.
(2) Typical values represent most likely parametric norms at V_{DD33} = 3.3 V, V_{DDIO} = 1.8 V or 3.3 V, T_A = +25°C, and at the *Recommended Operating Conditions* at the time of product characterization and are not ensured.
(3) Current into device pins is defined as positive. Current out of a device pin is defined as negative. Voltages are referenced to ground except V_{OD} and ΔV_{OD}, which are differential voltages.

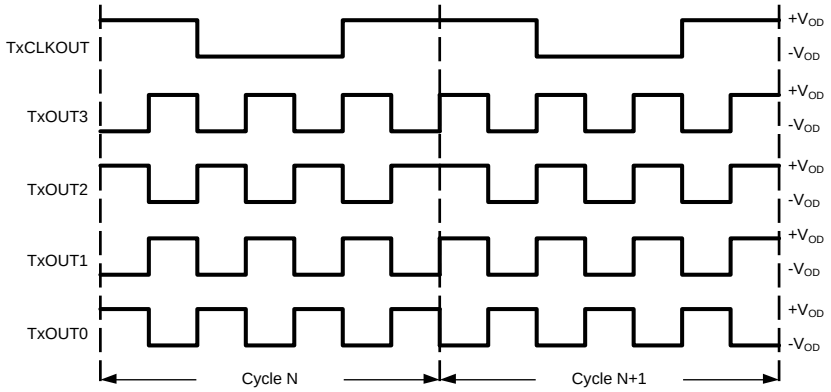


Figure 1. Checkerboard Data Pattern

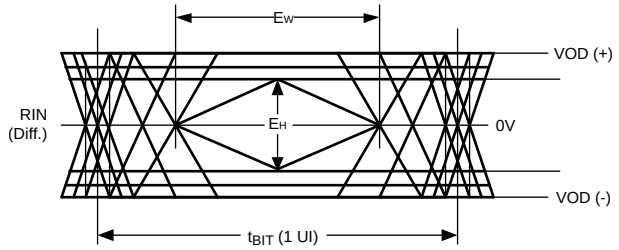


Figure 2. CML Output Driver

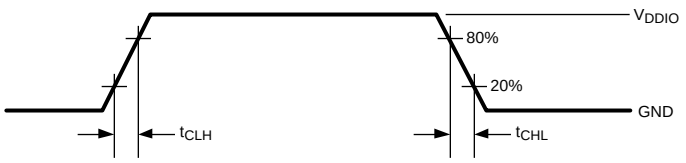


Figure 3. LVCMOS Transition Times

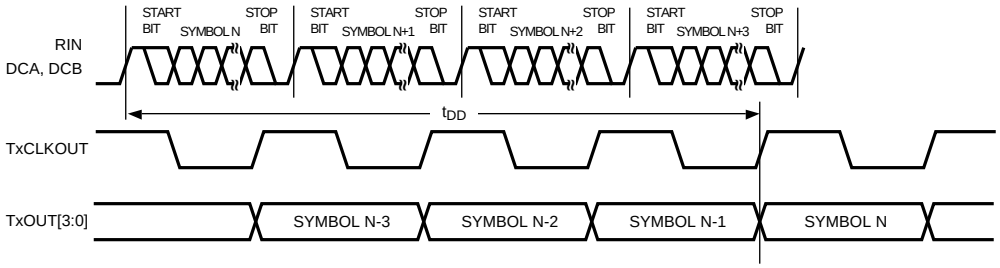


Figure 4. Latency Delay

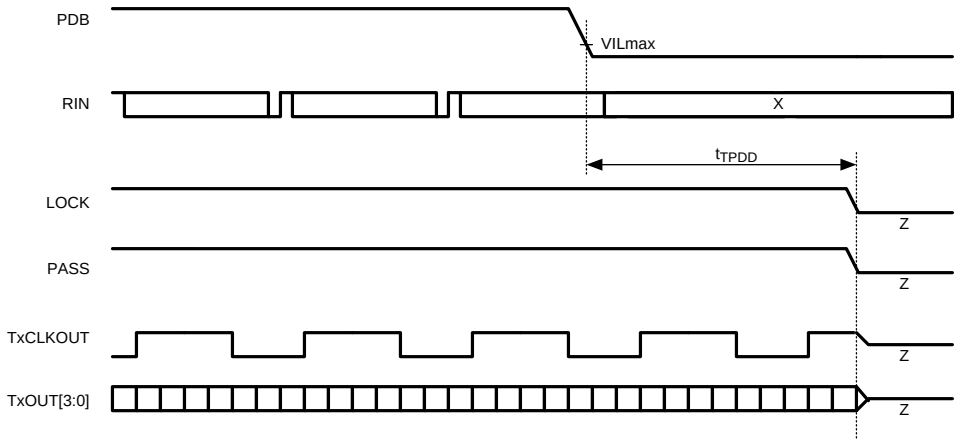


Figure 5. FPD-Link & LVCMOS Power Down Delay

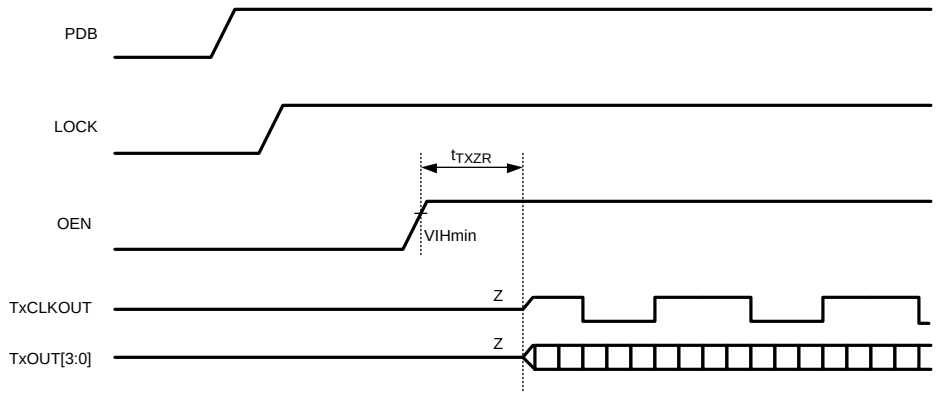


Figure 6. FPD-Link Outputs Enable Delay

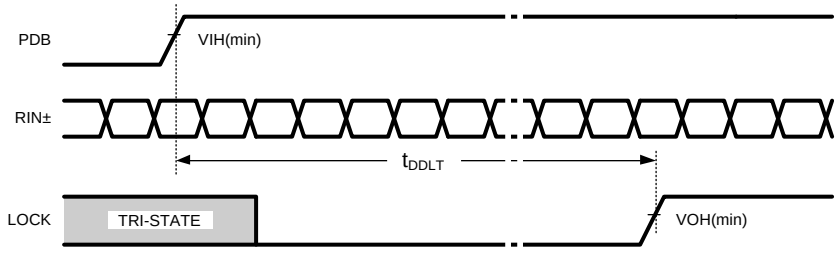


Figure 7. CML PLL Lock Time

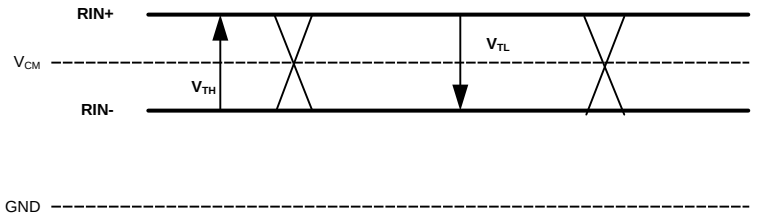


Figure 8. FPD-Link III Receiver DC V_{TH}/V_{TL} Definition

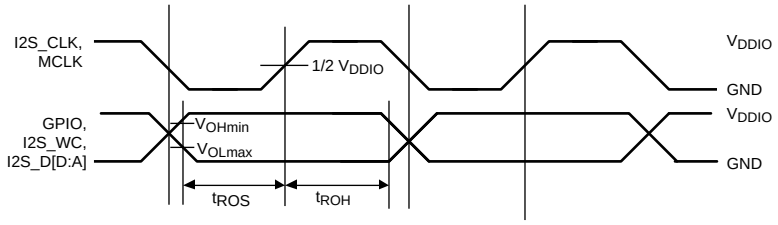


Figure 9. Output Data Valid (Setup and Hold) Times

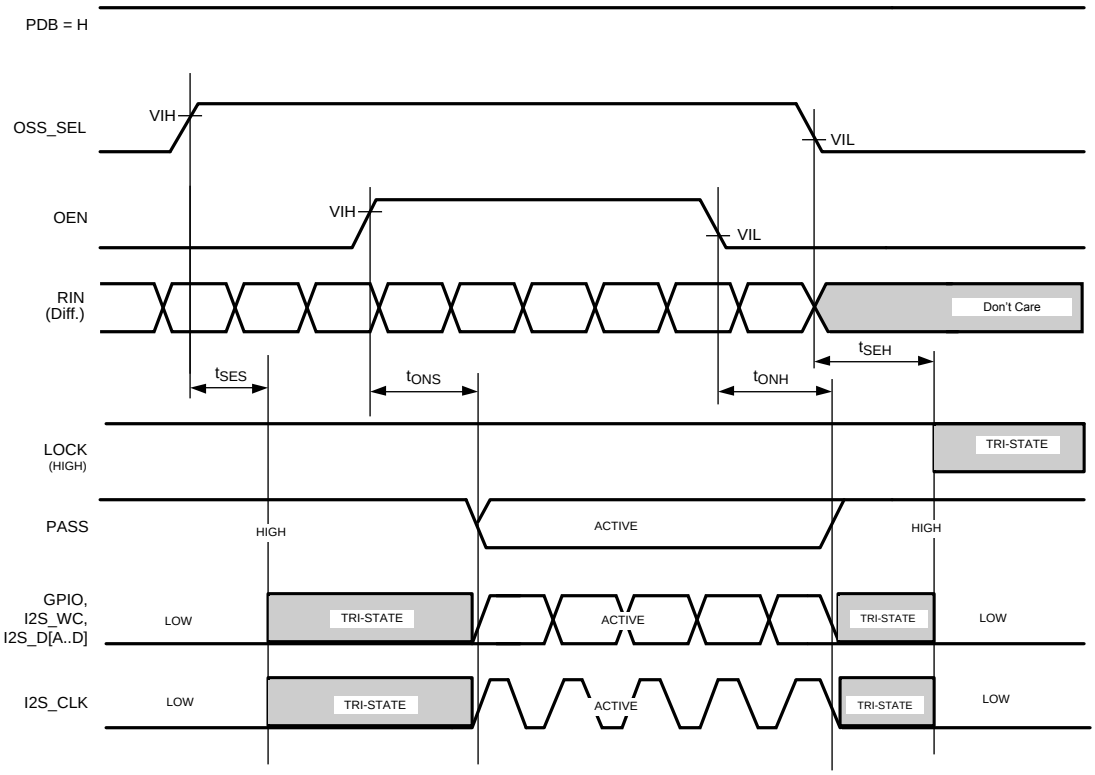


Figure 10. Output State (Setup and Hold) Times

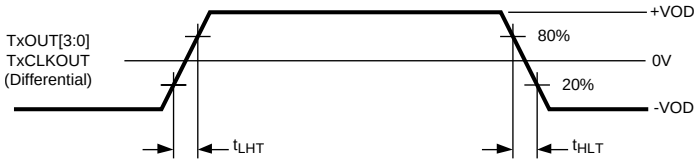


Figure 11. Input Transition Times

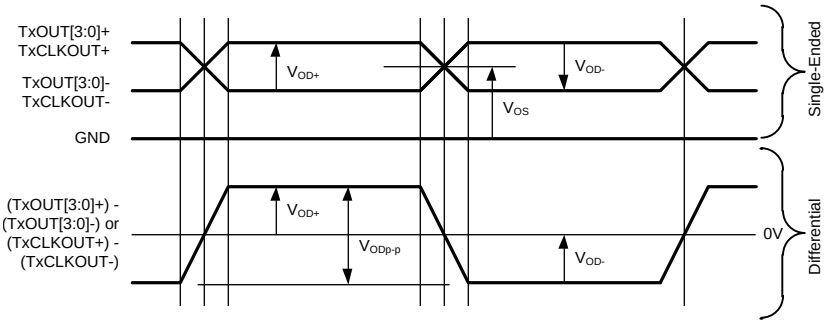


Figure 12. FPD-Link Single-Ended and Differential Waveforms

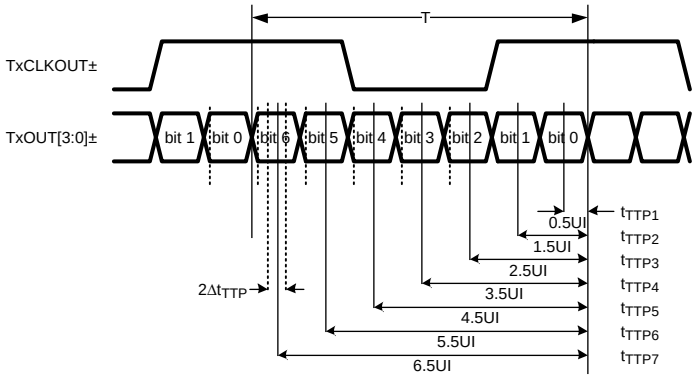
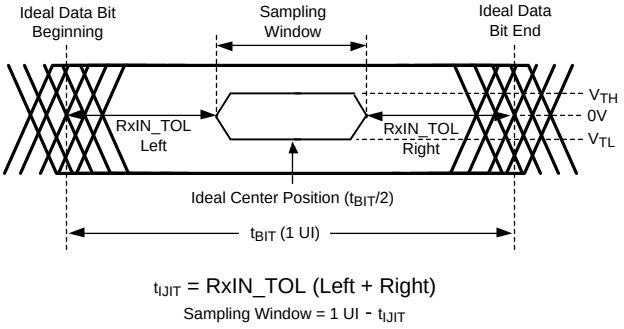


Figure 13. FPD-Link Transmitter Pulse Positions



t_{IJIT} = RxIN_TOL (Left + Right)

Sampling Window = 1 UI - t_{IJIT}

Figure 14. Receiver Input Jitter Tolerance

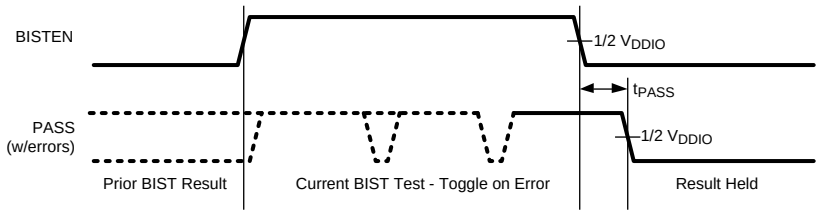


Figure 15. BIST PASS Waveform

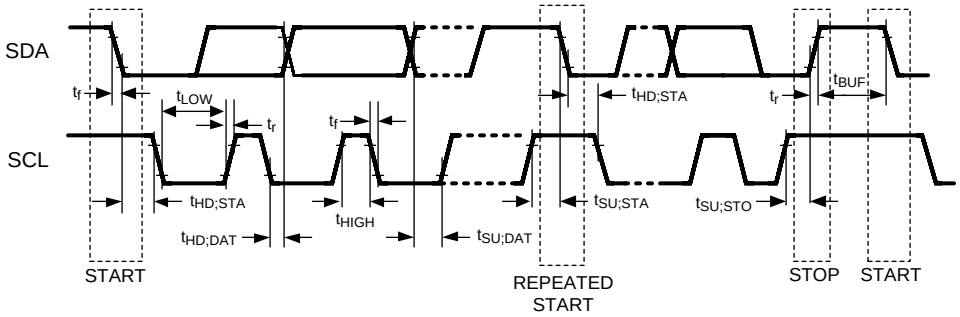


Figure 16. Serial Control Bus Timing Diagram

7.10 Typical Characteristics

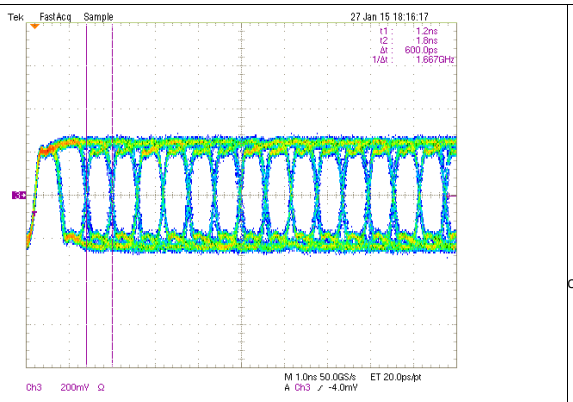


Figure 17. Serializer Output Stream with 48MHz Input Clock

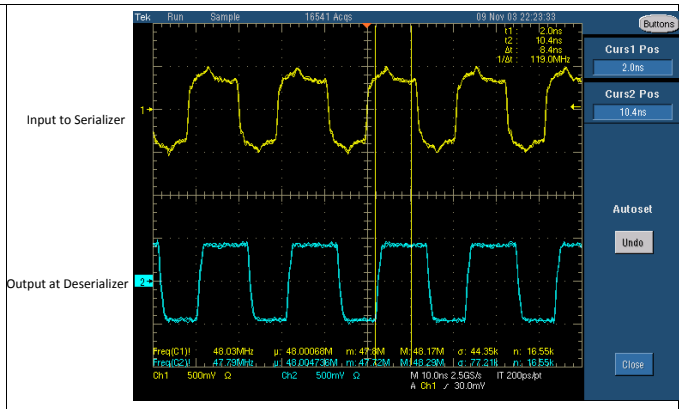


Figure 18. 48MHz Clock at Serializer and Deserializer

8 Detailed Description

8.1 Overview

The DS90UH928Q-Q1 receives a 35-bit symbol over a single serial FPD-Link III pair operating at up to 2.975 Gbps line rate and converts this stream into an FPD-Link Interface (4 LVDS data channels + 1 LVDS Clock). The FPD-Link III serial stream contains an embedded clock, video control signals, and the DC-balanced video data and audio data which enhance signal quality to support AC coupling.

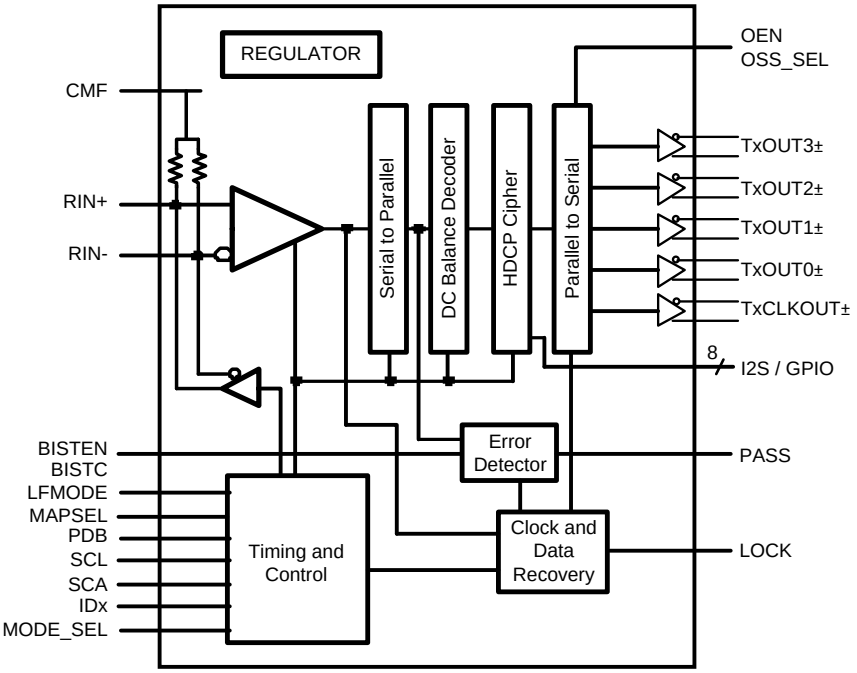
The DS90UH928Q-Q1 deserializer attains lock to a data stream without the use of a separate reference clock source, which greatly simplifies system complexity and overall cost. The deserializer also synchronizes to the serializer regardless of the data pattern, delivering true automatic “plug and lock” performance. It can lock to the incoming serial stream without the need of special training patterns or sync characters. The deserializer recovers the clock and data by extracting the embedded clock information, validating then deserializing the incoming data stream. It also applies decryption through a High-Bandwidth Digital Content Protection (HDCP) Cipher to this video and audio data stream following reception of the data from the FPD-Link III decoder. On-chip non-volatile memory stores the HDCP keys. All key exchange is done through the FPD-Link III bidirectional control interface. The decrypted FPD-Link LVDS video bus is provided to the display.

The DS90UH928Q-Q1 deserializer incorporates an I^2C compatible interface. The I^2C compatible interface allows programming of serializer or deserializer devices from a local host controller. In addition, the devices incorporate a bidirectional control channel (BCC) that allows communication between serializer/deserializer as well as remote I2C slave devices.

The bidirectional control channel (BCC) is implemented via embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I^2C transactions across the serial link from one I^2C bus to another. The implementation allows for arbitration with other I^2C compatible masters at either side of the serial link.

The DS90UH928Q-Q1 deserializer is intended for use with DS90UH925Q-Q1 or DS90UH927Q-Q1 serializers, but is also backward compatible with DS90UR905Q and DS90UR907Q FPD-Link II serializers.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 High Speed Forward Channel Data Transfer

The High Speed Forward Channel is composed of a 35-bit frame containing video data, sync signals, HDCP, I^2C, and I2S audio transmitted from serializer to deserializer. Figure 19 illustrates the serial stream PCLK cycle. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, DC-balanced and scrambled.

Figure 19. FPD-Link III Serial Stream

The device supports pixel clock ranges of 5 MHz to 15 MHz (LFMODE=1) and 15 MHz to 85 MHz (LFMODE=0). This corresponds to an application payload rate range of 155 Mbps to 2.635 Gbps, with an actual line rate range of 525 Mbps to 2.975 Gbps.

8.3.2 Low Speed Back Channel Data Transfer

The Low-Speed Back Channel of the DS90UH928Q-Q1 provides bidirectional communication between the display and host processor. The back channel control data is transferred over the single serial link along with the high-speed forward data, DC balance coding and embedded clock information. Together, the forward channel and back channel for the bidirectional control channel (BCC). This architecture provides a backward path across the serial link together with a high speed forward channel. The back channel contains the I^2C, HDCP, CRC and 4 bits of standard GPIO information with 10 Mbps line rate.

8.3.3 Backward Compatible Mode

The DS90UH928Q-Q1 is also backward compatible to the DS90UR905Q and DS90UR907Q for PCLK frequencies ranging from 15 MHz to 65 MHz. The deserializer receives 28-bits of data over a single serial FPD-Link II pair operating at a payload rate of 120 Mbps to 1.8 Gbps, corresponding to a line rate of 140 Mbps to 2.1 Gbps. The Backward Compatibility configuration can be selected through the MODE_SEL pin or programmed through the device control registers (Table 7). The bidirectional control channel, HDCP, bidirectional GPIOs, I2S, and interrupt (INTB) are not active in this mode. However, local I^2C access to the serializer is still available. Note: PCLK frequency range in this mode is 15 MHz to 65 MHz for LFMODE=0 and 5 MHZ to <15 MHz for LFMODE=1.

8.3.4 Input Equalization

An FPD-Link III input adaptive equalizer provides compensation for transmission medium losses and reduces medium-induced deterministic jitter. It equalizes up to 10m STP cables with 3 connection breaks at maximum serializer stream payload rate of 2.975 Gbps.

The adaptive equalizer may be set to a Long Cable Mode (LCBL), using the MODE_SEL pin (Table 5). This mode is typically used with longer cables where it may be desirable to start adaptive equalization from a higher default gain. In this mode, the device attempts to lock from a minimum floor AEQ value, defined by a value stored in the control registers (Table 7).

8.3.5 Common Mode Filter Pin (CMF)

The deserializer provides access to the center tap of the internal CML termination. A 0.1-µF capacitor must be connected from this pin to GND for additional common-mode filtering of the differential pair (Figure 39). This increases noise rejection capability in high-noise environments.

Feature Description (continued)

8.3.6 Power Down (PDB)

The deserializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin may be controlled by an external device, or through V_{DDIO}, where V_{DDIO} = 3.0 V to 3.6 V or V_{DD33}. To save power, disable the link when the display is not needed (PDB = LOW). Ensure that this pin is not driven HIGH before V_{DD33} and V_{DDIO} have reached final levels. When PDB is driven low, ensure that the pin is driven to 0 V for at least 1.5 ms before releasing or driving high (See *Recommended Operating Conditions*). In the case where PDB is pulled up to V_{DDIO} = 3.0 V to 3.6 V or V_{DD33} directly, a 10-kΩ pullup resistor and a >10-µF capacitor to ground are required (See Figure 39).

Toggling PDB low will POWER DOWN the device and RESET all control registers to default. During this time, PDB must be held low for a minimum of 2 ms (See *AC Electrical Characteristics*).

8.3.7 Video Control Signals

The video control signal bits embedded in the high-speed FPD-Link LVDS are subject to certain limitations relative to the video pixel clock period (PCLK). By default, the device applies a minimum pulse width filter on these signals to help eliminate spurious transitions.

Normal Mode Control Signals (VS, HS, DE) have the following restrictions:

- Horizontal Sync (HS): The video control signal pulse width must be 3 PCLKs or longer when the Control Signal Filter (register bit 0x03[4]) is enabled (default). Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). See Table 7. HS can have at most two transitions per 130 PCLKs.
- Vertical Sync (VS): The video control signal pulse is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.
- Data Enable Input (DE): The video control signal pulse width must be 3 PCLKs or longer when the Control Signal Filter (register bit 0x03[4]) is enabled (default). Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). See Table 7. DE can have at most two transitions per 130 PCLKs.

8.3.8 EMI Reduction Features

8.3.8.1 LVCMOS VDDIO Option

The 1.8 V/3.3 V LVCMOS inputs and outputs are powered from a separate VDDIO supply pin to offer compatibility with external system interface signals. Note: When configuring the V_{DDIO} power supplies, all the single-ended control input pins (except PDB) for device need to scale together with the same operating V_{DDIO} levels. If V_{DDIO} is selected to operate in the 3.0 V to 3.6 V range, V_{DDIO} must be operated within 300 mV of V_{DD33} (See *Recommended Operating Conditions*).

8.3.9 Built In Self Test (BIST)

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high speed serial link and the low-speed back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

8.3.9.1 BIST Configuration and Status

The BIST mode is enabled at the deserializer by pin (BISTEN) or BIST configuration register. The test may select either an external PCLK or the 33 MHz internal Oscillator clock (OSC) frequency. In the absence of PCLK, the user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received containing one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

Feature Description (continued)

The BIST status can be monitored real time on the deserializer PASS pin, with each detected error resulting in a half pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK status is valid throughout the entire duration of BIST.

See Figure 20 for the BIST mode flow diagram.

8.3.9.1.1 Sample BIST Sequence

1. BIST Mode is enabled via the BISTEN pin of Deserializer. The desired clock source is selected through the deserializer BISTC pin.
2. The serializer is awakened through the back channel if it is not already on. An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires LOCK, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.
3. To Stop BIST mode, set the BISTEN pin LOW. The deserializer stops checking the data, and the final test result is held on the PASS pin. If the test ran error free, the PASS output will remain HIGH. If there one or more errors were detected, the PASS output will output constant LOW. The PASS output state is held until a new BIST is run, the device is RESET, or the device is powered down. BIST duration is user-controlled and may be of any length.

The link returns to normal operation after the deserializer BISTEN pin is low. Figure 21 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect medium, or reducing signal condition enhancements (Rx Equalization).

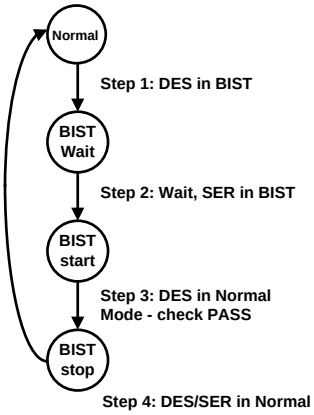


Figure 20. BIST Mode Flow Diagram

8.3.9.2 Forward Channel and Back Channel Error Checking

The deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer. Forward channel errors may also be read from register 0x25 (Table 7).

The back-channel data is checked for CRC errors once the serializer locks onto the back-channel serial stream, as indicated by link detect status (register bit 0x0C[0] - Table 7). CRC errors are recorded in an 8-bit register in the deserializer. The register is cleared when the serializer enters the BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps the record of the last BIST run until cleared or the serializer enters BIST mode again.

Feature Description (continued)

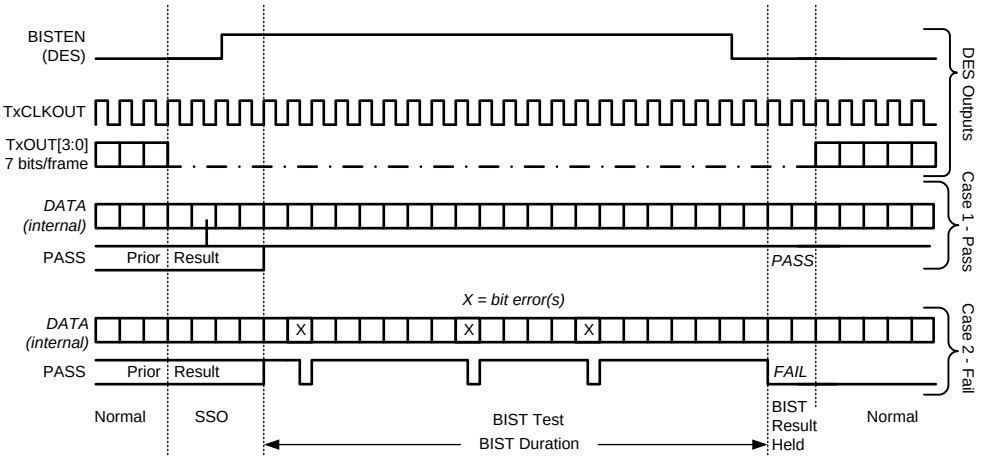


Figure 21. BIST Waveforms

8.3.10 Internal Pattern Generation

The DS90UH928Q-Q1 deserializer features an internal pattern generator. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no input is applied. If no clock is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to TI Application Note: ( ).

8.3.10.1 Pattern Options

The DS90UH928Q-Q1 deserializer pattern generator is capable of generating 17 default patterns for use in basic testing and debugging of panels. Each pattern can be inverted using register bits (see Table 7). The 17 default patterns are listed as follows:

1. White/Black (default/inverted)
2. Black/White
3. Red/Cyan
4. Green/Magenta
5. Blue/Yellow
6. Horizontally Scaled Black to White/White to Black
7. Horizontally Scaled Black to Red/Cyan to White
8. Horizontally Scaled Black to Green/Magenta to White
9. Horizontally Scaled Black to Blue/Yellow to White
10. Vertically Scaled Black to White/White to Black
11. Vertically Scaled Black to Red/Cyan to White
12. Vertically Scaled Black to Green/Magenta to White
13. Vertically Scaled Black to Blue/Yellow to White
14. Custom Color / Inverted configured in PGRS
15. Black-White/White-Black Checkerboard (or custom checkerboard color, configured in PGCTL)
16. YCBR/RBCY VCOM pattern, orientation is configurable from PGCTL
17. Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) – Note: not included in the auto-scrolling feature

Feature Description (continued)

8.3.10.2 Color Modes

By default, the Pattern Generator operates in 24-bit color mode, where all bits of the Red, Green, and Blue outputs are enabled. 18-bit color mode can be activated from the configuration registers (Table 7). In 18-bit mode, the 6 most significant bits (bits 7-2) of the Red, Green, and Blue outputs are enabled; the 2 least significant bits will be 0.

8.3.10.3 Video Timing Modes

The Pattern Generator has two video timing modes – external and internal. In external timing mode, the Pattern Generator detects the video frame timing present on the DE and VS inputs. If Vertical Sync signaling is not present on VS, the Pattern Generator determines Vertical Blank by detecting when the number of inactive pixel clocks (DE = 0) exceeds twice the detected active line length. In internal timing mode, the Pattern Generator uses custom video timing as configured in the control registers. The internal timing generation may also be driven by an external clock. By default, external timing mode is enabled. Internal timing or Internal timing with External Clock are enabled by the control registers (Table 7). If internal clock generation is used, register 0x39 bit 1 must be set.

8.3.10.4 External Timing

In external timing mode, the Pattern Generator passes the incoming DE, HS, and VS signals unmodified to the video control outputs after a two pixel clock delay. It extracts the active frame dimensions from the incoming signals in order to properly scale the brightness patterns. If the incoming video stream does not use the VS signal, the Pattern Generator determines the Vertical Blank time by detecting a long period of pixel clocks without DE asserted.

8.3.10.5 Pattern Inversion

The Pattern Generator also incorporates a global inversion control, located in the PGCFG register, which causes the output pattern to be bitwise-inverted. For example, the full screen Red pattern becomes full-screen cyan, and the Vertically Scaled Black to Green pattern becomes Vertically Scaled White to Magenta.

8.3.10.6 Auto Scrolling

The Pattern Generator supports an Auto-Scrolling mode, in which the output pattern cycles through a list of enabled pattern types. A sequence of up to 16 patterns may be defined in the registers. The patterns may appear in any order in the sequence and may also appear more than once.

8.3.10.7 Additional Features

Additional pattern generator features can be accessed through the Pattern Generator Indirect Register Map. It consists of the Pattern Generator Indirect Address (PGIA — Table 7) and the Pattern Generator Indirect Data (PGID — Table 7).

8.3.11 Image Enhancement Features

Several image enhancement features are provided. The White Balance LUTs allow the user to define and map the color profile of the display. Adaptive Hi-FRC Dithering enables the presentation of 'true color' images on an 18-bit display.

8.3.11.1 White Balance

The White Balance feature enables similar display appearance when using LCD's from different vendors. It compensates for native color temperature of the display, and adjusts relative intensities of R, G, and B to maintain specified color temperature. Programmable control registers are used to define the contents of three LUTs (8-bit color value for Red, Green and Blue) for the White Balance Feature. The LUTs map input RGB values to new output RGB values. There are three LUTs, one LUT for each color. Each LUT contains 256 entries, 8-bits per entry with a total size of 6144 bits (3 x 256 x 8). All entries are readable and writable. Calibrated values are loaded into registers through the I2C interface (deserializer is a slave device). This feature may also be applied to lower color depth applications such as 18–bit (666) and 16–bit (565). White balance is enabled and configured via serial control bus register.

Feature Description (continued)

8.3.11.1.1 LUT Contents

The user must define and load the contents of the LUT for each color (R,G,B). Regardless of the color depth being driven (888, 666, 656), the user must always provide contents for 3 complete LUTs - 256 colors x 8 bits x 3 tables. Unused bits - LSBs -shall be set to “0” by the user.

When 24-bit (888) input data is being driven to a 24-bit display, each LUT (R, G and B) must contain 256 unique 8-bit entries. The 8-bit white balanced data is then available at the output of the deserializer, and driven to the display.

The user must define and load the contents of the LUT for each color (R,G,B). Regardless of the color depth being driven (888, 666, 656), the user must always provide contents for 3 complete LUTs - 256 colors x 8 bits x 3 tables. Unused bits - LSBs -shall be set to “0” by the user. When 24-bit (888) input data is being driven to a 24-bit display, each LUT (R, G and B) must contain 256 unique 8-bit entries. The 8-bit white balanced data is then available at the output of the deserializer, and driven to the display.

Alternatively, with 6-bit input data the user may choose to load complete 8-bit values into each LUT. This mode of operation provides the user with finer resolution at the LUT output to more closely achieve the desired white point of the calibrated display. Although 8-bit data is loaded, only 64 unique 8-bit white balance output values are available for each color (R, G and B). The result is 8-bit white balanced data. Before driving to the output of the deserializer, the 8-bit data must be reduced to 6-bit with an FRC dithering function. To operate in this mode, the user must configure the deserializer to enable the FRC2 function.

Examples of the three types of LUT configurations described are shown in Figure 22.

8.3.11.1.2 Enabling White Balance

The user must load all 3 LUTs prior to enabling the white balance feature. The following sequence must be followed by the user.

To initialize white balance after power-on:

1. Load contents of all 3 LUTs . This requires a sequential loading of LUTs - first RED, second GREEN, third BLUE. 256, 8-bit entries must be loaded to each LUT. Page registers must be set to select each LUT.
2. Enable white balance. By default, the LUT data may not be reloaded after initialization at power-on.

An option does exist to allow LUT reloading after power-on and initial LUT loading (as described above). This option may only be used after enabling the white balance reload feature via the associated serial control bus register. In this mode the LUTs may be reloaded by the master controller via I2C. This provides the user with the flexibility to refresh LUTs periodically , or upon system requirements to change to a new set of LUT values. The host controller loads the updated LUT values via the serial bus interface. There is no need to disable the white balance feature while reloading the LUT data. Refreshing the white balance to the new set of LUT data will be seamless - no interruption of displayed data.

It is important to note that initial loading of LUT values requires that all 3 LUTs be loaded sequentially. When reloading, partial LUT updates may be made.

Feature Description (continued)

8-bit in / 8 bit out

Gray level Entry	Data Out (8-bits)
0	00000000b
1	00000001b
2	00000011b
3	00000011b
4	00000110b
5	00000110b
6	00000111b
7	00000111b
8	00001000b
9	00001010b
10	00001001b
11	00001011b
⋮	⋮
248	11111010b
249	11111010b
250	11111011b
251	11111011b
252	11111110b
253	11111101b
254	11111101b
255	11111111b

6-bit in / 6 bit out

Gray level Entry	Data Out (8-bits)
0	00000**00**b
1	N/A
2	N/A
3	N/A
4	00000**00**b
5	N/A
6	N/A
7	N/A
8	00001**00**b
9	N/A
10	N/A
11	N/A
⋮	⋮
248	11111**00**b
249	N/A
250	N/A
251	N/A
252	11111**00**b
253	N/A
254	N/A
255	N/A

6-bit in / 8 bit out

Gray level Entry	Data Out (8-bits)
0	00000001b
1	N/A
2	N/A
3	N/A
4	00000110b
5	N/A
6	N/A
7	N/A
8	00001011b
9	N/A
10	N/A
11	N/A
⋮	⋮
248	11111010b
249	N/A
250	N/A
251	N/A
252	11111111b
253	N/A
254	N/A
255	N/A

Figure 22. White Balance LUT Configuration

8.3.11.2 Adaptive Hi-FRC Dithering

The Adaptive FRC Dithering Feature delivers product-differentiating image quality. It reduces 24-bit RGB (8 bits per sub-pixel) to 18-bit RGB (6 bits per sub-pixel), smoothing color gradients, and allowing the flexibility to use lower cost 18-bit displays. FRC (Frame Rate Control) dithering is a method to emulate “missing” colors on a lower color depth LCD display by changing the pixel color slightly with every frame. FRC is achieved by controlling on and off pixels over multiple frames (Temporal). Static dithering regulates the number of on and off pixels in a small defined pixel group (Spatial). The FRC module includes both Temporal and Spatial methods and also Hi-FRC. Conventional FRC can display only 16,194,277 colors with 6-bit RGB source. “Hi-FRC” enables full (16,777,216) color on an 18-bit LCD panel. The “adaptive” FRC module also includes input pixel detection to apply specific Spatial dithering methods for smoother gray level transitions. When enabled, the lower LSBs of each RGB output are not active; only 18 bit data (6 bits per R,G and B) are driven to the display. This feature is enabled via serial control bus register. Two FRC functional blocks are available, and may be independently enabled. FRC1 precedes the white balance LUT, and is intended to be used when 24-bit data is being driven to an 18-bit display with a white balance LUT that is calibrated for an 18-bit data source. The second FRC block, RC2, follows the white balance block and is intended to be used when fine adjustment of color temperature is required on an 18-bit color display, or when a 24-bit source drives an 18-bit display with a white balance LUT calibrated for 24-bit source data.

For proper operation of the FRC dithering feature, the user must provide a description of the display timing control signals. The timing mode, “sync mode” (HS, VS) or “DE only” must be specified, along with the active polarity of the timing control signals. All this information is entered to device control registers via the serial bus interface.

Adaptive Hi-FRC dithering consists of several components. Initially, the incoming 8-bit data is expanded to 9-bit data. This allows the effective dithered result to support a total of 16.7 million colors. The incoming 9-bit data is evaluated, and one of four possible algorithms is selected. The majority of incoming data sequences are supported by the default dithering algorithm. Certain incoming data patterns (black/white pixel, full on/off sub-pixel) require special algorithms designed to eliminate visual artifacts associated with these specific gray level transitions. Three algorithms are defined to support these critical transitions.

An example of the default dithering algorithm is illustrated in Figure 23. The 1 or 0 value shown in the table describes whether the 6-bit value is increased by 1 (“1”) or left unchanged (“0”). In this case, the 3 truncated LSBs are “001”.

Feature Description (continued)

F0L0	Frame = 0, Line = 0
PD1	Pixel Data one
Cell Value 010	R[7:2]+0, G[7:2]+1, B[7:2]+0
LSB=001	three lsb of 9 bit data (8 to 9 for Hi-Frc)

Pixel Index	PD1	PD2	PD3	PD4	PD5	PD6	PD7	PD8	
LSB = 001									
F0L0	010	000	000	000	000	000	010	000	R = 4/32 G = 4/32 B = 4/32
F0L1	101	000	000	000	101	000	000	000	
F0L2	000	000	010	000	010	000	000	000	
F0L3	000	000	101	000	000	000	101	000	
F1L0	000	000	000	000	000	000	000	000	R = 4/32 G = 4/32 B = 4/32
F1L1	000	111	000	000	000	111	000	000	
F1L2	000	000	000	000	000	000	000	000	
F1L3	000	000	000	111	000	000	000	111	
F2L0	000	000	010	000	010	000	000	000	R = 4/32 G = 4/32 B = 4/32
F2L1	000	000	101	000	000	000	101	000	
F2L2	010	000	000	000	000	000	010	000	
F2L3	101	000	000	000	101	000	000	000	
F3L0	000	000	000	000	000	000	000	000	R = 4/32 G = 4/32 B = 4/32
F3L1	000	000	000	111	000	000	000	111	
F3L2	000	000	000	000	000	000	000	000	
F3L3	000	111	000	000	000	111	000	000	

Figure 23. Default FRC Algorithm

8.3.12 Serial Link Fault Detect

The DS90UH928Q-Q1 can detect fault conditions in the FPD-Link III interconnect. If a fault condition occurs, the Link Detect Status is 0 (cable is not detected) on bit 0 of address 0x0C (Table 7). The device will detect any of the following conditions:

1. Cable open
2. RIN+ to - short
3. RIN+ to GND short
4. RIN- to GND short
5. RIN+ to battery short
6. RIN- to battery short
7. Cable is linked incorrectly (RIN+/RIN- connections reversed)

NOTE

The device will detect any of the above conditions, but does not report specifically which one has occurred.

8.3.13 Oscillator Output

The deserializer provides an optional TxCLKOUT± output when the input clock (serial stream) has been lost. This is based on an internal oscillator and may be controlled from register 0x02, bit 5 (OSC Clock Output Enable) Table 7.

8.3.14 Interrupt Pin (INTB)

1. On the serializer, set register (HDCP_ICR) 0xC6[5] = 1 and 0xC6[0] = 1 (Table 7) to configure the interrupt.
2. On the serializer, read from HDCP_ISR register 0xC7 to arm the interrupt for the first time.

Feature Description (continued)

3. When INTB_IN is set LOW, the INTB pin on the serializer also pulls low, indicating an interrupt condition.
4. The external controller detects INTB = LOW and reads the HDCP_ISR register (Table 7) to determine the interrupt source. Reading this register also clears and resets the interrupt.

8.3.15 General-Purpose I/O

8.3.15.1 GPIO[3:0]

In normal operation, GPIO[3:0] may be used as general purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO modes may be configured from the registers (Table 7). GPIO[1:0] are dedicated pins and GPIO[3:2] are shared with I2S_DC and I2S_DD respectively. Note: if the DS90UH928Q-Q1 is paired with a DS90UH925Q-Q1 serializer, the devices must be configured into 18-bit mode to allow usage of GPIO pins on the serializer. To enable 18-bit mode, set serializer register 0x12[2] = 1. 18-bit mode will be auto-loaded into the deserializer from the serializer. See Table 1 for GPIO enable and configuration.

Table 1. GPIO Enable and Configuration

DESCRIPTION	DEVICE	FORWARD CHANNEL	BACK CHANNEL
GPIO3	DS90UH925Q-Q1/DS90UH927Q-Q1	0x0F = 0x03	0x0F = 0x05
	DS90UH928Q-Q1	0x1F = 0x05	0x1F = 0x03
GPIO2	DS90UH925Q-Q1/DS90UH927Q-Q1	0x0E = 0x30	0x0E = 0x50
	DS90UH928Q-Q1	0x1E = 0x50	0x1E = 0x30
GPIO1	DS90UH925Q-Q1/DS90UH927Q-Q1	0x0E = 0x03	0x0E = 0x05
	DS90UH928Q-Q1	0x1E = 0x05	0x1E = 0x03
GPIO0	DS90UH925Q-Q1/DS90UH927Q-Q1	0x0D = 0x03	0x0D = 0x05
	DS90UH928Q-Q1	0x1D = 0x05	0x1D = 0x03

The input value present on GPIO[3:0] may also be read from register, or configured to local output mode (Table 7).

8.3.15.2 GPIO[8:5]

GPIO_REG[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I2S pins and will override I2S input if enabled into GPIO_REG mode. See Table 2 for GPIO enable and configuration.

Note: Local GPIO value may be configured and read either through local register access, or remote register access through the Low-Speed Bidirectional Control Channel. Configuration and state of these pins are not transported from serializer to deserializer as is the case for GPIO[3:0].

Table 2. GPIO_REG and GPIO Local Enable and Configuration

DESCRIPTION	REGISTER CONFIGURATION	FUNCTION
GPIO_REG8	0x21 = 0x01	Output, L
	0x21 = 0x09	Output, H
	0x21 = 0x03	Input, Read: 0x6F[0]
GPIO_REG7	0x21 = 0x01	Output, L
	0x21 = 0x09	Output, H
	0x21 = 0x03	Input, Read: 0x6E[7]
GPIO_REG6	0x20 = 0x01	Output, L
	0x20 = 0x09	Output, H
	0x20 = 0x03	Input, Read: 0x6E[6]

Table 2. GPIO_REG and GPIO Local Enable and Configuration (continued)

DESCRIPTION	REGISTER CONFIGURATION	FUNCTION
GPIO_REG5	0x20 = 0x01	Output, L
	0x20 = 0x09	Output, H
	0x20 = 0x03	Input, Read: 0x6E[5]
GPIO3	0x1F = 0x01	Output, L
	0x1F = 0x09	Output, H
	0x1F = 0x03	Input, Read: 0x6E[3]
GPIO2	0x1E = 0x01	Output, L
	0x1E = 0x09	Output, H
	0x1E = 0x03	Input, Read: 0x6E[2]
GPIO1	0x1E = 0x01	Output, L
	0x1E = 0x09	Output, H
	0x1E = 0x03	Input, Read: 0x6E[1]
GPIO0	0x1D = 0x01	Output, L
	0x1D = 0x09	Output, H
	0x1D = 0x03	Input, Read: 0x6E[0]

8.3.16 I^2S Audio Interface

The DS90UH928Q-Q1 deserializer features six I2S output pins that, when paired with a DS90UH927Q-Q1serializer, supports surround sound audio applications. The bit clock (I2S_CLK) supports frequencies between 1 MHz and the smaller of <PCLK/2 or <13 MHz. Four I2S data outputs carry two channels of I2S-formatted digital audio each, with each channel delineated by the word select (I2C_WC) input. The I^2S audio interface is not available in Backwards Compatibility Mode (BKWD = 1).

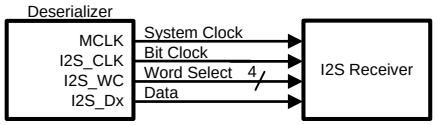


Figure 24. I2S Connection Diagram

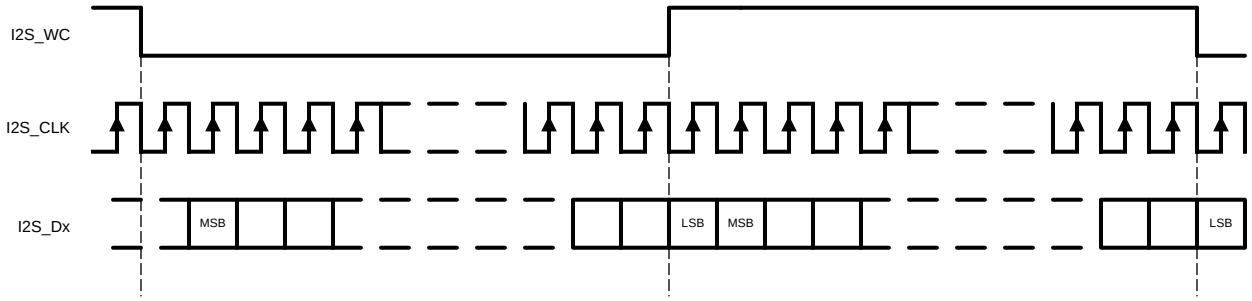


Figure 25. I2S Frame Timing Diagram

When paired with a DS90UH925Q-Q1, the DS90UH928Q-Q1 I2S interface supports a single I2S data output through I2S_DA (24-bit video mode), or two I2S data outputs through I2S_DA and I2S_DB (18-bit video mode).

8.3.16.1 I2S Transport Modes

By default, packetized audio is received during video blanking periods in dedicated Data Island Transport frames. The transport mode is set in the serializer and auto-loaded into the deserializer by default. The audio configuration may be disabled from control registers if Forward Channel Frame Transport of I2S data is desired. In frame transport, only I2S_DA is received to the DS90UH928Q-Q1 deserializer. Surround Sound Mode, which transmits all four I2S data inputs (I2S_D[D:A]), may only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UH927Q-Q1 serializer. If connected to a DS90UH925Q-Q1serializer, only I2S_DA and I2S_DB may be received.

8.3.16.2 I2S Repeater

I2S audio may be fanned-out and propagated in the repeater application. By default, data is propagated via Data Island Transport on the FPD-Link interface during the video blanking periods. If frame transport is desired, then the I2S pins should be connected from the deserializer to all serializers. Activating surround sound at the top-level serializer automatically configures downstream serializers and deserializers for surround sound transport utilizing Data Island Transport. If 4-channel operation utilizing I2S_DA and I2S_DB only is desired, this mode must be explicitly set in each serializer and deserializer control register throughout the repeater tree (Table 7).

A DS90UH928Q-Q1 deserializer configured in repeater mode may also regenerate I2S audio from its I2S input pins in lieu of Data Island frames. See the HDCP Repeater Connection Diagram (Figure 31) and the I2C Control Registers (Table 7) for additional details.

8.3.16.3 I2S Jitter Cleaning

The DS90UH928Q-Q1 features a standalone PLL to clean the I2S data jitter, supporting high-end car audio systems. If I2S_CLK frequency is less than 1MHz, this feature must be disabled through register 0x2B[7]. See Table 7.

8.3.16.4 MCLK

The deserializer has an I2S Master Clock Output (MCLK). It supports x1, x2, or x4 of I2S CLK Frequency. When the I2S PLL is disabled, the MCLK output is off. Table 3 covers the range of I2S sample rates and MCLK frequencies. By default, all the MCLK output frequencies are x2 of the I2S CLK frequencies. The MCLK frequencies can also be enabled through the register bits 0x3A[6:4] (I2S DIVSEL), shown in Table 7. To select desired MCLK frequency, write 0x3A[7], then write to bit [6:4] accordingly.

Table 3. Audio Interface Frequencies

SAMPLE RATE (kHz)	I2S DATA WORD SIZE (BITS)	I2S_CLK (MHz)	MCLK OUTPUT (MHz)	REGISTER 0x3A[6:4]'b
32	16	1.024	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
44.1		1.4112	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
48		1.536	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
96		3.072	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
192		6.144	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100

Table 3. Audio Interface Frequencies (continued)

SAMPLE RATE (kHz)	I2S DATA WORD SIZE (BITS)	I2S_CLK (MHz)	MCLK OUTPUT (MHz)	REGISTER 0x3A[6:4]'b
32	24	1.536	I2S_CLK x1	000
			I2S_CLK x2	001
			I2S_CLK x4	010
44.1		2.117	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
48		2.304	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
96		4.608	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
192		9.216	I2S_CLK x1	011
			I2S_CLK x2	100
			I2S_CLK x4	101
32	32	2.048	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
44.1		2.8224	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
48		3.072	I2S_CLK x1	001
			I2S_CLK x2	010
			I2S_CLK x4	011
96		6.144	I2S_CLK x1	010
			I2S_CLK x2	011
			I2S_CLK x4	100
192		12.288	I2S_CLK x1	011
			I2S_CLK x2	100
			I2S_CLK x4	110

8.4 Device Functional Modes

8.4.1 Clock and Output Status

When PDB is driven HIGH, the CDR PLL begins locking to the serial input and LOCK is TRI-STATE or LOW (depending on the value of the OEN setting). After the deserializer completes its lock sequence to the input serial data, the LOCK output is driven HIGH, indicating valid data and clock recovered from the serial input is available on the LVCMOS and LVDS outputs. The State of the outputs is based on the OEN and OSS_SEL setting (Table 4) or register bit (Table 7).

Table 4. Output State Table

INPUTS				OUTPUTS			
SERIAL INPUT	PDB	OEN	OSS_SEL	LOCK	PASS	DATA/GPIO/I2S	TxCLKOUT/TxOUT[3:0]
X	L	X	X	Z	Z	Z	Z
X	H	L	L	L or H	L	L	L
X	H	L	H	L or H	Z	Z	Z

Device Functional Modes (continued)

Table 4. Output State Table (continued)

INPUTS				OUTPUTS			
Static	H	H	L	L	L	L	L/OSC (Register EN)
Static	H	H	H	L	Previous Status	L	L
Active	H	H	L	L	L	L	L
Active	H	H	H	H	Valid	Valid	Valid

8.4.2 FPD-Link Input Frame and Color Bit Mapping Select

The DS90UH928Q-Q1 can be configured to output 24-bit color (RGB888) or 18-bit color (RGB666) with 2 different mapping schemes, shown in Figure 26, or MSBs on TxOUT[3], shown in Figure 27. Each frame corresponds to a single pixel clock (PCLK) cycle. The LVDS clock output from TxCLKOUT± follows a 4:3 duty cycle scheme, with each 28-bit pixel frame starting with two LVDS bit clock periods high, three low, and ending with two high. The mapping scheme is controlled by MAPSEL pin or by Register (Table 7).

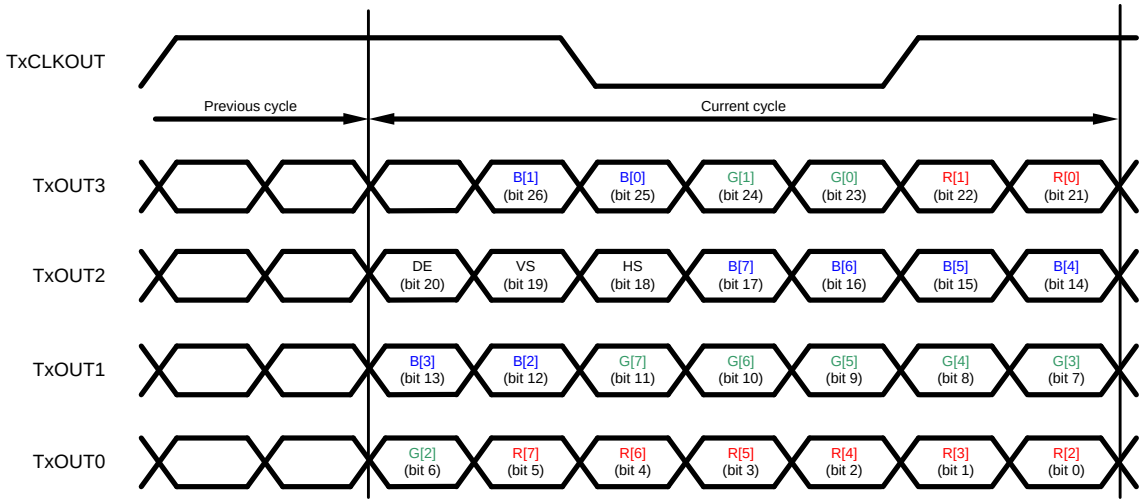


Figure 26. 24-bit Color FPD-Link Mapping: LSBs on TxOUT3 (MAPSEL=L)

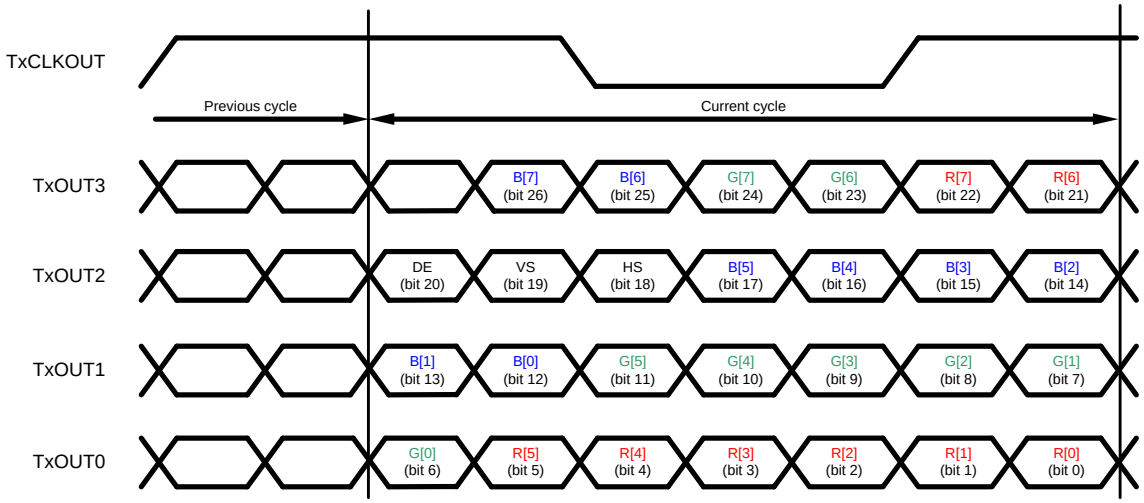


Figure 27. 24-bit ColorFPD-Link Mapping: MSBs on TxOUT3 (MAPSEL=H)

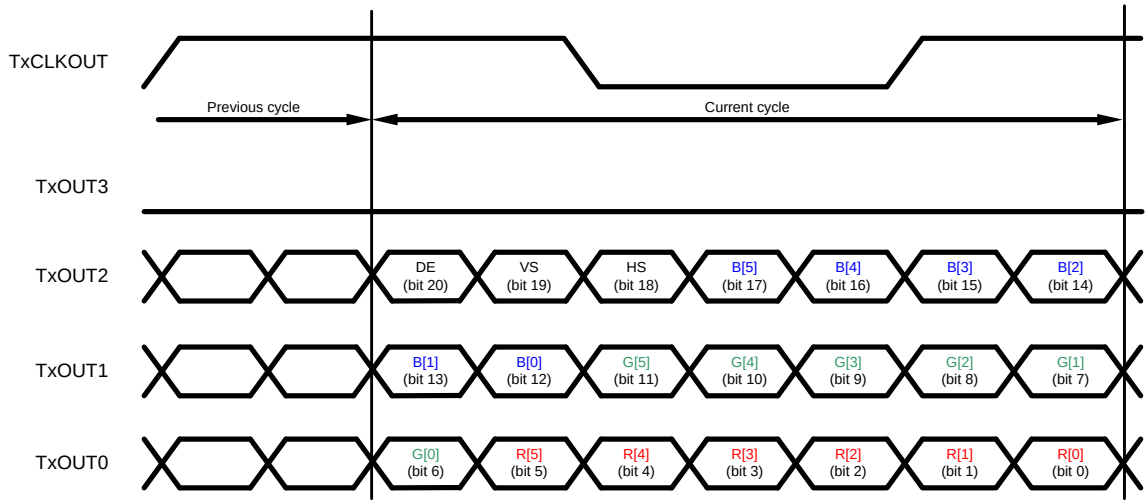


Figure 28. 18-bit Color FPD-Link Mapping (MAPSEL = L)

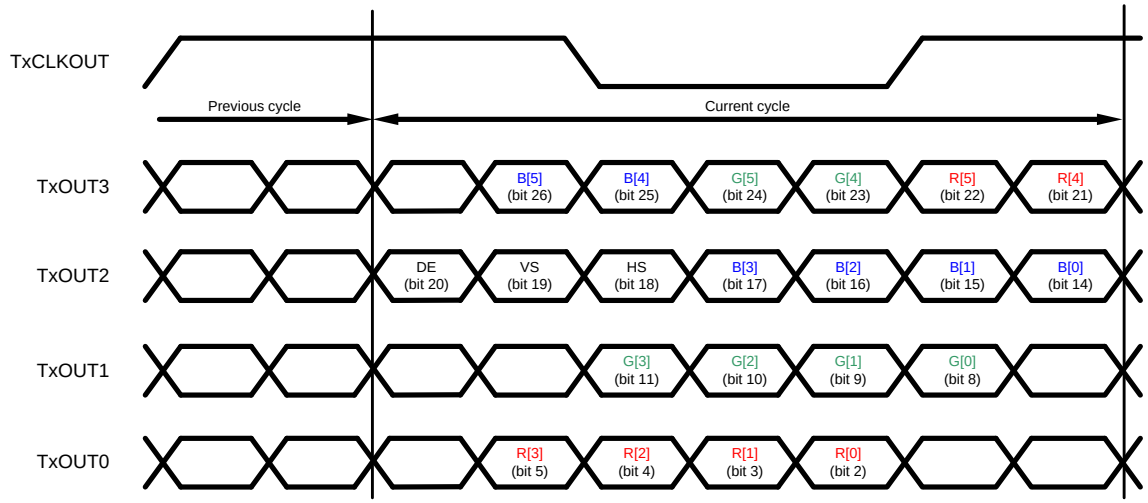


Figure 29. 18-bit Color FPD-Link Mapping (MAPSEL = H)

8.4.3 Low Frequency Optimization (LFMODE)

The LFMODE is set via register (Table 7) or by the LFMODE Pin. This mode optimizes device operation for lower input data clock ranges supported by the serializer. If LFMODE is Low (LFMODE=0, default), the TxCLKOUT± PCLK frequency is between 15 MHz and 85 MHz. If LFMODE is High (LFMODE=1), the TxCLKOUT± frequency is between 5 MHz and <15 MHz. Note: when the device LFMODE is changed, a PDB reset is required. When LFMODE is high (LFMODE=1), the line rate relative to the input data rate is multiplied by four. Thus, for the operating range of 5 MHz to <15 MHz, the line rate is 700 Mbps to <2.1 Gbps with an effective data payload of 175 Mbps to 525 Mbps. Note: for Backwards Compatibility Mode (BKWD=1), the line rate relative to the input data rate remains the same.

8.4.4 Mode Select (MODE_SEL)

Device configuration may be done via the MODE_SEL pin or via register (Table 7). A pullup resistor and a pulldown resistor of suggested values may be used to set the voltage ratio of the MODE_SEL input (VR4) and V_{DD33} to select one of the 9 possible selected modes. See Figure 30 and Table 5.

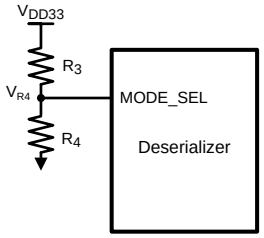


Figure 30. MODE_SEL Connection Diagram

Table 5. Configuration Select (MODE_SEL)

NO.	Ideal Ratio (V_{R4}/V_{DD33})	Ideal V_{R4} (V)	Suggested Resistor R_3 (kΩ, 1% tol)	Suggested Resistor R_4 (kΩ, 1% tol)	REPEAT	BKWD	I2S_B	LCBL
1	0	0	OPEN	40.2	L	L	L	L
2	0.120	0.397	294	40.2	L	L	H	L
3	0.164	0.540	255	49.9	H	L	L	L
4	0.223	0.737	267	76.8	H	L	H	L
5	0.286	0.943	255	102	L	L	L	H
6	0.365	1.205	226	130	L	L	H	H
7	0.446	1.472	205	165	H	L	L	H
8	0.541	1.786	162	191	H	L	H	H
9	0.629	2.075	124	210	L	H	L	L

8.4.5 Repeater Connections

The HDCP Repeater requires the following connections between the HDCP Receiver and each HDCP Transmitter Figure 31.

1. Video Data – Connect all FPD-Link data and clock pairs
2. I2C – Connect SCL and SDA signals. Both signals should be pulled up to V_{DD33} or V_{DDIO} = 3.0 V to 3.6 V with 4.7-kΩ resistors.
3. Audio (optional) – Connect I2S_CLK, I2S_WC, and I2S_Dx signals.
4. IDx pin – Each Transmitter and Receiver must have an unique I2C address.
5. REPEAT & MODE_SEL pins — All Transmitters and Receivers must be set into Repeater Mode.
6. Interrupt pin – Connect DS90UH928Q-Q1 INTB_IN pin to the DS90UH927Q-Q1 INTB pin. The signal must be pulled up to V_{DDIO} with a 10-kΩ resistor.

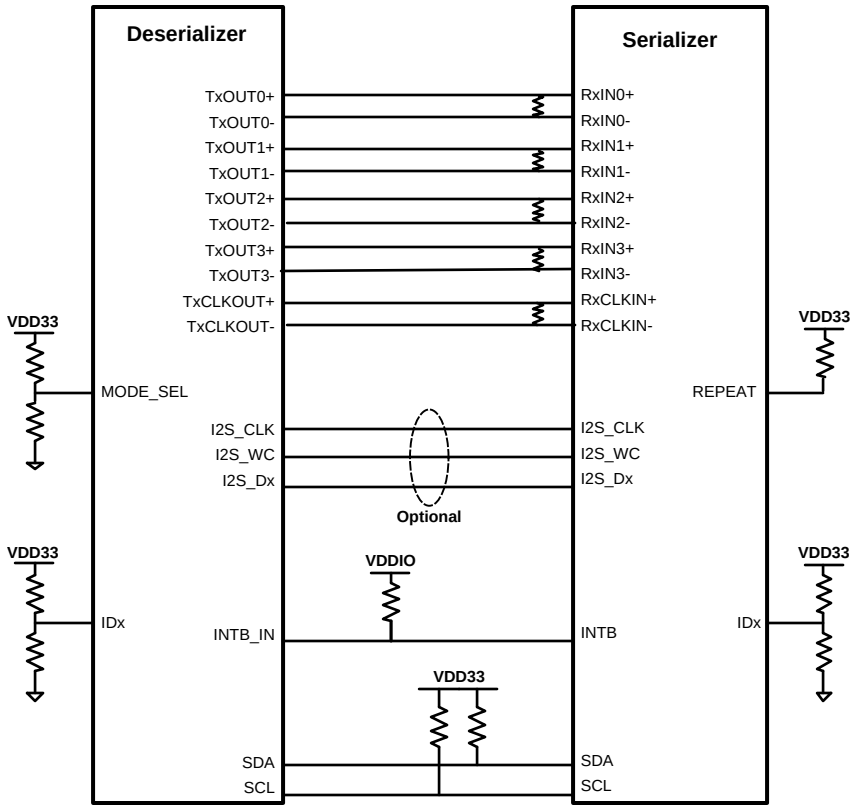


Figure 31. HDCP Repeater Connection Diagram

8.4.5.1 Repeater Fan-Out Electrical Requirements

Repeater applications requiring fan-out from one DS90UH928Q-Q1 deserializer to up to three DS90UH927Q-Q1 serializers requires special considerations for routing and termination of the FPD-Link differential traces. Figure 32 details the requirements that must be met for each signal pair:

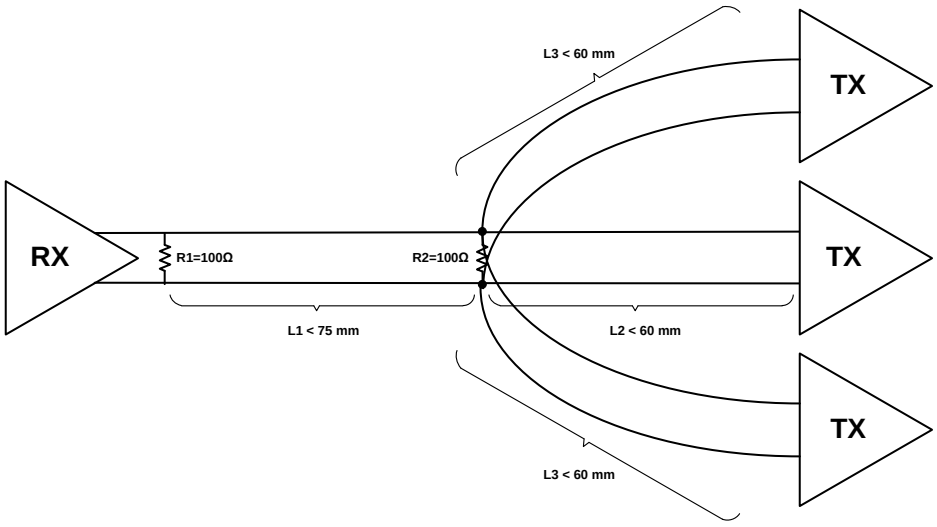


Figure 32. FPD-Link Fan-Out Electrical Requirements

8.4.6 HDCP I2S Audio Encryption

Depending on the quality and specifications of the audiovisual source, HDCP encryption of digital audio may be required. When HDCP is active, packetized Data Island Transport audio is also encrypted along with the video data per HDCP v.1.3. I2S audio transmitted in Forward Channel Frame Transport mode is not encrypted. System designers should consult the specific HDCP specifications to determine if encryption of digital audio is required by the specific application audiovisual source.

8.4.7 Repeater Configuration

The HDCP Cipher function is implemented in the deserializer per HDCP v1.3 specification. The DS90UH928Q-Q1 provides HDCP decryption of audiovisual content when connected to an HDCP capable FPD-Link III serializer. HDCP authentication and shared key generation is performed using the HDCP Control Channel, which is embedded in the forward and backward channels of the serial link. On-chip Non-Volatile Memory (NVM) is used to store the HDCP keys. The confidential HDCP keys are loaded by TI during the manufacturing process and are not accessible external to the device.

The supported HDCP Repeater application provides a mechanism to extend HDCP transmission over multiple links to multiple display devices. It authenticates all HDCP devices in the system and distributes protected content to the HDCP Receivers using the encryption mechanisms provided in the HDCP specification.

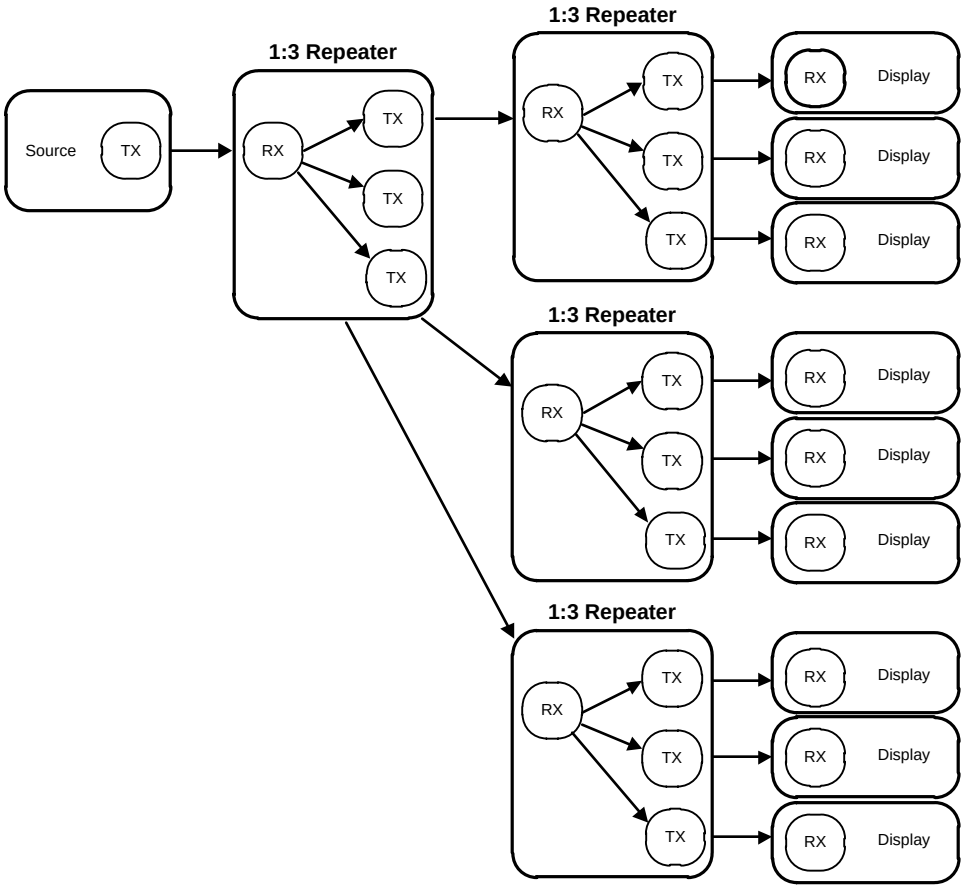


Figure 33. HDCP Maximum Repeater Application

In the HDCP repeater application, this document refers to the DS90UH927Q-Q1 or DS90UH925Q-Q1 as the HDCP Transmitter (TX), and refers to the DS90UH928Q-Q1 or DS90UH926Q-Q1 as the HDCP Receiver (RX). Figure 33 shows the maximum configuration supported for HDCP Repeater implementations. Two levels of HDCP Repeaters are supported with a maximum of three HDCP Transmitters per HDCP Receiver.

In a repeater application, the I^2C interface at each TX and RX is configured to transparently pass I^2C communications upstream or downstream to any I2C device within the system. This includes a mechanism for assigning alternate IDs (Slave Aliases) to downstream devices in the case of duplicate addresses.

To support HDCP Repeater operation, the RX includes the ability to control the downstream authentication process, assemble the KSV list for downstream HDCP Receivers, and pass the KSV list to the upstream HDCP Transmitter. An I^2C master within the RX communicates with the I^2C slave within the TX. The TX handles authenticating with a downstream HDCP Receiver and makes status available through the I^2C interface. The RX monitors the transmit port status for each TX and reads downstream KSV and KSV list values from the TX.

In addition to the I^2C interface used to control the authentication process, the HDCP Repeater implementation includes two other interfaces. The FPD-Link LVDS interface outputs the unencrypted video data. In addition to providing the video data, the LVDS interface communicates control information and packetized audio data. All audio and video data is decrypted at the output of the HDCP Receiver and is re-encrypted by the HDCP Transmitter. Figure 34 provides more detailed block diagram of a 1:2 HDCP repeater configuration.

If the repeater node includes a local output to a display, White Balancing and Hi-FRC dithering functions should not be used as they will block encrypted I2S audio and HDCP authentication.

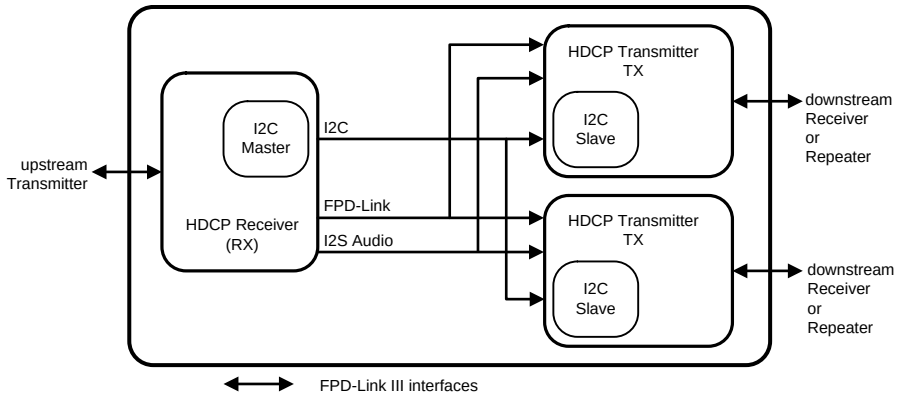


Figure 34. HDCP 1:2 Repeater Configuration

8.5 Programming

8.5.1 Serial Control Bus

The DS90UH928Q-Q1 may also be configured by the use of an I^2C compatible serial control bus. Multiple devices may share the serial control bus (up to 10 device addresses supported). The device address is set via a resistor divider (R1 and R2 — see Figure 35) connected to the IDx pin.

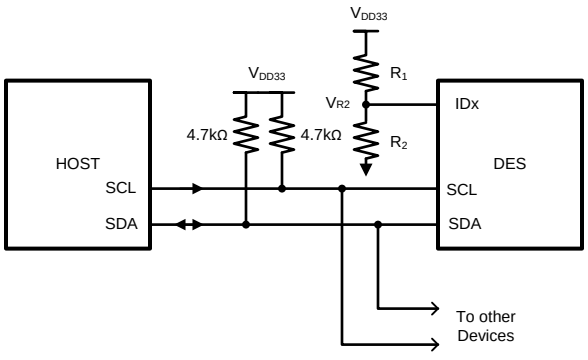


Figure 35. Serial Control Bus Connection

The serial control bus consists of two signals and an address configuration pin. SCL is a Serial Bus Clock Input/Output. SDA is the Serial Bus Data Input/Output signal. Both SCL and SDA signals require an external pullup resistor to V_{DD33} or V_{DDIO} = 3.0 V to 3.6 V. For most applications, a 4.7-kΩ pullup resistor to V_{DD33} is recommended. The signals are either pulled HIGH, or driven LOW.

Programming (continued)

The IDx pin configures the control interface to one of 10 possible device addresses. A pullup resistor and a pulldown resistor should be used to set the appropriate voltage ratio between the IDx input pin (V_{R2}) and V_{DD33}, each ratio corresponding to a specific device address. See Table 7 below.

Table 6. Serial Control Bus Addresses for IDx

NO.	IDEAL RATIO V_{R2} / V_{DD33}	IDEAL V_{R2} (V)	SUGGESTED RESISTOR R1 kΩ (1% tol)	SUGGESTED RESISTOR R2 kΩ (1% tol)	ADDRESS 7'b	ADDRESS 8'b
1	0	0	OPEN	40.2 or >10	0x2C	0x58
2	0.995	0.302	226	97.6	0x33	0x66
3	1.137	0.345	215	113	0x34	0x68
4	1.282	0.388	200	127	0x35	0x6A
5	1.413	0.428	187	140	0x36	0x6C
6	1.570	0.476	174	158	0x37	0x6E
7	1.707	0.517	154	165	0x38	0x70
8	1.848	0.560	150	191	0x39	0x72
9	1.997	0.605	137	210	0x3A	0x74
10	2.535	0.768	90.9	301	0x3B	0x76

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See Figure 36.

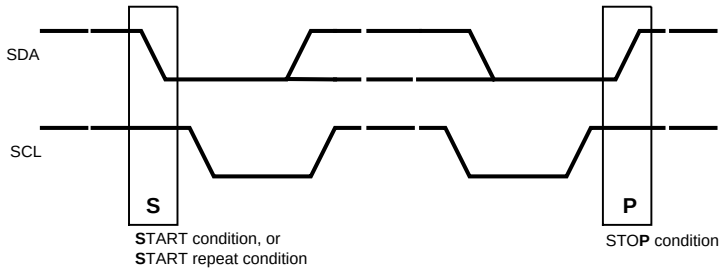


Figure 36. START and STOP Conditions

To communicate with a remote device, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus LOW. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled HIGH. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 37 and a WRITE is shown in Figure 38.

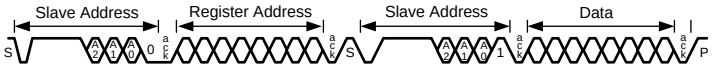


Figure 37. Serial Control Bus — READ

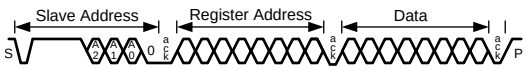


Figure 38. Serial Control Bus — WRITE

To support I²C transactions over the BCC. the I²C Master located at the DS90UH928Q-Q1 deserializer must support I²C clock stretching. For more information on I²C interface requirements and throughput considerations, please refer to TI Application Note SNLA131.

8.6 Register Maps

Table 7. Serial Control Bus Registers(1) (2)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
0	0x00	I2C Device ID	7:1	RW	IDx	Device ID	7–bit address of Deserializer Note: Read-only unless bit 0 is set
			0	RW		ID Setting	I2C ID Setting 0: Device ID is from IDx pin 1: Register I2C Device ID overrides IDx pin
1	0x01	Reset	7:3		0x04		Reserved
			2	RW		BC Enable	Back Channel Enable 0: Disable 1: Enable
			1	RW		Digital RESET1	Reset the entire digital block including registers This bit is self-clearing. 0: Normal operation (default) 1: Reset
			0	RW		Digital RESET0	Reset the entire digital block except registers This bit is self-clearing 0: Normal operation (default) 1: Reset
2	0x02	General Configuration 0	7	RW	0x00	OEN	LVCMOS Output Enable. Self-clearing on loss of LOCK 0: Disable, Tristate Outputs (default) 1: Enable
			6	RW		OEN/OSS_SEL Override	Output Enable and Output Sleep State Select override 0: Disable over-write (default) 1: Enable over-write
			5	RW		Auto Clock Enable	OSC Clock Output. Enable On loss of lock, OSC clock is output onto TxCLK± 0: Disable (default) 1: Enable
			4	RW		OSS_SEL	Output Sleep State Select. Enable Select to control output state during lock low period 0: Disable, Tri-State Outputs (default) 1: Enable
			3	RW		BKWD Override	Backwards Compatibility Mode Override 0: Use MODE_SEL pin (default) 1: Use register bit to set BKWD mode
			2	RW		BKWD Mode	Backwards Compatibility Mode Select 0: Backwards Compatibility Mode disabled (default) 1: Backwards Compatibility Mode enabled
			1	RW		LFMODE Override	Low Frequency Mode Override 0: Use LFMODE pin (default) 1: User register bit to set LFMODE
			0	RW		LFMODE	Low Frequency Mode 0: 15MHz ≤ PCLK ≤ 85MHz (default) 1: 5MHz ≤ PCLK < 15MHz

(1) Addresses not listed are reserved.
(2) Do not alter Reserved fields from their default values.

Register Maps (continued)

Table 7. Serial Control Bus Registers(1) (2) (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
3	0x03	General Configuration 1	7		0xF0		Reserved
			6	RW		Back channel CRC Generator Enable	Back Channel CRC Generator Enable 0: Disable 1: Enable (default)
			5	RW		Failsafe	Outputs Failsafe Mode. Determines the pull direction for undriven LVCMOS inputs 0: Pullup 1: Pulldown (default)
			4	RW		Filter Enable	HS, VS, DE two clock filter. When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected 0: Filtering disable 1: Filtering enable (default)
			3	RW		I2C Pass-Through	I2C Pass-Through Mode Read/Write transactions matching any entry in the DeviceAlias registers will be passed through to the remote serializer I2C interface. 0: Pass-Through Disabled (default) 1: Pass-Through Enabled
			2	RW		Auto ACK	Automatically Acknowledge I2C transactions independent of the forward channel Lock state. 0: Disable (default) 1: Enable
			1:0				Reserved
4	0x04	BCC Watchdog Control	7:1	RW	0xFE	BCC Watchdog Timer	BCC Watchdog Timer The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
			0	RW		BCC Watchdog Disable	Disable Bidirectional Control Channel Watchdog Timer 0: Enable (default) 1: Disable
5	0x05	I2C Control 1	7	RW	0x1E	I2C Pass-All	I2C Pass-Through All Transactions. Pass all local I2C transactions to the remote serializer. 0: Disable (default) 1: Enable
			6:4	RW		I2C SDA Hold	Internal I2C SDA Hold Time This field configures the amount of internal hold time is provided for the SDA input relative to the SCL input. Units are 50ns.
			3:0	RW		I2C Filter Depth	I2C Glitch Filter Depth This field configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.

Register Maps (continued)

Table 7. Serial Control Bus Registers(1) (2) (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
6	0x06	I2C Control 2	7	RW	0x00	Forward Channel Sequence Error	Control Channel Sequence Error Detected Indicates a sequence error has been detected in forward control channel. It this bit is set, an error may have occurred in the control channel operation.
			6	RW		Clear Sequence Error	Clears the Sequence Error Detect bit This bit is not self-clearing.
			5				Reserved
			4:3	RW		SDA Output Delay	SDA Output Delay This field configures output delay on the SDA output. Setting this value will increase output delay in units of 50ns. Nominal output delay values for SCL to SDA are: 00: 250ns (default) 01: 300ns 10: 350ns 11: 400ns
			2	RW		Local Write Disable	Disable Remote Writes to Local Registers through Serializer (Does not affect remote access to I2C slaves) 0: Remote write to local device registers (default) 1: Stop remote write to local device registers
			1	RW		I2C Bus Timer Speedup	Speed up I2C Bus Watchdog Timer 0: Timer expires after approximately 1s (default) 1: Timer expires after approximately 50µs
			0	RW		I2C Bus Timer Disable	Disable I2C Bus Watchdog Timer. When the I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1 second, the I2C bus is assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL
7	0x07	Remote ID	7:1	R	0x00	Remote ID	Remote Serializer ID RW if bit 0 is set
			0	RW		Freeze Device ID	Freeze Serializer Device ID 0: Auto-load Serializer Device ID (default) 1: Prevent auto-loading of Serializer Device ID from the remote device. The ID will be frozen at the value written.
8	0x08	Slave ID[0]	7:1	RW	0x00	Slave Device ID0	7-bit Remote Slave Device ID 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[0], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
9	0x09	Slave ID[1]	7:1	RW	0x00	Slave Device ID1	7-bit Remote Slave Device ID1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[1], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved

Register Maps (continued)

Table 7. Serial Control Bus Registers[1] [2] (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
10	0x0A	Slave ID[2]	7:1	RW	0x00	Slave Device ID2	7-bit Remote Slave Device ID2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[2], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
11	0x0B	Slave ID[3]	7:1	RW	0x00	Slave Device ID3	7-bit Remote Slave Device ID3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[3], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
12	0x0C	Slave ID[4]	7:1	RW	0x00	Slave Device ID4	7-bit Remote Slave Device ID4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[4], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
13	0x0D	Slave ID[5]	7:1	RW	0x00	Slave Device ID5	7-bit Remote Slave Device ID5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[5], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
14	0x0E	Slave ID[6]	7:1	RW	0x00	Slave Device ID6	7-bit Remote Slave Device ID6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[6], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
15	0x0F	Slave ID[7]	7:1	RW	0x00	Slave Device ID7	7-bit Remote Slave Device ID 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[7], the transaction will be re-mapped to this address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
16	0x10	Slave Alias[0]	7:1	RW	0x00	Slave Device Alias 0	7-bit Remote Slave Alias 0 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[0], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved

Register Maps (continued)

Table 7. Serial Control Bus Registers[1] [2] (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
17	0x11	Slave Alias[1]	7:1	RW	0x00	Slave Device Alias 1	7-bit Remote Slave Alias 1 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[1], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
18	0x12	Slave Alias[2]	7:1	RW	0x00	Slave Device Alias 2	7-bit Remote Slave Alias 2 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[2], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
19	0x13	Slave Alias[3]	7:1	RW	0x00	Slave Device Alias 3	7-bit Remote Slave Alias 3 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[3], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
20	0x14	Slave Alias[4]	7:1	RW	0x00	Slave Device Alias 4	7-bit Remote Slave Alias 4 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[4], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
21	0x15	Slave Alias[5]	7:1	RW	0x00	Slave Device Alias 5	7-bit Remote Slave Alias 5 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[5], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
22	0x16	Slave Alias[6]	7:1	RW	0x00	Slave Device Alias 6	7-bit Remote Slave Alias 6 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[6], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved
23	0x17	Slave Alias[7]	7:1	RW	0x00	Slave Device Alias 7	7-bit Remote Slave Alias 7 Configures the physical I2C address of the remote I2C Slave device attached to the remote Serializer. If an I2C transaction is addressed to the Slave Alias ID[7], the transaction will be re-mapped to the ID address before passing the transaction across the Bidirectional Control Channel to the Serializer.
			0				Reserved

Register Maps (continued)

Table 7. Serial Control Bus Registers(1) (2) (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
24	0x18	Mailbox[0]	7:0	RW	0x00	Mailbox Register 0	Mailbox Register 0 This register may be used to temporarily store temporary data, such as status or multi-master arbitration
25	0x19	Mailbox[1]	7:0	RW	0x00	Mailbox Register 1	Mailbox Register 1 This register may be used to temporarily store temporary data, such as status or multi-master arbitration
27	0x1B	Frequency Counter	7:0	RW	0x00	Frequency Count	Frequency Counter control A write to this register will enable a frequency counter to count the number of pixel clock during a specified time interval. The time interval is equal to the value written multiplied by the oscillator clock period (nominally 50ns). A read of the register returns the number of pixel clock edges seen during the enabled interval. The frequency counter will saturate at 0xff if it reaches the maximum value. The frequency counter will provide a rough estimate of the pixel clock period. If the pixel clock frequency is known, the frequency counter may be used to determine the actual oscillator clock frequency.
28	0x1C	General Status	7:4		0x00		Reserved
			3	R		I2S Locked	I2S Lock Status 0: I2S PLL controller not locked (default) 1: I2S PLL controller locked to input I2S clock
			2	R		CRC Error	CRC Error Detected 0: No CRC errors detected 1: CRC errors detected
			1				Reserved
			0	R		LOCK	Deserializer CDR and PLL Locked to recovered clock frequency 0: Deserializer not Locked (default) 1: Deserializer Locked to recovered clock
29	0x1D	GPIO0 Configuration	7:4	R	0x20	Revision ID	Device Revision ID: 0010: Production Device
			3	RW		GPIO0 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) 1: Output HIGH
			2	RW		GPIO0 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote device (default) 1: Enable GPIO control from remote device. The GPIO pin will be an output, and the value is received from the remote device.
			1	RW		GPIO0 Direction	Local GPIO Direction 0: Output (default) 1: Input
			0	RW		GPIO0 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation

Register Maps (continued)

Table 7. Serial Control Bus Registers(1) (2) (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
30	0x1E	GPIO1 and GPIO2 Configuration	7	RW	0x00	GPIO2 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) 1: Output HIGH
			6	RW		GPIO2 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote device (default) 1: Enable GPIO control from remote device. The GPIO pin will be an output, and the value is received from the remote device.
			5	RW		GPIO2 Direction	Local GPIO Direction 0: Output (default) 1: Input
			4	RW		GPIO2 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
			3	RW		GPIO1 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) 1: Output HIGH
			2	RW		GPIO1 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote device (default) 1: Enable GPIO control from remote device. The GPIO pin will be an output, and the value is received from the remote device.
			1	RW		GPIO1 Direction	Local GPIO Direction 1: Input 0: Output
			0	RW		GPIO1 Enable	GPIO function enable 1: Enable GPIO operation 0: Enable normal operation
31	0x1F	GPIO3 Configuration	7:4		0x00		Reserved
			3	RW		GPIO3 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is Output, and remote GPIO control is disabled. 0: Output LOW (default) 1: Output HIGH
			2	RW		GPIO3 Remote Enable	Remote GPIO Control 0: Disable GPIO control from remote device (default) 1: Enable GPIO control from remote device. The GPIO pin will be an output, and the value is received from the remote device.
			1	RW		GPIO3 Direction	Local GPIO Direction 0: Output (default) 1: Input
			0	RW		GPIO3 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation

Register Maps (continued)

Table 7. Serial Control Bus Registers(1) (2) (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
32	0x20	GPIO_REG5 and GPIO_REG6 Configuration	7	RW	0x00	GPIO_REG 6 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) 1: Output HIGH
			6				Reserved
			5	RW		GPIO_REG 6 Direction	Local GPIO Direction 0: Output (default) 1: Input
			4	RW		GPIO_REG 6 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
			3	RW		GPIO_REG 5 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) 1: Output HIGH
			2				Reserved
			1	RW		GPIO_REG 5 Direction	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
			0	RW		GPIO_REG 5 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
33	0x21	GPIO_REG7 and GPIO_REG8 Configuration	7	RW	0x00	GPIO_REG 8 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) 1: Output HIGH
			6				Reserved
			5	RW		GPIO_REG 8 Direction	Local GPIO Direction 0: Output (default) 1: Input
			4	RW		GPIO_REG 8 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation
			3	RW		GPIO_REG 7 Output Value	Local GPIO Output Value This value is output on the GPIO pin when the GPIO function is enabled, and the local GPIO direction is Output. 0: Output LOW (default) 1: Output HIGH
			2				Reserved
			1	RW		GPIO_REG 7 Direction	Local GPIO Direction 0: Output (default) 1: Input
			0	RW		GPO_REG 7 Enable	GPIO Function Enable 0: Enable normal operation (default) 1: Enable GPIO operation

Register Maps (continued)

Table 7. Serial Control Bus Registers[1] [2] (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
34	0x22	Data Path Control	7	RW	0x00	Override FC Configuration	Override Configuration Loaded by Forward Channel 0: Allow forward channel loading of this register (default) 1: Disable loading of this register from the forward channel, keeping locally written values intact Bits [6:0] are RW if this bit is set
			6	R		Pass RGB	Pass RGB on DE Setting this bit causes RGB data to be sent independent of DE in DS90UH928, which can be used to allow DS90UH928 to interoperate with DS90UB925 and DS90UB926. However, setting this bit prevents HDCP operation and blocks packetized audio. This bit does not need to be set in Backward Compatibility mode. 0: Normal operation (default) 1: Pass RGB independent of DE
			5	R		DE Polarity	This bit indicates the polarity of the DE (Data Enable) signal. 0: DE is positive (active high, idle low) (default) 1: DE is inverted (active low, idle high)
			4	R		I2S Repeater Regen	Regenerate I2S Data From Repeater I2S Pins 0: Output packetized audio on RGB video output pins. (default) 1: Repeater regenerates I2S from I2S pins
			3	R		I2S Channel B Enable Override	I2S Channel B Override 0: Set I2S Channel B Disabled (default) 1: Set I2S Channel B Enable from register
			2	R		18-bit Video Select	Video Color Depth Mode 0: Select 24-bit video mode (default) 1: Select 18-bit video mode
			1	R		I2S Transport Select	Select I2S Transport Mode 0: Enable I2S Data Island Transport (default) 1: Enable I2S Data Forward Channel Frame Transport
			0	R		I2S Channel B Enable	I2S Channel B Enable 0: I2S Channel B disabled (default) 1: Enable I2S Channel B
35	0x23	Rx Mode Status	7	RW	0x10	RGB Checksum Enable	Rx RGB Checksum Enable Setting this bit enables the Receiver to validate a one-byte checksum following each video line. Checksum failures are reported in the HDCP_STS register. 0: Disabled (default) 1: Enabled
			6:4				Reserved
			3	R		LFMODE Status	Low Frequency Mode (LFMODE) pin status 0: 15 ≤ TxCLKOUT ≤ 85MHz (default) 1: 5 ≤ TxCLKOUT < 15MHz
			2	R		REPEAT Status	Repeater Mode (REPEAT) pin Status 0: Non-repeater (default) 1: Repeater
			1	R		BKWD Status	Backward Compatible Mode (BKWD) Status 0: Compatible to DS90UB925/7Q (default) 1: Backward compatible to DS90UR905/7Q
			0	R		I2S Channel B Status	I2S Channel B Mode (I2S_DB) Status 0: I2S_DB inactive (default) 1: I2S_DB active

Register Maps (continued)

Table 7. Serial Control Bus Registers[1] [2] (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
36	0x24	BIST Control	7:4		0x08		Reserved
			3	RW		BIST Pin Config	BIST Pin Configuration 0: BIST enabled from register 1: BIST enabled from pin (default)
			2:1	RW		OSC Clock Source	Internal OSC clock select for Functional Mode or BIST. Functional Mode when PCLK is not present and 0x03[1]=1. 00: 33 MHz Oscillator (default) 01: 33 MHz Oscillator Note: In LFMODE=1, the internal oscillator is 12.5MHz
			0	RW		BIST Enable	BIST Control 0: Disabled (default) 1: Enabled
37	0x25	BIST Error	7:0	R	0x00	BIST Error Count	Errors Detected During BIST Records the number (up to 255) of forward-channel errors detected during BIST. The value stored in this register is only valid after BIST terminates (BISTEN = 0). Resets on PDB = 0 or start of another BIST (BISTEN = 1).
38	0x26	SCL High Time	7:0	RW	0x83	SCL High Time	I2C Master SCL High Time This field configures the high pulse width of the SCL output when the deserializer is the Master on the local I2C bus. Units are 50 ns for the nominal oscillator clock frequency.
39	0x27	SCL Low Time	7:0	RW	0x84	SCL Low Time	I2C SCL Low Time This field configures the low pulse width of the SCL output when the deserializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 50 ns for the nominal oscillator clock frequency.
40	0x28	Data Path Control 2	7	RW	0x00	Block I2S Auto Config	Override Forward Channel Configuration 0: Enable forward-channel loading of this register 1: Disable loading of this register from the forward channel, keeping local values intact
			6:4				Reserved
			3	RW		Aux I2S Enable	Auxiliary I2S Channel Enable 0: Normal GPIO[1:0] operation 1: Enable Aux I2S channel on GPIO1 (AUX word select) and GPIO0 (AUX data)
			2	RW		I2S Disable	Disable All I2S Outputs 0: I2S Outputs Enabled (default) 1: I2S Outputs Disabled
			1				Reserved
			0	RW		I2S Surround	Enable 5.1- or 7.1-channel I2S audio transport 0: 2-channel or 4-channel I2S audio is enabled as configured in register or MODE_SEL (default) 1: 5.1- or 7.1-channel audio is enabled Note that I2S Data Island Transport is the only option for surround audio. Also note that in a repeater, this bit may be overridden by the in-band I2S mode detection.

Register Maps (continued)

Table 7. Serial Control Bus Registers(1) (2) (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
41	0x29	FRC Control	7	RW	0x00	Timing Mode Select	Select Display Timing Mode 0: DE only Mode (default) 1: Sync Mode (VS,HS)
			6	RW		HS Polarity	Horizontal Sync Polarity Select 0: Active High (default) 1: Active Low
			5	RW		VS Polarity	Vertical Sync Polarity Select 0: Active High (default) 1: Active Low
			4	RW		DE Polarity	Data Enable Sync Polarity Select 0: Active High (default) 1: Active Low
			3	RW		FRC2 Enable	FRC2 Enable 0: FRC2 disable (default) 1: FRC2 enable
			2	RW		FRC1 Enable	FRC1 Enable 0: FRC1 disable (default) 1: FRC1 enable
			1	RW		Hi-FRC2 Enable	Hi-FRC2 Enable 0: Hi-FRC2 enable (default) 1: Hi-FRC2 disable
			0	RW		Hi-FRC1 Enable	Hi-FRC1 Enable 0: Hi-FRC1 enable (default) 1: Hi-FRC1 disable
42	0x2A	White Balance Control	7:6	RW	0x00	Page Setting	Control/LUT Setting Page Select 00: Configuration Registers (default) 01: Red LUT 10: Green LUT 11: Blue LUT
			5	RW		White Balance Enable	White Balance Enable 0: White Balance Disabled (default) 1: White Balance Enabled
			4	RW		LUT Reload Enable	Enable LUT Reload 0: Reload Disable (default) 1: Reload Enable
			3:0				Reserved
43	0x2B	I2S Control	7	RW	0x00	I2S PLL Override	Override I2S PLL 0: PLL override disabled (default) 1: PLL override enabled
			6	RW		I2S PLL Enable	Enable I2S PLL 0: I2S PLL is on for I2S data jitter cleaning (default) 1: I2S PLL is off. No jitter cleaning
			5:1				Reserved
			0	RW		I2S Clock Edge	I2S Clock Edge Select 0: I2S Data is strobed on the Falling Clock Edge (default) 1: I2S Data is strobed on the Rising Clock Edge

Register Maps (continued)

Table 7. Serial Control Bus Registers(1) (2) (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
53	0x35	AEQ Control	7		0x00		Reserved
			6	RW		AEQ Restart	Restart AEQ adaptation from initial (Floor) values 0: Normal operation (default) 1: Restart AEQ adaptation Note: This bit is not self-clearing. It must be set, then reset.
			5	RW		LCBL Override	Override LCBL Mode Set by MODE_SEL 0: LCBL controlled by MODE_SEL pin 1: LCBL controlled by register
			4	RW		LCBL	Set LCBL Mode 0: LCBL Mode disabled 1: LCBL Mode enabled. AEQ Floor value is controlled from Adaptive EQ MIN/MAX register
			3:0				Reserved
57	0x39	PG Internal Clock Enable	7:2		0x00		Reserved
			1	RW		PG INT CLK	Enable Pattern Generator Internal Clock This bit must be set to use the Pattern Generator Internal Clock Generation 0: Pattern Generator with external PCLK 1: Pattern Generator with internal PCLK See TI Application Note ( ) for details
			0				Reserved
58	0x3A	I2S DIVSEL	7	RW	0x00	MCLK Div Override	Override MCLK Divider Setting 0: No override for MCLK divider (default) 1: Override divider select for MCLK
			6:4	RW		MCLK Div	See Table 3
			3:0				Reserved
59	0x3B	Adaptive EQ Status	7:6				Reserved
			5:0			EQ Status	Equalizer Status Current equalizer level set by AEQ or Override Register
68	0x44	Adaptive Equalizer Bypass	7:5	RW	0x60	EQ Stage 1 Select Value	EQ Stage 1 select value. Used if adaptive EQ is bypassed. Used if adaptive EQ is bypassed.
			4				Reserved
			3:1	RW		EQ Stage 2 Select Value	EQ Stage 2 select value. Used if adaptive EQ is bypassed Used if adaptive EQ is bypassed.
			0	RW		Adaptive EQ Bypass	Bypass Adaptive EQ Overrides Adaptive EQ search and sets the EQ to the static value configured in this register 0: Enable adaptive EQ (default) 1: Disable adaptive EQ (to write EQ select values)
69	0x45	Adaptive EQ MIN/MAX	7:4	RW	0x88		Reserved
			3:0	RW		Adaptive EQ Floor	Adaptive Equalizer Floor Value Sets the AEQ floor value when Long Cable Mode (LCBL) is enabled by register or MODE_SEL
73	0x49	Map Select	7	R	0x00	MAPSEL Pin Status	Returns Status of MAPSEL pin
			6	RW		MAPSEL Override	Map Select (MAPSEL) Setting Override 0: MAPSEL set from pin 1: MAPSEL set from register
			5	RW		MAPSEL	Map Select (MAPSEL) Setting 0: LSBs on TxOUT3± 1: MSBs on TxOUT3±
			4:0				Reserved

Register Maps (continued)

Table 7. Serial Control Bus Registers[1] [2] (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
86	0x56	Loop-Through Driver	7:4		0x08		Reserved
			3	RW		Loop-Through Driver Enable	Enable CML Loop-Through Driver (CMLOUTP/CMLOUTN) 0: Enable 1: Disable (default)
			2:0				Reserved
100	0x64	Pattern Generator Control	7:4	RW	0x10	Pattern Generator Select	Fixed Pattern Select Selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. xxxx: normal/inverted 0000: Checkerboard 0001: White/Black (default) 0010: Black/White 0011: Red/Cyan 0100: Green/Magenta 0101: Blue/Yellow 0110: Horizontal Black-White/White-Black 0111: Horizontal Black-Red/White-Cyan 1000: Horizontal Black-Green/White-Magenta 1001: Horizontal Black-Blue/White-Yellow 1010: Vertical Black-White/White— Black 1011: Vertically Scaled Black to Red/White to Cyan 1100: Vertical Black-Green/White-Magenta 1101: Vertical Black-Blue/White-Yellow 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers 1111: VCOM See TI App Note AN-2198 ().
			3				***Reserved***
			2	RW		Color Bars Pattern	Enable Color Bars Pattern 0: Color Bars disabled (default) 1: Color Bars enabled Overrides the selection from bits [7:4]
			1	RW		VCOM Pattern Reverse	Reverse order of color bands in VCOM pattern 0: Color sequence from top left is (YCBR) (default) 1: Color sequence from top left is (RBCY)
			0	RW		Pattern Generator Enable	Pattern Generator Enable 0: Disable Pattern Generator (default) 1: Enable Pattern Generator See TI App Note AN-2198 ().

Register Maps (continued)

Table 7. Serial Control Bus Registers[1] [2] (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
101	0x65	Pattern Generator Configuration	7		0x00		Reserved
			6	RW		Checkerboard Scale	Scale Checkerboard Patterns: 0: Normal operation (each square is 1x1 pixel) (default) 1: Scale checkered patterns (VCOM and checkerboard) by 8 (each square is 8x8 pixels) Setting this bit gives better visibility of the checkered patterns.
			5	RW		Custom Checkerboard	Use Custom Checkerboard Color 0: Use white and black in the Checkerboard pattern (default) 1: Use the Custom Color and black in the Checkerboard pattern
			4	RW		PG 18–bit Mode	18-bit Mode Select: 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness. (default) 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits.
			3	RW		External Clock	Select External Clock Source: 0: Selects the internal divided clock when using internal timing (default) 1: Selects the external pixel clock when using internal timing. This bit has no effect in external timing mode (PATGEN_TSEL = 0).
			2	RW		Timing Select	Timing Select Control: 0: the Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals. (default) 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size. Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers.
			1	RW		Color Invert	Enable Inverted Color Patterns: 0: Do not invert the color output. (default) 1: Invert the color output.
			0	RW		Auto Scroll	Auto Scroll Enable: 0: The Pattern Generator retains the current pattern. (default) 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. See TI App Note AN-2198 ().
102	0x66	PGIA	7:0	RW	0x00	PG Indirect Address	This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See TI App Note AN-2198 ().
103	0x67	PGID	7:0	RW	0x00	PG Indirect Data	When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the read back value. See TI App Note AN-2198 ().

Register Maps (continued)

Table 7. Serial Control Bus Registers[1] [2] (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
110	0x6E	GPI Pin Status 1	7	R	0x00	GPI7 Pin Status	GPI7 Pin Status. Readable when REG_GPIO7 is set as an input.
			6	R		GPI6 Pin Status	GPI6 Pin Status. Readable when REG_GPIO6 is set as an input.
			5	R		GPI5 Pin Status	GPI5 Pin Status. Readable when REG_GPIO5 is set as an input.
			4				Reserved
			3	R		GPI3 Pin Status	GPI3 Pin Status. Readable when GPIO3 is set as an input.
			2	R		GPI2 Pin Status	GPI2 Pin Status. Readable when GPIO2 is set as an input.
			1	R		GPI1 Pin Status	GPI1 Pin Status. Readable when GPIO1 is set as an input.
			0	R		GPI0 Pin Status	GPI0 Pin Status. Readable when GPIO0 is set as an input.
111	0x6D	GPI Pin Status 2	7:1		0x00		Reserved
			0	R		GPI8 Pin Status	GPI8 Pin Status. Readable when REG_GPIO8 is set as an input.
128	0x80	RX_BKSV0	7:0	R	0x00	RX BKSV0	BKSV0: Value of byte 0 of the Receiver KSV
129	0x81	RX_BKSV1	7:0	R	0x00	RX BKSV1	BKSV1: Value of byte 1 of the Receiver KSV
130	0x82	RX_BKSV2	7:0	R	0x00	RX BKSV2	BKSV2: Value of byte 2 of the Receiver KSV
131	0x83	RX_BKSV3	7:0	R	0x00	RX BKSV3	BKSV3: Value of byte 3of the Receiver KSV.
132	0x84	RX_BKSV4	7:0	R	0x00	RX BKSV4	BKSV4: Value of byte 4of the Receiver KSV.
144	0x90	TX_KSV0	7:0	R	0x00	TX KSV0	KSV0: Value of byte 0 of the Transmitter KSV.
145	0x91	TX_KSV1	7:0	R	0x00	TX KSV1	KSV1: Value of byte 1 of the Transmitter KSV.
146	0x92	TX_KSV2	7:0	R	0x00	TX KSV2	KSV2: Value of byte 2 of the Transmitter KSV.
147	0x93	TX_KSV3	7:0	R	0x00	TX KSV3	KSV3: Value of byte 3 of the Transmitter KSV.
148	0x94	TX_KSV4	7:0	R	0x00	TX KSV4	KSV4: Value of byte 4 of the Transmitter KSV.
152	0x98	TX_AN0	7:0	R	0x00	TX AN0	TX_AN0: Value of byte 0 of the Transmitter AN Value
153	0x99	TX_AN1	7:0	R	0x00	TX AN1	TX_AN1: Value of byte 1 of the Transmitter AN Value
154	0x9A	TX_AN2	7:0	R	0x00	TX AN2	TX_AN2: Value of byte 2 of the Transmitter AN Value
155	0x9B	TX_AN3	7:0	R	0x00	TX AN3	TX_AN3: Value of byte 3 of the Transmitter AN Value
156	0x9C	TX_AN4	7:0	R	0x00	TX AN4	TX_AN4: Value of byte 4 of the Transmitter AN Value
157	0x9D	TX_AN5	7:0	R	0x00	TX AN5	TX_AN5: Value of byte 5 of the Transmitter AN Value
158	0x9E	TX_AN6	7:0	R	0x00	TX AN6	TX_AN6: Value of byte 6 of the Transmitter AN Value
159	0x9F	TX_AN7	7:0	R	0x00	TX AN7	TX_AN7: Value of byte 7 of the Transmitter AN Value

Register Maps (continued)

Table 7. Serial Control Bus Registers(1) (2) (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
192	0xC0	HDCP Debug 1	7		0x00		Reserved
			6	R		HDCP Timeout Disable	HDCP I2C Timeout Disable Setting this bit to a 1 will disable the bus timeout function in the HDCP I2C master. When enabled, the bus timeout function allows the I2C master to assume the bus is free if no signaling occurs for more than 1 second. Set via the HDCP_DBG register in the HDCP Transmitter.
			5:4				Reserved
			3	R		RGB Checksum Enable	Enable RBG video line checksum Enables sending of ones-complement checksum for each 8-bit RBG data channel following end of each video data line. Set via the HDCP_DBG register in the HDCP Transmitter.
			2	R		Fast LV	Fast Link Verification HDCP periodically verifies that the HDCP Receiver is correctly synchronized. Setting this bit will increase the rate at which synchronization is verified. When set to a 1, Pj is computed every 2 frames and Ri is computed every 16 frames. When set to a 0, Pj is computed every 16 frames and Ri is computed every 128 frames. Set via the HDCP_DBG register in the HDCP Transmitter.
			1	R		Timer Speedup	Timer Speedup Speed up HDCP authentication timers. Set via the HDCP_DBG register in the HDCP Transmitter.
			0	R		HDCP I2C Fast	HDCP I2C Fast mode Enable Setting this bit to a 1 will enable the HDCP I2C Master in the HDCP Receiver to operation with Fast mode timing. If set to a 0, the I2C Master will operation with Standard mode timing. Set via the HDCP_DBG register in the HDCP Transmitter.
193	0xC1	HDCP Debug 2	7:2		0x00		Reserved
			1	RW		No Decrypt	Disable HDCP Decryption When disabled, the HDCP Receiver will output encrypted RGB data. This provides a simple method for verifying that the link is encrypted. 0: HDCP Decryption enabled 1: HDCP Decryption disabled
			0				Reserved
196	0xC4	HDCP Status	7:2		0x00		Reserved
			1	R		RGB Checksum ERR	RGB Checksum Error Detected If RGB Checksum in enabled through the HDCP Transmitter HDCP_DBG register, this bit will indicate if a checksum error is detected. This register may be cleared by writing any value to this register
			0	R		AUTHED	HDCP Authenticated Indicates the HDCP authentication has completed successfully. The controller may now send video data requiring content protection. This bit will be cleared if authentication is lost or if the controller restarts authentication.

Register Maps (continued)

Table 7. Serial Control Bus Registers(1) (2) (continued)

ADD (dec)	ADD (hex)	Register Name	Bit	Register Type	Default (hex)	Function	Description
224	0xE0	RPTR TX0	7:1	R	0x00	PORT0_ADDR	Transmit Port 0 I2C Address Indicates the I2C address for the Repeater Transmit Port.
			0	R		PORT0_VALID	Transmit Port 0 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register 0: Address Invalid (default) 1: Address Valid
225	0xE1	RPTR TX1	7:1	R	0x00	PORT1_ADDR	Transmit Port 1 I2C Address Indicates the I2C address for the Repeater Transmit Port.
			0	R		PORT1_VALID	Transmit Port 1 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register 0: Address Invalid (default) 1: Address Valid
226	0xE2	RPTR TX2	7:1	R	0x00	PORT2_ADDR	Transmit Port 2 I2C Address Indicates the I2C address for the Repeater Transmit Port.
			0	R		PORT2_VALID	Transmit Port 2 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register 0: Address Invalid (default) 1: Address Valid
227	0xE3	RPTR TX3	7:1	R	0x00	PORT3_ADDR	Transmit Port 3 I2C Address Indicates the I2C address for the Repeater Transmit Port.
			0	R		PORT3_VALID	Transmit Port 3 Valid Indicates that the HDCP Repeater has a transmit port at the I2C Address identified by upper 7 bits of this register 0: Address Invalid (default) 1: Address Valid
240	0xF0	HDCP RX ID	7:0	R	0x5F	ID0	First byte ID code, '_'
241	0xF1		7:0	R	0x55	ID1	Second byte of ID code, 'U'
242	0xF2		7:0	R	0x48	ID2	Third byte of ID code. 'H'
243	0xF3		7:0	R	0x39	ID3	Forth byte of ID code: '9'
244	0xF4		7:0	R	0x32	ID4	Fifth byte of ID code: "2"
245	0xF5		7:0	R	0x38	ID5	Sixth byte of ID code: "8"

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DS90UH928Q-Q1 deserializer, in conjunction with a DS90UH925Q-Q1 or DS90UH927Q-Q1 serializer, provides a solution for secure distribution of content-protected digital video and audio within automotive infotainment systems. It converts a high-speed serialized interface with an embedded clock, delivered over a single signal pair (FPD-Link III), to four LVDS data/control streams, one LVDS clock pair (FPD-Link), and I2S audio data. The digital video and audio data is protected using the industry standard HDCP copy protection scheme.The serial bus scheme, FPD-Link III, supports high speed forward channel data transmission and low speed full duplex back channel communication over a single differential link. Consolidation of audio, video data and control over a single differential pair reduces the interconnect size and weight, while also eliminating skew issues and simplifying system design.

9.2 Typical Application

Figure 39 shows a typical application of the DS90UH928Q-Q1 deserializer for an 85 MHz 24-bit Color Display Application. Inputs utilize 0.1-µF coupling capacitors to the line and the deserializer provides internal termination. The voltage rating of the coupling capacitors should be ≥50 V and should use a small body capacitor size, such as 0402 or 0602, to help ensure good signal integrity. The FPD-Link LVDS differential outputs require 100-Ω termination resistors at the receiving device or display.

Bypass capacitors must be placed near the power supply pins. At a minimum, three 4.7-µF capacitors, one placed at each power supply pin, are required for local device bypassing. If additional bypass capacitors are used, place the smaller value components closer to the pin. Ferrite beads are required on the two supplies (V_{DD33} and V_{DDIO}) for effective noise suppression. Pins VDD33_A and VDD33_B should be connected directly to ensure ESD performance. The interface to the display is FPD-Link LVDS. The VDDIO pin may be connected to 3.3 V or 1.8 V. A delay capacitor (>10 µF) and pullup resistor (10 kΩ) should be placed on the PDB signal to delay the enabling of the device until power is stable.

Typical Application (continued)

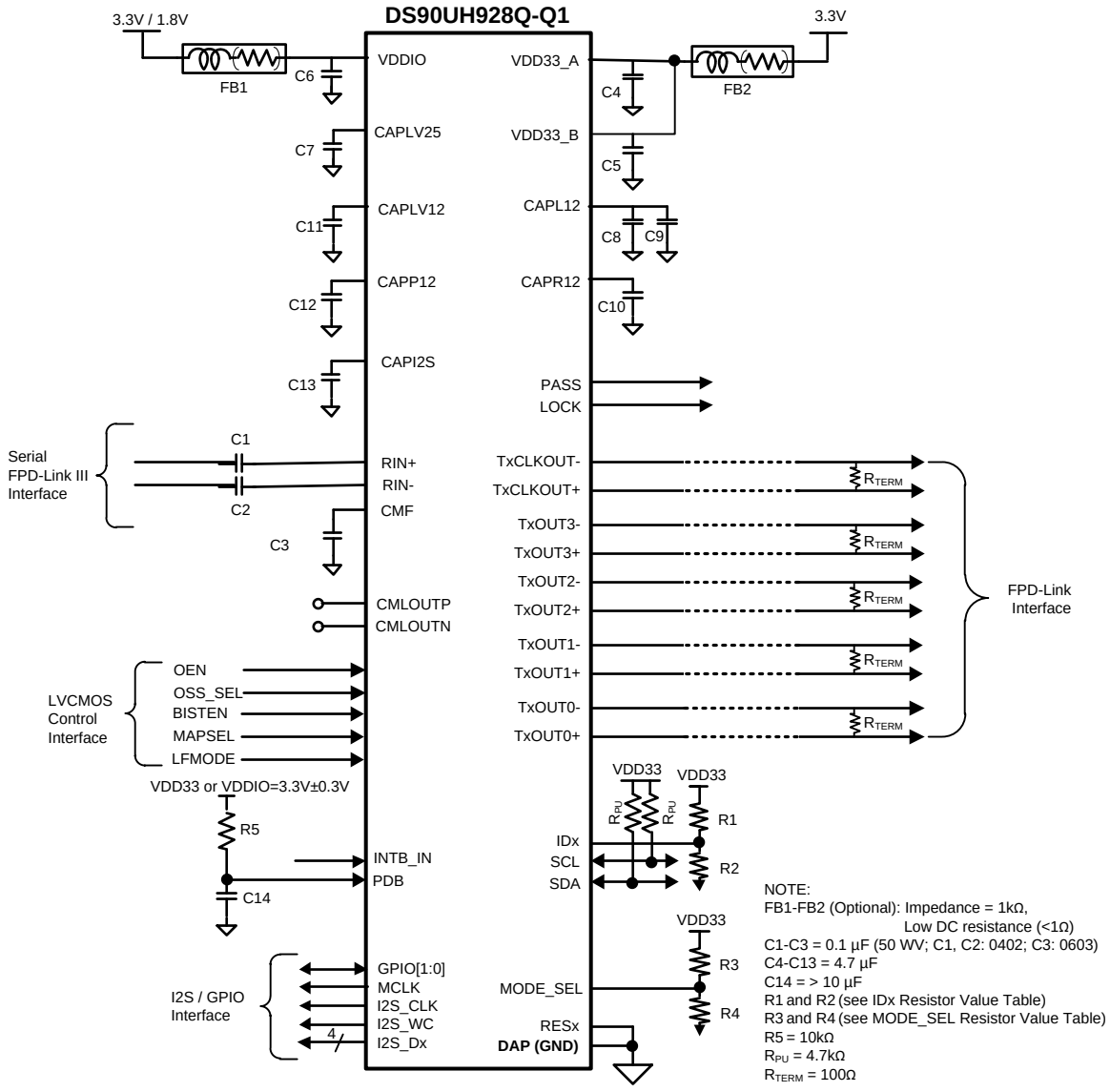


Figure 39. Typical Connection Diagram

Typical Application (continued)

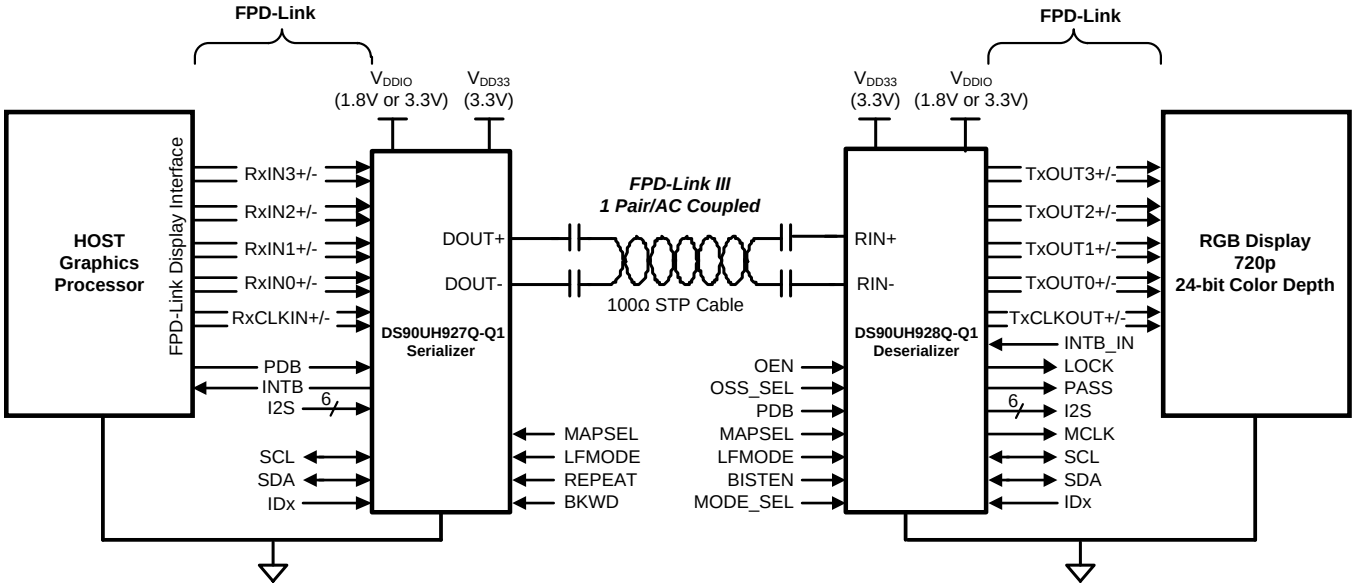


Figure 40. Typical Display System Diagram

9.2.1 Design Requirements

For the typical design application, use the following as input parameters:

Table 8. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V or 3.3 V
VDD33	3.3 V
AC Coupling Capacitor for RIN±	100 nF
PCLK Frequency	78 MHz

9.2.2 Detailed Design Procedure

9.2.2.1 Transmission Media

The DS90UH927Q-Q1 and DS90UH928Q-Q1 chipset is intended to be used in a point-to-point configuration through a shielded twisted pair cable. The serializer and deserializer provide internal termination to minimize impedance discontinuities. The interconnect (cable and connector) between the serializer and deserializer should have a differential impedance of 100 Ω. The maximum length of cable that can be used is dependant on the quality of the cable (gauge, impedance), connector, board (discontinuities, power plane), the electrical environment (for example, power stability, ground noise, input clock jitter, PCLK frequency, etc.) and the application environment.

The resulting signal quality at the receiving end of the transmission media may be assessed by monitoring the differential eye opening of the serial data stream. The Receiver CML Monitor Driver Output Specifications define the acceptable data eye opening width and eye opening height. A differential probe should be used to measure across the termination resistor at the CMLOUT± pin Figure 2.

9.2.2.2 Display Application

The DS90UH928Q-Q1, in conjunction with the DS90UH925Q-Q1 or DS90UH927Q-Q1, is intended for interfacing with a HDCP compliant host (graphics processor) and a display supporting 24-bit color depth (RGB888) and high definition (720p) digital video format. It can receive an 8-bit RGB stream with a pixel clock rate up to 85 MHz together with three control bits (VS, HS and DE) and four I2S audio streams. The included HDCP 1.3 compliant cipher block allows the authentication of the HDCP Deserializer, which decrypts both video and audio contents. The HDCP keys are pre-loaded by TI into Non-Volatile Memory (NVM) for maximum security.

9.2.3 Application Curves

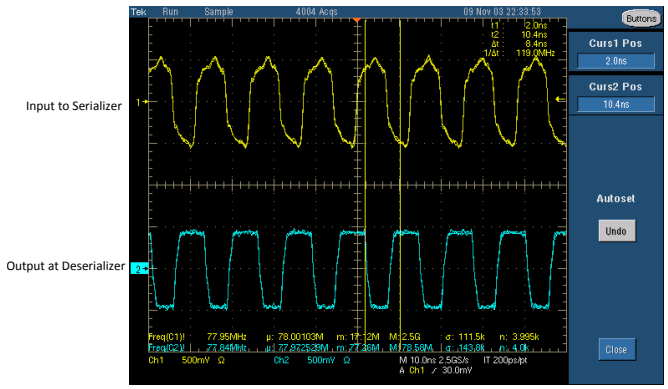


Figure 41. 78-MHz Clock at Serializer and Deserializer

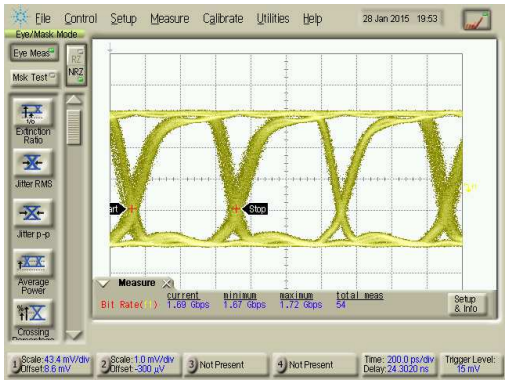


Figure 42. CMLOUT of Deserializer from 48-MHz Input Clock

10 Power Supply Recommendations

This section describes power-up requirements and the PDB pin. The power supply ramp (V_{DD33} and V_{DDIO}) should be faster than 1.5 ms with a monotonic rise. A large capacitor on the PDB pin is needed to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. The PDB pin requires a 10-kΩ pullup to V_{DD33} and a >10-µF capacitor to GND to delay the PDB input signal rise. If PDB is driven externally, do not drive the pin HIGH until V_{DD33} and V_{DDIO} have reached steady state. All inputs must not be driven until both V_{DD33} and V_{DDIO} have reached steady state. Pins VDD33_A and VDD33_B should both be externally connected, bypassed, and driven to the same potential (they are not internally connected).

11 Layout

11.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS serializer and deserializer devices should be designed to provide low-noise power to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mil) for power / ground sandwiches. This arrangement utilizes the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 µF to 10 µF. Tantalum capacitors may be in the 2.2 µF to 10 µF range. The voltage rating of the capacitors should be at least 5X the power supply voltage being used.

MLCC surface mount capacitors are recommended due to their smaller parasitic properties. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50 µF to 100 µF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path. A small body size X7R chip capacitor, such as

Layout Guidelines (continued)

0603 or 0805, is recommended for external bypass. A small body sized capacitor has less inductance. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 MHz to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs. This device requires only one common ground plane to connect all device related ground pins.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

At least 9 thermal vias are necessary from the device center DAP to the ground plane. They connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the LLP style package, including PCB design and manufacturing requirements, is provided in TI Application Note SNOA401.

Stencil parameters such as aperture area ratio and the fabrication process have a significant impact on paste deposition. Inspection of the stencil prior to placement of the WQFN package is highly recommended to improve board assembly yields. If the via and aperture openings are not carefully monitored, the solder may flow unevenly through the DAP. Stencil parameters for aperture opening and via locations are shown below:

Table 9. No Pullback WQFN Stencil Aperture Summary

DEVICE	PIN COUNT	MKT Dwg	PCB I/O Pad Size (mm)	PCB PITCH (mm)	PCB DAP SIZE (mm)	STENCIL I/O APERTURE (mm)	STENCIL DAP Aperture (mm)	NUMBER of DAP APERTURE OPENINGS
DS90UH928Q-Q1	48	RHS0048A	0.25 x 0.4	0.5	5.1 x 5.1	0.25 x 0.6	5.1 x 5.1	1

Figure 43 shows the PCB layout example derived from the layout design of the DS90UH928QEVM Evaluation Board. The graphic and layout description are used to determine both proper routing and proper solder techniques when designing the Serializer board.

11.1.1 CML Interconnect Guidelines

See SNLA008 and SNLA035 for full details.

- Use 100-Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - – S = space between the pair
  - – 2S = space between pairs
  - – 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500 Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the *LVDS Owner's Manual* (SNLA187).

11.2 Layout Example

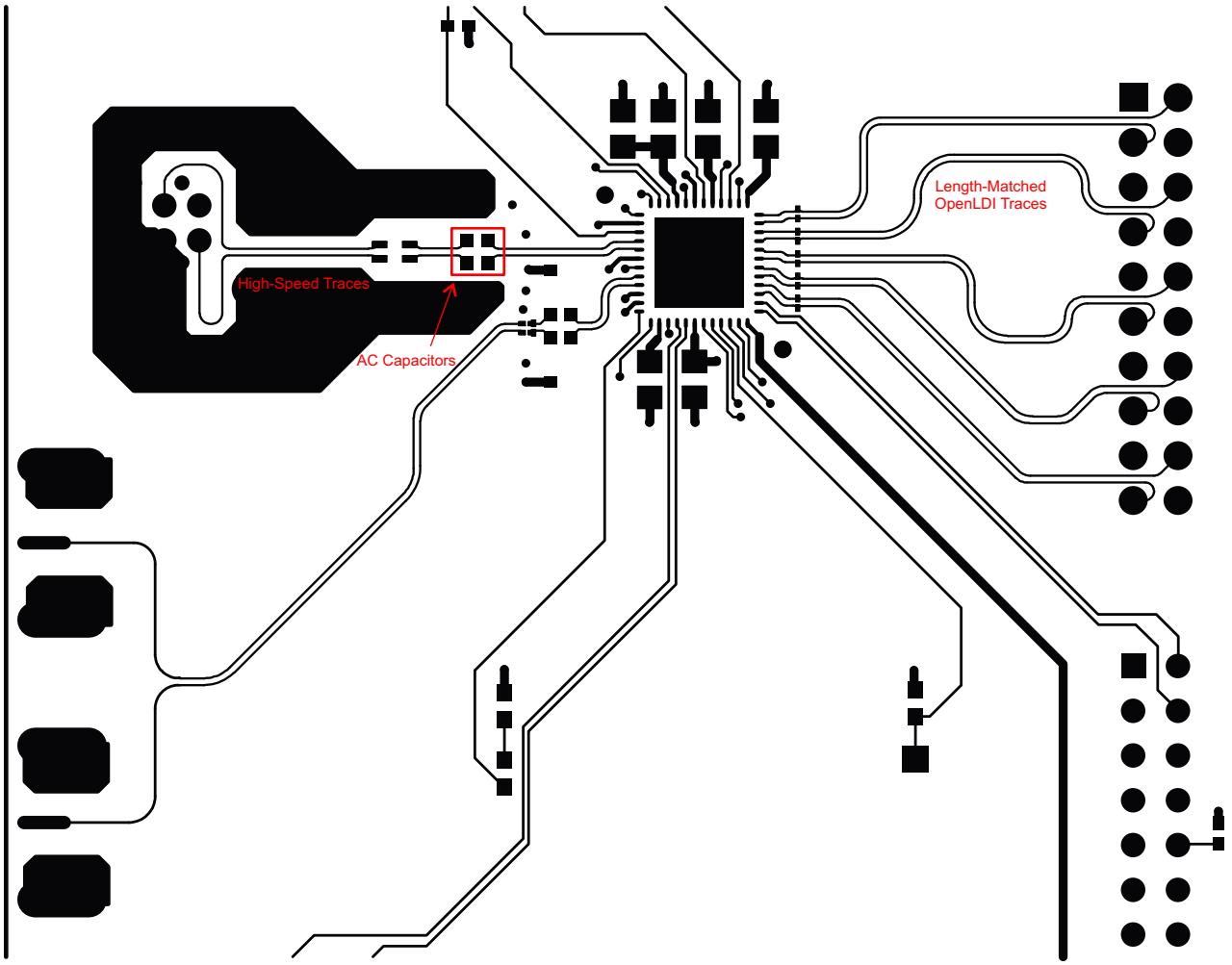


Figure 43. DS90UH928Q-Q1 Deserializer Example Layout

Layout Example (continued)

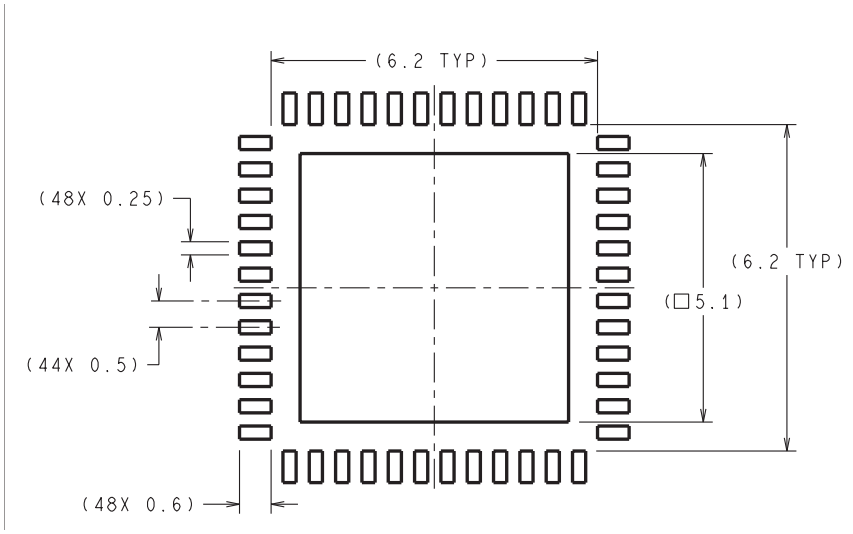


Figure 44. 48-Pin WQFN Stencil Example of Via and Opening Placement

12 器件和文档支持

12.1 文档支持

12.1.1 相关文档

相关文档如下：

- *AN-1108《通道链路 PCB 和互连设计指南》*，SNLA008
- *AN-905《传输线路 RAPIDESIGNER 操作和应用指南》*，SNLA035
- *AN-1187《无引线框架封装 (LLP)》*，SNOA401
- *《LVDS 所有者手册》*，SNLA187
- *AN-2173《通过具有双向控制通道的 FPD-Link III 进行 I2C 通信》*，SNLA131

12.2 商标

All trademarks are the property of their respective owners.

12.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

12.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、首字母缩略词和定义。

13 机械封装和可订购信息

以下页中包括机械封装和可订购信息。 这些信息是针对指定器件可提供的最新数据。 这些数据会在无通知且不对本文档进行修订的情况下发生改变。 欲获得该数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90UH928QSQ/NOPB	Active	Production	WQFN (RHS) | 48	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UH928QSQ
DS90UH928QSQ/NOPB.A	Active	Production	WQFN (RHS) | 48	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UH928QSQ
DS90UH928QSQ/NOPB.B	Active	Production	WQFN (RHS) | 48	1000 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UH928QSQ
DS90UH928QSQE/NOPB	Active	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UH928QSQ
DS90UH928QSQE/NOPB.A	Active	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UH928QSQ
DS90UH928QSQE/NOPB.B	Active	Production	WQFN (RHS) | 48	250 | SMALL T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UH928QSQ
DS90UH928QSQX/NOPB	Active	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UH928QSQ
DS90UH928QSQX/NOPB.A	Active	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UH928QSQ
DS90UH928QSQX/NOPB.B	Active	Production	WQFN (RHS) | 48	2500 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 105	UH928QSQ

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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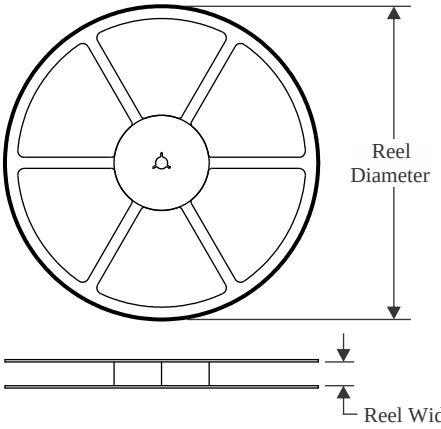
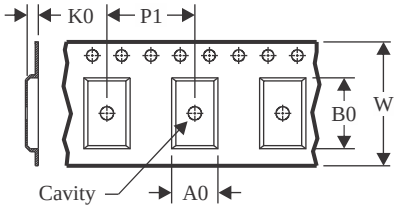
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

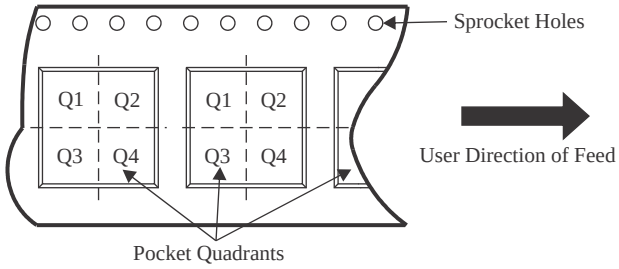


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

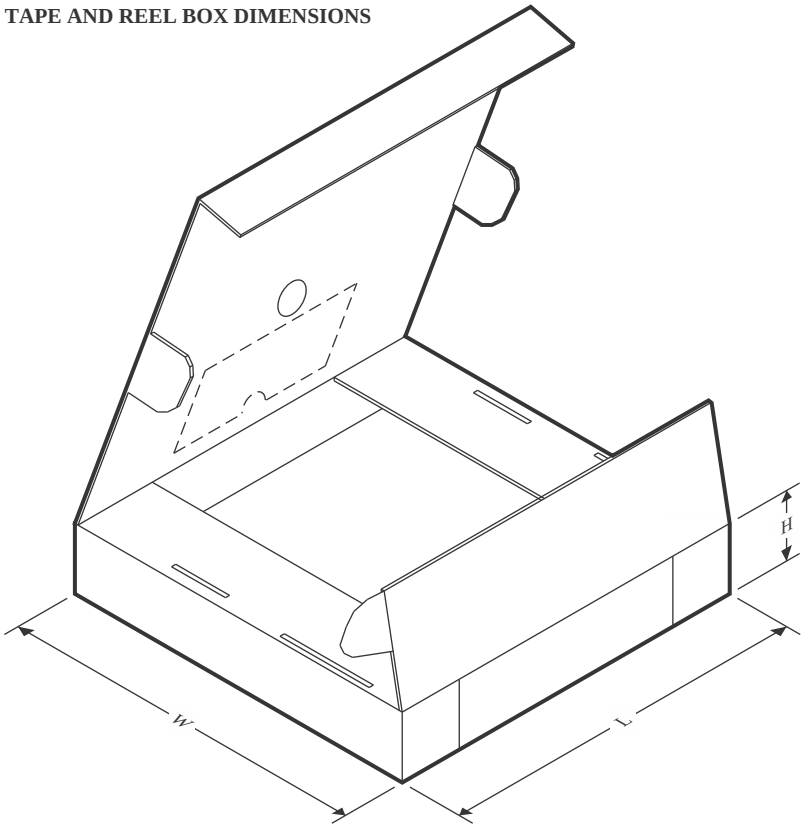
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UH928QSQ/NOPB	WQFN	RHS	48	1000	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UH928QSQE/NOPB	WQFN	RHS	48	250	178.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1
DS90UH928QSQX/NOPB	WQFN	RHS	48	2500	330.0	16.4	7.3	7.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

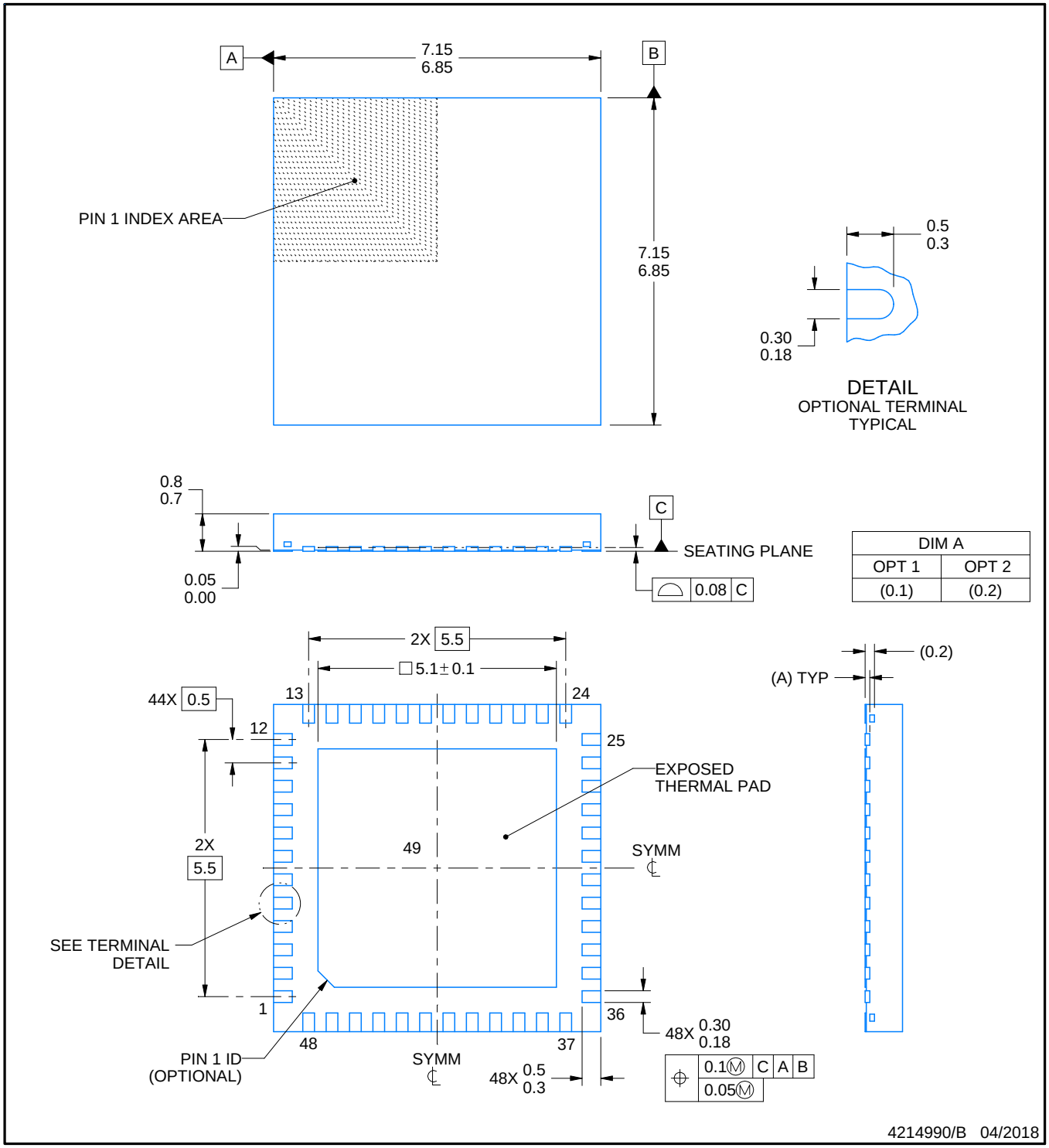
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UH928QSQ/NOPB	WQFN	RHS	48	1000	356.0	356.0	36.0
DS90UH928QSQE/NOPB	WQFN	RHS	48	250	208.0	191.0	35.0
DS90UH928QSQX/NOPB	WQFN	RHS	48	2500	356.0	356.0	36.0

PACKAGE OUTLINE

RHS0048A

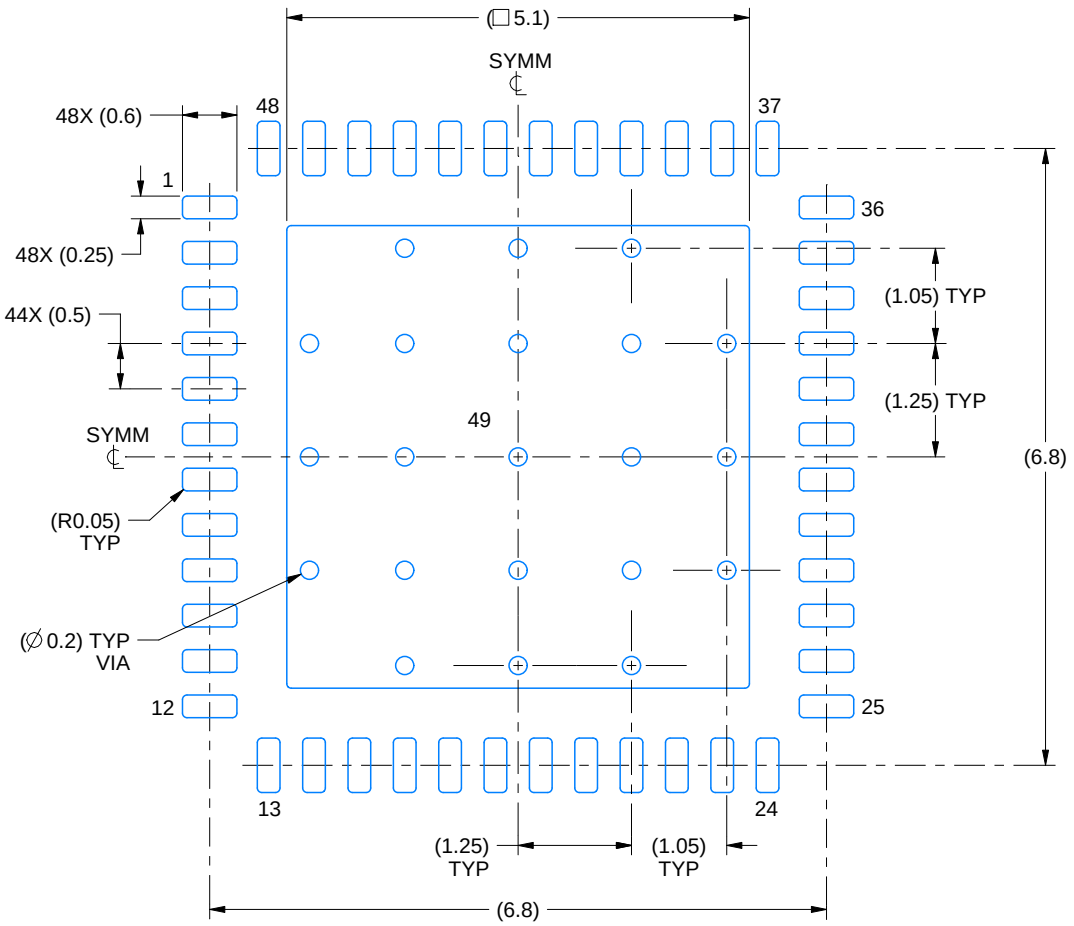
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

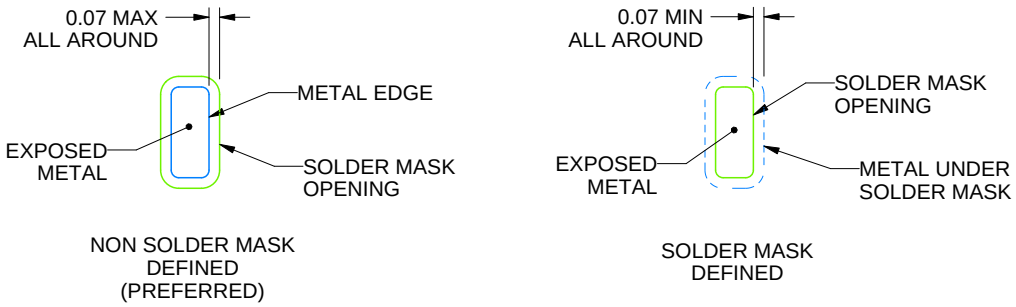


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:12X



SOLDER MASK DETAILS

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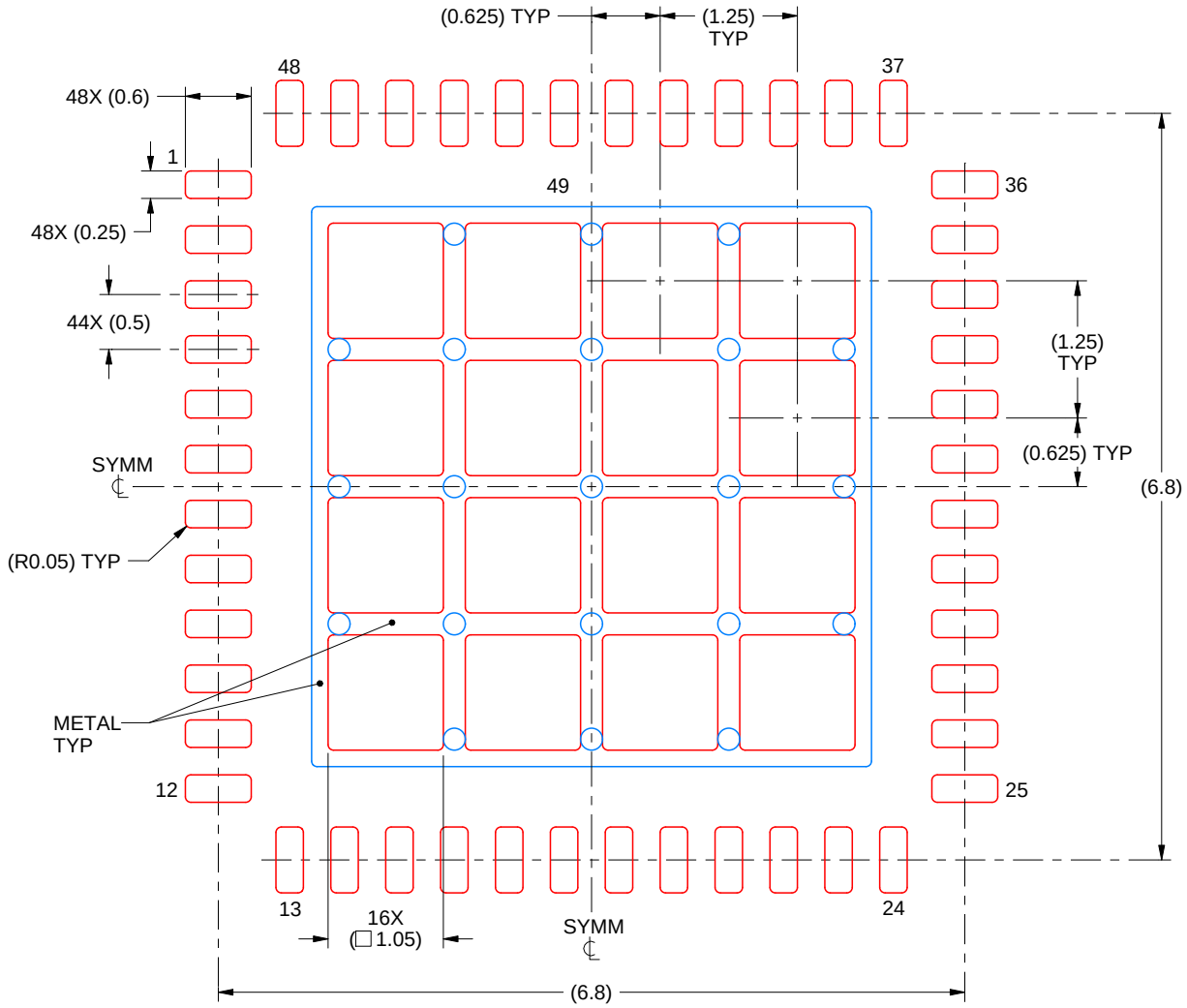
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49
68% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:15X

4214990/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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