带 HDCP 的 DS90UH947-Q1 1080p OpenLDI 到 FPD-Link III 串行器

1 特性

- 符合面向汽车应用的 AEC-Q100 标准
  - 器件温度等级 2：–40°C 至 +105°C，T_A
- 支持高达 170 MHz 的时钟频率，可实现 WUXGA (1920x1200) 和 1080p60 分辨率和 24 位色深
- 单路和双路 FPD-Link III 输出
  - 单链路：高达 96MHz 的像素时钟
  - 双链路：高达 170MHz 的像素时钟
- 单通道和双通道 OpenLDI (LVDS) 接收器
  - 可配置的 18 位 RGB 或 24 位 RGB
- 具有片上密钥存储的集成型 HDCP v1.4 密码引擎
- 高速反向通道，支持高达 2Mbps 的 GPIO
- 具有自动温度和老化补偿功能，支持长达 15 米的电缆
- 具有 1Mbps 快速模式增强版的 I2C（主/从）
- SPI 直通接口
- 向后兼容 DS90UH926Q-Q1 和 DS90UH928Q-Q1 FPD-Link III 解串器

2 应用

- 汽车信息娱乐：
  - 车载信息娱乐 (IVI) 主机和人机交互界面 (HMI) 模块
  - 后座娱乐系统
  - 数字仪表组
- 安全和监控摄像头

3 说明

DS90UH947-Q1 是一款 OpenLDI 到 FPD-Link III 桥接器件，与 FPD-Link IIIDS90UH940-Q1/DS90UH948-Q1解串器配合使用，可通过经济高效的 50Ω 单端同轴电缆或 100Ω 差分屏蔽双绞线 (STP) 电缆提供单通道或双通道高速串行流。它对 OpenLDI 输入进行串行化处理，支持高达 WUXGA 和 1080p60 的视频分辨率（24 位色深）。

FPD-Link III 接口支持通过同一条差分链路进行视频和音频数据传输以及全双工控制（包括 I2C 和 SPI 通信）。通过两个差分对实现视频数据和控制的整合可减小互连线尺寸和重量，并简化系统设计。通过使用低压差分信令、数据换序和随机生成更大限度地减少了电磁干扰 (EMI)。在向后兼容模式下，该器件在单一差分链路上最高可支持 WXGA 和 720p 分辨率（24 位色深）。

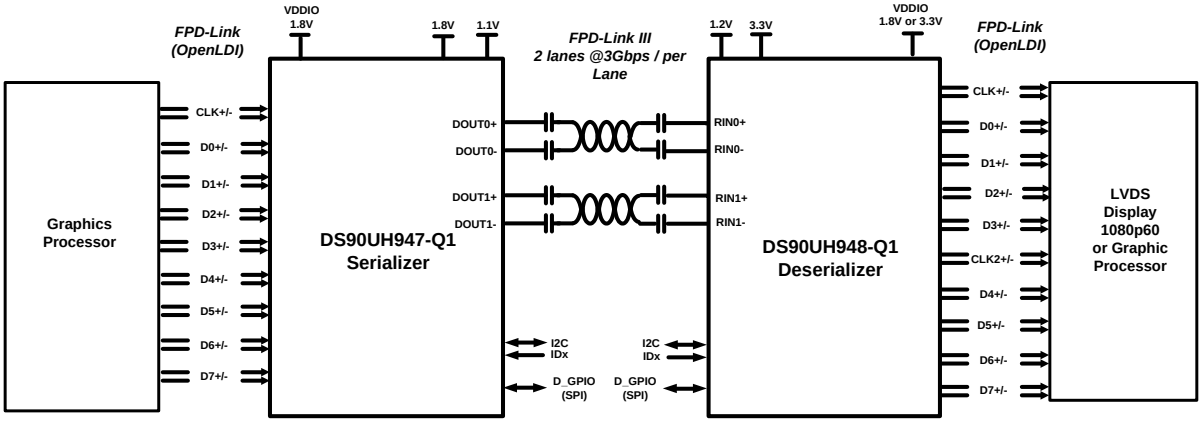
DS90UH947-Q1 支持通过外部 I2S 接口接收多通道音频。该器件接收的音频数据会被加密并通过 FPD-Link III 接口发送出去，之后再由解串器重新生成。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
DS90UH947-Q1	VQFN (64)	9.00mm x 9.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

应用 图



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4 修订历史记录

Changes from Original (November 2014) to Revision A **Page**

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- Change I_{TJIT} specification from min to max and added test conditions to the *AC Electrical Characteristics* table ... 9
- Removed t_{PLD} Max specification in the *AC Electrical Characteristics* table ... 9
- Added additional HSCC information to the *SPI Mode Configuration* section ... 22
- Changed register information about GPIO0 modes x00 and x10 ... 42
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- Added registers 0x40, 0x41, 0x42 ... 52
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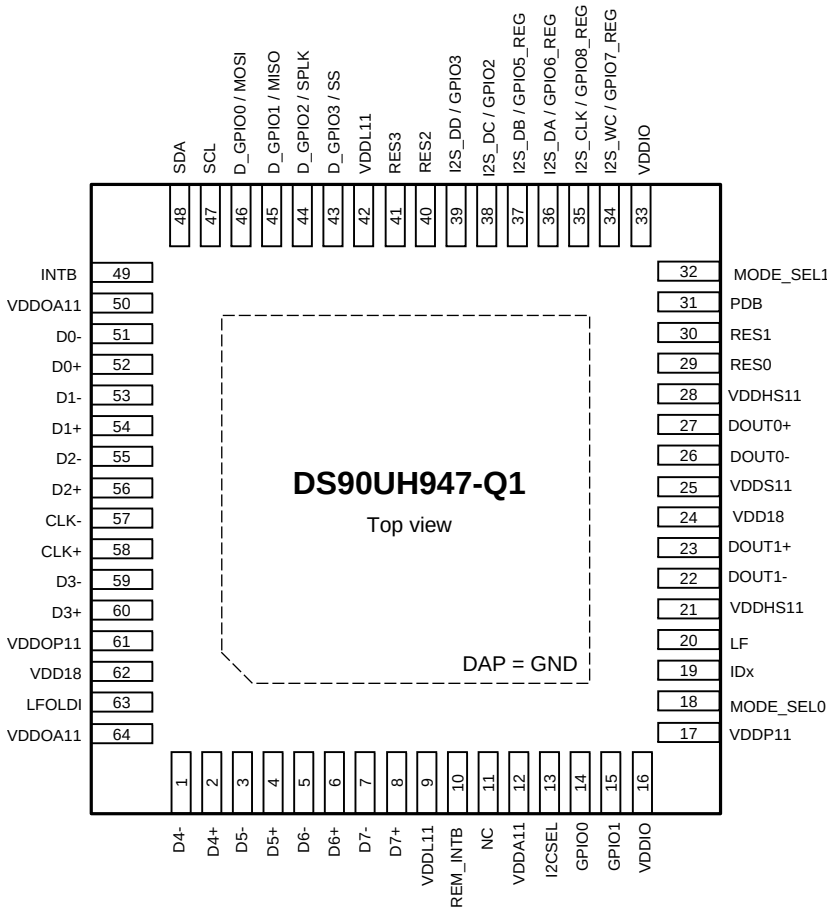
5 Pin Configuration and Functions

RGC Package
64-Pin VQFN
Top View



Pin Functions

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
LVDS INPUT PINS			
D7- D6- D5- D4- D3- D2- D1- D0-	7 5 3 1 59 55 53 51	I, LVDS	Inverting LVDS Data Inputs Each pair requires external 100-Ω differential termination for standard LVDS levels
D7+ D6+ D5+ D4+ D3+ D2+ D1+ D0+	8 6 4 2 60 56 54 52	I, LVDS	True LVDS Data Inputs Each pair requires external 100-Ω differential termination for standard LVDS levels
CLK-	57	I, LVDS	Inverting LVDS Clock Input Each pair requires external 100-Ω differential termination for standard LVDS levels

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
CLK+	58	I, LVDS	True LVDS Clock Input Each pair requires external 100-Ω differential termination for standard LVDS levels
LFOLDI	63	Analog	OpenLDI Loop Filter Connect to a 10-nF capacitor to GND
FPD-LINK III SERIAL PINS			
DOUT0-	26	I/O	FPD-Link III Inverting Output 0 The output must be coupled with a 33-nF capacitor
DOUT0+	27	I/O	FPD-Link III True Output 0 The output must be coupled with a 33-nF capacitor
DOUT1-	22	I/O	FPD-Link III Inverting Output 1 The output must be coupled with a 33-nF capacitor
DOUT1+	23	I/O	FPD-Link III True Output 1 The output must be coupled with a 33-nF capacitor
LF	20	Analog	FPD-Link III Loop Filter Connect to a 10-nF capacitor to GND
CONTROL PINS			
SDA	48	IO, Open-Drain	I2C Data Input / Output Interface Open-drain. Must have an external pullup resistor to 1.8 V or 3.3 V. **DO NOT FLOAT.** Recommended pullup: 4.7 kΩ.
SCL	47	IO, Open-Drain	I2C Clock Input / Output Interface Open-drain. Must have an external pullup resistor to 1.8 V or 3.3 V. **DO NOT FLOAT.** Recommended pullup: 4.7 kΩ.
I2CSEL	13	I, LVCMOS	I2C Voltage Level Strap Option Tie to V_{DDIO} with a 10-kΩ resistor for 1.8-V I2C operation. Leave floating for 3.3-V I2C operation. This pin is read as an input at power up.
IDx	19	I, Analog	I2C Address Select External pullup to VDD18 is required under all conditions. **DO NOT FLOAT.** Connect to external pullup and pulldown resistors to create a voltage divider.
MODE_SEL0	18	Analog	Mode Select 0 Input. Refer to Table 7.
MODE_SEL1	32	Analog	Mode Select 1 Input. Refer to Table 8.
PDB	31	I, LVCMOS	Power-Down Mode Input Pin
INTB	49	O, Open-Drain	Remote interrupt INTB = H, Normal Operation INTB = L, Interrupt Request Recommended pullup: 4.7 kΩ to V_{DDIO}. **DO NOT FLOAT.**
REM_INTB	10	O, LVCMOS	LVCMOS Output REM_INTB will directly mirror the status of the INTB_IN signal from the remote device. No separate serializer register read will be required to reset and change the status of this pin.
SPI PINS			
MOSI	46	IO, LVCMOS	SPI Master Output Slave Input Only available in Dual Link Mode. Shared with D_GPIO0
MISO	45	IO, LVCMOS	SPI Master Input Slave Output Only available in Dual Link Mode. Shared with D_GPIO1
SPLK	44	IO, LVCMOS	SPI Clock Only available in Dual Link Mode. Shared with D_GPIO2
SS	43	IO, LVCMOS	SPI Slave Select Only available in Dual Link Mode. Shared with D_GPIO3
HIGH-SPEED GPIO PINS			
D_GPIO0	46	IO, LVCMOS	High-Speed GPIO0 Only available in Dual Link Mode. Shared with MOSI
D_GPIO1	45	IO, LVCMOS	High-Speed GPIO1 Only available in Dual Link Mode. Shared with MISO
D_GPIO2	44	IO, LVCMOS	High-Speed GPIO2 Only available in Dual Link Mode. Shared with SPLK

Pin Functions (continued)

PIN		I/O, TYPE	DESCRIPTION
NAME	NO.		
D_GPIO3	43	IO, LVCMOS	High-Speed GPIO3 Only available in Dual Link Mode. Shared with SS
GPIO PINS			
GPIO0	14	IO, LVCMOS	General-Purpose Input/Output 0
GPIO1	15	IO, LVCMOS	General-Purpose Input/Output 1
GPIO2	38	IO, LVCMOS	General-Purpose Input/Output 2 Shared with I2S_DC
GPIO3	39	IO, LVCMOS	General-Purpose Input/Output 3 Shared with I2S_DD
REGISTER-ONLY GPIO PINS			
GPIO5_REG	37	IO, LVCMOS	General-Purpose Input/Output 5 Local register control only. Shared with I2S_DB
GPIO6_REG	36	IO, LVCMOS	General-Purpose Input/Output 6 Local register control only. Shared with I2S_DA
GPIO7_REG	34	IO, LVCMOS	General-Purpose Input/Output 7 Local register control only. Shared with I2S_WC
GPIO8_REG	35	IO, LVCMOS	General-Purpose Input/Output 8 Local register control only. Shared with I2S_CLK
SLAVE MODE LOCAL I2S CHANNEL PINS			
I2S_WC	34	I, LVCMOS	Slave Mode I2S Word Clock Input. Shared with GPIO7_REG
I2S_CLK	35	I, LVCMOS	Slave Mode I2S Clock Input. Shared with GPIO8_REG
I2S_DA	36	I, LVCMOS	Slave Mode I2S Data Input. Shared with GPIO6_REG
I2S_DB	37	I, LVCMOS	Slave Mode I2S Data Input. Shared with GPIO5_REG
I2S_DC	38	I, LVCMOS	Slave Mode I2S Data Input. Shared with GPIO2
I2S_DD	39	I, LVCMOS	Slave Mode I2S Data Input. Shared with GPIO3
POWER AND GROUND PINS			
VDD18	24 62	Power	1.8-V (±5%) supply. Refer to Figure 35 or Figure 36.
VDDOA11	50 64	Power	1.1-V (±5%) supply. Refer to Figure 35 or Figure 36.
VDDA11	12	Power	1.1-V (±5%) supply. Refer to Figure 35 or Figure 36.
VDDHS11	21 28	Power	1.1-V (±5%) supply. Refer to Figure 35 or Figure 36.
VDDL11	9 42	Power	1.1-V (±5%) supply. Refer to Figure 35 or Figure 36.
VDDOP11	61	Power	1.1-V (±5%) supply. Refer to Figure 35 or Figure 36.
VDDP11	17	Power	1.1-V (±5%) supply. Refer to Figure 35 or Figure 36.
VDDS11	25	Power	1.1-V (±5%) supply. Refer to Figure 35 or Figure 36.
VDDIO	16 33	Power	1.8-V (±5%) LVCMOS I/O Power. Refer to Figure 35 or Figure 36.
GND	Thermal Pad		Ground.
OTHER PINS			
RES0 RES2 RES3	29 40 41		Reserved. Tie to GND.
RES1	30		Reserved. Connect with 50Ω to GND.
NC	11		No connect. Leave floating Do not connect to VDD or GND.

6 Specifications

6.1 Absolute Maximum Ratings

See (1)(2)(2)

		MIN	MAX	UNIT
V_{DD11}	Supply Voltage	–0.3	1.7	V
V_{DD18}	Supply Voltage	–0.3	2.5	V
V_{DDIO}	Supply Voltage	–0.3	2.5	V
	OpenLDI Inputs	–0.3	2.75	V
	LVCMOS I/O Voltage	–0.3	V_{DDIO} + 0.3	V
	1.8-V Tolerant I/O	–0.3	2.5	V
	3.3-V Tolerant I/O	–0.3	4.0	V
	FPD-Link III Output Voltage	−0.3	1.7	V
	Junction Temperature		150	°C
T_{stg}	Storage Temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For soldering specifications, see product folder at www.ti.com and *Absolute Maximum Ratings for Soldering* (SNOA549).

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2		±2000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C5		±750	
		(IEC 61000-4-2) R_D = 330 Ω, C_S = 150 pF	Air Discharge (D_{OUT0+}, D_{OUT0-}, D_{OUT1+}, D_{OUT1-})	±15000	
			Contact Discharge (D_{OUT0+}, D_{OUT0-}, D_{OUT1+}, D_{OUT1-})	±8000	
		(ISO10605) R_D = 330 Ω, C_S = 150 pF R_D = 2 kΩ, C_S = 150 pF or 330 pF	Air Discharge (D_{OUT0+}, D_{OUT0-}, D_{OUT1+}, D_{OUT1-})	±15000	
			Contact Discharge (D_{OUT0+}, D_{OUT0-}, D_{OUT1+}, D_{OUT1-})	±8000	

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{DD11}	Supply Voltage	1.045	1.1	1.155	V
V_{DD18}	Supply Voltage	1.71	1.8	1.89	V
V_{DDIO}	LVCMOS Supply Voltage	1.71	1.8	1.89	V
	V_{DDI2C}, 1.8-V Operation	1.71	1.8	1.89	V
	V_{DDI2C}, 3.3-V Operation	3.135	3.3	3.465	V
T_A	Operating Free Air Temperature	−40	25	105	°C
T_{CLH1}	Allowable ending ambient temperature for continuous PLL lock when ambient temperature is rising under the following condition: −40°C ≤ starting ambient temperature (T_S) < 0°C.(1)	T_S		80	°C
T_{CLH2}	Allowable ending ambient temperature for continuous PLL lock when ambient temperature is rising under the following condition: 0°C ≤ starting ambient temperature (T_S) ≤ 105°C.(1)	T_S		105	°C

(1) The input and output PLLs are calibrated at the ambient start up temperature (T_S) when the device is powered on or when reset using the PDB pin. The PLLs will stay locked up to the specified ending temperature. A more detailed description can be found in “Handling System Temperature Ramps on the DS90Ux949, DS90Ux929 and DS90Ux947”.

Recommended Operating Conditions (continued)

		MIN	NOM	MAX	UNIT
T_{CHL1}	Allowable ending ambient temperature for continuous PLL lock when ambient temperature is rising under the following condition: 45°C < starting ambient temperature (T_S) ≤ 105°C.(1)	25		T_S	°C
T_{CHL2}	Allowable ending ambient temperature for continuous PLL lock when ambient temperature is rising under the following condition: −20°C ≤ starting ambient temperature (T_S) ≤ 45°C.(1)	T_S − 20		T_S	°C
	OpenLDI Clock Frequency (Single Link)	25		170	MHz
	OpenLDI Clock Frequency (Dual Link)	50		170	MHz

6.4 Thermal Information

THERMAL METRIC(1)		DS90UH947-Q1 VQFN 64 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	25.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	11.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report (SPRA953).

6.5 DC Electrical Characteristics

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
1.8-V LVCMOS I/O							
V_{IH}	High Level Input Voltage		PDB, I2CSEL,D_GPIO0/ MOSI, D_GPIO1/MISO, D_GPIO2/SPLK, D_GPIO3/SS, I2S_DC/GPIO2, I2S_DD/GPIO3, I2S_DB/GPIO5_REG, I2S_DA/GPIO6_REG, I2S_CLK/GPIO8_REG, I2S_WC/GPIO7_REG	0.65 × V_{DDIO}			V
V_{IL}	Low Level Input Voltage			0		0.35 × V_{DDIO}	V
I_{IN}	Input Current	V_{IN} = 0 V or 1.89 V		−10		10	µA
V_{OH}	High Level Output Voltage	I_{OH} = −4 mA	Same as above	0.7 × V_{DDIO}		V_{DDIO}	V
V_{OL}	Low Level Output Voltage	I_{OL} = 4 mA		GND		0.3 × V_{DDIO}	V
I_{OS}	Output Short-Circuit Current	V_{OUT} = 0 V			-30		mA
I_{OZ}	TRI-STATE™ Output Current	V_{OUT} = 0 V or V_{DDIO}, PDB = L		−10		10	µA
OpenLDI INPUTS							
$\|V_{ID}\|$	Differential Input Voltage		D[7:0], CLK	100		600	mV
V_{CM}	Common-Mode Voltage		D[7:0]	0		2.4	V

DC Electrical Characteristics (continued)

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
I_{IN}	Input Current	PDB = H		–10		10	µA

DC Electrical Characteristics (continued)

over recommended operating supply and temperature ranges (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
FPD-LINK III DIFFERENTIAL DRIVER							
V_{ODp-p}	Output Differential Voltage		DOUT[1:0]+, DOUT[1:0]-	900		1200	mV_{p-p}
ΔV_{OD}	Output Voltage Unbalance				1	50	mV
V_{OS}	Output Differential Offset Voltage				550		mV
ΔV_{OS}	Offset Voltage Unbalance				1	50	mV
I_{OS}	Output Short Circuit Current	FPD-Link III Outputs = 0 V			-20		mA
R_T	Termination Resistance	Single-ended		40	50	60	Ω
SUPPLY CURRENT							
I_{DD11}	Supply Current, Normal Operation	Checkerboard Pattern			335	469	mA
I_{DD18}					50	75	mA
Total Power	Total Power, Normal Operation	Checkerboard Pattern			459	684	mW
I_{DDZ}	Supply Current, Power Down Mode	PDB = L			5	15	mA
I_{DDZ18}					5	15	mA

6.6 AC Electrical Characteristics

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
GPIO FREQUENCY (1)							
$R_{b,FC}$	Forward Channel GPIO Frequency	Single-Lane, CLK = 25 MHz - 96 MHz	GPIO[3:0], D_GPIO[3:0]			0.25 × CLK	MHz
		Dual-Lane, CLK/2 = 25 MHz - 85 MHz				0.125 × CLK	
$t_{GPIO,FC}$	GPIO Pulse Width, Forward Channel	Single-Lane, CLK = 25 MHz - 96 MHz	GPIO[3:0], D_GPIO[3:0]	>2 / CLK			s
		Dual-Lane, CLK/2 = 25 MHz - 85 MHz		>2 / (CLK/2)			
OpenLDI INPUTS							
I_{TJIT} (2)	Input Total Jitter Tolerance	Jitter frequency ≤ CLK/40	CLK±, D[7:0]±			0.2	UI_{OLDI} (3)
FPD-LINK III OUTPUT							
t_{LHT}	Low Voltage Differential Low-to-High Transition Time				80		ps
t_{HLT}	Low Voltage Differential High-to-Low Transition Time				80		ps
t_{XZD}	Output Active to OFF Delay	PDB = L			100		ns
t_{PLD}	Lock Time (OpenLDI Rx)				5		ms
t_{SD}	Delay — Latency		CLK±		294		T (4)

(1) Back channel rates are available on the companion deserializer datasheet.
(2) Includes data to clock skew, pulse position variation.
(3) One bit period of the OpenLDI input.
(4) Video pixel clock period when device in dual pixel OpenLDI input and dual FPD-Link III output modes.

AC Electrical Characteristics (continued)

Over recommended operating supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	PIN/FREQ.	MIN	TYP	MAX	UNIT
t_{DJIT}	Output Total Jitter(Figure 6)	Random Pattern	Single-Lane: High pass filter CLK/20		0.3		UI_{FPD3} (5)
			Dual-lane: High pass filter CLK/40				
λ_{STXBW}	Jitter Transfer Function (-3-dB Bandwidth)				1		MHz
δ_{STX}	Jitter Transfer Function Peaking				0.1		dB

(5) One bit period of the serializer output.

6.7 DC and AC Serial Control Bus Characteristics

over V_{DDI2C} supply and temperature ranges unless otherwise specified. V_{DDI2C} can be 1.8V (±5%) or 3.3V (±5%) (refer to I2CSEL pin description for 1.8-V or 3.3-V operation).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IH,I2C}$	Input High Level, I2C	SDA and SCL, V_{DDI2C} = 1.8 V	0.7 × V_{DDI2C}			V
		SDA and SCL, V_{DDI2C} = 3.3 V	0.7 × V_{DDI2C}			V
$V_{IL,I2C}$	Input Low Level Voltage, I2C	SDA and SCL, V_{DDI2C} = 1.8 V			0.3 × V_{DDI2C}	V
		SDA and SCL, V_{DDI2C} = 3.3 V			0.3 × V_{DDI2C}	V
V_{HY}	Input Hysteresis, I2C	SDA and SCL, V_{DDI2C} = 1.8 V or 3.3 V		>50		mV
$V_{OL,I2C}$	Output Low Level, I2C	SDA and SCL, V_{DDI2C} = 1.8-V, Fast-Mode, 3-mA Sink Current	GND		0.2 × V_{DDI2C}	V
		SDA and SCL, V_{DDI2C} = 3.3-V, 3-mA Sink Current	GND		0.4	V
$I_{IN,I2C}$	Input Current, I2C	SDA and SCL, V_{DDI2C} = 0 V	-10		+10	µA
		SDA and SCL, V_{DDI2C} = V_{DD18} or V_{DD33}	-10		10	µA
$C_{IN,I2C}$	Input Capacitance, I2C	SDA and SCL		5		pF

6.8 Recommended Timing for the Serial Control Bus

over I^2C supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL Clock Frequency	Standard-Mode	>0		100	kHz
		Fast-Mode	>0		400	kHz
		Fast-Mode Plus	>0		1	MHz
t_{LOW}	SCL Low Period	Standard-Mode	4.7			µs
		Fast-Mode	1.3			µs
		Fast-Mode Plus	0.5			µs
t_{HIGH}	SCL High Period	Standard-Mode	4.0			µs
		Fast-Mode	0.6			µs
		Fast-Mode Plus	0.26			µs
$t_{HD;STA}$	Hold time for a start or a repeated start condition	Standard-Mode	4.0			µs
		Fast-Mode	0.6			µs
		Fast-Mode Plus	0.26			µs

Recommended Timing for the Serial Control Bus (continued)

over I^2C supply and temperature ranges unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{SU;STA}$	Set Up time for a start or a repeated start condition	Standard-Mode	4.7			µs
		Fast-Mode	0.6			µs
		Fast-Mode Plus	0.26			µs
$t_{HD;DAT}$	Data Hold Time	Standard-Mode	0			µs
		Fast-Mode	0			µs
		Fast-Mode Plus	0			µs
$t_{SU;DAT}$	Data Set Up Time	Standard-Mode	250			ns
		Fast-Mode	100			ns
		Fast-Mode Plus	50			ns
$t_{SU;STO}$	Set Up Time for STOP Condition	Standard-Mode	4.0			µs
		Fast-Mode	0.6			µs
		Fast-Mode Plus	0.26			µs
t_{BUF}	Bus Free Time Between STOP and START	Standard-Mode	4.7			µs
		Fast-Mode	1.3			µs
		Fast-Mode Plus	0.5			µs
t_r	SCL and SDA Rise Time,	Standard-Mode			1000	ns
		Fast-Mode			300	ns
		Fast-Mode Plus			120	ns
t_f	SCL and SDA Fall Time,	Standard-Mode			300	ns
		Fast-Mode			300	ns
		Fast-Mode Plus			120	ns
t_{SP}	Input Filter	Fast-Mode			50	ns
		Fast-Mode Plus			50	ns

6.9 Timing Diagrams

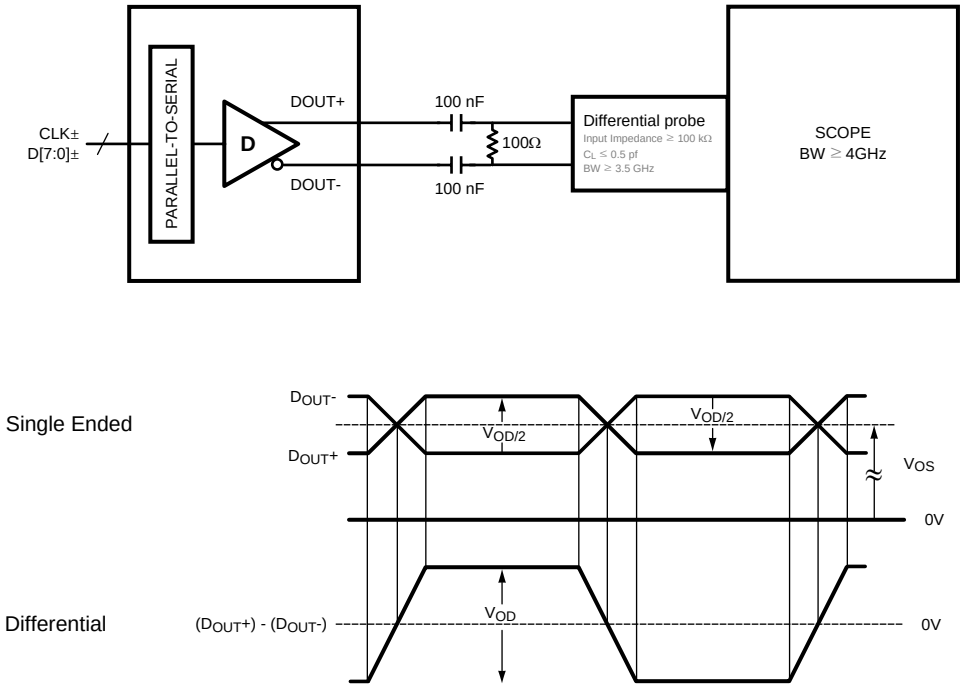


Figure 1. Serializer V_{OD} Output

Timing Diagrams (continued)

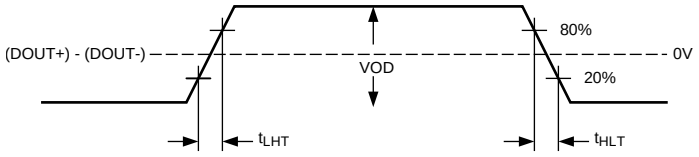


Figure 2. Output Transition Times

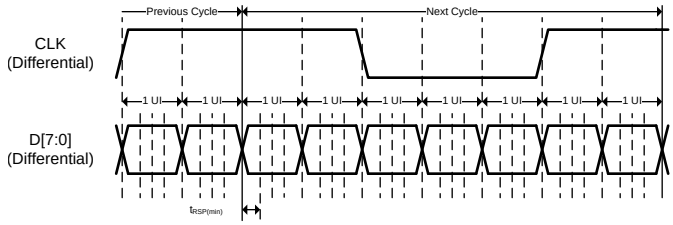


Figure 3. OpenLDI Input Clock and Data Jitter

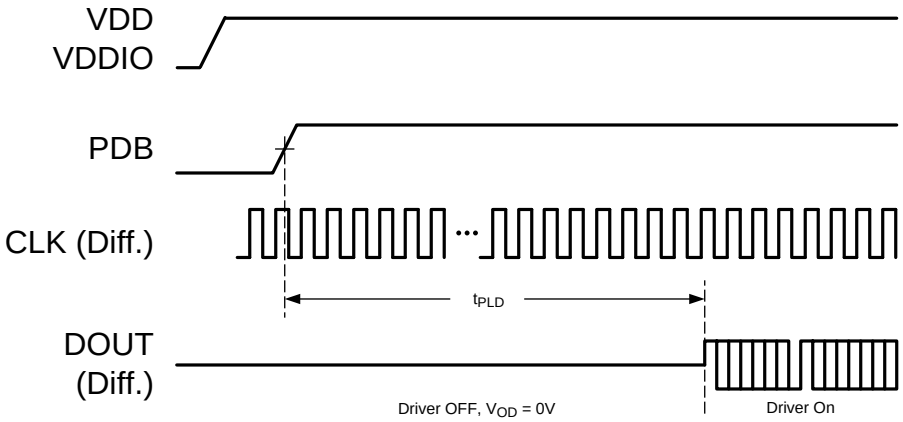


Figure 4. Serializer Lock Time

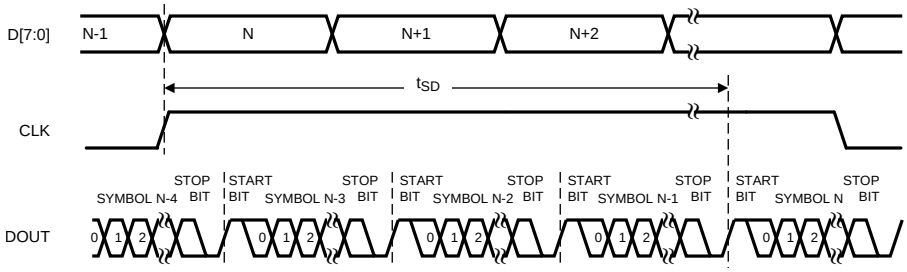


Figure 5. Latency Delay

Timing Diagrams (continued)

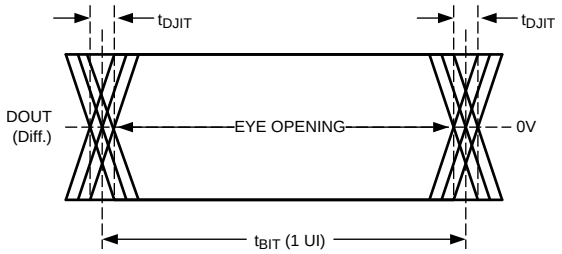


Figure 6. Serializer Output Jitter

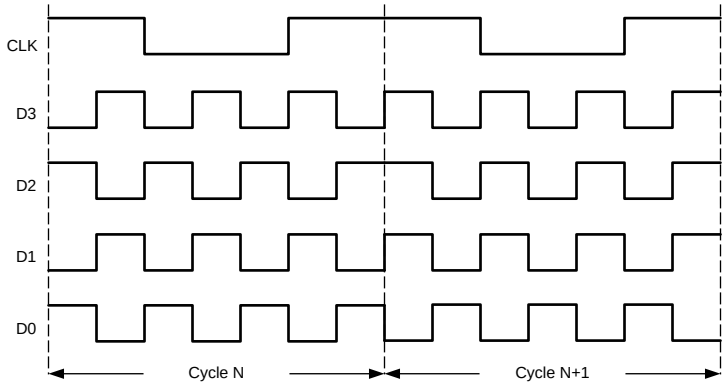


Figure 7. Single OpenLDI Checkerboard Data Pattern

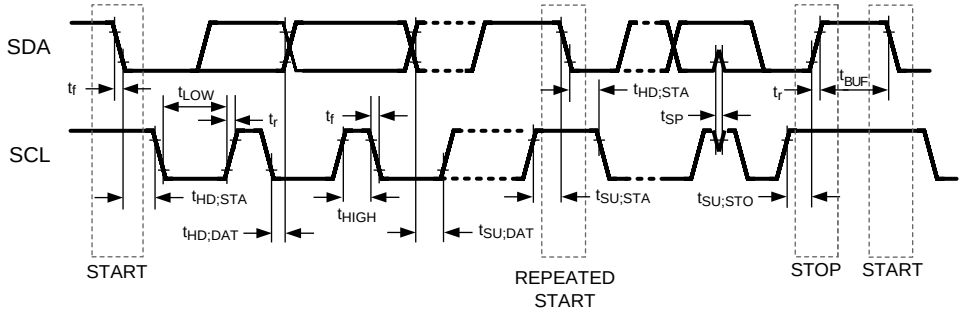


Figure 8. Serial Control Bus Timing Diagram

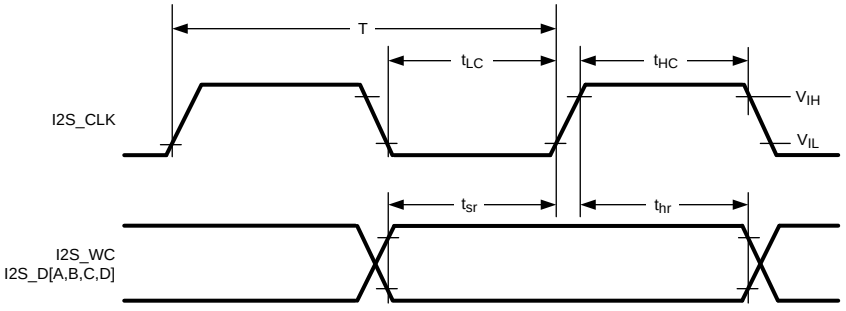


Figure 9. I2S Timing Diagram

6.10 Typical Characteristics

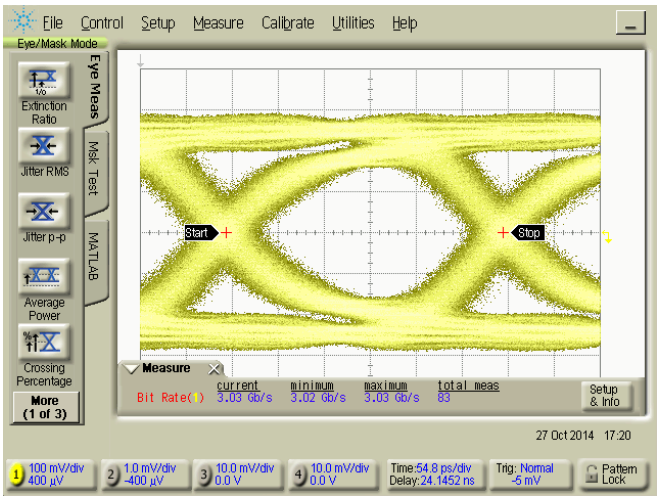


Figure 10. Serializer Output at 2.975 Gbps (85-MHz OpenLDI Clock)

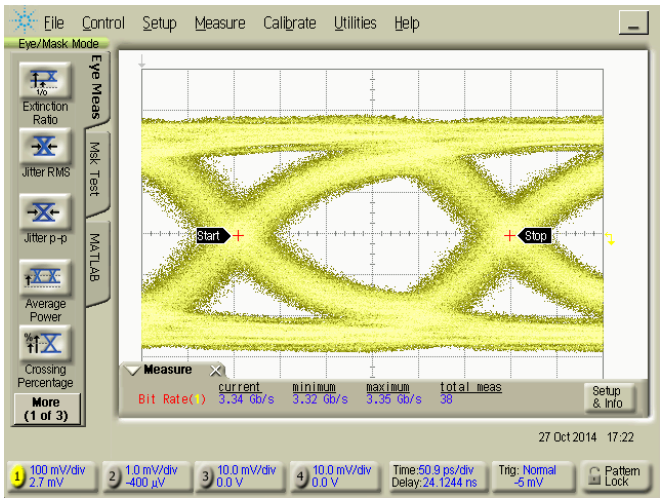


Figure 11. Serializer Output at 3.36 Gbps (96-MHz OpenLDI Clock)

7 Detailed Description

7.1 Overview

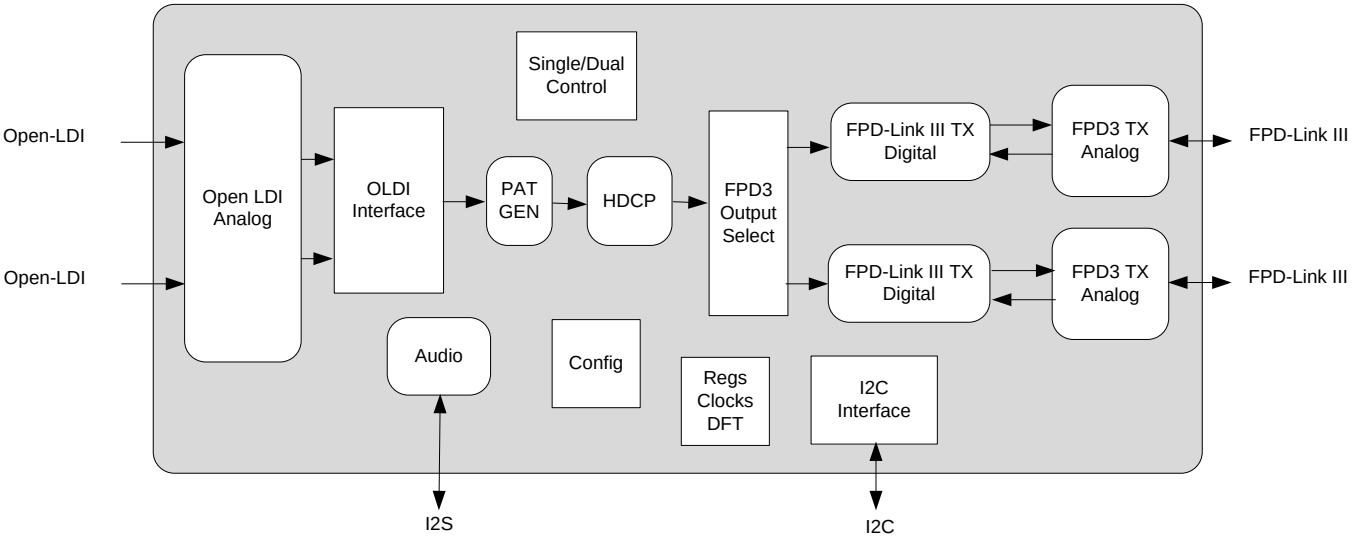
The DS90UH947-Q1 converts a single or dual FPD-Link (Open LDI) interface (up to 8 LVDS lanes + 1 clock) to an FPD-Link III interface. This device transmits a 35-bit symbol over a single serial pair operating up to 3.36Gbps line rate, or two serial pairs operating up to 2.975Gbps line rate. The serial stream contains an embedded clock, video control signals, RGB video data, and audio data. The payload is DC-balanced to enhance signal quality and support AC coupling.

The DS90UH947-Q1 serializer is intended for use with a DS90UH926Q-Q1, DS90UH928Q-Q1, DS90UH940-Q1, DS90UH948-Q1 deserializer.

The DS90UH947-Q1 serializer and companion deserializer incorporate an I2C compatible interface. The I2C compatible interface allows programming of serializer or deserializer devices from a local host controller. In addition, the devices incorporate a bidirectional control channel (BCC) that allows communication between serializer/deserializer as well as remote I2C slave devices.

The bidirectional control channel (BCC) is implemented via embedded signaling in the high-speed forward channel (serializer to deserializer) combined with lower speed signaling in the reverse channel (deserializer to serializer). Through this interface, the BCC provides a mechanism to bridge I2C transactions across the serial link from one I2C bus to another. The implementation allows for arbitration with other I2C compatible masters at either side of the serial link.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 High-Speed Forward Channel Data Transfer

The High-Speed Forward Channel is composed of 35 bits of data containing RGB data, sync signals, I2C, GPIOs, and I2S audio transmitted from serializer to deserializer. Figure 12 shows the serial stream per clock cycle. This data payload is optimized for signal transmission over an AC coupled link. Data is randomized, balanced and scrambled.

Figure 12. FPD-Link III Serial Stream

Feature Description (continued)

The device supports OpenLDI clocks in the range of 25 MHz to 96 MHz over one lane, or 50 MHz to 170 MHz over two lanes. The FPD-Link III serial stream rate is 3.36 Gbps maximum (875 Mbps minimum) , or 2.975 Gbps maximum per lane (875 Mbps minimum) when transmitting over both lanes.

7.3.2 Back Channel Data Transfer

The Backward Channel provides bidirectional communication between the display and host processor. The information is carried from the deserializer to the serializer as serial frames. The back channel control data is transferred over both serial links along with the high-speed forward data, DC balance coding and embedded clock information. This architecture provides a backward path across the serial link together with a high-speed forward channel. The back channel contains the I2C, CRC and 4 bits of standard GPIO information with 5, 10, or 20 Mbps line rate (configured by the compatible deserializer).

7.3.3 FPD-Link III Port Register Access

The DS90UH947-Q1 contains two downstream ports, therefore some registers must be duplicated to allow control and monitoring of the two ports. To facilitate this, a TX_PORT_SEL register controls access to the two sets of registers. Registers that are shared between ports (not duplicated) will be available independent of the settings in the TX_PORT_SEL register.

Setting the TX_PORT0_SEL or TX_PORT1_SEL bit will allow a read of the register for the selected port. If both bits are set, port1 registers will be returned. Writes will occur to ports for which the select bit is set, allowing simultaneous writes to both ports if both select bits are set.

Setting the PORT1_I2C_EN bit will enable a second I^2C slave address, allowing access to the second port registers through the second I^2C address. If this bit is set, the TX_PORT0_SEL and TX_PORT1_SEL bits will be ignored.

7.3.4 OpenLDI Input Frame and Color Bit Mapping Select

The DS90UH947-Q1 can be configured to accept 24-bit color (8-bit RGB) with 2 different mapping schemes, shown in Figure 13 and Figure 14. Each frame corresponds to a single pixel clock (PCLK) cycle. The LVDS clock input to CLK± follows a 4:3 duty cycle scheme, with each 28-bit pixel frame starting with two LVDS bit clock periods high, three low, and ending with two high. The mapping scheme is controlled by MAPSEL strap option or by Register (Table 10).

Feature Description (continued)

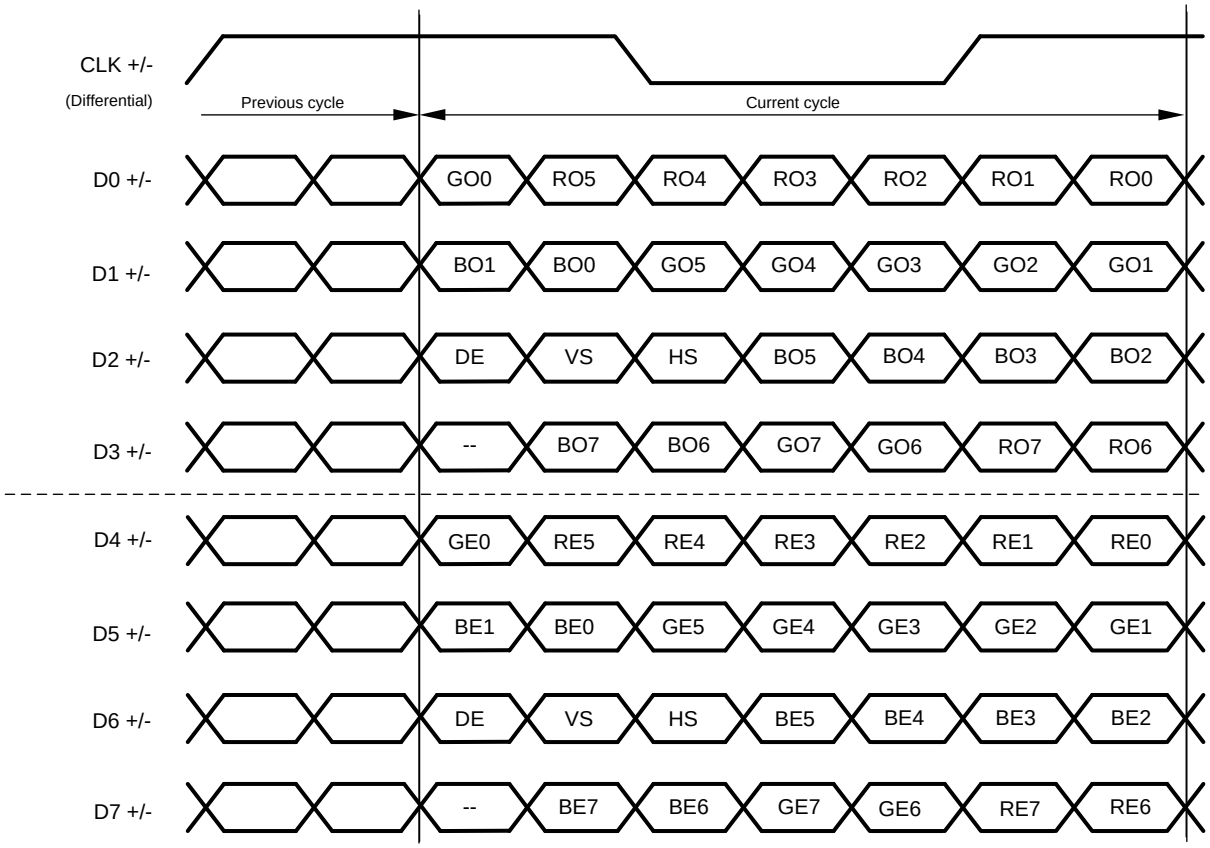


Figure 13. 24-Bit Color Dual Pixel Mapping: MSBs on D3/D7 (OpenLDI Mapping)

Feature Description (continued)

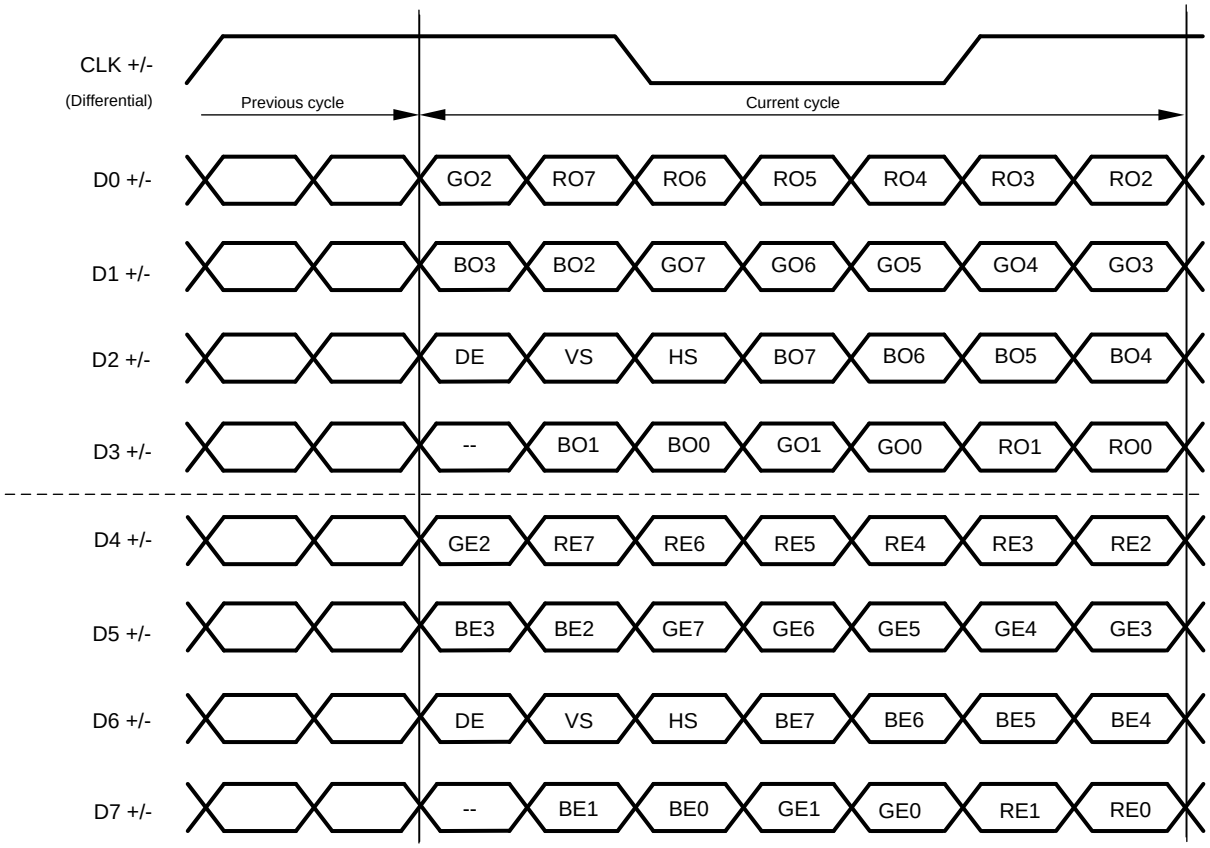


Figure 14. 24-Bit Color Dual Pixel Mapping: LSBs on D3/D7 (SPWG Mapping)

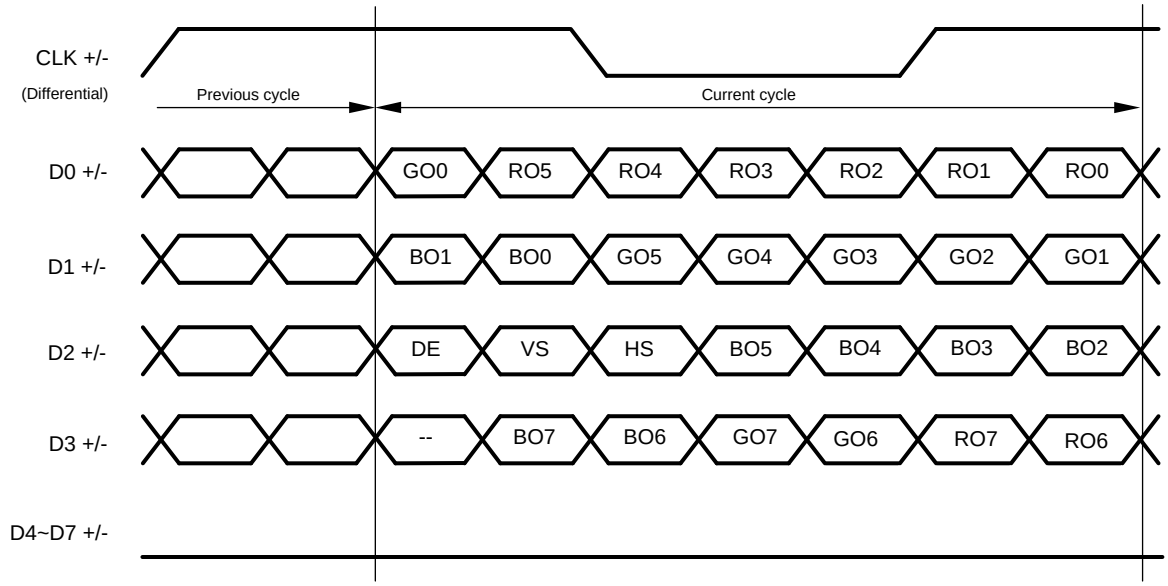


Figure 15. 24-Bit Color Single Pixel Mapping: MSBs on D3 (OpenLDI Mapping)

Feature Description (continued)

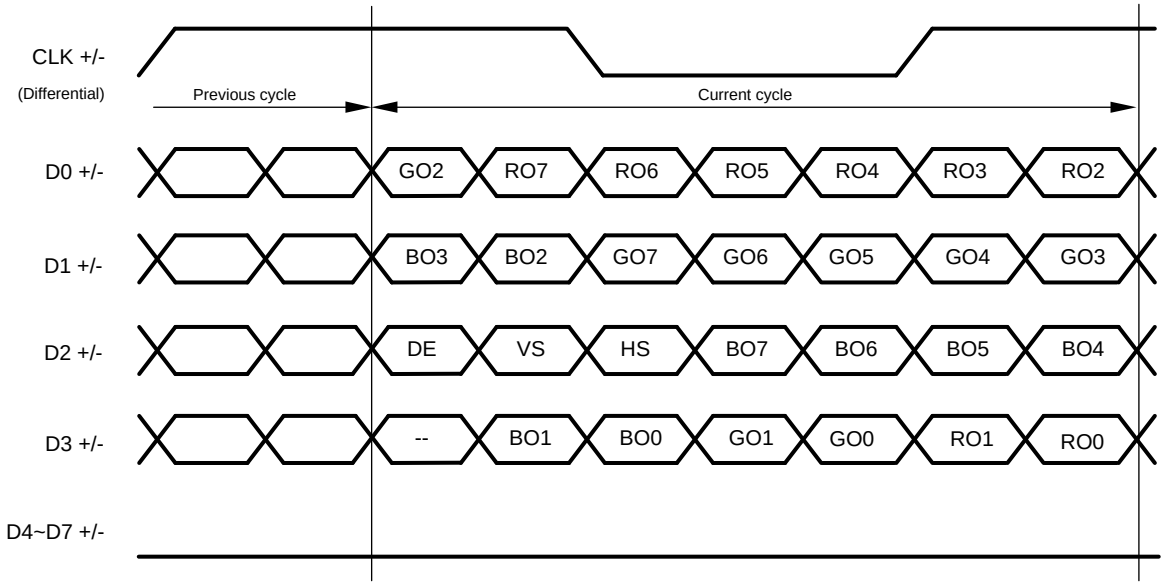


Figure 16. 24-Bit Color Single Pixel Mapping: LSBs on D3 (SPWG Mapping)

7.3.5 Video Control Signals

The video control signal bits embedded in the high-speed FPD-Link LVDS are subject to certain limitations relative to the video pixel clock period (PCLK). By default, the DS90UH947-Q1 applies a minimum pulse width filter on these signals to help eliminate spurious transitions.

Normal Mode Control Signals (VS, HS, DE) have the following restrictions:

- Horizontal Sync (HS): The video control signal pulse width must be 3 PCLKs or longer when the Control Signal Filter (register bit 0x03[4]) is enabled (default). Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). See Table 10. HS can have at most two transitions per 130 PCLKs.
- Vertical Sync (VS): The video control signal pulse is limited to 1 transition per 130 PCLKs. Thus, the minimum pulse width is 130 PCLKs.
- Data Enable Input (DE): The video control signal pulse width must be 3 PCLKs or longer when the Control Signal Filter (register bit 0x03[4]) is enabled (default). Disabling the Control Signal Filter removes this restriction (minimum is 1 PCLK). See Table 10. DE can have at most two transitions per 130 PCLKs.

7.3.6 Power Down (PDB)

The Serializer has a PDB input pin to ENABLE or POWER DOWN the device. This pin may be controlled by an external device, or through V_{DDIO}, where V_{DDIO} = 1.71 V to 1.89 V. To save power, disable the link when the display is not needed (PDB = LOW). Ensure that this pin is not driven HIGH before all power supplies have reached final levels. When PDB is driven low, ensure that the pin is driven to 0V for at least 3ms before releasing or driving high. In the case where PDB is pulled up to V_{DDIO} directly, a 10-kΩ pull-up resistor and a >10µF capacitor to ground are required (See *Power-Up Requirements and PDB Pin*).

Toggling PDB low will POWER DOWN the device and RESET all control registers to default. During this time, PDB must be held low for a minimum of 3ms before going high again.

7.3.7 Serial Link Fault Detect

The DS90UH947-Q1 can detect fault conditions in the FPD-Link III interconnect. If a fault condition occurs, the Link Detect Status is 0 (cable is not detected) on bit 0 of address 0x0C (Table 10). The DS90UH947-Q1 will detect any of the following conditions:

1. Cable open
2. “+” to “-” short

Feature Description (continued)

3. ”+” to GND short
4. ”-” to GND short
5. ”+” to battery short
6. ”-” to battery short
7. Cable is linked incorrectly (DOUT+/DOUT- connections reversed)

Note: The device will detect any of the above conditions, but does not report specifically which one has occurred.

7.3.8 Interrupt Pin (INTB)

The INTB pin is an active low interrupt output pin that acts as an interrupt for various local and remote interrupt conditions (see registers 0xC6 and 0xC7 of *Register Maps*). For the remote interrupt condition, the INTB pin works in conjunction with the INTB_IN pin on the deserializer. This interrupt signal, when configured, will propagate from the deserializer to the serializer.

1. On the Serializer, set register 0xC6[5] = 1 and 0xC6[0] = 1
2. Deserializer INTB_IN pin is set *LOW* by some downstream device.
3. Serializer pulls INTB pin *LOW*. The signal is active *LOW*, so a *LOW* indicates an interrupt condition.
4. External controller detects INTB = LOW; to determine interrupt source, read HDCP_ISR register.
5. A read to HDCP_ISR will clear the interrupt at the Serializer, releasing INTB.
6. The external controller typically must then access the remote device to determine downstream interrupt source and clear the interrupt driving the Deserializer INTB_IN. This would be when the downstream device releases the INTB_IN pin on the Deserializer. The system is now ready to return to step (2) at next falling edge of INTB_IN.

7.3.9 Remote Interrupt Pin (REM_INTB)

REM_INTB will mirror the status of INTB_IN pin on the deserializer and does not need to be cleared. If the serializer is not linked to the deserializer, REM_INTB will be high.

7.3.10 General-Purpose I/O

7.3.10.1 GPIO[3:0] Configuration

In normal operation, GPIO[3:0] may be used as general-purpose IOs in either forward channel (outputs) or back channel (inputs) mode. GPIO modes may be configured from the registers. See Table 1 for GPIO enable and configuration.

Table 1. GPIO Enable and Configuration

DESCRIPTION	DEVICE	FORWARD CHANNEL	BACK CHANNEL
GPIO3	Serializer	0x0F[3:0] = 0x3	0x0F[3:0] = 0x5
	Deserializer	0x1F[3:0] = 0x5	0x1F[3:0] = 0x3
GPIO2	Serializer	0x0E[7:4] = 0x3	0x0E[7:4] = 0x5
	Deserializer	0x1E[7:4] = 0x5	0x1E[7:4] = 0x3
GPIO1	Serializer	0x0E[3:0] = 0x3	0x0E[3:0] = 0x5
	Deserializer	0x1E[3:0] = 0x5	0x1E[3:0] = 0x3
GPIO0	Serializer	0x0D[3:0] = 0x3	0x0D[3:0] = 0x5
	Deserializer	0x1D[3:0] = 0x5	0x1D[3:0] = 0x3

7.3.10.2 Back Channel Configuration

The D_GPIO[3:0] pins can be configured to obtain different sampling rates depending on the mode as well as back channel frequency. These different modes are controlled by a compatible deserializer. Consult the appropriate deserializer datasheet for details on how to configure the back channel frequency. See Table 2 for details about D_GPIOs in various modes.

Table 2. Back Channel D_GPIO Effective Frequency

HSCC_MODE (on DES)	MODE	NUMBER OF D_GPIOs	SAMPLES PER FRAMe	D_GPIO Effective Frequency(1) (kHz)			D_GPIOs ALLOWED
				5 Mbps BC(2)	10 Mbps BC(3)	20 Mbps BC(4)	
000	Normal	4	1	33	66	133	D_GPIO[3:0]
011	Fast	4	6	200	400	800	D_GPIO[3:0]
010	Fast	2	10	333	666	1333	D_GPIO[1:0]
001	Fast	1	15	500	1000	2000	D_GPIO0

(1) The effective frequency assumes the worst case back channel frequency (-20%) and a 4X sampling rate.
(2) 5 Mbps corresponds to BC FREQ SELECT = 0 & BC_HS_CTL = 0 on deserializer.
(3) 10 Mbps corresponds to BC FREQ SELECT = 1 & BC_HS_CTL = 0 on deserializer.
(4) 20 Mbps corresponds to BC FREQ SELECT = X & BC_HS_CTL = 1 on deserializer.

7.3.10.3 GPIO_REG[8:5] Configuration

GPIO_REG[8:5] are register-only GPIOs and may be programmed as outputs or read as inputs through local register bits only. Where applicable, these bits are shared with I2S pins and will override I^2S input if enabled into GPIO_REG mode. See Table 3 for GPIO enable and configuration.

Note: Local GPIO value may be configured and read either through local register access, or remote register access through the Bidirectional Control Channel. Configuration and state of these pins are not transported from serializer to deserializer as is the case for GPIO[3:0].

Table 3. GPIO_REG and GPIO Local Enable and Configuration

DESCRIPTION	REGISTER CONFIGURATION	FUNCTION
GPIO_REG8	0x11[7:4] = 0x01	Output, L
	0x11[7:4] = 0x09	Output, H
	0x11[7:4] = 0x03	Input, Read: 0x1D[0]
GPIO_REG7	0x11[3:0] = 0x1	Output, L
	0x11[3:0] = 0x9	Output, H
	0x11[3:0] = 0x3	Input, Read: 0x1C[7]
GPIO_REG6	0x10[7:4] = 0x1	Output, L
	0x10[7:4] = 0x9	Output, H
	0x10[7:4] = 0x3	Input, Read: 0x1C[6]
GPIO_REG5	0x10[3:0] = 0x1	Output, L
	0x10[3:0] = 0x9	Output, H
	0x10[3:0] = 0x3	Input, Read: 0x1C[5]
GPIO3	0x0F[3:0] = 0x1	Output, L
	0x0F[3:0] = 0x9	Output, H
	0x0F[3:0] = 0x3	Input, Read: 0x1C[3]
GPIO2	0x0E[7:4] = 0x1	Output, L
	0x0E[7:4] = 0x9	Output, H
	0x0E[7:4] = 0x3	Input, Read: 0x1C[2]
GPIO1	0x0E[3:0] = 0x1	Output, L
	0x0E[3:0] = 0x9	Output, H
	0x0E[3:0] = 0x3	Input, Read: 0x1C[1]
GPIO0	0x0D[3:0] = 0x1	Output, L
	0x0D[3:0] = 0x9	Output, H
	0x0D[3:0] = 0x3	Input, Read: 0x1C[0]

7.3.11 SPI Communication

The SPI Control Channel utilizes the secondary link in a 2-lane FPD-Link III implementation. Two possible modes are available, Forward Channel and Reverse Channel modes. In Forward Channel mode, the SPI Master is located at the Serializer, such that the direction of sending SPI data is in the same direction as the video data. In Reverse Channel mode, the SPI Master is located at the Deserializer, such that the direction of sending SPI data is in the opposite direction as the video data.

The SPI Control Channel can operate in a high-speed mode when writing data, but must operate at lower frequencies when reading data. During SPI reads, data is clocked from the slave to the master on the SPI clock falling edge. Thus, the SPI read must operate with a clock period that is greater than the round trip data latency. On the other hand, for SPI writes, data can be sent at much higher frequencies where the MISO pin can be ignored by the master.

SPI data rates are not symmetrical for the two modes of operation. Data over the forward channel can be sent much faster than data over the reverse channel.

NOTE

SPI cannot be used to access Serializer / Deserializer registers.

7.3.11.1 SPI Mode Configuration

SPI is configured over I^2C using the High-Speed Control Channel Configuration (HSCC_CONTROL) register 0x43 on the deserializer. HSCC_MODE (0x43[2:0]) must be configured for either High-Speed, Forward Channel SPI mode (110) or High-Speed, Reverse Channel SPI mode (111).

The High-Speed Control Channel should be enabled only after Rx lock has been established.

7.3.11.2 Forward Channel SPI Operation

In Forward Channel SPI operation, the SPI master located at the Serializer generates the SPI Clock (SPLK), Master Out / Slave In data (MOSI), and active low Slave Select (SS). The Serializer oversamples the SPI signals directly using the video pixel clock. The three sampled values for SPLK, MOSI, and SS are each sent on data bits in the forward channel frame. At the Deserializer, the SPI signals are regenerated using the pixel clock. In order to preserve setup and hold time, the Deserializer will hold MOSI data while the SPLK signal is high. In addition, it delays SPLK by one pixel clock relative to the MOSI data, increasing setup by one pixel clock.

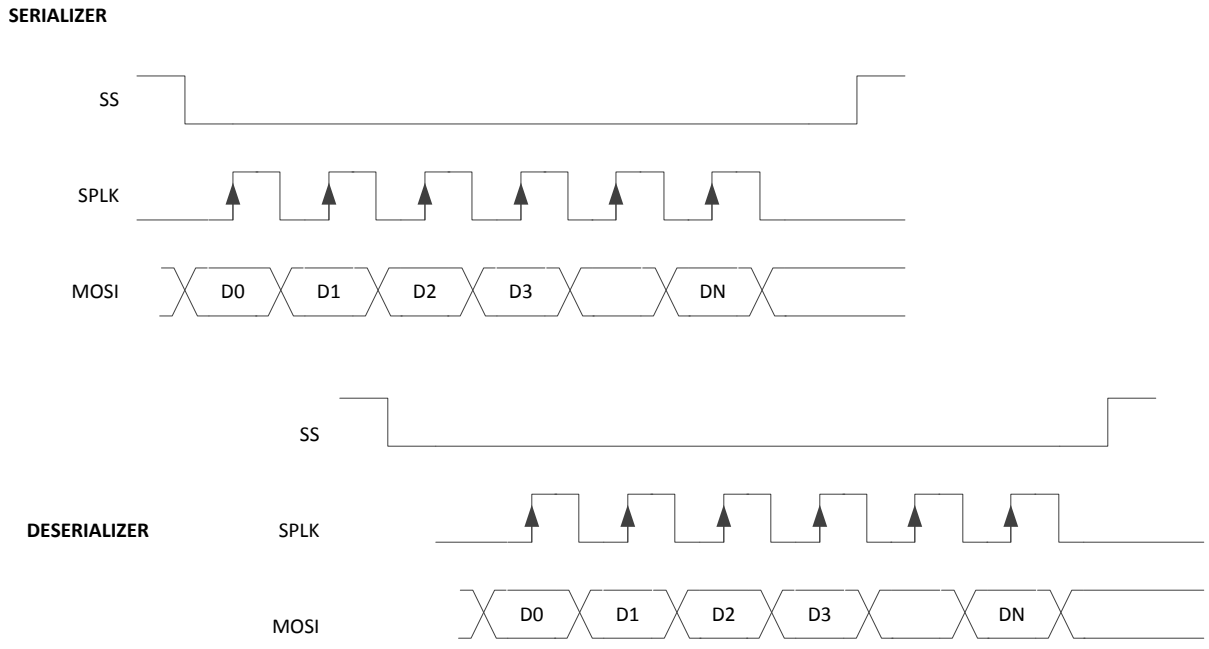


Figure 17. Forward Channel SPI Write

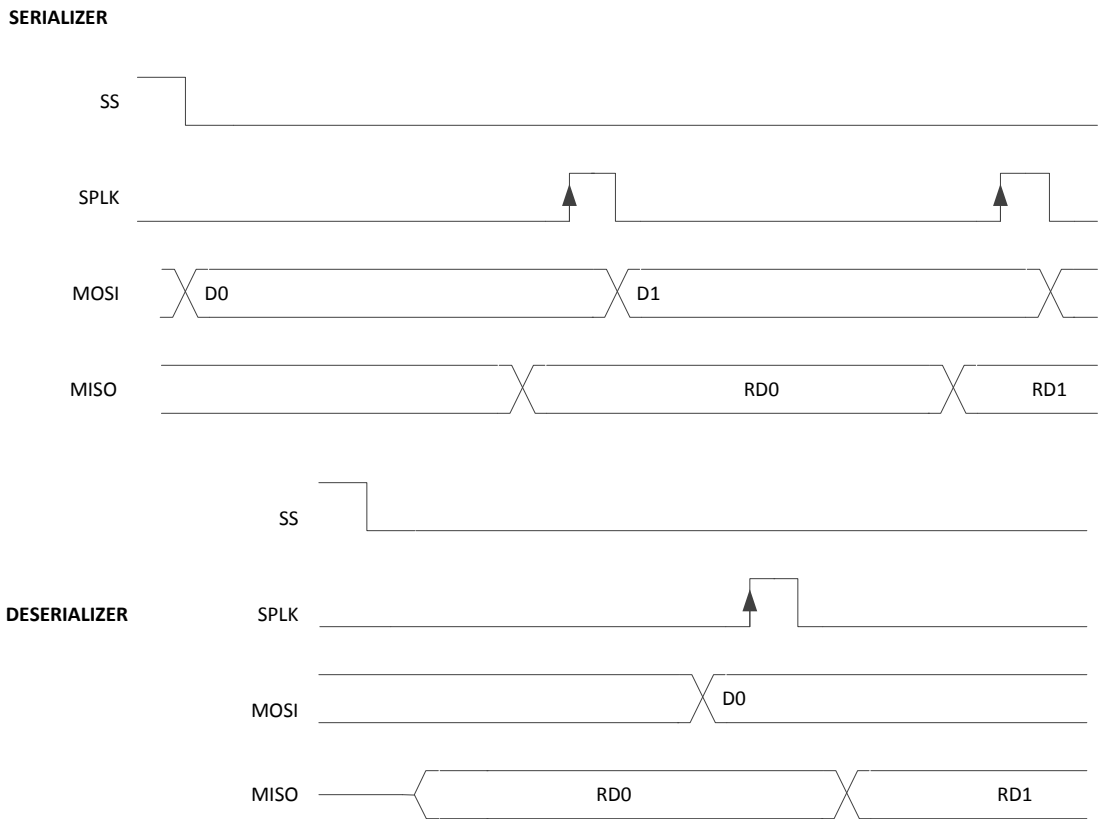


Figure 18. Forward Channel SPI Read

7.3.11.3 Reverse Channel SPI Operation

In Reverse Channel SPI operation, the Deserializer samples the Slave Select (SS), SPI clock (SCLK) into the internal oscillator clock domain. In addition, upon detection of the active SPI clock edge, the Deserializer samples the SPI data (MOSI). The SPI data samples are stored in a buffer to be passed to the Serializer over the back channel. The Deserializer sends SPI information in a back channel frame to the Serializer. In each back channel frame, the Deserializer sends an indication of the Slave Select value. The Slave Select should be inactive (high) for at least one back-channel frame period to ensure propagation to the Serializer.

Because data is delivered in separate back channel frames and buffered, the data may be regenerated in bursts. The following figure shows an example of the SPI data regeneration when the data arrives in three back channel frames. The first frame delivered the SS active indication, the second frame delivered the first three data bits, and the third frame delivers the additional data bits.

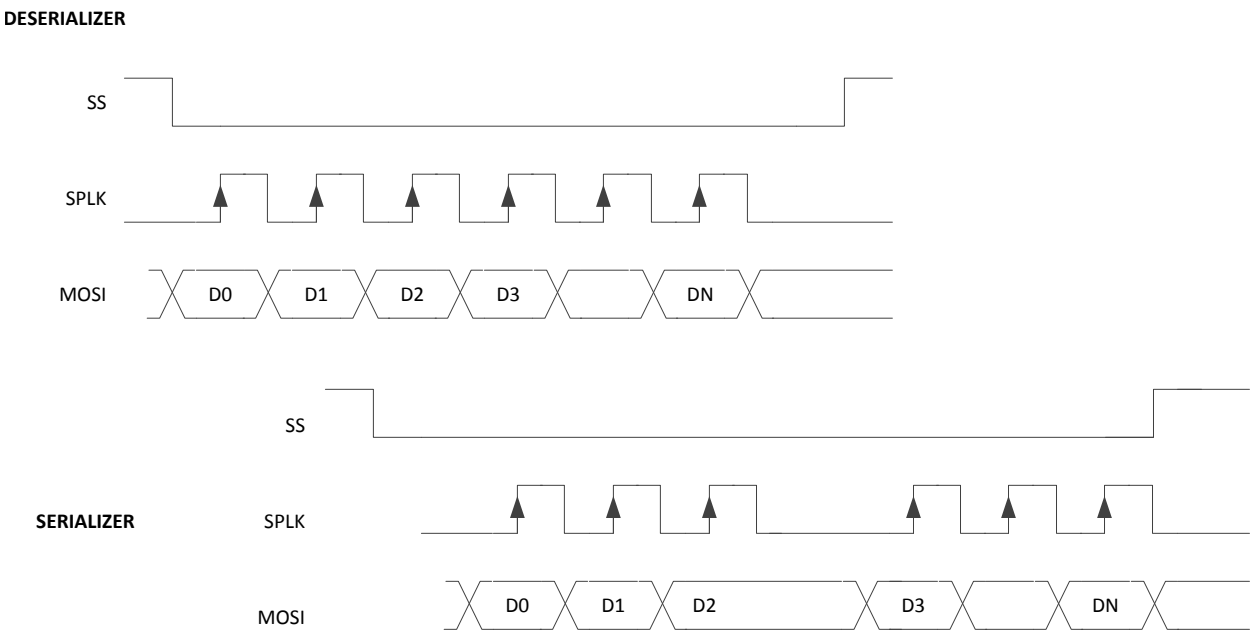


Figure 19. Reverse Channel SPI Write

For Reverse Channel SPI reads, the SPI master must wait for a round-trip response before generating the sampling edge of the SPI clock. This is similar to operation in Forward channel mode. Note that at most one data/clock sample will be sent per back channel frame.

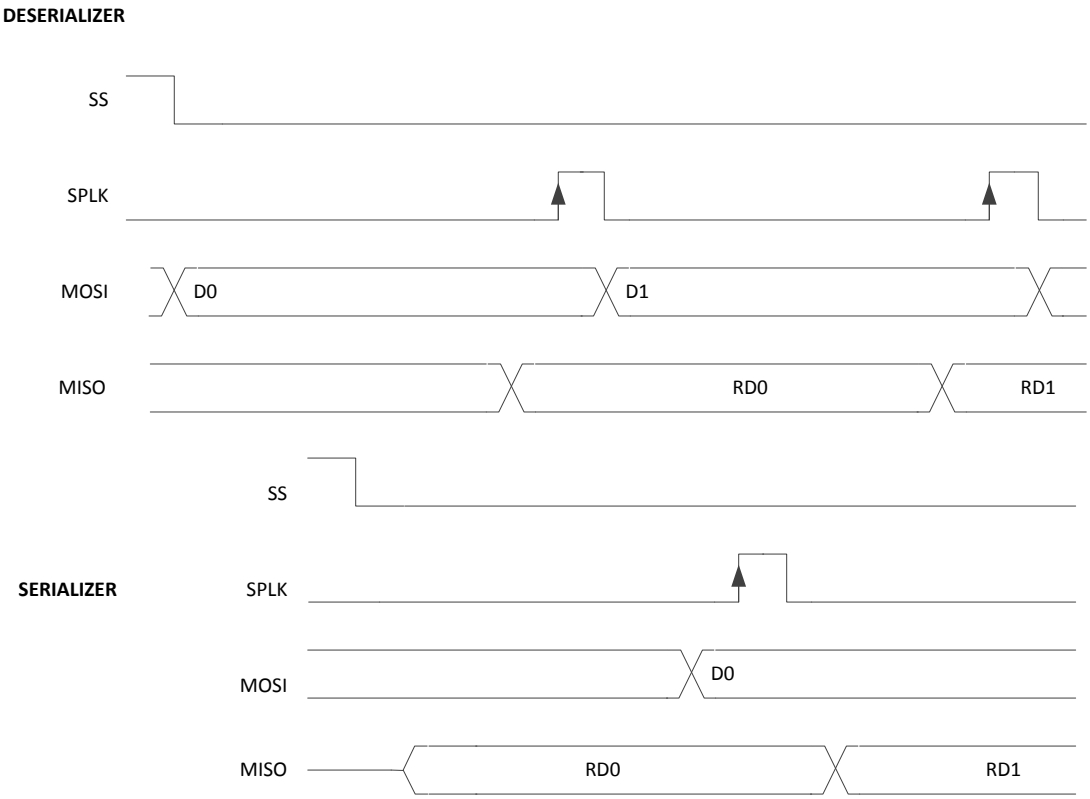


Figure 20. Reverse Channel SPI Read

For both Reverse Channel SPI writes and reads, the SPI_SS signal should be deasserted for at least one back channel frame period.

Table 4. SPI SS Deassertion Requirement

BACK CHANNEL FREQUENCY	DEASSERTION REQUIREMENT
5 Mbps	7.5 µs
10 Mbps	3.75 µs
20 Mbps	1.875 µs

7.3.12 Backward Compatibility

This FPD-Link III serializer is backward compatible to the DS90UH926Q-Q1 and DS90UH928Q-Q1 for OpenLDI clock frequencies ranging from 25 MHz to 85 MHz. Backward compatibility does not need to be enabled. When paired with a backward compatible device, the serializer will auto-detect to 1-lane FPD-Link III on the primary channel (DOUT0±).

7.3.13 Audio Modes

7.3.13.1 I2S Audio Interface

The DS90UH947-Q1 serializer features six I^{2}S input pins that, when paired with a compatible deserializer, supports 7.1 High-Definition (HD) Surround Sound audio applications. The bit clock (I2S_CLK) supports frequencies between 1MHz and the lesser of CLK/2 or 13 MHz. Four I^{2}S data inputs transport two channels of I^{2}S-formatted digital audio each, with each channel delineated by the word select (I2S_WC) input. Refer to Figure 21 and Figure 22 for I2S connection diagram and timing information.

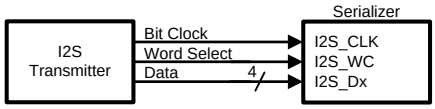


Figure 21. I^{2}S Connection Diagram

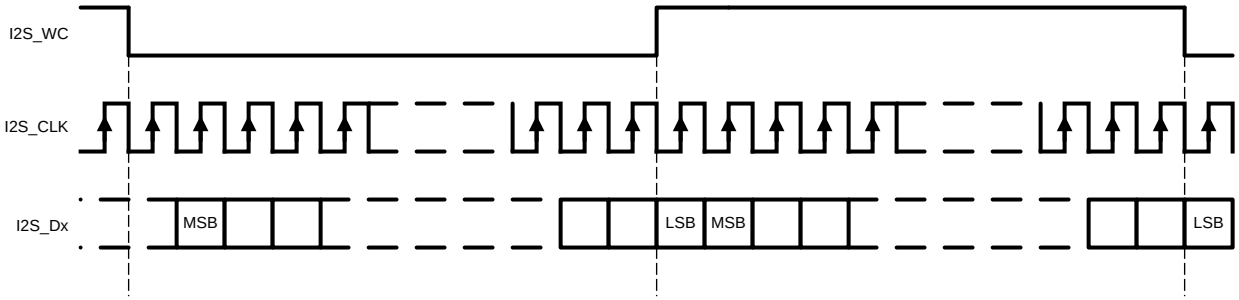


Figure 22. I2S Frame Timing Diagram

Table 5 covers several common I^{2}S sample rates:

Table 5. Audio Interface Frequencies

SAMPLE RATE (kHz)	I^{2}S DATA WORD SIZE (bits)	I^{2}S CLK (MHz)
32	16	1.024
44.1	16	1.411
48	16	1.536
96	16	3.072
192	16	6.144
32	24	1.536
44.1	24	2.117

Table 5. Audio Interface Frequencies (continued)

SAMPLE RATE (kHz)	I^2S DATA WORD SIZE (bits)	I^2S CLK (MHz)
48	24	2.304
96	24	4.608
192	24	9.216
32	32	2.048
44.1	32	2.822
48	32	3.072
96	32	6.144
192	32	12.288

7.3.13.1.1 I2S Transport Modes

By default, audio is packetized and transmitted during video blanking periods in dedicated Data Island Transport frames. Data Island frames may be disabled from control registers if Forward Channel Frame Transport of I^2S data is desired. In this mode, only I2S_DA is transmitted to a DS90UH928Q-Q1,DS90UH940-Q1, or DS90UH948-Q1 deserializer. If connected to a DS90UH926Q-Q1 deserializer, I2S_DA and I2S_DB are transmitted. Surround Sound Mode, which transmits all four I^2S data inputs (I2S_D[A..D]), may only be operated in Data Island Transport mode. This mode is only available when connected to a DS90UH928Q-Q1,DS90UH940-Q1, or DS90UH948-Q1 deserializer.

7.3.13.1.2 I2S Repeater

I^2S audio may be fanned-out and propagated in the repeater application. By default, data is propagated via Data Island Transport during the video blanking periods. If frame transport is desired, then the I^2S pins should be connected from the deserializer to all serializers. Activating surround sound at the top-level deserializer automatically configures downstream serializers and deserializers for surround sound transport utilizing Data Island Transport. If 4-channel operation utilizing I2S_DA and I2S_DB only is desired, this mode must be explicitly set in each serializer and deserializer control register throughout the repeater tree (Table 10).

7.3.13.2 TDM Audio Interface

In addition to the I2S audio interface, the DS90UH947-Q1 serializer also supports TDM format. Since a number of specifications for TDM format are in common use, the DS90UH947-Q1 offers flexible support for word length, bit clock, number of channels to be multiplexed, etc. For example, let's assume that word clock signal (I2S_WC) period = 256 × bit clock (I2S_CLK) time period. In this case, the DS90UH947-Q1 can multiplex 4 channels with maximum word length of 64 bits each, or 8 channels with maximum word length of 32 bits each. Figure 23 illustrates the multiplexing of 8 channels with 24 bit word length, in a format similar to I2S.

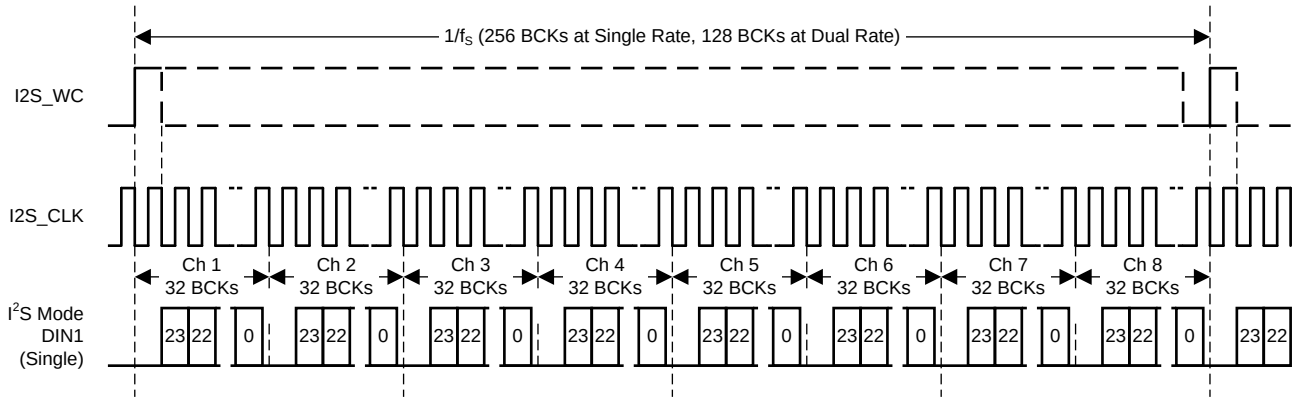


Figure 23. TDM Format

7.3.14 HDCP Repeater

The supported Repeater application provides a mechanism to extend transmission over multiple links to multiple display devices.

7.3.14.1 HDCP

The HDCP Cipher function is implemented in the deserializer per HDCP v1.4 specification. The DS90UH947-Q1 provides HDCP encryption of audiovisual content when connected to an HDCP video source. HDCP authentication and shared key generation is performed using the HDCP Control Channel, which is embedded in the forward and backward channels of the serial link. On-chip Non-Volatile Memory (NVM) is used to store the HDCP keys. The confidential HDCP keys are loaded by TI during the manufacturing process and are not accessible external to the device.

7.3.14.2 HDCP Repeater

The supported HDCP Repeater application provides a mechanism to extend HDCP transmission over multiple links to multiple display devices. It authenticates all HDCP devices in the system and distributes protected content to the HDCP Receivers using the encryption mechanisms provided in the HDCP specification.

7.3.14.2.1 Repeater Configuration

In the HDCP repeater application, this document refers to the DS90UH947-Q1 as the HDCP Transmitter (TX), and refers to the DS90UH948-Q1 as the HDCP Receiver (RX). Figure 24 shows the maximum configuration supported for HDCP Repeater implementations. Two levels of HDCP Repeaters are supported with a maximum of three HDCP Transmitters per HDCP Receiver.

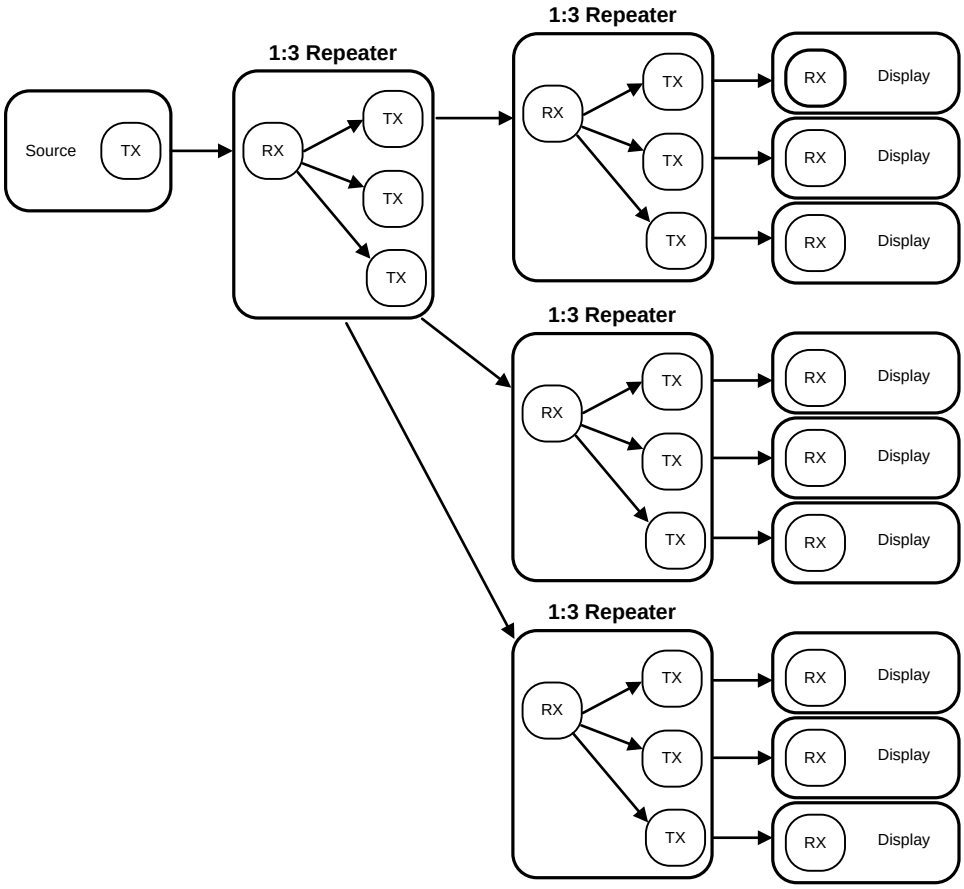


Figure 24. HDCP Maximum Repeater Application

In a repeater application, the I^2C interface at each TX and RX is configured to transparently pass I^2C communications upstream or downstream to any I^2C device within the system. This includes a mechanism for assigning alternate IDs (Slave Aliases) to downstream devices in the case of duplicate addresses.

To support HDCP Repeater operation, the RX includes the ability to control the downstream authentication process, assemble the KSV list for downstream HDCP Receivers, and pass the KSV list to the upstream HDCP Transmitter. An I^2C master within the RX communicates with the I^2C slave within the TX. The TX handles authenticating with a downstream HDCP Receiver and makes status available through the I^2C interface. The RX monitors the transmit port status for each TX and reads downstream KSV and KSV list values from the TX.

In addition to the I^2C interface used to control the authentication process, the HDCP Repeater implementation includes two other interfaces. The FPD-Link LVDS interface outputs the unencrypted video data. In addition to providing the video data, the LVDS interface communicates control information and packetized audio data. All audio and video data is decrypted at the output of the HDCP Receiver and is re-encrypted by the HDCP Transmitter. Figure 25 provides more detailed block diagram of a 1:2 HDCP repeater configuration.

If the repeater node includes a local output to a display, White Balancing and Hi-FRC dithering functions should not be used as they will block encrypted I2S audio and HDCP authentication.

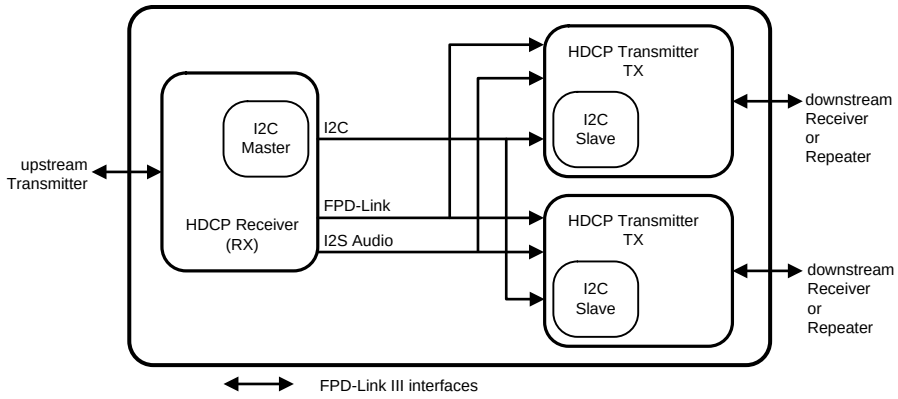


Figure 25. HDCP 1:2 Repeater Configuration

7.3.14.2.2 Repeater Connections

The HDCP Repeater requires the following connections between the HDCP Receiver and each HDCP Transmitter Figure 26.

1. Video Data – Connect all FPD-Link data and clock pairs. Single pixel OpenLDI (D[3:0]) or Dual pixel OpenLDI (D[7:0]) are both possible, provided the Deserializer and all Serializers are configured in the same mode.
2. I^2C – Connect SCL and SDA signals.
3. Audio (optional) – Connect I2S_CLK, I2S_WC, and I2S_Dx signals. Audio is normally transported on the OpenLDI interface.
4. IDx pin – Each Transmitter and Receiver must have an unique I2C address.
5. MODE_SEL pins — All Transmitters and Receivers must be set into Repeater Mode. OpenLDI settings (single pixel vs. dual pixel) must also match.
6. Interrupt pin – Connect DS90UH948-Q1 INTB_IN pin to the DS90UH947-Q1 INTB pin. The signal must be pulled up to V_{DDIO} with a 10kΩ resistor.

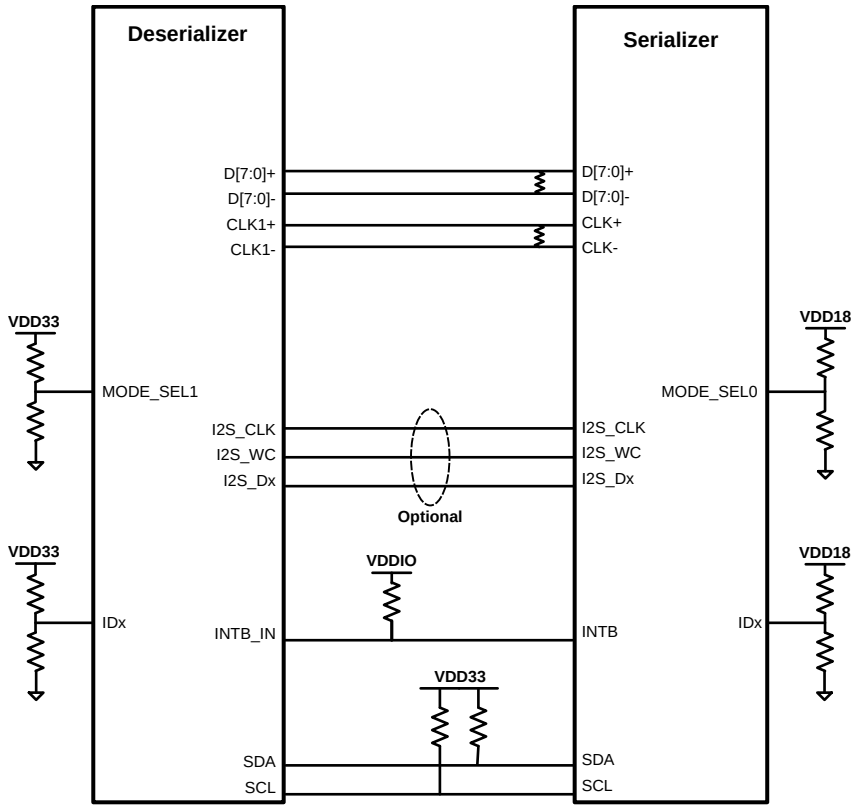


Figure 26. HDCP Repeater Connection Diagram

7.3.14.2.2.1 Repeater Fan-Out Electrical Requirements

Repeater applications requiring fan-out from one DS90UH948-Q1 Deserializer to up to three DS90UH947-Q1 Serializers requires special considerations for routing and termination of the FPD-Link differential traces. Figure 27 details the requirements that must be met for each signal pair:

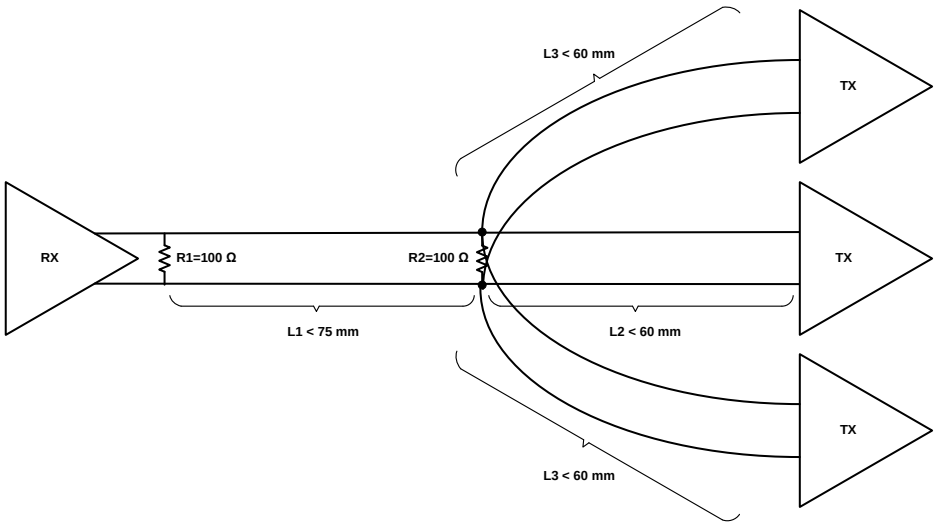


Figure 27. FPD-Link Fan-Out Electrical Requirements

7.3.14.2.2.2 HDCP I2S Audio Encryption

Depending on the quality and specifications of the audiovisual source, HDCP encryption of digital audio may be required. When HDCP is active, packetized Data Island Transport audio is also encrypted along with the video data per HDCP v1.4. I^2S audio transmitted in Forward Channel Frame Transport mode is not encrypted. System designers should consult the specific HDCP specifications to determine if encryption of digital audio is required by the specific application audiovisual source.

7.3.15 Built-In Self Test (BIST)

An optional At-Speed Built-In Self Test (BIST) feature supports testing of the high-speed serial link and back channel without external data connections. This is useful in the prototype stage, equipment production, in-system test, and system diagnostics.

7.3.15.1 BIST Configuration and Status

The BIST mode is enabled at the deserializer by pin (BISTEN) or BIST configuration register. The test may select either an external OpenLDI clock or the internal Oscillator clock (OSC) frequency. In the absence of OpenLDI clock, the user can select the internal OSC frequency at the deserializer through the BISTC pin or BIST configuration register.

When BIST is activated at the deserializer, a BIST enable signal is sent to the serializer through the Back Channel. The serializer outputs a test pattern and drives the link at speed. The deserializer detects the test pattern and monitors it for errors. The deserializer PASS output pin toggles to flag each frame received containing one or more errors. The serializer also tracks errors indicated by the CRC fields in each back channel frame.

The BIST status can be monitored real time on the deserializer PASS pin, with each detected error resulting in a half pixel clock period toggled LOW. After BIST is deactivated, the result of the last test is held on the PASS output until reset (new BIST test or Power Down). A high on PASS indicates NO ERRORS were detected. A Low on PASS indicates one or more errors were detected. The duration of the test is controlled by the pulse width applied to the deserializer BISTEN pin. LOCK is valid throughout the entire duration of BIST.

See Figure 28 for the BIST mode flow diagram.

Step 1: The Serializer is paired with another FPD-Link III Deserializer, BIST Mode is enabled via the BISTEN pin or through register on the Deserializer. Right after BIST is enabled, part of the BIST sequence requires bit 0x04[5] be toggled locally on the Serializer (set 0x04[5]=1, then set 0x04[5]=0). The desired clock source is selected through the deserializer BISTC pin, or through register on the Deserializer.

Step 2: An all-zeros pattern is balanced, scrambled, randomized, and sent through the FPD-Link III interface to the deserializer. Once the serializer and the deserializer are in BIST mode and the deserializer acquires Lock, the PASS pin of the deserializer goes high and BIST starts checking the data stream. If an error in the payload (1 to 35) is detected, the PASS pin will switch low for one half of the clock period. During the BIST test, the PASS output can be monitored and counted to determine the payload error rate.

Step 3: To Stop the BIST mode, the deserializer BISTEN pin is set Low. The deserializer stops checking the data. The final test result is held on the PASS pin. If the test ran error free, the PASS output will remain HIGH. If there one or more errors were detected, the PASS output will output constant LOW. The PASS output state is held until a new BIST is run, the device is RESET, or the device is powered down. The BIST duration is user controlled by the duration of the BISTEN signal.

Step 4: The link returns to normal operation after the deserializer BISTEN pin is low. Figure 29 shows the waveform diagram of a typical BIST test for two cases. Case 1 is error free, and Case 2 shows one with multiple errors. In most cases it is difficult to generate errors due to the robustness of the link (differential data transmission etc.), thus they may be introduced by greatly extending the cable length, faulting the interconnect medium, or reducing signal condition enhancements (Rx Equalization).

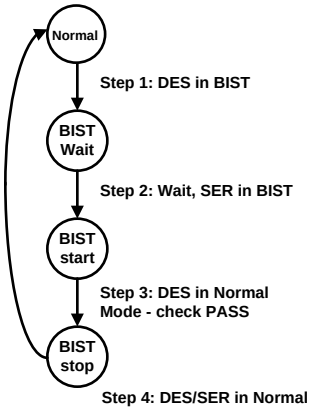


Figure 28. BIST Mode Flow Diagram

7.3.15.2 Forward Channel and Back Channel Error Checking

While in BIST mode, the serializer stops sampling the FPD-Link input pins and switches over to an internal all zeroes pattern. The internal all-zeroes pattern goes through scrambler, DC-balancing, etc. and is transmitted over the serial link to the deserializer. The deserializer, on locking to the serial stream, compares the recovered serial stream with all-zeroes and records any errors in status registers. Errors are also dynamically reported on the PASS pin of the deserializer.

The back-channel data is checked for CRC errors once the serializer locks onto the back-channel serial stream, as indicated by link detect status (register bit 0x0C[0] - Table 10). CRC errors are recorded in an 8-bit register in the deserializer. The register is cleared when the serializer enters BIST mode. As soon as the serializer enters BIST mode, the functional mode CRC register starts recording any back channel CRC errors. The BIST mode CRC error register is active in BIST mode only and keeps a record of the last BIST run until cleared or the serializer enters BIST mode again.

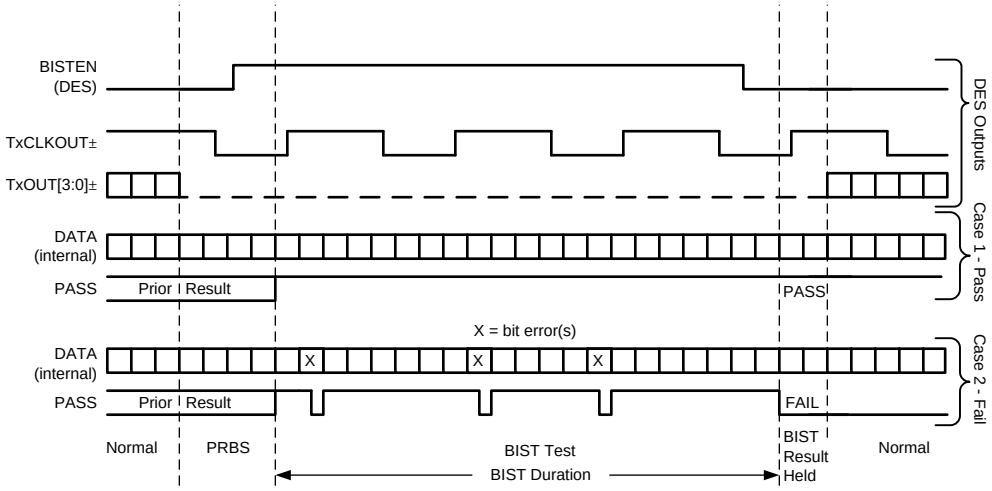


Figure 29. BIST Waveforms, in Conjunction With Deserializer Signals

7.3.16 Internal Pattern Generation

The DS90UH947-Q1 serializer provides an internal pattern generation feature. It allows basic testing and debugging of an integrated panel. The test patterns are simple and repetitive and allow for a quick visual verification of panel operation. As long as the device is not in power down mode, the test pattern will be displayed even if no input is applied. If no clock is received, the test pattern can be configured to use a programmed oscillator frequency. For detailed information, refer to *AN-2198 Exploring Int Test Patt Gen Feat of 720p FPD-Link III Devices* (SNLA132).

7.3.16.1 Pattern Options

The DS90UH947-Q1 serializer pattern generator is capable of generating 17 default patterns for use in basic testing and debugging of panels. Each can be inverted using register bits (Table 10), shown below:

1. White/Black (default/inverted)
2. Black/White
3. Red/Cyan
4. Green/Magenta
5. Blue/Yellow
6. Horizontally Scaled Black to White/White to Black
7. Horizontally Scaled Black to Red/Cyan to White
8. Horizontally Scaled Black to Green/Magenta to White
9. Horizontally Scaled Black to Blue/Yellow to White
10. Vertically Scaled Black to White/White to Black
11. Vertically Scaled Black to Red/Cyan to White
12. Vertically Scaled Black to Green/Magenta to White
13. Vertically Scaled Black to Blue/Yellow to White
14. Custom Color (or its inversion) configured in PGRS
15. Black-White/White-Black Checkerboard (or custom checkerboard color, configured in PGCTL)
16. YCBR/RBCY VCOM pattern, orientation is configurable from PGCTL
17. Color Bars (White, Yellow, Cyan, Green, Magenta, Red, Blue, Black) – Note: not included in the auto-scrolling feature

Additionally, the Pattern Generator incorporates one user-configurable full-screen 24-bit color, which is controlled by the PGRS, PGGS, and PGBS registers. This is pattern #14. One of the pattern options is statically selected in the PGCTL register when Auto-Scrolling is disabled. The PGTSC and PGTSO1-8 registers control the pattern selection and order when Auto-Scrolling is enabled.

7.3.16.2 Color Modes

By default, the Pattern Generator operates in 24-bit color mode, where all bits of the Red, Green, and Blue outputs are enabled. 18-bit color mode can be activated from the configuration registers (Table 10). In 18-bit mode, the 6 most significant bits (bits 7-2) of the Red, Green, and Blue outputs are enabled; the 2 least significant bits will be 0.

7.3.16.3 Video Timing Modes

The Pattern Generator has two video timing modes – external and internal. In external timing mode, the Pattern Generator detects the video frame timing present on the DE and VS inputs. If Vertical Sync signaling is not present on VS, the Pattern Generator determines Vertical Blank by detecting when the number of inactive pixel clocks (DE = 0) exceeds twice the detected active line length. In internal timing mode, the Pattern Generator uses custom video timing as configured in the control registers. The internal timing generation may also be driven by an external clock. By default, external timing mode is enabled. Internal timing or Internal timing with External Clock are enabled by the control registers (Table 10).

7.3.16.4 External Timing

In external timing mode, the Pattern Generator passes the incoming DE, HS, and VS signals unmodified to the video control outputs after a two pixel clock delay. It extracts the active frame dimensions from the incoming signals in order to properly scale the brightness patterns. If the incoming video stream does not use the VS signal, the Pattern Generator determines the Vertical Blank time by detecting a long period of pixel clocks without DE asserted.

7.3.16.5 Pattern Inversion

The Pattern Generator also incorporates a global inversion control, located in the PGCFG register, which causes the output pattern to be bitwise-inverted. For example, the full screen Red pattern becomes full-screen cyan, and the Vertically Scaled Black to Green pattern becomes Vertically Scaled White to Magenta.

7.3.16.6 Auto Scrolling

The Pattern Generator supports an Auto-Scrolling mode, in which the output pattern cycles through a list of enabled pattern types. A sequence of up to 16 patterns may be defined in the registers. The patterns may appear in any order in the sequence and may also appear more than once.

7.3.16.7 Additional Features

Additional pattern generator features can be accessed through the Pattern Generator Indirect Register Map. It consists of the Pattern Generator Indirect Address (PGIA reg_0x66 — Table 10) and the Pattern Generator Indirect Data (PGID reg_0x67 — Table 10). See *AN-2198 Exploring Int Test Patt Gen Feat of 720p FPD-Link III Devices* (SNLA132).

7.4 Device Functional Modes

7.4.1 Mode Select Configuration Settings (MODE_SEL[1:0])

Configuration of the device may be done via the MODE_SEL[1:0] input pins, or via the configuration register bits. A pull-up resistor and a pull-down resistor of suggested values may be used to set the voltage ratio of the MODE_SEL[1:0] inputs. See Table 7 and Table 8. These values will be latched into register location during power-up:

Table 6. MODE_SEL[1:0] Settings

MODE	SETTING	FUNCTION
OLDI_DUAL: OpenLDI Interface	0	Single-pixel OpenLDI interface.
	1	Dual-pixel OpenLDI interface.
REPEATER: Configure Repeater	0	Disable repeater mode.
	1	Enable repeater mode.
MAPSEL: OpenLDI Bit Mapping	0	OpenLDI bit mapping.
	1	SPWG bit mapping.
COAX: Cable Type	0	Enable FPD-Link III for twisted pair cabling.
	1	Enable FPD-Link III for coaxial cabling.

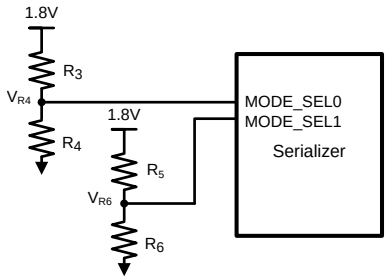


Figure 30. MODE_SEL[1:0] Connection Diagram

Table 7. Configuration Select (MODE_SEL0)

#	RATIO V_{R4}/V_{DD18}	TARGET V_{R4} (V)	SUGGESTED RESISTOR PULL-UP R3 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R4 kΩ (1% tol)	OLDI_DUAL	REPEATER
1	0	0	OPEN	Any value less than 100	0	0
2	0.213	0.383	115	30.9	0	1
5	0.560	1.008	82.5	105	1	0
6	0.676	1.216	51.1	107	1	1

Table 8. Configuration Select (MODE_SEL1)

#	RATIO V_{R6}/V_{DD18}	TARGET V_{R6} (V)	SUGGESTED RESISTOR PULL-UP R5 kΩ (1% tol)	SUGGESTED RESISTOR PULL-DOWN R6 kΩ (1% tol)	MAPSEL	COAX
1	0	0	OPEN	Any value less than 100	0	0
2	0.213	0.383	115	30.9	0	0
3	0.328	0.591	107	52.3	0	1
4	0.444	0.799	113	90.9	0	1
5	0.560	1.008	82.5	105	1	0
6	0.676	1.216	51.1	107	1	0
7	0.792	1.425	30.9	118	1	1
8	1	1.8	Any value less than 100	OPEN	1	1

The strapped values can be viewed and/or modified in the following locations:

- OLDI_DUAL : Latched into OLDI_IN_MODE (0x4F[6], inverted from strap value).
- REPEATER : Latched into TX_RPTR (0xC2[5]).
- MAPSEL : Latched into OLDI_MAPSEL (0x4F[7]).
- COAX : Latched into DUAL_CTL1[7], COAX_MODE (0x5B[7]).

7.4.2 FPD-Link III Modes of Operation

The FPD-Link III transmit logic supports several modes of operation, dependent on the downstream receiver as well as the video being delivered. The following modes are supported:

7.4.2.1 Single Link Operation

Single Link mode transmits the video over a single FPD-Link III to a single receiver. Single link mode supports frequencies up to 96MHz for 24-bit video when paired with the DS90UH940-Q1/DS90UH948-Q1. This mode is compatible with the DS90UH926Q-Q1/DS90UH928Q-Q1 when operating below 85MHz.

In Forced Single mode (set via DUAL_CTL1 register), the secondary TX Phy and back channel are disabled.

7.4.2.2 Dual Link Operation

In Dual Link mode, the FPD-Link III TX splits a single video stream and sends alternating pixels on two downstream links. If HDCP is enabled, a single HDCP connection is created for the video that is sent on the two links. The receiver must be a DS90UH948-Q1 or DS90UH940-Q1, capable of receiving the dual-stream video. Dual link mode is capable of supporting an OpenLDI clock frequency of up to 170MHz, with each FPD-Link III TX port running at one-half the frequency. This allows support for full 1080p video. The secondary FPD-Link III link could be used for high-speed control.

Dual Link mode may be automatically configured when connected to a DS90UH948-Q1/DS90UH940-Q1, if the video meets minimum frequency requirements. Dual Link mode may also be forced using the DUAL_CTL1 register.

7.4.2.3 Replicate Mode

In this mode, the FPD-Link III TX operates as a 1:2 HDCP Repeater. A second HDCP core is implemented to support HDCP authentication and encryption to independent HDCP-capable receivers. The same video (up to 85MHz, 24-bit color) is delivered to each receiver.

Replicate mode may be automatically configured when connected to two independent Deserializers.

7.4.2.4 Auto-Detection of FPD-Link III Modes

The DS90UH947-Q1 automatically detects the capabilities of downstream links and can resolve whether a single device, dual-capable device, or multiple single link devices are connected.

In addition to the downstream device capabilities, the DS90UH947-Q1 will be able to detect the OpenLDI pixel clock frequency to select the proper operating mode.

If the DS90UH947-Q1 detects two independent devices, it will operate in Replicate mode, sending the single channel video on both connections. If the device detects a device on the secondary link, but not the first, it can send the video only on the second link.

Auto-detection can be disabled to allow forced modes of operation using the Dual Link Control Register (DUAL_CTL1).

7.5 Programming

7.5.1 Serial Control Bus

This serializer may also be configured by the use of a I2C compatible serial control bus. Multiple devices may share the serial control bus (up to 8 device addresses supported). The device address is set via a resistor divider (R1 and R2 — see Figure 31 below) connected to the IDx pin.

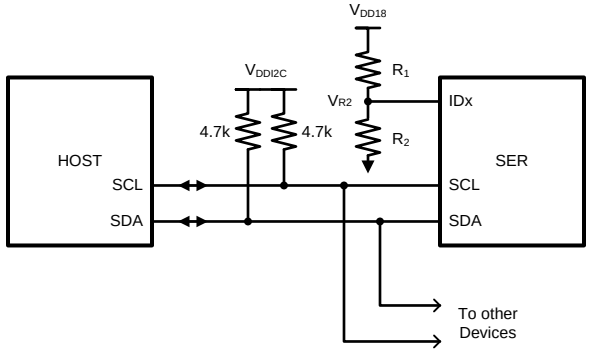


Figure 31. Serial Control Bus Connection

The serial control bus consists of two signals, SCL and SDA. SCL is a Serial Bus Clock Input. SDA is the Serial Bus Data Input / Output signal. Both SCL and SDA signals require an external pull-up resistor to V_{DD18} or V_{DD33}. For most applications, a 4.7-kΩ pull-up resistor is recommended. However, the pull-up resistor value may be adjusted for capacitive loading and data rate requirements. The signals are either pulled High, or driven Low.

The IDx pin configures the control interface to one of 8 possible device addresses. A pull-up resistor and a pull-down resistor may be used to set the appropriate voltage on the IDx input pin See Table 10 below.

Table 9. Serial Control Bus Addresses For IDx

#	RATIO V_{R2} / V_{DD18}	IDEAL V_{R2} (V)	SUGGESTED RESISTOR R1 kΩ (1% tol)	SUGGESTED RESISTOR R2 kΩ (1% tol)	7-BIT ADDRESS	8-BIT ADDRESS
1	0	0	Any value less than 100	40.2	0x0C	0x18
2	0.212	0.381	133	35.7	0x0E	0x1C
3	0.327	0.589	147	71.5	0x10	0x20
4	0.442	0.795	115	90.9	0x12	0x24
5	0.557	1.002	90.9	115	0x14	0x28
6	0.673	1.212	66.5	137	0x16	0x2C
7	0.789	1.421	21.5	80.6	0x18	0x30
8	1	1.8	Any value less than 100	OPEN	0x1A	0x34

The Serial Bus protocol is controlled by START, START-Repeated, and STOP phases. A START occurs when SCL transitions Low while SDA is High. A STOP occurs when SDA transitions High while SCL is also HIGH. See Figure 32

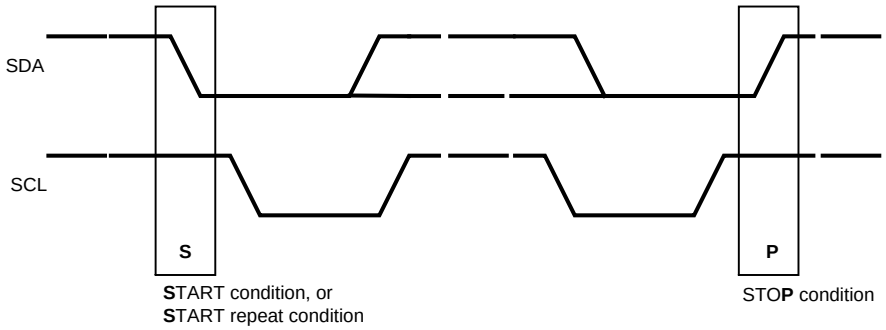


Figure 32. Start And Stop Conditions

To communicate with an I^2C slave, the host controller (master) sends the slave address and listens for a response from the slave. This response is referred to as an acknowledge bit (ACK). If a slave on the bus is addressed correctly, it Acknowledges (ACKs) the master by driving the SDA bus low. If the address doesn't match a device's slave address, it Not-acknowledges (NACKs) the master by letting SDA be pulled High. ACKs also occur on the bus when data is being transmitted. When the master is writing data, the slave ACKs after every data byte is successfully received. When the master is reading data, the master ACKs after every data byte is received to let the slave know it wants to receive another data byte. When the master wants to stop reading, it NACKs after the last data byte and creates a stop condition on the bus. All communication on the bus begins with either a Start condition or a Repeated Start condition. All communication on the bus ends with a Stop condition. A READ is shown in Figure 25 and a WRITE is shown in Figure 26.

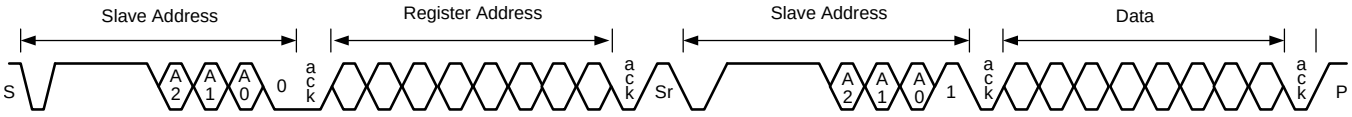


Figure 33. Serial Control Bus — Read

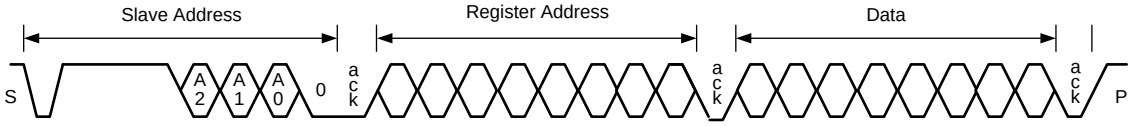


Figure 34. Serial Control Bus — Write

The I^2C Master located at the serializer must support I_2C clock stretching. For more information on I^2C interface requirements and throughput considerations, refer to the *I2C Communication Over FPD-Link III with Bidirectional Control Channel* application note (SNLA131).

7.5.2 Multi-Master Arbitration Support

The Bidirectional Control Channel in the FPD-Link III devices implements I^2C compatible bus arbitration in the proxy I^2C master implementation. When sending a data bit, each I_2C master senses the value on the SDA line. If the master is sending a logic 1 but senses a logic 0, the master has lost arbitration. It will stop driving SDA, retrying the transaction when the bus becomes idle. Thus, multiple I^2C masters may be implemented in the system.

If the system does require master-slave operation in both directions across the BCC, some method of communication must be used to ensure only one direction of operation occurs at any time. The communication method could include using available read/write registers in the deserializer to allow masters to communicate with each other to pass control between the two masters. An example would be to use register 0x18 or 0x19 in the deserializer as a mailbox register to pass control of the channel from one master to another.

7.5.3 I2C Restrictions on Multi-Master Operation

The I^2C specification does not provide for arbitration between masters under certain conditions. The system should make sure the following conditions cannot occur to prevent undefined conditions on the I^2C bus:

- One master generates a repeated Start while another master is sending a data bit.
- One master generates a Stop while another master is sending a data bit.
- One master generates a repeated Start while another master sends a Stop.

Note that these restrictions mainly apply to accessing the same register offsets within a specific I2C slave.

7.5.4 Multi-Master Access to Device Registers for Newer FPD-Link III Devices

When using the latest generation of FPD-Link III devices, DS90UH947-Q1 or DS90UH940-Q1/DS90UH948-Q1 registers may be accessed simultaneously from both local and remote I^2C masters. These devices have internal logic to properly arbitrate between sources to allow proper read and write access without risk of corruption.

Access to remote I^2C slaves would still be allowed in only one direction at a time .

7.5.5 Multi-Master Access to Device Registers for Older FPD-Link III Devices

When using older FPD-Link III devices, simultaneous access to serializer or deserializer registers from both local and remote I^2C masters may cause incorrect operation, thus restrictions should be imposed on accessing of serializer and deserializer registers. The likelihood of an error occurrence is relatively small, but it is possible for collision on reads and writes to occur, resulting in an errored read or write.

Two basic options are recommended. The first is to allow device register access only from one controller. This would allow only the Host controller to access the serializer registers (local) and the deserializer registers (remote). A controller at the deserializer would not be allowed to access the deserializer or serializer registers.

The second basic option is to allow local register access only with no access to remote serializer or deserializer registers. The Host controller would be allowed to access the serializer registers while a controller at the deserializer could access those register only. Access to remote I^2C slaves would still be allowed in one direction .

In a very limited case, remote and local access could be allowed to the deserializer registers at the same time. Register access is guaranteed to work correctly if both local and remote masters are accessing the same deserializer register. This allows a simple method of passing control of the Bidirectional Control Channel from one master to another.

7.5.6 Restrictions on Control Channel Direction for Multi-Master Operation

Only one direction should be active at any time across the Bidirectional Control Channel. If both directions are required, some method of transferring control between I^2C masters should be implemented.

7.6 Register Maps

Table 10. Serial Control Bus Registers

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
0	0x00	I2C Device ID	7:1	RW	IDx	Device ID Port0/Port1	7-bit address of Serializer. Defaults to address configured by the IDx strap pin. If PORT1_I2C_EN is set, this value defaults to the IDx strap value + 1 for Port1. If PORT1_SEL is set, this field refers to Port1 operation.
			0	RW		ID Setting	I2C ID setting. 0: Device I2C address is from IDx pin (default). 1: Device I2C address is from 0x00[7:1].
1	0x01	Reset	7:2		0x00		***Reserved***.
			1	RW		Digital RESET1	Reset the entire digital block including registers. This bit is self-clearing. 0: Normal operation (default). 1: Reset.
			0	RW		Digital RESET0	Reset the entire digital block except registers. This bit is self-clearing. 0: Normal operation (default). 1: Reset. Registers which are loaded by pin strap will be restored to their original strap value when this bit is set. These registers show 'Strap' as their default value in this table. Registers 0x18, 0x19, 0x1A, and 0x48-0x55 are also restored to their default value when this bit is set.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
3	0x03	General Configuration	7	RW	0xD2	Back channel CRC Checker Enable	Enable/disable back channel CRC Checker. 0: Disable. 1: Enable (default).
			6				***Reserved***.
			5	RW		I2C Remote Write Auto Acknowledge Port0/Port1	Automatically acknowledge I2C remote writes. When enabled, I2C writes to the Deserializer (or any remote I2C Slave, if I2C PASS ALL is enabled) are immediately acknowledged without waiting for the Deserializer to acknowledge the write. This allows higher throughput on the I2C bus. Note: this mode will prevent any NACK from a remote device from reaching the I2C master. 0: Disable (default). 1: Enable. If PORT1_SEL is set, this field refers to Port1 operation.
			4	RW		Filter Enable	HS, VS, DE two-clock filter. When enabled, pulses less than two full PCLK cycles on the DE, HS, and VS inputs will be rejected. 0: Filtering disable. 1: Filtering enable (default).
			3	RW		I2C Pass-through Port0/Port1	I2C pass-through mode. Read/Write transactions matching any entry in the Slave Alias registers will be passed through to the remote Deserializer. 0: Pass-through disabled (default). 1: Pass-through enabled. If PORT1_SEL is set, this field refers to Port1 operation.
			2				***Reserved.***
			1	RW		PCLK Auto	Switch over to internal oscillator in the absence of PCLK. 0: Disable auto-switch. 1: Enable auto-switch (default).
			0				***Reserved.***
4	0x04	Mode Select	7	RW	0x80	Failsafe State	Input failsafe state. 0: Failsafe to High. 1: Failsafe to Low (default).
			6				***Reserved.***
			5	RW		CRC Error Reset	Clear back channel CRC Error counters. This bit is NOT self-clearing. 0: Normal operation (default). 1: Clear counters.
			4				Reserved.
			3:0				Reserved.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
5	0x05	I2C Control	7:5		0x00		***Reserved.***
			4:3	RW		SDA Output Delay	Configures output delay on the SDA output. Setting this value will increase output delay in units of 40ns. Nominal output delay values for SCL to SDA are: 00: 240ns (default). 01: 280ns. 10: 320ns. 11: 360ns.
			2	RW		Local Write Disable	Disable remote writes to local registers. Setting this bit to 1 will prevent remote writes to local device registers from across the control channel. This prevents writes to the Serializer registers from an I2C master attached to the Deserializer. Setting this bit does not affect remote access to I2C slaves at the Serializer. 0: Enable (default). 1: Disable.
			1	RW		I2C Bus Timer Speedup	Speed up I2C bus Watchdog Timer. 0: Watchdog Timer expires after approximately 1s (default). 1: Watchdog Timer expires after approximately 50µs.
			0	RW		I2C Bus Timer Disable	Disable I2C bus Watchdog Timer. The I2C Watchdog Timer may be used to detect when the I2C bus is free or hung up following an invalid termination of a transaction. If SDA is high and no signaling occurs for approximately 1s, the I2C bus will be assumed to be free. If SDA is low and no signaling occurs, the device will attempt to clear the bus by driving 9 clocks on SCL. 0: Enable (default). 1: Disable.
6	0x06	DES ID	7:1	RW	0x00	DES Device ID Port0/Port1	7-bit I2C address of the remote Deserializer. A value of 0 in this field disables I2C access to the remote Deserializer. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but should also assert the FREEZE DEVICE ID bit to prevent overwriting by the Bidirectional Control Channel. If PORT1_SEL is set, this field refers to Port1 operation.
			0	RW		Freeze Device ID Port0/Port1	Freeze Deserializer Device ID. 1: Prevents auto-loading of the Deserializer Device ID by the Bidirectional Control Channel. The ID will be frozen at the value written. 0: Allows auto-loading of the Deserializer Device ID from the Bidirectional Control Channel. If PORT1_SEL is set, this field refers to Port1 operation.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
7	0x07	Slave ID[0]	7:1	RW	0x00	Slave ID 0 Port0/Port1	7-bit I2C address of the remote Slave 0 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 0, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 0. If PORT1_SEL is set, this field refers to Port1 operation.
			0				***Reserved.***
8	0x08	Slave Alias[0]	7:1	RW	0x00	Slave Alias ID 0 Port0/Port1	7-bit Slave Alias ID of the remote Slave 0 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 0 register. A value of 0 in this field disables access to the remote Slave 0. If PORT1_SEL is set, this field refers to Port1 operation.
			0				***Reserved.***
10	0x0A	CRC Errors	7:0	R	0x00	CRC Error LSB Port0/Port1	Number of back channel CRC errors – 8 least significant bits. Cleared by 0x04[5]. If PORT1_SEL is set, this field refers to Port1 operation.
11	0x0B		7:0	R	0x00	CRC Error MSB Port0/Port1	Number of back channel CRC errors – 8 most significant bits. Cleared by 0x04[5]. If PORT1_SEL is set, this field refers to Port1 operation.
12	0x0C	General Status	7:4		0x00		***Reserved.***
			3	R		BIST CRC Error Port0/Port1	Back channel CRC error(s) during BIST communication with Deserializer. This bit is cleared upon loss of link, restart of BIST, or assertion of CRC Error Reset bit in 0x04[5]. 0: No CRC errors detected during BIST. 1: CRC error(s) detected during BIST. If PORT1_SEL is set, this field refers to Port1 operation.
			2	R		PCLK Detect	Pixel clock status: 0: Valid PCLK not detected at OpenLDI input. 1: Valid PCLK detected at OpenLDI input. When the OpenLDI input is suddenly removed, this bit will remain asserted until and invalid (out of range) clock is applied.
			1	R		DES Error Port0/Port1	CRC error(s) during normal communication with Deserializer. This bit is cleared upon loss of link or assertion of 0x04[5]. 0: No CRC errors detected. 1: CRC error(s) detected. If PORT1_SEL is set, this field refers to Port1 operation.
			0	R		LINK Detect Port0/Port1	LINK detect status: 0: Cable link not detected. 1: Cable link detected. If PORT1_SEL is set, this field refers to Port1 operation.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
13	0x0D	GPIO0 Configuration (If PORT1_SEL is set, this register controls the D_GPIO0 pin)	7:4	R	0x00	Revision ID	Revision ID: 0010: Production device.
			3	RW		GPIO0 Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is set to output, and remote GPIO control is disabled. 0: Output LOW (default). 1: Output HIGH.
			2:0	RW		GPIO0 Mode	Determines operating mode for the GPIO pin: x00: Functional input mode. x10: TRI-STATE. 001: GPIO mode, output. 011: GPIO mode, input. 101: Remote-hold mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-hold mode, data is maintained on link loss. 111: Remote-default mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-default mode, GPIO's Output Value bit is output on link loss.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
14	0x0E	GPIO1 and GPIO2 Configuration (If PORT1_SEL is set, this register controls the D_GPIO1 and D_GPIO2 pins)	7	RW	0x00	GPIO2 Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is set to output, and remote GPIO control is disabled. 0: Output LOW (default). 1: Output HIGH.
			6:4	RW		GPIO2 Mode	Determines operating mode for the GPIO pin: x00: Functional input mode. x10: TRI-STATE. 001: GPIO mode, output. 011: GPIO mode, input. 101: Remote-hold mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-hold mode, data is maintained on link loss. 111: Remote-default mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-default mode, GPIO's Output Value bit is output on link loss.
			3	RW		GPIO1 Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is set to output, and remote GPIO control is disabled. 0: Output LOW (default). 1: Output HIGH.
			2:0	RW		GPIO1 Mode	Determines operating mode for the GPIO pin: x00: Functional input mode. x10: TRI-STATE. 001: GPIO mode, output. 011: GPIO mode, input. 101: Remote-hold mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-hold mode, data is maintained on link loss. 111: Remote-default mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-default mode, GPIO's Output Value bit is output on link loss.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
15	0x0F	GPIO3 Configuration (If PORT1_SEL is set, this register controls the D_GPIO3 pin)	7:4		0x00		***Reserved.***
			3	RW		GPIO3 Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled, the local GPIO direction is set to output, and remote GPIO control is disabled. 0: Output LOW (default). 1: Output HIGH.
			2:0	RW		GPIO3 Mode	Determines operating mode for the GPIO pin: x00: Functional input mode. x10: TRI-STATE. 001: GPIO mode, output. 011: GPIO mode, input. 101: Remote-hold mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-hold mode, data is maintained on link loss. 111: Remote-default mode. The GPIO pin will be an output, and the value is received from the remote Deserializer. In remote-default mode, GPIO's Output Value bit is output on link loss.
16	0x10	GPIO5_REG and GPIO6_REG Configuration	7	RW	0x00	GPIO6_REG Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is set to output. 0: Output LOW (default). 1: Output HIGH.
			6				***Reserved.***
			5:4	RW		GPIO6_REG Mode	Determines operating mode for the GPIO pin: 00: Functional input mode. 10: TRI-STATE. 01: GPIO mode, output. 11: GPIO mode; input.
			3	RW		GPIO5_REG Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is set to output. 0: Output LOW (default). 1: Output HIGH.
			2				***Reserved.***
			1:0	RW		GPIO5_REG Mode	Determines operating mode for the GPIO pin: 00: Functional input mode. 10: TRI-STATE. 01: GPIO mode, output. 11: GPIO mode; input.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
17	0x11	GPIO7_REG and GPIO8_REG Configuration	7	RW	0x00	GPIO8_REG Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is set to output. 0: Output LOW (default). 1: Output HIGH.
			6				***Reserved.***
			5:4	RW		GPIO8_REG Mode	Determines operating mode for the GPIO pin: 00: Functional input mode. 10: TRI-STATE. 01: GPIO mode, output. 11: GPIO mode; input.
			3	RW		GPIO7_REG Output Value	Local GPIO Output Value. This value is output on the GPIO pin when the GPIO function is enabled and the local GPIO direction is set to output. 0: Output LOW (default). 1: Output HIGH.
			2				***Reserved.***
			1:0	RW		GPIO7_REG Mode	Determines operating mode for the GPIO pin: 00: Functional input mode. 10: TRI-STATE. 01: GPIO mode, output. 11: GPIO mode; input.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
18	0x12	Data Path Control	7		0x00		***Reserved.***
			6	RW		PASS RGB	Setting this bit causes RGB data to be sent independent of DE in UH devices, which can be used to allow UH devices to interoperate with UB devices. However, setting this bit prevents HDCP operation and blocks packetized audio. This bit does not need to be set in UB devices. 1: Pass RGB independent of DE. 0: Normal operation.
			5	RW		DE Polarity	This bit indicates the polarity of the DE (Data Enable) signal. 1: DE is inverted (active low, idle high). 0: DE is positive (active high, idle low).
			4	RW		I2S Repeater Regen	Regenerate I2S data from Repeater I2S pins. 0: Repeater pass through I2S from video pins (default). 1: Repeater regenerate I2S from I2S pins.
			3	RW		I2S CHANNEL B ENABLE OVERRIDE	1: Set I2S Channel B Enable from reg_12[0]. 0: I2S Channel B Disabled.
			2	RW		Video Select	Selects 18-bit or 24-bit video. 1: Select 18-bit video mode. 0: Select 24-bit video mode.
			1	RW		I2S Transport Select	Select I2S transport mode: 0: Enable I2S Data Island transport (default). 1: Enable I2S Data Forward Channel Frame transport.
			0	RW		I2S CHANNEL B ENABLE	I2S Channel B Enable. 1: Enable I2S Channel B on B1 input. 0: I2S Channel B disabled. Note that in a repeater, this bit may be overridden by the in-band I2S mode detection.
19	0x13	General-Purpose Control	7	R	0x88	MODE_SEL1 Done	Indicates MODE_SEL1 value has stabilized and has been latched.
			6:4	R		MODE_SEL1 Decode	Returns the 3-bit decode of the MODE_SEL1 pin.
			3	R		MODE_SEL0 Done	Indicates MODE_SEL0 value has stabilized and has been latched.
			2:0	R		MODE_SEL0 Decode	Returns the 3-bit decode of the MODE_SEL0 pin.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
20	0x14	BIST Control	7:3		0x00		***Reserved.***
			2:1	RW		OSC Clock Source	Allows choosing different OSC clock frequencies for forward channel frame. OSC Clock Frequency in Functional Mode when PCLK is not present and 0x03[2]=1. 00: 50MHz Oscillator. 01: 50 MHz Oscillator. 10: 100 MHz Oscillator. 11: 25 MHz Oscillator. Clock Source in BIST mode i.e. when 0x14[0]=1. 00: External Pixel Clock. 01: 50 MHz Oscillator. 10: 100 MHz Oscillator. 11: 25 MHz Oscillator.
			0	R		BIST Enable	BIST control: 0: Disabled (default). 1: Enabled.
21	0x15	I2C Voltage Select	7:0	RW	0x01	I2C Voltage Select	Selects 1.8 or 3.3V for the I2C_SDA and I2C_SCL pins. This register is loaded from the I2C_VSEL strap option from the I2CSEL pin at power-up. At power-up, a logic LOW will select 3.3V operation, while a logic HIGH (pull-up resistor attached) will select 1.8V signaling. Issuing either of the digital resets via register 0x01 will cause the I2C_VSEL value to be reset to 3.3V operation. Reads of this register return the status of the I2C_VSEL control: 0: Select 1.8V signaling. 1: Select 3.3V signaling. This bit may be overwritten via register access or via eFuse program by writing an 8-bit value to this register: Write 0xb5 to set I2C_VSEL. Write 0xb6 to clear I2C_VSEL.
22	0x16	BCC Watchdog Control	7:1	RW	0xFE	Timer Value	The watchdog timer allows termination of a control channel transaction if it fails to complete within a programmed amount of time. This field sets the Bidirectional Control Channel Watchdog Timeout value in units of 2 milliseconds. This field should not be set to 0.
			0	RW		Timer Control	Disable Bidirectional Control Channel (BCC) Watchdog Timer: 0: Enable BCC Watchdog Timer operation (default). 1: Disable BCC Watchdog Timer operation.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
23	0x17	I2C Control	7	RW	0x1E	I2C Pass All	0: Enable Forward Control Channel pass-through only of I2C accesses to I2C Slave IDs matching either the remote Deserializer Slave ID or the remote Slave ID (default). 1: Enable Forward Control Channel pass-through of all I2C accesses to I2C Slave IDs that do not match the Serializer I2C Slave ID.
			6:4	RW		SDA Hold Time	Internal SDA hold time: Configures the amount of internal hold time provided for the SDA input relative to the SCL input. Units are 40 nanoseconds.
			3:0	RW		I2C Filter Depth	Configures the maximum width of glitch pulses on the SCL and SDA inputs that will be rejected. Units are 5 nanoseconds.
24	0x18	SCL High Time	7:0	RW	0xA1	SCL HIGH Time	I2C Master SCL High Time: This field configures the high pulse width of the SCL output when the Serializer is the Master on the local I2C bus. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL high time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional oscillator clock periods. Min_delay = 38.0952ns * (TX_SCL_HIGH + 5).
25	0x19	SCL Low Time	7:0	RW	0xA5	SCL LOW Time	I2C SCL Low Time: This field configures the low pulse width of the SCL output when the Serializer is the Master on the local I2C bus. This value is also used as the SDA setup time by the I2C Slave for providing data prior to releasing SCL during accesses over the Bidirectional Control Channel. Units are 40 ns for the nominal oscillator clock frequency. The default value is set to provide a minimum 5us SCL low time with the internal oscillator clock running at 26.25MHz rather than the nominal 25MHz. Delay includes 5 additional clock periods. Min_delay = 38.0952ns * (TX_SCL_LOW + 5).
26	0x1A	Data Path Control 2	7	RW	0x00	BLOCK_REPEATER_I2S_MODE	Block automatic I2S mode configuration in repeater. 0: I2S mode (2-channel, 4-channel, or surround) is detected from the in-band audio signaling in a repeater. 1: Disable automatic detection of I2S mode.
			6:2				Reserved.
			1	RW	0x00	MODE_28B	Enable 28-bit Serializer Mode. 0: 24-bit high-speed data + 3 low-speed control (DE, HS, VS). 1: 28-bit high-speed data mode.
			0	RW		I2S Surround	Enable 5.1- or 7.1-channel I2S audio transport: 0: 2-channel or 4-channel I2S audio is enabled as configured in register 0x12 bits 3 and 0 (default). 1: 5.1- or 7.1-channel audio is enabled. Note that I2S Data Island Transport is the only option for surround audio. Also note that in a repeater, this bit may be overridden by the in-band I2S mode detection.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
27	0x1B	BIST BC Error Count	7:0	R	0x00	BIST BC Error Port0/Port1	BIST back channel CRC error counter. This register stores the back channel CRC error count during BIST Mode (saturates at 255 errors). Clears when a new BIST is initiated or by 0x04[5]. If PORT1_SEL is set, this register indicates Port1 operation.
28	0x1C	GPIO Pin Status 1	7	R	0x00	GPIO7_REG Pin Status	GPIO7_REG input pin status. Note: status valid only if pin is set to GPI (input) mode.
			6	R		GPIO6_REG Pin Status	GPIO6_REG input pin status. Note: status valid only if pin is set to GPI (input) mode.
			5	R		GPIO5_REG Pin Status	GPIO5_REG input pin status. Note: status valid only if pin is set to GPI (input) mode.
			4				***Reserved.***
			3	R		GPIO3 Pin Status D_GPIO3 Pin Status	GPIO3 input pin status. Note: status valid only if pin is set to GPI (input) mode. If PORT1_SEL is set, this register indicates D_GPIO3 operation.
			2	R		GPIO2 Pin Status D_GPIO2 Pin Status	GPIO2 input pin status. Note: status valid only if pin is set to GPI (input) mode. If PORT1_SEL is set, this register indicates D_GPIO2 operation.
			1	R		GPIO1 Pin Status D_GPIO1 Pin Status	GPIO1 input pin status. Note: status valid only if pin is set to GPI (input) mode. If PORT1_SEL is set, this register indicates D_GPIO1 operation.
			0	R		GPIO0 Pin Status D_GPIO0 Pin Status	GPIO0 input pin status. Note: status valid only if pin is set to GPI (input) mode. If PORT1_SEL is set, this register indicates D_GPIO0 operation.
29	0x1D	GPIO Pin Status 2	7:1		0x00		***Reserved***
			0	R		GPIO8_REG Pin Status	GPIO8_REG input pin status. Note: status valid only if pin is set to GPI (input) mode.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
30	0x1E	Port Select	7:3		0x01		Reserved.
			2	RW		PORT1_I2C_EN	Port1 I2C Enable: Enables secondary I2C address. The second I2C address provides access to port1 registers as well as registers that are shared between ports 0 and 1. The second I2C address value will be set to DeviceID + 1 (7-bit format). The PORT1_I2C_EN bit must also be set to allow accessing remote devices over the second link when the device is in Replicate mode.
			1	RW		PORT1_SEL	Selects Port 1 for Register Access from primary I2C Address. For writes, Port 1 registers and shared registers will both be written. For reads, Port 1 registers and shared registers will be read. This bit must be cleared to read Port 0 registers. If this bit is set, GPIO[3:0] registers control operation for D_GPIO[3:0] registers. This bit is ignored if PORT1_I2C_EN is set.
			0	RW		PORT0_SEL	Selects Port 0 for Register Access from primary I2C Address. For writes, Port 0 registers and shared registers will both be written. For reads, Port 0 registers and shared registers will be read. Note that if PORT1_SEL is also set, then Port 1 registers will be read. This bit is ignored if PORT1_I2C_EN is set.
31	0x1F	Frequency Counter	7:0	RW	0x00	Frequency Count	Frequency Counter control: A write to this register will enable a frequency counter to count the number of pixel clock during a specified time interval. The time interval is equal to the value written multiplied by the oscillator clock period (nominally 40ns). A read of the register returns the number of pixel clock edges seen during the enabled interval. The frequency counter will freeze at 0xff if it reaches the maximum value. The frequency counter will provide a rough estimate of the pixel clock period. If the pixel clock frequency is known, the frequency counter may be used to determine the actual oscillator clock frequency.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
32	0x20	Deserializer Capabilities	7	RW	0x00	FREEZE DES CAP Port0/Port1	Freeze Deserializer Capabilities. Prevent auto-loading of the Deserializer Capabilities by the Bidirectional Control Channel. The Capabilities will be frozen at the values written in registers 0x20 and 0x21.
			6				Reserved.
			5	RW		Send_Freq Port0/Port1	Send Frequency Training Pattern.
			4	RW	0x00	Send_EQ Port0/Port1	Send Equalization Training Pattern.
			3	RW		Dual Link Capable Port0/Port1	Dual link capabilities. Indicates if the Deserializer is capable of dual link operation.
			2	RW		Dual Channel Port0/Port1	In a dual-link device, indicates if this is the primary or secondary channel. 0: Primary channel (channel 0). 1: Secondary channel (channel 1).
			1	RW		VID_24B_HD_AUD Port0/Port1	Deserializer supports 24-bit video concurrently with HD audio. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
			0	RW		DES_CAP_FC_GPIO Port0/Port1	Deserializer supports GPIO in the Forward Channel Frame. This field is automatically configured by the Bidirectional Control Channel once RX Lock has been detected. Software may overwrite this value, but must also set the FREEZE DES CAP bit to prevent overwriting by the Bidirectional Control Channel.
38	0x26	Link Detect Control	7:2				Reserved.
			1:0	RW	0x00	LINK DETECT TIMER	Bidirectional Control Channel Link Detect Timer. This field configures the link detection timeout period. If the timer expires without valid communication over the reverse channel, link detect will be deasserted. 00: 325 microseconds. 01: 162 microseconds. 10: 650 microseconds. 11: 1.3 milliseconds.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
64	0x40	ANA_IA_CNTL	7:5		0x00		Reserved.
			4:2	RW		ANA_IA_SEL	Analog register select Selects target for register access 000b: Disabled 001b - 011b: Reserved 100b: OLDI Registers 101b: FPD3 TX Registers 11xb: Reserved
			1	RW		ANA_AUTO_INC	Analog Register Auto Increment 0: Disable auto-increment mode 1: Enable auto-increment mode. Upon completion of a read or write, the register address will automatically be incremented by 1.
			0	RW		ANA_IA_READ	Start Analog Register Read 0: Write analog register 1: Read analog register
65	0x41	ANA_IA_ADDR	7:0	RW	0x00	ANA_IA_ADDR	Analog register offset This register contains the 8-bit register offset for the indirect access.
66	0x42	ANA_IA_DATA	7:0	RW	0x00	ANA_IA_DATA	Analog register data Writing this register will cause an indirect write of the ANA_IA_DATA value to the selected analog block register. Reading this register will return the value of the selected analog block register.
72	0x48	APB_CTL	7:5				Reserved.
			4:3	RW	0x00	APB_SELECT	APB Select: Selects target for register access: 00 : Reserved. 01 : Reserved. 10 : Configuration Data (read only). 11 : Die ID (read only).
			2	RW		APB_AUTO_INC	APB Auto Increment: Enables auto-increment mode. Upon completion of an APB read or write, the APB address will automatically be incremented by 0x1.
			1	RW		APB_READ	Start APB Read: Setting this bit to a 1 will begin an APB read. Read data will be available in the APB_DATA0 register. The APB_ADR0 register should be programmed prior to setting this bit. This bit will be cleared when the read is complete.
			0	RW		APB_ENABLE	APB Interface Enable: Set to a 1 to enable the APB interface. The APB_SELECT bits indicate what device is selected.
73	0x49	APB_ADR0	7:0	RW	0x00	APB_ADR0	APB address byte 0 (LSB).
75	0x4B	APB_DATA0	7:0	RW	0x00	APB_DATA0	Byte 0 (LSB) of the APB Interface Data.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
79	0x4F	BRIDGE_CTL	7	RW	Strap	OLDI_MAPSEL	OpenLDI Bit Map Select. Determines data mapping on the OpenLDI interface. 0: SPWG mapping. 1: OpenLDI mapping. OLDI_MAPSEL is initially loaded from the MODE_SEL1 pin strap options.
			6	RW	Strap	OLDI_IN_MODE	OpenLDI Receiver Input Mode. Determines operating mode of OpenLDI Receive Interface. 0: Dual-pixel mode. 1: Single-pixel mode. OLDI_IN_MODE is initially loaded from the MODE_SEL0 pin strap options.
			5	RW	0x00	OLDI_IN_SWAP	OLDI Receive input swap: Swaps OLDI input ports. If OLDI_IN_MODE is set to 1 (single), then the secondary port is used. If OLDI_IN_MODE is set to 0 (dual), then the ports are swapped.
			4:2				Reserved.
			1	RW	0x00	CFG_INIT	Initialize Configuration from Non-Volatile Memory: Causes a reload of the configuration data from the non-volatile memory. This bit will be cleared when the initialization is complete.
			0				Reserved.
80	0x50	BRIDGE_STS	7:6				Reserved.
			5	R	0x00	HDCP_INT	HDCP Interrupt Status: Indicates an HDCP Transmitter Interrupt is pending. HDCP Transmit interrupts are serviced through the HDCP Interrupt Control and Status registers.
			4	R		INIT_DONE	Initialization Done: Initialization sequence has completed. This step will complete after configuration complete (CFG_DONE).
			3				Reserved.
			2	R	0x00	CFG_DONE	Configuration Complete: Indicates automatic configuration has completed. This step will complete prior to initialization complete (INIT_DONE).
			1	R	0x01	CFG_CKSUM	Configuration checksum status: Indicates result of Configuration checksum during initialization. The device verifies the 2's complement checksum in the last 128 bytes of the EEPROM. A value of 1 indicates the checksum passed.
			0				Reserved.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
84	0x54	BRIDGE_CFG	7:3				Reserved.
			2	RW	0x00	AUDIO_TDM	Enable TDM Audio: Setting this bit to a 1 will enable TDM audio for the I2S audio. Parallel I2S data on the I2S pins will be serialized onto a single I2S_DA signal for sending over the serial link.
			1	RW	0x01	AUDIO_MODE	Audio Mode: Selects source for audio to be sent over the FPD-Link III downstream link. 0 :Disabled. 1 : I2S audio from I2S pins.
			0				Reserved.
84	0x55	AUDIO_CFG	7	RW	0x00	TDM_2_PARALLEL	EnableTDM to parallel I2S audio conversion: When this bit is set, the TDM to parallel I2S conversion is enabled. TDM audio data on the I2S_DA pin will be split onto four I2S data signals.
			6:0				Reserved.
87	0x57	TDM_CONFIG	7:4				Reserved.
			3	RW	0x00	TDM_FS_MODE	TDM Frame Sync Mode: Sets active level for the Frame Sync for the TDM audio. The Frame Sync signal provides an active pulse to indicate the first sample data on the TDM data signal. 0 : Active high Frame Sync. 1 : Active low Frame Sync (similar to I2S word select). This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
			2	RW	0x00	TDM_DELAY	TDM Data Delay: Controls data delay for TDM audio samples from the active Frame Sync edge. 0 : Data is not delayed from Frame Sync (data is left justified). 1 : Data is delayed 1 bit from Frame Sync. This bit is used for both the output of the I2S to TDM conversion and the input of the TDM to I2S conversion.
			1:0	RW	0x02	TDM_FS_WIDTH	TDM Frame Sync Width: Indicates width of TDM Frame Sync pulse for I2S to TDM conversion. 00 : FS is 50/50 duty cycle. 01 : FS is one slot/channel wide. 1x : FS is 1 clock pulse wide.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
90	0x5A	DUAL_STS	7	R	0x00	FPD3_LINK_RDY	FPD-Link III Ready: This bit indicates that the FPD-Link III has detected a valid downstream connection and determined capabilities for the downstream link.
			6	R		FPD3_TX_STS	FPD-Link III transmit status: This bit indicates that the FPD-Link III transmitter is active and the receiver is LOCKED to the transmit clock. It is only asserted once a valid input has been detected, and the FPD-Link III transmit connection has entered the correct mode (Single vs. Dual mode).
			5:4	R		FPD3_PORT_STS	FPD-Link III Port Status: If FPD3_TX_STS is set to a 1, this field indicates the port mode status as follows: 00: Dual FPD-Link III Transmitter mode. 01: Single FPD-Link III Transmit on port 0. 10: Single FPD-Link III Transmit on port 1. 11: Replicate FPD-Link III Transmit on both ports.
			3	R		OLDI_CLK_DET	OpenLDI clock detect indication from the OpenLDI PLL controller.
			2	R		OLDI_PLL_LOCK	OpenLDI PLL lock status: Indicates the OpenLDI PLL has locked to the incoming OpenLDI clock.
			1	R		NO_OLDI_CLK	No OpenLDI clock detected: This bit indicates the Frequency Detect Circuit did not detect an OpenLDI clock greater than the value specified in the FREQ_LOW register.
			0	R		FREQ_STABLE	OLDI Frequency is stable: Indicates the Frequency Detection circuit has detected a stable OLDI clock frequency.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
91	0x5B	DUAL_CTL1	7	RW	Strap	FPD3_COAX_MODE	FPD-Link III Coax Mode: Enables configuration for the FPD-Link III Interface cabling type: 0 : Twisted Pair. 1 : Coax. This bit is loaded from the MODE_SEL1 pin at power-up.
			6	RW	0x20	DUAL_SWAP	Dual Swap Control: Indicates current status of the Dual Swap control. If automatic correction of Dual Swap is disabled via the DISABLE_DUAL_SWAP control, this bit may be modified by software.
			5	RW		RST_PLL_FREQ	Reset FPD-Link III PLL on Frequency Change: When set to a 1, frequency changes detected by the Frequency Detect circuit will result in a reset of the FPD3 PLL.
			4	RW		FREQ_DET_PLL	Frequency Detect Select PLL Clock. Determines the clock source for the Frequency detection circuit: 0 : OpenLDI clock (prior to PLL). 1: OpenLDI PLL clock.
			3	RW		DUAL_ALIGN_DE	Dual Align on DE: In dual-link mode, if this bit is set to a 1, the odd/even data will be sent on the primary/secondary links respectively, based on the assertion of DE. If this bit is set to a 0, data will be sent on alternating links without regard to odd/even pixel position.
			2	RW		DISABLE_DUAL	Disable Dual Mode: During Auto-detect operation, setting this bit to a 1 will disable Dual FPD-Link III operation. 0: Normal Auto-detect operation. 1: Only Single or Replicate operation supported. This bit will have no effect if FORCE_LINK is set.
			1	RW		FORCE_DUAL	Force dual mode: When FORCE_LINK bit is set, the value on this bit controls single versus dual operation: 0: Single FPD-Link III Transmitter mode. 1: Dual FPD-Link III Transmitter mode.
			0	RW		FORCE_LINK	Force Link Mode: Forces link to dual or single mode, based on the FORCE_DUAL control setting. If this bit is 0, mode setting will be automatically set based on downstream device capabilities as well as the incoming data frequency. 1 : Forced Single or Dual FPD-Link III mode. 0 : Auto-Detect FPD-Link III mode.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
92	0x5C	DUAL_CTL2	7	RW	0x00	DISABLE_DUAL_SWAP	Disable Dual Swap: Prevents automatic correction of swapped Dual link connection. Setting this bit allows writes to the DUAL_SWAP control in the DUAL_CTL1 register.
			6	RW		FORCE_LINK_RDY	Force Link Ready. Forces link ready indication, bypassing back channel link detection.
			5	RW		FORCE_CLK_DET	Force Clock Detect. Forces the OpenLDI clock detect circuit to indicate presence of a valid input clock. This bypasses the clock detect circuit, allowing operation with an input clock that does not meet frequency or stability requirements.
			4:3	RW		FREQ_STBL_THR	Frequency Stability Threshold: The Frequency detect circuit can be used to detect a stable clock frequency. The Stability Threshold determines the amount of time required for the clock frequency to stay within the FREQ_HYST range to be considered stable: 00 : 160us. 01 : 640us. 10 : 1.28ms. 11 : 2.55ms.
			2:0	RW	0x02	FREQ_HYST	Frequency Detect Hysteresis: The Frequency detect hysteresis setting allows ignoring minor fluctuations in frequency. A new frequency measurement will be captured only if the measured frequency differs from the current measured frequency by more than the FREQ_HYST setting. The FREQ_HYST setting is in MHz.
93	0x5D	FREQ_LOW	7				Reserved.
			6	RW	0x00	OLDI_RST_MODE	OLDI Phy Reset Mode: 0 : Reset OLDI Phy on change in mode or frequency. 1 : Don't reset OLDI Phy on change in mode or frequency.
			5:0	RW	0x06	FREQ_LO_THR	Frequency Low Threshold: Sets the low threshold for the OLDI Clock frequency detect circuit in MHz. This value is used to determine if the OLDI clock frequency is too low for proper operation.
94	0x5E	FREQ_HIGH	7				Reserved.
			6:0	RW	44	FREQ_HI_THR	Frequency High Threshold: Sets the high threshold for the OLDI Clock frequency detect circuit in MHz.
95	0x5F	OpenLDI Frequency	7:0	R	0x00	OLDI_FREQ	OLDI Pixel Frequency: Returns the value of the OLDI pixel Frequency of the video data. This register indicates the pixel rate for the incoming data. If the OLDI interface is in single-pixel mode, the pixel frequency is the same as the OLDI frequency. If the OLDI interface is in dual-pixel mode, the pixel frequency is 2x the OLDI frequency. A value of 0 indicates the OLDI receiver is not detecting a valid signal. When the OpenLDI input is suddenly removed, this register will retain its value.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
96	0x60	SPI_TIMING1	7:4	RW	0x02	SPI_HOLD	SPI Data Hold from SPI clock: These bits set the minimum hold time for SPI data following the SPI clock sampling edge. In addition, this also sets the minimum active pulse width for the SPI output clock. Hold = (SPI_HOLD + 1) * 40ns. For example, default setting of 2 will result in 120ns data hold time.
			3:0	RW	0x02	SPI_SETUP	SPI Data Setup to SPI Clock: These bits set the minimum setup time for SPI data to the SPI clock active edge. In addition, this also sets the minimum inactive width for the SPI output clock. Setup = (SPI_SETUP + 1) * 40ns. For example, default setting of 2 will result in 120ns data setup time.
97	0x61	SPI_TIMING2	7:4				Reserved.
			3:0	RW	0x00	SPI_SS_SETUP	SPI Slave Select Setup: This field controls the delay from assertion of the Slave Select low to initial data timing. Delays are in units of 40ns. Delay = (SPI_SS_SETUP + 1) * 40ns.
98	0x62	SPI_CONFIG	7	R	0x00	SPI_MSTR_OVER	SPI Master Overflow Detection: This flag is set if the SPI Master detects an overflow condition. This occurs if the SPI Master is unable to regenerate the remote SPI data at a fast enough rate to keep up with data arriving from the remote Deserializer. If this condition occurs, it suggests the SPI_SETUP and SPI_HOLD times should be set to smaller values. This flag is cleared by setting the SPI_CLR_OVER bit in this register.
			6:3				Reserved.
			2	RW	0x00	SPI_CLR_OVER	Clear SPI Master Overflow Flag: Setting this bit to 1 will clear the SPI Master Overflow Detection flag (SPI_MSTR_OVER). This bit is not self-clearing and must be set back to 0.
			1	R	0x00	SPI_CPHA	SPI Clock Phase setting: Determines which phase of the SPI clock is used for sampling data. 0: Data sampled on leading (first) clock edge. 1: Data sampled on trailing (second) clock edge. This bit is read-only, with a value of 0. The DS90UH947-Q1 does not support CPHA of 1.
			0	RW	0x00	SPI_CPOL	SPI Clock Polarity setting: Determines the base (inactive) value of the SPI clock. 0: base value of the clock is 0. 1: base value of the clock is 1. This bit affects both capture and propagation of SPI signals.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
100	0x64	Pattern Generator Control	7:4	RW	0x10	Pattern Generator Select	Fixed Pattern Select Selects the pattern to output when in Fixed Pattern Mode. Scaled patterns are evenly distributed across the horizontal or vertical active regions. This field is ignored when Auto-Scrolling Mode is enabled. xxxx: normal/inverted. 0000: Checkerboard. 0001: White/Black (default). 0010: Black/White. 0011: Red/Cyan. 0100: Green/Magenta. 0101: Blue/Yellow. 0110: Horizontal Black-White/White-Black. 0111: Horizontal Black-Red/White-Cyan. 1000: Horizontal Black-Green/White-Magenta. 1001: Horizontal Black-Blue/White-Yellow. 1010: Vertical Black-White/White-Black. 1011: Vertical Black-Red/White-Cyan. 1100: Vertical Black-Green/White-Magenta. 1101: Vertical Black-Blue/White-Yellow. 1110: Custom color (or its inversion) configured in PGRS, PGGS, PGBS registers. 1111: VCOM. See TI App Note AN-2198.
			3				***Reserved.***
			2	RW		Color Bars Pattern	Enable color bars: 0: Color Bars disabled (default). 1: Color Bars enabled. Overrides the selection from reg_0x64[7:4].
			1	RW		VCOM Pattern Reverse	Reverse order of color bands in VCOM pattern: 0: Color sequence from top left is (YCBR) (default). 1: Color sequence from top left is (RBCY).
			0	RW		Pattern Generator Enable	Pattern Generator enable: 0: Disable Pattern Generator (default). 1: Enable Pattern Generator.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
101	0x65	Pattern Generator Configuration	7		0x00		***Reserved.***
			6	RW		Checkerboard Scale	Scale Checkered Patterns: 0: Normal operation (each square is 1x1 pixel) (default). 1: Scale checkered patterns (VCOM and checkerboard) by 8 (each square is 8x8 pixels). Setting this bit gives better visibility of the checkered patterns.
			5	RW		Custom Checkerboard	Use Custom Checkerboard Color: 0: Use white and black in the Checkerboard pattern (default). 1: Use the Custom Color and black in the Checkerboard pattern.
			4	RW		PG 18–bit Mode	18-bit Mode Select: 0: Enable 24-bit pattern generation. Scaled patterns use 256 levels of brightness (default). 1: Enable 18-bit color pattern generation. Scaled patterns will have 64 levels of brightness and the R, G, and B outputs use the six most significant color bits.
			3	RW		External Clock	Select External Clock Source: 0: Selects the internal divided clock when using internal timing (default). 1: Selects the external pixel clock when using internal timing. This bit has no effect in external timing mode (PATGEN_TSEL = 0).
			2	RW		Timing Select	Timing Select Control: 0: The Pattern Generator uses external video timing from the pixel clock, Data Enable, Horizontal Sync, and Vertical Sync signals (default). 1: The Pattern Generator creates its own video timing as configured in the Pattern Generator Total Frame Size, Active Frame Size. Horizontal Sync Width, Vertical Sync Width, Horizontal Back Porch, Vertical Back Porch, and Sync Configuration registers. See TI App Note AN-2198.
			1	RW		Color Invert	Enable Inverted Color Patterns: 0: Do not invert the color output (default). 1: Invert the color output. See TI App Note AN-2198.
			0	RW		Auto Scroll	Auto Scroll Enable: 0: The Pattern Generator retains the current pattern (default). 1: The Pattern Generator will automatically move to the next enabled pattern after the number of frames specified in the Pattern Generator Frame Time (PGFT) register. See TI App Note AN-2198.
102	0x66	PGIA	7:0	RW	0x00	PG Indirect Address	This 8-bit field sets the indirect address for accesses to indirectly-mapped registers. It should be written prior to reading or writing the Pattern Generator Indirect Data register. See TI App Note AN-2198

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
103	0x67	PGID	7:0	RW	0x00	PG Indirect Data	When writing to indirect registers, this register contains the data to be written. When reading from indirect registers, this register contains the read back value. See TI App Note AN-2198
112	0x70	Slave ID[1]	7:1	RW	0x00	Slave ID 1 Port0/Port1	7-bit I2C address of the remote Slave 1 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 1, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 1. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***
113	0x71	Slave ID[2]	7:1	RW	0x00	Slave ID 2 Port0/Port1	7-bit I2C address of the remote Slave 2 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 2, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 2. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***
114	0x72	Slave ID[3]	7:1	RW	0x00	Slave ID 3 Port0/Port1	7-bit I2C address of the remote Slave 3 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 3, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 3. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***
115	0x73	Slave ID[4]	7:1	RW	0x00	Slave ID 4 Port0/Port1	7-bit I2C address of the remote Slave 4 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 4, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 4. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
116	0x74	Slave ID[5]	7:1	RW	0x00	Slave ID 5 Port0/Port1	7-bit I2C address of the remote Slave 5 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 5, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 5. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***
117	0x75	Slave ID[6]	7:1	RW	0x00	Slave ID 6 Port0/Port1	7-bit I2C address of the remote Slave 6 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 6, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 6. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***
118	0x76	Slave ID[7]	7:1	RW	0x00	Slave ID 7 Port0/Port1	7-bit I2C address of the remote Slave 7 attached to the remote Deserializer. If an I2C transaction is addressed to Slave Alias ID 7, the transaction will be remapped to this address before passing the transaction across the Bidirectional Control Channel to the Deserializer. A value of 0 in this field disables access to the remote Slave 7. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***
119	0x77	Slave Alias[1]	7:1	RW	0x00	Slave Alias ID 1 Port0/Port1	7-bit Slave Alias ID of the remote Slave 1 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 1 register. A value of 0 in this field disables access to the remote Slave 1. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***
120	0x78	Slave Alias[2]	7:1	RW	0x00	Slave Alias ID 2 Port0/Port1	7-bit Slave Alias ID of the remote Slave 2 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 2 register. A value of 0 in this field disables access to the remote Slave 2. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***
121	0x79	Slave Alias[3]	7:1	RW	0x00	Slave Alias ID 3 Port0/Port1	7-bit Slave Alias ID of the remote Slave 3 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 3 register. A value of 0 in this field disables access to the remote Slave 3. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
122	0x7A	Slave Alias[4]	7:1	RW	0x00	Slave Alias ID 4 Port0/Port1	7-bit Slave Alias ID of the remote Slave 4 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 4 register. A value of 0 in this field disables access to the remote Slave 4. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***
123	0x7B	Slave Alias[5]	7:1	RW	0x00	Slave Alias ID 5 Port0/Port1	7-bit Slave Alias ID of the remote Slave 5 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 5 register. A value of 0 in this field disables access to the remote Slave 5. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***
124	0x7C	Slave Alias[6]	7:1	RW	0x00	Slave Alias ID 6 Port0/Port1	7-bit Slave Alias ID of the remote Slave 6 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 6 register. A value of 0 in this field disables access to the remote Slave 6. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***
125	0x7D	Slave Alias[7]	7:1	RW	0x00	Slave Alias ID 7 Port0/Port1	7-bit Slave Alias ID of the remote Slave 7 attached to the remote Deserializer. The transaction will be remapped to the address specified in the Slave ID 7 register. A value of 0 in this field disables access to the remote Slave 7. If Port1_SEL is set, this register controls Port1 operation.
			0				***Reserved.***
128	0x80	RX_BKSV0	7:0	R	0x00	BKSV0	BKSV0: Value of byte0 of the Receiver KSV.
129	0x81	RX_BKSV1	7:0	R	0x00	BKSV1	BKSV1: Value of byte1 of the Receiver KSV.
130	0x82	RX_BKSV2	7:0	R	0x00	BKSV2	BKSV2: Value of byte2 of the Receiver KSV.
131	0x83	RX_BKSV3	7:0	R	0x00	BKSV3	BKSV3: Value of byte3 of the Receiver KSV.
132	0x84	RX_BKSV4	7:0	R	0x00	BKSV4	BKSV4: Value of byte4 of the Receiver KSV.
144	0x90	TX_KSV0	7:0	R	0x00	TX_KSV0	TX_KSV0: Value of byte0 of the Transmitter KSV.
145	0x91	TX_KSV1	7:0	R	0x00	TX_KSV1	TX_KSV1: Value of byte1 of the Transmitter KSV.
146	0x92	TX_KSV2	7:0	R	0x00	TX_KSV2	TX_KSV2: Value of byte2 of the Transmitter KSV.
147	0x93	TX_KSV3	7:0	R	0x00	TX_KSV3	TX_KSV3: Value of byte3 of the Transmitter KSV.
148	0x94	TX_KSV4	7:0	R	0x00	TX_KSV4	TX_KSV4: Value of byte4 of the Transmitter KSV.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
160	0xA0	RX_BCAPS	7				Reserved.
			6	R	0x00	Repeater	Repeater: Indicates if the attached Receiver supports downstream connections. This bit is valid once the Bksv is ready as indicated by the BKSV_RDY bit in the HDCP.
			5	R	0x00	KSV_FIFO_RDY	KSV FIFO Ready: Indicates the receiver has built the list of attached KSVs and computed the verification value V'.
			4	R	0x01	FAST_I2C	Fast I2C: The HDCP Receiver supports fast I2C. Since the I2C is embedded in the serial data, this bit is not relevant.
			3:2	R			Reserved.
			1	R	0x01	FEATURES_1_1	1.1_Features: The HDCP Receiver supports the Enhanced Encryption Status Signaling (EESS), Advance Cipher, and Enhanced Link Verification options.
			0	R	0x01	FAST_REAUTH	Fast Reauthentication: The HDCP Receiver is capable of receiving (unencrypted) video signal during the session re-authentication.
161	0xA1	RX_BSTATUS0	7	R	0x00	MAX_DEVS_EXCEEDED	Maximum Devices Exceeded: Indicates a topology error was detected. Indicates the number of downstream devices has exceeded the depth of the Repeater's KSV FIFO.
			6:0	R		DEVICE_COUNT	Device Count: Total number of attached downstream device. For a Repeater, this will indicate the number of downstream devices, not including the Repeater. For an HDCP Receiver that is not also a Repeater, this field will be 0.
162	0xA2	RX_BSTATUS1	7:4				Reserved.
			3	R	0x00	MAX_CASC_EXCEEDED	Maximum Cascade Exceeded: Indicates a topology error was detected. Indicates that more than seven levels of repeaters have been cascad-ed together.
			2:0	R		Cascade Depth	Cascade Depth: Indicates the number of attached levels of devices for the Repeater.
163	0xA3	KSV_FIFO	7:0	R	0x00	KSV_FIFO	KSV FIFO: Each read of the KSV FIFO returns one byte of the KSV FIFO list composed by the downstream Receiver.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
192	0xC0	HDCP_DBG	7		0x00		Reserved.
			6	RW		HDCP_I2C_TO_DIS	HDCP I2C Timeout Disable: Setting this bit to a 1 will disable the bus timeout function in the HDCP I2C master. When enabled, the bus timeout function allows the I2C master to assume the bus is free if no signaling occurs for more than 1 second.
			5				Reserved.
			4	RW		DIS_RI_SYNC	Disable Ri Synchronization check: Ri is normally checked both before and after the start of frame 128. The check at frame 127 ensures synchronization between the two. Setting this bit to a 1 will disable the check at frame 127.
			3	RW		RGB_CHKSUM_EN	Enable RBG video line checksum: Enables sending of ones-complement checksum for each 8-bit RBG data channel following end of each video data line.
			2	RW		FC_TESTMODE	Frame Counter Testmode: Speeds up frame counter used for Pj and Ri verification. When set to a 1, Pj is computed every 2 frames and Ri is computed every 16 frames. When set to a 0, Pj is computed every 16 frames and Ri is computed every 128 frames.
			1	RW		TMR_SPEEDUP	Timer Speedup: Speed up HDCP authentication timers.
			0	RW		HDCP_I2C_FAST	HDCP I2C Fast Mode Enable: Setting this bit to a 1 will enable the HDCP I2C Master in the HDCP Receiver to operation with Fast mode timing. If set to a 0, the I2C Master will operation with Standard mode timing. This bit is mirrored in the IND_STS register.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
194	0xC2	HDCP_CFG	7	RW	0x80	ENH_LV	Enable Enhanced Link Verification: Enables enhanced link verification. Allows checking of the encryption Pj value on every 16th frame. 1 = Enhanced Link Verification enabled. 0 = Enhanced Link Verification disabled.
			6	RW		HDCP_EESS	Enable Enhanced Encryption Status Signaling: Enables Enhanced Encryption Status Signaling (EESS) instead of the Original Encryption Status Signaling (OESS). 1 = EESS mode enabled. 0 = OESS mode enabled.
			5	RW		TX_RPTR	Transmit Repeater Enable: Enables the transmitter to act as a repeater. In this mode, the HDCP Transmitter incorporates the additional authentication steps required of an HDCP Repeater. 1 = Transmit Repeater mode enabled. 0 = Transmit Repeater mode disabled.
			4:3	RW		ENC_MODE	Encryption Control Mode: Determines mode for controlling whether encryption is required for video frames. 00 = Enc_Authenticated. 01 = Enc_Reg_Control. 10 = Enc_Always. 11 = Enc_InBand_Control (per frame). If the Repeater strap option is set at power-up, Enc_InBand_Control (ENC_MODE == 11) will be se-lected. Otherwise, the default will be Enc_Authenticated mode (ENC_MODE == 00).
			2	RW		WAIT_100MS	Enable 100MS Wait: The HDCP 1.3 specification allows for a 100Ms wait to allow the HDCP Receiver to compute the initial encryption values. The FPD-LinkIII implementation guarantees that the Receiver will complete the computations before the HDCP Transmitter. Thus the timer is unnecessary. To enable the 100ms timer, set this bit to a 1.
			1	RW		RX_DET_SEL	RX Detect Select: Controls assertion of the Receiver Detect Interrupt. If set to 0, the Receiver Detect Interrupt will be asserted on detection of an FPD-Link III Receiver. If set to 1, the Receiver Detect Interrupt will also require a receive lock indication from the receiver.
			0	RW		HDCP_AVMUTE	Enable AVMUTE: Setting this bit to a 1 will initiate AVMUTE operation. The transmitter will ignore encryption status controls while in this state. If this bit is set to a 0, normal operation will resume. This bit may only be set if the HDCP_EESS bit is also set.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
195	0xC3	HDCP_CTL	7	RW	0x00	HDCP_RST	HDCP Reset : Setting this bit will reset the HDCP transmitter and dis-able HDCP authentication. This bit is self-clearing.
			6				Reserved.
			5	RW	0x00	KSV_LIST_VALID	KSV List Valid : The controller sets this bit after validating the Repeater's KSV List against the Key revocation list. This allows completion of the Authentication process. This bit is self-clearing.
			4	RW		KSV_VALID	KSV Valid : The controller sets this bit after validating the Receiver's KSV against the Key revocation list. This allows continuation of the Authentication process. This bit will be cleared upon assertion of the KSV_RDY flag in the HDCP_STS register. Setting this bit to a 0 will have no effect.
			3	RW		HDCP_ENC_DIS	HDCP Encrypt Disable : Disables HDCP encryption. Setting this bit to a 1 will cause video data to be sent without encryption. Authen-tication status will be maintained. This bit is self-clearing.
			2	RW		HDCP_ENC_EN	HDCP Encrypt Enable : Enables HDCP encryption. When set, if the device is authenticated, encrypted data will be sent. If device is not authenticated, a blue screen will be sent. Encryption should always be enabled when video data requiring content protection is being supplied to the transmitter. When this bit is not set, video data will be sent without encryption. Note that when CFG_ENC_MODE is set to Enc_Always, this bit will be read only with a value of 1.
			1	RW		HDCP_DIS	HDCP Disable: Disables HDCP authentication. Setting this bit to a 1 will disable the HDCP authentication. This bit is self-clearing.
			0	RW		HDCP_EN	HDCP Enable/Restart: Enables HDCP authentication. If HDCP is already en-abled, setting this bit to a 1 will restart authentication. Setting this bit to a 0 will have no effect. A register read will return the current HDCP enabled status.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
196	0xC4	HDCP_STS	7	R	0x00	I2C_ERR_DET	HDCP I2C Error Detected: This bit indicates an error was detected on the embedded communications channel with the HDCP Receiver. Setting of this bit might indicate that a problem exists on the link between the HDCP Transmitter and HDCP Receiver. This bit will be cleared on read.
			6	R		RX_INT	RX Interrupt : Status of the RX Interrupt signal. The signal is received from the attached HDCP Receiver and is the status on the INTB_IN pin of the HDCP Receiver. The signal is active low, so a 0 indicates an interrupt condition.
			5	R		RX_LOCK_DET	Receiver Lock Detect : This bit indicates that the downstream Receiver has indicated Receive Lock to incoming serial data.
			4	R		DOWN_HPD	Downstream Hot Plug Detect: This bit indicates a downstream repeater has reported a Hot Plug event, indicating addition of a new receiver. This bit will be cleared on read.
			3	R		RX_DETECT	Receiver Detect : This bit indicates that a downstream Receiver has been detected.
			2	R		KSV_LIST_RDY	HDCP Repeater KSV List Ready : This bit indicates that the Receiver KSV list has been read and is available in the KSV_FIFO registers. The device will wait for the controller to set the KSV_LIST_VALID bit in the HDCP_CTL register before continuing. This bit will be cleared once the controller sets the KSV_LIST_VALID bit.
			1	R		KSV_RDY	HDCP Receiver KSV Ready : This bit indicates that the Receiver KSV has been read and is available in the HDCP_BKSV registers. If the de-vice is not a Repeater, it will wait for the controller to set the KSV_VALID bit in the HDCP_CTL register before continuing. This bit will be cleared once the controller sets the KSV_VALID bit.
			0	R		AUTHED	HDCP Authenticated: Indicates the HDCP authentication has completed successfully. The controller may now send video data re-quiring content protection. This bit will be cleared if authentication is lost or if the controller restarts authen-tication.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
198	0xC6	ICR	7	RW	0x00	IE_IND_ACC	Interrupt on Indirect Access Complete: Enables interrupt on completion of Indirect Register Access.
			6	RW		IE_RXDET_INT	Interrupt on Receiver Detect: Enables interrupt on detection of a downstream Receiver. If HDCP_CFG:RX_DET_SEL is set to a 1, the interrupt will wait for Receiver Lock Detect.
			5	RW		IE_RX_INT	Interrupt on Receiver interrupt: Enables interrupt on indication from the HDCP Receiver. Allows propagation of interrupts from downstream devices.
			4	RW	0x00	IE_LIST_RDY	Interrupt on KSV List Ready: Enables interrupt on KSV List Ready.
			3	RW		IE_KSV_RDY	Interrupt on KSV Ready: Enables interrupt on KSV Ready.
			2	RW		IE_AUTH_FAIL	Interrupt on Authentication Failure: Enables interrupt on authentication failure or loss of authentication.
			1	RW		IE_AUTH_PASS	Interrupt on Authentication Pass: Enables interrupt on successful completion of authentication.
			0	RW		INT_EN	Global Interrupt Enable: Enables interrupt on the interrupt signal to the controller.
199	0xC7	ISR	7	R	0x00	IS_IND_ACC	Interrupt on Indirect Access Complete: Indirect Register Access has completed.
			6	R		IS_RXDET_INT	Interrupt on Receiver Detect interrupt: A downstream receiver has been detected. If HDCP_CFG:RX_DET_SEL is set to a 1, the interrupt will wait for Receiver Lock Detect.
			5	R		IS_RX_INT	Interrupt on Receiver interrupt: Receiver has indicated an interrupt request from down-stream device.
			4	R	0x00	IS_LIST_RDY	Interrupt on KSV List Ready: The KSV list is ready for reading by the controller.
			3	R		IS_KSV_RDY	Interrupt on KSV Ready: The Receiver KSV is ready for reading by the controller.
			2	R		IS_AUTH_FAIL	Interrupt on Authentication Failure: Authentication failure or loss of authentication has occurred.
			1	R		IS_AUTH_PASS	Interrupt on Authentication Pass: Authentication has completed successfully.
			0	R		INT	Global Interrupt: Set if any enabled interrupt is indicated.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
200	0xC8	NVM_CTL	7	R	0x00	NVM_PASS	NVM Verify pass: This bit indicates the completion status of the NVM verification process. This bit is valid only when NVM_DONE is asserted. 0: NVM Verify failed. 1: NVM Verify passed.
			6	R		NVM_DONE	NVM Verify done: This bit indicates that the NVM Verifcation has completed.
			5	RW			Reserved.
			4:3	R			Reserved.
			2	RW	0x00	NVM_VFY	NVM Verify: Setting this bit will enable a verification of the NVM con-tents. This is done by reading all NVM keys, computing a SHA-1 hash value, and verifying against the SHA-1 hash stored in NVM. This bit will be cleared upon com-pletion of the NVM Verification.
			1	RW			Reserved.
			0	RW			Reserved.
206	0xCE	BLUE_SCREEN	7:0	RW	0xFF	BLUE_SCREEN_VAL	Blue Screen Data Value: Provides the 8-bit data value sent on the Blue channel when the HDCP Transmitter is sending a blue screen.
208	0xD0	IND_STS	7	RW	0x00	IA_RST	Indirect Access Reset: Setting this bit to a 1 will reset the I2C Master in the HDCP Receiver. As this may leave the I2C bus in an indeterminate state, it should only be done if the Indirect Access mechanism is not able to complete due to an error on the destination I2C bus.
			6	RW		I2C_TO_SPEED	I2C Timer Speedup: For diagnostic purposes allow speedup of of the 1 second idle timer to 50us. Texas Instruments use only, should be marked as Reserved in datasheet.
			5	RW		I2C_TO_DIS	I2C Timeout Disable: Setting this bit to a 1 will disable the bus timeout function in the I2C master. When enabled, the bus timeout function allows the I2C master to assume the bus is free if no signaling occurs for more than 1 second.
			4	RW		I2C_FAST	I2C Fast mode Enable: Setting this bit to a 1 will enable the I2C Master in the HDCP Receiver to operation with Fast mode timing. If set to a 0, the I2C Master will operation with Standard mode timing.
			3:2				Reserved.
			1	R	0x00	IA_ACK	Indirect Access Acknowledge: The acknowledge bit indicates that a valid acknowledge was received upon completion of the I2C read or write to the slave. A value of 0 indicates the read/write did not complete successfully.
			0	R		IA_DONE	Indirect Access Done: Set to a 1 to indicate completion of Indirect Register Access. This bit will be cleared or read or by start of a new Indirect Register Access.

Table 10. Serial Control Bus Registers (continued)

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
209	0xD1	IND_SAR	7:1	RW	0x00	IA_SADDR	Indirect Access Slave Address: This field should be programmed with the slave address for the I2C slave to be accessed.
			0	RW		IA_RW	Indirect Access Read/Write: 1 = Read. 0 = Write.
210	0xD2	IND_OAR	7:0	RW	0x00	IA_OFFSET	Indirect Access Offset: This field should be programmed with the register address for the I2C indirect access.
211	0xD3	IND_DATA	7:0	RW	0x00	IA_DATA	Indirect Access Data: For an indirect write, this field should be written with the write data. For an indirect read, this field will contain the result of a successful read.
224	0xE0	HDCP_DBG_ALIAS	7:0	R		HDCP_DBG	Read-only alias of HDCP_DBG register.
226	0xE2	HDCP_CFG_ALIAS	7:0	R		HDCP_CFG	Read-only alias of HDCP_CFG register.
227	0xE3	HDCP_CTL_ALIAS	7:0	R		HDCP_CTL	Read-only alias of HDCP_CTL register.
228	0xE4	HDCP_STS_ALIAS	7:0	R		HDCP_STS	Read-only alias of HDCP_STS register.
230	0xE6	HDCP_ICR_ALIAS	7:0	R		HDCP_ICR	Read-only alias of HDCP_ICR register.
231	0xE7	HDCP_ISR_ALIAS	7:0	R		HDCP_ISR	Read-only alias of HDCP_ISR register.
240	0xF0	TX ID	7:0	R	0x5F	ID0	First byte ID code: "_".
241	0xF1		7:0	R	0x55	ID1	Second byte of ID code: "U".
242	0xF2		7:0	R	0x48	ID2	Third byte of ID code: "H".
243	0xF3		7:0	R	0x39	ID3	Fourth byte of ID code: "9".
244	0xF4		7:0	R	0x34	ID4	Fifth byte of ID code: "4".
245	0xF5		7:0	R	0x37	ID5	Sixth byte of ID code: “7”.

NOTE

Registers 0x40, 0x41, and 0x42 of the Serial Control Bus Registers are used to access the Page 0x10 registers.

Table 11. Page 0x10 Registers

ADD (dec)	ADD (hex)	REGISTER NAME	BIT(S)	REGISTER TYPE	DEFAULT (hex)	FUNCTION	DESCRIPTION
71	0x47	OVERRIDE	7	RW	0x00	REG_OV_CLK_DIV_RSTN	Override bit for reset divider
			6				Reserved, when writing to this register always write 0b to this bit.
			5	RW		REG_OV_PLL_LOCK	Enable PLL lock override bit
			4:0				Reserved, when writing to this register always write 00000b to these bits.
73	0x49	STATE_MACHINE_OVERRIDE	7:5		0x00		Reserved
			4	RW		REG_OV_STATE	Enable State Machine override bit 0: Normal operation (default) 1: Enable override
			3:0	RW		REG_STATE	0000b: Reset 0001b - 0101b: Reserved 0110: PFD_CLOSE_LOOP_TIMER 0111b - 1111b: Reserved

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Applications Information

The DS90UH947-Q1, in conjunction with the DS90UH940-Q1/DS90UH948-Q1 deserializer, is intended to interface between a host (graphics processor) and a display, supporting 24-bit color depth (RGB888) and high definition (1080p) digital video format. It can receive an 8-bit RGB stream with a pixel clock rate up to 170 MHz together with four I2S audio streams when paired with the DS90UH940-Q1/DS90UH948-Q1 deserializer.

8.2 Typical Applications

Bypass capacitors should be placed near the power supply pins. A capacitor and resistor are placed on the PDB pin to delay the enabling of the device until power is stable. See below for typical STP and coax connection diagrams.

Typical Applications (continued)

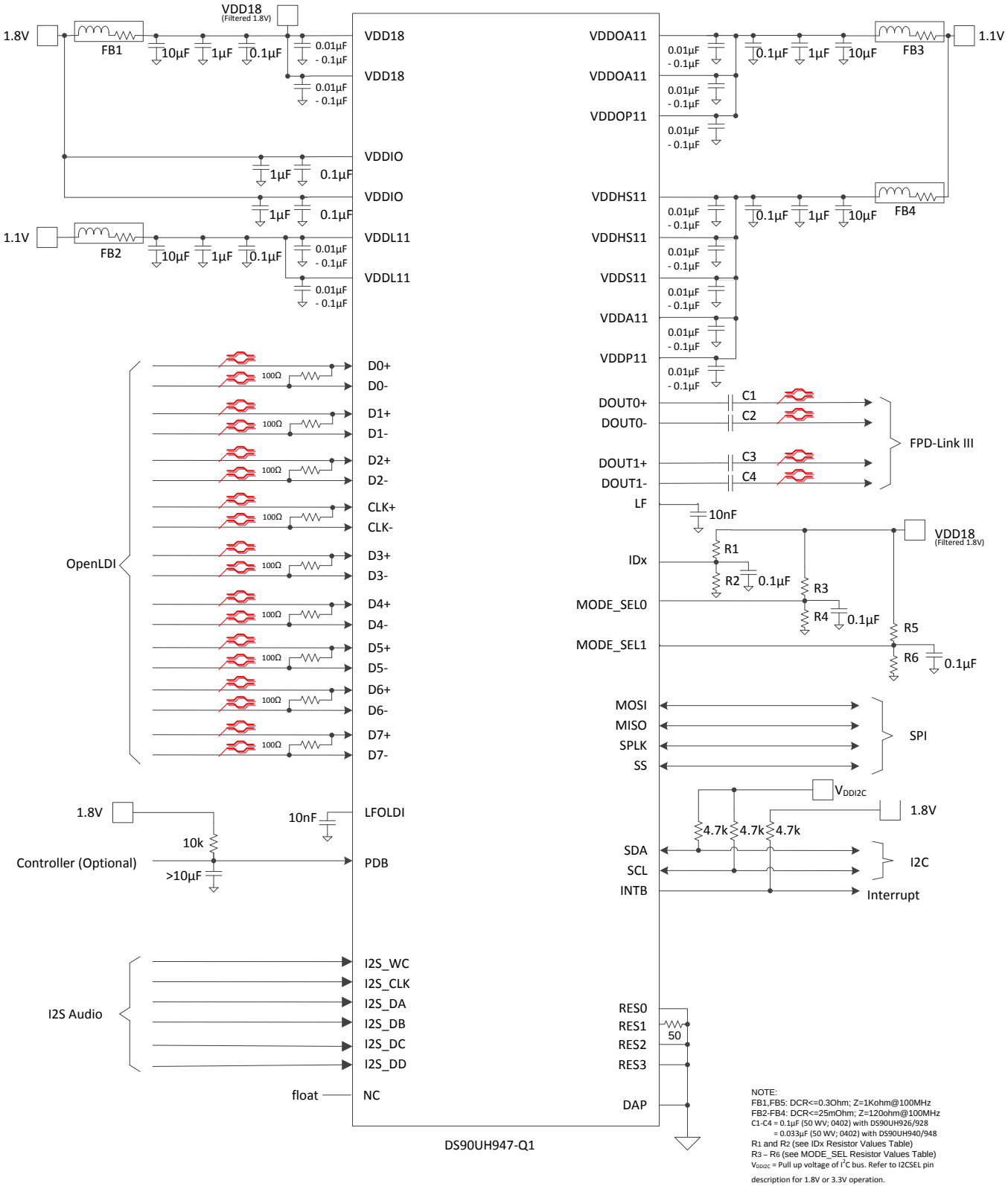


Figure 35. Typical Application Connection -- STP

Typical Applications (continued)

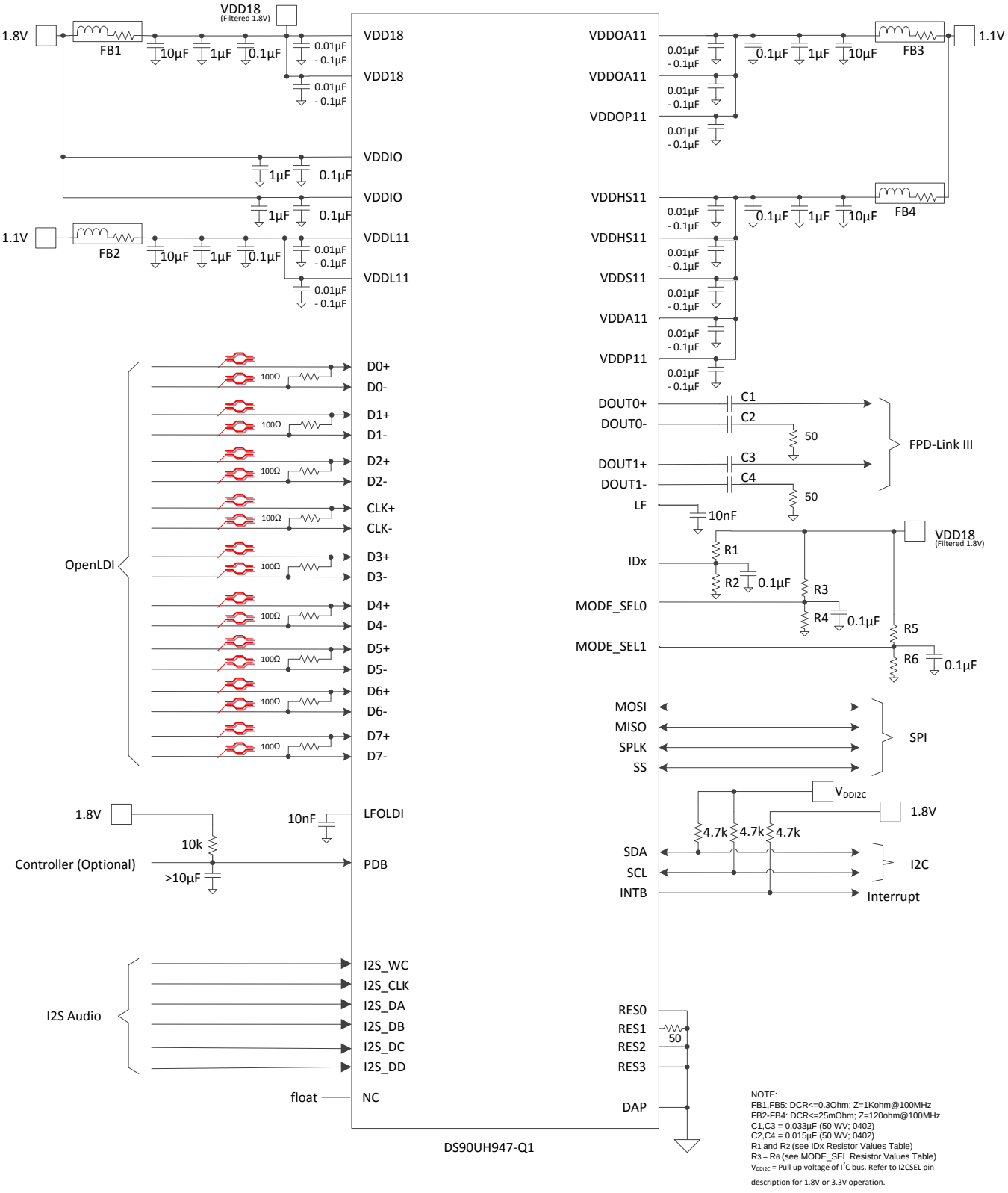
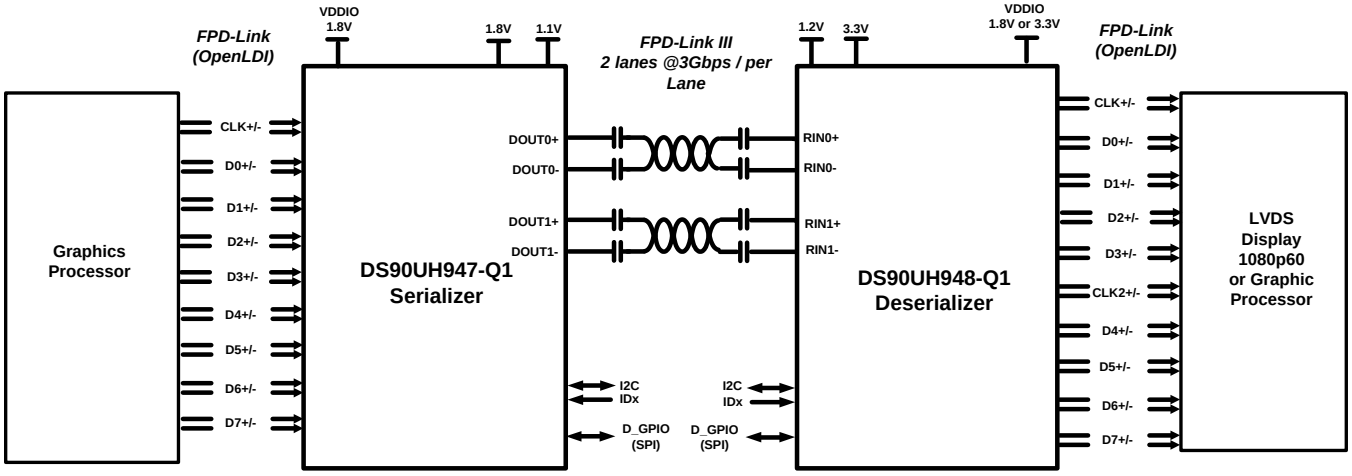


Figure 36. Typical Application Connection -- Coax

Typical Applications (continued)



HDCP – High-Bandwidth Digital Content Protection

Figure 37. Typical System Diagram

8.2.1 Design Requirements

The SER/DES supports only AC-coupled interconnects through an integrated DC-balanced decoding scheme. External AC coupling capacitors must be placed in series in the FPD-Link III signal path as illustrated in Figure 38.

Table 12. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
VDDIO	1.8 V
AC Coupling Capacitor for DOUT0± and DOUT1± with 92x deserializers	100 nF
AC Coupling Capacitor for DOUT0± and DOUT1± with 94x deserializers	33 nF

For applications utilizing single-ended 50Ω coaxial cable, the unused data pins (DOUT0-, DOUT1-) should utilize a 15nF capacitor and should be terminated with a 50Ω resistor.

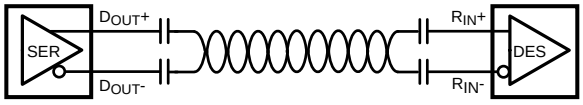


Figure 38. AC-Coupled Connection (STP)

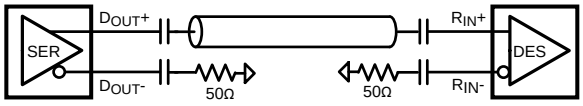


Figure 39. AC-Coupled Connection (Coaxial)

For high-speed FPD–Link III transmissions, the smallest available package should be used for the AC coupling capacitor. This will help minimize degradation of signal quality due to package parasitics.

8.2.2 Detailed Design Procedure

8.2.2.1 High-Speed Interconnect Guidelines

See *AN-1108 Channel-Link PCB and Interconnect Design-In Guidelines* (SNLA008) and *Transmission Line RAPIDESIGNER Operation and Applications Guide* (SNLA035) for full details.

- Use 100-Ω coupled differential pairs
- Use the S/2S/3S rule in spacings
  - S = space between the pair
  - 2S = space between pairs
  - 3S = space to LVCMOS signal
- Minimize the number of Vias
- Use differential connectors when operating above 500Mbps line speed
- Maintain balance of the traces
- Minimize skew within the pair
- Terminate as close to the TX outputs and RX inputs as possible

Additional general guidance can be found in the LVDS Owner's Manual - available in PDF format from the Texas Instruments web site at: *LVDS Owner's Manual* (SNLA187).

8.2.3 Application Curves

8.2.3.1 Application Performance Plots

Figure 40 corresponds to 1080p60 video application with 2-lane FPD-Link III output. Figure 41 corresponds to 3.36-Gbps single-lane output from 96-MHz input OpenLDI clock.

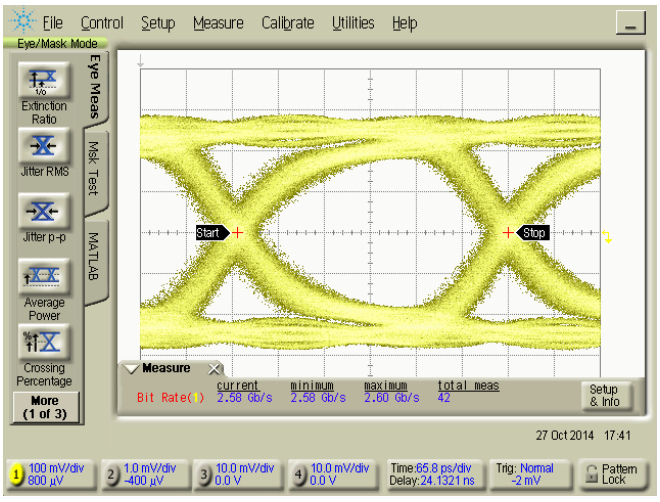


Figure 40. 1080p60 Video at 2.6-Gbps Serial Line Rate (One of Two Lanes)

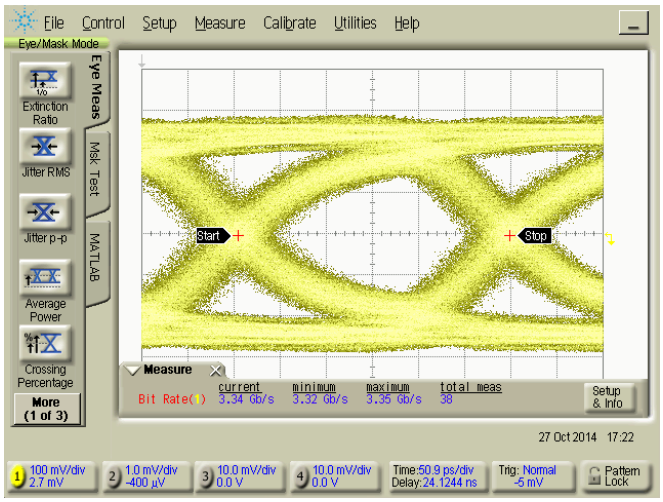


Figure 41. Serializer Output at 3.36 Gbps (96-MHz OpenLDI Clock)

9 Power Supply Recommendations

This device provides separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. The Pin Functions table provides guidance on which circuit blocks are connected to which power pins. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs.

9.1 Power-Up Requirements and PDB Pin

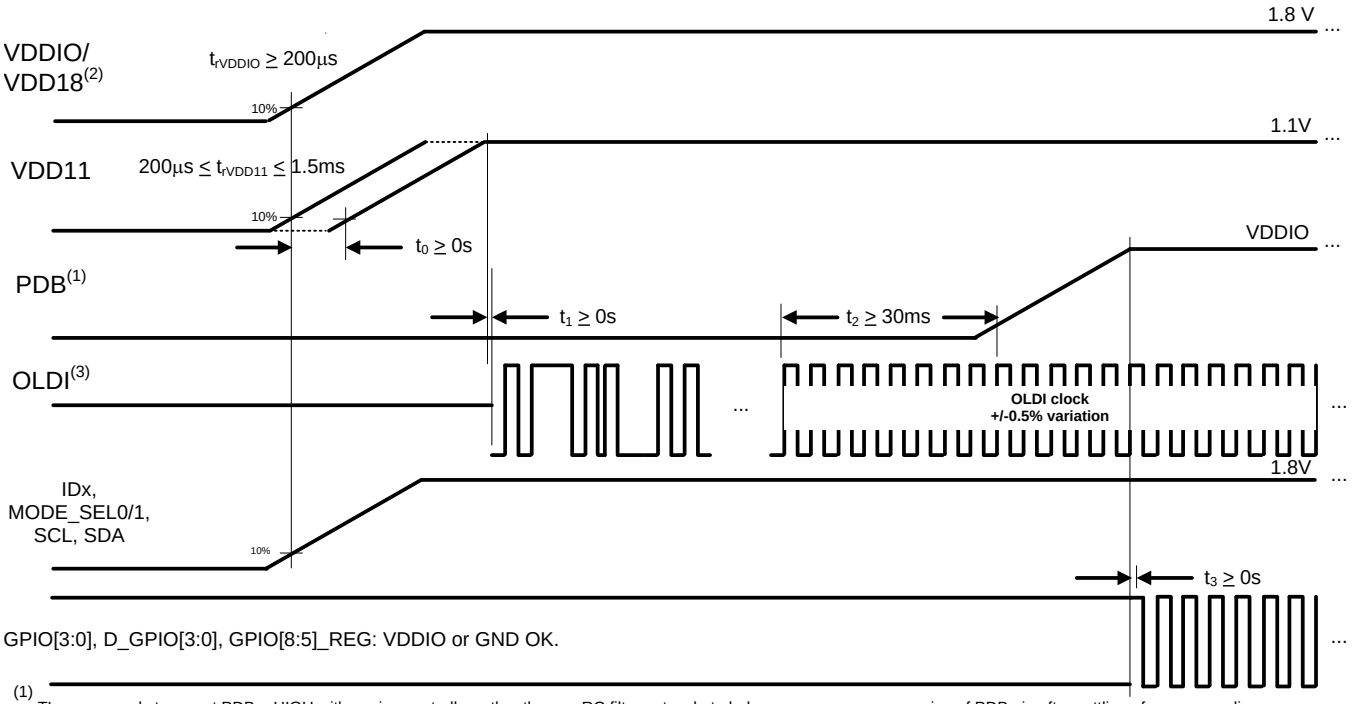
The power supply ramp should be faster than 1.5 ms with a monotonic rise. A large capacitor on the PDB pin is needed to ensure PDB arrives after all the supply pins have settled to the recommended operating voltage. When PDB pin is pulled up to V_{DDIO}, a 10-kΩ pull-up and a >10-µF capacitor to GND are required to delay the PDB input signal rise. All inputs must not be driven until all power supplies have reached steady state.

The recommended power up sequence is as follows:

- V_{DD18}
- V_{DD11}
- Wait until all supplies have settled
- Activate PDB
- Apply OpenLDI input

After power up write the following to the device:

```
Reg0x40=0x10 // select OLDI register
Reg0x41=0x49 // force PLL controller in PPM reset state
Reg0x42=0x16
Reg0x41=0x47 // force PLL LOCK Low
Reg0x42=0x20
Reg0x42=0xA0 // reset PLL divider
Reg0x42=0x20
Reg0x42=0x00 // release PLL LOCK control
Reg0x41=0x49 // release PLL state control
Reg0x42=0x00
```



(1) TI recommends to assert PDB = HIGH with a microcontroller rather than an RC filter network to help ensure proper sequencing of PDB pin after settling of power supplies.
(2) If VDDIO is applied before VDD18, VDDIO will bias to ~0.750mV
(3) Electrical Characteristics of the LVDS should follow TIA/EIA-644-A and OpenLDI specification

Figure 42. Recommended Power Sequencing

10 Layout

10.1 Layout Guidelines

Circuit board layout and stack-up for the LVDS serializer and deserializer devices should be designed to provide low-noise power to the device. Good layout practice will also separate high frequency or high-level inputs and outputs to minimize unwanted stray noise, feedback and interference. Power system performance may be greatly improved by using thin dielectrics (2 to 4 mil) for power / ground sandwiches. This arrangement utilizes the plane capacitance for the PCB power system and has low-inductance, which has proven effectiveness especially at high frequencies, and makes the value and placement of external bypass capacitors less critical. External bypass capacitors should include both RF ceramic and tantalum electrolytic types. RF capacitors may use values in the range of 0.01 μF to 10 μF. Tantalum capacitors may be in the 2.2-μF to 10-μF range. The voltage rating of the tantalum capacitors should be at least 5X the power supply voltage being used.

MLCC surface mount capacitors are recommended due to their smaller parasitic properties. When using multiple capacitors per supply pin, locate the smaller value closer to the pin. A large bulk capacitor is recommended at the point of power entry. This is typically in the 50μF to 100μF range and will smooth low frequency switching noise. It is recommended to connect power and ground pins directly to the power and ground planes with bypass capacitors connected to the plane with via on both ends of the capacitor. Connecting power or ground pins to an external bypass capacitor will increase the inductance of the path. A small body size X7R chip capacitor, such as 0603 or 0805, is recommended for external bypass. A small body sized capacitor has less inductance. The user must pay attention to the resonance frequency of these external bypass capacitors, usually in the range of 20 MHz to 30 MHz. To provide effective bypassing, multiple capacitors are often used to achieve low impedance between the supply rails over the frequency of interest. At high frequency, it is also a common practice to use two vias from power and ground pins to the planes, reducing the impedance at high frequency.

Some devices provide separate power and ground pins for different portions of the circuit. This is done to isolate switching noise effects between different sections of the circuit. Separate planes on the PCB are typically not required. Pin Description tables typically provide guidance on which circuit blocks are connected to which power pin pairs. In some cases, an external filter many be used to provide clean power to sensitive circuits such as PLLs. For DS90UH947-Q1, only one common ground plane is required to connect all device related ground pins.

Use at least a four layer board with a power and ground plane. Locate LVCMOS signals away from the LVDS lines to prevent coupling from the LVCMOS lines to the LVDS lines. Closely coupled differential lines of 100 Ω are typically recommended for LVDS interconnect. The closely coupled lines help to ensure that coupled noise will appear as common mode and thus is rejected by the receivers. The tightly coupled lines will also radiate less.

At least 9 thermal vias are necessary from the device center DAP to the ground plane. They connect the device ground to the PCB ground plane, as well as conduct heat from the exposed pad of the package to the PCB ground plane. More information on the LLP style package, including PCB design and manufacturing requirements, is provided in the *AN-1187 Leadless Leadframe Package (LLP)* (SNOA401).

10.2 Layout Example

Figure 43 is derived from a layout design of the DS90UH947-Q1. This graphic is used to demonstrate proper high-speed routing when designing in the Serializer.

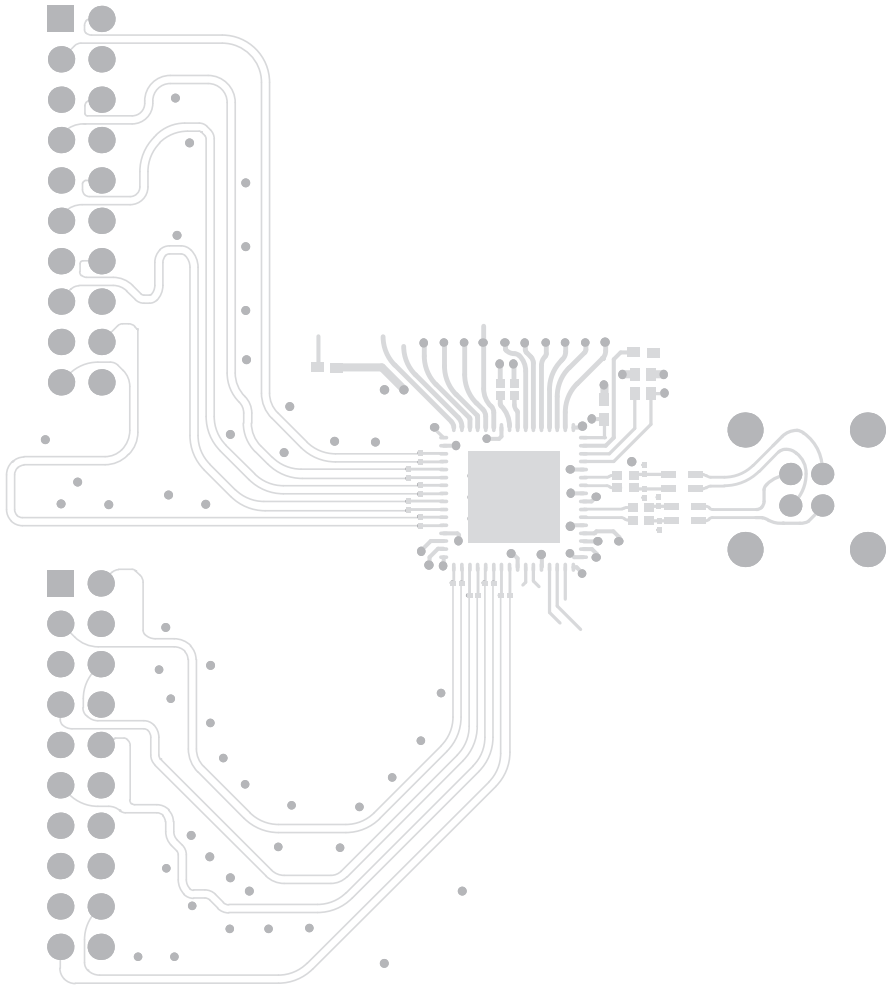


Figure 43. DS90UH947-Q1 Serializer Layout Example

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

- *《焊接的绝对最大额定值》*(SNOA549)
- *《半导体和 IC 封装热指标》*(SPRA953)
- *《AN-1108 通道链路 PCB 和互连设计指南》*(SNLA008)
- *《传输线路 RAPIDESIGNER 操作和 应用 指南》*(SNLA035)
- *《AN-1187 无引线框架封装 (LLP)》*(SNOA401)
- *《LVDS 用户手册》*(SNLA187)
- *《通过具有双向控制通道的 FPD-Link III 进行 I2C 通信》*(SNLA131)
- *《使用 DS90Ux92x FPD-Link III 器件的 I2S 音频接口》* (SNLA221)
- *《AN-2198 探索 720p FPD-Link III 器件的内部测试图案生成特性》*(SNLA132)

11.2 商标

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11.3 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.4 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
DS90UH947TRGCRQ1	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UH947Q
DS90UH947TRGCRQ1.A	Active	Production	VQFN (RGC) | 64	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UH947Q
DS90UH947TRGCTQ1	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UH947Q
DS90UH947TRGCTQ1.A	Active	Production	VQFN (RGC) | 64	250 | SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 105	UH947Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

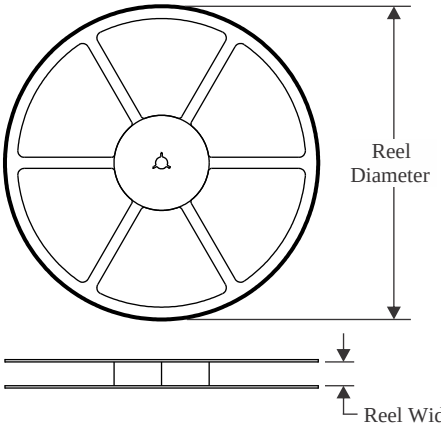
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

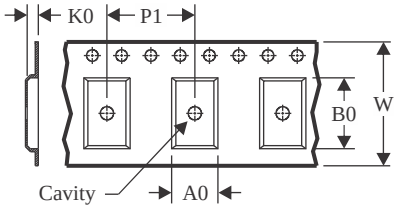
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

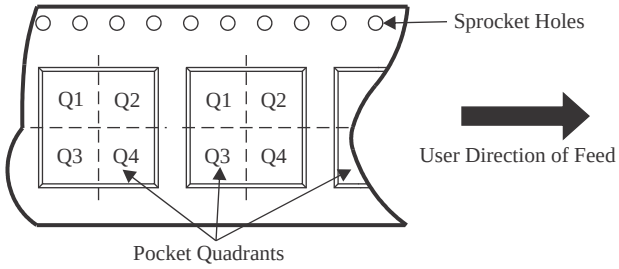


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

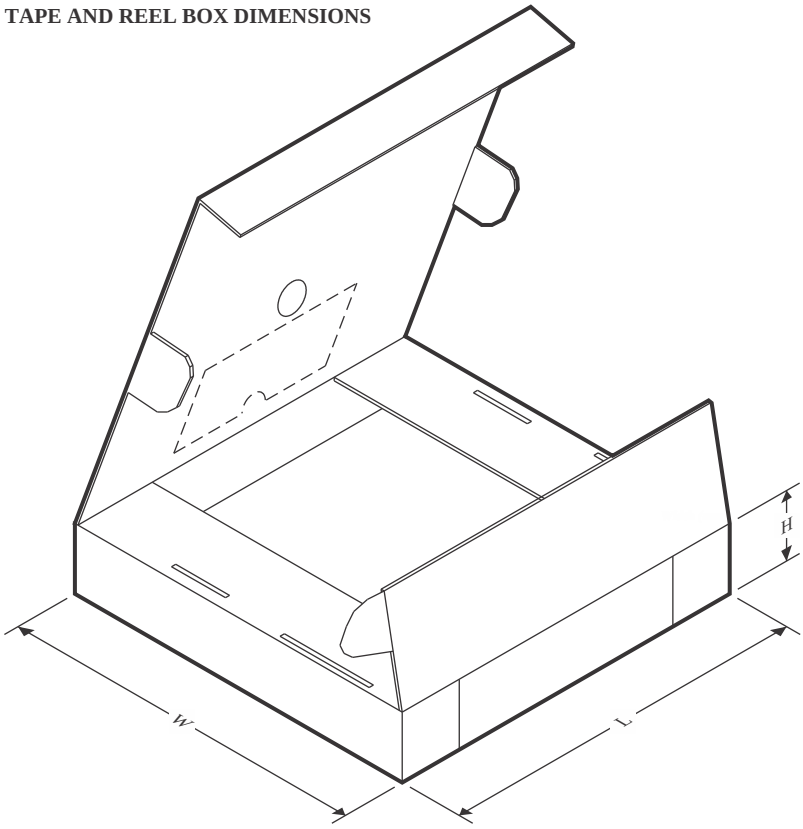
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DS90UH947TRGCRQ1	VQFN	RGC	64	2000	330.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1
DS90UH947TRGCTQ1	VQFN	RGC	64	250	178.0	16.4	9.3	9.3	1.3	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DS90UH947TRGCRQ1	VQFN	RGC	64	2000	356.0	356.0	36.0
DS90UH947TRGCTQ1	VQFN	RGC	64	250	208.0	191.0	35.0

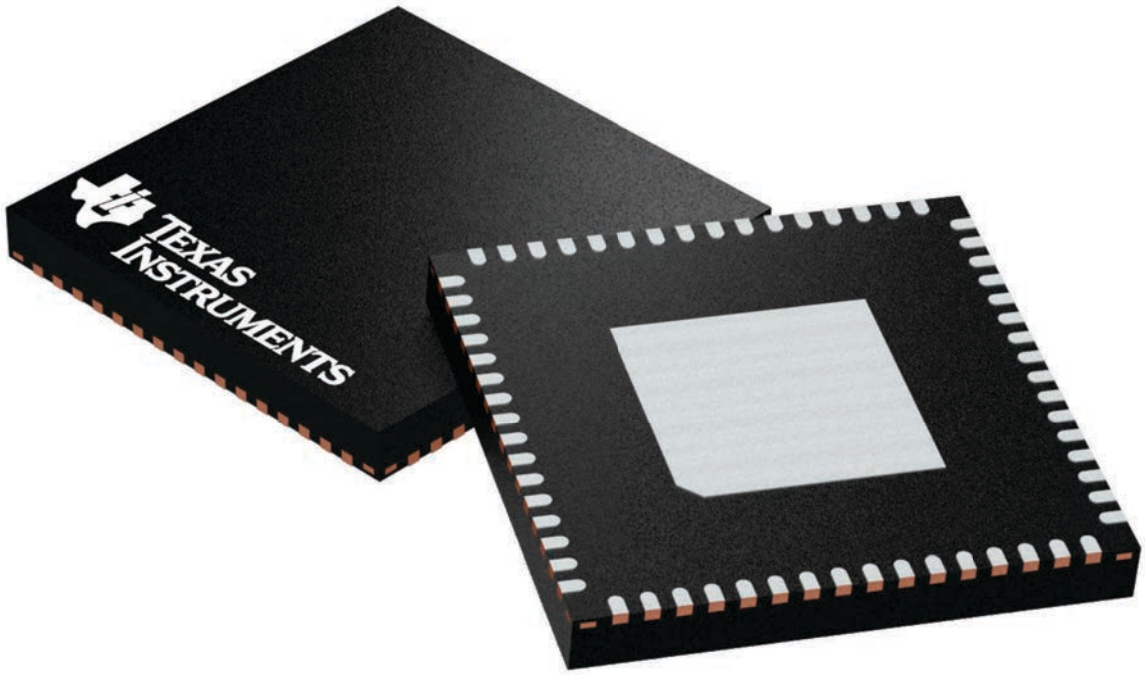
GENERIC PACKAGE VIEW

RGC 64

VQFN - 1 mm max height

9 x 9, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

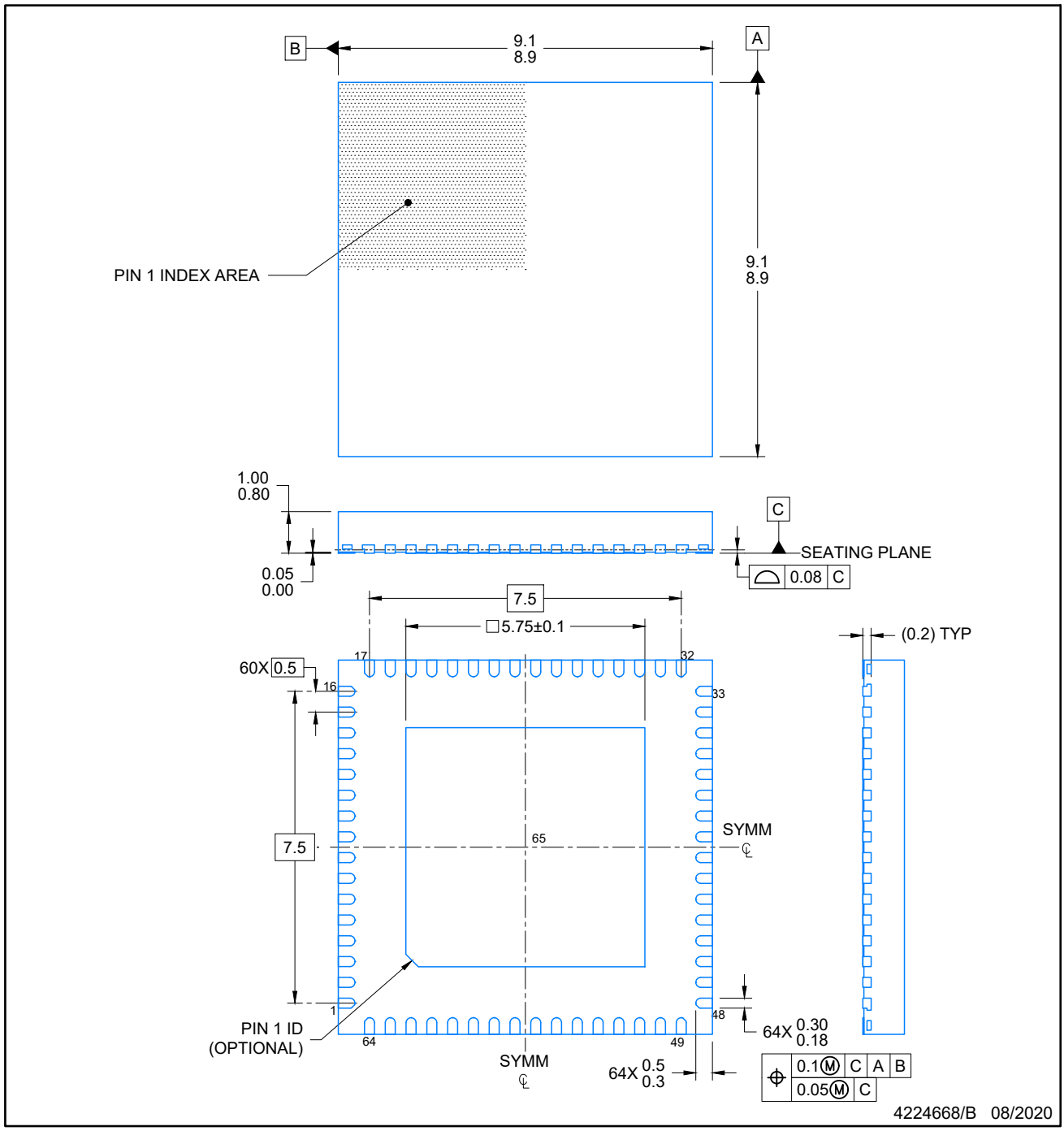
4224597/A

PACKAGE OUTLINE

RGC0064K

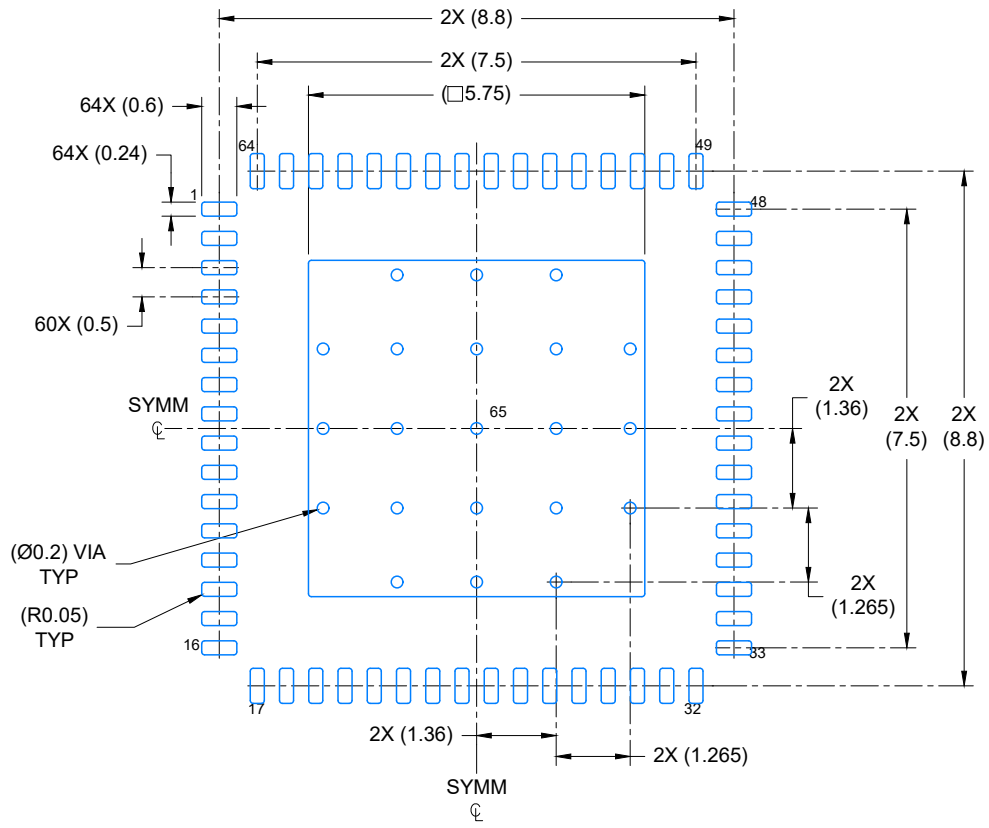
VQFN - 1 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

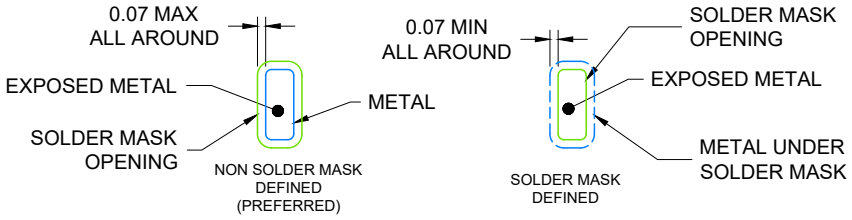


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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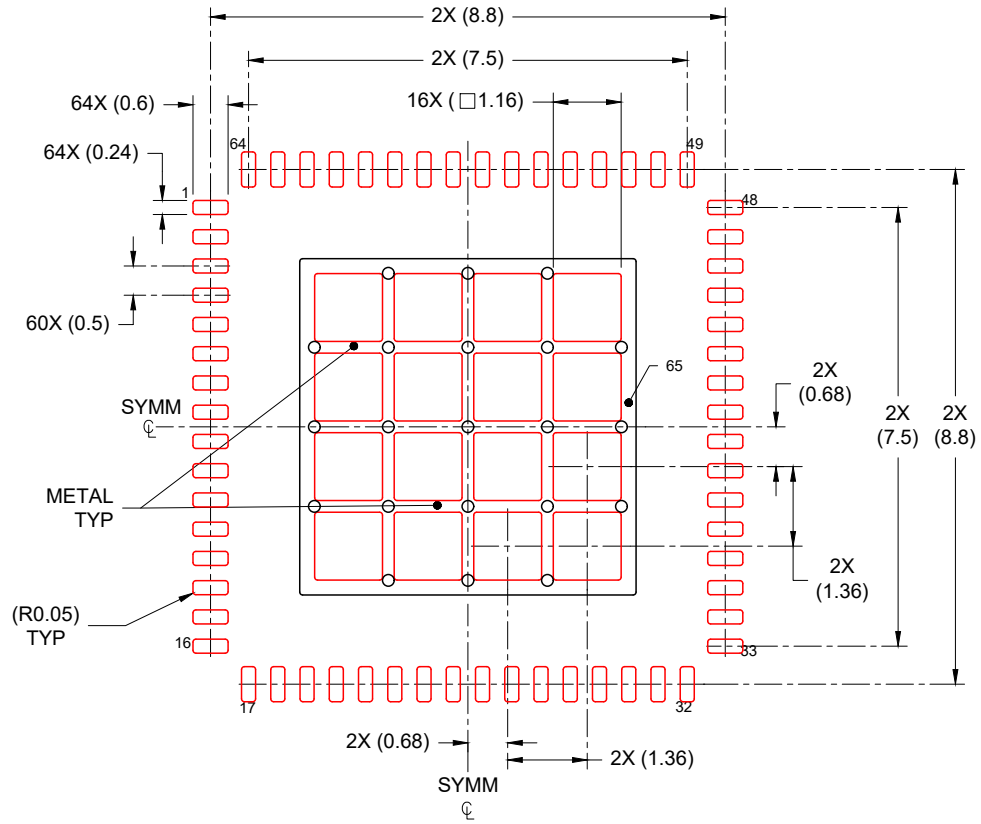
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
65% PRINTED COVERAGE BY AREA
SCALE: 8X

4224668/B 08/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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