TRF7970A 多协议全集成式 13.56MHz RFID 和近场通信 (NFC) 收发器 IC

1 器件概述

1.1 特性

- 支持近场通信 (NFC) 标准 NFCIP-1 (ISO/IEC 18092) 和 NFCIP-2 (ISO/IEC 21481)
- 完全集成了以下标准的协议处理：ISO/IEC 15693、ISO/IEC 18000-3、ISO/IEC 14443 A 和 B 以及 FeliCa™
- 集成式编码器、解码器和数据组帧功能，用于 NFC 发起方运行模式以及有源和无源目标方运行模式，适合所有三种比特率（106kbps、212kbps、424kbps）以及卡仿真
- 借助带有可编程唤醒电平的射频场检测器，实现 NFC 无源应答器仿真
- 通过射频场检测器避免 NFC 物理碰撞
- 通过集成的状态机实现 ISO/IEC 14443 A 防撞（破坏的字节）（应答器仿真或 NFC 无源目标）
- 输入电压范围：2.7VDC 至 5.5VDC
- 可编程输出功率：+20dBm (100mW)，+23dBm (200mW)
- 从 1.8VDC 至 5.5 VDC 的可编程 I/O 电压电平
- 来自 13.56MHz 或者 27.12MHz 晶振或者振荡器的可编程系统时钟频率输出 (RF，RF/2，RF/4)
- 针对其它系统组件（微控制器 (MCU)，外设，指示器）的集成电压稳压器输出，20mA（最大值）
- 可编程调制深度
- 具有针对“读取漏洞”消除和邻近读取器系统或者周围环境频带内噪声检测的具有接收信号强度指示器 (RSSI) 的双接收器架构
- 针对超低功耗系统设计的可编程功率模式（断电时 < 1μA）
- 并行或 SPI 接口（带有 127 字节 FIFO）
- 温度范围：-40°C 至 110°C
- 32 引脚 QFN 封装 (5mm × 5mm)

1.2 应用范围

- 移动器件（平板电脑、手机）
- 安全配对（ *Bluetooth*®， Wi-Fi®，其他配对无线网络）
- 公共运输或者赛事票务
- 护照或者付费 (POS) 读取器系统
- 近程无线通信任务（固件升级）
- 产品识别或者认证
- 医疗设备或者消耗品
- 访问控制、数字门锁
- 电子业务卡共享

1.3 说明

TRF7970A 器件是一款用于 13.56MHz NFC/RFID 系统的集成式模拟前端 (AFE) 和多协议数据组帧器件，支持所有的三种 NFC 工作模式：读/写器模式、对等模式和卡仿真模式，符合 ISO/IEC 14443 A 和 B、Sony FeliCa、ISO/IEC 15693、NFCIP-1 (ISO/IEC 18092) 和 NFCIP-2 (ISO/IEC 21481) 等标准。该器件具有内置的编程选项，因此适合于 NFC、接近和邻近识别系统的广泛 应用 。

通过在控制寄存器内选择所需的协议可对此器件进行配置。通过对所有控制寄存器进行直接存取，可根据需要对不同的读取器参数进行微调。

TRF7970A 器件针对所有符合板载 ISO 协议的组帧和同步任务，支持高达 848kbps 的数据速率。TRF7970A 器件还支持 NFC 论坛标签类型 1、2、3、4 和 5 的读写器模式。可通过使用该器件提供的直接模式之一来实现其他标准甚至自定义协议。这些直接模式可让用户完全控制 AFE，并且还可以访问原始子载波数据或者未组帧但已经是 ISO 格式的数据和相关（提取的）时钟信号。

接收器系统具有双输入接收器架构，可最大程度实现通信稳定。接收器还包括多种自动和手动增益控制选项。在 RSSI 寄存器中可获取从应答器、周围信号源或者内部电平接收到的信号强度。

可使用 SPI 或并行接口进行 MCU 和 TRF7970A 器件间的通信。当使用内置的硬件编码器和解码器时，发送和接收功能使用一个 127 字节的 FIFO 寄存器。对于直接发送或接收功能，由于编码器或解码器可被旁路绕开，所以 MCU 可实时地处理数据。

TRF7970A 器件支持 2.7V 至 5.5V 的宽电源电压范围以及 MCU I/O 接口的 1.8V 至 5.5V 数据通信电平。

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

当使用 5V 电源时，发送器对于 50Ω 负载具有 100mW (+20dBm) 或 200mW (+23dBm) 等效值的可选输出功率电平，并支持可选调制深度的 OOK 和 ASK 调制。

内置的可编程辅助稳压器为 MCU 和读取器系统内的其他外部电路提供高达 20mA 的电源。

通过具有可编程唤醒电平、八种可选电源模式以及超低功耗运行模式的集成射频场检测器，可以轻松开发可靠、经济高效且电池寿命长的设计。

要评估 TRF7970A 多协议收发器 IC，可使用TRF7970AEVM、TRF7970ATB 或 DLP-7970ABP。

器件信息

器件型号	封装	封装尺寸
TRF7970ARHB	VQFN (32)	5mm x 5mm

1.4 功能方框图

图 1-1 显示了方框图。

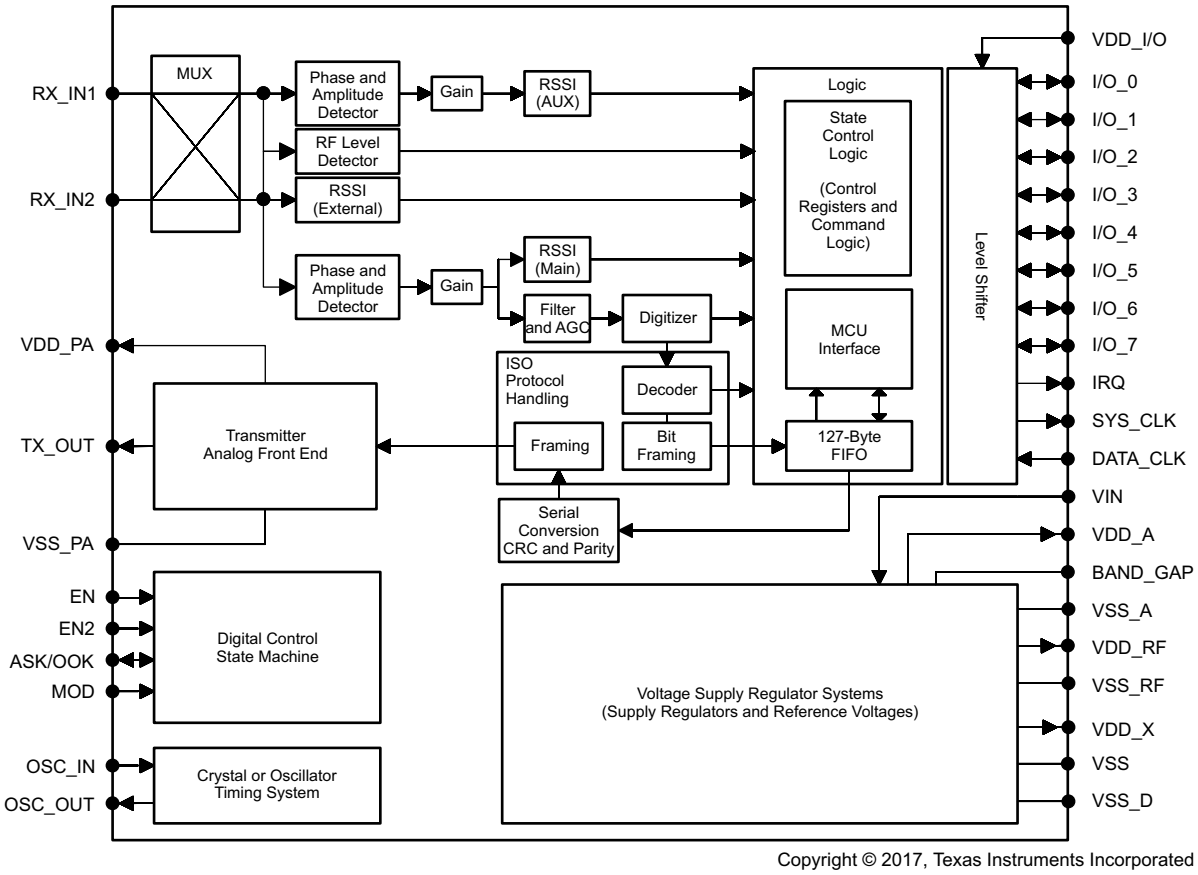

图 **1-1.** 方框图

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2 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from April 18, 2014 to March 27, 2017 **Page**

- 通篇更正了 ISO/IEC 标准代号；例如，将 ISO14443 更改为 ISO/IEC 14443 1
- 更改了以下部分的内容：节 1.3 - *说明* 1
- Added Section 3.1, *Related Products* 6
- Moved T_{STG} from Section 5.2 to Section 5.1, *Absolute Maximum Ratings* 9
- Moved Section 5.2 and changed title from *Handling Ratings* to *ESD Ratings* 9
- Added V_{OL} and V_{OH} to Section 5.4, *Electrical Characteristics* 10
- Changed the TYP value of the f_{D_CLKmax} parameter from 8 to 4 MHz in Section 5.4, *Electrical Characteristics* 10
- Throughout document, removed support for application control of Automatic Gain Control (AGC) and Receiver Gain Adjust, because these features were designed for test functionality and not for production use 12
- Added NFC Type 5 tags to supported list in Section 6.1.1, *RFID and NFC Operation – Reader and Writer* 12
- Removed the paragraph that started "The desired system of operation (bit rate) is achieved by..." from Section 6.1.2, *NFC Device Operation – Initiator* 13
- Removed the paragraph that started "The desired system of operation (bit rate) is achieved by..." from Section 6.1.3, *NFC Device Operation – Target* 13
- Throughout document, changed "tag" emulation or emulator to "card" emulation or emulator 13
- Added the sentence that starts "For interoperability purposes, TI recommends..." in the first bulleted list item in Section 6.1.3, *NFC Device Operation – Target* 14
- Changed POLLING to SENSF_REQ in the bulleted list item that starts "If the first command is a SENSF_REQ..." and deleted the sentence that started "The POLLING response is sent in..." in Section 6.1.3, *NFC Device Operation – Target* 14
- Updated the bulleted list item that starts "If the first command is ATR_REQ..." in Section 6.1.3, *NFC Device Operation – Target* 14
- Changed "coded as ISO14443" to "SENSB_REQ" in the bulleted list item that starts "If the first command is a SENSB_REQ..." in Section 6.1.3, *NFC Device Operation – Target* 14
- Changed "FeliCa" to "peer-to-peer" in Section 6.1.3.1, *Active Target*, and Section 6.1.3.2, *Passive Target* 14
- Updated the paragraph that starts "The transmission of a response must occur after RF collision avoidance..." in Section 6.1.3.1, *Active Target* 14
- Updated the paragraph that starts "The transmit system in passive target mode..." in Section 6.1.3.2, *Passive Target* 14
- Updated the description in Section 6.1.3.3, *Card Emulation* 15
- Added the sentence that starts "For applications in which the TRF7970A may be subjected..." in the second paragraph of 节 6.3, *Power Supplies* 15
- Changed V_{DD_A} to V_{DD_X} in the last sentence that reads "The V_{DD_X} output current should not exceed 20 mA." in the NOTE in *Analog Supply Regulator: V_{DD_A}* 16
- Removed the paragraph that started "The RF power amplifier regulator..." from *Digital Supply Regulator: V_{DD_X}* 16
- Changed 250 mV to 400 mV in "...a "Delta Voltage" of 400 mV below V_{IN}..." 16
- Added the paragraph that starts "As V_{DD_RF} is increased, the system..." in 节 6.3.2, *Supply Regulator Settings* 18
- Removed the paragraphs that started "The main receiver also has..." and "By default, the AGC window comparator..." from 节 6.4.2, *Receiver Gain and Filter Stages* 21
- Changed 表 6-5 to match 表 6-37 22
- Updated 节 6.5, *Receiver – Digital Section*, to clarify and remove duplicate content 22
- Updated the description in 节 6.5.1.2, *External RSSI* 26
- Removed "Equivalent Series Resistance" from 表 6-9, *Minimum Crystal Recommendations* 28
- Removed mention of 3-wire SPI and replaced "IRQ" with "Slave Select" in the first paragraph of 节 6.10.1, *General Introduction* 30
- Updated the description of FIFO level interrupts in 节 6.10.1.4, *FIFO Operation* 34
- Added "but recommended" to "It is optional but recommended to read the FIFO Status register..." in 节 6.10.3, *Reception of Air Interface Data* 36
- Changed the title of 节 6.10.4, *Data Transmission From MCU to TRF7970A* 37
- Removed the sentence that started "The choice of one of these modes over another..." from 节 6.10.5, *Serial Interface Communication (SPI)* 37
- Updated the paragraph that starts "TI recommends resetting the FIFO after receiving data..." in 节 6.10.5.1, *Serial Interface Mode With Slave Select (SS)* 42
- Added the NOTE that starts "An additional direct mode..." in 节 6.10.6, *Direct Mode* 43

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- Added 节 6.11, *TRF7970A Initialization* 48
- Changed the application report that is referenced in 节 6.12, *Special Direct Mode for Improved MIFARE™ Compatibility* 49
- Changed POLLING to SENSF_REQ and updated description in the list item that starts "If the first command is a SENSF_REQ..." 50
- Updated the description in the list item that starts "If the first command is ATR_REQ..." 50
- Corrected description of B1 Irq_col in 表 6-18, *IRQ Status Register (0x0C) for NFC and Card Emulation Operation*: changed from "(as defined in register 0x01)" to "(as defined in register 0x10)" 51
- Removed mention of collision avoidance commands from 节 6.13.2, *Initiator* 51
- Added and updated comments in 表 6-19, *Address and Command Word Bit Distribution* 51
- Removed command code 0x15, Close Slot Sequence, from 表 6-19, *Address and Command Word Bit Distribution* 51
- Added the sentence that starts "This command should be sent after a Software Initialization command..." in 节 6.14.1.1, *Idle (0x00)* 52
- Changed the description in 节 6.14.1.3, *Initial RF Collision Avoidance (0x04)* 53
- Changed the description in 节 6.14.1.4, *Response RF Collision Avoidance (0x05)* 53
- Changed the description in 节 6.14.1.5, *Response RF Collision Avoidance (0x06, n = 0)* 53
- Added "This is used by the ISO/IEC 15693 protocol" to 节 6.14.1.11, *Transmit Next Time Slot (0x14)* 54
- Corrected description of B1 Irq_col in 表 6-43, *IRQ Status Register (0x0C)*: changed from "(as defined in register 0x01)" to "(as defined in register 0x10)" 66
- Changed the description of B5:B3 in 表 6-47 from "...Auxiliary RSSI represents the signal level at RX_IN2" to "...Auxiliary RSSI represents the signal level at RX_IN1" 68
- Removed former Section 7.1, *TRF7970A Reader System Using Parallel Microcontroller Interface* 75
- Changed 图 7-1, *Application Schematic – SPI With SS Mode MCU Interface* 75
- Updated the description in 节 7.1.2, *Schematic* 75
- 添加了节 8.1“*入门和后续步骤*” 78
- 添加了节 8.2“*器件命名规则*” 78
- 添加了节 8.3“*工具和软件*” 79
- 更新了节 8.4“*文档支持*” 79

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3 Device Characteristics

Table 3-1 lists the supported modes of operation for the TRF7970A device.

Table 3-1. Supported Modes of Operation

P2P INITIATOR OR READER/WRITER		CARD EMULATION		P2P TARGET	
TECHNOLOGY	BIT RATE (kbps)	TECHNOLOGY	BIT RATE (kbps)	TECHNOLOGY	BIT RATE (kbps)
NFC-A and NFC-B (ISO/IEC 14443 A and B)	106, 212, 424, 848 (1)	NFC-A, NFC-B	106	NFC-A	106
NFC-F (JIS: X6319-4)	212, 424	N/A	N/A	NFC-F	212, 424
NFC-V (ISO/IEC 15693)	6.7, 26.7	N/A	N/A	N/A	N/A

(1) 848 kbps applies to reader/writer mode only.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for TI Wireless Connectivity Connect more with the industry's broadest wireless connectivity portfolio.

Products for NFC / RFID TI provides one of the industry's most differentiated NFC and RFID product portfolios and is your solution to meet a broad range of NFC connectivity and RFID identification needs.

Companion Products for TRF7970A Review products that are frequently purchased or used with this product.

Reference Designs for TRF7970A The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market. Search and download designs at ti.com/tidesigns.

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4 Terminal Configuration and Functions

4.1 Pin Diagram

Figure 4-1 shows the pinout for the 32-pin RHB package.

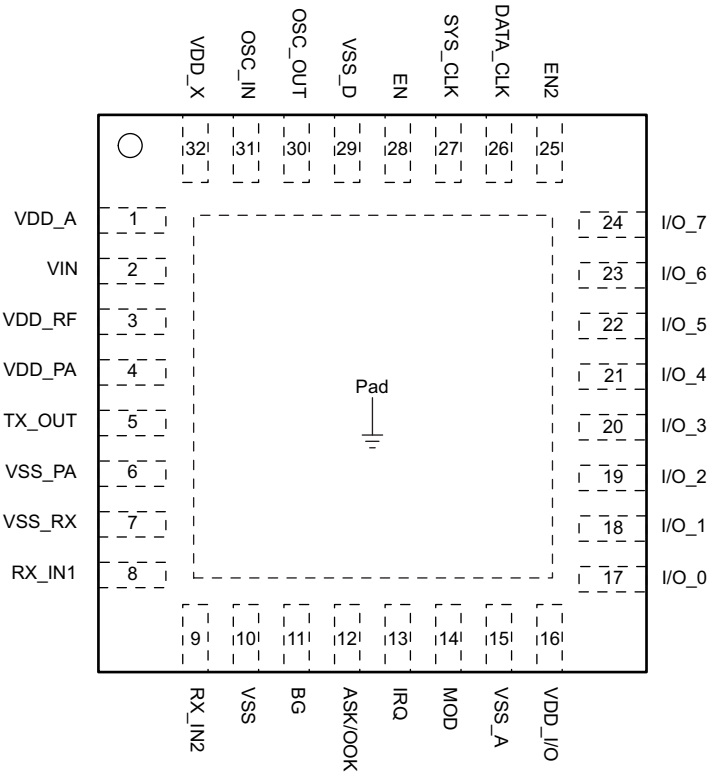

Figure 4-1. 32-Pin RHB Package (Top View)

4.2 Signal Descriptions

Table 4-1 describes the signals.

Table 4-1. Terminal Functions

TERMINAL		TYPE (1)	DESCRIPTION
NAME	NO.		
V_{DD_A}	1	OUT	Internal regulated supply (2.7 V to 3.4 V) for analog circuitry
V_{IN}	2	SUP	External supply input to chip (2.7 V to 5.5 V)
V_{DD_RF}	3	OUT	Internal regulated supply (2.7 V to 5 V), normally connected to V_{DD_PA} (pin 4)
V_{DD_PA}	4	INP	Supply for PA; normally connected externally to V_{DD_RF} (pin 3)
TX_OUT	5	OUT	RF output (selectable output power, 100 mW or 200 mW, with V_{DD} = 5 V)
V_{SS_PA}	6	SUP	Negative supply for PA; normally connected to circuit ground
V_{SS_RX}	7	SUP	Negative supply for RX inputs; normally connected to circuit ground
RX_IN1	8	INP	Main RX input
RX_IN2	9	INP	Auxiliary RX input
V_{SS}	10	SUP	Chip substrate ground
BAND_GAP	11	OUT	Bandgap voltage (V_{BG} = 1.6 V); internal analog voltage reference
ASK/OOK	12	BID	Selection between ASK and OOK modulation (0 = ASK, 1 = OOK) for direct mode 0 or 1. Can be configured as an output to provide the received analog signal output.

(1) SUP = Supply, INP = Input, BID = Bidirectional, OUT = Output

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Table 4-1. Terminal Functions (continued)

TERMINAL		TYPE (1)	DESCRIPTION
NAME	NO.		
IRQ	13	OUT	Interrupt request
MOD	14	INP	External data modulation input for direct mode 0 or 1
		OUT	Subcarrier digital data output (see registers 0x1A and 0x1B)
V_{SS_A}	15	SUP	Negative supply for internal analog circuits; connected to GND
$V_{DD_I/O}$	16	INP	Supply for I/O communications (1.8 V to V_{IN}) level shifter. V_{IN} should be never exceeded.
I/O_0	17	BID	I/O pin for parallel communication
I/O_1	18	BID	I/O pin for parallel communication
I/O_2	19	BID	I/O pin for parallel communication TX enable (in special direct mode)
I/O_3	20	BID	I/O pin for parallel communication TX data (in special direct mode)
I/O_4	21	BID	I/O pin for parallel communication Slave select signal in SPI mode
I/O_5	22	BID	I/O pin for parallel communication Data clock output in direct mode 1 and special direct mode
I/O_6	23	BID	I/O pin for parallel communication MISO for serial communication (SPI) Serial bit data output in direct mode 1 or subcarrier signal in direct mode 0
I/O_7	24	BID	I/O pin for parallel communication. MOSI for serial communication (SPI)
EN2	25	INP	Selection of power down mode. If EN2 is connected to V_{IN}, then V_{DD_X} is active during power down mode 2 (for example, to supply the MCU).
DATA_CLK	26	INP	Data clock input for MCU communication (parallel and serial)
SYS_CLK	27	OUT	If EN = 1 (EN2 = don't care) the system clock for MCU is configured. Depending on the crystal that is used, options are as follows (see register 0x09): 13.56-MHz crystal: Off, 3.39 MHz, 6.78 MHz, or 13.56 MHz 27.12-MHz crystal: Off, 6.78 MHz, 13.56 MHz, or 27.12 MHz If EN = 0 and EN2 = 1, then system clock is set to 60 kHz
EN	28	INP	Chip enable input (If EN = 0, then chip is in sleep or power-down mode).
V_{SS_D}	29	SUP	Negative supply for internal digital circuits
OSC_OUT	30	OUT	Crystal or oscillator output
OSC_IN	31	INP	Crystal or oscillator input
		OUT	Crystal oscillator output
V_{DD_X}	32	OUT	Internally regulated supply (2.7 V to 3.4 V) for digital circuit and external devices (for example, an MCU)
Thermal Pad	PAD	SUP	Chip substrate ground

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5 Specifications

5.1 Absolute Maximum Ratings(1) (2)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{IN}	Input voltage range		–0.3	6	V
I_{IN}	Maximum current V_{IN}			150	mA
T_J	Maximum operating virtual junction temperature	Any condition		140	°C
		Continuous operation, long-term reliability(3)		125	°C
T_{STG}	Storage temperature		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* are not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to substrate ground terminal V_{SS}.
(3) The maximum junction temperature for continuous operation is limited by package constraints. Operation above this temperature may result in reduced reliability or lifetime of the device.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V
		Machine model (MM)	±200	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±500 V may actually have higher performance.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
V_{IN}	Operating input voltage		2.7	5	5.5	V
T_A	Operating ambient temperature		–40	25	110	°C
T_J	Operating virtual junction temperature		–40	25	125	°C
V_{IL}	Input voltage, logic low	I/O lines, IRQ, SYS_CLK, DATA_CLK, EN, EN2, ASK/OOK, MOD			0.2 × $V_{DD_I/O}$	V
V_{IH}	Input voltage threshold, logic high	I/O lines, IRQ, SYS_CLK, DATA_CLK, EN, EN2, ASK/OOK, MOD	0.8 × $V_{DD_I/O}$			V

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5.4 Electrical Characteristics

TYP operating conditions are T_A = 25°C, VIN = 5 V, full-power mode (unless otherwise noted)
MIN and MAX operating conditions are over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL}	Low-level output voltage			0.2 × $V_{DD_I/O}$		V
V_{OH}	High-level output voltage			0.8 × $V_{DD_I/O}$		V
I_{PD1}	Supply current in power down mode 1	All building blocks disabled, including supply-voltage regulators; measured after 500-ms settling time (EN = 0, EN2 = 0)		0.5	5	µA
I_{PD2}	Supply current in power down mode 2 (sleep mode)	The SYS_CLK generator and V_{DD_X} remain active to support external circuitry; measured after 100-ms settling time (EN = 0, EN2 = 1)		120	200	µA
I_{STBY}	Supply current in stand-by mode	Oscillator running, supply-voltage regulators in low-consumption mode (EN = 1, EN2 = x)		1.9	3.5	mA
I_{ON1}	Supply current without antenna driver current	Oscillator, regulators, RX and AGC active, TX is off		10.5	14	mA
I_{ON2}	Supply current, TX (half power)	Oscillator, regulators, RX and AGC and TX active, P_{OUT} = 100 mW		70	78	mA
I_{ON3}	Supply current, TX (full power)	Oscillator, regulators, RX and AGC and TX active, P_{OUT} = 200 mW		130	150	mA
V_{POR}	Power-on-reset voltage	Input voltage at V_{IN}	1.4	2	2.6	V
V_{BG}	Bandgap voltage (pin 11)	Internal analog reference voltage	1.5	1.6	1.7	V
V_{DD_A}	Regulated output voltage for analog circuitry (pin 1)	V_{IN} = 5 V	3.1	3.4	3.8	V
V_{DD_X}	Regulated supply for external circuitry	Output voltage pin 32, V_{IN} = 5 V	3.1	3.4	3.8	V
I_{VDD_Xmax}	Maximum output current of V_{DD_X}	Output current pin 32, V_{IN} = 5 V			20	mA
R_{RFOUT}	Antenna driver output resistance (1)	Half-power mode, V_{IN} = 2.7 V to 5.5 V		8	12	Ω
		Full-power mode, V_{IN} = 2.7 V to 5.5 V		4	6	
R_{RFIN}	RX_IN1 and RX_IN2 input resistance		4	10	20	kΩ
V_{RF_INmax}	Maximum RF input voltage at RX_IN1 and RX_IN2	V_{RF_INmax} should not exceed V_{IN}		3.5		V_{pp}
V_{RF_INmin}	Minimum RF input voltage at RX_IN1 and RX_IN2 (input sensitivity) (2)	$f_{SUBCARRIER}$ = 424 kHz		1.4	2.5	mV_{pp}
		$f_{SUBCARRIER}$ = 848 kHz		2.1	3	
f_{SYS_CLK}	SYS_CLK frequency	In power mode 2, EN = 0, EN2 = 1	25	60	120	kHz
f_C	Carrier frequency	Defined by external crystal		13.56		MHz
$t_{CRYSTAL}$	Crystal run-in time	Time until oscillator stable bit is set (register 0x0F) (3)		3		ms
f_{D_CLKmax}	Maximum DATA_CLK frequency (4)	Depends on capacitive load on the I/O lines, TI recommends 2 MHz (4)	2	4	10	MHz
R_{OUT}	Output resistance I/O_0 to I/O_7			500	800	Ω
R_{SYS_CLK}	Output resistance R_{SYS_CLK}			200	400	Ω

(1) Antenna driver output resistance
(2) Measured with subcarrier signal at RX_IN1 or RX_IN2 and measured the digital output at MOD pin with register 0x1A bit 6 = 1.
(3) Depends on the crystal parameters and components
(4) TI recommends a DATA_CLK speed of 2 MHz. Higher data clock depends on the capacitive load. Maximum SPI clock speed should not exceed 10 MHz. This clock speed is acceptable only when external capacitive load is less than 30 pF. MISO driver has a typical output resistance of 400 Ω (12-ns time constant when 30-pF load used).

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5.5 Thermal Resistance Characteristics

PACKAGE	θ_{JC}	θ_{JA} (1)	POWER RATING (2)	
			$T_A \le 25°C$	$T_A \le 85°C$
RHB (32 pin)	31°C/W	36.4°C/W	2.7 W	1.1 W

(1) This data was taken using the JEDEC standard high-K test PCB.
(2) Power rating is determined with a junction temperature of 125°C. This is the temperature at which distortion starts to increase substantially. Thermal management of the final PCB should strive to keep the junction temperature at or below 125°C for best performance and long-term reliability.

5.6 Switching Characteristics

TYP operating conditions are T_A = 25°C, VIN = 5 V, full-power mode (unless otherwise noted)
MIN and MAX operating conditions are over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{LO/HI}$	DATA_CLK time high or low, one half of DATA_CLK at 50% duty cycle	Depends on capacitive load on the I/O lines (1)	250	62.5	50	ns
$t_{STE,LEAD}$	Slave select lead time, slave select low to clock			200		ns
$t_{STE,LAG}$	Slave select lag time, last clock to slave select high			200		ns
$t_{STE,DIS}$	Slave select disable time, slave select rising edge to next slave select falling edge		300			ns
$t_{SU,SI}$	MOSI input data setup time		15			ns
$t_{HD,SI}$	MOSI input data hold time		15			ns
$t_{SU,SO}$	MISO input data setup time		15			ns
$t_{HD,SO}$	MISO input data hold time		15			ns
$t_{VALID,SO}$	MISO output data valid time	DATA_CLK edge to MISO valid, $C_L \le 30$ pF	30	50	75	ns

(1) TI recommends a DATA_CLK speed of 2 MHz. Higher data clock depends on the capacitive load. Maximum SPI clock speed should not exceed 10 MHz. This clock speed is acceptable only when external capacitive load is less than 30 pF. MISO driver has a typical output resistance of 400 Ω (12-ns time constant when 30-pF load used).

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6 Detailed Description

6.1 Overview

6.1.1 RFID and NFC Operation – Reader and Writer

The TRF7970A is a high-performance 13.56-MHz HF RFID and NFC transceiver IC composed of an integrated analog front end (AFE) and a built-in data framing engine for ISO/IEC 15693, ISO/IEC 14443 A and B, and FeliCa. This includes data rates up to 848 kbps for ISO/IEC 14443 with all framing and synchronization tasks on board (in default mode). The TRF7970A also supports NFC tag type 1, 2, 3, 4, and 5 operations. This architecture lets the customer build a complete cost-effective yet high-performance multiprotocol 13.56-MHz RFID and NFC system together with a low-cost microcontroller.

Other standards and even custom protocols can be implemented by using either of the direct modes that the device offers. These direct modes (0 and 1) allow the user to fully control the analog front end (AFE) and also gain access to the raw subcarrier data or the unframed but already ISO formatted data and the associated (extracted) clock signal.

The receiver system has a dual input receiver architecture. The receivers also include various automatic and manual gain control options. The received input bandwidth can be selected to cover a broad range of input subcarrier signal options.

The received signal strength from transponders, ambient sources, or internal levels is available through the RSSI register. The receiver output is selectable among a digitized subcarrier signal and any of the integrated subcarrier decoders. The selected subcarrier decoder delivers the data bit stream and the data clock as outputs.

The TRF7970A also includes a receiver framing engine. This receiver framing engine performs the CRC or parity check, removes the EOF and SOF settings, and organizes the data in bytes for ISO/IEC 14443 A and B, ISO/IEC 15693, and FeliCa protocols. Framed data is then accessible to the microcontroller (MCU) through a 127-byte FIFO register.

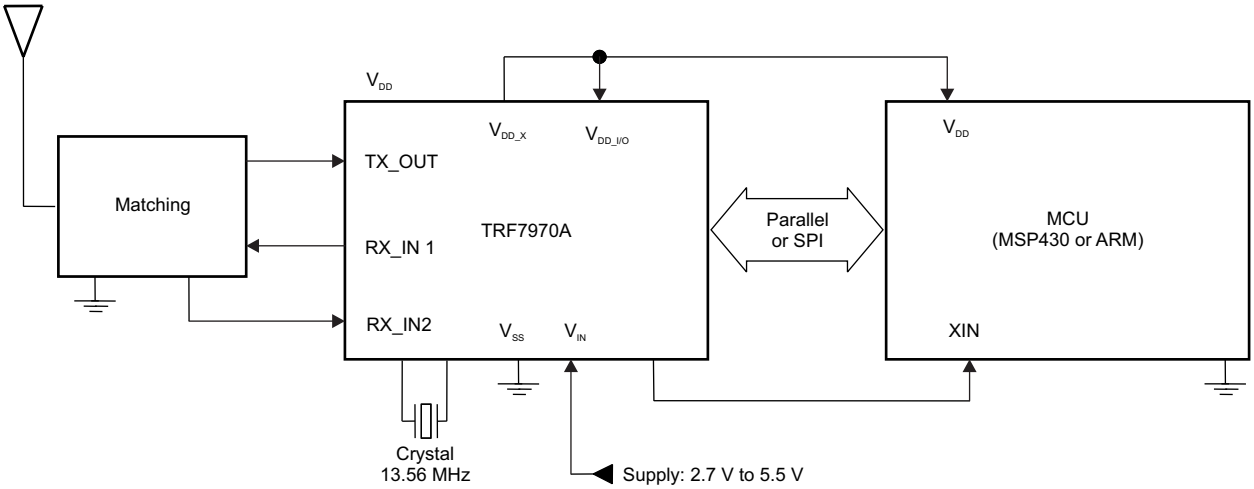

Figure 6-1. Application Block Diagram

A parallel or serial interface (SPI) can be used for the communication between the MCU and the TRF7970A reader. When the built-in hardware encoders and decoders are used, transmit and receive functions use a 127-byte FIFO register. For direct transmit or receive functions, the encoders and decoders can be bypassed so that the MCU can process the data in real time. The TRF7970A supports data communication voltage levels from 1.8 V to 5.5 V for the MCU I/O interface. The transmitter has selectable output-power levels of 100 mW (+20 dBm) or 200 mW (+23 dBm) equivalent into a 50-Ω load when using a 5-V supply.

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The transmitter supports OOK and ASK modulation with selectable modulation depth. The TRF7970A also includes a data transmission engine that comprises low-level encoding for ISO/IEC 15693, ISO/IEC 14443 A and B, and FeliCa. Included with the transmit data coding is the automatic generation of Start Of Frame (SOF), End Of Frame (EOF), Cyclic Redundancy Check (CRC), and parity bits.

Several integrated voltage regulators ensure a proper power-supply noise rejection for the complete reader system. The built-in programmable auxiliary voltage regulator V_{DD_X} (pin 32), is able to deliver up to 20 mA to supply a microcontroller and additional external circuits within the reader system.

6.1.2 NFC Device Operation – Initiator

The transmitting system includes an RF level detector (programmable level) which is used for initial (or response) RF collision avoidance. The RF collision avoidance sequence is started by sending a direct command. If successful, the NFC initiator can send the data or commands, the MCU has loaded in the FIFO register. The coding of this data is done by hardware coders in ISO/IEC 14443 A and B, or FeliCa format. The coders also provide CRC and parity bits (if required) and automatically add preambles, SOF, EOF, and synchronization bytes as defined by selected protocol.

The receiver system offers the same analog features (AGC, AM or PM, bandwidth selection, and so on) as described previously in RFID and NFC reader and writer description. The system comprises integrated decoders for passive targets (ISO/IEC 14443 A or ISO/IEC 14443 B tag or FeliCa) or active targets (ISO/IEC 14443 A or ISO/IEC 14443 B reader or FeliCa). For all this options, the system also supports framing including CRC and parity check and removal of SOF, EOF, and synchronization bytes as specified by the selected protocol.

6.1.3 NFC Device Operation – Target

The activation of NFC target is done when a sufficient RF field level is detected on the antenna. The level needed for wake-up is selectable and is stored in a nonvolatile register.

When the activation occurs, the system performs automatic power-up and waits for the first command to be received. Based on this command, the system knows if it should operate as passive or active target and at what bit rate. After activation, the receiver system offers the same analog features (for example, AGC, AM/PM, and bandwidth selection) as in the case of an RFID reader.

When used as the NFC target, the chip is typically in a power down or standby mode. If EN2 = H, the chip keeps the supply system on. If EN2 = L and EN = L, the chip is in complete power down. To operate as NFC target or card emulator, the MCU must load a value different from zero (0) in the Target Detection Level register (B0-B2) to enable the RF measurement system (supplied by VEXT, so it can also operate during complete power down and consume only 3.5 µA). The RF measurement constantly monitors the RF signal on the antenna input. When the RF level on the antenna input exceeds the level defined in the in Target Detection Level register, the chip is automatically activated (EN is internally forced high).

When the voltage supply system and the oscillator are started and are stable, osc_ok goes high (B6 of RSSI Level and Oscillator Status register) and IRQ is sent with bit B2 = 1 of IRQ register (field change). Bit B7 NFC Target Protocol in register directly displays the status of RF level detection (running constantly also during normal operation). This informs the MCU that the chip should start operation as NFC TARGET device. When the first command from the INITIATOR is received, another IRQ sent with B6 (RX start) set in the IRQ register. The MCU must set EN = H (confirm the power up) in the time between the two IRQs, because the internal power-up ends after the second IRQ. The type and coding of the first initiator (or reader in the case of a card emulator) command defines the communication protocol type that the target must use. Therefore, the communication protocol type is available in the NFC Target Protocol register immediately after receiving the first command.

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Based on the first command from the INITIATOR, the following actions are taken:

- If the first command is SENS_REQ or ALL_REQ, the TARGET must enter the SDD protocol for 106-kbps passive communication to begin; afterward, the baud rate can be changed to 212 kbps or 424 kbps, which is determined by the NFC initiator device. If bit B5 in the NFC Target Detection Level register is not set, the MCU handles the SDD and the command received is send to FIFO. For interoperability purposes, TI recommends allowing the MCU to handle the SDD process rather than use the TRF7970A Auto-SDD feature to ensure interoperability with other NFC devices. If the RF field is turned off (B7 in NFC Target Protocol register is low) at any time, the system sends an IRQ to the MCU with bit B2 (RF field change) in the IRQ register set high. This informs the MCU that the procedure was aborted and the system must be reset. The clock extractor is automatically activated in this mode.
- If the command is SENS_REQ or ALL_REQ and the card emulation bit in ISO Control register is set, the system emulates an ISO/IEC 14443 A or ISO/IEC 14443 B tag. The procedure does not differ from the one previously described for the case of a passive target at 106 kbps. The clock extractor is automatically activated in this mode.
- If the first command is a SENSF_REQ, the system becomes the TARGET in passive communication using 212 kbps or 424 kbps. The SDD is relatively simple and is handled by the MCU directly.
- If the first command is ATR_REQ, the system operates as an active TARGET using the same communication speed and bit coding as used by the INITIATOR. Again, all of the replies are handled by the MCU. The MCU should handle the timing requirements for collision avoidance. This is done by using external RSSI to detect external RF fields before enabling RF on the TRF7970A.
- If the first command is a SENSB_REQ request and the card emulation bit is set in the ISO Control register, the system enters ISO/IEC 14443 B emulation mode. The anticollision must be handled by the MCU, and the chip provides all physical level coding, decoding, and framing for this protocol.

6.1.3.1 Active Target

If the first command received by the RF interface defines the system as an active target, then the receiver selects the appropriate data decoders (ISO/IEC 14443 A or ISO/IEC 14443 B reader or peer-to-peer) and framing option. Only the raw (decoded) data is forwarded to the MCU through the FIFO. SOF, EOF, preamble, sync bytes, CRC, and parity bytes are checked by the framer and discarded.

The transmission of a response must occur after RF collision avoidance has been processed. The recommended method for RF collision avoidance is to use external RSSI to detect any external RF field. If successful, the NFC initiator can send the data that the MCU has loaded in the FIFO register. The coding of this data is done by hardware coders either in ISO/IEC 14443 A format (106-kbps system) or in peer-to-peer format for (212-kbps and 424-kbps systems). The coders also provide CRC and parity bits (if required) and automatically add preambles, SOF, EOF, and synchronization bytes as defined by selected protocol.

6.1.3.2 Passive Target

If the first command received by the RF interface defines the system as a passive target, then the receiver selects the appropriate data decoders (ISO/IEC 14443 A or ISO/IEC 14443 B reader or peer-to-peer) and framing option. Again, only the raw (decoded) data is forwarded to the MCU through the FIFO; SOF, EOF, preamble, sync bytes, CRC, and parity bytes are checked by the framer and discarded. The receiver works same as in the case of an active target.

The transmit system in passive target mode differs from active target and operates similar to the standard tag. There is no RF collision avoidance sequence, and encoders are used to code the data for ISO/IEC 14443 A or ISO/IEC 14443 B tag (at 106 kbps, to start) or peer-to-peer (at 212 kbps, to start) format. The coding system adds all of the SOF, EOF, CRC, parity bits, and synchronization bytes that are required by protocol. The response is transmitted over-the-air with a method known as load modulation.

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6.1.3.3 Card Emulation

The chip can enter this mode by setting appropriate option bits. The chip can emulate ISO/IEC 14443 A and B card types. For ISO/IEC 14443 A and B, the emulation supports 106-kbps data rate to start. For ISO/IEC 14443 A, the anticollision algorithm can be performed using an internal state machine, which relieves the MCU of any real-time tasks; however, this method can present interoperability challenges with other NFC devices due to timing requirements. To ensure best interoperability, TI recommends allowing the MCU to manage the anticollision process, instead. The unique ID required for anticollision is provided by the MCU after wakeup of the system.

6.2 System Block Diagram

图 6-2 shows a block diagram of the TRF7970A.

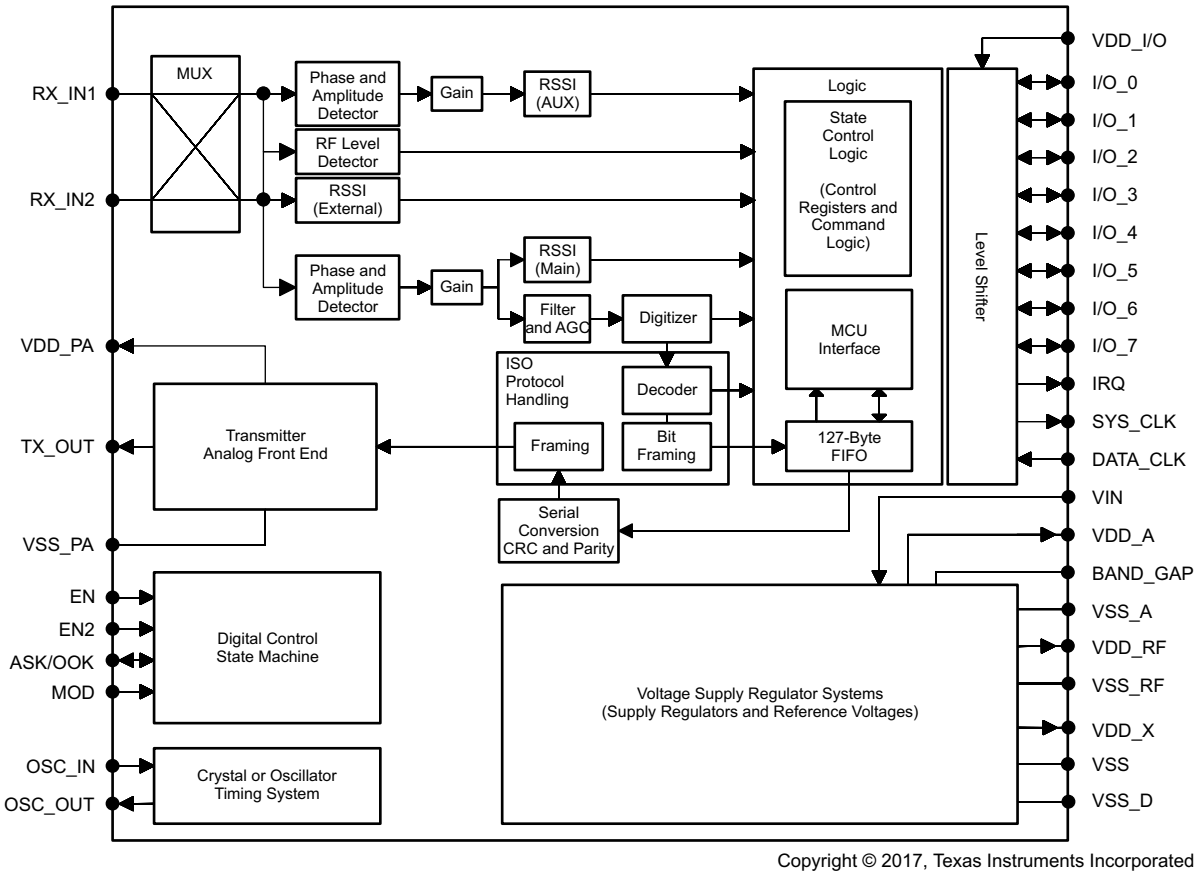

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图 6-2. System Block Diagram

6.3 Power Supplies

The TRF7970A positive supply input V_{IN} (pin 2) sources three internal regulators with output voltages V_{DD_RF}, V_{DD_A} and V_{DD_X}. All regulators use external bypass capacitors for supply noise filtering and must be connected as indicated in reference schematics. These regulators provide a high power supply reject ratio (PSRR) as required for RFID reader systems. All regulators are supplied by V_{IN} (pin 2).

The regulators are not independent and have common control bits in register 0x0B for output voltage setting. The regulators can be configured to operate in either automatic or manual mode (register 0x0B, bit 7). The automatic regulator setting mode ensures an optimal compromise between PSRR and the highest possible supply voltage for RF output (to ensure maximum RF power output). The manual mode allows the user to manually configure the regulator settings. For applications in which the TRF7970A may be subjected to external noise, manually reducing the regulator settings can improve RF performance.

6.3.1 Supply Arrangements

Regulator Supply Input: V_{IN}

The positive supply at V_{IN} (pin 2) has an input voltage range of 2.7 V to 5.5 V. V_{IN} provides the supply input sources for three internal regulators with the output voltages V_{DD_RF}, V_{DD_A}, and V_{DD_X}. External bypass capacitors for supply noise filtering must be used (per reference schematics).

注

V_{IN} must be the highest voltage supplied to the TRF7970A.

RF Power Amplifier Regulator: V_{DD_RF}

The V_{DD_RF} (pin 3) regulator is supplying the RF power amplifier. The voltage regulator can be set for either 5-V or 3-V operation. External bypass capacitors for supply noise filtering must be used (per reference schematics). When configured for 5-V manual-operation, the V_{DD_RF} output voltage can be set from 4.3 V to 5 V in 100-mV steps. In 3-V manual-operation, the output can be programmed from 2.7 V to 3.4 V in 100-mV steps. The maximum output current capability for 5-V operation is 150 mA and for 3-V operation is 100 mA.

Analog Supply Regulator: V_{DD_A}

Regulator V_{DD_A} (pin 1) supplies the analog circuits of the device. The output voltage setting depends on the input voltage and can be set for 5-V and 3-V operation. When configured for 5-V manual-operation, the output voltage is fixed at 3.4 V. External bypass capacitors for supply noise filtering must be used (per reference schematics). When configured for 3-V manual-operation, the V_{DD_A} output can be set from 2.7 V to 3.4 V in 100-mV steps (see 表 6-2).

注

The configuration of V_{DD_A} and V_{DD_X} regulators are not independent from each other. The V_{DD_X} output current should not exceed 20 mA.

Digital Supply Regulator: V_{DD_X}

The digital supply regulator V_{DD_X} (pin 32) provides the power for the internal digital building blocks and can also be used to supply external electronics within the reader system. When configured for 3-V operation, the output voltage can be set from 2.7 to 3.4 V in 100-mV steps. External bypass capacitors for supply noise filtering must be used (per reference schematics).

注

The configuration of the V_{DD_A} and V_{DD_X} regulators are not independent from each other. The V_{DD_X} output current should not exceed 20 mA.

By default, the regulators are set in automatic regulator setting mode. In this mode, the regulators are automatically set every time the system is activated by setting EN input High or each time the automatic regulator setting bit, B7 in register 0x0B is set to a 1. The action is started on the 0 to 1 transition. This means that, if the user wants to rerun the automatic setting from a state in which the automatic setting bit is already high, the automatic setting bit (B7 in register 0x0B) should be changed: 1-0-1.

By default, the regulator setting algorithm sets the regulator outputs to a "Delta Voltage" of 400 mV below V_{IN}, but not higher than 5 V for V_{DD_RF} and 3.4 V for V_{DD_A} and V_{DD_A}.

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Power Amplifier Supply: V_{DD_PA}

The power amplifier of the TRF7970A is supplied through V_{DD_PA} (pin 4). The positive supply pin for the RF power amplifier is externally connected to the regulator output V_{DD_RF} (pin 3).

I/O Level Shifter Supply: $V_{DD_I/O}$

The TRF7970A has a separate supply input $V_{DD_I/O}$ (pin 16) for the built-in I/O level shifter. The supported input voltage ranges from 1.8 V to V_{IN}, not exceeding 5.5 V. Pin 16 is used to supply the I/O interface pins (I/O_0 to I/O_7), IRQ, SYS_CLK, and DATA_CLK pins of the reader. In typical applications, $V_{DD_I/O}$ is directly connected to V_{DD_X}, while V_{DD_X} also supplies the MCU. This ensures that the I/O signal levels of the MCU match the logic levels of the TRF7970A.

Negative Supply Connections: V_{SS}, V_{SS_TX}, V_{SS_RX}, V_{SS_A}, V_{SS_PA}

The negative supply connections V_{SS_X} of each functional block are all externally connected to GND.

The substrate connection is V_{SS} (pin 10), the analog negative supply is V_{SS_A} (pin 15), the logic negative supply is V_{SS_D} (pin 29), the RF output stage negative supply is V_{SS_PA} (pin 6), and the negative supply for the RF receiver V_{SS_RX} (pin 7).

6.3.2 Supply Regulator Settings

The input supply voltage mode of the reader needs to be selected. This is done in the Chip Status Control register (0x00). Bit 0 in register 0x00 selects between 5-V or 3-V input supply voltage. The default configuration is 5 V, which reflects an operating supply voltage range of 4.3 V to 5.5 V. If the supply voltage is below 4.3 V, the 3-V configuration should be used.

As V_{DD_RF} is increased, the system can become more susceptible to noise coupling on the RX lines. For minimum noise coupling, TI recommends using the value of 0x00. For improved range, higher V_{DD_RF} voltages may be set, but complete system testing is required to determine the value which provides optimal performance.

The various regulators can be configured to operate in automatic or manual mode. This is done in the Regulator and I/O Control register (0x0B), as shown in 表 6-1 and 表 6-2.

表 6-1. Supply Regulator Setting: 5-V System

REGISTER ADDRESS (hex)	OPTION BITS SETTING IN REGULATOR CONTROL REGISTER (1)								COMMENTS
	B7	B6	B5	B4	B3	B2	B1	B0	
Automatic Mode (default)									
0B	1	x	x	x	x	x	0	0	Automatic regulator setting 400-mV difference
Manual Mode									
0B	0	x	x	x	x	1	1	1	V_{DD_RF} = 5 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	1	1	0	V_{DD_RF} = 4.9 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	1	0	1	V_{DD_RF} = 4.8 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	1	0	0	V_{DD_RF} = 4.7 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	0	1	1	V_{DD_RF} = 4.6 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	0	1	0	V_{DD_RF} = 4.5 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	0	0	1	V_{DD_RF} = 4.4 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	0	0	0	V_{DD_RF} = 4.3 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V

(1) x = Don't care

表 6-2. Supply Regulator Setting: 3-V System

REGISTER ADDRESS (hex)	OPTION BITS SETTING IN REGULATOR CONTROL REGISTER (1)								COMMENTS
	B7	B6	B5	B4	B3	B2	B1	B0	
Automatic Mode (default)									
0B	1	x	x	x	x	x	0	0	Automatic regulator setting 400-mV difference
Manual Mode									
0B	0	x	x	x	x	1	1	1	V_{DD_RF} = 3.4 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0	x	x	x	x	1	1	0	V_{DD_RF} = 3.3 V, V_{DD_A} = 3.3 V, V_{DD_X} = 3.3 V
0B	0	x	x	x	x	1	0	1	V_{DD_RF} = 3.2 V, V_{DD_A} = 3.2 V, V_{DD_X} = 3.2 V
0B	0	x	x	x	x	1	0	0	V_{DD_RF} = 3.1 V, V_{DD_A} = 3.1 V, V_{DD_X} = 3.1 V
0B	0	x	x	x	x	0	1	1	V_{DD_RF} = 3.0 V, V_{DD_A} = 3.0 V, V_{DD_X} = 3.0 V
0B	0	x	x	x	x	0	1	0	V_{DD_RF} = 2.9 V, V_{DD_A} = 2.9 V, V_{DD_X} = 2.9 V
0B	0	x	x	x	x	0	0	1	V_{DD_RF} = 2.8 V, V_{DD_A} = 2.8 V, V_{DD_X} = 2.8 V
0B	0	x	x	x	x	0	0	0	V_{DD_RF} = 2.7 V, V_{DD_A} = 2.7 V, V_{DD_X} = 2.7 V

(1) x = Don't care

The regulator configuration function adjusts the regulator outputs by default to 400 mV below V_{IN} level, but not higher than 5 V for V_{DD_RF}, 3.4 V for V_{DD_A} and V_{DD_X}. This ensures the highest possible supply voltage for the RF output stage while maintaining an adequate PSRR (power supply rejection ratio).

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6.3.3 Power Modes

The chip has several power states, which are controlled by two input pins (EN and EN2) and several bits in the chip status control register (0x00) (see 表 6-3 and 表 6-4).

表 6-3. 3.3-V Operation Power Modes(1)

MODE	EN2	EN	CHIP STATUS CONTROL REGISTER (0x00)	REGULATOR CONTROL REGISTER (0x0B)	TRANSMITTER	RECEIVER	SYS_CLK (13.56 MHz)	SYS_CLK (60 kHz)	V_{DD_X}	TYPICAL CURRENT (mA)	TYPICAL POWER OUT (dBm)
Power down	0	0	XX	XX	OFF	OFF	OFF	OFF	OFF	<0.001	-
Sleep mode	1	0	XX	XX	OFF	OFF	OFF	ON	ON	0.120	-
Standby mode at +3.3 VDC	X	1	80	00	OFF	OFF	ON	X	ON	2	-
Mode 1 at +3.3 VDC	X	1	00	00	OFF	OFF	ON	X	ON	3	-
Mode 2 at +3.3 VDC	X	1	02	00	OFF	ON	ON	X	ON	9	-
Mode 3 (half power) at +3.3 VDC	X	1	30	07	ON	ON	ON	X	ON	53	14.5
Mode 4 (full power) at +3.3 VDC	X	1	20	07	ON	ON	ON	X	ON	67	17

(1) X = Don't care

表 6-4. 5-V Operation Power Modes(1)

MODE	EN2	EN	CHIP STATUS CONTROL REGISTER (0x00)	REGULATOR CONTROL REGISTER (0x0B)	TRANSMITTER	RECEIVER	SYS_CLK (13.56 MHz)	SYS_CLK (60 kHz)	V_{DD_X}	TYPICAL CURRENT (mA)	TYPICAL POWER OUT (dBm)
Power down	0	0	XX	XX	OFF	OFF	OFF	OFF	OFF	<0.001	-
Sleep mode	1	0	XX	XX	OFF	OFF	OFF	ON	ON	0.120	-
Standby mode at +5 VDC	X	1	81	07	OFF	OFF	ON	X	ON	3	-
Mode 1 at +5 VDC	X	1	01	07	OFF	OFF	ON	X	ON	5	-
Mode 2 at +5 VDC	X	1	03	07	OFF	ON	ON	X	ON	10.5	-
Mode 3 (half power) at +5 VDC	X	1	31	07	ON	ON	ON	X	ON	70	20
Mode 4 (full power) at +5 VDC	X	1	21	07	ON	ON	ON	X	ON	130	23

(1) X = Don't care

表 6-3 and 表 6-4 show the configuration for the different power modes when using a 3.3-V or 5-V system supply, respectively. The main reader enable signal is pin EN. When EN is set high, all of the reader regulators are enabled, the 13.56-MHz oscillator is running and the SYS_CLK (output clock for external microcontroller) is also available.

The input pin EN2 has two functions:

- A direct connection from EN2 to V_{IN} to ensure the availability of the regulated supply V_{DD_X} and an auxiliary clock signal (60 kHz, SYS_CLK) for an external MCU. This mode (EN = 0, EN2 = 1) is intended for systems in which the MCU is also being supplied by the reader supply regulator (V_{DD_X}) and the MCU clock is supplied by the SYS_CLK output of the reader. This allows the MCU supply and clock to be available during sleep mode.
- EN2 enables the start-up of the reader system from complete power down (EN = 0, EN2 = 0). In this case the EN input is being controlled by the MCU (or other system device) that is without supply voltage during complete power down (thus unable to control the EN input). A rising edge applied to the EN2 input (which has an approximately 1-V threshold level) starts the reader supply system and 13.56-MHz oscillator (identical to condition EN = 1).

When user MCU is controlling EN and EN2, a delay of 1 ms between EN and EN2 must be used. If the MCU controls only EN, TI recommends connecting EN2 to either V_{IN} or GND, depending on the application MCU requirements for V_{DD_X} and SYS_CLK.

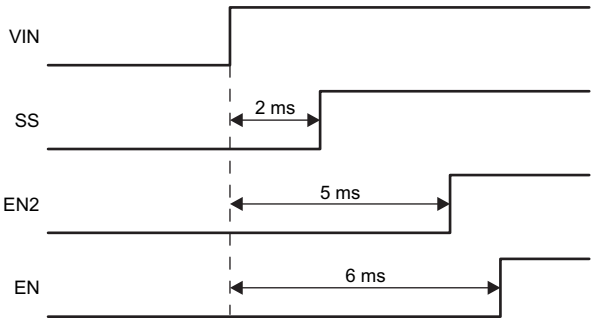

图 6-3. Nominal Start-up Sequence Using SPI With SS (MCU Controls EN2)

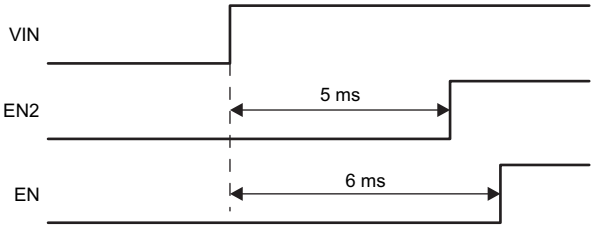

图 6-4. Nominal Start-up Sequence Using Parallel (MCU Controls EN2)

This start-up mode lasts until all of the regulators have settled and the 13.56-MHz oscillator has stabilized. If the EN input is set high (EN = 1) by the MCU (or other system device), the reader stays active. If the EN input is not set high (EN = 0) within 100 µs after the SYS_CLK output is switched from auxiliary clock (60 kHz) to high-frequency clock (derived from the crystal oscillator), the reader system returns to complete Power-Down Mode 1. This option can be used to wake-up the reader system from complete Power Down (PD Mode 1) by using a pushbutton switch or by sending a single pulse.

After the reader EN line is high, the other power modes are selected by control bits within the chip status control register (0x00). The power mode options and states are listed in 表 6-3.

When EN is set high (or on rising edge of EN2 and then confirmed by EN = 1) the supply regulators are activated and the 13.56-MHz oscillator is started. When the supplies are settled and the oscillator frequency is stable, the SYS_CLK output is switched from the auxiliary frequency of 60 kHz to the 13.56-MHz frequency derived from the crystal oscillator. At this point, the reader is ready to communicate and perform the required tasks. When this occurs, osc_ok (B6) of the RSSI Level and Oscillator Status register is set. The MCU can then program the Chip Status Control register 0x00 and select the operation mode by programming the additional registers.

- Standby Mode (bit 7 = 1 of register 0x00), the reader is capable of recovering to full operation in 100 µs.
- Mode 1 (active mode with RF output disabled, bit 5 = 0 and bit 1 = 0 of register 0x00) is a low power mode which allows the reader to recover to full operation within 25 µs.
- Mode 2 (active mode with only the RF receiver active, bit 1 = 1 of register 0x00) can be used to measure the external RF field (as described in RSSI measurements paragraph) if reader-to-reader anticollision is implemented.
- Modes 3 and 4 (active modes with the entire RF section active, bit 5 = 1 of register 0x00) are the normal modes used for normal transmit and receive operations.

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6.4 Receiver – Analog Section

6.4.1 Main and Auxiliary Receivers

The TRF7970A has two receiver inputs: RX_IN1 (pin 8) and RX_IN2 (pin 9). Each of the input is connected to an external capacitive voltage divider to ensure that the modulated signal from the tag is available on at least one of the two inputs. This architecture eliminates any possible communication holes that may occur from the tag to the reader.

The two RX inputs (RX_IN1 and RX_IN2) are multiplexed into two receivers - the main receiver and the auxiliary receiver. Only the main receiver is used for reception, the auxiliary receiver is used for signal quality monitoring. Receiver input multiplexing is controlled by bit B3 in the Chip Status Control register (address 0x00).

After start-up, RX_IN1 is multiplexed to the main receiver which is composed of an RF envelope detection, first gain and band-pass filtering stage, second gain and filtering stage with AGC. Only the main receiver is connected to the digitizing stage which output is connected to the digital processing block. The main receiver also has an RSSI measuring stage, which measures the strength of the demodulated signal (subcarrier signal).

The primary function of the auxiliary receiver is to monitor the RX signal quality by measuring the RSSI of the demodulated subcarrier signal (internal RSSI). After start-up, RX_IN2 is multiplexed to the auxiliary receiver. The auxiliary receiver has an RF envelope detection stage, first gain and filtering with AGC stage and finally the auxiliary RSSI block.

The default MUX setting is RX_IN1 connected to the main receiver and RX_IN2 connected to the auxiliary receiver. To determine the signal quality, the response from the tag is detected by the "main" (pin RX_IN1) and "auxiliary" (pin RX_IN2) RSSI. Both values measured and stored in the RSSI Levels and Oscillator Status register (address 0x0F). The MCU can read the RSSI values from the TRF7970A RSSI register and make the decision if swapping the input- signals is preferable or not. Setting B3 in Chip Status Control register (address 0x00) to 1 connects RX_IN1 (pin 8) to the auxiliary received and RX_IN2 (pin 9) to the main receiver.

The main and auxiliary receiver input stages are RF envelope detectors. The RF amplitude at RX_IN1 and RX_IN2 should be approximately 3 VPP for a V_{IN}supply level greater than 3.3 V. If the V_{IN} level is lower, the RF input peak-to-peak voltage level should not exceed the V_{IN}level.

6.4.2 Receiver Gain and Filter Stages

The first gain and filtering stage has a nominal gain of 15 dB with an adjustable band-pass filter. The band-pass filter has programmable 3-dB corner frequencies between 110 kHz to 450 kHz for the high-pass filter and 570 kHz to 1500 kHz for the low-pass filter. After the band-pass filter, there is another gain-and-filtering stage with a nominal gain of 8 dB and with frequency characteristics identical to the first band-pass stage.

The internal filters are configured automatically depending on the selected ISO communication standard in the ISO Control register (address 0x01). If required, additional fine tuning can be done by writing directly to the RX Special Setting registers (address 0x0A).

表 6-5 shows the various settings for the receiver analog section. Setting B4, B5, B6, and B7 to 0 results in a band-pass characteristic of 240 kHz to 1.4 MHz, which is appropriate for ISO/IEC 14443 B 106 kbps, ISO/IEC 14443 A and B data rates of 212 kbps and 424 kbps, and FeliCa 424 kbps.

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表 6-5. RX Special Setting Register (0x0A)

Function: Sets the gains and filters directly			
Default: 0x40 at POR = H or EN = L, and at each write to the ISO Control register (0x01). When bits B7, B6, B5 and B4 are all zero, the filters are set for ISO/IEC 14443 B (240 kHz to 1.4 MHz).			
Bit	**Name**	**Function**	**Description**
B7	C212	Band-pass 110 kHz to 570 kHz	Appropriate for 212-kHz subcarrier system (FeliCa)
B6	C424	Band-pass 200 kHz to 900 kHz	Appropriate for 424-kHz subcarrier used in ISO/IEC 15693
B5	M848	Band-pass 450 kHz to 1.5 MHz	Appropriate for Manchester-coded 848-kHz subcarrier used in ISO/IEC 14443 A and B
B4	hbt	Band-pass 100 kHz to 1.5 MHz Gain reduced for 18 dB	Appropriate for highest bit rate (848 kbps) used in high-bit-rate ISO/IEC 14443
B3	gd1	00 = Gain reduction 0 dB 01 = Gain reduction for 5 dB 10 = Gain reduction for 10 dB 11 = Gain reduction for 15 dB	Sets the RX gain reduction and reduces sensitivity
B2	gd2		
B1	Reserved		
B0	Reserved		

6.5 Receiver – Digital Section

The output of the TRF7970A analog receiver block is a digitized subcarrier signal and is the input to the digital receiver block, which consists of two sections that partly overlap. The digitized subcarrier signal is a digital representation of the modulation signal on the RF envelope. The two sections of the digital receiver block are the *protocol bit decoder* section and the *framing logic* section.

The protocol bit decoder section converts the subcarrier coded signal into a serial bit stream and a data clock. The decoder logic is designed for maximum error tolerance. This tolerance lets the decoder section successfully decode even partly corrupted subcarrier signals that would otherwise be lost due to noise or interference.

The framing logic section formats the serial bit stream data from the protocol bit decoder stage into data bytes. During the formatting process, special signals such as the start of frame (SOF), end of frame (EOF), start of communication, and end of communication are automatically removed. The parity bits and CRC bytes are also checked and removed. The end result is "clean or raw" data that is sent to the 127-byte FIFO register where it can be read by the external microcontroller system. Providing the data this way, in conjunction with the timing register settings of the TRF7970A, means that the firmware developer does not need to know the finer details of the ISO protocols to create a very robust application, especially in low-cost platforms in which code space is at a premium and high performance is still required.

The start of the receive operation (successfully received SOF) sets the IRQ flags in the IRQ Status register (0x0C). The end of the receive operation is signaled to the external system MCU by setting pin 13 (IRQ) to high. When data is received in the FIFO, an interrupt is sent to the MCU to signal that there is data to be read from the FIFO. The FIFO Status register (0x1C) should be used to provide the number of bytes that should be clocked out during the actual FIFO read. Additionally, an interrupt is sent to the MCU when the received data occupies 75% of the FIFO capacity to signal that the data should be removed from the FIFO. By default, that interrupt is triggered once the received data packet is longer than 124 bytes. This setting can be modified in the Adjustable FIFO IRQ Levels register (0x14).

Any error in the data format, parity, or CRC is detected and notified to the external system by setting pin 13 (IRQ) to high. The source condition of the interrupt is available in the IRQ Status register (0x0C). 节 6.15.3.3.1 describes the bit coding description of this register. The information in the IRQ Status register differs if the chip is configured as an RFID reader or as an NFC device (including card emulation). 节 6.13 describes NFC operation.

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The framing section also supports bit-collision detection as specified in ISO/IEC 14443 A and ISO/IEC 15693. When a bit collision is detected, an interrupt request is sent and a flag is set in the IRQ Status register (0x0C). For ISO/IEC 14443 A specifically, the position of the bit collision is written in two registers: partly in the Collision Position register (0x0E) and partly in the Collision Position and Interrupt Mask register (0x0D) (bits B6 and B7).

This collision position is presented as sequential bit number, where the count starts immediately after the start bit. This means a collision in the first bit of a UID would give the value 00 0001 0000 in these registers when their contents are combined after being read (the count starts with 0 and the first 16 bits are the command code and the number of valid bits [NVB] byte).

The receive section also contains two timers.

The RX wait time timer is controlled by the value in the RX Wait Time register (0x08). This timer defines the time interval after the end of the transmit operation during which the receive decoders are not active (held in reset state). This prevents false detections resulting from transients following the transmit operation. The value of the RX Wait Time register (0x08) defines the time in increments of 9.44 µs. This register is preset at every write to the ISO Control register (0x01) according to the minimum tag response time defined by each standard.

The RX no response timer is controlled by the RX No Response Wait Time register (0x07). This timer measures the time from the start of the slot in the anticollision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in the IRQ Status register (0x0C). This enables the external controller to be relieved of the task of detecting empty slots. The wait time is stored in the register in increments of 37.76 µs. This register is also preset automatically for every new protocol selection.

The main register controlling the digital part of the receiver is the ISO Control register (0x01). By writing to this register, the user selects the protocol to be used. With each new write in this register, all related registers are preset to their defaults for the protocol, so no further adjustments in other registers are needed for proper operation. 表 6-6 describes the bit fields of the ISO Control register (0x01).

注

If changes to other registers are needed to fine-tune the system, those changes must be made after setting the ISO Control register (0x01).

表 6-6. Coding of the ISO Control Register

BIT	SIGNAL NAME	FUNCTION	COMMENTS
B7	rx_crc_n	Receiving without CRC	1 = No RX CRC 0 = RX CRC
B6	dir_mode	Direct mode type	0 = Output is subcarrier data 1 = Output is bit stream and clock from decoder selected by ISO bits
B5	rfid	RFID mode	0 = RFID reader mode 1 = NFC or card emulator mode
B4	iso_4	RFID protocol, NFC target	RFID: Mode selection NFC: 0 = NFC target 1 = NFC initiator
B3	iso_3	RFID protocol, NFC mode	RFID: Mode selection (see 表 6-7) NFC: 0 = Passive mode 1 = Active mode
B2	iso_2	RFID protocol, Card Emulation	RFID: Mode selection NFC: 0 = NFC normal modes 1 = Card emulation mode
B1	iso_1	RFID protocol, NFC bit rate	RFID: Mode selection NFC: Bit rate selection or Card Emulation selection (see 表 6-8)
B0	iso_0	RFID protocol, NFC bit rate	RFID: Mode selection NFC: Bit rate selection or Card Emulation selection (see 表 6-8)

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表 6-7. Coding of the ISO Control Register For RFID Mode (B5 = 0)

Iso_4	Iso_3	Iso_2	Iso_1	Iso_0	PROTOCOL	REMARKS
0	0	0	0	0	ISO/IEC 15693 low bit rate, one subcarrier, 1 out of 4	
0	0	0	0	1	ISO/IEC 15693 low bit rate, one subcarrier, 1 out of 256	
0	0	0	1	0	ISO/IEC 15693 high bit rate, one subcarrier, 1 out of 4	Default for RFID IC
0	0	0	1	1	ISO/IEC 15693 high bit rate, one subcarrier, 1 out of 256	
0	0	1	0	0	ISO/IEC 15693 low bit rate, double subcarrier, 1 out of 4	
0	0	1	0	1	ISO/IEC 15693 low bit rate, double subcarrier, 1 out of 256	
0	0	1	1	0	ISO/IEC 15693 high bit rate, double subcarrier, 1 out of 4	
0	0	1	1	1	ISO/IEC 15693 high bit rate, double subcarrier, 1 out of 256	
0	1	0	0	0	ISO/IEC 14443 A, bit rate 106 kbps	
0	1	0	0	1	ISO/IEC 14443 A high bit rate 212 kbps	RX bit rate when TX rate different from RX rate (see register 0x03)
0	1	0	1	0	ISO/IEC 14443 A high bit rate 424 kbps	
0	1	0	1	1	ISO/IEC 14443 A high bit rate 848 kbps	
0	1	1	0	0	ISO/IEC 14443 B, bit rate 106 kbps	
0	1	1	0	1	ISO/IEC 14443 B high bit rate 212 kbps	RX bit rate when TX rate different from RX rate (see register 0x03)
0	1	1	1	0	ISO/IEC 14443 B high bit rate 424 kbps	
0	1	1	1	1	ISO/IEC 14443 B high bit rate 848 kbps	
1	0	0	1	1	Reserved	
1	0	1	0	0	Reserved	
1	1	0	1	0	FeliCa 212 kbps	
1	1	0	1	1	FeliCa 424 kbps	

表 6-8. Coding of the ISO Control Register For NFC Mode (B5 = 1, B2 = 0) or Card Emulation (B5 = 1, B2 = 1)

Iso_1	Iso_0	NFC (B5 = 1, B2 = 0)	CARD EMULATION (B5 = 1, B2 = 1)
0	0	N/A	ISO/IEC 14443 A
0	1	106 kbps	ISO/IEC 14443 B
1	0	212 kbps	N/A
1	1	424 kbps	N/A

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6.5.1 Received Signal Strength Indicator (RSSI)

The TRF7970A incorporates in total three independent RSSI building blocks: Internal Main RSSI, Internal Auxiliary RSSI, and External RSSI. The internal RSSI blocks measure the amplitude of the subcarrier signal, and the external RSSI block measures the amplitude of the RF carrier signal at the receiver input.

6.5.1.1 Internal RSSI – Main and Auxiliary Receivers

Each receiver path has its own RSSI block to measure the envelope of the demodulated RF signal (subcarrier). Internal Main RSSI and Internal Auxiliary RSSI are identical however connected to different RF input pins. The Internal RSSI is intended for diagnostic purposes to set the correct RX path conditions.

The internal RSSI values can be used to adjust the RX gain settings or determine which RX path (main or auxiliary) provides the greater amplitude and, hence, to determine if the MUX may need to be reprogrammed to swap the RX input signal. The measuring system latches the peak value, so the RSSI level can be read after the end of each receive packet. The RSSI register values are reset with every transmission (TX) by the reader. This ensures an updated RSSI measurement for each new tag response.

The Internal RSSI has 7 steps (3 bit) with a typical increment of approximately 4 dB. The operating range is between 600 mV_{PP} and 4.2 V_{PP} with a typical step size of approximately 600 mV. Both Internal Main and Internal Auxiliary RSSI values are stored in the RSSI Levels and Oscillator Status register (0x0F). The nominal relationship between the input RF peak level and the RSSI value is shown in 图 6-5.

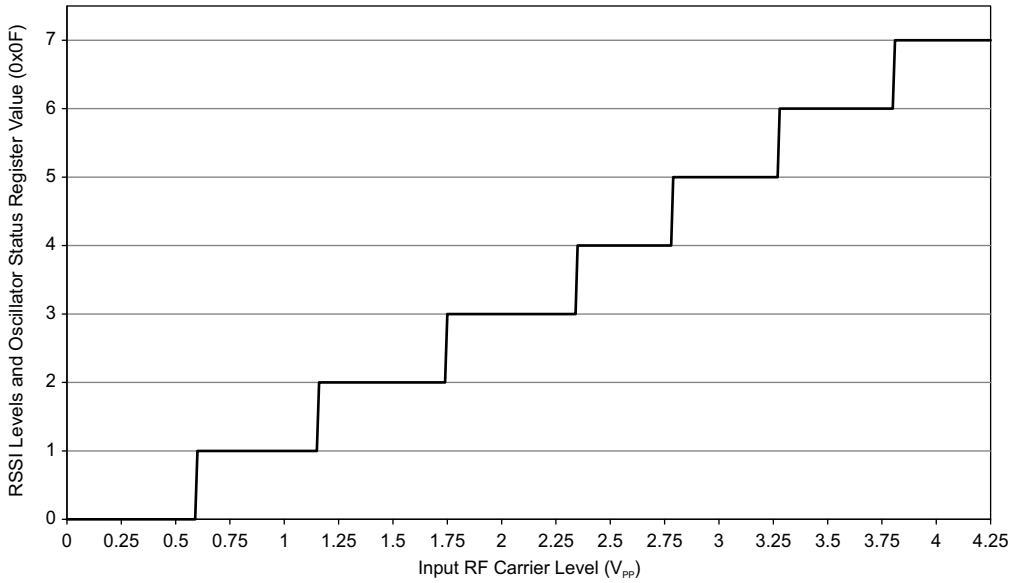

图 6-5. Digital Internal RSSI (Main and Auxiliary) Value vs RF Input Level in V_{PP} (V)

This RSSI measurement is done during the communication to the Tag; this means the TX must be on. Bit 1 in the Chip Status Control register (0x00) defines if Internal RSSI or the External RSSI value is stored in the RSSI Levels and Oscillator Status register (0x0F). Direct command 0x18 is used to trigger an Internal RSSI measurement.

6.5.1.2 External RSSI

The external RSSI is mainly used to check for any external 13.56-MHz signals at the receiver RX_IN1 input. The external RSSI measurement should be used before turning on the transmitter to prevent RF field collisions. This is especially important for active mode, when both devices emit their own RF field. The level of the RF signal received at the antenna is measured and stored in the RSSI Levels and Oscillator Status register (0x0F). 图 6-6 shows the relationship between the voltage at the RX_IN1 input and the 3-bit code.

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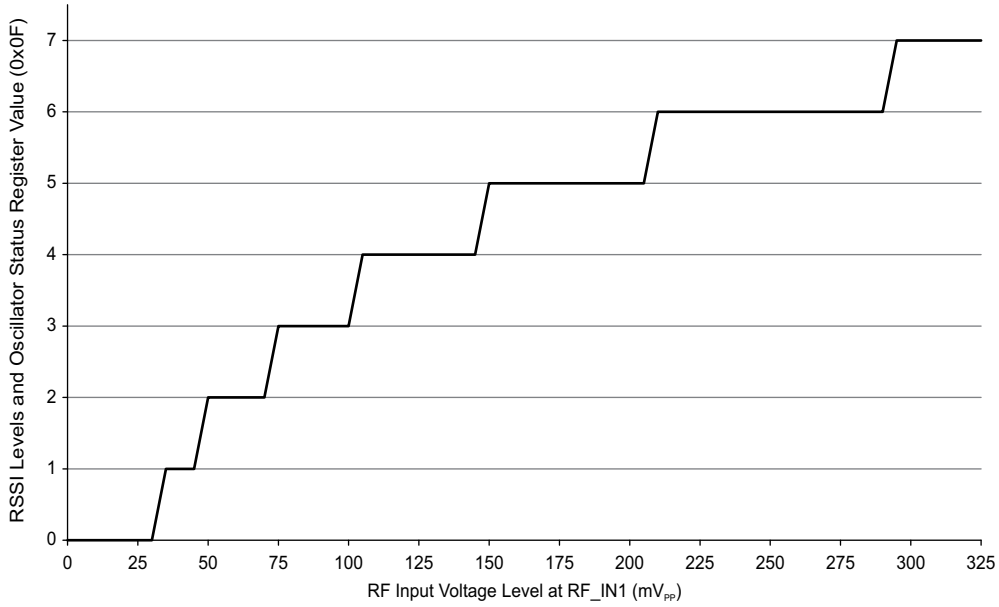

图 6-6. Digital External RSSI Value vs RF Input Level in V_{PP} (mV)

The relation between the 3-bit code and the external RF field strength (A/m) sensed by the antenna must be determined by calculation or by experiments for each antenna design. The antenna Q-factor and connection to the RF input influence the result. Direct command 0x19 is used to trigger an external RSSI measurement.

For clarity, to check the internal or external RSSI value independent of any other operation, the user must:

1. Set transmitter to desired state (on or off) using Bit 5 of Chip Status Control register (0x00) and enable receiver using Bit 1.
2. Check internal or external RSSI using direct commands 0x18 or 0x19, respectively. This action places the RSSI value in the RSSI register.
3. Delay at least 50 µs.
4. Read the RSSI register using direct command 0x0F; values range from 0x40 to 0x7F.
5. Repeat steps 1 to 4 as needed. The register is reset when it is read.

6.6 Oscillator Section

The 13.56-MHz or 27.12-MHz crystal (or oscillator) is controlled by the Chip Status Control register (0x00) and the EN and EN2 terminals. The oscillator generates the RF frequency for the RF output stage as well as the clock source for the digital section. The buffered clock signal is available at pin 27 (SYS_CLK) for any other external circuits. B4 and B5 inside the Modulation and SYS_CLK register (0x09) can be used to divide the external SYS_CLK signal at pin 27 by 1, 2, or 4.

Typical start-up time from complete power down is in the range of 3.5 ms.

During Power Down Mode 2 (EN = 0, EN2 = 1) the frequency of SYS_CLK is switched to 60 kHz (typical).

The crystal needs to be connected between pin 30 and pin 31. The external shunt capacitors values for C_1 and C_2 must be calculated based on the specified load capacitance of the crystal being used. The external shunt capacitors are calculated as two identical capacitors in series plus the stray capacitance of the TRF7970A and parasitic PCB capacitance in parallel to the crystal.

The parasitic capacitance (C_S, stray and parasitic PCB capacitance) can be estimated at 4 to 5 pF (typical).

As an example, using a crystal with a required load capacitance (C_L) of 18 pF, the calculation is shown in 公式 1.

$C_1 = C_2 = 2 \times (C_L – C_S) = 2 \times (18\ pF – 4.5\ pF) = 27\ pF$ (1)

A 27-pF capacitor must be placed on pins 30 and 31 to ensure proper crystal oscillator operation.

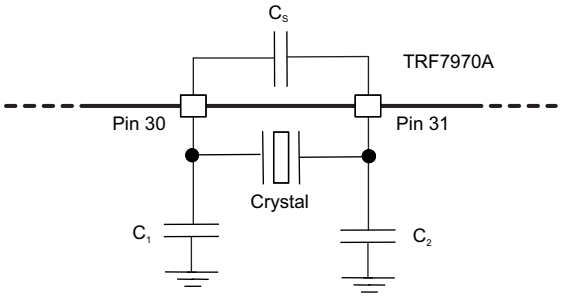

图 6-7. Crystal Block Diagram

Any crystal used with TRF7970A should meet the minimum characteristics in 表 6-9.

表 6-9. Minimum Crystal Recommendations

PARAMETER	SPECIFICATION
Frequency	13.56 MHz or 27.12 MHz
Mode of operation	Fundamental
Type of resonance	Parallel
Frequency tolerance	±20 ppm
Aging	< 5 ppm/year
Operation temperature range	–40°C to 85°C

As an alternative, an external clock oscillator source can be connected to pin 31 to provide the system clock; pin 30 can be left open.

6.7 Transmitter – Analog Section

The 13.56-MHz oscillator generates the RF signal for the PA stage. The power amplifier consists of a driver with selectable output resistance of nominal 4 Ω or 8 Ω. The transmit power level is set by bit B4 in the Chip Status Control register (0x00). The transmit power levels are selectable between 100 mW (half power) or 200 mW (full power) when configured for 5-V automatic operation. The transmit power levels are selectable between 33 mW (half power) or 70 mW (full power) when configured for 3-V automatic operation.

The ASK modulation depth is controlled by bits B0, B1, and B2 in the Modulator and SYS_CLK Control register (0x09). The ASK modulation depth range can be adjusted between 7% to 30% or 100% (OOK).

External control of the transmit modulation depth is possible by setting the ISO Control register (0x01) to direct mode. While operating the TRF7970A in direct mode, the transmit modulation is made possible by selecting the modulation type ASK or OOK at pin 12. External control of the modulation type is made possible only if enabled by setting B6 in the Modulator and SYS_CLK Control register (0x09) to 1.

In normal operation mode, the length of the modulation pulse is defined by the protocol selected in the ISO Control register (0x01). With a high-Q antenna, the modulation pulse is typically prolonged, and the tag detects a longer pulse than intended. For such cases, the modulation pulse length needs to be corrected by using the TX Pulse Length Control register (0x06).

If the register contains all zeros, then the pulse length is governed by the protocol selection. If the register contains a value other than 0x00, the pulse length is equal to the value of the register multiplied by 73.7 ns; therefore, the pulse length can be adjusted between 73.7 ns and 18.8 µs in 73.7-ns increments.

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6.8 Transmitter – Digital Section

The digital part of the transmitter is a mirror of the receiver. The settings controlled the ISO Control register (0x01) are applied to the transmitter just like the receiver. In the TRF7970A default mode the TRF7970A automatically adds these special signals: start of communication, end of communication, SOF, EOF, parity bits, and CRC bytes.

The data is then coded to modulation pulse levels and sent to the RF output stage modulation control unit. Similar to working with the receiver, this means that the external system MCU must only load the FIFO with data, and all the microcoding is done automatically, again saving the firmware developer code space and time. Additionally, all of the registers used for transmit parameter control are automatically preset to optimum values when a new selection is entered into the ISO Control register (0x01).

注

The FIFO must be reset before starting any transmission with direct command 0x0F.

There are two ways to start the transmit operation:

- Send the transmit command and the number of bytes to be transmitted first, and then start to send the data to the FIFO. The transmission starts when first data byte is written into the FIFO.
- Load the number of bytes to be sent into registers 0x1D and 0x1E and load the data to be sent into the FIFO (address 0x1F), followed by sending a transmit command (see Direct Commands section). The transmission then starts when the transmit command is received.

注

If the data length is longer than the FIFO, the TRF7970A notifies the external system MCU when most of the data from the FIFO has been transmitted by sending an interrupt request with a flag in the IRQ register to indicate a FIFO low or high status. The external system should respond by loading the next data packet into the FIFO.

At the end of a transmit operation, the external system MCU is notified by interrupt request (IRQ) with a flag in IRQ register (0x0C) indicating TX is complete (example value = 0x80).

The TX Length registers also support incomplete byte transmission. The high two nibbles in register 0x1D and the nibble composed of bits B4 through B7 in register 0x1E store the number of complete bytes to be transmitted. Bit B0 in register 0x1E is a flag indicating that there are also additional bits to be transmitted that do not form a complete byte. The number of bits is stored in bits B1 through B3 of the same register (0x1E).

Some protocols have options, and there are two sublevel configuration registers to select the TX protocol options.

- ISO/IEC 14443 B TX Options register (0x02). This register controls the SOF and EOF selection and EGT selection for the ISO/IEC 14443 B protocol.
- ISO/IEC 14443 A High Bit Rate Options and Parity register (0x03). This register enables the use of different bit rates for RX and TX operations in the ISO/IEC 14443 high bit rate protocol and also selects the parity method in the ISO/IEC 14443 A high bit rate protocol.

The digital section also has a timer. The timer can be used to start the transmit operation at a specified time in accordance with a selected event.

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6.9 Transmitter – External Power Amplifier and Subcarrier Detector

The TRF7970A can be used in conjunction with an external TX power amplifier or external subcarrier detector for the receiver path. In this case, certain registers must be programmed as shown here:

- Bit B6 of the Regulator and I/O Control register (0x0B) must be set to 1. This setting has two functions: first, to provide a modulated signal for the transmitter if needed, and second, to configure the TRF7970A receiver inputs for an external demodulated subcarrier input.
- Bit B3 of the Modulation and SYS_CLK Control register (0x09) must be set to 1 (see 节 6.15.3.2.8). This function configures the ASK/OOK pin for either a digital or analog output (B3 = 0 enables a digital output, B3 = 1 enables an analog output). The design of an external power amplifier requires detailed RF knowledge. There are also readily designed and certified high-power HF reader modules on the market.

6.10 TRF7970A IC Communication Interface

6.10.1 General Introduction

The communication interface to the reader can be configured in two ways: with a eight line parallel interface (D0:D7) plus DATA_CLK, or with a 4-wire Serial Peripheral Interface (SPI). The SPI interface uses traditional Master Out/Slave In (MOSI), Master In/Slave Out (MISO), Slave Select, and DATA_CLK lines.

These communication modes are mutually exclusive; that is, only one mode can be used at a time in the application.

When the SPI interface is selected, the unused I/O_2, I/O_1, and I/O_0 pins must be hard-wired as shown in 表 6-10. At power up, the TRF7970A samples the status of these three pins and then enters one of the possible SPI modes.

The TRF7970A always behaves as the slave device, and the microcontroller (MCU) behaves as the master device. The MCU initiates all communications with the TRF7970A, and the TRF7970A makes use of the Interrupt Request (IRQ) pin in both parallel and SPI modes to prompt the MCU for servicing attention.

表 6-10. Pin Assignment in Parallel and Serial Interface Connection or Direct Mode

PIN	PARALLEL	PARALLEL (DIRECT MODE)	SPI WITH SS	SPI WITHOUT SS(1)
DATA_ CLK	DATA_CLK	DATA_CLK	DATA_CLK from master	DATA_CLK from master
I/O_7	A/D[7]	Not used	MOSI(2) = data in (reader in)	MOSI(2) = data in (reader in)
I/O_6	A/D[6]	Direct mode, data out (subcarrier or bit stream)	MISO(3) = data out (MCU out)	MISO(3) = data out (MCU out)
I/O_5(4)	A/D[5]	Direct mode, strobe – bit clock out	See (4).	See (4).
I/O_4	A/D[4]	Not used	SS – slave select(5)	Not used
I/O_3	A/D[3]	Not used	Not used	Not used
I/O_2	A/D[2]	Not used	At VDD	At VDD
I/O_1	A/D[1]	Not used	At VDD	At V_{SS}
I/O_0	A/D[0]	Not used	At V_{SS}	At V_{SS}
IRQ	IRQ interrupt	IRQ interrupt	IRQ interrupt	IRQ interrupt

(1) FIFO is not accessible in SPI without SS mode. See the *TRF7970A Silicon Errata* for detailed information.
(2) MOSI = master out, slave in
(3) MISO = master in, slave out
(4) I/O_5 pin is used only for information when data is put out of the chip (for example, reading 1 byte from the chip). It is necessary first to write in the address of the register (8 clocks) and then to generate another 8 clocks for reading out the data. The I/O_5 pin goes high during the second 8 clocks. But for normal SPI operations, I/O_5 pin is not used.
(5) Slave select pin is active low

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Communication is initialized by a start condition, which is expected to be followed by an Address/Command word (Adr/Cmd). The Adr/Cmd word is 8 bits long, and 表 6-11 shows its format.

表 6-11. Address and Command Word Bit Distribution

BIT	DESCRIPTION	BIT FUNCTION	ADDRESS	COMMAND
B7	Command control bit	0 = Address 1 = Command	0	1
B6	Read/Write	0 = Write 1 = Read	R/W	0
B5	Continuous address mode	1 = Continuous mode	R/W	0
B4	Address/Command bit 4		Adr 4	Cmd 4
B3	Address/Command bit 3		Adr 3	Cmd 3
B2	Address/Command bit 2		Adr 2	Cmd 2
B1	Address/Command bit 1		Adr 1	Cmd 1
B0	Address/Command bit 0		Adr 0	Cmd 0

The MSB (bit 7) determines if the word is to be used as a command or as an address. The last two columns of 表 6-11 show the function of the separate bits if either address or command is written. Data is expected once the address word is sent. In continuous-address mode (Cont. mode = 1), the first data that follows the address is written (or read) to (from) the given address. For each additional data, the address is incremented by one. Continuous mode can be used to write to a block of control registers in a single stream without changing the address; for example, setup of the predefined standard control registers from the MCU nonvolatile memory to the reader. In noncontinuous address mode (simple addressed mode), only one data word is expected after the address.

Address Mode is used to write or read the configuration registers or the FIFO. When writing more than 12 bytes to the FIFO, the Continuous Address Mode should be set to 1.

Command Mode is used to enter a command resulting in reader action (for example, initialize transmission, enable reader, and turn reader on or off).

The following sections give examples of the expected communications between an MCU and the TRF7970A.

6.10.1.1 Continuous Address Mode

图 6-8 summarizes the continuous address mode communication. 图 6-8 and 图 6-9 show the signals between the MCU and the TRF7970A.

表 6-12. Continuous Address Mode

Start	Adr x	Data(x)	Data(x+1)	Data(x+2)	Data(x+3)	Data(x+4)	...	Data(x+n)	StopCont

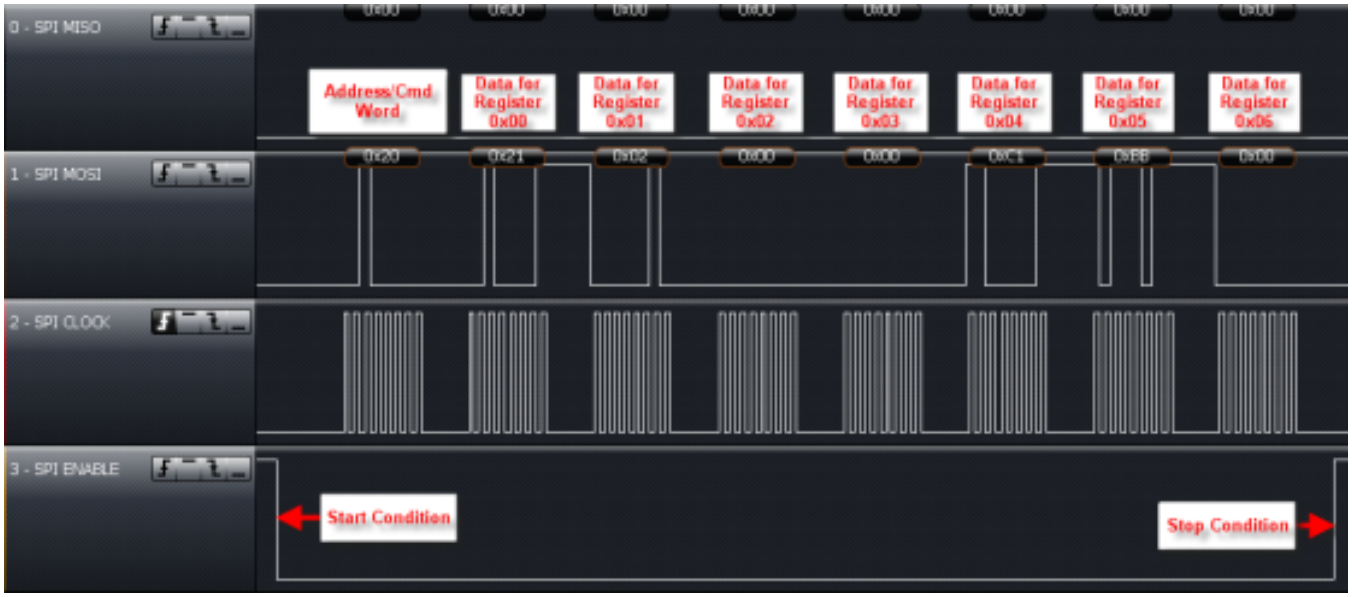

图 6-8. Continuous Address Register Write Example Starting With Register 0x00 Using SPI With SS

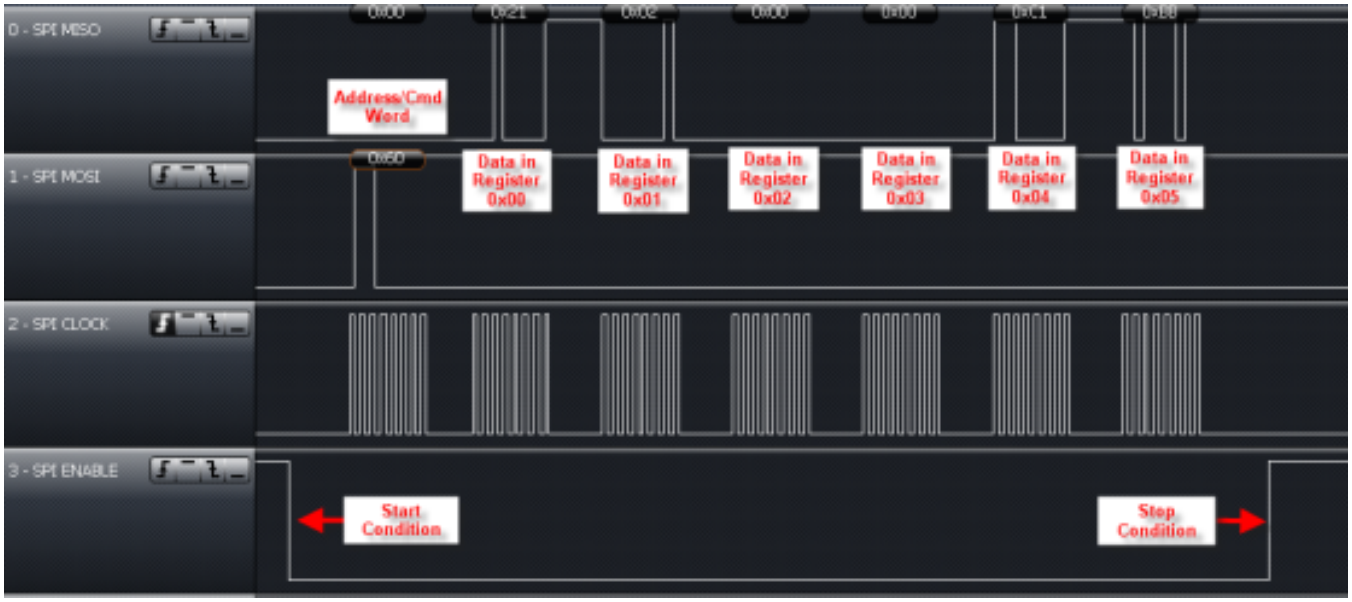

图 6-9. Continuous Address Register Read Example Starting With Register 0x00 Using SPI With SS

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6.10.1.2 Noncontinuous Address Mode (Single Address Mode)

表 6-13 summarizes the noncontinuous address (single address) mode communication. 图 6-10 and 图 6-11 show the signals between the MCU and the TRF7970A.

表 6-13. Noncontinuous Address Mode (Single Address Mode)

Start	Adr x	Data(x)	Adr y	Data(y)	...	Adr z	Data(z)	StopSgl

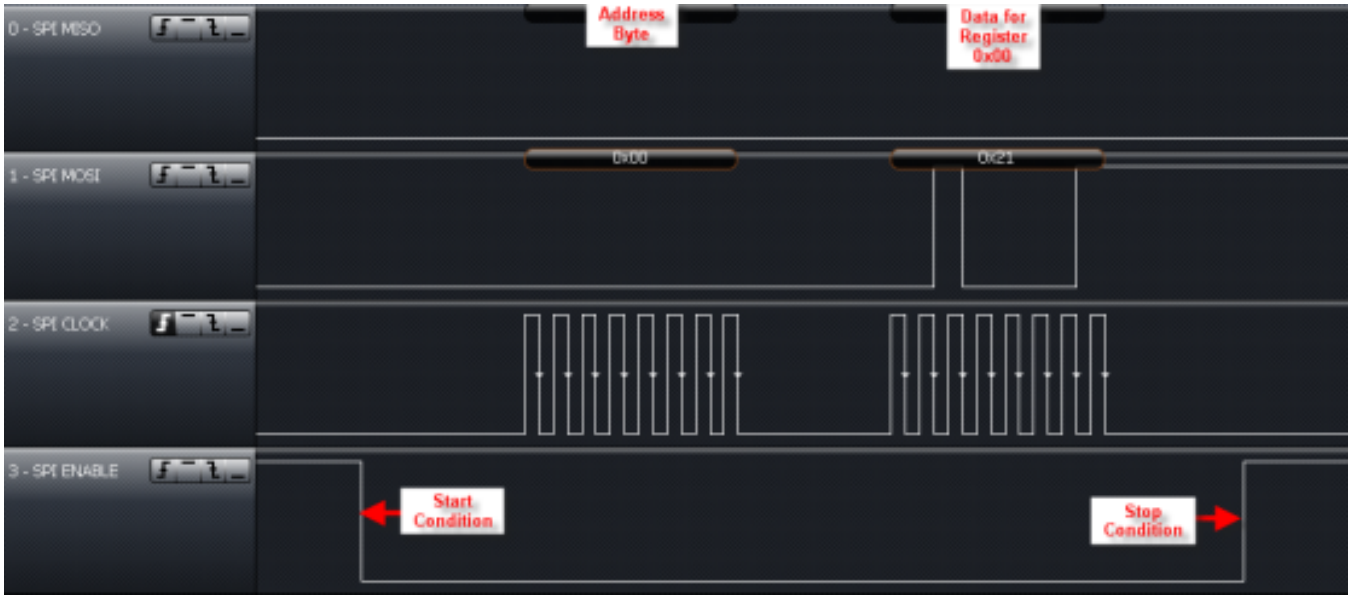

图 6-10. Single Address Register Write Example of Register 0x00 Using SPI With SS

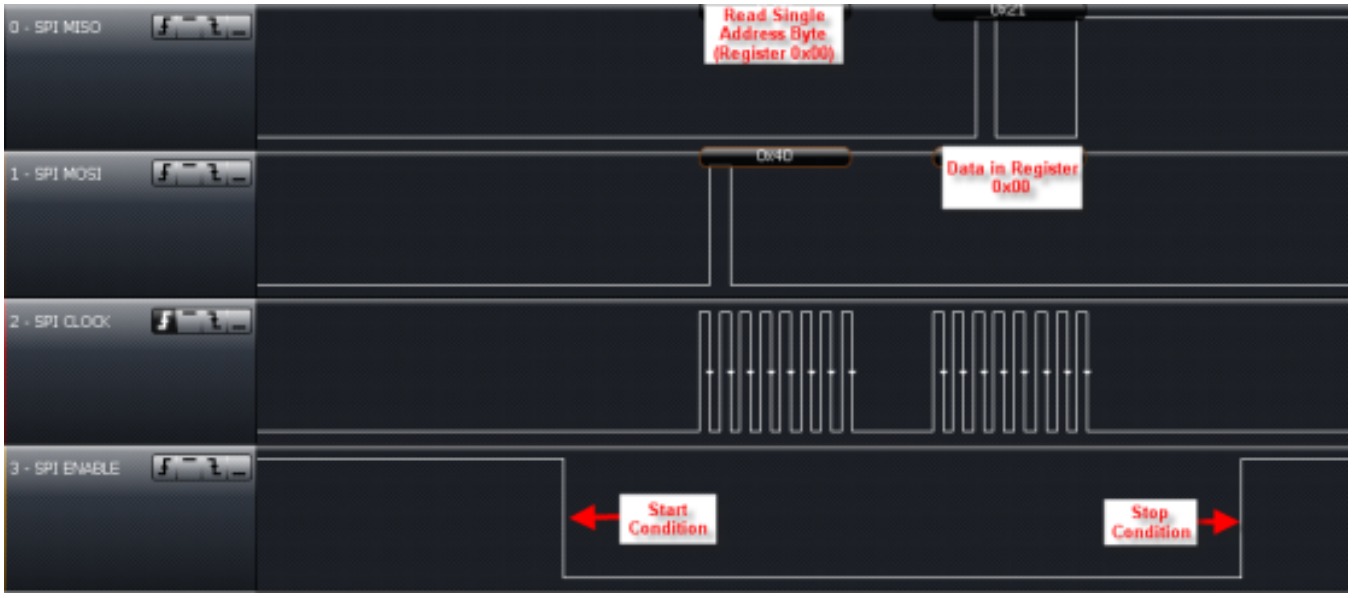

图 6-11. Single Address Register Read Example of Register 0x00 Using SPI With SS

6.10.1.3 Direct Command Mode

表 6-14 summarizes the direct command mode communication. 图 6-12 shows the signals between the MCU and the TRF7970A.

表 6-14. Direct Command Mode

Start	Cmd x	(Optional data or command)	Stop

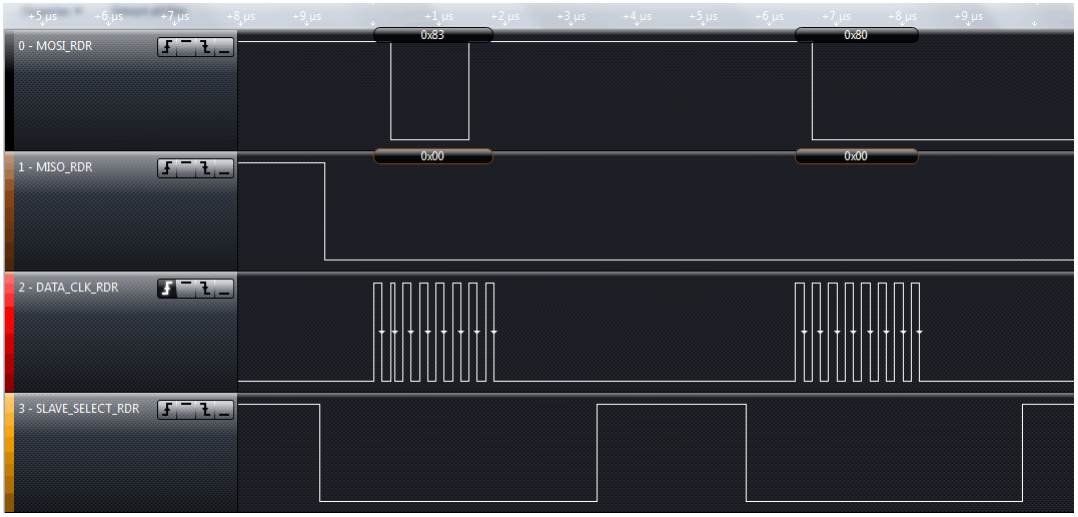

图 6-12. Direct Command Example of Sending 0x0F (Reset) Using SPI With SS

节 6.14 describes the other direct command codes from the MCU to the TRF7970A IC.

6.10.1.4 FIFO Operation

The FIFO is a 127-byte register at address 0x1F with byte storage locations 0 to 126. FIFO data is loaded in a cyclical manner and can be cleared by a reset command (0x0F) (see 图 6-12 showing this direct command).

Associated with the FIFO are two counters and three FIFO status flags. The first counter is a 7-bit FIFO byte counter (bits B0 to B6 in register 0x1C) that tracks the number of bytes loaded into the FIFO. If the number of bytes in the FIFO is n, the register value is n (number of bytes in FIFO register). For example, if 8 bytes are in the FIFO, the FIFO counter (Register 0x1C) has the hexadecimal value of 0x08 (binary value of 00001000).

A second counter (12 bits wide) indicates the number of bytes being transmitted (registers 0x1D and 0x1E) in a data frame. An extension to the transmission-byte counter is a 4-bit broken-byte counter also provided in register 0x1E (bits B0 to B3). Together these counters make up the TX length value that determines when the reader generates the EOF byte.

During transmission, the FIFO is checked for an almost-empty condition, and during reception for an almost-full condition. The maximum number of bytes that can be loaded into the FIFO in a single sequence is 127 bytes.

注

The number of bytes in a frame, transmitted or received, can be greater than 127 bytes.

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During transmission, the MCU loads the TRF7970A FIFO (or during reception the MCU removes data from the FIFO), and the FIFO counter counts the number of bytes being loaded into the FIFO. Meanwhile, the byte counter keeps track of the number of bytes being transmitted. An interrupt request is generated if the number of bytes in the FIFO triggers the watermark levels, which are configured in the Adjustable FIFO IRQ Levels register (0x14). The default setting is for the interrupt to be triggered when receiving 124 bytes during RX or having 4 bytes remaining during TX. These watermark levels are used so that MCU can send new data or read the data as necessary. The MCU must also validate the number of data bytes to be sent, so as to not surpass the value defined in the TX Length Byte registers (0x1D and 0x1E). The MCU also signals the transmit logic when the last byte of data is sent or was removed from the FIFO during reception.

图 6-13 shows an example of checking the FIFO Status register using SPI with SS.

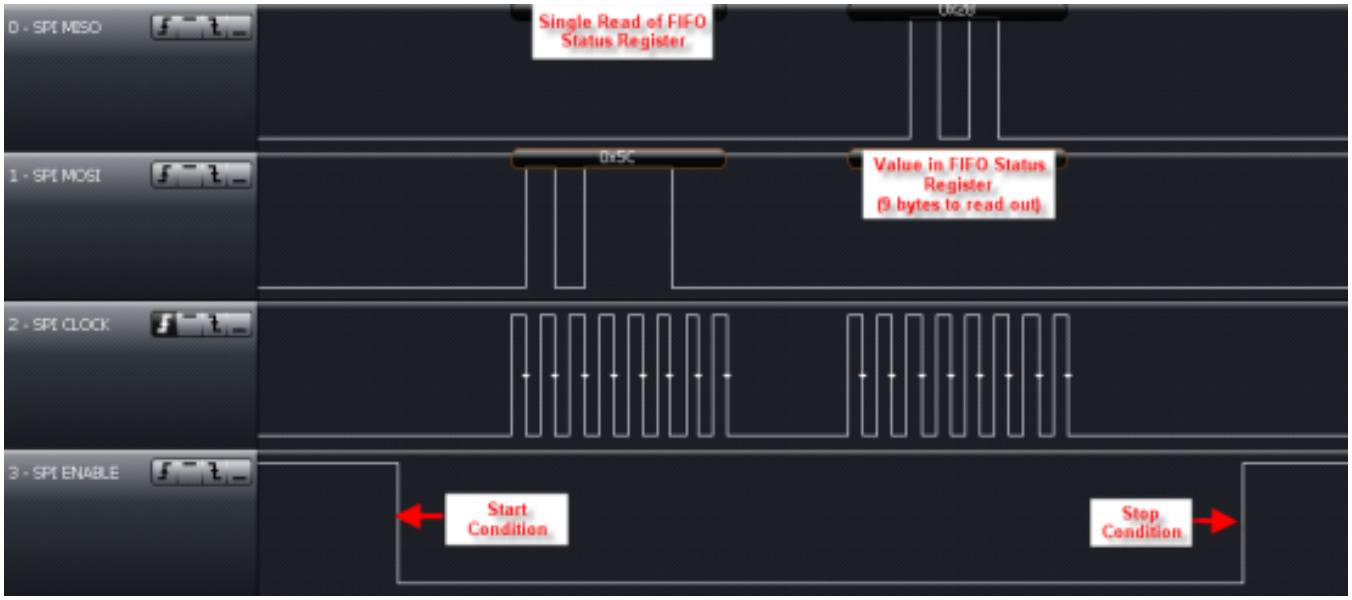

图 6-13. Example of Checking the FIFO Status Register Using SPI With SS

6.10.2 Parallel Interface Mode

In parallel mode, the start condition is generated on the rising edge of the I/O_7 pin while the CLK is high.

This is used to reset the interface logic. 图 6-14, 图 6-15, and 图 6-16 show the sequence of the data, with an 8-bit address word first, followed by data.

Communication is ended by:

- The StopSmpl condition, where a falling edge on the I/O_7 pin is expected while CLK is high.
- The StopCont condition, where the I/O_7 pin must have a successive rising and falling edge while CLK is low to reset the parallel interface and be ready for the new communication sequence.
- The *StopSmpl* condition is also used to terminate the direct mode.

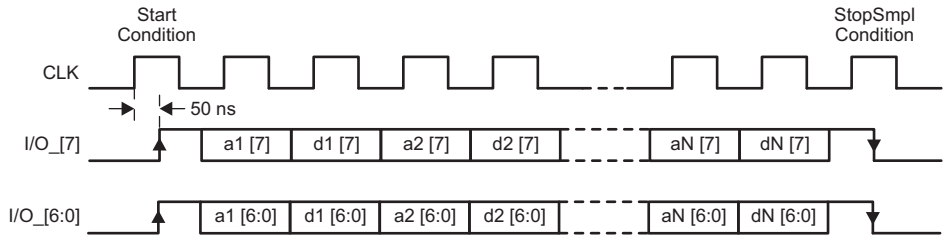

图 6-14. Parallel Interface Communication With Simple Stop Condition (StopSmpl)

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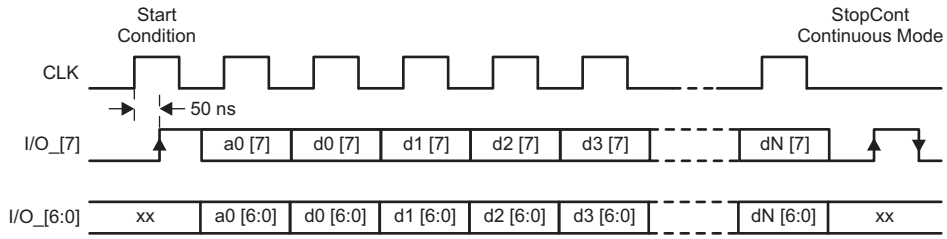

图 6-15. Parallel Interface Communication With Continuous Stop Condition (StopCont)

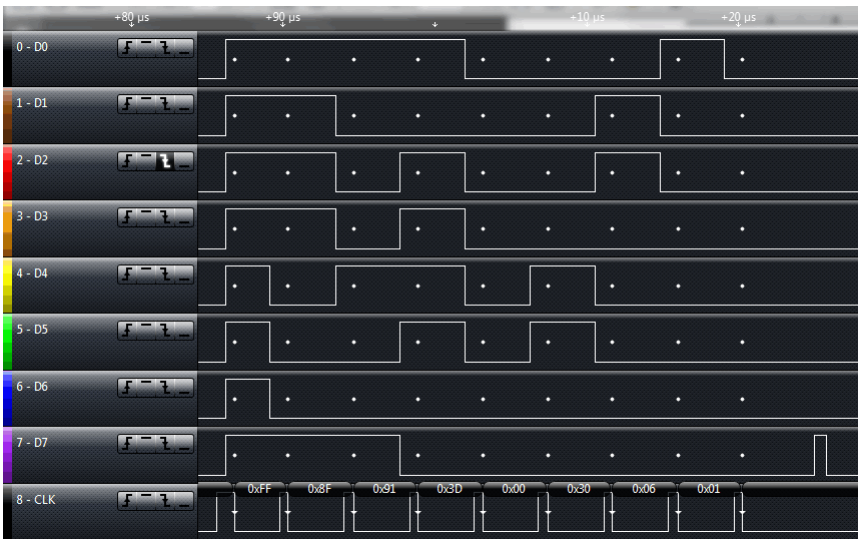

图 6-16. Example of Parallel Interface Communication With Continuous Stop Condition

6.10.3 Reception of Air Interface Data

At the start of a receive operation (when SOF is successfully detected), B6 is set in the IRQ Status register. An RX complete interrupt request is sent to the MCU at the end of the receive operation if the receive data string is shorter than or equal to the number of bytes configured in the Adjustable FIFO IRQ Levels register (0x14). An IRQ_FIFO interrupt request is sent to the MCU during the receive operation if the data string is greater than the level set in the Adjustable FIFO IRQ Levels register (0x14). After receiving an IRQ_FIFO or RX complete interrupt, the MCU must read the FIFO Status register (0x1C) to determine the number of bytes to be read from the FIFO. Next, the MCU must read the data in the FIFO. It is optional but recommended to read the FIFO Status register (0x1C) after reading FIFO data to determine if the receive is complete. In the case of an IRQ_FIFO, the MCU should expect either another IRQ_FIFO or RX complete interrupt. This is repeated until an RX complete interrupt is generated. The MCU receives the interrupt request, then checks to determine the reason for the interrupt by reading the IRQ Status register (0x0C), after which the MCU reads the data from the FIFO.

If the reader detects a receive error, the corresponding error flag is set (framing error, CRC error) in the IRQ Status register, indicating to the MCU that reception was not completed correctly.

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6.10.4 Data Transmission From MCU to TRF7970A

Before beginning data transmission, the FIFO should always be cleared with a reset command (0x0F). Data transmission is initiated with a selected command (see 节 6.14). The MCU then commands the reader to do a continuous write command (0x3D) starting from register 0x1D. Data written into register 0x1D is the TX Length Byte 1 (upper and middle nibbles), while the following byte in register 0x1E is the TX Length Byte 2 (lower nibble and broken byte length) (see 表 6-57 and 表 6-58) . Note that the TX byte length determines when the reader sends the end of frame (EOF) byte. After the TX length bytes are written, FIFO data is loaded in register 0x1F with byte storage locations 0 to 127. Data transmission begins automatically after the first byte is written into the FIFO. The loading of TX length bytes and the FIFO can be done with a continuous-write command, as the addresses are sequential.

At the start of transmission, the flag B7 (IRQ_TX) is set in the IRQ Status register, and at the end of the transmit operation, an interrupt is sent to inform the MCU that the task is complete.

6.10.5 Serial Interface Communication (SPI)

When an SPI interface is used, I/O pins I/O_2, I/O_1, and I/O_0 must be hard wired according to 表 6-10. On power up, the TRF7970A looks for the status of these pins and then enters into the corresponding mode.

The serial communications work in the same manner as the parallel communications with respect to the FIFO, except for the following condition. On receiving an IRQ from the reader, the MCU reads the TRF7970A IRQ Status register to determine how to service the reader. After this, the MCU must to do a dummy read to clear the reader's IRQ status register. The dummy read is required in SPI mode because the reader's IRQ status register needs an additional clock cycle to clear the register. This is not required in parallel mode because the additional clock cycle is included in the Stop condition. When first establishing communications with the TRF7970A, the SOFT_INIT (0x03) and IDLE (0x00) commands should be sent first from the MCU (see 表 6-19).

The procedure for a dummy read is as follows (see 图 6-17 and 图 6-18):

1. Start the dummy read:
    1. When using slave select (SS): set SS bit low.
    2. When not using SS: start condition is when Data Clock is high (see 表 6-10).
2. Send address word to IRQ status register (0x0C) with read and continuous address mode bits set to 1 (see 表 6-10).
3. Read 1 byte (8 bits) from IRQ status register (0x0C).
4. Dummy-read 1 byte from register 0x0D (collision position and interrupt mask).
5. Stop the dummy read:
    1. When using slave select (SS): set SS bit high.
    2. When not using SS: stop condition when Data Clock is high.

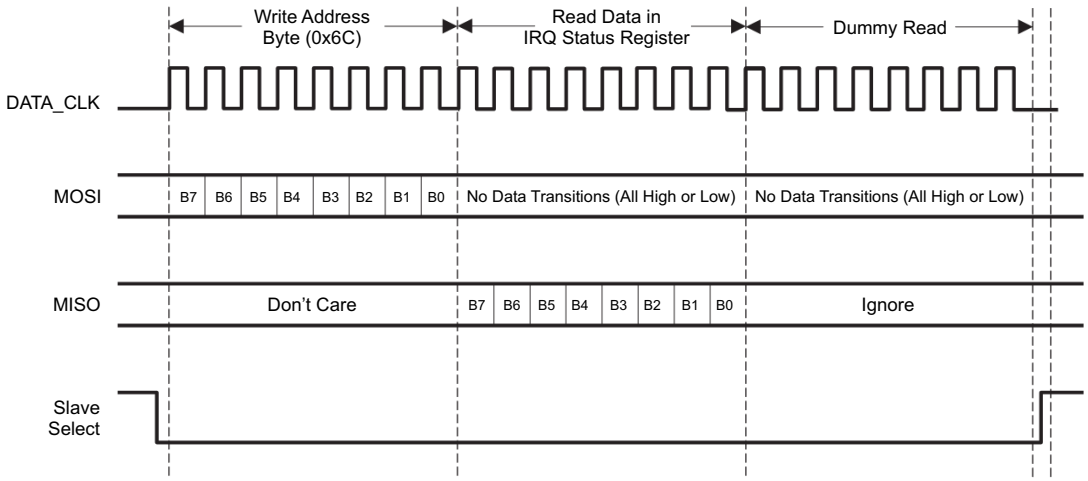

图 6-17. Procedure for Dummy Read

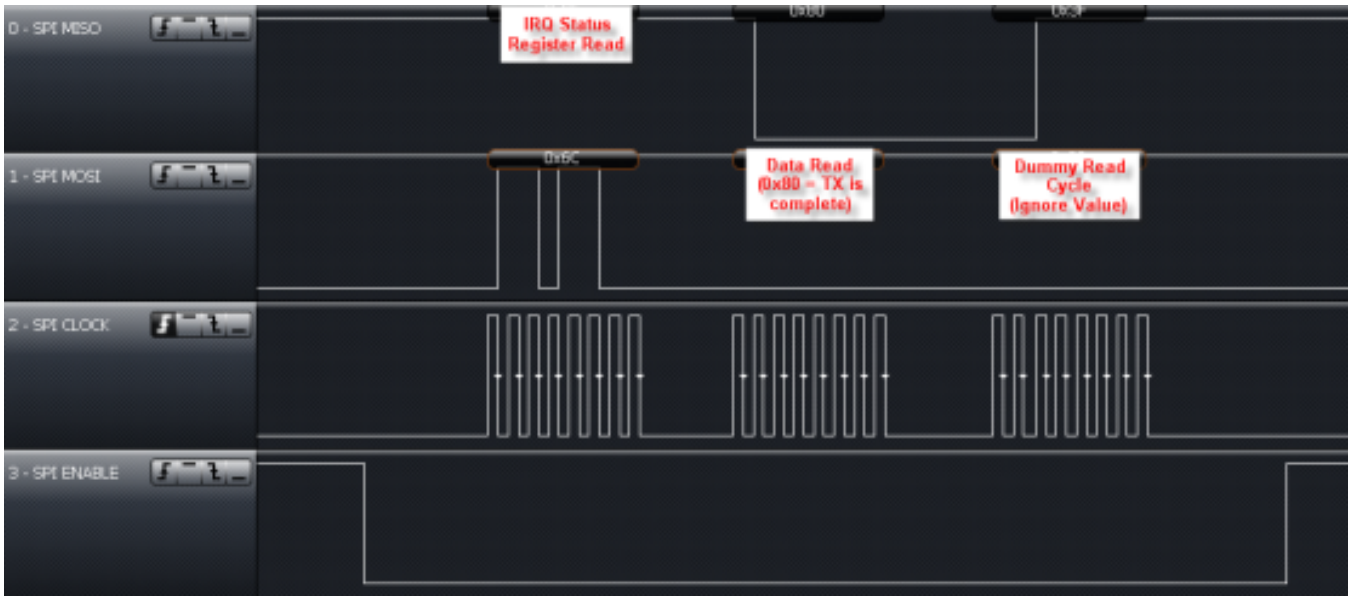

图 6-18. Example of Dummy Read Using SPI With SS

6.10.5.1 Serial Interface Mode With Slave Select (SS)

The serial interface is in reset while the Slave Select signal is high. Serial data in (MOSI) changes on the rising edge, and is validated in the reader on the falling edge, as shown in 图 6-19. Communication is terminated when the Slave Select signal goes high.

All words must be 8 bits long with the MSB transmitted first.

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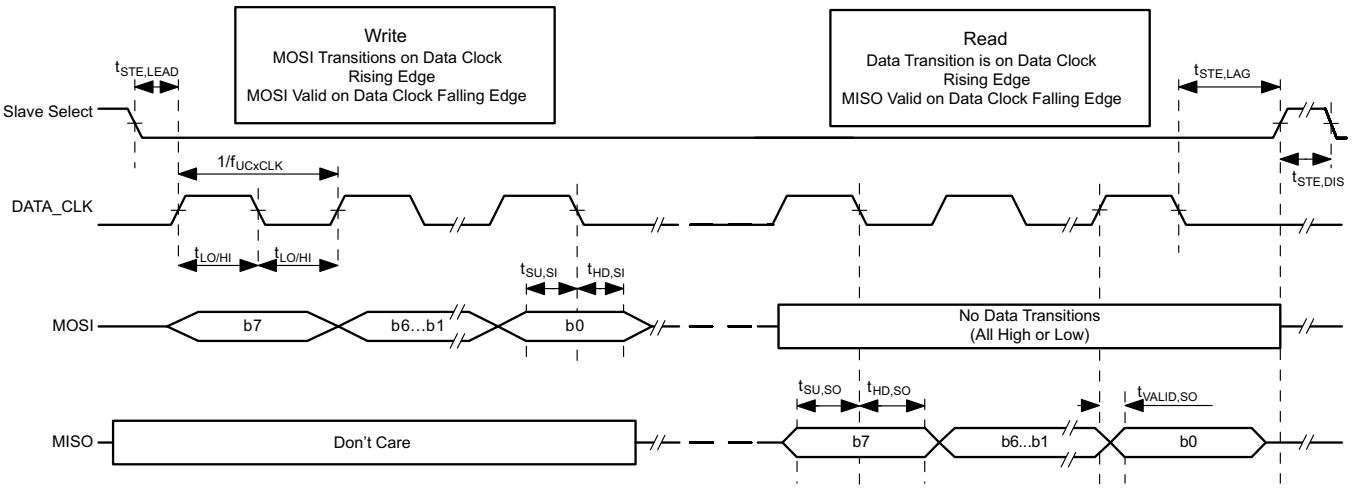

图 6-19. SPI With Slave Select Timing Diagram

The read command is sent out on the MOSI pin, MSB first, in the first eight clock cycles. MOSI data changes on the rising edge, and is validated in the reader on the falling edge, as shown in 图 6-19. During the write cycle, the serial data out (MISO) is not valid. After the last read command bit (B0) is validated at the eighth falling edge of SCLK, valid data can be read on the MISO pin at the falling edge of SCLK. It takes eight clock edges to read out the full byte (MSB first). See Section 5.4 for electrical specifications related to 图 6-19.

图 6-20 and 图 6-21 show the continuous read operation.

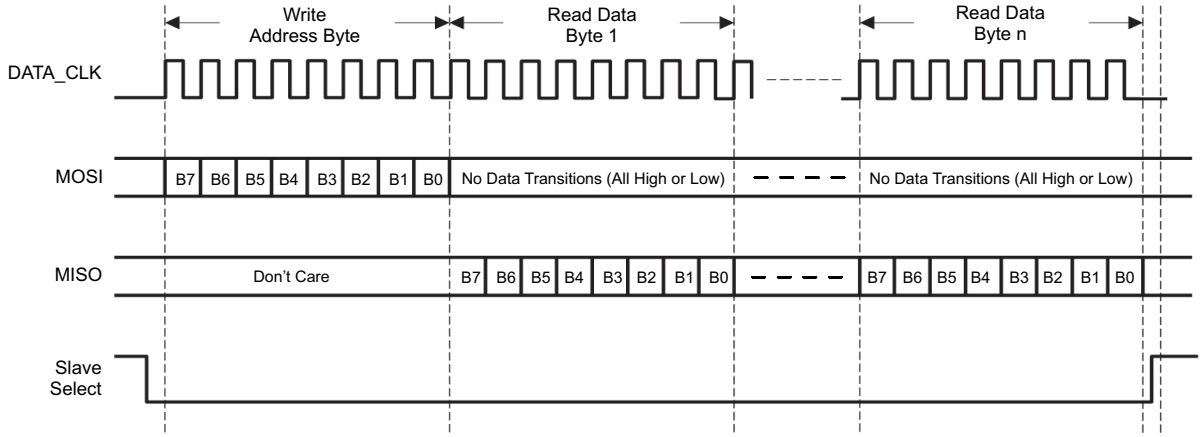

图 6-20. Continuous Read Operation Using SPI With Slave Select

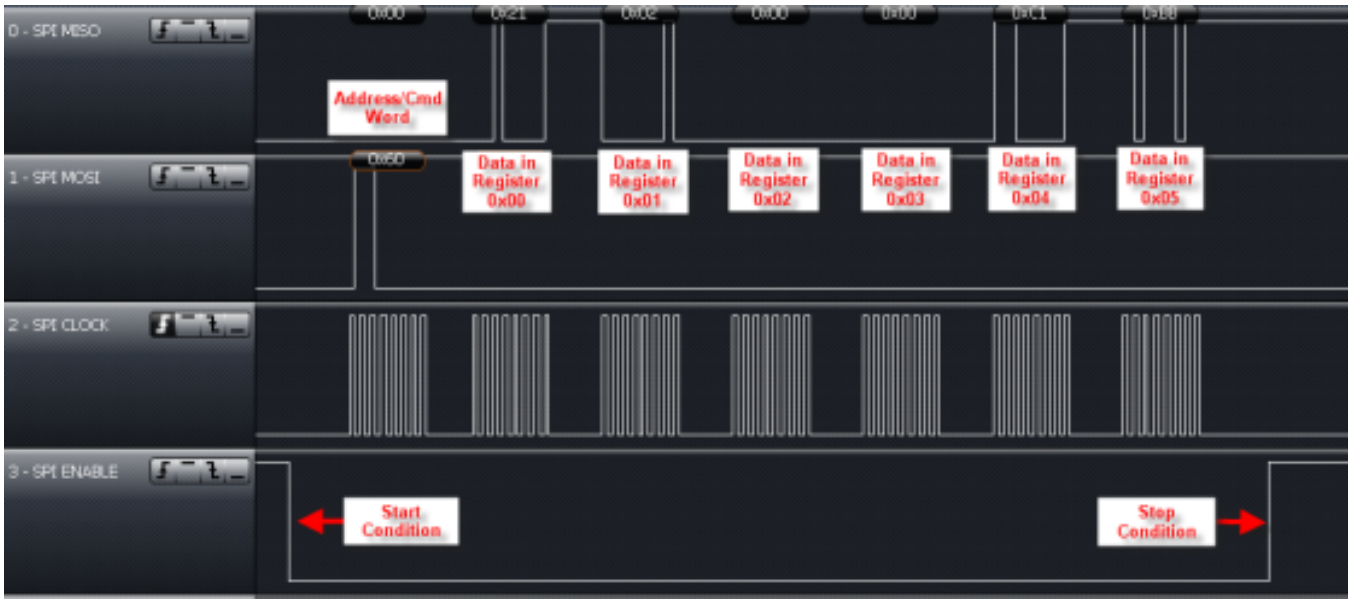

图 6-21. Continuous Read of Registers 0x00 to 0x05 Using SPI With SS

图 6-22 shows an example of performing a single slot inventory command. Reader registers (in this example) are configured for 5 VDC in and default operation.

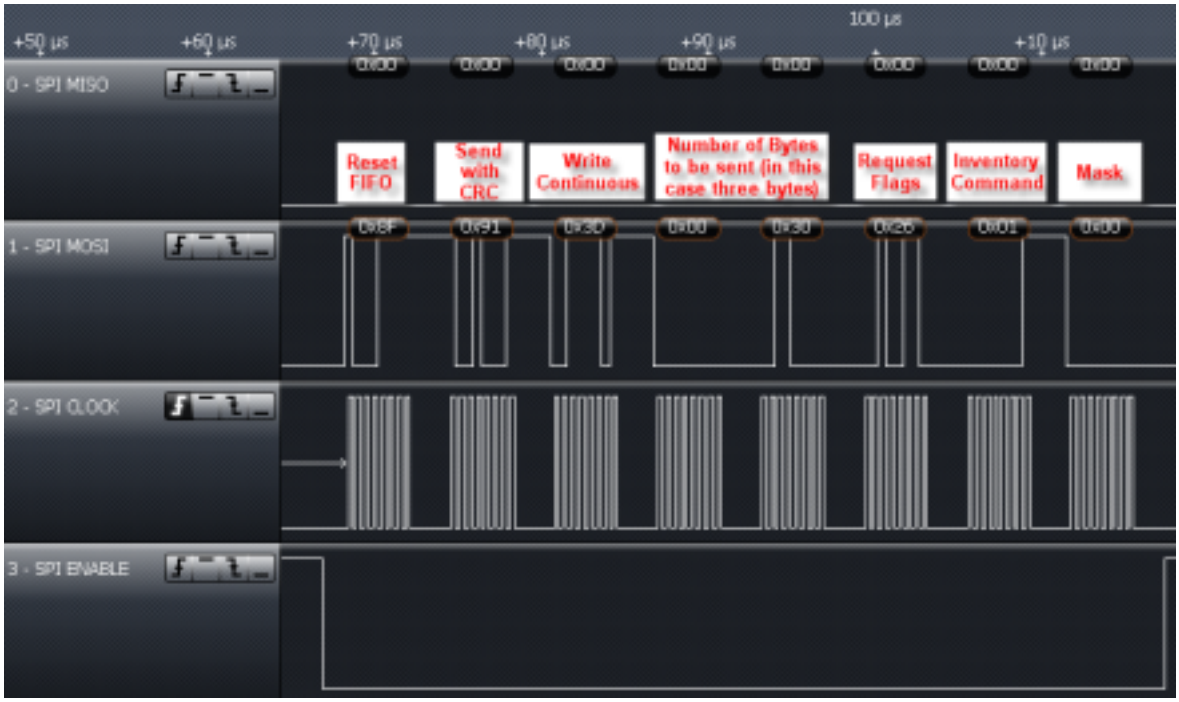

图 6-22. Inventory Command Sent From MCU to TRF7970A

The TRF7970A takes these bytes from the MCU and then send out Request Flags, Inventory Command, and Mask over the air to the ISO/IEC 15693 transponder. After these three bytes have been transmitted, an interrupt occurs to indicate back to the reader that the transmission has been completed. In the example in 图 6-23, this IRQ occurs approximately 1.6 ms after the SS line goes high after the Inventory command is sent out.

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图 6-23. IRQ After Inventory Command

The IRQ status register read (0x6C) yields 0x80, which indicates that TX is indeed complete. This is followed by a dummy clock. Then, if a tag is in the field and no error is detected by the reader, a second interrupt is expected and occurs (in this example) approximately 4 ms after first IRQ is read and cleared.

In the continuation of the example (see 图 6-24), the IRQ Status Register is read using method previously recommended, followed by a single read of the FIFO Status register, which indicates that there are 10 bytes to be read out.

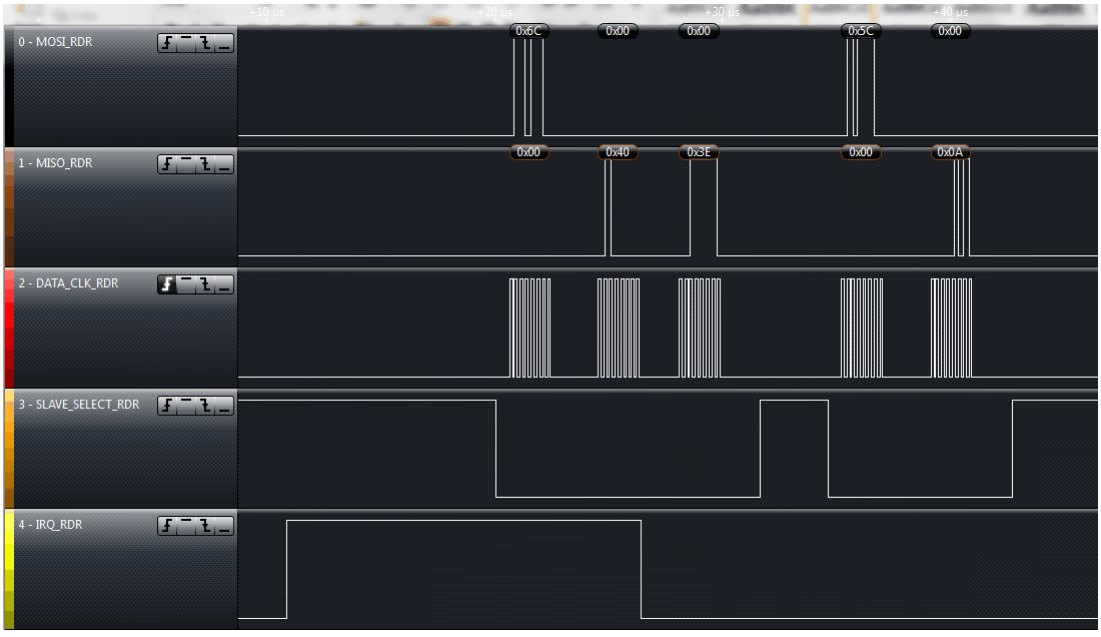

图 6-24. Read IRQ Status Register After Inventory Command

This is then followed by a continuous read of the FIFO (see 图 6-25). The first byte is (and should be) 0x00 for no error. The next byte is the DSFID (usually shipped by manufacturer as 0x00), then the UID, shown here up to the next most significant byte, the MFG code [shown as 0x07 (TI silicon)].

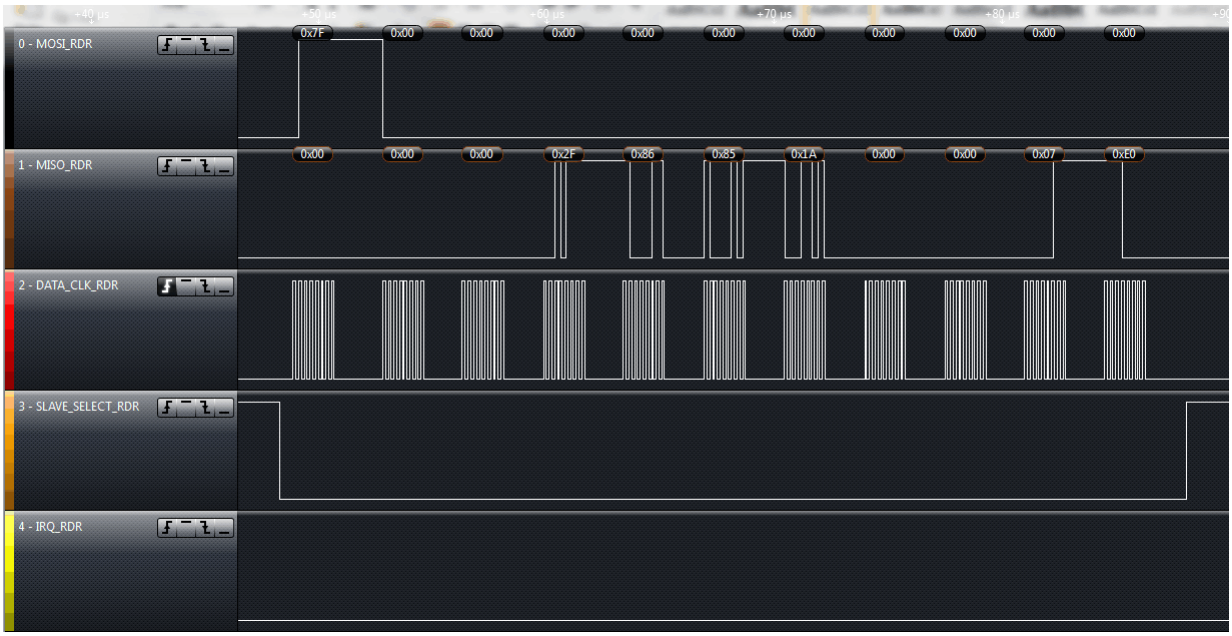

图 6-25. Continuous Read of FIFO After Inventory Command

TI recommends resetting the FIFO after receiving data. Additionally, the RSSI value of the tag can be read out at this point. In the example in 图 6-26, the transponder is very close to the antenna, so value of 0x7F is recovered.

图 6-26. Reset FIFO and Read RSSI

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6.10.6 Direct Mode

Direct mode allows the user to configure the reader in one of two ways. Direct mode 0 (bit 6 = 0, as defined in ISO Control register) allows the user to use only the front-end functions of the reader, bypassing the protocol implementation in the reader. For transmit functions, the user has direct access to the transmit modulator through the MOD pin (pin 14). On the receive side, the user has direct access to the subcarrier signal (digitized RF envelope signal) on I/O_6 (pin 23).

Direct mode 1 (bit 6 = 1, as defined in ISO Control register) uses the subcarrier signal decoder of the selected protocol (as defined in ISO Control register). This means that the receive output is not the subcarrier signal but the decoded serial bit stream and bit clock signals. The serial data is available on I/O_6 (pin 23) and the bit clock is available on I/O_5 (pin 22). The transmit side is identical; the user has direct control over the RF modulation through the MOD input. This mode is provided so that the user can implement a protocol that has the same bit coding as one of the protocols implemented in the reader, but needs a different framing format.

To select direct mode, the user must first choose which direct mode to enter by writing B6 in the ISO Control register. This bit determines if the receive output is the direct subcarrier signal (B6 = 0) or the serial data of the selected decoder. If B6 = 1, then the user must also define which protocol should be used for bit decoding by writing the appropriate setting in the ISO Control register.

The reader actually enters the direct mode when B6 (direct) is set to 1 in the chip status control register. Direct mode starts immediately. The write command should not be terminated with a stop condition (see communication protocol), because the stop condition terminates the direct mode and clears B6. This is necessary as the direct mode uses one or two I/O pins (I/O_6, I/O_5). Normal parallel communication is not possible in direct mode. Sending a stop condition terminates direct mode.

注

An additional direct mode known as special direct mode can be used to communicate with certain tags not compliant with ISO standards. For full details on how to use this feature, see *Using Special Direct Mode With the TRF7970A*.

图 6-27 shows the different configurations available in direct mode.

- In mode 0, the reader is used as an AFE only, and protocol handling is bypassed.
- In mode 1, framing is not done, but SOF and EOF are present. This allows for a user-selectable framing level based on an existing ISO standard.
- In mode 2, data is ISO-standard formatted. SOF, EOF, and error checking are removed, so the microprocessor receives only bytes of raw data through a 127-byte FIFO.

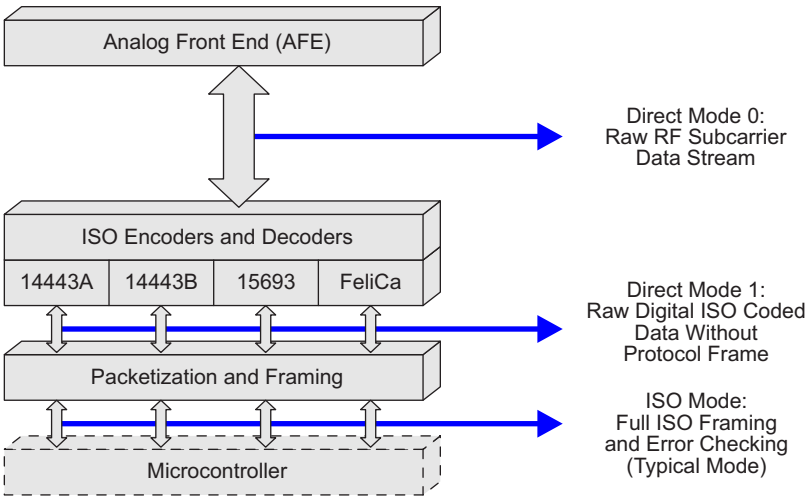

图 6-27. User-Configurable Modes

The steps to enter direct mode are listed below, using SPI with SS communication method only as one example, as direct modes are also possible with parallel and SPI without SS. The must enter direct mode 0 to accommodate card type communications that are not compliant with ISO standards. Direct mode can be entered at any time, so if a card type started with ISO standard communications, then deviated from the standard after being identified and selected, the ability to go into direct mode 0 is very useful.

Step 1: Configure Pins I/O_0 to I/O_2 for SPI with SS

Step 2: Set Pin 12 of the TRF7970A (ASK/OOK pin) to 0 for ASK or 1 for OOK

Step 3: Program the TRF7970A registers

The following registers must be explicitly set before going into the direct mode.

1. ISO Control register (0x01) to the appropriate standard
   - 0x02 for ISO/IEC 15693 High Data Rate
   - 0x08 for ISO/IEC 14443 A (106 kbps)
   - 0x1A for FeliCa 212 kbps
   - 0x1B for FeliCa 424 kbps
2. Modulator and SYS_CLK register (0x09) to the appropriate clock speed and modulation
   - 0x21 for 6.78 MHz Clock and OOK (100%) modulation
   - 0x20 for 6.78 MHz Clock and ASK 10% modulation
   - 0x22 for 6.78 MHz Clock and ASK 7% modulation
   - 0x23 for 6.78 MHz Clock and ASK 8.5% modulation
   - 0x24 for 6.78 MHz Clock and ASK 13% modulation
   - 0x25 for 6.78 MHz Clock and ASK 16% modulation
     (See register 0x09 definition for all other possible values)

Example register setting for ISO/IEC 14443 A at 106 kbps:

- ISO Control register (0x01) to 0x08
- RX No Response Wait Time register (0x07) to 0x0E
- RX Wait Time register (0x08) to 0x07
- Modulator control register (0x09) to 0x21 (or any custom modulation)
- RX Special Settings register (0x0A) to 0x20

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Step 4: Entering Direct Mode 0

The following registers must be programmed to enter direct mode 0:

1. Set bit B6 of the Modulator and SYS_CLK Control register (0x09) to 1.
2. Set bit B6 of the ISO Control (Register 01) to 0 for direct mode 0 (default its 0)
3. Set bit B6 of the Chip Status Control register (0x00) to 1 to enter direct mode
4. Send extra eight clock cycles (see 图 6-28, this step is TRF7970A specific)

注

- It is important that the last write is not terminated with a stop condition. For SPI, this means that Slave Select (I/O_4) stays low.
- Sending a Stop condition terminates the direct mode and clears bit B6 in the Chip Status Control register (0x00).

注

Access to Registers, FIFO, and IRQ is not available during direct mode 0.

The reader enters the direct mode 0 when bit 6 of the Chip Status Control register (0x00) is set to a 1 and stays in direct mode 0 until a stop condition is sent from the microcontroller.

注

The write command should not be terminated with a stop condition (for example, in SPI mode this is done by bringing the Slave Select line high after the register write), because the stop condition terminates the direct mode and clears bit 6 of the Chip Status Control register (0x00), making it a 0.

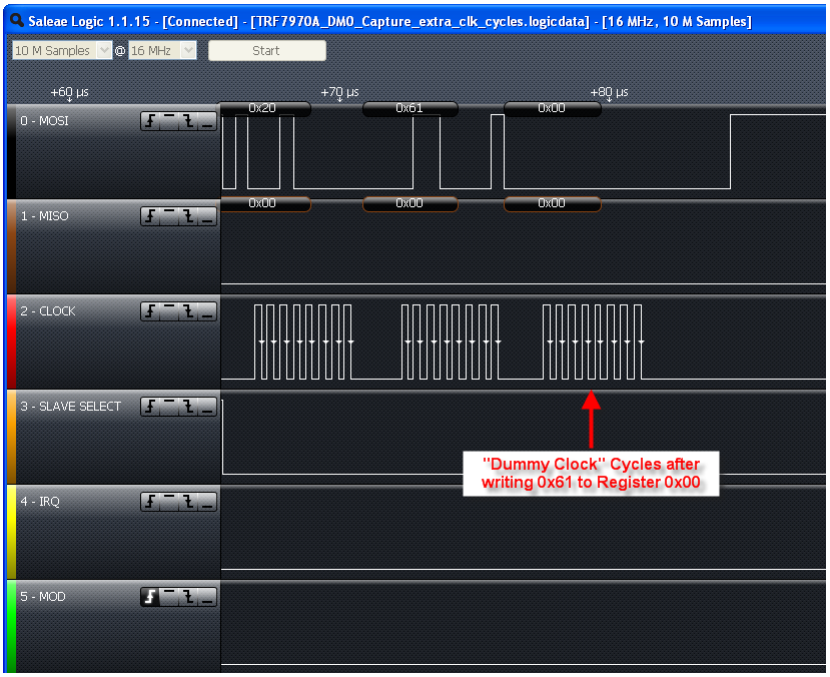

图 6-28. Entering Direct Mode 0

Step 5: Transmit Data Using Direct Mode

The application now has direct control over the RF modulation through the MOD input (see 图 6-29).

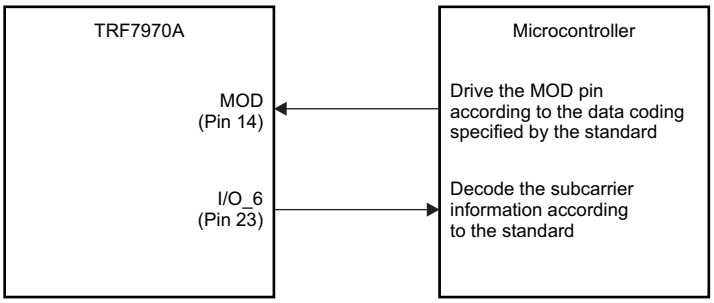

图 6-29. Direct Control Signals

The microcontroller is responsible for generating data according to the coding specified by the particular standard. The microcontroller must generate SOF, EOF, Data, and CRC. In direct mode, the FIFO is not used and no IRQs are generated. See the applicable ISO standard to understand bit and frame definitions. 图 6-30 shows an example of what the developer sees when using DM0 in an actual application. This figure clearly shows the relationship between the MOD pin being controlled by the MCU and the resulting modulated 13.56-MHz carrier signal.

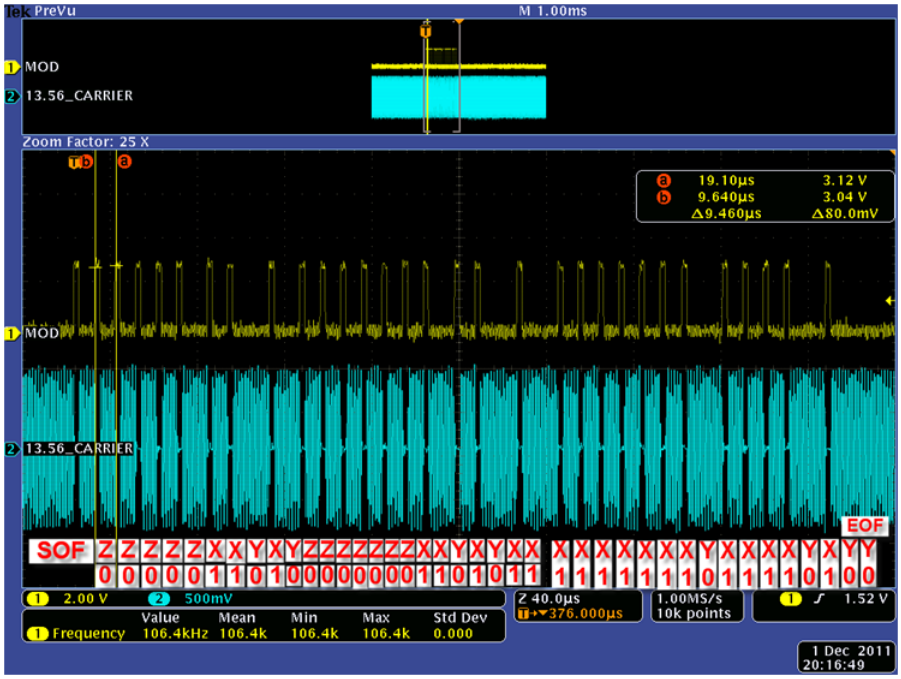

图 6-30. TX Sequence Out in DM0

Step 6: Receive Data Using Direct Mode

After the TX operation is complete, the tag responds to the request and the subcarrier data is available on pin I/O_6. The microcontroller needs to decode the subcarrier signal according to the standard. This includes decoding the SOF, data bits, CRC, and EOF. The CRC then needs to be checked to verify data integrity. The receive data bytes must be buffered locally.

As an example of the receive data bits and framing level according to the ISO/IEC 14443 A standard is shown in 图 6-31 (taken from ISO/IEC 14443 specification and TRF7970A air interface).

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- 128/fc = 9.435 µs = t_b (106-kbps data rate)
- 64/fc = 4.719 µs = t_x time
- 32/fc = 2.359 µs = t_1 time

Table 7 — Parameters for sequences

Parameter	Bit rate			
	fc/128	fc/64	fc/32	fc/16
t_b	128/fc	64/fc	32/fc	16/fc
t_x	64/fc	32/fc	16/fc	8/fc
t_1	see t_1 of Table 3	see t_1 of Table 5		

Figure 10 together with the timing parameters in Table 7 illustrate sequences X, Y and Z.

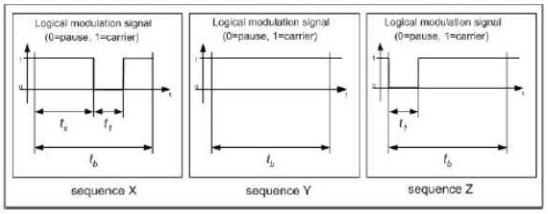


Figure 10 — Sequences for Type A communication PCD to PICC

The above sequences shall be used to code the following information:

— logic "1": sequence X,

— logic "0": sequence Y with the following two exceptions:

i) If there are two or more contiguous "0"s, sequence Z shall be used from the second "0" on,

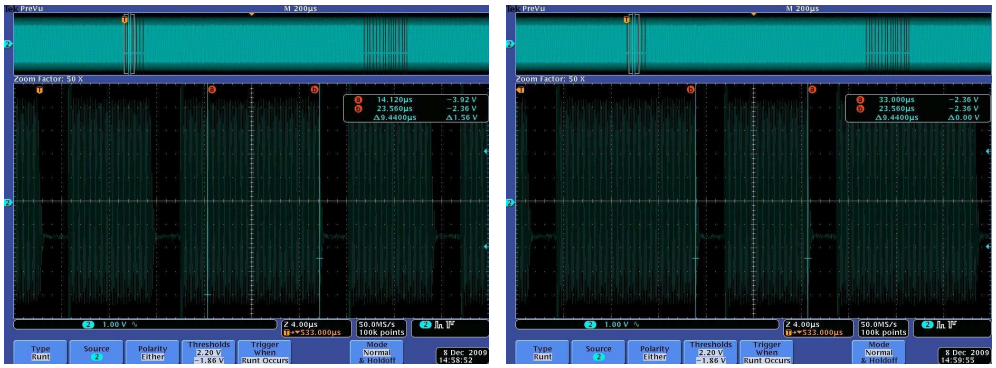
ii) If the first bit after a "start of frame" is "0", sequence Z shall be used to represent this and any "0"s which follow directly thereafter.

— start of communication: sequence Z,

— end of communication: logic "0" followed by sequence Y,

— no information: at least two sequences Y.

t_b = 9.44 µs | t_x = 4.72 µs | t_1 = 2.48 µs



Sequence Y = Carrier for 9.44 µs

Sequence Z = Pause for 2 to 3 µs, Carrier for Remainder of 9.44 µs

图 6-31. Receive Data Bits and Framing Level

图 6-32 shows an example of what the developer should expect on the I/O_6 line during the RX process while in direct mode 0.

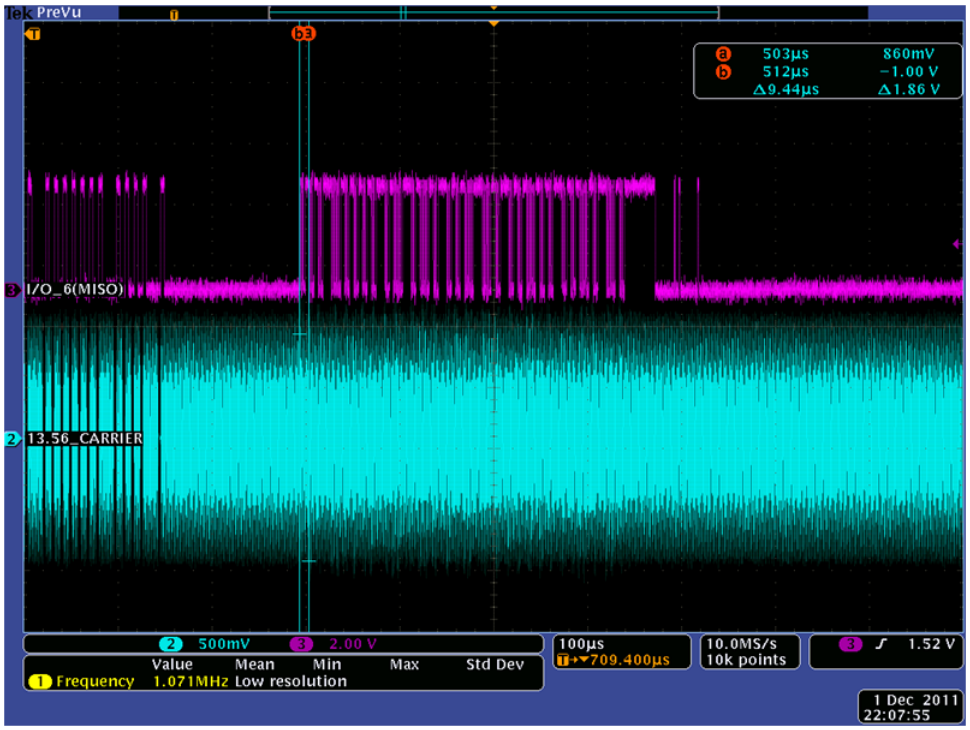


图 6-32. RX Sequence on I/O_6 in DM0 (Analog Capture)

Step 7: Terminating Direct Mode 0

After the EOF is received, data transmission is over, and direct mode 0 can be terminated by sending a Stop Condition (in the case of SPI, make the Slave Select go high). The TRF7970A is returned to default state.

6.11 TRF7970A Initialization

To properly initialize the TRF7970A, perform these steps:

1. Raise the EN, EN2, and SS lines at the correct intervals after power up (for timing diagrams, see 图 6-3 and 图 6-4).
2. Issue a Software Initialization direct command (0x03), followed by an Idle direct command (0x00) to soft reset the TRF7970A.

注

表 6-21 lists the initial register settings for the TRF7970A after the Software Initialization command.

---

3. Delay 1 ms to allow the TRF7970A to fully process the soft reset.
4. Issue a Reset FIFO direct command (0x0F).
5. Write the Modulator and SYS_CLK Control register (0x09) with the appropriate application-specific setting for the crystal and system clock settings.
6. (Optional) Write the Regulator and I/O Control register (0x0B) with the appropriate application-specific setting.
7. Write the NFC Target Detection Level register (0x18) with the value of 0x00. For details on this requirement, see the *TRF7970A Silicon Errata*.

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6.12 Special Direct Mode for Improved MIFARE™ Compatibility

See *Using Special Direct Mode With the TRF7970A*.

6.13 NFC Modes

6.13.1 Target

When used as the NFC target, the chip is typically in a power down or standby mode. If EN2 = H, the chip keeps the supply system on. If EN2 = L and EN = L the chip is in complete power down. To operate as NFC target or card emulator, the MCU must load a value different from zero (0) in Target Detection Level register (b0-b2) which enables the RF measurement system (supplied by VEXT, so it can operate also during complete power down and consumes only 3.5 µA). The RF measurement constantly monitors the RF signal on the antenna input. When the RF level on the antenna input exceeds the level defined in the in Target Detection Level register, the chip is automatically activated (EN is internal forced high). The typical RF value that causes power-up for each value of B0 to B2 and the function of Target Detection Level register is listed in 表 6-15.

NFC Target Detection Level Register (0x18) – defines level for RF level for wake-up and gives information of NFCID size. This register is directly supplied by VEXT to ensure data retention during complete power down.

表 6-15. NFC Target Detection Level Register

BIT	SIGNAL NAME	FUNCTION	COMMENTS
B7	Id_s1	NFCID1 size used in 106 kbps passive target SDD	
B6	Id_s0		
B5	Sdd_en	1 = Enables internal SDD protocol	Automatic SDD using internal state machine and ID stored in NFCID Number register(1)
B4		N/A	
B3	Hi_rf	Extended range for RF measurements	
B2	Rfdet_h2	RF field level required for system wake-up. If all bits are 0, the RF level detection is switched off.	Comparator output is displayed in NFC Target Protocol register B7 (rf_h)
B1	Rfdet_h1		
B0	Rfdet_h0		

(1) See the *TRF7970A Silicon Errata* for details on automatic SDD dependencies.

Default: reset to 00 at POR on VEXT (not on POR based on V_{DD_X}), not reset at EN = 0

表 6-16. Bits B0 to B3 of the NFC Target Detection Level Register

	B0 B1 B2	000	001	010	011	100	101	110	111
B3 = 0	RF Vpp	Not active	480 mV	350 mV	250 mV	220 mV	190 mV	180 mV	170 mV
B3 = 1	RF Vpp	Not active	1500 mV	700 mV	500 mV	450 mV	400 mV	320 mV	280 mV

When the voltage supply system and the oscillator are started and is stable, the osc_ok goes high (B6 of RSSI Level and Oscillator Status register) and IRQ is sent with bit B2 = 1 of IRQ register (field change). Bit B7 NFC Target Protocol in register directly displays the status of RF level detection (running constantly also during normal operation). This informs the MCU that the chip should start operation as an NFC TARGET device.

When the first command from the INITIATOR is received another IRQ sent with B6 (RX start) set in IRQ register. The MCU must set EN = H (confirm the power-up) in the time between the two IRQs as the internal power-up ends after the second IRQ. The type and coding of the first initiator (or reader in the case of a card emulator) command define the communication protocol type which the target must use. So the communication protocol type is available in the NFC Target Protocol register immediately after receiving the first command. The coding of the NFC Target Protocol register is described next.

NFC Target Protocol Register (0x19) – displays the bit rate and protocol type (active or passive) transmitted by initiator in the first command. It also displays the comparator outputs of both RF level detectors.

表 6-17. NFC Target Protocol Register

BIT	NAME	FUNCTION	DESCRIPTION
B7	Rf_h	1 = RF level is above the set wake-up level	The wake-up level is defined by bits b0-b3 of NFC Target Detection Level register
B6	Rf_l	1 = RF level is above the RF collision avoidance level	The collision avoidance level is defined by bits b0-b2 of NFC Low Field Detection Level register
B5		N/A	
B4	FeliCa	1 = FeliCa type 0 = ISO/IEC 14443 A type	The first initiator command had physical level coding like FeliCa or like ISO/IEC 14443 A
B3	Pas106	Passive target 106 kbps or card emulation	The first initiator/reader command was SENS_REQ or ALL_REQ
B2	Pas14443B	Card emulation ISO/IEC 14443 B	The first reader command was of ISO/IEC 14443 B type
B1	Nfcbr1	Bit rate of first received command	00 = N/A 01 = 106 kbps 10 = 212 kbps 11 = 424 kbps
B0	Nfcbr0		

Default: reset to 00 at POR and EN = L. B0 to B4 are automatically reset after MCU read operation. B6 and B7 continuously display the RF level comparator outputs.

Based on the first command from INITIATOR following actions are taken:

- If the first command is SENS_REQ or ALL_REQ, the TARGET must enter the SDD protocol for 106 kbps passive communication. If bit B5 in NFC Target Detection Level register is not set, the MCU handles the SDD and the command received is send to FIFO. If the RF field is turned off (B7 in the NFC Target Protocol register goes low) at any time, the system sends an IRQ to the MCU with bit B2 (RF field change) in the IRQ register set high. This informs the MCU that the procedure was aborted and the system must be reset. The clock extractor is automatically activated in this mode.
- If the command is SENS_REQ or ALL_REQ and the card emulation bit in the ISO Control register is set, the system emulates an ISO/IEC 14443 A card. The procedure does not differ from the one previously described for a passive target at 106 kbps. The clock extractor is automatically activated in this mode.
- If the first command is a SENSF_REQ, the system becomes a TARGET in passive communication using 212 kbps or 424 kbps. The SDD is relatively simple and is handled by the MCU directly.
- If the first command is ATR_REQ, the system operates as an active TARGET using the same communication speed and bit coding as used by the INITIATOR. Again, all of the replies are handled by the MCU. The MCU should check for collision avoidance by checking the external RSSI as described in 节 6.5.1.2. When no RF field is detected from the external RSSI result, then the MCU can begin the process to send the reply.
- If the first command is coded as ISO/IEC 14443 B and the card emulation bit is set in the ISO Control register, the system enters ISO/IEC 14443 B emulator mode. The anticollision must be handled by the MCU, and the chip provides all physical level coding, decoding, and framing for this protocol.

表 6-18 shows the function of the IRQ Status register in NFC and card emulation. This register is preset to 0 at POR = H or EN = L and at each write to ISO Control. It is also automatically reset at the end of read phase. The reset also removes the IRQ flag.

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表 6-18. IRQ Status Register (0x0C) for NFC and Card Emulation Operation (1)

BIT	NAME	FUNCTION	DESCRIPTION
B7	Irq_tx	IRQ set due to end of TX	Signals that TX is in progress. The flag is set at the start of TX but the interrupt request (IRQ = 1) is sent when TX is finished.
B6	Irg_srx	IRQ set due to RX start	Signals that RX SOF was received and RX is in progress. The flag is set at the start of RX but the interrupt request (IRQ = 1) is sent when RX is finished.
B5	Irq_fifo	Signals the FIFO level	Signals FIFO high or low as set in the Adjustable FIFO IRQ Levels (0x14) register
B4	Irq_err1	CRC error	Indicates receive CRC error only if B7 (no RX CRC) of ISO Control register is set to 0.
B3	Irq_err2	Parity error	Indicates parity error for ISO/IEC 14443 A
B2	Irq_err3	Byte framing or EOF error	Indicates framing error
B1	Irq_col	Collision error	Collision error for ISO/IEC 14443 A and ISO/IEC 15693 single subcarrier. Bit is set if more than 6 or 7 (as defined in register 0x10) are detected inside 1 bit period of ISO/IEC 14443 A 106 kbps. Collision error bit can also be triggered by external noise.
B0	Irq_noresp	No-response time interrupt	No response within the "No-response time" defined in RX No-response Wait Time register (0x07). Signals the MCU that next slot command can be sent. Only for ISO/IEC 15693.

(1) Displays the cause of IRQ and TX/RX status

6.13.2 Initiator

The chip is fully controlled by the MCU as in RFID reader operation. The MCU activates the chip and writes the mode selection in the ISO Control register. The normal transmit and receive procedure (through the FIFO) are used to communicate with the TARGET device as described in 节 6.10.

6.14 Direct Commands from MCU to Reader

6.14.1 Command Codes

表 6-19 summarizes the command codes.

表 6-19. Address and Command Word Bit Distribution

COMMAND CODE	COMMAND	COMMENTS
0x00	Idle	
0x03	Software initialization	Same as Power on Reset
0x04	Perform RF collision avoidance	Does not function as expected. See the *TRF7970A Errata* for details.
0x05	Perform response RF collision avoidance	Does not function as expected. See the *TRF7970A Errata* for details.
0x06	Perform response RF collision avoidance (n = 0)	Does not function as expected. See the *TRF7970A Errata* for details.
0x0F	Reset FIFO	
0x10	Transmission without CRC	
0x11	Transmission with CRC	
0x12	Delayed transmission without CRC	
0x13	Delayed transmission with CRC	
0x14	End of frame and transmit next time slot	Used for ISO/IEC 15693 only
0x16	Block receiver	
0x17	Enable receiver	
0x18	Test internal RF (RSSI at RX input with TX off)	

表 6-19. Address and Command Word Bit Distribution (continued)

COMMAND CODE	COMMAND	COMMENTS
0x19	Test external RF (RSSI at RX input with TX on)	

The command code values from 表 6-19 are substituted in 表 6-20, bits 0 through 4. Also, the most-significant bit (MSB) in 表 6-20 must be set to 1. (表 6-20 is same as 表 6-11, shown here again for easy reference).

表 6-20. Address and Command Word Bit Distribution

BIT	DESCRIPTION	BIT FUNCTION	ADDRESS	COMMAND
B7	Command control bit	0 = Address 1 = Command	0	1
B6	Read/Write	0 = Write 1 = Read	R/W	0
B5	Continuous address mode	1 = Continuous mode	R/W	0
B4	Address/Command bit 4		Adr 4	Cmd 4
B3	Address/Command bit 3		Adr 3	Cmd 3
B2	Address/Command bit 2		Adr 2	Cmd 2
B1	Address/Command bit 1		Adr 1	Cmd 1
B0	Address/Command bit 0		Adr 0	Cmd 0

The MSB determines if the word is to be used as a command or address. The last two columns of 表 6-20 show the function of each bit, depending on whether address or command is written. Command mode is used to enter a command resulting in reader action (initialize transmission, enable reader, and turn reader on or off).

6.14.1.1 Idle (0x00)

This command issues dummy clock cycles. In parallel mode, one cycle is issued. In SPI mode, eight cycles are issued. This command should be sent after a Software Initialization command to allow the command to finish operation.

6.14.1.2 Software Initialization (0x03)

This command starts a power-on reset. After sending this command, the register values change as shown in 表 6-21.

表 6-21. Register Values After Sending Software Initialization (0x03)

ADDRESS	REGISTER	VALUE
0x00	Chip status control	0x01
0x01	ISO control	0x21 (1)
0x02	ISO/IEC 14443 B TX options	0x00
0x03	ISO/IEC 14443 A high bit rate options	0x00
0x04	TX timer high byte control	0xC1 (1)
0x05	TX timer low byte control	0xC1 (1)
0x06	TX pulse length control	0x00
0x07	RX no response wait time	0x0E
0x08	RX wait time	0x07 (1)
0x09	Modulator and SYS_CLK control	0x91
0x0A	RX special setting	0x10 (1)

(1) Differs from default at POR

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表 6-21. Register Values After Sending Software Initialization (0x03) (continued)

ADDRESS	REGISTER	VALUE
0x0B	Regulator and I/O control	0x87
0x0C	IRQ status	0x00
0x0D	Collision position and interrupt mask	0x3E
0x0E	Collision position	0x00
0x0F	RSSI levels and oscillator status	0x40
0x10	Special function	0x00
0x11	Special function	0x00
0x12	RAM	0x00
0x13	RAM	0x00
0x14	Adjustable FIFO IRQ levels	0x00
0x15	Reserved	0x00
0x16	NFC low field detection level	0x00
0x18	NFC target detection level	0x00 (2)
0x19	NFC target protocol	0x00
0x1A	Test	0x00
0x1B	Test	0x00
0x1C	FIFO status	0x00

(2) Default value may not always be 0x00. See the *TRF7970A Errata* for details.

6.14.1.3 Initial RF Collision Avoidance (0x04)

See the *TRF7970A Errata*.

6.14.1.4 Response RF Collision Avoidance (0x05)

See the *TRF7970A Errata*.

6.14.1.5 Response RF Collision Avoidance (0x06, n = 0)

See the *TRF7970A Errata*.

6.14.1.6 Reset FIFO (0x0F)

The reset command clears the FIFO contents and FIFO Status register (0x1C). It also clears the register storing the collision error location (0x0E).

6.14.1.7 Transmission With CRC (0x11)

The transmission command must be sent first, followed by transmission length bytes, and FIFO data. The reader starts transmitting after the first byte is loaded into the FIFO. The CRC byte is included in the transmitted sequence.

6.14.1.8 Transmission Without CRC (0x10)

Same as 节 6.14.1.7 with CRC excluded.

6.14.1.9 Delayed Transmission With CRC (0x13)

The transmission command must be sent first, followed by the transmission length bytes, and FIFO data.

The reader transmission is triggered by the TX timer.

6.14.1.10 Delayed Transmission Without CRC (0x12)

Same as 节 6.14.1.9 with CRC excluded.

6.14.1.11 Transmit Next Time Slot (0x14)

When this command is received, the reader transmits the next slot command. The next slot sign is defined by the protocol selection. This is used by the ISO/IEC 15693 protocol.

6.14.1.12 Block Receiver (0x16)

The block receiver command puts the digital part of receiver (bit decoder and framer) in reset mode. This is useful in an extremely noisy environment, where the noise level could otherwise cause a constant switching of the subcarrier input of the digital part of the receiver. The receiver (if not in reset) would try to catch a SOF signal, and if the noise pattern matched the SOF pattern, an interrupt would be generated, falsely signaling the start of an RX operation. A constant flow of interrupt requests can be a problem for the external system (MCU), so the external system can stop this by putting the receive decoders in reset mode. The reset mode can be terminated in two ways. The external system can send the enable receiver command. The reset mode is also automatically terminated at the end of a TX operation. The receiver can stay in reset after end of TX if the RX wait time register (0x08) is set. In this case, the receiver is enabled at the end of the wait time following the transmit operation.

6.14.1.13 Enable Receiver (0x17)

This command clears the reset mode in the digital part of the receiver if the reset mode was entered by the block receiver command.

6.14.1.14 Test Internal RF (RSSI at RX Input With TX ON) (0x18)

The level of the RF carrier at RF_IN1 and RF_IN2 inputs is measured. Operating range between 300 mV_P and 2.1 V_P (step size is 300 mV). The two values are displayed in the RSSI Levels and Oscillator Status register (0x0F). The command is intended for diagnostic purposes to set correct RF_IN levels. Optimum RFIN input level is approximately 1.6 V_P or code 5 to 6. The nominal relationship between the RF peak level and RSSI code is shown in 表 6-22 and in 节 6.5.1.1.

注

If the command is executed immediately after power-up and before any communication with a tag is performed, the command must be preceded by Enable RX command. The Check RF commands require full operation, so the receiver must be activated by Enable RX or by a normal Tag communication for the Check RF command to work properly.

表 6-22. Test Internal RF Peak Level to RSSI Codes

RF_IN1 [mV_{PP}]	300	600	900	1200	1500	1800	2100
Decimal Code	1	2	3	4	5	6	7
Binary Code	001	010	011	001	101	011	111

6.14.1.15 Test External RF (RSSI at RX Input with TX OFF) (0x19)

This command can be used in active mode when the RF receiver is switched on but RF output is switched off. This means bit B1 = 1 in Chip Status Control Register. The level of RF signal received on the antenna is measured and displayed in the RSSI Levels and Oscillator Status register (0x0F). The relation between the 3 bit code and the external RF field strength [A/m] must be determinate by calculation or by experiments for each antenna type as the antenna Q and connection to the RF input influence the result. The nominal relation between the RF peak to peak voltage in the RF_IN1 input and RSSI code is shown in 表 6-23 and in 节 6.5.1.2.

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注

If the command is executed immediately after power-up and before any communication with a tag is performed, the command must be preceded by an Enable RX command. The Check RF commands require full operation, so the receiver must be activated by Enable RX or by a normal Tag communication for the Check RF command to work properly.

表 6-23. Test External RF Peak Level to RSSI Codes

RF_IN1 [mV_{PP}]	40	60	80	100	140	180	300
Decimal Code	1	2	3	4	5	6	7
Binary Code	001	010	011	001	101	011	111

6.15 Register Description

6.15.1 Register Preset

After power up and the EN pin low-to-high transition, the reader is in the default mode. The default configuration is ISO/IEC 15693, single subcarrier, high data rate, 1-out-of-4 operation. The low-level option registers (0x02 to 0x0B) are automatically set to adapt the circuitry optimally to the appropriate protocol parameters. When entering another protocol (by writing to the ISO Control register 0x01), the low-level option registers (0x02 to 0x0B) are automatically configured to the new protocol parameters. After selecting the protocol, it is possible to change some low-level register contents if needed. However, changing to another protocol and then back, reloads the default settings, and so then the custom settings must be reloaded.

The Clo0 and Clo1 register (0x09) bits, which define the microcontroller frequency available on the SYS_CLK pin, are the only 2 bits in the configuration registers that are not cleared during protocol selection.

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6.15.2 Register Overview

表 6-24 lists the registers.

表 6-24. Register Definitions

ADDRESS	REGISTER	READ/WRITE	SECTION
Main Control Registers			
0x00	Chip status control	R/W	节 6.15.3.1.1
0x01	ISO Control	R/W	节 6.15.3.1.2
Protocol Subsetting Registers			
0x02	ISO/IEC 14443 B TX options	R/W	节 6.15.3.2.1
0x03	ISO/IEC 14443 A high bit rate options	R/W	节 6.15.3.2.2
0x04	TX timer high byte control	R/W	节 6.15.3.2.3
0x05	TX timer low byte control	R/W	节 6.15.3.2.4
0x06	TX pulse length control	R/W	节 6.15.3.2.5
0x07	RX no response wait time	R/W	节 6.15.3.2.6
0x08	RX wait time	R/W	节 6.15.3.2.7
0x09	Modulator and SYS_CLK control	R/W	节 6.15.3.2.8
0x0A	RX special setting	R/W	节 6.15.3.2.9
0x0B	Regulator and I/O control	R/W	节 6.15.3.2.10
0x10	Special function register (preset 0x00)	R/W	节 6.15.3.3.4
0x11	Special function register (preset 0x00)	R/W	节 6.15.3.3.5
0x14	Adjustable FIFO IRQ levels	R/W	节 6.15.3.3.6
0x15	Reserved	R/W	
0x16	NFC low field level	R/W	节 6.15.3.3.7
0x17	NFCID1 number (up to 10 bytes wide)	W	节 6.15.3.3.8
0x18	NFC target detection level	R/W	节 6.15.3.3.9
0x19	NFC target protocol	R/W	节 6.15.3.3.10
Status Registers			
0x0C	IRQ status	R	节 6.15.3.3.1
0x0D	Collision position and interrupt mask register	R/W	节 6.15.3.3.2
0x0E	Collision position	R	节 6.15.3.3.2
0x0F	RSSI levels and oscillator status	R	节 6.15.3.3.3
RAM			
0x12	RAM	R/W	N/A
0x13	RAM	R/W	N/A
Test Registers			
0x1A	Test (preset 0x00)	R/W	节 6.15.3.4.1
0x1B	Test (preset 0x00)	R/W	节 6.15.3.4.2
FIFO Registers			
0x1C	FIFO status	R	节 6.15.3.5.1
0x1D	TX length byte 1	R/W	节 6.15.3.5.2
0x1E	TX length byte 2	R/W	节 6.15.3.5.2
0x1F	FIFO I/O register	R/W	N/A

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6.15.3 Detailed Register Description

6.15.3.1 Main Configuration Registers

6.15.3.1.1 Chip Status Control Register (0x00)

表 6-25 describes the Chip Status Control register.

表 6-25. Chip Status Control Register (0x00)

Function: Control of Power mode, RF on or off, Active or Passive mode, Direct mode			
Default: 0x01, preset at EN = L or POR = H			
Bit	**Name**	**Function**	**Description**
B7	stby	1 = Standby mode	Standby mode keeps all supply regulators and the 13.56-MHz SYS_CLK oscillator running. (Typical start-up time to full operation is 100 µs.)
		0 = Active mode	Active mode (default)
B6	direct	1 = Direct mode 0 or 1	Provides user direct access to AFE (direct mode 0) or allows user to add custom framing (direct mode 1). Bit 6 of the ISO Control register must be set by user before entering direct mode 0 or 1.
		0 = Direct I 2 (default)	Uses SPI or parallel communication with automatic framing and ISO decoders
B5	rf_on	1 = RF output active	Transmitter on, receivers on
		0 = RF output not active	Transmitter off
B4	rf_pwr	1 = Half output power	TX_OUT (pin 5) = 8-Ω output impedance P = 100 mW (20 dBm) at 5 V, P = 33 mW (+15 dBm) at 3.3 V
		0 = Full output power	TX_OUT (pin 5) = 4-Ω output impedance P = 200 mW (+23 dBm) at 5 V, P = 70 mW (+18 dBm) at 3.3 V
B3	pm_on	1 = Selects aux RX input	RX_IN2 input is used
		0 = Selects main RX input	RX_IN1 input is used
B2	Reserved		
B1	rec_on	1 = Receiver activated for external field measurement	Forced enabling of receiver and TX oscillator. Used for external field measurement.
		0 = Automatic enable	Allows enable of the receiver by bit 5 of this register (0x00)
B0	vrs5_3	1 = 5-V operation 0 = 3-V operation	Selects the V_{IN} voltage range

6.15.3.1.2 ISO Control Register (0x01)

表 6-26 describes the ISO Control register.

表 6-26. ISO Control Register (0x01)

Function: Controls the selection of ISO standard protocol, direct mode and receive CRC			
Default: 0x02 (ISO/IEC 15693 high bit rate, one subcarrier, 1 out of 4); it is preset at EN = L or POR = H			
Bit	**Name**	**Function**	**Description**
B7	rx_crc_n	CRC Receive selection	0 = RX CRC (CRC is present in the response) 1 = no RX CRC (CRC is not present in the response)(1)
B6	dir_mode	Direct mode type selection	0 = Direct Mode 0 1 = Direct mode 1
B5	rfid	RFID / Reserved	0 = RFID mode 1 = NFC or card emulation mode
B4	iso_4	RFID / NFC Target	RFID: See 表 6-27 for B0:B4 settings based on ISO protocol in application NFC: 0 = target 1 = initiator

(1) Only applicable to ISO/IEC 14443 A and ISO/IEC 15693

表 6-26. ISO Control Register (0x01) (continued)

B3	iso_3	RFID / NFC Mode	NFC: 0 = passive mode 1 = active mode
B2	iso_2	RFID / Card Emulation	NFC: 0 = NFC Normal Modes 1 = Card Emulation Mode
B1	iso_1	RFID / NFC bit rate	NFC: 0 = bit rate selection or card emulation selection, see 表 6-28
B0	iso_0	RFID / NFC bit rate	NFC: 0 = bit rate selection or card emulation selection, see 表 6-28

表 6-27. ISO Control Register ISO_x Settings, RFID Mode

ISO_4	ISO_3	ISO_2	ISO_1	ISO_0	PROTOCOL	REMARKS
0	0	0	0	0	ISO/IEC 15693 low bit rate, 6.62 kbps, one subcarrier, 1 out of 4	
0	0	0	0	1	ISO/IEC 15693 low bit rate, 6.62 kbps, one subcarrier, 1 out of 256	
0	0	0	1	0	ISO/IEC 15693 high bit rate, 26.48 kbps, one subcarrier, 1 out of 4	Default for reader
0	0	0	1	1	ISO/IEC 15693 high bit rate, 26.48 kbps, one subcarrier, 1 out of 256	
0	0	1	0	0	ISO/IEC 15693 low bit rate, 6.67 kbps, double subcarrier, 1 out of 4	
0	0	1	0	1	ISO/IEC 15693 low bit rate, 6.67 kbps, double subcarrier, 1 out of 256	
0	0	1	1	0	ISO/IEC 15693 high bit rate, 26.69 kbps, double subcarrier, 1 out of 4	
0	0	1	1	1	ISO/IEC 15693 high bit rate, 26.69 kbps, double subcarrier, 1 out of 256	
0	1	0	0	0	ISO/IEC 14443 A RX bit rate, 106 kbps	RX bit rate (1)
0	1	0	0	1	ISO/IEC 14443 A RX high bit rate, 212 kbps	
0	1	0	1	0	ISO/IEC 14443 A RX high bit rate, 424 kbps	
0	1	0	1	1	ISO/IEC 14443 A RX high bit rate, 848 kbps	
0	1	1	0	0	ISO/IEC 14443 B RX bit rate, 106 kbps	RX bit rate (1)
0	1	1	0	1	ISO/IEC 14443 B RX high bit rate, 212 kbps	
0	1	1	1	0	ISO/IEC 14443 B RX high bit rate, 424 kbps	
0	1	1	1	1	ISO/IEC 14443 B RX high bit rate, 848 kbps	
1	0	0	1	1	Reserved	
1	0	1	0	0	Reserved	
1	1	0	1	0	FeliCa 212 kbps	
1	1	0	1	1	FeliCa 424 kbps	

(1) For ISO/IEC 14443 A or B, when bit rate of TX is different from RX, settings can be done in register 0x02 or 0x03.

表 6-28. ISO Control Register ISO_x Settings, NFC Mode (B5 = 1, B2 = 0) or Card Emulation (B5 = 1, B2 = 1)

ISO_1	ISO_0	NFC (B5 = 1, B2 = 0)	CARD EMULATION (B5 = 1, B2 = 1)
0	0	N/A	ISO/IEC 14443 A
0	1	106 kbps	ISO/IEC 14443 B
1	0	212 kbps	N/A
1	1	424 kbps	N/A

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6.15.3.2 Control Registers – Sublevel Configuration Registers

6.15.3.2.1 ISO/IEC 14443 TX Options Register (0x02)

表 6-29 describes the ISO/IEC 14443 TX Options register.

表 6-29. ISO/IEC 14443 TX Options Register (0x02)

Function: Selects the ISO subsets for ISO/IEC 14443 – TX			
Default: 0x00 at POR = H or EN = L			
Bit	**Name**	**Function**	**Description**
B7	egt2	TX EGT time select MSB	Three bit code defines the number of etu (0-7) which separate two characters. ISO/IEC 14443 B TX only.
B6	egt1	TX EGT time select	
B5	egt0	TX EGT time select LSB	
B4	eof_l0	1 = EOF→ 0 length 11 etu 0 = EOF→ 0 length 10 etu	ISO/IEC 14443 B TX only
B3	sof_l1	1 = SOF→ 1 length 03 etu 0 = SOF→ 1 length 02 etu	
B2	sof _l0	1 = SOF→ 0 length 11 etu 0 = SOF→ 0 length 10 etu	
B1	l_egt	1 = EGT after each byte 0 = EGT after last byte is omitted	
B0	Auto SDD_SAK	1 = ISO/IEC 14443 A Layer 4 compliant (in SAK response) 0 = Not Layer 4 compliant (in SAK response)	For use with Auto SDD configuration, makes B6 in ISO/IEC 14443 A response 1 or 0, indicating Layer 4 compliance (or not), for all other cases, this bit is unused

6.15.3.2.2 ISO/IEC 14443 High-Bit-Rate and Parity Options Register (0x03)

表 6-30 describes the ISO/IEC 14443 High-Bit-Rate and Parity Options register.

表 6-30. ISO/IEC 14443 High-Bit-Rate and Parity Options Register (0x03)

Function: Selects the ISO subsets for ISO/IEC 14443 – TX			
Default: 0x00 at POR = H or EN = L, and at each write to ISO Control register			
Bit	**Name**	**Function**	**Description**
B7	dif_tx_br	TX bit rate different from RX bit rate enable	Valid for ISO/IEC 14443 A or B high bit rate
B6	tx_br1	TX bit rate	tx_br1 = 0, tx_br = 0 → 106 kbps tx_br1 = 0, tx_br = 1 → 212 kbps tx_br1 = 1, tx_br = 0 → 424 kbps tx_br1 = 1, tx_br = 1 → 848 kbps
B5	tx_br0		
B4	parity-2tx	1 = parity odd except last byte which is even for TX	For ISO/IEC 14443 A high bit rate, coding and decoding
B3	parity-2rx	1 = parity odd except last byte which is even for RX	
B2			Unused
B1			Unused
B0			Unused

6.15.3.2.3 TX Timer High Byte Control Register (0x04)

表 6-31 describes the TX Timer High Byte Control register.

表 6-31. TX Timer High Byte Control Register (0x04)

Function: For Timings			
Default: 0xC2 at POR = H or EN = L, and at each write to ISO Control register			
Bit	**Name**	**Function**	**Description**
B7	tm_st1	Timer Start Condition	tm_st1 = 0, tm_st0 = 0 → beginning of TX SOF tm_st1 = 0, tm_st0 = 1 → end of TX SOF tm_st1 = 1, tm_st0 = 0 → beginning of RX SOF tm_st1 = 1, tm_st0 = 1 → end of RX SOF
B6	tm_st0	Timer Start Condition	
B5	tm_lengthD	Timer Length MSB	
B4	tm_lengthC	Timer Length	
B3	tm_lengthB	Timer Length	
B2	tm_lengthA	Timer Length	
B1	tm_length9	Timer Length	
B0	tm_length8	Timer Length LSB	

6.15.3.2.4 TX Timer Low Byte Control Register (0x05)

表 6-32 describes the TX Timer Low Byte Control register.

表 6-32. TX Timer Low Byte Control Register (0x05)

Function: For Timings			
Default: 0x00 at POR = H or EN = L, and at each write to ISO Control register			
Bit	**Name**	**Function**	**Description**
B7	tm_length7	Timer Length MSB	Defines the time when delayed transmission is started. RX wait range is 590 ns to 9.76 ms (1 to 16383) Step size is 590 ns All bits low = timer disabled (0x00) Preset 0x00 for all other protocols
B6	tm_length6	Timer Length	
B5	tm_length5	Timer Length	
B4	tm_length4	Timer Length	
B3	tm_length3	Timer Length	
B2	tm_length2	Timer Length	
B1	tm_length1	Timer Length	
B0	tm_length0	Timer Length LSB	

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6.15.3.2.5 TX Pulse Length Control Register (0x06)

The length of the modulation pulse is defined by the protocol selected in the ISO Control register 0x01. With a high Q antenna, the modulation pulse is typically prolonged, and the tag detects a longer pulse than intended. For such cases, the modulation pulse length can be corrected by using the TX Pulse Length Control register (0x06). If the register contains all zeros, then the pulse length is governed by the protocol selection. If the register contains a value other than 0x00, the pulse length is equal to the value of the register in 73.7-ns increments. This means the range of adjustment can be 73.7 ns to 18.8 µs.

表 6-33 describes the TX Pulse Length Control register.

表 6-33. TX Pulse Length Control Register (0x06)

Function: Controls the length of TX pulse			
Default: 0x00 at POR = H or EN = L and at each write to ISO Control register.			
Bit	**Name**	**Function**	**Description**
B7	Pul_p2	Pulse length MSB	The pulse range is 73.7 ns to 18.8 µs (1….255), step size 73.7 ns. All bits low (00): pulse length control is disabled. The following default timings are preset by the ISO Control register (0x01): 9.44 µs → ISO/IEC 15693 (TI Tag-It HF-I) 11 µs → Reserved 2.36 µs → ISO/IEC 14443 A at 106 kbps 1.4 µs → ISO/IEC 14443 A at 212 kbps 737 ns → ISO/IEC 14443 A at 424 kbps 442 ns → ISO/IEC 14443 A at 848 kbps; pulse length control disabled
B6	Pul_p1		
B5	Pul_p0		
B4	Pul_c4		
B3	Pul_c3		
B2	Pul_c2		
B1	Pul_c1		
B0	Pul_c0	Pulse length LSB	

6.15.3.2.6 RX No Response Wait Time Register (0x07)

The RX No Response timer is controlled by the RX NO Response Wait Time Register 0x07. This timer measures the time from the start of slot in the anticollision sequence until the start of tag response. If there is no tag response in the defined time, an interrupt request is sent and a flag is set in IRQ status control register 0x0C. This enables the external controller to be relieved of the task of detecting empty slots. The wait time is stored in the register in increments of 37.76 µs. This register is also preset, automatically, for every new protocol selection. Sending a Reset FIFO (0x0F) direct command after a TX Complete interrupt will disable this feature.

表 6-34 describes the RX No Response Wait Time register.

表 6-34. RX No Response Wait Time Register (0x07)

Function: Defines the time when "no response" interrupt is sent; only for ISO/IEC 15693			
Default: 0x0E at POR = H or EN = L and at each write to ISO Control register			
Bit	**Name**	**Function**	**Description**
B7	NoResp7	No response MSB	Defines the time when "no response" interrupt is sent. It starts from the end of TX EOF. RX no response wait range is 37.76 µs to 9628 µs (1 to 255), step size is: 37.76 µs. The following default timings are preset by the ISO Control register (0x01): 390 µs → Reserved 529 µs → for all protocols supported, but not listed here 604 µs → Reserved 755 µs → ISO/IEC 15693 high data rate (TI Tag-It HF-I) 1812 µs → ISO/IEC 15693 low data rate (TI Tag-It HF-I)
B6	NoResp6		
B5	NoResp5		
B4	NoResp4		
B3	NoResp3		
B2	NoResp2		
B1	NoResp1		
B0	NoResp0	No response LSB	

6.15.3.2.7 RX Wait Time Register (0x08)

The RX-wait-time timer is controlled by the value in the RX wait time register 0x08. This timer defines the time after the end of the transmit operation in which the receive decoders are not active (held in reset state). This prevents incorrect detections resulting from transients following the transmit operation. The value of the RX wait time register defines this time in increments of 9.44 µs. This register is preset at every write to ISO Control register 0x01 according to the minimum tag response time defined by each standard.

表 6-35 describes the RX Wait Time register.

表 6-35. RX Wait Time Register (0x08)

Function: Defines the time after TX EOF when the RX input is disregarded for example, to block out electromagnetic disturbance generated by the responding card.			
Default: 0x1F at POR = H or EN = L and at each write to*ISO control* register.			
Bit	**Name**	**Function**	**Description**
B7	Rxw7	RX wait time	Defines the time after the TX EOF during which the RX input is ignored. Time starts from the end of TX EOF. RX wait range is 9.44 µs to 2407 µs (1 to 255), Step size 9.44 µs. The following default timings are preset by the ISO Control register (0x01): 9.44 µs → FeliCa 66 µs → ISO/IEC 14443 A and B 180 µs → Reserved 293 µs → ISO/IEC 15693 (TI Tag-It HF-I)
B6	Rxw6		
B5	Rxw5		
B4	Rxw4		
B3	Rxw3		
B2	Rxw2		
B1	Rxw1		
B1	Rxw0		

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6.15.3.2.8 Modulator and SYS_CLK Control Register (0x09)

The frequency of SYS_CLK (pin 27) is programmable by the bits B4 and B5 of this register. The frequency of the TRF7970A system clock oscillator is divided by 1, 2 or 4 resulting in available SYS_CLK frequencies of 13.56 MHz or 6.78 MHz or 3.39 MHz.

The ASK modulation depth is controlled by bits B0, B1 and B2. The range of ASK modulation is 7% to 30% or 100% (OOK). The selection between ASK and OOK (100%) modulation can also be done using direct input OOK (pin 12). The direct control of OOK/ASK using OOK pin is only possible if the function is enabled by setting B6 = 1 (en_ook_p) in this register (0x09) and the ISO Control Register (0x01, B6 = 1). When configured this way, the MOD (pin 14) is used as input for the modulation signal.

表 6-36 describes the Modulator and SYS_CLK Control register.

表 6-36. Modulator and SYS_CLK Control Register (0x09)

<table>
<tr><td colspan="6">Function: Controls the modulation input and depth, ASK / OOK control and clock output to external system (MCU)</td></tr>
<tr><td colspan="6">Default: 0x91 at POR = H or EN = L, and at each write to ISO control register, except Clo1 and Clo0.</td></tr>
<tr><th>Bit</th><th>Name</th><th>Function</th><th colspan="3">Description</th></tr>
<tr><td>B7</td><td>27MHz</td><td>Enables 27.12-MHz crystal</td><td colspan="3">Default = 1 (enabled)</td></tr>
<tr><td>B6</td><td>en_ook_p</td><td>1 = Enables external selection of ASK or OOK modulation
0 = Default operation as defined in B0 to B2 (0x09)</td><td colspan="3">Enable ASK/OOK pin (pin 12) for "on the fly change" between any preselected ASK modulation as defined by B0 to B2 and OOK modulation:
If B6 is 1, pin 12 is configured as follows:
1 = OOK modulation
0 = Modulation as defined in B0 to B2 (0x09)</td></tr>
<tr><td rowspan="5">B5

B4</td><td rowspan="5">Clo1

Clo0</td><td rowspan="5">SYS_CLK output frequency MSB

SYS_CLK output frequency LSB</td><td>Clo1</td><td>Clo0</td><td>SYS_CLK Output (if 13.56-MHz crystal is used)
SYS_CLK Output (if 27.12-MHz crystal is used)</td></tr>
<tr><td>0</td><td>0</td><td>Disabled
Disabled</td></tr>
<tr><td>0</td><td>1</td><td>3.39 MHz
6.78 MHz</td></tr>
<tr><td>1</td><td>0</td><td>6.78 MHz
13.56 MHz</td></tr>
<tr><td>1</td><td>1</td><td>13.56 MHz
27.12 MHz</td></tr>
<tr><td>B3</td><td>en_ana</td><td>1 = Sets pin 12 (ASK/OOK) as an analog output
0 = Default</td><td colspan="3">For test and measurement purpose. ASK/OOK pin 12 can be used to monitor the analog subcarrier signal before the digitizing with DC level equal to AGND.</td></tr>
<tr><td rowspan="5">B2

B1

B0</td><td rowspan="5">Pm2

Pm1

Pm0</td><td rowspan="5">Modulation depth MSB

Modulation depth

Modulation depth LSB</td><td>Pm2</td><td>Pm1</td><td>Pm0
Mod Type and %</td></tr>
<tr><td>0</td><td>0</td><td>0
ASK 10%</td></tr>
<tr><td>0</td><td>0</td><td>1
OOK (100%)</td></tr>
<tr><td>0</td><td>1</td><td>0
ASK 7%</td></tr>
<tr><td>0</td><td>1</td><td>1
ASK 8.5%</td></tr>
<tr><td>1</td><td>0</td><td>0
ASK 13%</td></tr>
<tr><td>1</td><td>0</td><td>1
ASK 16%</td></tr>
<tr><td>1</td><td>1</td><td>0
ASK 22%</td></tr>
<tr><td>1</td><td>1</td><td>1
ASK 30%</td></tr>
</table>

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6.15.3.2.9 RX Special Setting Register (0x0A)

表 6-37 describes the RX Special Setting register.

表 6-37. RX Special Setting Register (0x0A)

Function: Sets the gains and filters directly			
Default: 0x40 at POR = H or EN = L, and at each write to the ISO Control register 0x01. When bits B7, B6, B5 and B4 are all zero, the filters are set for ISO/IEC 14443 B (240 kHz to 1.4 MHz).			
Bit	**Name**	**Function**	**Description**
B7	C212	Band-pass 110 kHz to 570 kHz	Appropriate for 212-kHz subcarrier system (FeliCa)
B6	C424	Band-pass 200 kHz to 900 kHz	Appropriate for 424-kHz subcarrier used in ISO/IEC 15693
B5	M848	Band-pass 450 kHz to 1.5 MHz	Appropriate for Manchester-coded 848-kHz subcarrier used in ISO/IEC 14443 A and B
B4	hbt	Band-pass 100 kHz to 1.5 MHz Gain reduced for 18 dB	Appropriate for highest bit rate (848 kbps) used in high-bit-rate ISO/IEC 14443
B3	gd1	00 = Gain reduction 0 dB 01 = Gain reduction for 5 dB 10 = Gain reduction for 10 dB 11 = Gain reduction for 15 dB	Sets the RX gain reduction and reduces sensitivity
B2	gd2		
B1	Reserved		
B0	Reserved		

注

The setting of bits B4, B5, B6 and B7 to 0 selects bandpass characteristic of 240 kHz to 1.4 MHz. This is appropriate for ISO/IEC 14443 B, FeliCa protocol, and ISO/IEC 14443 A higher bit rates of 212 kbps and 424 kbps.

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6.15.3.2.10 Regulator and I/O Control Register (0x0B)

表 6-38 describes the Regulator and I/O Control register.

表 6-38. Regulator and I/O Control Register (0x0B)

Function: Control the three voltage regulators			
Default: 0x87 at POR = H or EN = L			
Bit	**Name**	**Function**	**Description**
B7	auto_reg	0 = Manual settings; see B0 to B2 in 表 6-39 and 表 6-40 1 = Automatic setting (see 表 6-41 and 表 6-42)	Auto system sets V_{DD_RF} = V_{IN} – 250 mV and V_{DD_A} = V_{IN} – 250 mV and V_{DD_X}= V_{IN} – 250 mV, but not higher than 3.4 V.
B6	en_ext_pa	Support for external power amplifier	Internal peak detectors are disabled, receiver inputs (RX_IN1 and RX_IN2) accept externally demodulated subcarrier. At the same time ASK/OOK pin 12 becomes modulation output for external TX amplifier.
B5	io_low	1 = enable low peripheral communication voltage	When B5 = 1, maintains the output driving capabilities of the I/O pins connected to the level shifter under low voltage operation. Should be set 1 when $V_{DD_I/O}$ voltage is between 1.8 V to 2.7 V.
B4	Unused	No function	Default is 0.
B3	Unused	No function	Default is 0.
B2	vrs2	Voltage set MSB voltage set LSB	Vrs3_5 = L: V_{DD_RF}, V_{DD_A}, V_{DD_X} range 2.7 V to 3.4 V; see 表 6-39 and 表 6-40
B1	vrs1		
B0	vrs0		

表 6-39. Supply-Regulator Setting – Manual 5-V System

REGISTER	OPTION BITS SETTING IN CONTROL REGISTER								ACTION
	B7	B6	B5	B4	B3	B2	B1	B0	
00								1	5-V system
0B	0								Manual regulator setting
0B	0					1	1	1	V_{DD_RF} = 5 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					1	1	0	V_{DD_RF} = 4.9 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					1	0	1	V_{DD_RF} = 4.8 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					1	0	0	V_{DD_RF} = 4.7 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					0	1	1	V_{DD_RF} = 4.6 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					0	1	0	V_{DD_RF} = 4.5 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					0	0	1	V_{DD_RF} = 4.4 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V
0B	0					0	0	0	V_{DD_RF} = 4.3 V, V_{DD_A} = 3.4 V, V_{DD_X} = 3.4 V

表 6-40. Supply-Regulator Setting – Manual 3-V System

REGISTER	OPTION BITS SETTING IN CONTROL REGISTER								ACTION
	B7	B6	B5	B4	B3	B2	B1	B0	
00								0	3-V system
0B	0								Manual regulator setting
0B	0					1	1	1	V_{DD_RF} = 3.4 V, V_{DD_A} and V_{DD_X} = 3.4 V
0B	0					1	1	0	V_{DD_RF} = 3.3 V, V_{DD_A} and V_{DD_X} = 3.3 V
0B	0					1	0	1	V_{DD_RF} = 3.2 V, V_{DD_A} and V_{DD_X} = 3.2 V
0B	0					1	0	0	V_{DD_RF} = 3.1 V, V_{DD_A} and V_{DD_X} = 3.1 V
0B	0					0	1	1	V_{DD_RF} = 3.0 V, V_{DD_A} and V_{DD_X} = 3.0 V
0B	0					0	1	0	V_{DD_RF} = 2.9 V, V_{DD_A} and V_{DD_X} = 2.9 V
0B	0					0	0	1	V_{DD_RF} = 2.8 V, V_{DD_A} and V_{DD_X} = 2.8 V
0B	0					0	0	0	V_{DD_RF} = 2.7 V, V_{DD_A} and V_{DD_X} = 2.7 V

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表 6-41. Supply-Regulator Setting – Automatic 5-V System

REGISTER	OPTION BITS SETTING IN CONTROL REGISTER								ACTION
	B7	B6	B5	B4	B3	B2	B1	B0	
00								1	5-V system
0B	1					x(1)	0	0	Automatic regulator setting 400-mV difference

(1) x = don't care

表 6-42. Supply-Regulator Setting – Automatic 3-V System

REGISTER	OPTION BITS SETTING IN CONTROL REGISTER								ACTION
	B7	B6	B5	B4	B3	B2	B1	B0	
00								0	3-V system
0B	1					x(1)	0	0	Automatic regulator setting 400-mV difference

(1) x = don't care

6.15.3.3 Status Registers

6.15.3.3.1 IRQ Status Register (0x0C)

表 6-43 describes the IRQ Status register.

表 6-43. IRQ Status Register (0x0C)

Function: Information available about TRF7970A IRQ and TX/RX status			
Default: 0x00 at POR = H or EN = L, and at each write to the ISO Control Register 0x01. It is also automatically reset at the end of a read phase. The reset also removes the IRQ flag.			
Bit	**Name**	**Function**	**Description**
B7	Irq_tx	IRQ set due to end of TX	Signals that TX is in progress. The flag is set at the start of TX but the interrupt request (IRQ = 1) is sent when TX is finished.
B6	Irg_srx	IRQ set due to RX start	Signals that RX SOF was received and RX is in progress. The flag is set at the start of RX but the interrupt request (IRQ = 1) is sent when RX is finished.
B5	Irq_fifo	Signals the FIFO level	Signals FIFO high or low as set in the Adjustable FIFO IRQ Levels (0x14) register
B4	Irq_err1	CRC error	Indicates receive CRC error only if B7 (no RX CRC) of ISO Control register is set to 0.
B3	Irq_err2	Parity error	Indicates parity error for ISO/IEC 14443 A
B2	Irq_err3	Byte framing or EOF error	Indicates framing error
B1	Irq_col	Collision error	Collision error for ISO/IEC 14443 A and ISO/IEC 15693 single subcarrier. Bit is set if more then 6 or 7 (as defined in register 0x10) are detected in 1 bit period of ISO/IEC 14443 A 106 kbps. Collision error bit can also be triggered by external noise.
B0	Irq_noresp	No response time interrupt	No response within the "No-response time" defined in RX No Response Wait Time register (0x07). Signals the MCU that the next slot command can be sent. Only for ISO/IEC 15693.

To reset (clear) the register 0x0C and the IRQ line, the register must be read. During Transmit the decoder is disabled, only bits B5 and B7 can be changed. During Receive only bit B6 can be changed, but does not trigger the IRQ line immediately. The IRQ signal is set at the end of Transmit and Receive phase.

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表 6-44 describes the IRQ Status register when used for NFC and card emulation operation.

表 6-44. IRQ Status Register (0x0C) for NFC and Card Emulation Operation

Function: Information available about TRF7970A IRQ and TX/RX status			
Default: 0x00 at POR = H or EN = L, and at each write to the ISO Control Register 0x01. It is also automatically reset at the end of a read phase. The reset also removes the IRQ flag.			
Bit	**Name**	**Function**	**Description**
B7	Irq_tx	IRQ set due to end of TX	Signals that TX is in progress. The flag is set at the start of TX but the interrupt request (IRQ = 1) is sent when TX is finished.
B6	Irg_srx	IRQ set due to RX start	Signals that RX SOF was received and RX is in progress. The flag is set at the start of RX but the interrupt request (IRQ = 1) is sent when RX is finished.
B5	Irq_fifo	Signals the FIFO level	Signals FIFO high or low as set in the Adjustable FIFO IRQ Levels (0x14) register
B4	Irq_err1	Protocol error	Any protocol error
B3	Irq_sdd	SDD completed	SDD (passive target at 106 kbps) successfully finished
B2	Irq_rf	RF field change	Sufficient RF signal level for operation was reached or lost
B1	Irq_col	RF collision avoidance finished	The system has finished collision avoidance and the minimum wait time is elapsed.
B0	Irq_col_err	RF collision avoidance not finished successfully	The external RF field was present so the collision avoidance could not be carried out.

6.15.3.3.2 Interrupt Mask Register (0x0D) and Collision Position Register (0x0E)

表 6-45 describes the Interrupt Mask register. 表 6-46 describes the Collision Position register.

表 6-45. Interrupt Mask Register (0x0D)

Default: 0x3E at POR = H and EN = L. Collision bits reset automatically after read operation.			
Bit	**Name**	**Function**	**Description**
B7	Col9	Bit position of collision MSB	Supports ISO/IEC 14443 A
B6	Col8	Bit position of collision	
B5	En_irq_fifo	Interrupt enable for FIFO	Default = 1
B4	En_irq_err1	Interrupt enable for CRC	Default = 1
B3	En_irq_err2	Interrupt enable for Parity	Default = 1
B2	En_irq_err3	Interrupt enable for Framing error or EOF	Default = 1
B1	En_irq_col	Interrupt enable for collision error	Default = 1
B0	En_irq_noresp	Enables no-response interrupt	Default = 0

表 6-46. Collision Position Register (0x0E)

Function: Displays the bit position of collision or error			
Default: 0x00 at POR = H and EN = L. Automatically reset after read operation.			
Bit	**Name**	**Function**	**Description**
B7	Col7	Bit position of collision MSB	ISO/IEC 14443 A mainly supported, in the other protocols this register shows the bit position of error. Frame, SOF, EOF, parity, or CRC error.
B6	Col6		
B5	Col5		
B4	Col4		
B3	Col3		
B2	Col2		
B1	Col1		
B0	Col0	Bit position of collision LSB	

6.15.3.3.3 RSSI Levels and Oscillator Status Register (0x0F)

表 6-47 describes the RSSI Levels and Oscillator Status register.

表 6-47. RSSI Levels and Oscillator Status Register (0x0F)

Function: Displays the signal strength on both reception channels and RF amplitude during RF-off state. The RSSI values are valid from reception start till start of next transmission.			
Bit	**Name**	**Function**	**Description**
B7	Unused		
B6	osc_ok	Crystal oscillator stable indicator	13.56-MHz frequency stable (approximately 200 µs)
B5	rssi_x2	MSB RSSI value of auxiliary RX (RX_IN2)	Auxiliary channel is by default RX_IN2. The input can be swapped by B3 = 1 (Chip Status Control register 0x00). If "swapped", the Auxiliary channel is connected to RX_IN1 and, hence, the Auxiliary RSSI represents the signal level at RX_IN1.
B4	rssi_x1	Auxiliary channel RSSI	
B3	rssi_x0	MSB RSSI value of auxiliary RX (RX_IN2)	
B2	rssi_2	MSB RSSI value of main RX (RX_IN1)	Active channel is default and can be set with option bit B3 = 0 of Chip Status Control register 0x00.
B1	rssi_1	Main channel RSSI	
B0	rssi_0	LSB RSSI value of main RX (RX_IN1)	

RSSI measurement block is measuring the demodulated envelope signal (except in case of direct command for RF amplitude measurement described later in direct commands section). The measuring system is latching the peak value, so the RSSI level can be read after the end of receive packet. The RSSI value is reset during next transmit action of the reader, so the new tag response level can be measured. The RSSI levels calculated to the RF_IN1 and RF_IN2 are presented in 节 6.5.1.1 and 节 6.5.1.2. The RSSI has 7 steps (3 bits) with 4-dB increment. The input level is the peak-to-peak modulation level of RF signal measured on one side envelope (positive or negative).

6.15.3.3.4 Special Functions Register (0x10)

表 6-48 describes the Special Functions register at address 0x10.

表 6-48. Special Functions Register (0x10)

Function: User configurable options for ISO/IEC 14443 A specific operations			
Bit	**Name**	**Function**	**Description**
B7		Reserved	Reserved
B6		Reserved	Reserved
B5	par43	Disables parity checking for ISO/IEC 14443 A	
B4	next_slot_37us	0 = 18.88 µs 1 = 37.77 µs	Sets the time grid for next slot command in ISO/IEC 15693
B3	Sp_dir_mode	Bit stream transmit for MIFARE at 106 kbps	Enables direct mode for transmitting ISO/IEC 14443 A data, bypassing the FIFO and feeding the data bit stream directly onto the encoder.
B2	4_bit_RX	0 = normal receive 1 = 4-bit receive	Enable 4-bit replay for example, ACK, NACK used by some cards; for example, MIFARE Ultralight
B1	14_anticoll	0 = anticollision framing (0x93, 0x95, 0x97) 1 = normal framing (no broken bytes)	Disable anticollision frames for ISO/IEC 14443 A (this bit should be set to 1 after anticollision is finished)
B0	col_7_6	0 = 7 subcarrier pulses 1 = 6 subcarrier pulses	Selects the number of subcarrier pulses that trigger collision error in ISO/IEC 14443 A at 106 kbps

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6.15.3.3.5 Special Functions Register (0x11)

表 6-49 describes the Special Functions register at address 0x11.

表 6-49. Special Functions Register (0x11)

Function: Indicate IRQ status for RX operations.			
Bit	**Name**	**Function**	**Description**
B7	Reserved		Reserved
B6	Reserved		Reserved
B5	Reserved		Reserved
B4	Reserved		Reserved
B3	Reserved		Reserved
B2	Reserved		Reserved
B1	Reserved		Reserved
B0	irg_srx	Copy of the RX start signal (Bit 6) of the IRQ Status register (0x0C)	Signals the RX SOF was received and the RX is in progress. IRQ when RX is completed.

6.15.3.3.6 Adjustable FIFO IRQ Levels Register (0x14)

表 6-50 describes the Adjustable FIFO IRQ Levels register.

表 6-50. Adjustable FIFO IRQ Levels Register (0x14)

Function: Adjusts level at which FIFO indicates status by IRQ					
Default: 0x00 at POR = H and EN = L					
Bit	**Name**	**Function**	**Description**		
B7	Reserved		Reserved		
B6	Reserved		Reserved		
B5	Reserved		Reserved		
B4	Reserved		Reserved		
B3	Wlh_1	FIFO high IRQ level (during RX)	**Wlh_1** 0 0 1 1	**Wlh_0** 0 1 0 1	**IRQ Level** 124 120 112 96
B2	Wlh_0				
B1	Wll_1	FIFO low IRQ level (during TX)	**Wll_1** 0 0 1 1	**Wll_0** 0 1 0 1	**IRQ Level** 4 8 16 32
B0	Wll_0				

6.15.3.3.7 NFC Low Field Level Register (0x16)

表 6-51 describes the NFC Low Field Level register.

表 6-51. NFC Low Field Level Register (0x16)

Function: Defines level for RF collision avoidance			
Default: 0x00 at POR = H and EN = L.			
Bit	**Name**	**Function**	**Description**
B7	Clex_dis	Disable clock extractor	NFC passive 106-kbps and ISO/IEC 14443 A card emulation
B6	Hash6	N/A	
B5	Hash5	N/A	
B4	Hash4	N/A	
B3	Hash3	N/A	
B2	Rfdet_l2	RF field level for RF collision avoidance	Comparator output is displayed in B6 of the NFC Target Protocol register (0x19)
B1	Rfdet_l1		
B0	Rfdet_l0		

6.15.3.3.8 NFCID1 Number Register (0x17)

This register is used to hold the ID of the TRF7970A for use during card emulation and NFC peer-to-peer target operations.

The procedure for writing the ID into register 0x17 is the following:

1. Write bits 5, 6, and 7 in register 0x18 to enable SDD anticollision (bit 5), and set bit 6 and 7 to select the ID length of 4, 7, or 10 bytes.
2. Write the ID into register 0x17. This should be done using write continuous mode with 4, 7, or 10 bytes (according to what was set in register 0x18 bits 6 and 7).

6.15.3.3.9 NFC Target Detection Level Register (0x18)

表 6-52 describes the NFC Target Detection Level register.

表 6-52. NFC Target Detection Level Register (0x18)

<table>
<tr><td colspan="5">Function: Defines level for RF wake up, enables automatic SDD and gives NFCID size. This register is supplied by Vin to ensure data retention during complete power down.</td></tr>
<tr><td colspan="5">Default: 0x00 at POR on Vin (not POR based on V_{DD_X}) and not reset at EN = 0</td></tr>
<tr><td>Bit</td><td>Name</td><td>Function</td><td colspan="2">Description</td></tr>
<tr><td rowspan="5">B7
B6</td><td rowspan="5">Id_s1
Id_s0</td><td rowspan="5">NFCID1 size used in 106-kbps passive target SDD</td><td>Id_s1</td><td>Id_s0</td><td>NFCID1 Size (bytes)</td></tr>
<tr><td>0</td><td>0</td><td>4</td></tr>
<tr><td>0</td><td>1</td><td>7</td></tr>
<tr><td>1</td><td>0</td><td>10</td></tr>
<tr><td>1</td><td>1</td><td>Not allowed</td></tr>
<tr><td>B5</td><td>Sdd_en</td><td></td><td colspan="3">Automatic SDD using internal state machine and ID stored in the NFCID1 Number register (0x17)</td></tr>
<tr><td>B4</td><td></td><td>N/A</td><td colspan="3"></td></tr>
<tr><td>B3</td><td>Hi_rf</td><td>Extended range for RF measurements</td><td colspan="3"></td></tr>
<tr><td>B2</td><td>Rfdet_h2</td><td rowspan="3">RF field level required for system wakeup. If all bits are 0, then the RF level detection is off.</td><td colspan="3" rowspan="3">Comparator output is displayed in B7 of the NFC Target Protocol register (0x19)</td></tr>
<tr><td>B1</td><td>Rfdet_h1</td></tr>
<tr><td>B0</td><td>Rfdet_h0</td></tr>
</table>

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6.15.3.3.10 NFC Target Protocol Register (0x19)

This register is used (when read) to display the bit rate and protocol type when an NFC/RFID Initiator/Reader is presented. An example use of this scenario would be when the TRF7970A is placed into card emulation (Type A or Type B) and another TRF7970A or NFC device (polling for other NFC devices) is presented to the TRF7970A in card emulation mode. The IRQ indicates that a field was detected (IRQ Status = 0x04) or that Auto SDD has completed (IRQ Status = 0x08, if configured for AutoSDD).

If Auto SDD is set and 0x04 is returned in IRQ status, then this register can be read out to see which commands are coming in for gaining knowledge of the polling cycle sequence. Then, when the correct first matching command (that is, REQA or REQB) is issued from Reader or Initiator, if AutoSDD is set, the IRQ fires and the IRQ Status is 0x08, indicating completion of the SDD. The next IRQ should return 0x40 as status, the Register 0x19 can be checked to make sure it is correct value (that is, 0xC9 for Type A at 106 kbps or 0xC5 for Type B at 106 kbps) indicating there are bytes in the FIFO and a read of the FIFO status indicates how many bytes to read out. For example, after AutoSDD is completed, there are four bytes in the FIFO, and these should be the RATS command coming in from the reader, which the MCU controlling the TRF7970A in Card Emulation mode must respond to. If AutoSDD is not set, as another example with the TRF7970A in ISO/IEC 14443 B Card Emulation mode, then the field detect happens as previously described and IRQs also fire to indicate RX is complete (0x40). This register must be checked and compared against case statement structure that is set up for the value of this register to be 0xC5, indicating that an ISO/IEC 14443 B command at 106 kbps was issued. When this register (0x19) is 0xC5, then the FIFO Status can be read and should hold a value of 0x03, and when read, be the REQB command (0x05, 0x00, 0x00); the controlling MCU must respond with the ATQB response. The next steps for either of these examples follow the relevant portions of the ISO/IEC 14443-3 or -4 standards, then the NFC Forum specifications, depending on the system use case or application.

表 6-53 describes the NFC Target Protocol register.

表 6-53. NFC Target Protocol Register (0x19)

Function: Displays the bit rate and protocol type (active or passive) transmitted by initiator in first command. It also displays the comparator outputs of both RF level detectors.			
Default: 0x00 at POR = H and EN = L. B0 to B4 are automatically reset after MCU continuous read operation. B6 and B7 continuously display the RF level comparator outputs.			
Bit	**Name**	**Function**	**Description**
B7	Rf_h	RF level is above the wake-up level setting	The wakeup level is defined by bits B0 to B2 in the NFC Target Detection Level register (0x18)
B6	Rf_l	RF level is above the RF collision avoidance level setting	The collision avoidance level is defined by bits B0 – B2 in the register 0x16 (NFC Low Field Detection Level)
B5	Reserved	Reserved	Reserved
B4	FeliCa	1 = FeliCa 0 = ISO/IEC 14443 A	The first initiator command had physical level coding of FeliCa or ISO/IEC 14443 A
B3	Pas_106	Passive target at 106 kbps or transponder emulation	The first initiator/reader command was SENS_REQ or ALL_REQ
B2	Pas_14443B	ISO/IEC 14443 B transponder emulation	The first reader command was ISO/IEC 14443 B
B1	NFCBR1	Bit rate of first received command	00 = Reserved 01 = 106 kbps 10 = 212 kbps 11 = 424 kbps
B0	NFCBR0		

6.15.3.4 Test Registers

6.15.3.4.1 Test Register (0x1A)

表 6-54 describes the Test register at address 0x1A.

表 6-54. Test Register (0x1A) (for Test or Direct Use)

Default: 0x00 at POR = H and EN = L.			
Bit	**Name**	**Function**	**Description**
B7	OOK_Subc_In	Subcarrier input	OOK pin becomes decoder digital input
B6	MOD_Subc_Out	Subcarrier output	MOD pin becomes receiver digitized subcarrier output
B5	MOD_Direct	Direct TX modulation and RX reset	MOD pin becomes input for TX modulation control by the MCU
B4	o_sel	First stage output selection	o_sel = L: First stage output used for analog out and digitizing o_sel = H: Second Stage output used for analog out and digitizing
B3	low2	Second stage gain –6 dB, HP corner frequency / 2	
B2	low1	First stage gain –6 dB, HP corner frequency / 2	
B1	zun	Input followers test	
B0	Test_AGC	AGC test, AGC level is seen on rssi_210 bits	

6.15.3.4.2 Test Register (0x1B)

表 6-55 describes the Test register at address 0x1B.

表 6-55. Test Register (0x1B) (for Test or Direct Use)

Default: 0x00 at POR = H and EN = L. When a test_dec or test_io is set IC is switched to test mode. Test Mode persists until a stop condition arrives. At stop condition the test_dec and test_io bits are cleared.			
Bit	**Name**	**Function**	**Description**
B7	test_rf_level	RF level test	
B6			
B5			
B4			
B3	test_io1	I/O test	Not implemented
B2	test_io0		
B1	test_dec	Decoder test mode	
B0	clock_su	Coder clock 13.56 MHz	For faster test of coders

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6.15.3.5 FIFO Control Registers

节 6.15.3.5.1 describes the FIFO Status register.

6.15.3.5.1 FIFO Status Register (0x1C)

表 6-56. FIFO Status Register (0x1C)

Function: Number of bytes available to be read from FIFO (= N number of bytes, in hexadecimal)			
Bit	**Name**	**Function**	**Description**
B7	Foverflow	FIFO overflow error	Bit is set when FIFO has more than 127 bytes presented to it
B6	Fb6	FIFO bytes fb[6]	Bits B0:B6 indicate how many bytes are in the FIFO to be read out (= N number of bytes, in hex)
B5	Fb5	FIFO bytes fb[5]	
B4	Fb4	FIFO bytes fb[4]	
B3	Fb3	FIFO bytes fb[3]	
B2	Fb2	FIFO bytes fb[2]	
B1	Fb1	FIFO bytes fb[1]	
B0	Fb0	FIFO bytes fb[0]	

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6.15.3.5.2 TX Length Byte1 Register (0x1D), TX Length Byte2 Register (0x1E)

表 6-57 describes the TX Length Byte1 register. 表 6-58 describes the TX Length Byte2 register.

表 6-57. TX Length Byte1 Register (0x1D)

Function: High 2 nibbles of complete, intended bytes to be transferred through FIFO			
Register default is set to 0x00 at POR and EN = 0. It is also automatically reset at TX EOF			
Bit	**Name**	**Function**	**Description**
B7	Txl11	Number of complete byte bn[11]	High nibble of complete, intended bytes to be transmitted
B6	Txl10	Number of complete byte bn[10]	
B5	Txl9	Number of complete byte bn[9]	
B4	Txl8	Number of complete byte bn[8]	
B3	Txl7	Number of complete byte bn[7]	Middle nibble of complete, intended bytes to be transmitted
B2	Txl6	Number of complete byte bn[6]	
B1	Txl5	Number of complete byte bn[5]	
B0	Txl4	Number of complete byte bn[4]	

表 6-58. TX Length Byte2 Register (0x1E)

Function: Low nibbles of complete bytes to be transferred through FIFO; Information about a broken byte and number of bits to be transferred from it			
Default: 0x00 at POR and EN = 0. It is also automatically reset at TX EOF			
Bit	**Name**	**Function**	**Description**
B7	Txl3	Number of complete byte bn[3]	Low nibble of complete, intended bytes to be transmitted
B6	Txl2	Number of complete byte bn[2]	
B5	Txl1	Number of complete byte bn[1]	
B4	Txl0	Number of complete byte bn[0]	
B3	Bb2	Broken byte number of bits bb[2]	Number of bits in the last broken byte to be transmitted. Valid only when broken byte flag is set.
B2	Bb1	Broken byte number of bits bb[1]	
B1	Bb0	Broken byte number of bits bb[0]	
B0	Bbf	Broken byte flag	B0 = 1 indicates that last byte is not complete 8 bits wide.

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7 Applications, Implementation, and Layout

注

Information in the following Applications section is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 TRF7970A Reader System Using SPI With SS Mode

7.1.1 General Application Considerations

图 7-1 shows and application schematic optimized for all TRF7970A modes using the Serial Port Interface (SPI). Short SPI lines, proper isolation of radio frequency lines, and a proper ground area are essential to avoid interference. The recommended clock frequency on the DATA_CLK line is 2 MHz. This figure also shows matching to a 50-Ω port, which allows connecting to a properly matched 50-Ω antenna circuit or RF measurement equipment (for example, a spectrum analyzer or power meter).

7.1.2 Schematic

图 7-1 shows a sample application schematic for SPI with an SS mode MCU interface.

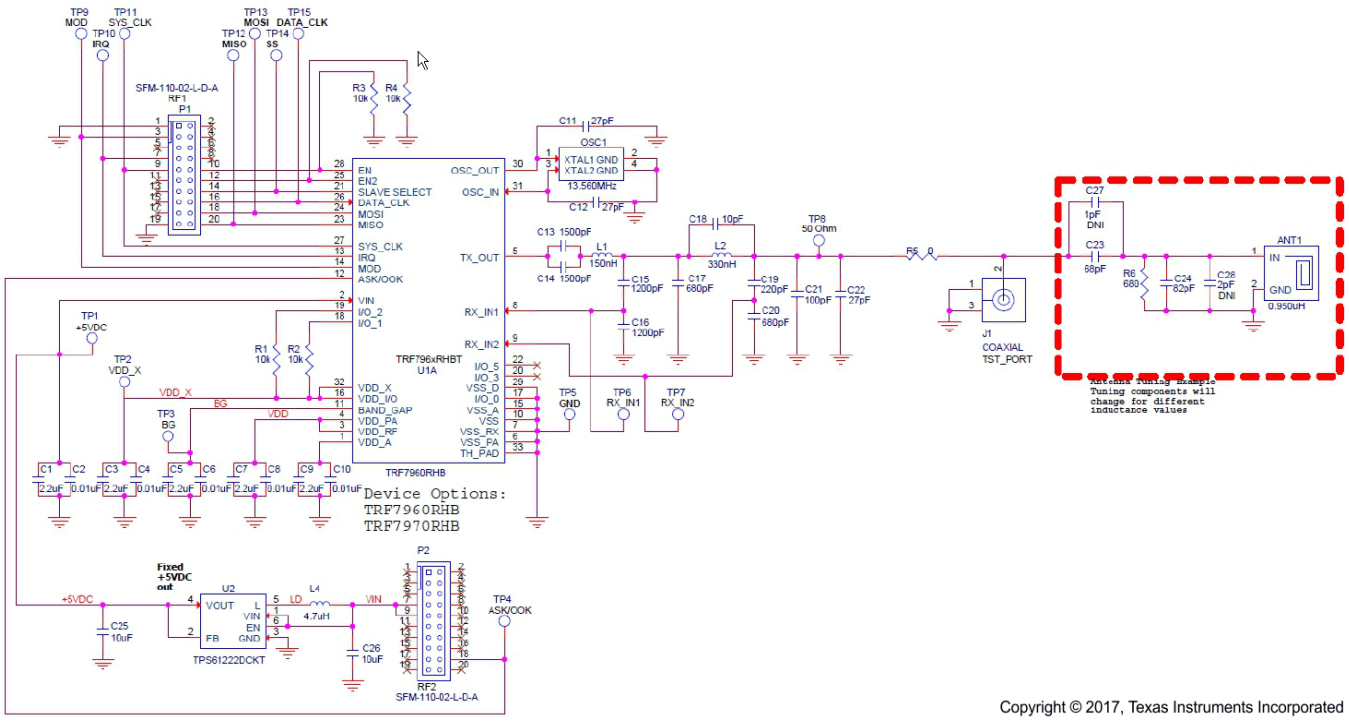

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图 7-1. Application Schematic – SPI With SS Mode MCU Interface

Minimum MCU requirements depend on application requirements and coding style. If only one ISO protocol or a limited command set of a protocol needs to be supported, MCU Flash and RAM requirements can be significantly reduced. Recursive inventory and anticollision commands require more RAM than single slotted operations. For example, an ISO/IEC 15693-only application that supports anticollision needs approximately 7KB of flash memory and 500 bytes of RAM. In contrast, a full NFC stack that supports peer-to-peer, card emulation, and reader/writer modes needs 65KB of flash memory and 4KB of RAM. An MCU that can run its GPIOs at 13.56 MHz is required for direct mode 0 operations.

7.2 Layout Considerations

Keep all decoupling capacitors as close to the IC as possible, with the high-frequency decoupling capacitors (10 nF) closer than the low-frequency decoupling capacitors (2.2 µF).

Place ground vias as close as possible to the ground side of the capacitors and reader IC pins to minimize possible ground loops.

TI recommends not using any inductor sizes smaller than 0603, as the output power can be compromised. If smaller inductors are necessary, output performance must be confirmed in the final application.

Pay close attention to the required load capacitance of the crystal, and adjust the two external shunt capacitors accordingly. Follow the recommendations of the crystal manufacturer for those values.

There should be a common ground plane for the digital and analog sections. The multiple ground sections or islands should have vias that tie the different sections of the planes together.

Ensure that the exposed thermal pad at the center of the reader IC is properly laid out. It should be tied to ground to help dissipate any heat from the package.

All trace line lengths should be made as short as possible, particularly the RF output path, crystal connections, and control lines from the reader to the microprocessor. Proper placement of the TRF7970A, microprocessor, crystal, and RF connection or connector help facilitate this.

Avoid crossing of digital lines under RF signal lines. Also, avoid crossing of digital lines with other digital lines when possible. If the crossings are unavoidable, 90° crossings should be used to minimize coupling of the lines.

Depending on the production test plan, consider possible implementations of test pads or test vias for use during testing. The necessary pads or vias should be placed in accordance with the proposed test plan to enable easy access to those test points.

If the system implementation is complex (for example, if the RFID reader module is a subsystem of a greater system with other modules (*Bluetooth*, Wi-Fi, microprocessors, and clocks), special considerations should be taken to ensure that there is no noise coupling into the supply lines. If needed, special filtering or regulator considerations should be used to minimize or eliminate noise in these systems.

For more information/details on layout considerations, see the *TRF796x HF-RFID Reader Layout Design Guide*.

7.3 Impedance Matching TX_Out (Pin 5) to 50 Ω

The output impedance of the TRF7970A when operated at full power out setting is nominally 4 + j0 (4 Ω real). This impedance must be matched to a resonant circuit and TI recommends matching circuit from 4 Ω to 50 Ω, as commercially available test equipment (for example, spectrum analyzers, power meters, and network analyzers) are 50-Ω systems. 图 7-2 shows an impedance-matching reference circuit. 图 7-3 shows a Smith chart simulation based on this circuit. This section explains how the values were calculated.

Starting with the 4-Ω source, the process of going from 4 Ω to 50 Ω can be represented on a Smith Chart simulator (available from http://www.fritz.dellsperger.net/). The elements are combined where appropriate (see 图 7-2).

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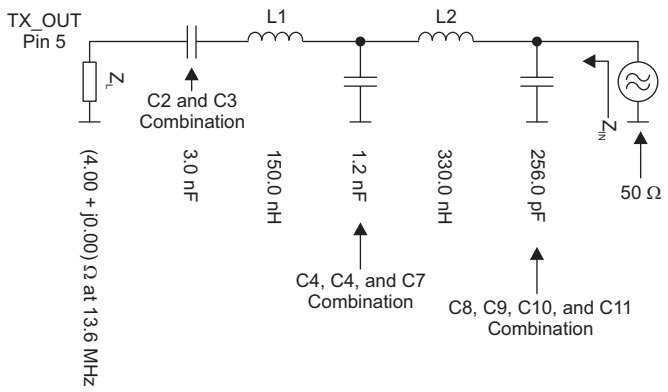


图 7-2. Impedance Matching Circuit

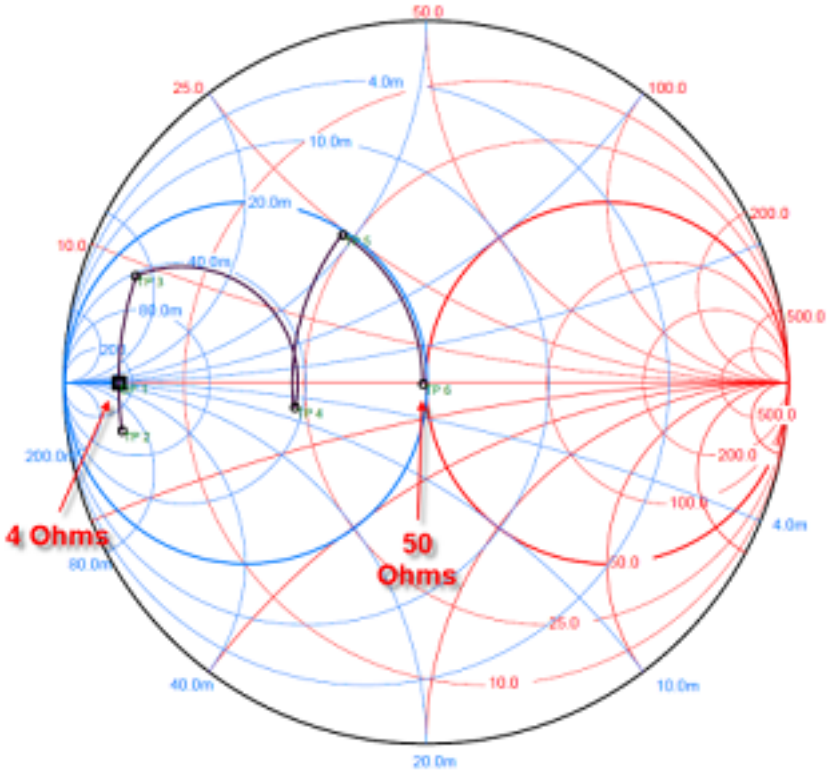


图 7-3. Smith Chart Simulation

Resulting power out can be measured with a power meter or spectrum analyzer with power meter function or other equipment capable of making a "hot" measurement. Observe maximum power input levels on test equipment and use attenuators whenever available to avoid damage to equipment. Expected output power levels under various operating conditions are shown in 表 6-25.

7.4 Reader Antenna Design Guidelines

For HF antenna design considerations using the TRF7970A, see these documents:

- *Antenna Matching for the TRF7960 RFID Reader*
- *TRF7960TB HF RFID Reader Module User's Guide*

8 器件和文档支持

8.1 入门和下一步

有关 TI NFC/RFID 器件以及有助于开发的工具和软件的更多信息，请访问 NFC/RFID 概述。

8.2 器件命名规则

为了标示产品开发周期所处的阶段，TI 为器件的部件号分配了前缀。每个商用系列产品成员都具有以下三个前缀之一：x、p 或无前缀。这些前缀代表了从工程原型（带有前缀 x）到完全合格的生产器件（无前缀）的产品开发进化阶段。

器件开发进化流程：

xTRF... – 实验器件，不一定代表最终器件的电气规格

pTRF... – 最终器件，符合最终产品的电气规格，但是未完成质量和可靠性验证

TRF... – 完全合格的生产器件

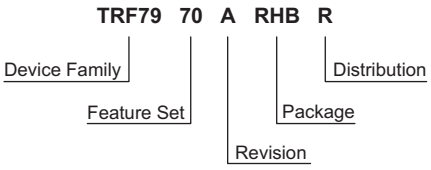
具有 **x** 或 **p** 前缀的器件供货时附带如下免责声明：

“开发的产品用于内部评估用途。”

生产器件已进行完全特性化，并且器件的质量和可靠性已经完全论证。TI 的标准保修证书适用。

预测显示原型器件的故障率大于标准生产器件。由于这些器件的预计最终使用故障率仍未定义，德州仪器 (TI) 建议不要将它们用于任何生产系统。只有合格的产品器件将被使用。

TI 器件的命名规则也包括一个带有器件系列名称的后缀。此后缀表示封装类型和可选的温度范围。图 8-1 提供了解读完整器件名称的图例。



Device Family	TRF79 = NFC/RFID Transceiver
Feature Set	70 = Feature Set
Revision	A = Silicon Revision
Package	See Packaging Information or www.ti.com/package
Distribution	R = Large Reel T = Small Reel

图 **8-1.** 器件命名规则

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8.3 工具与软件

设计套件和评估模块

NFC 收发器附加目标板模块 TRF7970ATB 评估模块让软件应用开发人员能够熟悉所选的德州仪器 (TI) 嵌入式微控制器平台上的 TRF7970A 多协议全集成 13.56MHz NFC/HF RFID IC 的功能，而无需担心射频部分。

NFC 收发器 Booster Pack 插件模块 第三方提供商 DLP Design 所提供的 NFC/RFID BoosterPack 插件模块 (DLP-7970ABP) 是一款附加电路板，旨在满足所有 TI MCU LaunchPad 开发套件的需求。此 BoosterPack 插件模块能够让软件应用开发人员熟悉所选的 TI 嵌入式微控制器平台上的 TRF7970A 多协议全集成式 13.56MHz NFC 和 HF RFID IC 的功能，而无需担心射频部分的开发。

NFC 收发器评估模块 TRF7970AEVM 是一种自成一体的开发平台，可用于评估 NFC 收发器 TRF7970A 的性能。TRF7970A 是一款多协议全集成式 13.56MHz NFC/RFID 收发器 IC。该评估模块与这个 IC 一起可用于开发和评估自定义固件、客户设计的天线以及潜在应答器，适用于各种 NFC/RFID 应用。

8.4 文档支持

以下文档对 TRF7970A 器件进行了介绍。www.ti.com.cn 网站上提供了这些文档的副本。

接收文档更新通知

要接收文档更新通知（包括器件勘误表），请转至 ti.com.cn 上相关器件的产品文件夹（例如 TRF7970A）。单击右上角的“提醒我”(Alert me) 按钮。点击后，您将每周定期收到已更改的产品信息（如果有的话）。有关更改的详细信息，请查阅已修订文档的修订历史记录。

勘误

《TRF7970A 器件勘误表》 介绍了 TRF7970A 的功能技术规格的已知例外情况。

应用手册

《在断电模式下最大限度减小 TRF79xx 电流使用量》 此应用报告为 TRF79xx 器件系列（TRF796x、TRF796xA 和 TRF7970A）提供了电路和固件设计建议，以便减少断电模式下的电流消耗。此手册种考虑了各种设计，并根据这些设计的电流消耗进行了分析。此应用报告特别强调了由电池供电的双电压系统。

《使用 TRF7970A 的 NFC/HF RFID 读/写器》 近场通信 (NFC) 市场正在涌入医疗、消费品、零售、工业、汽车和智能电网等多个领域。读/写器是 TRF7970A 支持的三种工作模式之一。使用读/写器模式时，用户可以配置 TRF7970A 以读取类型 2、类型 3、类型 4A、类型 4B 和类型 5 标签平台（也称为应答器）。标签可以存储 NFC 数据交换格式 (NDEF) 消息或事先定义的专有数据。此应用报告介绍了读/写器模式的基本概念以及如何针对每种支持的技术正确配置 TRF7907A 收发器。

《TRF7970A NFC 读取器天线多路复用》 此应用报告介绍了使用单个 TRF7970A NFC 收发器 IC 实现多个读取器天线的情况。为了进行演示，此报告中使用了带有 TRF7970A BoosterPack 插件模块的 MSP430F5529 LaunchPad 开发套件。该演示支持 ISO/IEC 15693 以及 ISO/IEC 14443 A 和 B 通信协议。

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《使用 **MSP430** 和 **TRF79xxA** 进行 **NFC/RFID** 读取器超低功耗卡存在检测》NFC 和 RFID 读取器电池供电型 应用 必须具有事先定义和限定的能量消耗预算以及低成本才能实现产品。多年来，卡存在检测领域已涌现多种技术和策略，试图解决这两个问题。此应用报告的目的是进一步优化这些技术和策略，方法是在现有设计中增加一个简单电路和小型固件控制逻辑环路，从而在原先确定的卡检测解决方案的基础上带来巨大改进。

8.5 社区资源

下列链接能连接到 TI 社区资源。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

TI E2E™ 社区

***TI** 工程师间 **(E2E)** 社区*。 此社区的创建目的在于促进工程师之间的协作。在 e2e.ti.com 中，您可以咨询问题、分享知识、拓展思路并与同行工程师一道帮助解决问题。

8.6 商标

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG.
MIFARE is a trademark of NXP Semiconductors.
FeliCa is a trademark of Sony Corporation.
Wi-Fi is a registered trademark of Wi-Fi Alliance.

8.7 静电放电警告

ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。 精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms and definitions.

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9 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。这些数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TRF7970ARHBR	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	TRF 7970A
TRF7970ARHBR.B	Active	Production	VQFN (RHB) | 32	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	TRF 7970A
TRF7970ARHBT	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	TRF 7970A
TRF7970ARHBT.B	Active	Production	VQFN (RHB) | 32	250 | SMALL T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 110	TRF 7970A

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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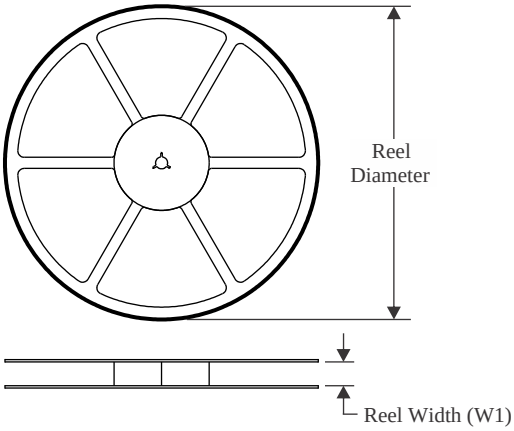
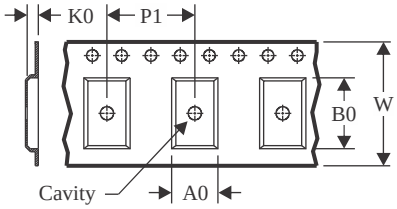
TAPE AND REEL INFORMATION

REEL DIMENSIONS

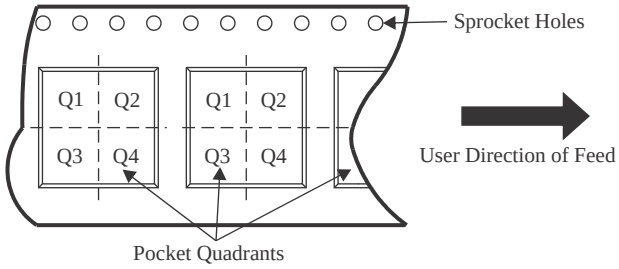


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

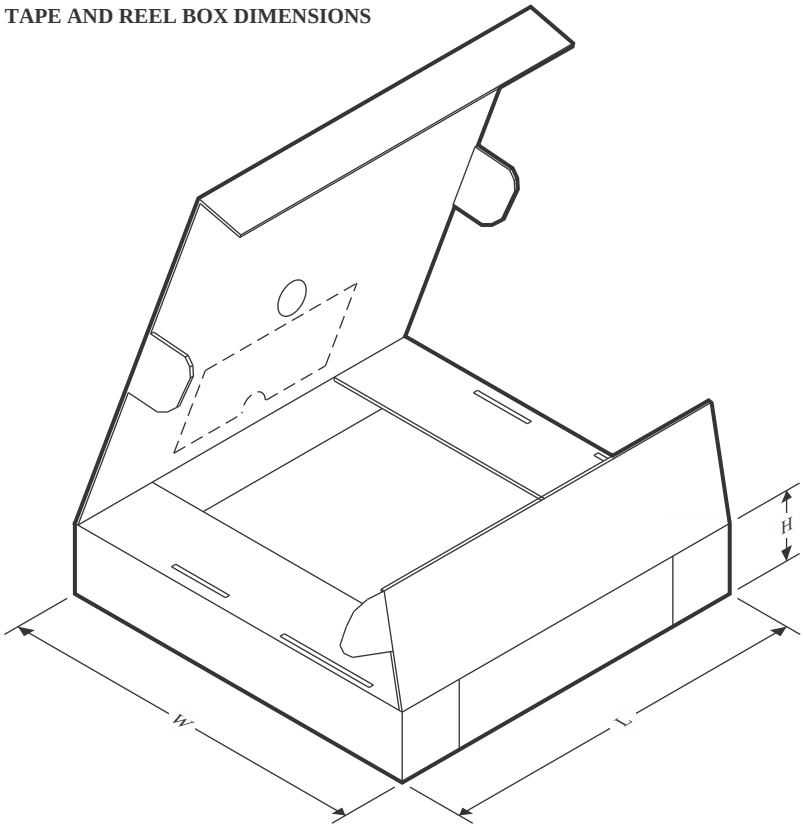
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRF7970ARHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TRF7970ARHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRF7970ARHBR	VQFN	RHB	32	3000	356.0	356.0	35.0
TRF7970ARHBT	VQFN	RHB	32	250	210.0	185.0	35.0

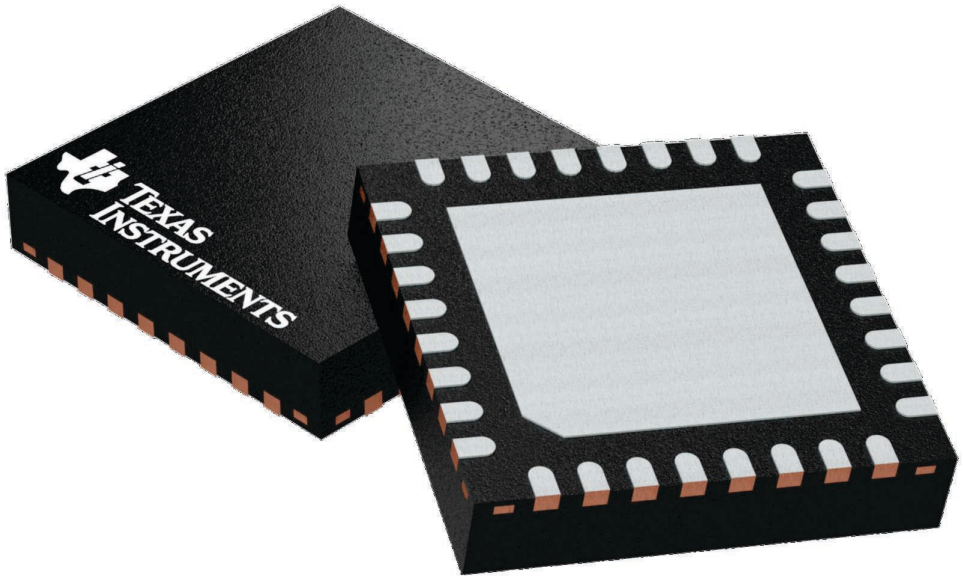
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

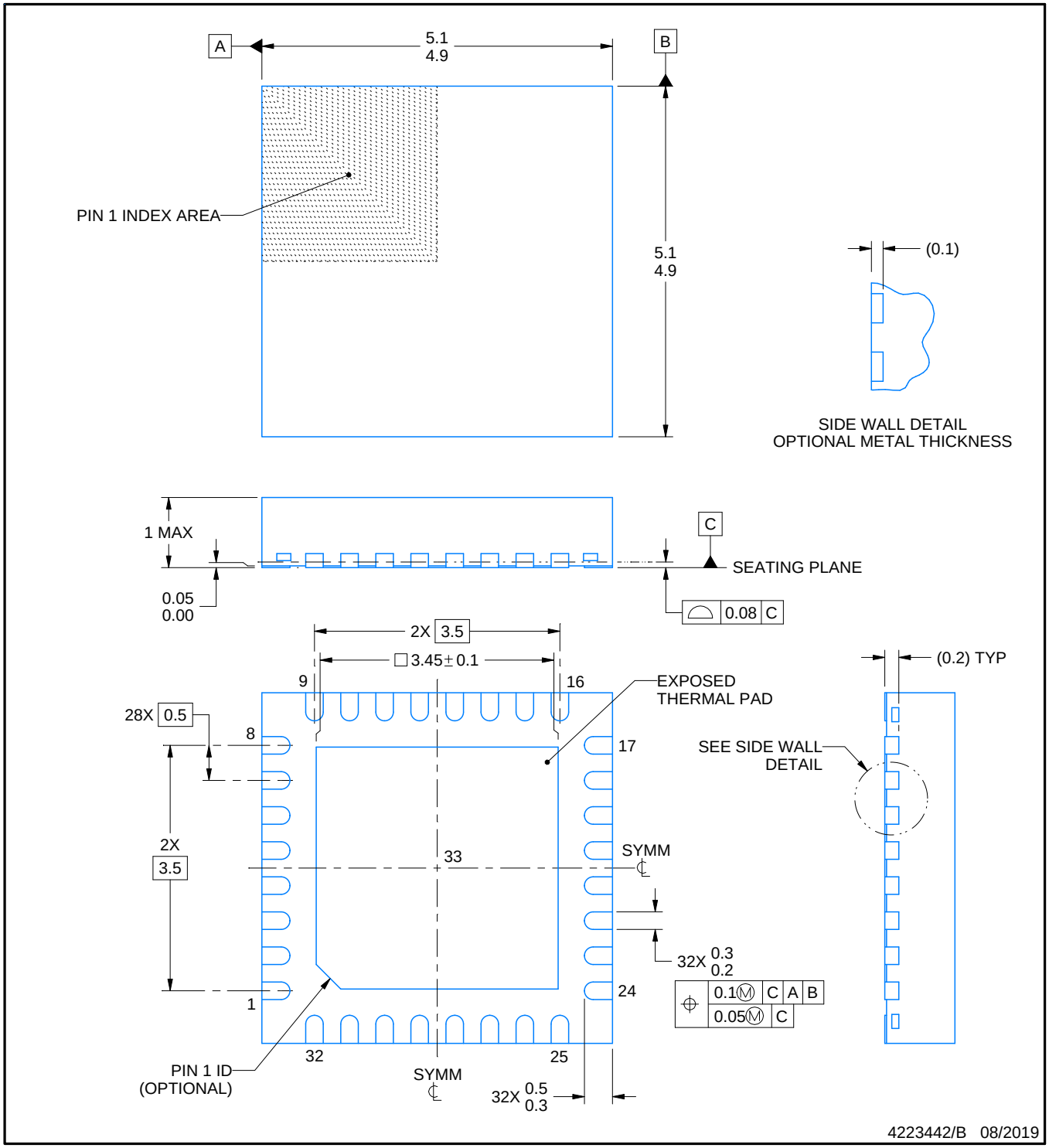
4224745/A

RHB0032E

PACKAGE OUTLINE

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

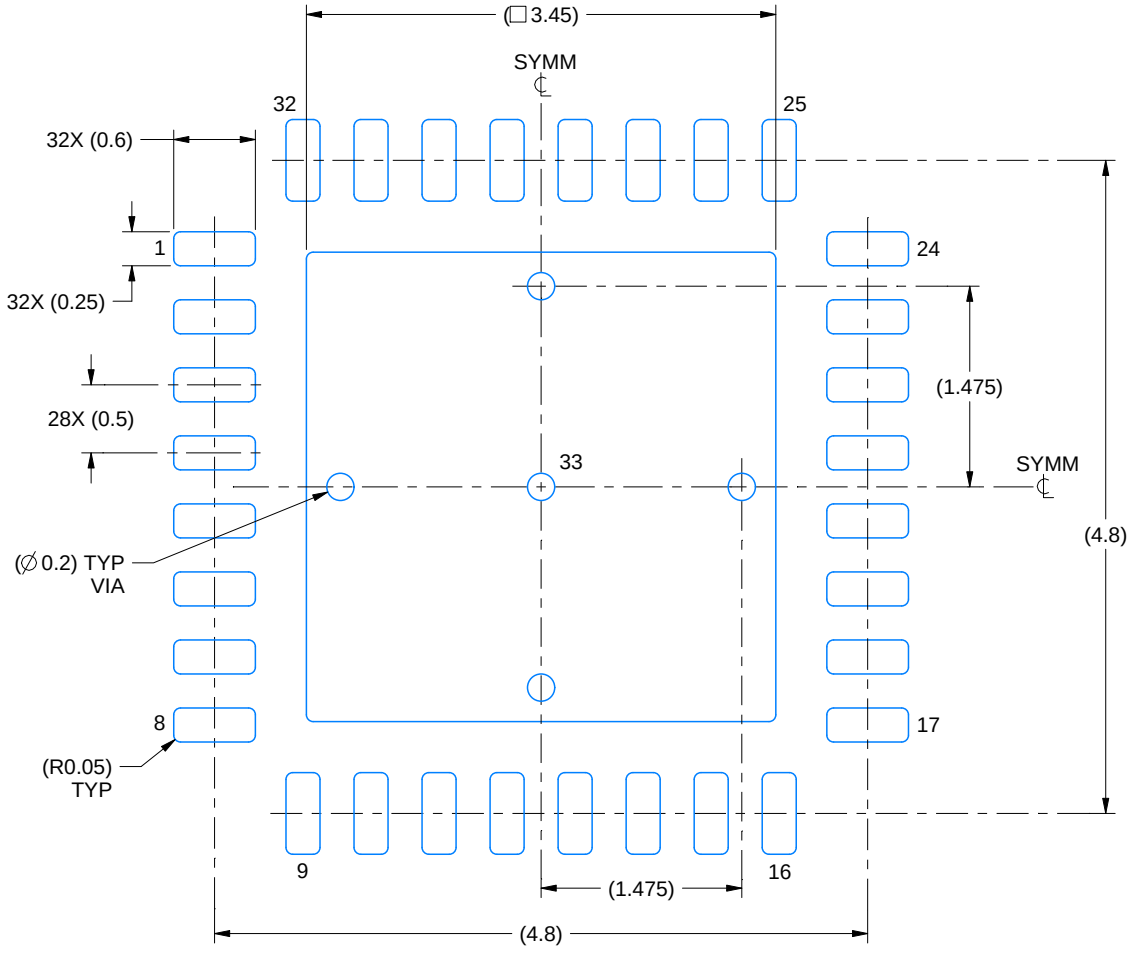
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

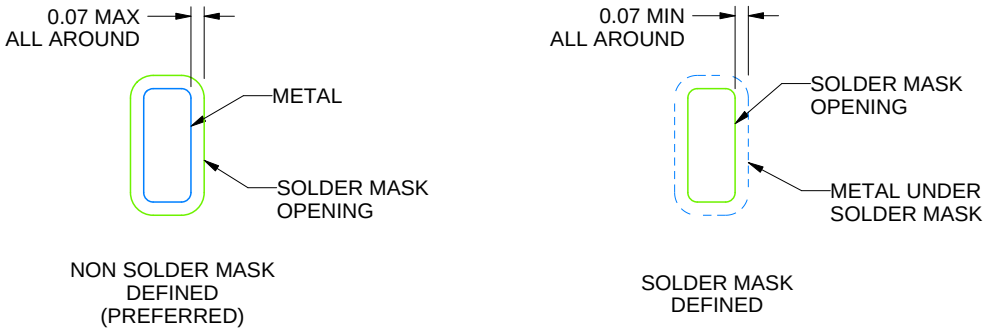
RHB0032E

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
SCALE:18X

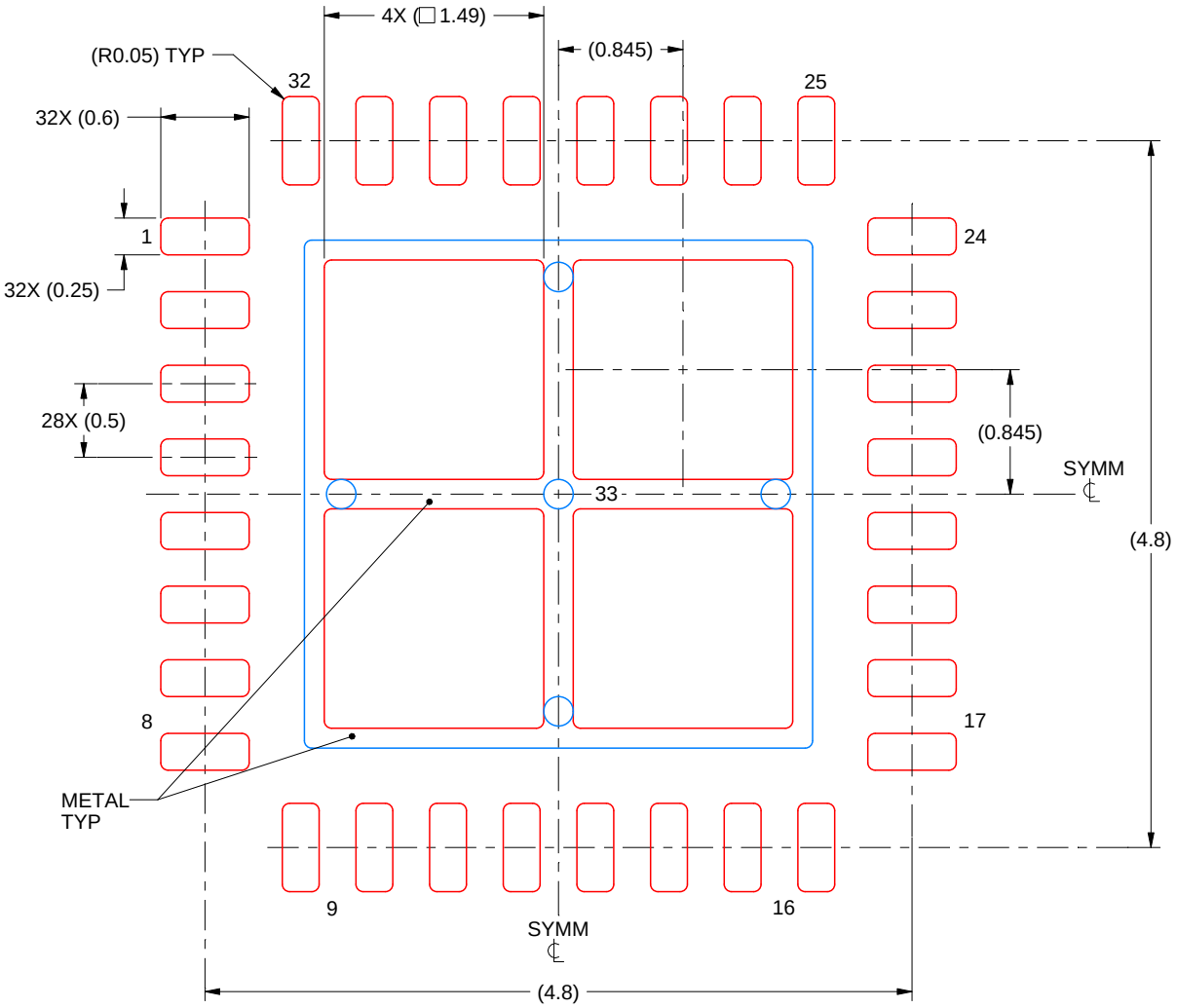


SOLDER MASK DETAILS

4223442/B 08/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要通知和免责声明

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