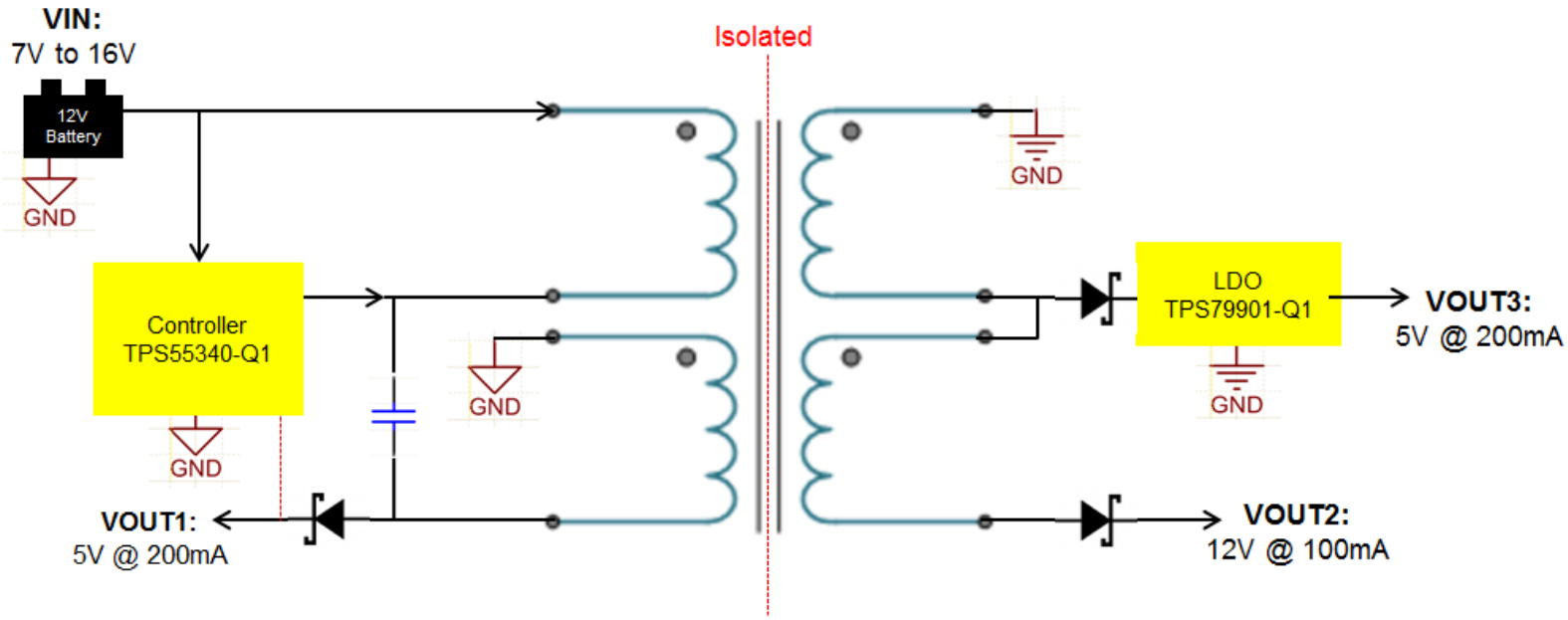
PMP20550 Test Report

The following test report is for the PMP20550 board. This board is a SEPIC with two additional isolated outputs.

The contents of this test report are as follows:

A. Start Up
B. Output DC Levels for all Loading Conditions
C. Output Ripple
D. Switch Node
E. Transient Response
F. Bode Analysis
G. Efficiency
H. Thermal
I. Board Image

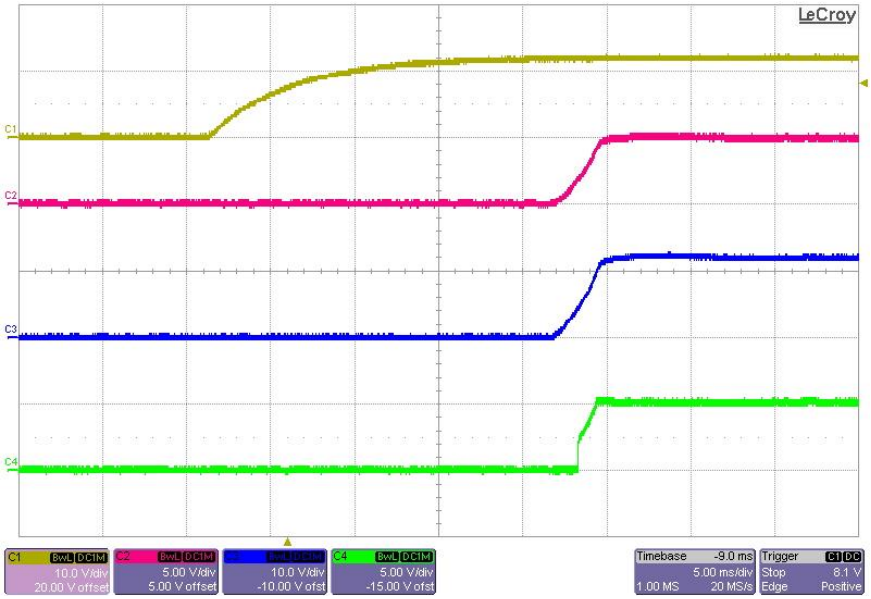


Note: In the following report the output voltage rails will be referred to as VOUT1, VOUT2, and VOUT3.

A – Start Up

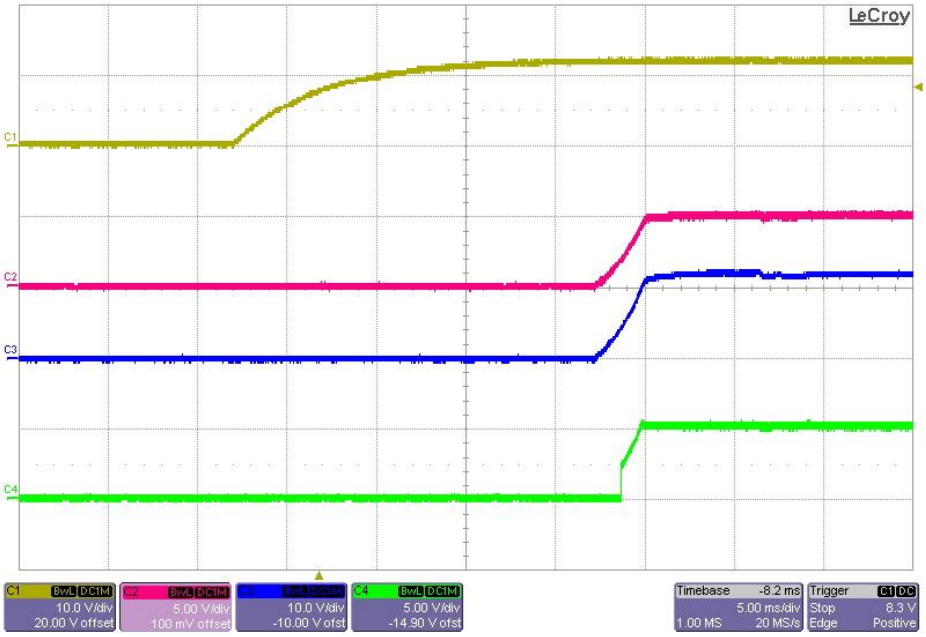
The photo below shows the start up for the board. The outputs are all at no load. The input voltage is 12V.

Channel 1 – Yellow: Input Voltage – (10V/Division; DC Coupled; BWL)
Channel 2 – Pink: VOUT1 – (5V/Division; DC Coupled; BWL)
Channel 3 – Blue: VOUT2 – (10V/Division; DC Coupled; BWL)
Channel 4 – Green: VOUT3 – (5V/Division; DC Coupled; BWL)



The photo below shows the start up for the board. The outputs are all at full load (VOUT1 @ 200mA, VOUT2 @ 100mA, and VOUT3 @ 200mA). The input voltage is 12V.

Channel 1 – Yellow: Input Voltage – (10V/Division; DC Coupled; BWL)
Channel 2 – Pink: VOUT1 – (5V/Division; DC Coupled; BWL)
Channel 3 – Blue: VOUT2 – (10V/Division; DC Coupled; BWL)
Channel 4 – Green: VOUT3 – (5V/Division; DC Coupled; BWL)



B – Output DC Levels

The chart below shows the output voltage DC levels for VOUT1, VOUT2, and VOUT3 for all possible loading combinations.

VIN	VOUT 1	IOUT 1 (mA)	VOUT 2	IOUT 2 (mA)	VOUT 3	IOUT 3 (mA)
No Load Conditions						
7	5.03	0	11.70	0	5.06	0
12	5.03	0	11.70	0	5.06	0
16	5.03	0	11.71	0	5.06	0
Full Load Conditions						
7	5.03	200	11.69	100	5.06	200
12	5.03	200	11.76	100	5.06	200
16	5.03	200	11.78	100	5.06	200
All Combos						
7	5.03	0	11.47	100	5.06	0
7	5.03	0	11.59	0	5.06	200
7	5.03	0	11.28	100	5.06	200
7	5.03	200	11.98	0	5.06	0
7	5.03	200	11.78	100	5.06	0
7	5.03	200	11.93	0	5.06	200
12	5.03	0	11.51	100	5.06	0
12	5.03	0	11.63	0	5.06	200
12	5.03	0	11.41	100	5.06	200
12	5.03	200	11.97	0	5.06	0
12	5.03	200	11.81	100	5.06	0
12	5.03	200	11.94	0	5.06	200
16	5.03	0	11.53	100	5.06	0
16	5.03	0	11.64	0	5.06	200
16	5.03	0	11.46	100	5.06	200
16	5.03	200	11.97	0	5.06	0
16	5.03	200	11.82	100	5.06	0
16	5.03	200	11.95	0	5.06	200

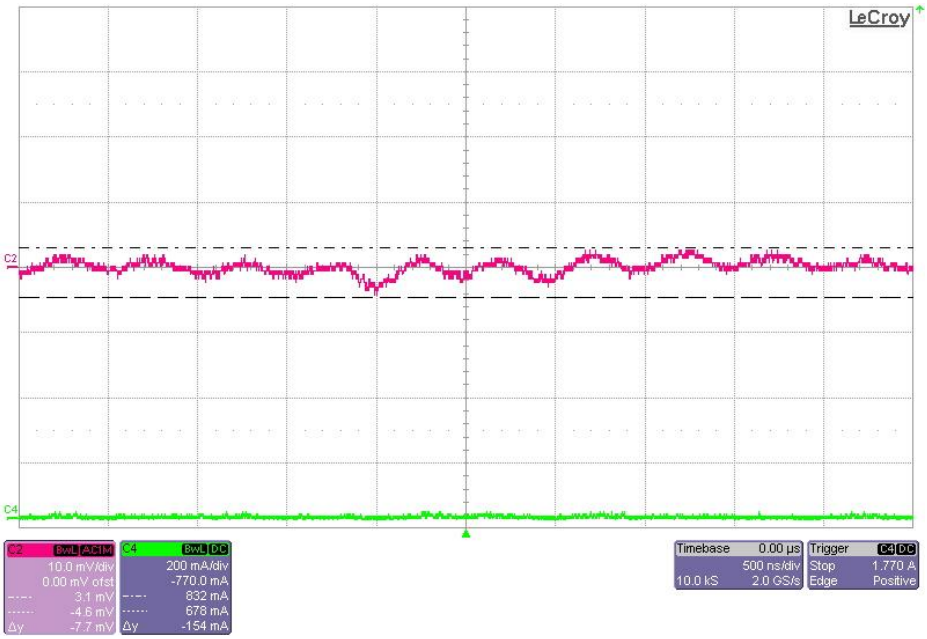
VOUT1 DC Fluctuation: 0%
VOUT2 DC Fluctuation: 5.8%
VOUT3 DC Fluctuation: 0%

Note: The highest the voltage into the LDO reaches is 6.22V (7VIN, IOUT1 = 0.2A, IOUT2 = 0A, IOUT3 = 0.2A).

C – Output Ripple

The photos below show the output ripple. The output is at **no load**. The input voltage is 12V.

Channel 1 – Pink: VOUT1 Output Voltage – (10mV/Division; AC Coupled; BWL)
Channel 2 – Green: Output Current – (200mA/Division; DC Coupled; BWL)

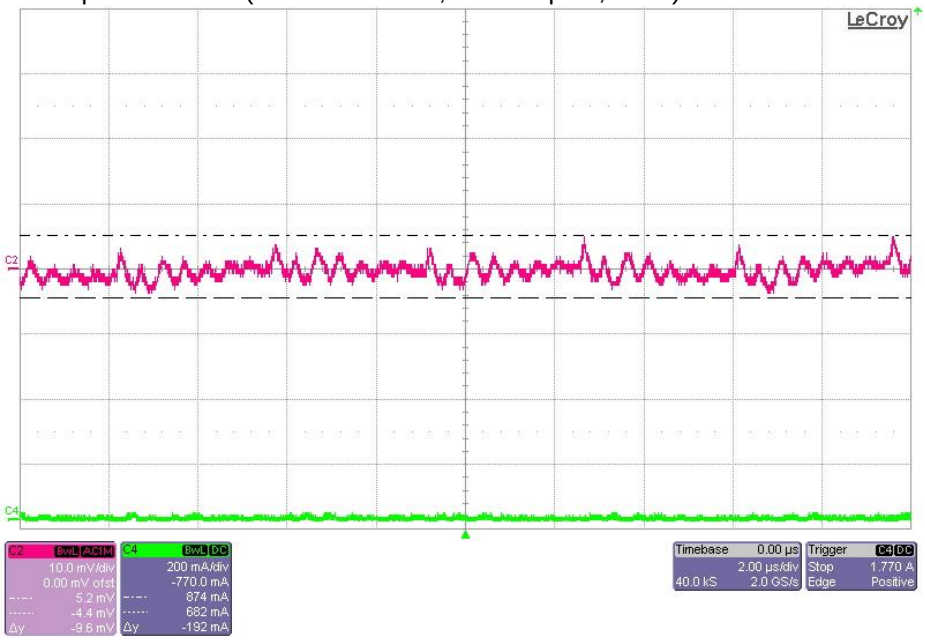


VOUT1 Ripple – No Load – 7.7mVpp = 0.153 %

Channel 1 – Pink: VOUT2 Output Voltage – (10mV/Division; AC Coupled; BWL)
Channel 2 – Green: Output Current – (200mA/Division; DC Coupled; BWL)

VOUT2 Ripple – No Load –8.8mVpp = 0.07%

Channel 1 – Pink: VOUT3 Output Voltage – (10mV/Division; AC Coupled; BWL)
Channel 2 – Green: Output Current – (200mA/Division; DC Coupled; BWL)



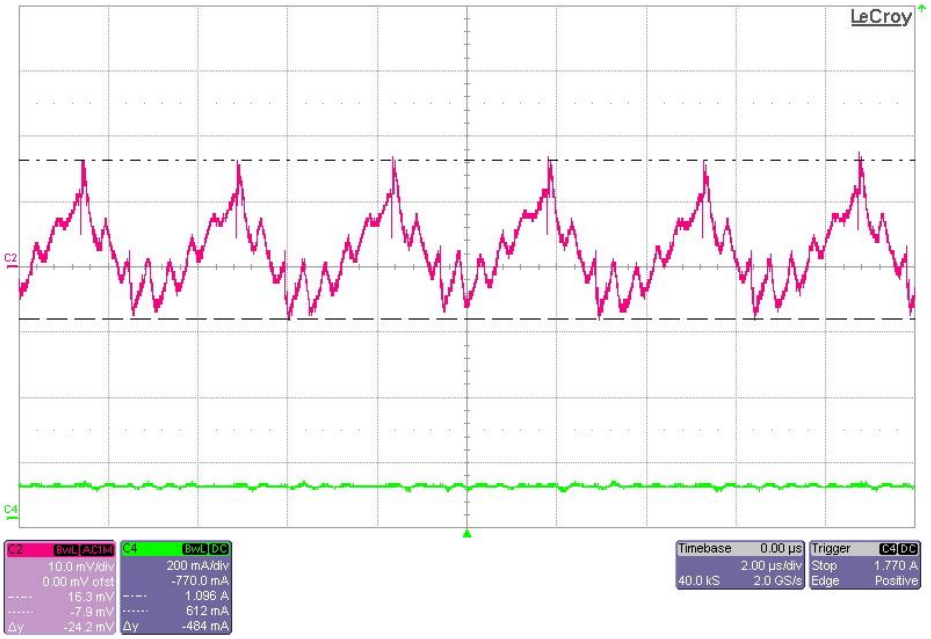
VOUT3 Ripple – No Load – 9.6mVpp = 0.18 %

The photos below show the output ripple. The output is loaded with an electronic load at the **full load** for all rails (VOUT1 @ 200mA, VOUT2 @ 100mA, and VOUT3 @ 200mA). The input voltage is 12V.

Channel 1 – Pink: VOUT1 Output Voltage – (10mV/Division; AC Coupled; BWL)
Channel 2 – Green: Output Current – (200mA/Division; DC Coupled; BWL)

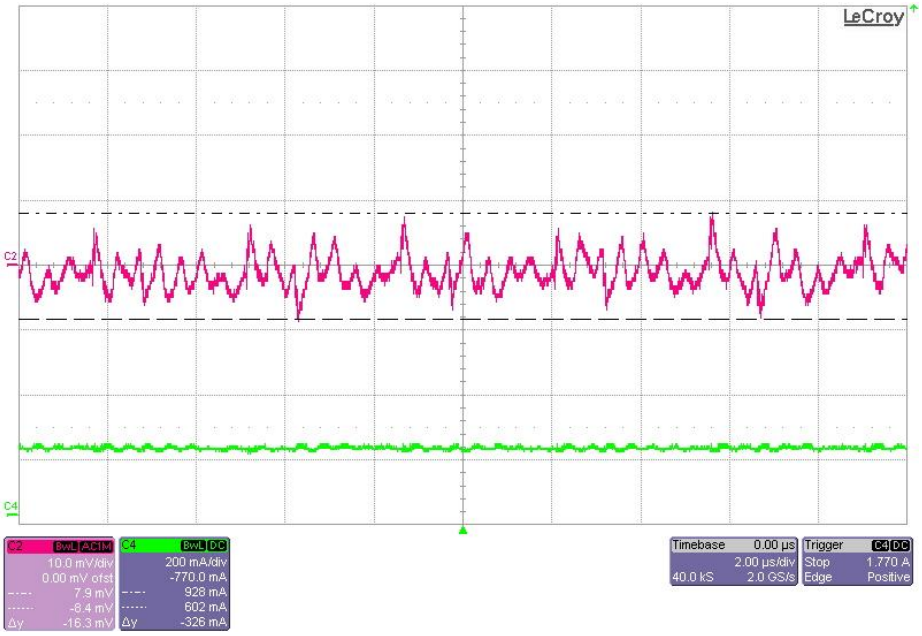
VOUT1 Ripple – Full Load – 24.7mVpp = 0.49 %

Channel 1 – Pink: VOUT2 Output Voltage – (10mV/Division; AC Coupled; BWL)
Channel 2 – Green: Output Current – (200mA/Division; DC Coupled; BWL)



VOUT2 Ripple – Full Load – 24.2mVpp = 0.2 %

Channel 1 – Pink: VOUT3 Output Voltage – (10mV/Division; AC Coupled; BWL)
Channel 2 – Green: Output Current – (200mA/Division; DC Coupled; BWL)

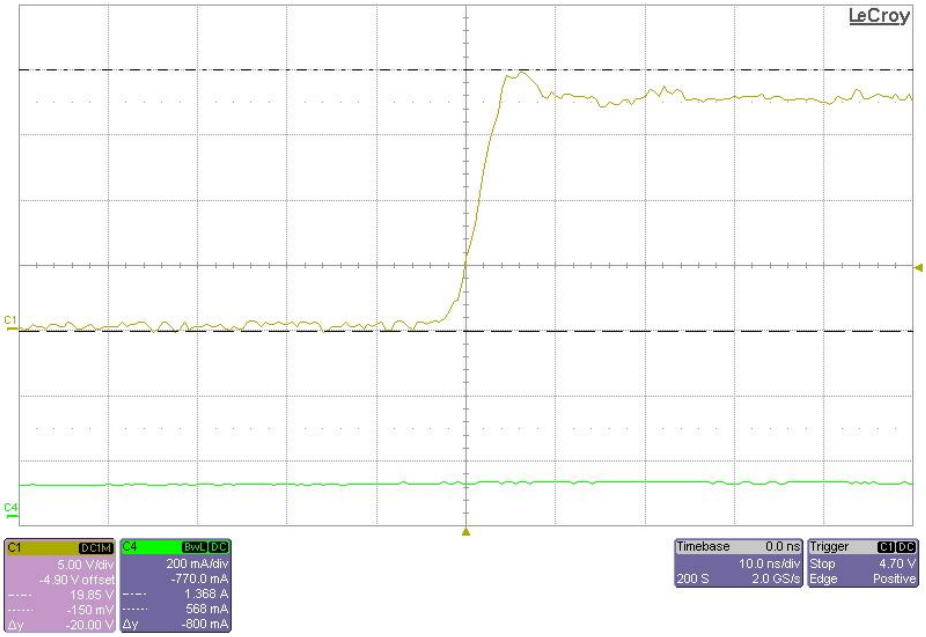


VOUT3 Ripple – Full Load – 16.3mVpp = 0.32 %

D – Switch Node

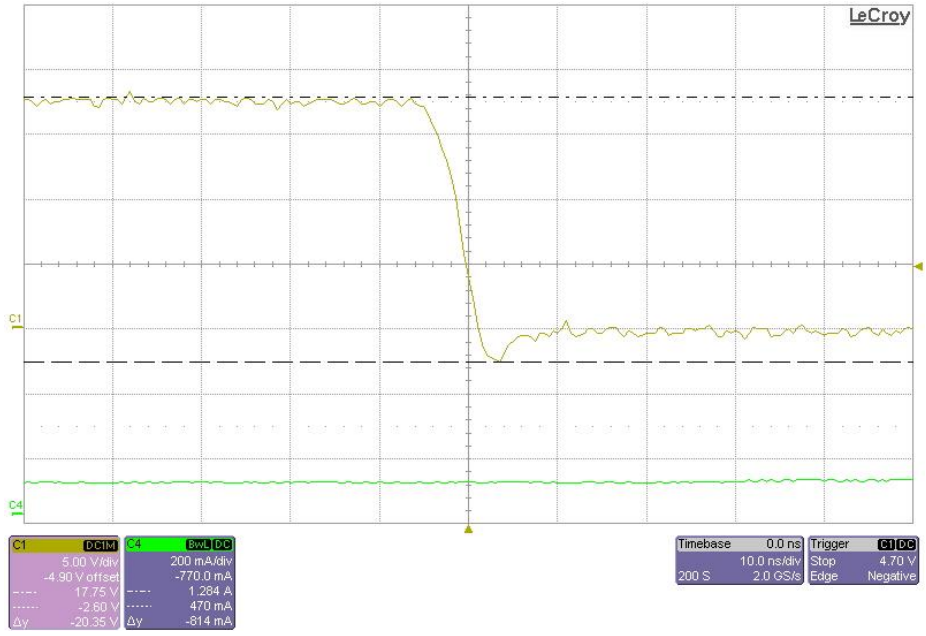
The photos below show the switch node waveform. The output is loaded with an electronic load at the full load for all rails (VOUT1 @ 200mA, VOUT2 @ 100mA, and VOUT3 @ 200mA). The input voltage is 12V.

Channel 1 – Yellow: Switch Node Voltage – (5V/Division; DC Coupled)
Channel 2 – Green: Output Current on VOUT1 – (200mA/Division; DC Coupled; BWL)



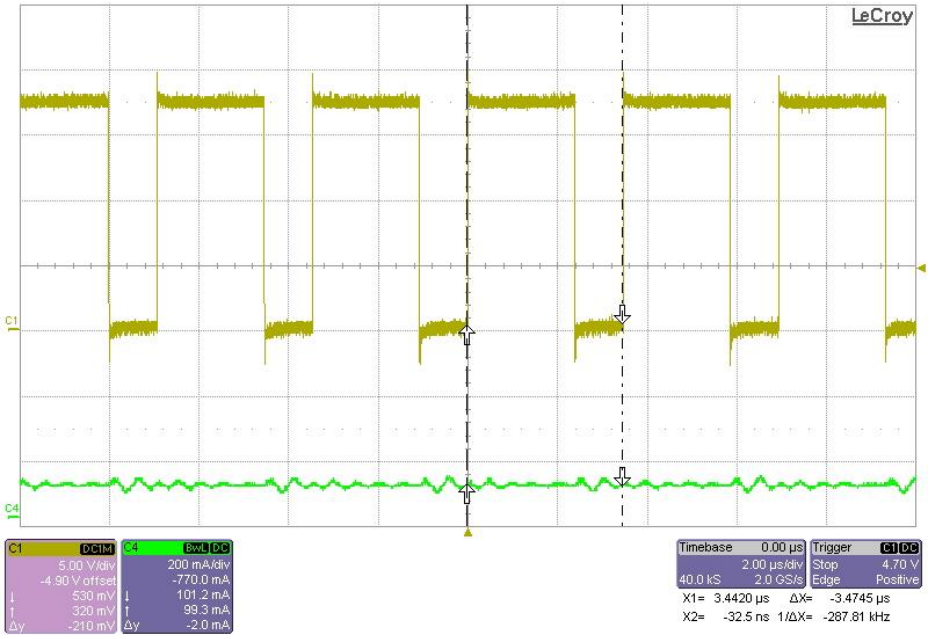
Switch Node Rising Edge

Channel 1 – Yellow: Switch Node Voltage – (5V/Division; DC Coupled)
Channel 2 – Green: Output Current on VOUT1 – (200mA/Division; DC Coupled; BWL)



Switch Node Falling Edge

Channel 1 – Yellow: Switch Node Voltage – (5V/Division; DC Coupled)
Channel 2 – Green: Output Current on VOUT1 – (200mA/Division; DC Coupled; BWL)

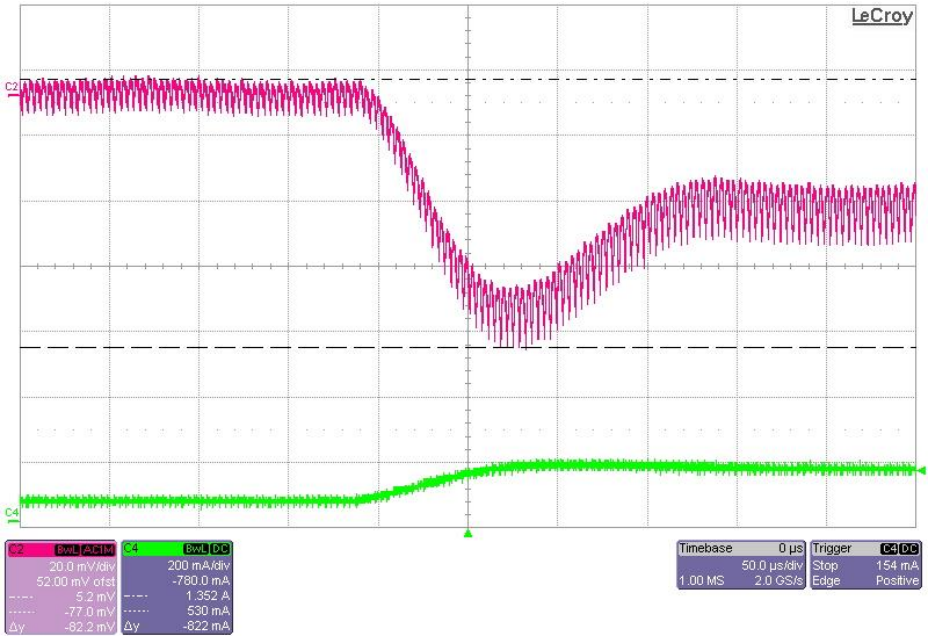


Switch Node Cycling – 287.8 kHz

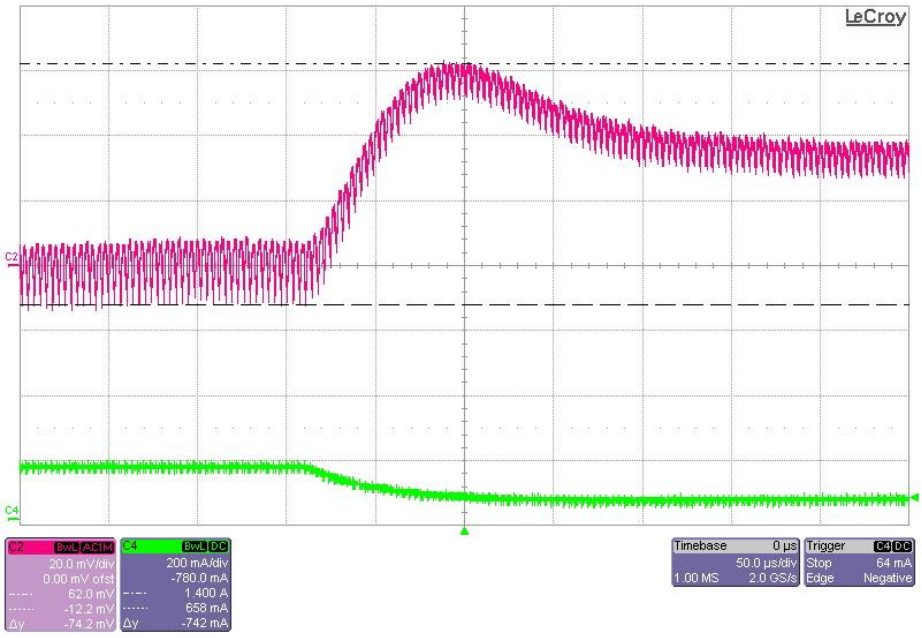
E – Transient

The photos below show the output voltage fluctuation as the load is pulsed from 25% to 75%. The input voltage is 12V. The other two outputs are **fully loaded** during the load transients on one output.

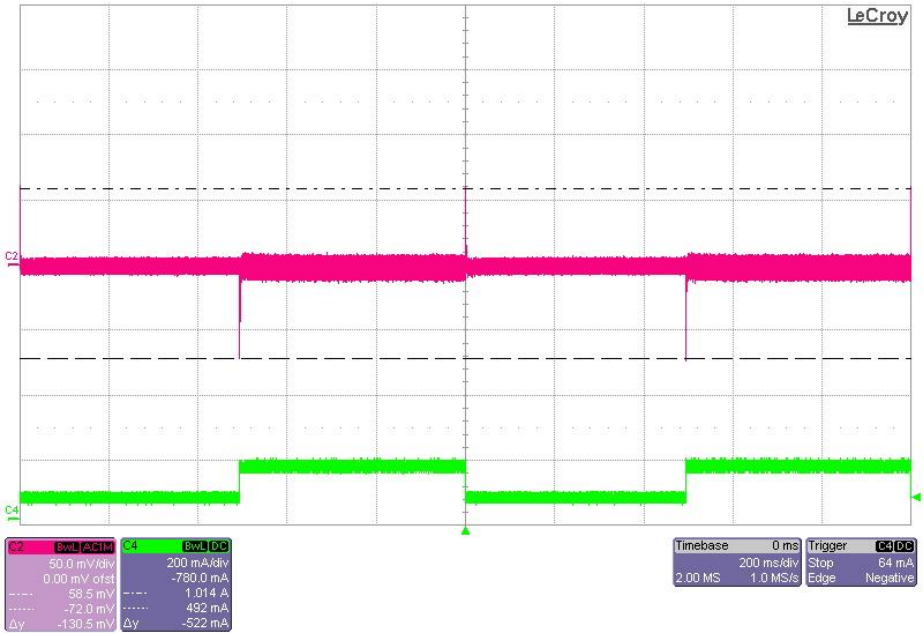
Channel 1 – Pink: Output Voltage – (Varies; AC Coupled; BWL)
Channel 2 – Green: Output Current – (Varies; DC Coupled; BWL)



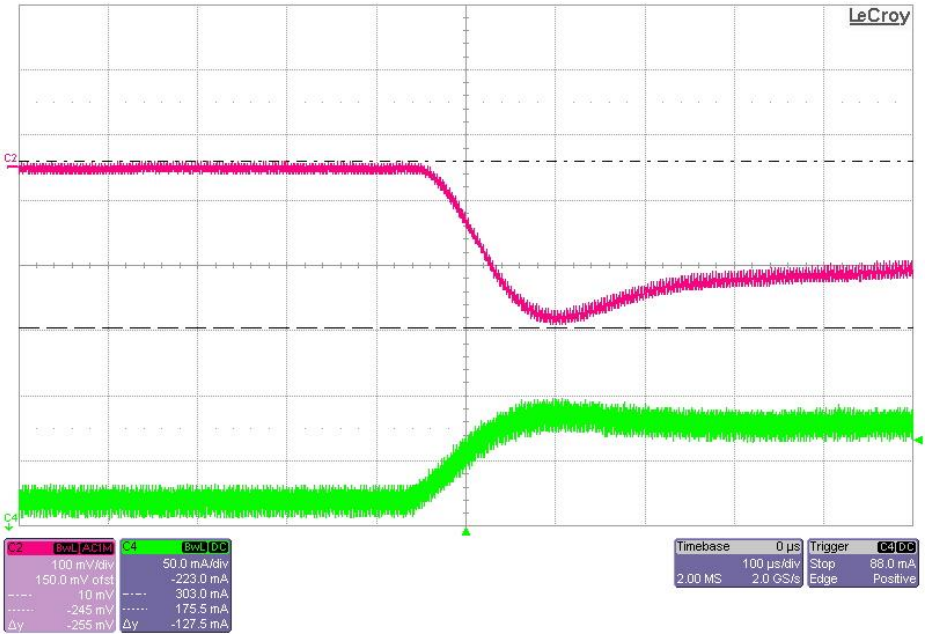
VOUT1 – Rising Edge – 82.2mV = 1.64%



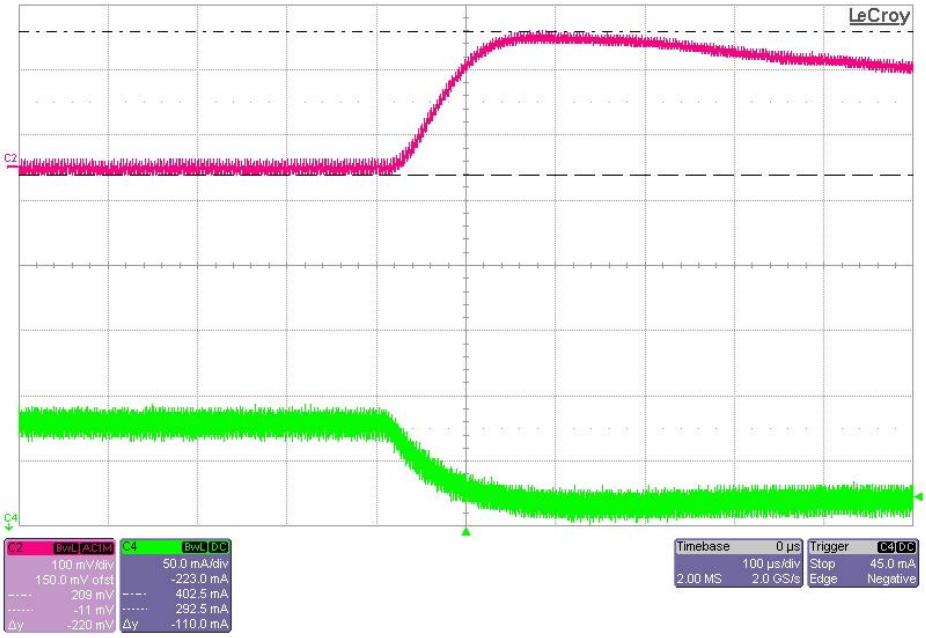
VOUT1 – Falling Edge – 74.2mV = 1.48%



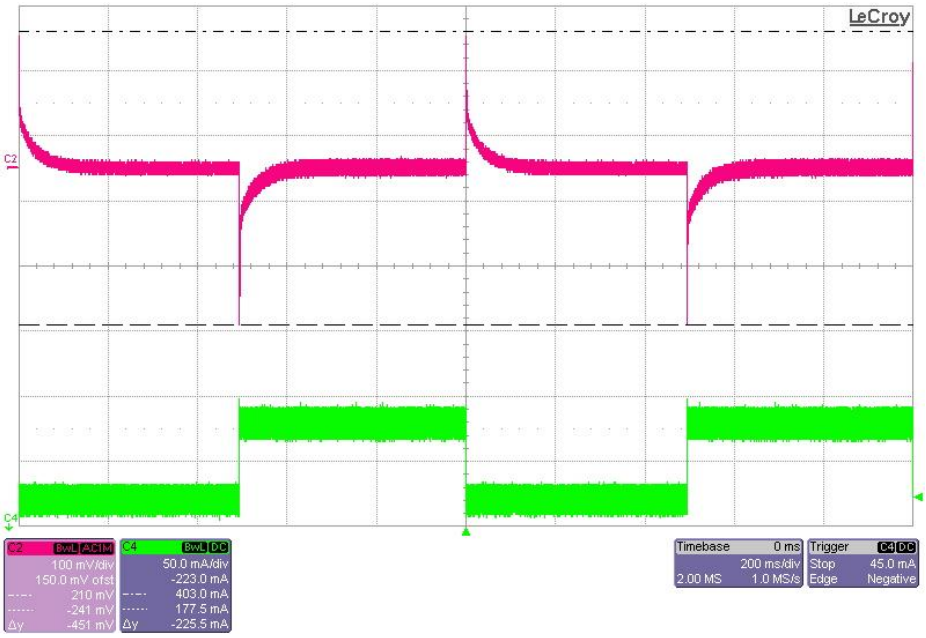
VOUT1 – Cycling



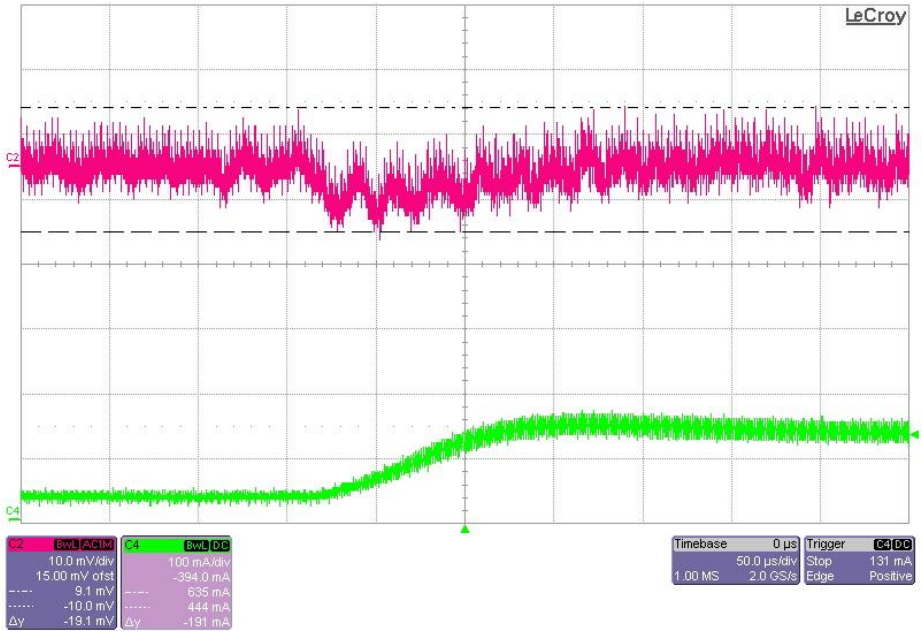
VOUT2 – Rising Edge – 255mV = 2.1%



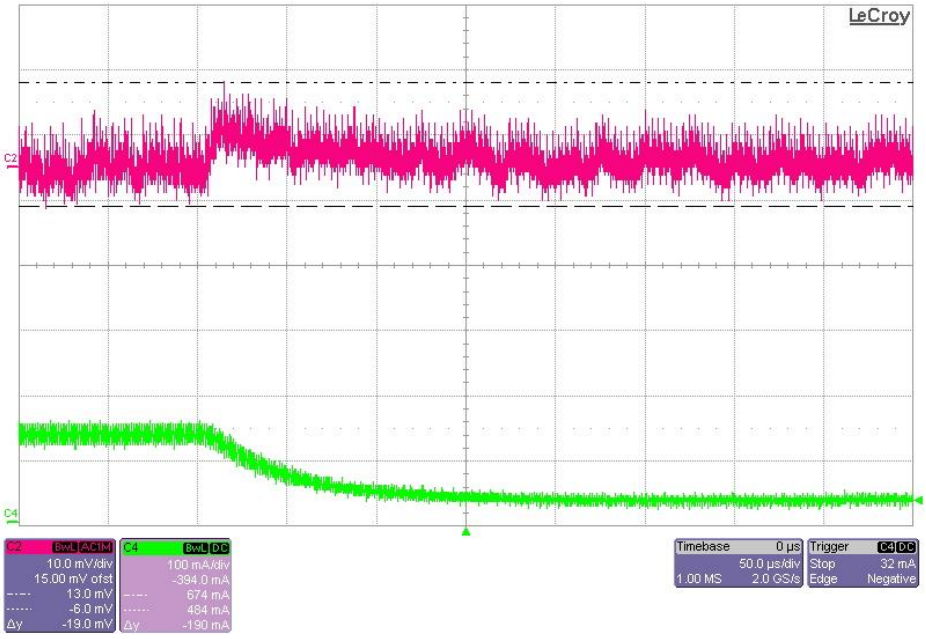
VOUT2- Falling Edge – 220mV = 1.83%



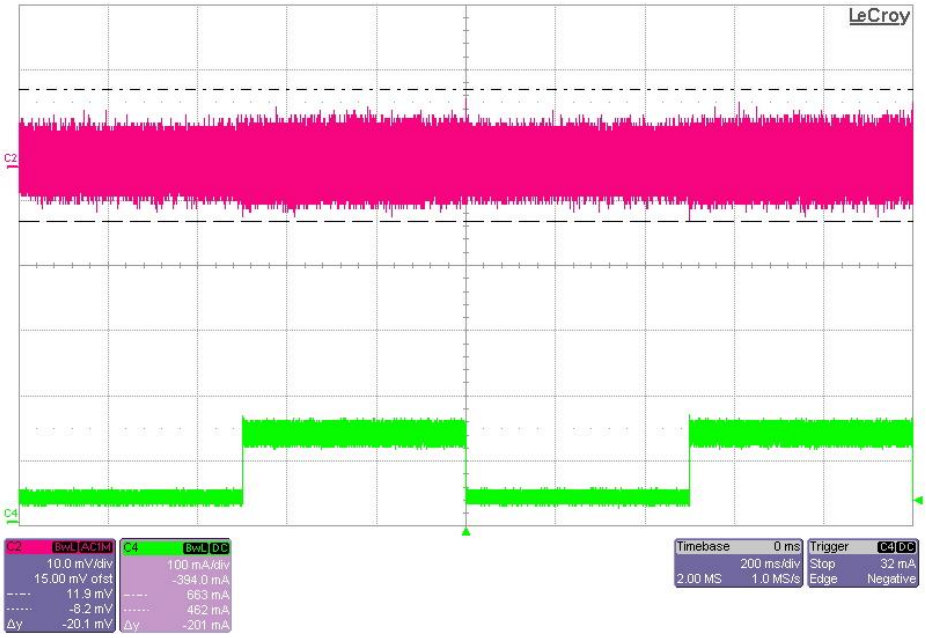
VOUT2 - Cycling



VOUT3 – Rising Edge – 19.1mV = 0.38%

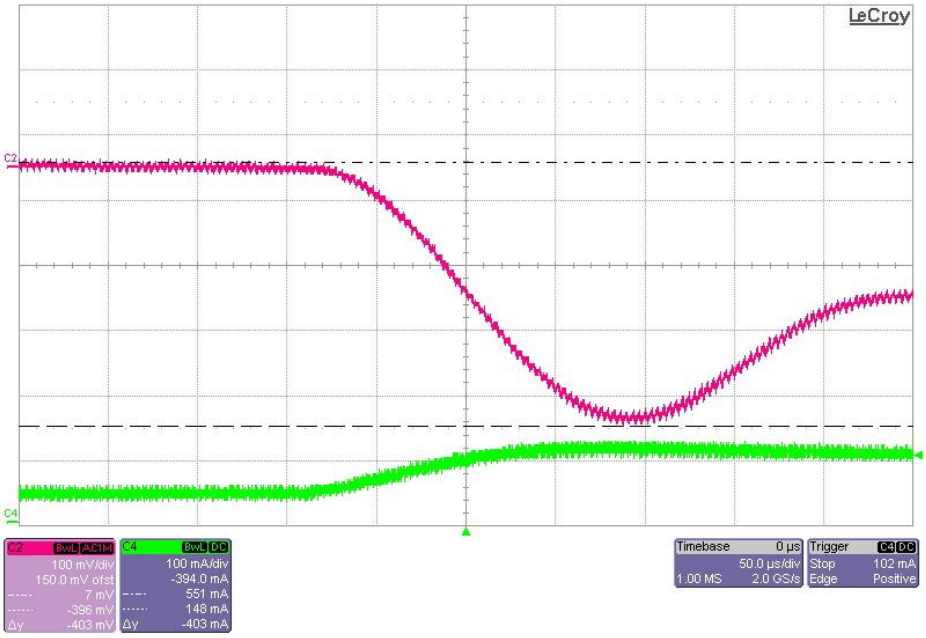


VOUT3 – Falling Edge – 19.0mV = 0.38%

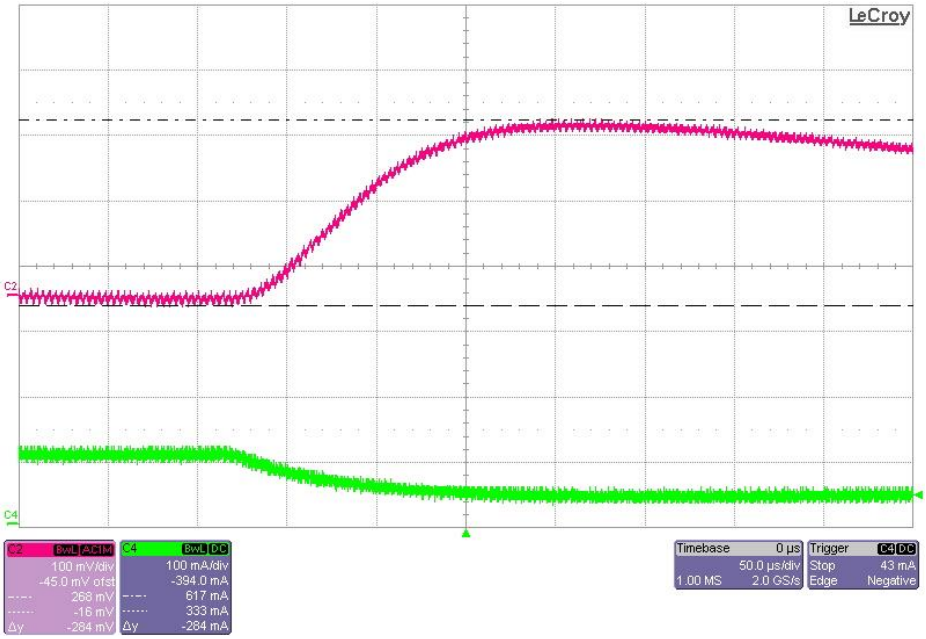


VOUT3 – Cycling

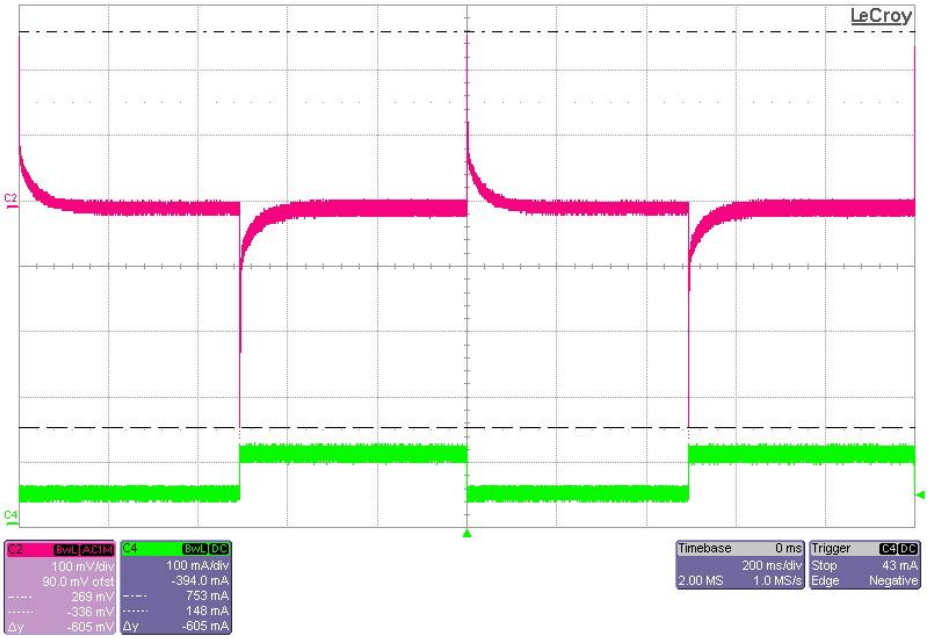
The photos below show the output voltage fluctuation as the load is pulsed from 25% to 75%. The input voltage is 12V. The other two outputs are at **no load** during the load transients on one output.



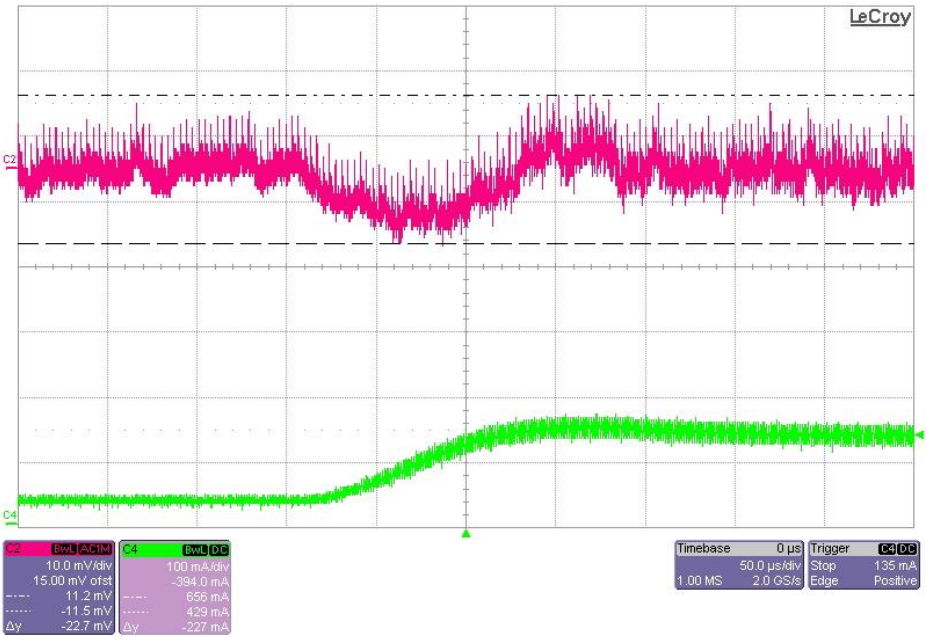
VOUT2 – Rising Edge – 403mV = 3.33%



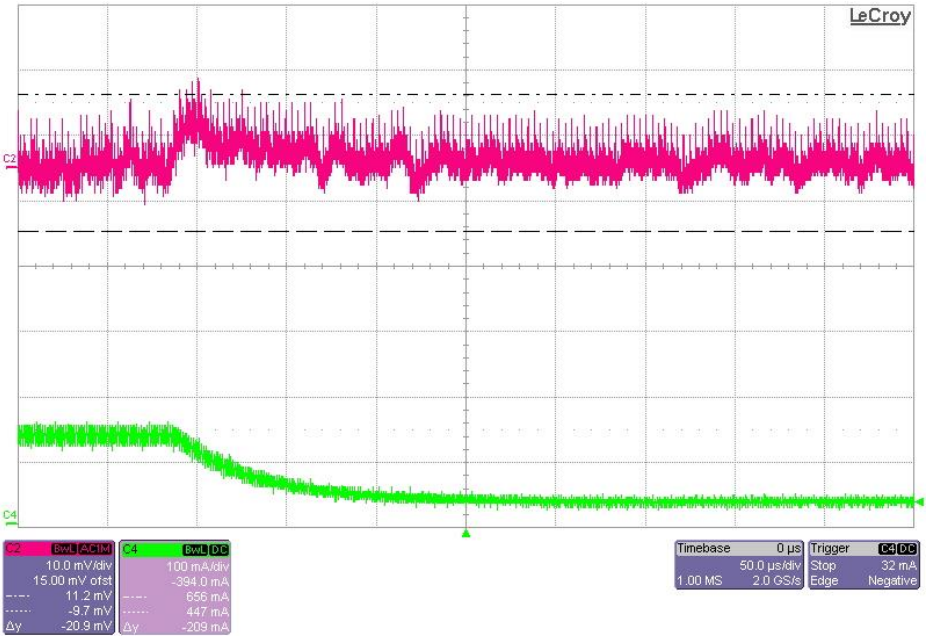
VOUT2 – Falling Edge – 284mV = 2.36%



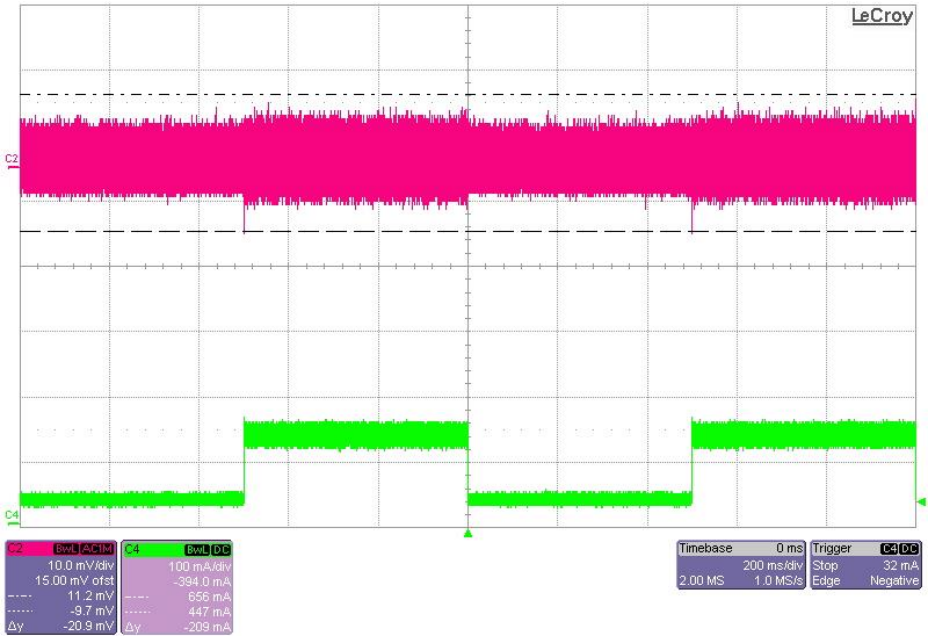
VOUT 2 - Cycling



VOUT3 – Rising Edge – 22.7mV = 0.45%



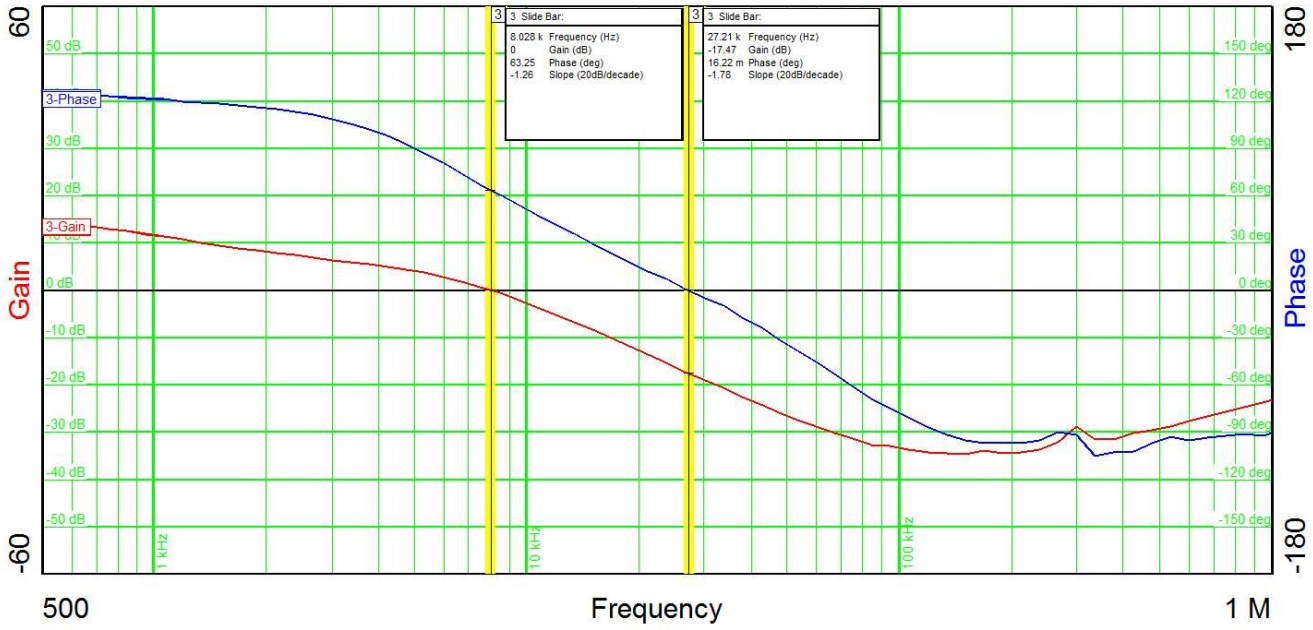
VOUT3 – Falling Edge – 20.9mV = 0.41%



VOUT3 – Cycling

F – Bode Analysis

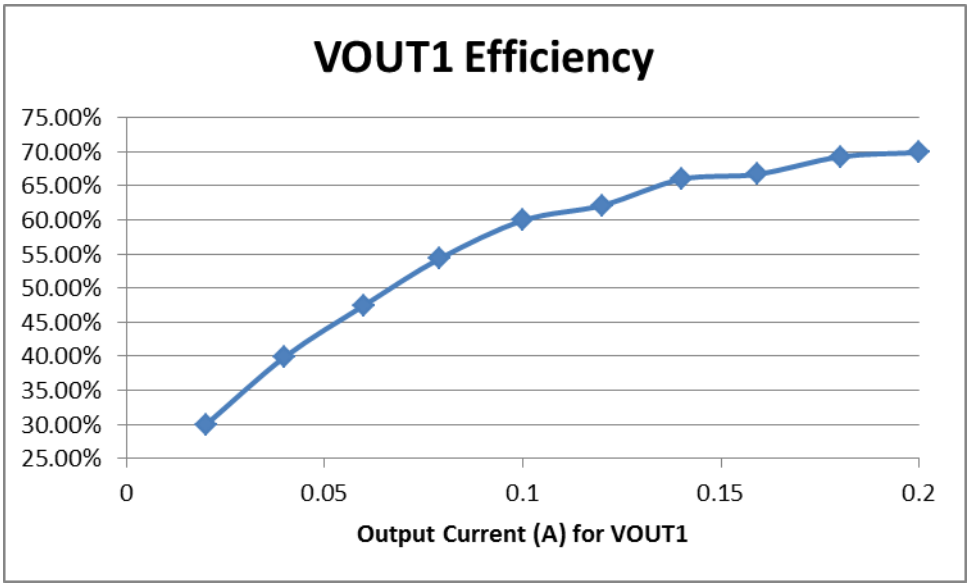
The below image is from the Venable Bode Analyzer. This plot shows gain versus frequency and phase versus frequency for the VOUT1 power rail using the TPS55340-Q1 controller.

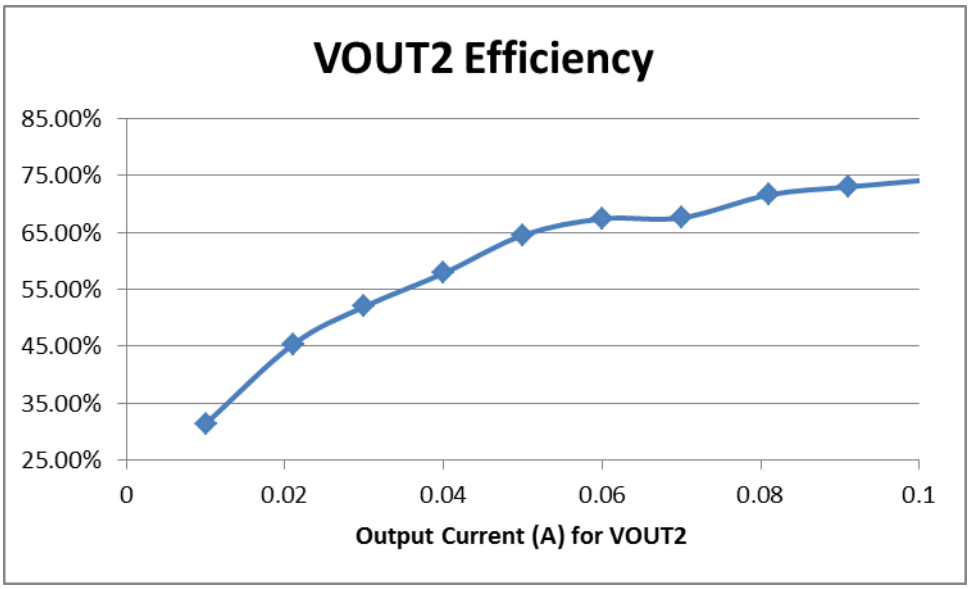


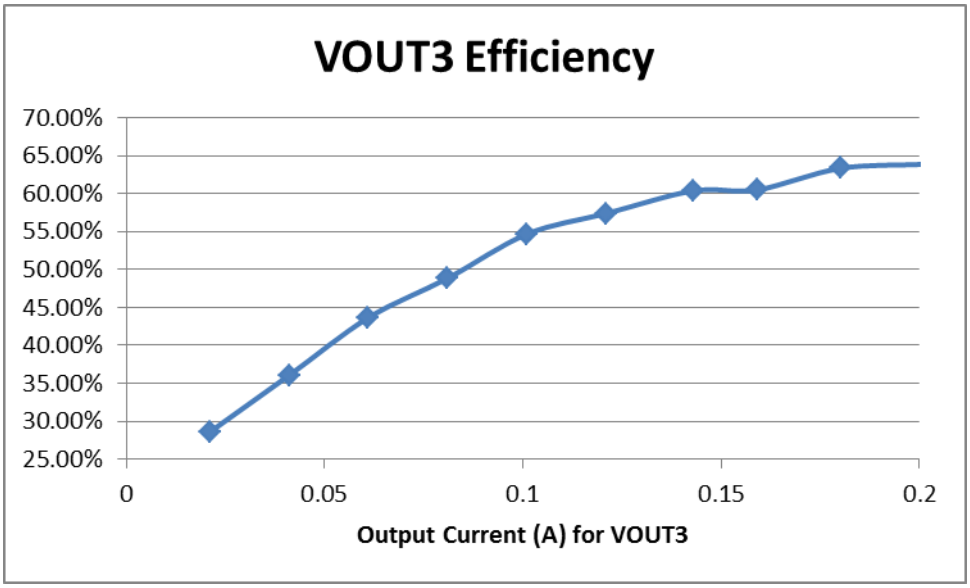
VOUT1 – Bode Plot - Phase Margin = 63.2 degrees – Gain margin = 17.4 dB

G – Efficiency

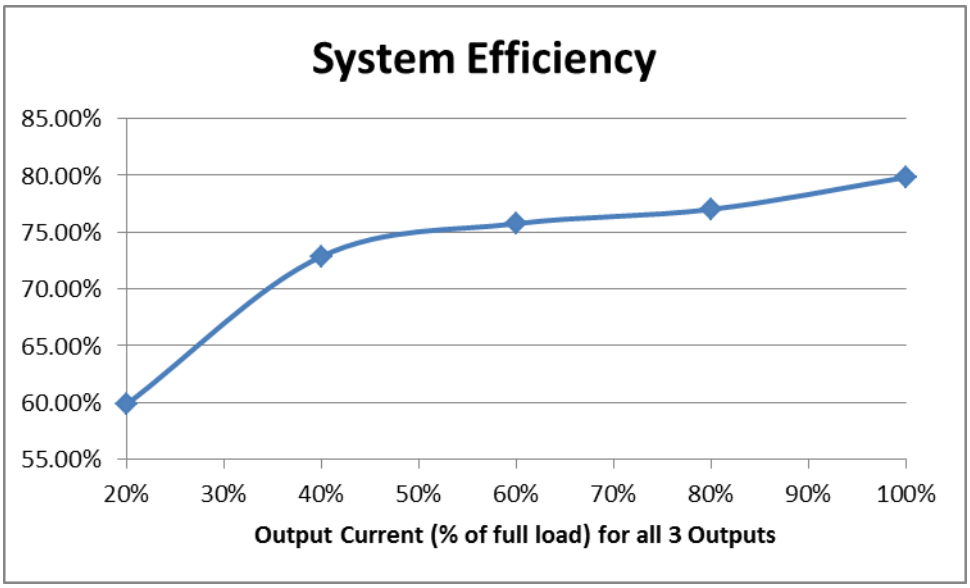
The below three plots show the efficiency data for the three different output rails. It is important to note that there are preloads on VOUT1, VOUT2, and VOUT3 rails as well as current draw from the LDO on VOUT2. All of these current draws lead to a decreased efficiency.





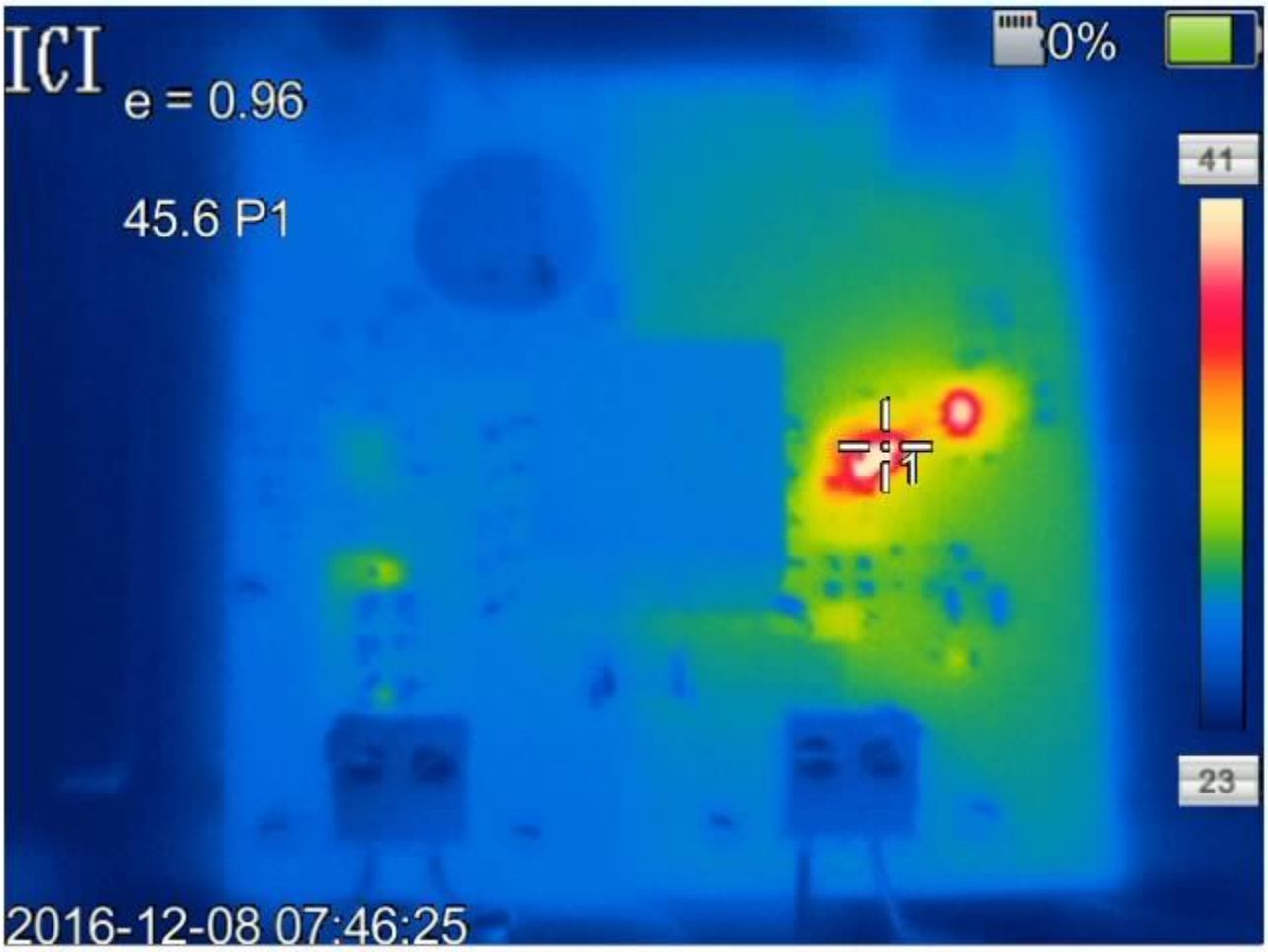


The below plot is an efficiency plot showing the efficiency of the entire system. The three outputs are all loaded simultaneous. The currents are at 20%, 40%, 60%, 80%, and 100% of their full loads.



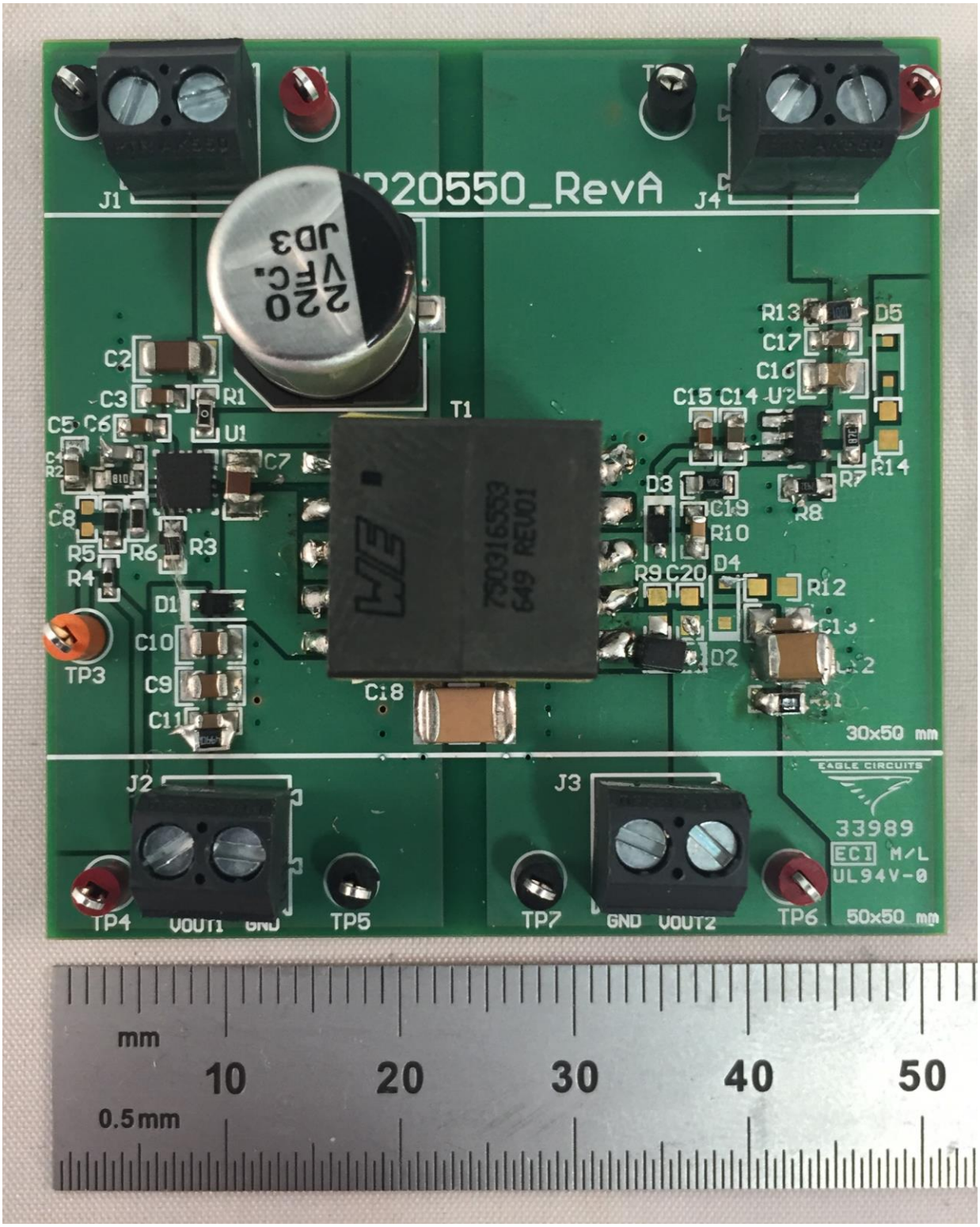
H – Thermal

Below is the thermal image taken of the board while operating at full load on all 3 outputs.



I – Board Image

Below is an image showing the board.



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