TI Designs

48-V Three-Phase Inverter With Shunt-Based In-Line Motor Phase Current Sensing Reference Design

Description

The TIDA-00913 reference design realizes a 48-V/10-A three-phase GaN inverter with precision in-line shunt-based phase current sensing for accurate control of precision drives such as servo drives. One of the largest challenges with in-line shunt-based phase current sensing is the high common-mode voltage transients during PWM switching. The INA240 bidirectional current sense amplifier overcomes this problem using enhanced PWM rejection. The reference design provides an output voltage from 0 to 3.3 V, scaled to ±16.5 A with a 1.65-V mid voltage for high phase-current accuracy over the entire temperature range. The TIDA-00913 offers a TI BoosterPack™ compatible interface to connect to a C2000™ MCU LaunchPad™ development kit for easy performance evaluation.

Resources

TIDA-00913	Design Folder
INA240	Product Folder
REF3333	Product Folder
TMP302	Product Folder
LMG5200	Product Folder
LM5018	Product Folder
TIDA-00909	Tool Folder
InstaSPIN-MOTION™ LaunchPad	Tool Folder

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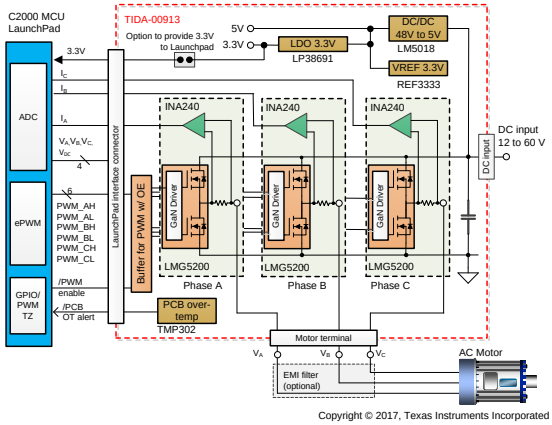
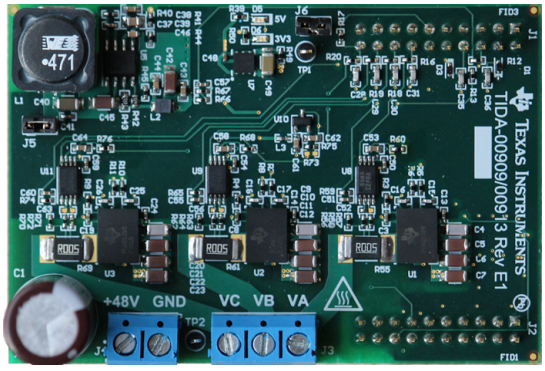
Features

- Wide Input Voltage Range 12- to 60-V Three-Phase GaN Inverter With 7-A_{RMS} Output Current per Phase and Non-isolated Phase Current Sensing
- Precision In-Line Phase Current Sensing With 5-mΩ Shunt, ±16.5-A Full-Scale Range, and ±10-A Nominal Range
- High Accuracy Phase Current Sensing Over Temperature Range From –25°C to 85°C; Uncalibrated Accuracy <±0.5%; Calibrated Accuracy <±0.1%
- Reduces System Cost Using Non-Isolated Current Sense Amplifier INA240 With Superior AC Common-Mode Rejection Operating up to PWM Switching Frequencies up to 100 kHz
- Reduced BOM and Easy Layout due to INA240 Bidirectional, Zero-Drift Current Sense Amplifier That Directly Interfaces to 3.3-V ADC
- TI BoosterPack Compatible Interface With 3.3-V I/O for Easy Performance Evaluation With C2000 MCU LaunchPad Development Kit

Applications

- Servo Drives and Motion Control
- Computer Numerical Control (CNC) Drives
- Manufacturing Robots
- Service Robots
- Non-Military Drones





1 System Overview

1.1 System Description

Precision phase current sensing is critical in many industrial drive applications like servo drives, CNC drives, and manufacturing robots, where accurate position and torque control is required. Due to excellent linearity, a shunt-based solution is often preferred, especially for current ranges below 50 A. For low-voltage drives with DC-link voltages in the range of 24 to 60 V, the current shunt is typically placed either inline to the phase or between the bottom switch and GND, as shown in Figure 1.

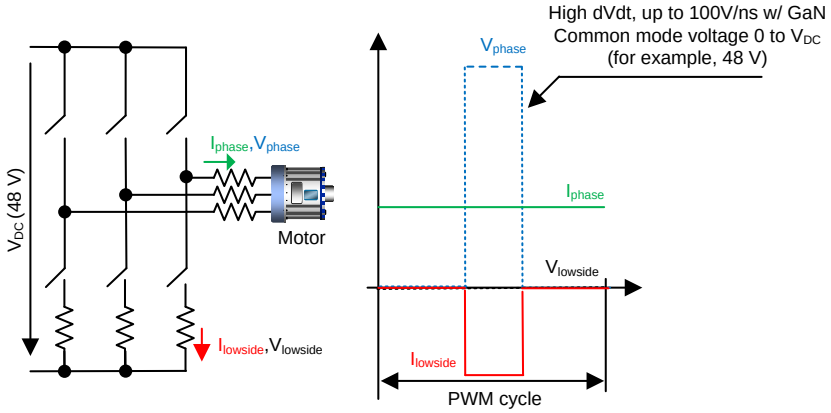


Figure 1. Typical Current Shunt Placement in Three-Phase Inverters

The disadvantage of the low-side shunt is that the low-side shunt current is equal to the inverted phase current only while the low-side switch is on. When the low-side switch is off, there is no phase current measurement possible. This approach does not typically allow for high-precision phase current sensing. A further disadvantage of a low-side shunt solution is that it cannot detect a phase to GND short, which can happen due to miswiring a motor terminal phase to GND. Due to the discontinuous low-side current and the low on-time at very low duty cycles, a current sense amplifier has to be chosen with a high bandwidth and especially a high slew rate, typically 10 V/µs or higher. This amplifier ensures the output settles within less than one or a few microseconds depending on the PWM switching frequency and minimum duty cycle. The inline phase current shunt overcomes these problems and allows for high-precision, accurate phase current sensing.

However, one of the largest challenges with in-line shunt base current sensing is the presence of high common-mode voltage transient during PWM switching. During PWM switching, the common-mode voltage at the phase current shunt transitions from DC– (0 V) to DC+ (for example, 48 V) and vice versa with common-mode voltage transients up to 100 V/ns.

Typical non-isolated differential amplifiers suffer performance and the ability to handle the common-mode input as it quickly toggles between large and small voltages is compromised. Often an isolated amplifier solution was used to improve performance, but increased system cost and BOM.

The INA240 bidirectional, zero-drift, current sense amplifier with enhanced PWM rejection solves that problem. The INA240 is designed for common mode voltages from –4 to 80 V with high common-mode rejection techniques to reduce large $\Delta V/\Delta t$ transients before the system is disturbed as a result of these large signals. In conjunction with signal bandwidth, the high AC CMRR allows the INA240 to provide minimal output transients and ringing compared with standard circuit approaches.

For three-phase inverters, the differential signal from the phase current shunts can now be directly connected to the INA240 differential inputs and a highly accurate output with minimal common-mode transient artifacts is available.

Figure 2 shows the in-line phase current shunt topology as realized with the TIDA-00913. For precision phase current measurements with high linearity, the TIDA-00913 design employs three in-line phase current shunts and three differential precision current sense amplifiers INA240 with high common-mode and high AC common-mode transient immunity.

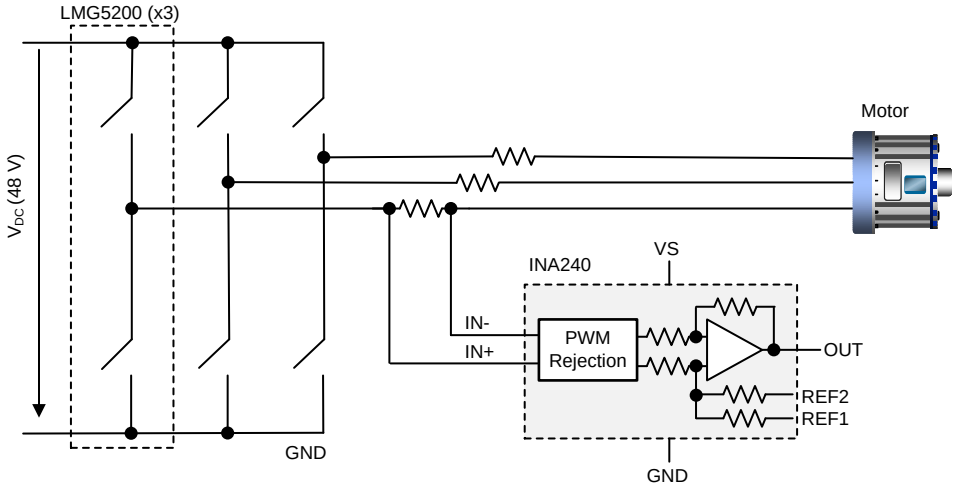


Figure 2. Inline Shunt Phase Current Sensing With INA240 Current Sense Amplifier

The TIDA-00913 three-phase inverter is realized with three LMG5200 GaN half-bridge power modules to allow high PWM switching frequencies. Onboard power management provides a 5-V rail to supply the LMG5200 gate driver and 3.3-V band-gap reference well a 3.3-V rail for the INA240 current sense amplifiers and temperature switch. The TIDA-00913 offers a TI BoosterPack compatible interface to connect to a C2000 MCU LaunchPad for easy performance evaluation.

For details on the three-phase GaN inverter topology and test results, see the TIDA-00909 product page.

1.2 Key System-Level Specifications

Table 1 provides the key specifications of the TIDA-00913 48-V inverter with the shunt-based in-line phase current sensing reference design. The TIDA-00913 design is compliant to the TI BoosterPack 40-pin standard (www.ti.com/byob).

The design can be directly connected to a C2000 LaunchPad to either the first 40-pin instance (J1-J3 and J4-J2) or the second 40-pin instance (J5-J7 and J8-J6). A jumper option is provided on the TIDA-00913 to the power the LaunchPad with 3.3 V. Table 2 and Table 3 introduce the TIDA-00913 pin assignments.

Table 1. Three-Phase Inverter Key Specifications

PARAMETER	TYPICAL VALUE	COMMENTS
DC input voltage	48 V (12 to 60 V)	80-V absolute max
Maximum three-phase output current	$7A_{RMS}$ ($10\text{-}A_{PEAK}$) per phase	See Figure 51 for maximum three-phase output current versus ambient temperature with natural convection
Maximum input power	400 W (at 48 V)	—
Power FET type	GaN technology	Half-bridge power module with integrated high-side and low-side gate drivers (LMG5200)
PWM switching frequency	40 to 100 kHz	—
PWM deadband	12.5 ns	—
Maximum efficiency at 100-kHz PWM	98.5%	At 400-W input power
Phase currents sense and amplifier	5-mΩ shunt per INA240	Differential, non-isolated current sense amplifier with 20 V/V and enhanced PWM rejection (INA240)(1).
Phase current maximum range	±16.5 A	Scaled to 0 to 3.3 V; inverted with 1.65-V bias
Phase current accuracy (–25°C to 85°C)	±0.5% (uncalibrated), ±0.1% (calibrated)	Over nominal range ±10 A; one-time calibration of offset and gain at 25ºC
EMI input and output filter	External	—
PCB layer stack	Four-layer, 70-µm copper	—
PCB size	53.4 mm × 78.9 mm	Dimensions in mil: 2105 mil × 3107 mil
Temperature range	–40ºC to 85ºC	See Figure 51 for maximum three-phase output current versus ambient temperature with natural convection
PCB over-temperature alert	> 85ºC	Configurable from 70ºC to 85ºC (TMP302B)
Interface-to-host processor	TI BoosterPack compatible	Refer to Table 2 and Table 3 for pin assignment
3.3-V supply current for LaunchPad	300 mA or 500 mA (max), see Section 2.1	Jumper option (J3) to provide 3.3-V supply for C2000™ MCU LaunchPad™

(1) Inverted phase current output voltage for optimized layout

Table 2. Interface Specification—Header J1

PIN	SIGNAL	I/O (3.3 V)	PIN	SIGNAL	I/O (3.3 V)
J1-1	3.3-V supply (optional)	O or NC (jumper selectable)	J1-2	NC	—
J1-3	NC	—	J1-4	GND	GND
J1-5	NC	—	J1-6	VDC	O (0 to 3.3 V)(1)
J1-7	NC	—	J1-8	VA	O (0 to 3.3 V)(1)
J1-9	NC	—	J1-10	VB	O (0 to 3.3 V)(1)
J1-11	VREF	O (3.3 V, 10 ppm)	J1-12	VC	O (0 V to 3.3 V)(1)
J1-13	NC	—	J1-14	IA	O (0 to 3.3 V)
J1-15	NC	—	J1-16	IB	O (0 to 3.3 V)
J1-17	NC	—	J1-18	IC	O (0 to 3.3 V)
J1-19	NC	—	J1-20	VREF	O (3.3 V, 10 ppm/K)

(1) Overvoltage protection with Schottky diodes ensures output voltage remains below 3.6 V.

Table 3. Interface Specification—Header J2

PIN	SIGNAL	I/O (3.3 V)	PIN	SIGNAL	I/O (3.3 V)
J2-1	PWM A (high-side)	I (10k PD)	J2-2	GND	GND
J2-3	PWM A (low-side)	I (10k PD)	J2-4	NC	—
J2-5	PWM B (high-side)	I (10k PD)	J2-6	NC	—
J2-7	PWM B (low-side)	I (10k PD)	J2-8	NC	—
J2-9	PWM C (high-side)	I (10k PD)	J2-10	NC	—
J2-11	PWM C (low-side)	I (10k PD)	J2-12	NC	—
J2-13	/PCB OT alert	O (open drain, 10k PU)	J2-14	NC	—
J2-15	NC	—	J2-16	/PWM enable (active low)	I (10k PU)
J2-17	NC	—	J2-18	NC	—
J2-19	NC	—	J2-20	NC	—

1.3 Block Diagram

Figure 3 shows the system block diagram of the three-phase GaN inverter with the TIDA-00913 device indicated in the red-dotted box.

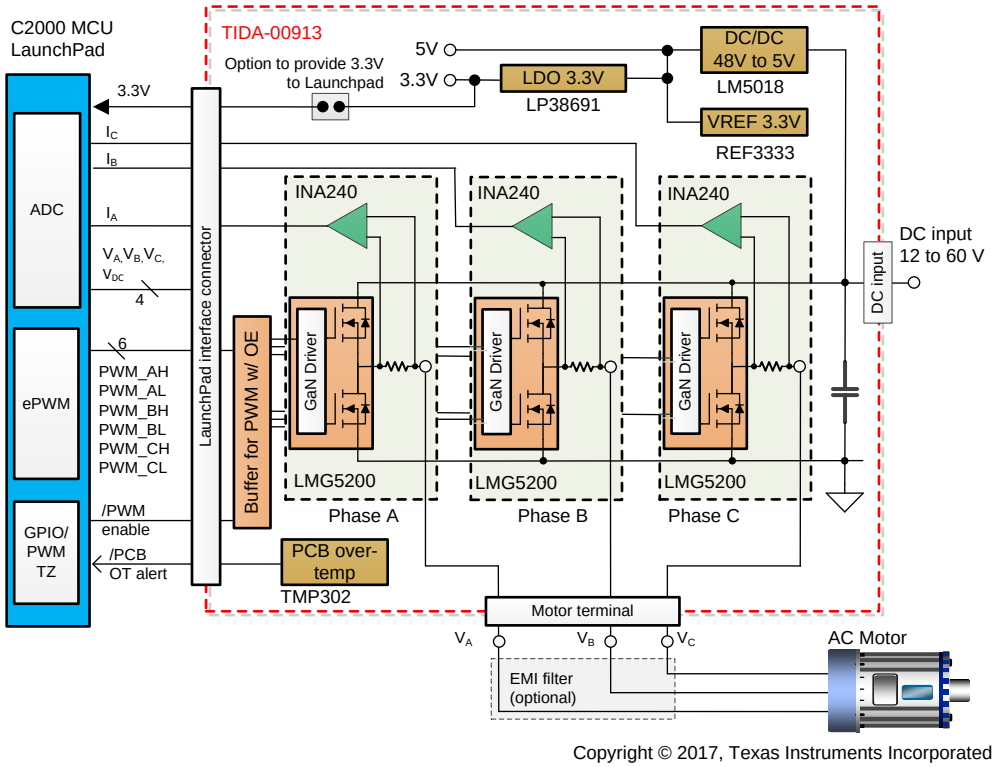


Figure 3. TIDA-00913 Block Diagram

The TIDA-00913 three-phase inverter with shunt-based phased precision phase current sensing accepts input DC voltages from 12- to 60-V DC, the nominal DC input voltage is 48 V. A wide input voltage range DC/DC converter LM5018 generates the 5-V rail to supply the LMG5200 gate driver and the 3.3-V band-gap reference, a 3.3-V LDO supplies the current sense amplifier, input buffer and temperature switch.

Each of the three inverter half-bridges employ an integrated 80-V/10-A GaN half-bridge module (LMG5200), a 5-mΩ phase current shunt and a differential current sense amplifier (INA240) with a gain of 20 V/V and a midpoint voltage of 1.65 V, set by the 3.3-V reference (REF3333). A temperature switch (TMP302) monitors the PCB temperature close the GaN power module.

The TIDA-00913 interface connector to a host processor, like C2000 MCU provides the PWM high- and low-side input signals, the phase current sense amplifier output voltage and the scaled, low-pass filtered phase voltage for each of the three phases. The PWM signals are buffered. A PWM enable signal (active low) allows the host processor to enable and disable all three complementary PWM simultaneously through the onboard buffer. The interface connector also provides the scaled DC-link voltage as well as a PCB over-temperature alert (active low).

The three-phase motor is connected to the three-phase motor terminal. An optional electromagnetic interference (EMI) filter can be added for slew rate reduction, as explained in Section 2.3.3.

The C2000 MCU LaunchPad with the TMS320F28069M device is connected to the TIDA-00913 device and implements a sensorless, speed-variable, field-oriented control of a synchronous motor using the InstaSPIN-FOC™ software. A binary example firmware for the TMS320F28069M device on the InstaSPIN-MOTION™ LaunchPad has been provided to evaluate the TIDA-00913 design with a 48-V low-voltage servo motor (http://www.ti.com/tool/lvservomtr).

1.4 Highlighted Products

The TIDA-000913 reference design features the following key devices from Texas Instruments.

1.4.1 INA240

The INA240 is a voltage-output, current sense amplifier with enhanced PWM rejection that can sense drops across shunt resistors over a wide common-mode voltage range from –4 to 80 V, independent of the supply voltage (see Figure 4). Enhanced PWM rejection provides high levels of suppression for large common-mode transients (ΔV/Δt) in systems that use pulse-width modulation (PWM) signals such as three-phase inverters in motor drives. This feature allows for accurate current measurements without large transients and associated recovery ripple on the output voltage.

This device operates from a single 2.7- to 5.5-V power supply, drawing a maximum of 2.4 mA of supply current. Four fixed gains are available: 20 V/V, 50 V/V, 100 V/V, and 200 V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full scale. All versions are specified over the extended operating temperature range (–40°C to 125°C), and are offered in an 8-pin TSSOP package.

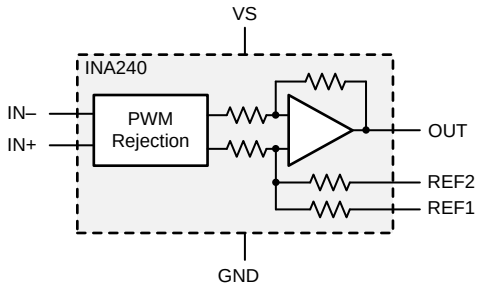


Figure 4. INA240 Functional Block Diagram

Table 4 lists the features and benefits of the INA240 amplifier.

Table 4. INA240 Features and Benefits

FEATURES	BENEFITS
Fast-transient, common-mode, voltage input filtering (enhanced PWM rejection) and high AC CMRR: 93 dB at 50 kHz and 132-dB DC CMRR	Enables non-isolated, shunt-based, precision-phase-current measurement with three-phase inverters with a high-switching frequency of 40 kHz and above
Wide common-mode input voltage range: –4 to 80 V	Provides sufficient headroom for transient overvoltage and undervoltage in three-phase inverters with 48- to 60-V DC link voltage
Low offset voltage (V_{OS} = ±25 µV) and low gain error (0.2%)	Low offset and gain error enables accurate current sensing without calibration
Low offset voltage drift (0.25 µV/°C) and gain error drift (2.5 ppm/°C)	Ultra-low offset and gain error drift allows highly-accurate current sensing over entire temperature range without temperature-dependent calibration
400-kHz signal bandwidth	High signal bandwidth supports low-latency phase current measurement of high-speed motors as well as low latency detection of high-current transients such as during a short-circuit event
Integrated output, midpoint voltage, reference voltage divider	Allows using an external ADC reference to set the INA240 midpoint voltage to half of the ADC reference voltage, which eliminates any offset generated by the ADC reference voltage drift
Integrated precision-gain-setting resistors	Very-low offset drift, easier PCB layout, and reduced BOM

1.4.2 LMG5200

The LMG5200 80-V GaN half-bridge power stage provides an integrated power stage solution using enhancement-mode Gallium Nitride (GaN) FETs. The device consists of two GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration, as Figure 5 shows.

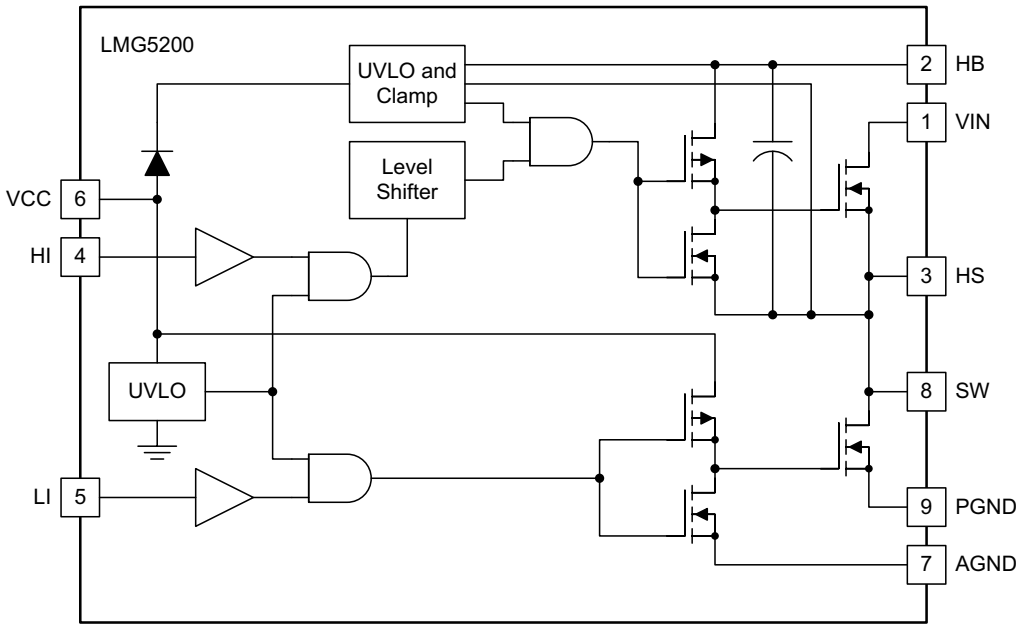


Figure 5. LMG5200 Functional Block Diagram

GaN FETs provide significant advantages for power conversion as they have near-zero reverse recovery and very-small input capacitance CISS. The LMG5200 is mounted on a completely bond-wire-free package platform with minimized package parasitic elements. The LMG5200 device is available in a 6×8×2-mm lead free package and can be easily mounted on PCBs. The LMG5200 reduces the board requirements for maintaining clearance and creepage requirements for medium-voltage GaN applications while minimizing the loop inductances to ensure fast switching. The LMG5200 is specified over the extended operating temperature range (–40°C to 125°C).

Table 5 lists the features and benefits of the LMG5200 device.

Table 5. LMG5200 Features and Benefits

FEATURES	BENEFITS
Integrated high-side and low-side GaN driver and 80-V GaN FETs; 14-mΩ devices for 10-A DC operation	Enables up to 60-V DC, three-phase inverter with 7-A_{RMS} phase current at a 100-kHz high-switching frequency for low-inductance and high-speed drives
Integrated 80-V, 14 -mΩ, GaN FETs and GaN driver with completely bond-wire-free package	Minimized package parasitic elements enable ultra-fast switching for reduced switching losses to reduce or eliminate heatsink
GaN FETs have zero reverse recovery (third quadrant operation) and very-small input capacitance CISS	Reduce or eliminates ringing in hard switching, which reduces EMI; very low overshoot and undershoot allows higher nominal DC-link voltage than Si-FET for same max rated voltage
Excellent propagation delay matching (2-ns FETs)	Enables ultra-low deadband per half-bridge for major reduction of switching losses in three-phase inverter applications
Independent high-side and low-side TTL inputs	Direct PWM interface to 3.3-V MCU
Single 5-V gate driver supply with bootstrap voltage clamping and undervoltage lockout	Ease power management; UVLO ensures simultaneous shutdown of high-side and low-side GaN FET in case of gate driver undervoltage
LMG5200 optimized pinout	Simple PCB layout with minimum inductance for reduced switching losses

1.4.3 LM5018 or LM5017

The LM5018 is a 100-V, 300-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The LM5018 device is available in WSON-8 and HSOP PowerPAD™-8 plastic integrated circuit packages. The LM5017 is a drop-in compatible version for a 600-mA supply current.

Table 6 lists the features and benefits of the LM5018 regulator.

Table 6. LM5018 Features and Benefits

FEATURES	BENEFITS
Wide 7.5- to 100-V input range	Allows use for point-of-load for three-phase inverters with wide-input DC-link voltage from 12 to 80 V
Integrated 100-V high-side and low-side switches	Reduced BOM cost, easier layout
Constant on-time (COT) control scheme employed in the LM5018	No loop compensation required, provides excellent transient response, and enables very-high step-down ratios, such as 48 to 5 V used in the TIDA-00913 design
Integrated peak-current limit circuit and thermal shutdown	Protects against overload conditions

For more information on each of these devices, see their respective product folders at www.TI.com or click on the links for the product folders on the first page of this reference design under the *Resources* section.

2 System Design Theory

The three-phase GaN inverter is realized with three 80-V/10-A LMG5200 GaN half-bridge power modules. The phase current sensing is realized with an in-line shunt and the INA240 precision current-sense amplifier with enhanced PWM rejection that can sense drops across shunt resistors over a wide common-mode voltage range from –4 to 80 V, independent of the supply voltage. Enhanced PWM rejection provides high levels of suppression for large common-mode transients (ΔV/Δt) in systems that use PWM signals such as three-phase inverters in motor drives. This feature allows for accurate current measurements without large transients and associated recovery ripple on the output voltage.

The PCB employs two separated ground planes. The power ground (PGND) and the logic/analog ground (GND). Both ground planes are connected in star configuration through a net tie and optional two 0-Ω resistors to minimize crosstalk of high switching frequency currents in the power ground plane into the logic plane.

The following sections outline the hardware design guidelines for each functional subsystem.

2.1 Precision Phase Current Sensing

2.1.1 In-Line Phase Current Sensing Subcircuit

One of the three in-line phase current sensing subcircuits are shown in Figure 6.

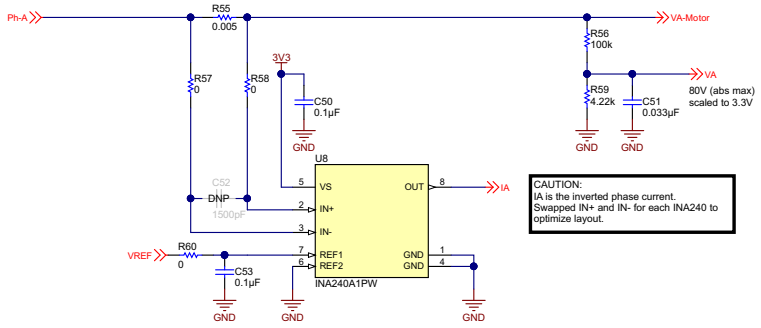


Figure 6. Schematic of In-Line Phase-Current Sense Solution for Phase A

2.1.2 INA240—High-Performance In-Line Motor Current Sensor

The INA240 is configured as a bidirectional current sense amplifier. When the differential input equals 0 V, the output of the INA240 is 1.65 V, and it swings in either direction depending on the motor current flow.

The power supply of the INA240 is a regulated 3.3-V voltage source. This ensures voltage compliance with the LaunchPad ADC.

The output of the INA240 is determined as per Equation 1:

$$IA\left[V\right] = \left(-IL_A\left[A\right] \times 5\ m\Omega\right) \times 20\left[\frac{V}{V}\right] + 1.65\ V \tag{1}$$

Note that the phase current direction is actually inverted for the purposes of having an optimal layout. The maximum phase current range is from –16.5 to 16.5 A. The corresponding output voltage ranges from 0 to 3.3 V with 1.65 V representing a 0-A phase current.

Figure 6 shows R55 is directly connected to the switch node output (SW pin) of the LMG5200 device. The shunt is connected through a Kelvin connection and optional, differential RC low-pass filter (R57, R56, and C52) to the differential inputs IN+ and IN– of the INA240A1 device. In this TI Design, the low-pass filter is not required and the two series resistors have been selected as 0 Ω and the capacitor C52 has not been populated on all three phases. The INA240A1 device has a fixed gain of 20 V/V. To convert the bipolar input voltage across the shunt into a unipolar output voltage that is suitable for an ADC with a 3.3-V input voltage range, the mid-voltage of the INA240A1 (U8) is set to 1.65 V.

2.1.3 REF3333—Setting Output Reference of Phase Current Sensing Circuit

The precision, low-drift 3.3-V reference REF3333 is connected through an optional RC low-pass filter (R60 and C53) to the REF1 pin of INA240. The REF2 pin is connected to GND. By default, the low-pass filter is not used and R60 is set to 0 Ω, which is the same on the other two phases as shown in Figure 6. An internal, precision divide-by-2 function in the INA240 device creates a precision, ultra-low drift, 1.65-V bias voltage at the INA240 OUT pin. Figure 7 shows the schematic of one half-bridge.

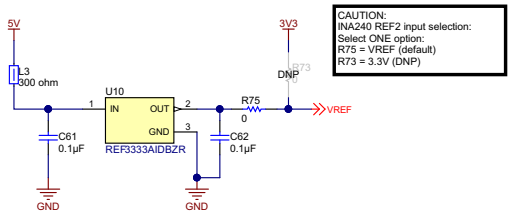


Figure 7. Schematic of 3.3-V Reference Circuit

2.2 Phase Voltage and DC Input Voltage Sensing

The phase voltage for each phase and the DC-link voltage, which is equal to the input voltage, are sensed through a resistor divider. Figure 8 shows an example of this for the DC-link voltage (R56, R59) with a low-pass filter (C51) to attenuate the PWM carrier frequency. The phase voltage is scaled to 3.3 V, assuming an absolute maximum voltage of 80 V according to Equation 2:

$$VA[V] = V\_A[V] \times \frac{1}{24.7} \tag{2}$$

The cutoff frequency (f – 3 dB) of the low-pass filter has been set to 1 kHz, which provides around 32 dB of attenuation to reject a 40-kHz PWM carrier frequency and 40 dB for a 100-kHz PWM carrier frequency. The DC-link voltage is sensed through the same resistor divider (see Figure 8) and low-pass filter to ensure all voltages have the same transient response and delay.

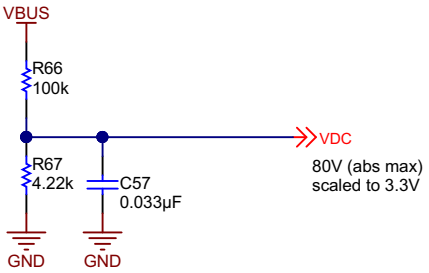


Figure 8. Schematic of DC-Link Voltage Sense

2.3 Three-Phase GaN Inverter Power Stage

The three-phase GaN inverter is realized with three LMG5200 GaN half-bridge power modules. A bulk capacitor of 220 µF is used to buffer the 48-V DC input. The PCB employs two separated ground planes: the power ground (PGND) and the logic or analog ground (GND). Both ground planes are connected in a star configuration through a net tie and two optional 0-Ω resistors to minimize the crosstalk of high-switching frequency currents in the power ground plane into the logic plane.

2.3.1 LMG5200 GaN Half-Bridge Power Stage

The LMG5200 80-V GaN half-bridge power stage provides an integrated and easy-to-use power stage solution using enhancement-mode GaN FETs. The device consists of two GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration. GaN FETs provide significant advantages for power conversion as they have near-zero reverse recovery and very small input capacitance CISS. The LMG5200 is mounted on a completely bond-wire-free package platform with minimized package parasitic elements. The PCB space is further reduced due to high integration and the fact that only a few additional passive components are required. Figure 9 shows the schematic of one half-bridge.

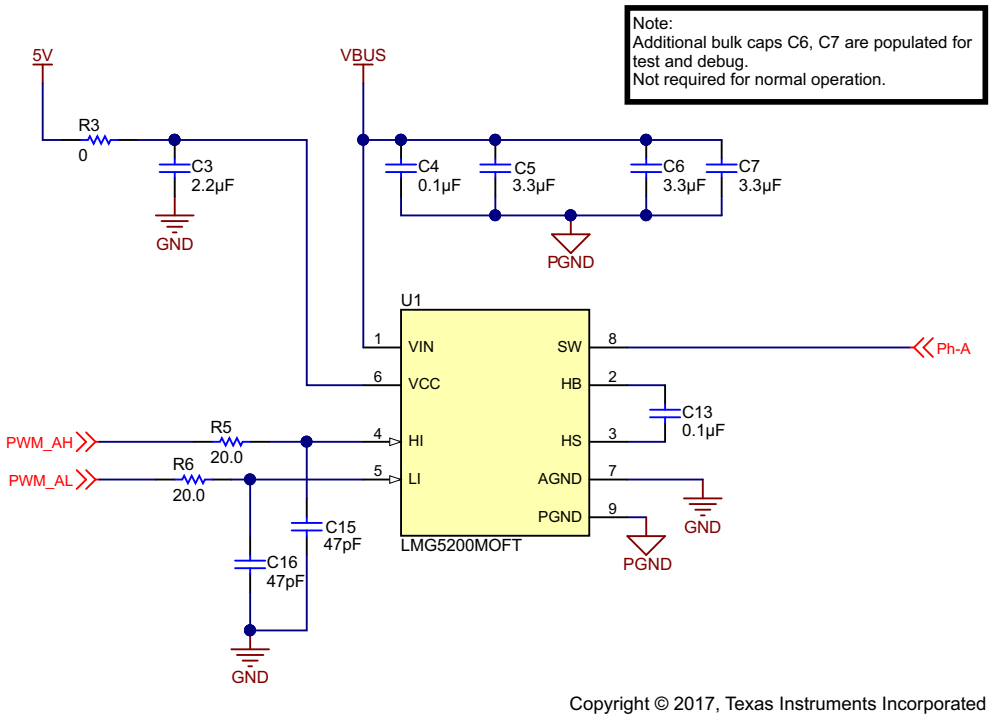


Figure 9. Schematic of Half-Bridge Power Stage for Phase A

Due to the high integration of the LMG5200 power stage, very few passive components are required. The 48-V DC-link voltage is connected between the LMG5200 VIN pin and referenced to the PGND pin. Local ceramic bypass capacitors C4 (100 nF) and C5, C6, and C7 (each 3.3 µF) are placed in parallel close between the VIN and PGND pins to minimize loop inductance. C6 and C7 are optional and not required for normal operation, as the *Test Results* outline in Section 4.2.3. Section 5.3 outlines the optimized layout for low EMI.

The LMG5200 integrated gate driver is supplied with 5 V. A 2.2-µF ceramic bypass capacitor C3 is placed close to the VCC pin and AGND pin. The series resistor R3 has been placed for testing and debugging such as current consumption measurement and was set to 0 Ω for the final board. Sequencing is not required for the 5 V at V_{CC} and the 48 V at V_{IN}, neither during the power up or power down of the input DC voltage.

The complementary PWM signals for the high-side and low-side switch from the MCU are low-pass filtered with R5/C14 and R6/C16 and reject high-frequency impulse noise to avoid false switching. The 100-n ceramic bootstrap capacitor C13 is placed close to the HB (high-side, gate-driver bootstrap rail) and HS (high-side, GaN-FET source connection) pins. The switch node (SW) pin is connected to the motor phase-A terminal through a series inline shunt for phase current sensing, which Section 2.1 outlines.

2.3.2 Power-Stage PCB Over-Temperature Switch

To sense an over-temperature event with the PCB power stage, the TMP302 family of temperature switch devices has been selected as it offers trip-point accuracy of ±0.2°C from 40°C to 125°C and pin-selectable trip points from 55°C to 125°C in 5°C steps with an optional 5°C or 10°C hysteresis. The TMP302B micro-package temperature switch has been chosen and placed closed to the LMG5200 half-bridge module (see the schematic in Figure 10). The TMP302B switch is configured to trip above 85°C by pulling up the TMP302B TRIPSET0 and TRIPSET1 pins to 3.3 V. The hysteresis is set to 5°C by pulling the HYSTSET pin down to GND. The /OT pin is an open-drain and has a 10-k pullup to 3.3 V. An over-temperature event is indicated through the /OT pin set low. The TMP302B switch is connected to the 3.3-V rail and logic GND, but placed very close to the power ground plane of the phase-A half-bridge.

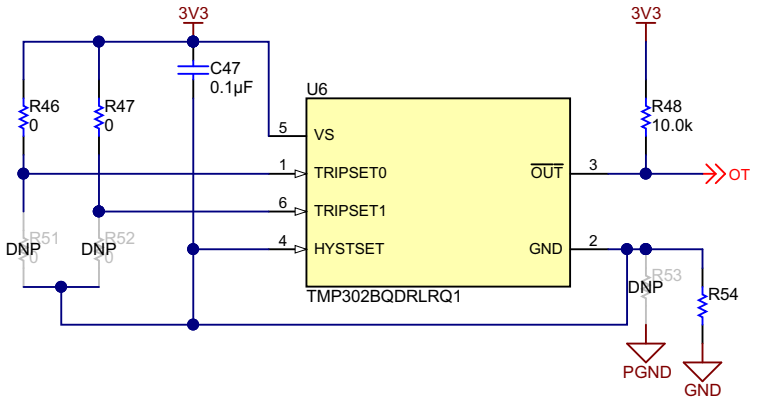


Figure 10. Schematic of 85ºC PCB Temperature Switch

2.3.3 Optional Output LCR EMI Filter

Phase voltage transients higher than specified for the corresponding motor may deteriorate the winding insulation. Typical motor isolation ratings are below 10 kV/µs. Due to the very-high slew rate of the GaN inverter of around 50 V/ns, an output LCR EMI filter may be added in series to each phase terminal to reduce the slew rate at the motor phase terminals, respectively. Figure 11 shows the topology of the output LCR filter applicable to each phase.

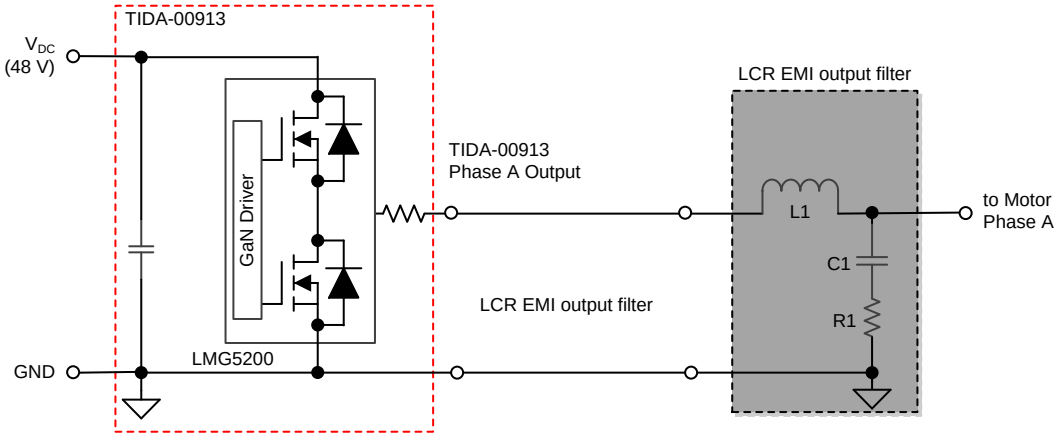


Figure 11. Output LCR Filter Topology

For more details on the optional LCR EMI filter, see the TIDA-00909 TI Design.

2.4 Interface-to-Host MCU

The interface-to-host processor, such as the C2000 MCU, is compliant to a 3.3-V I/O and provides all the required signals like the complementary PWM signals for phase A, B, and C; a PWM trip and disable signal as well as accurate phase current, phase voltage, and DC-link voltage feedback to control the three-phase GaN inverter. Additional feedback signals, like the over-temperature trip (/OT), further help to protect the three-phase GaN power stage.

To allow quick and easy evaluation with a C2000 MCU, the TIDA-00913 host-processor interface headers are TI BoosterPack compatible. The TIDA-00913 fits both upper and lower headers of an 80-pin C2000 MCU LaunchPad, like the LAUNCHXL-F28069M. Additionally, the TIDA-00913 host interface offers the option to provide the 3.3-V rail to power the C2000 LaunchPad, as well. This option ensures proper power-up sequencing of the entire system. The details of the pin assignment are outlined in Section 1.2, Table 2, and Table 3, respectively.

Figure 12 shows the schematic of the host port interface.

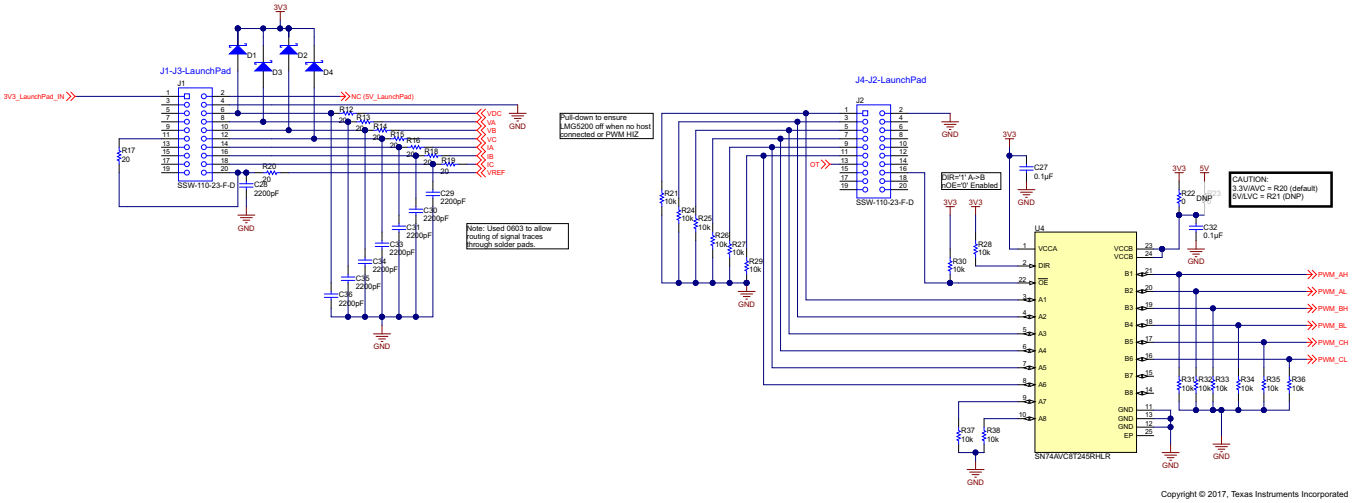


Figure 12. Schematic of Host Interface Connectors J1 and J2

All eight analog feedback signals (I_A, I_B, I_C, V_A, V_B, V_C, V_{DC}, and V_{REF}) include an RF filter with a high enough capacitor of 2200 pF to drive the switched-capacitor ADC input embedded in the C2000 MCU. The capacitors are a magnitude of 1000 larger than the integrated switched capacitor in the ADC of a C2000 Piccolo MCU. This magnitude properly ensures that the input signals settle to 0.1% or better, even during short sampling periods of less than 100 ns without requiring an additional buffer amplifier. The phase voltage and DC-link voltage signals have additional Schottky diodes clamped to 3.3 V to ensure the ADC input voltage remains below 3.6 V, even if a voltage higher than the 80-V input has been accidently applied to the TIDA-00913.

The complementary PWM signals are buffered through the SN74AVC8T245 8-bit dual-supply bus transceiver. During power-up, the output of the bus transceiver remains high impedance due to the 10-k pullup (R30) at the /OE pin. All PWM input and output pins on either side of the SN74AVC8T245 transceiver have pulldown resistors. These pulldown resistors ensure that the PWM signals remain low and the LMG5200 remains off if no host processor is connected or the PWM pins of the host processor are high impedance during power up or power down.

2.5 Power Management

The onboard power management consists of an EMI input filter, a wide-input voltage DC-DC buck converter to generate the 5-V rail, and an LDO for the 3.3-V rail.

2.5.1 EMI Input Filter

An input filter is used to reduce the input voltage ripple accordingly. The design follows the *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* application report [10]. In the case of the TIDA-00913 design, this input filter consists of a PI-filter (π) with the cutoff frequency around 1/10th of the switching frequency of the DC-DC converters to have 40 dB of attenuation at the DC-DC converter switching frequency of around 150 kHz. The inductor L2 is set to 33 µH, which yields a capacitor value of 3.3 µF for C42 (see Equation 3).

$$fc = \frac{1}{2 \times \pi \times \sqrt{L2 \times C42}} \quad (3)$$

2.5.2 48- to 5-V DC-DC Converter

The DC-DC buck converter has been designed for a nominal input voltage range from 12 to 60 V with an input voltage capability of at least 80 V. The output voltage is set to 5 V. The DC-DC buck-converter feedback circuit has been designed for minimum output voltage ripple and at least 400 mA of output current. The power supply has been entirely designed using WEBENCH® Power Designer [8], using the following parameter specifications in Table 7:

Table 7. DC-DC Buck Converter Parameter

PARAMETER	TYPICAL VALUE	MIN AND MAX VALUES
DC-link voltage	48 V	10 V or 80 V
Output voltage	5 V	±5%
Output voltage ripple	< 50m Vpp	As low as possible
Output current	50 mA	≥ 300 mA
Temperature range	–40.85°C (125°C)	—

Using these settings, the LM5018 is the device chosen to fit the design specification. To meet the minimum ripple, the WEBENCH output ripple option for "Low O/P Ripple Solution" has been selected for the design. Figure 13 shows the proposed WEBENCH recommendation using these settings:

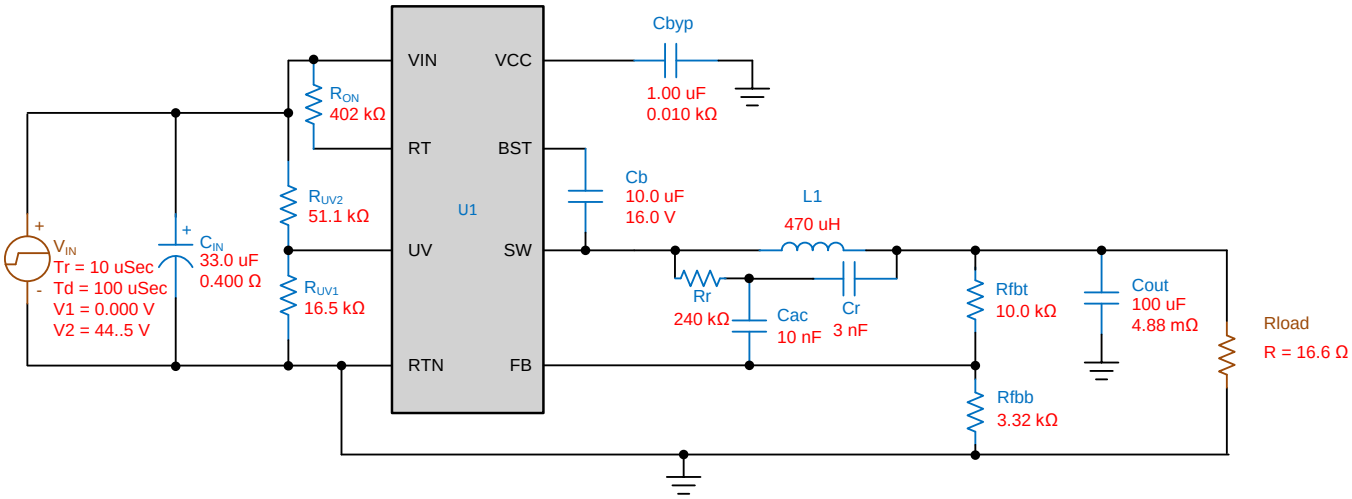


Figure 13. WEBENCH Schematics Proposal for 48- to 5-V Power Supply With Minimum Output Voltage Ripple

Minor changes to the WEBENCH proposals have been made in the final schematics of the TIDA-00913 design. Figure 14 shows the final passive components. Some examples of these minor changes are: An inductor L1 with higher saturation current was chosen to allow higher output current out to 600 mA by replacing the LM5018 device with the LM5017 if required. The feedback filter R40, C38, and C39 help minimize the ripple on the 5-V output rail. The undervoltage lockout (UVLO) was set to 7.35 V by setting R43 to 100 k and R45 to 20 k and the hysteresis was set to 2 V. For details on calculating all passive components, see the LM5018 datasheet (SNVS787).

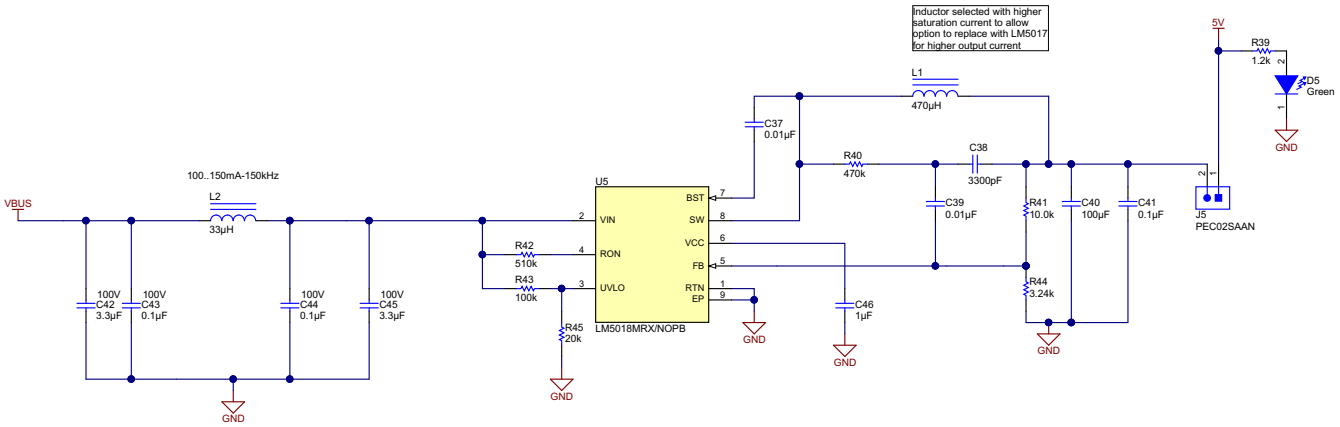


Figure 14. 48-V to 5-V DC-DC Buck Converter With Input EMI Filter

2.5.3 3.3-V Rail

For the 3.3-V rail, an LDO with at least 300-mA output current capability and high-input ripple rejection at 100 kHz was chosen (see Figure 15). The LP38691 device meets these requirements. The output bulk capacitor of 100 µF was chosen for high ripple rejection at 100 kHz, which is close to the switching frequency of the 5-V input. With the 100-µF capacitor, the ripple rejection of the LP38691 device was increased to 50 dB at 100 kHz. The jumper J6, when populated, provides the 3.3-V rail of the TIDA-00913 to also power the C2000 LaunchPad. The maximum load current is 300 mA.

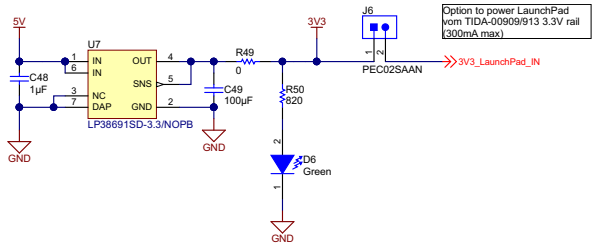


Figure 15. 5-V to 3.3-V LDO

3 Getting Started Hardware and Software

3.1 TIDA-00913 PCB Overview

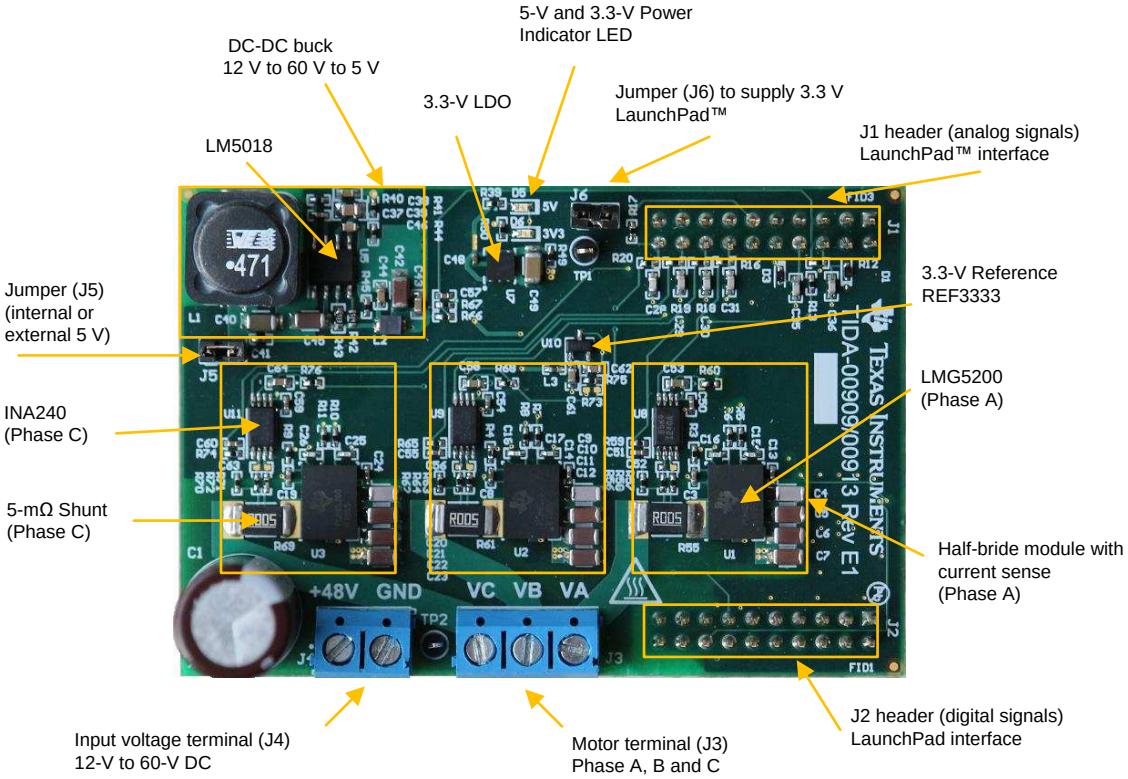


Figure 16. TIDA-00913 PCB—Top View

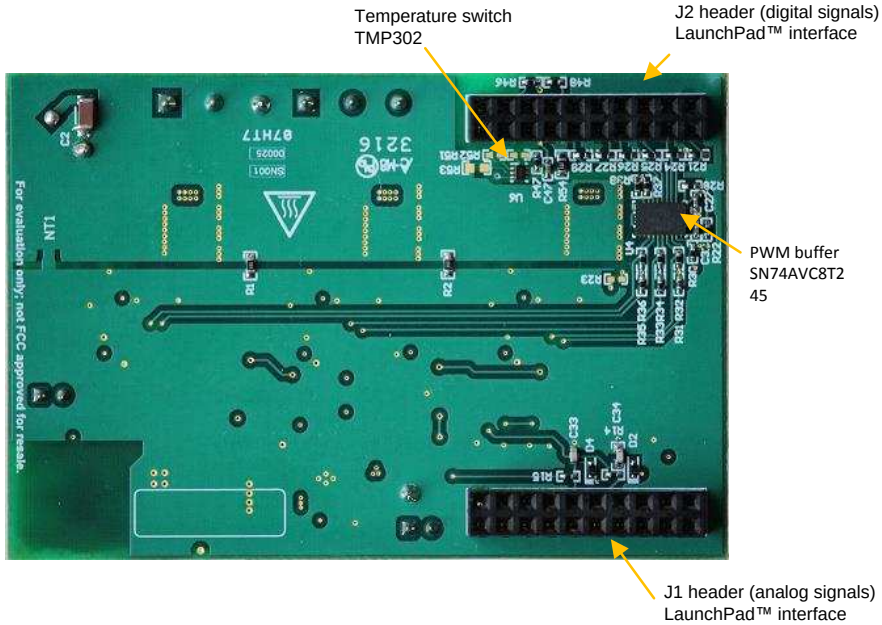


Figure 17. TIDA-00913 PCB—Bottom View

3.2 TIDA-00913 Jumper Settings

The TIDA-00913 employs two jumpers: The jumper J5 allows using an external 5-V supply, if desired. The default setting is J5 populated to use the onboard 5-V supply. The jumper J6, when populated, provides 3.3 V to the J1-1 interface pin to supply to the C2000 LaunchPad with 3.3 V. The maximum continuous current is 300 mA.

Table 8 shows the TIDA-00913 jumper settings.

Table 8. TIDA-00913 Jumper Settings

JUMPER	FUNCTION	POPULATED	NOT POPULATED
J5	5-V supply	Onboard (default)	External 5 V
J6	3.3-V supply at J1-1 interface connector to LaunchPad	3.3 V (default)	Not connected

CAUTION

When the jumper J3 is populated, ensure that the C2000 LaunchPad is not powered through a USB. To ensure this, remove the JP1 and JP2 jumpers on the C2000 InstaSPIN-MOTION LaunchPad.

3.3 Interface to C2000 InstaSPIN-MOTION LaunchPad

The TIDA-00913 interface specification is compliant to the TI BoosterPack standard. See the pin assignment in Table 2 and Table 3 in Section 1.2. The TIDA-00913 board can either be connected to the C2000 InstaSPIN-MOTION LaunchPad headers J1 through J3 and J2 through J4 or to the extended headers J5 through J7 and J6 through J8.

CAUTION

- When connecting the TIDA-00913 to the LaunchPad, pay attention that the bottom-side solder joints do not connect to the additional jumpers and headers of the LaunchPad.
- The phase current I_A, I_B, and I_C equivalent output voltage at connectors J1-14, J1-16, and J1-18 is inverted versus the DRV8301 BoosterPack.
- When J6 is populated so that the TIDA-00913 provides the 3.3 V to supply the LaunchPad, ensure that the LaunchPad is not powered from a USB. To ensure this, remove the JP1 and JP2 jumpers on the InstaSPIN-MOTION LaunchPad, as Figure 18 shows.

Figure 18 shows the TIDA-00913 connected to the InstaSPIN-MOTION LaunchPad headers J5 through J7 and J6 through J8. Note that the TIDA-00913 powers the LaunchPad; therefore, the TIDA-00913 J6 is populated and the jumpers JP1 and JP2 on the LaunchPad are not populated.

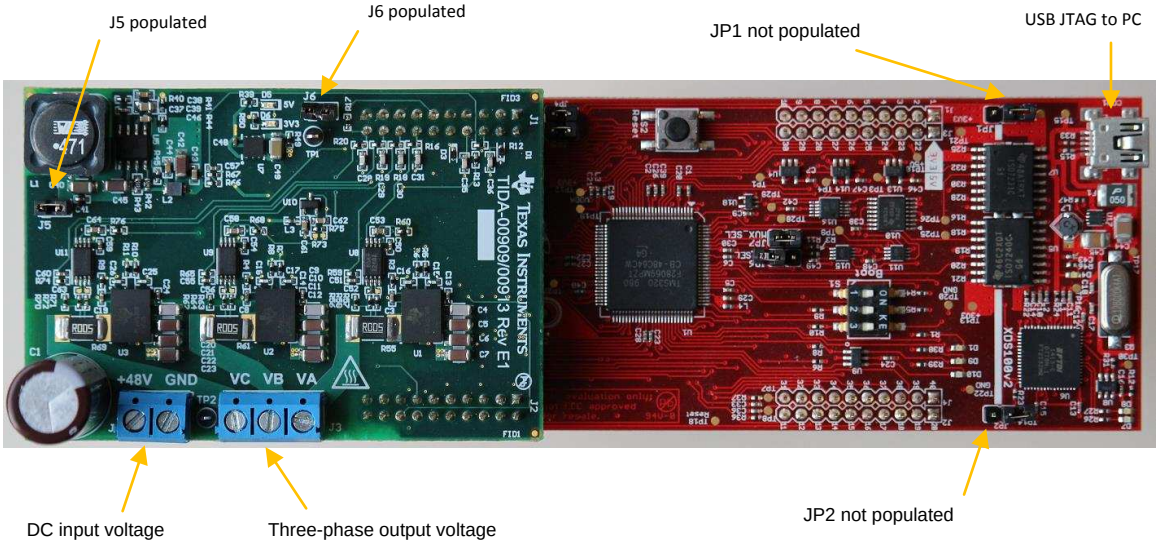


Figure 18. TIDA-00913 LaunchPad Connection Example

Connect the DC power supply (12 to 60 V, 48-V nominal) to the DC input voltage connector (J4) and the three-phase motor to the three-phase output voltage connector (J3). Validate that the three-phase motor can handle the high slew rates of the phase voltages during PWM switching; otherwise, consider using a low-pass LCR filter to reduce the slew rate of the phase voltage according to the requirements of the motor.

3.4 InstaSPIN-FOC Example Project for Teknic Servo Motor M-2310P-LN-04K

The software example is created for the InstaSPIN-MOTION LaunchPad using headers J5 or J7 and J6 or J8. Ensure the TIDA-00913 board is connected to the InstaSPIN-MOTION LaunchPad as Figure 18 showed.

Be sure to install the Texas Instrument's MotorWare™ software package revision 1.01.00.16 in the default install path *C:\ti\MOTORWARE\motorware_1_01_00_16*.

Unzip the TIDA-00913 software package for the example to the *C:\ti\tida-00913* folder.

Follow the next steps in Section 3.4.1 to create an InstaSPIN-FOC project example for the TIDA-00913 hardware connected to the InstaSPIN-MOTION LaunchPad.

3.4.1 Set up TIDA-00913 Board Specific Project Folders in MotorWare Software

1. Navigate to folder: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\solutions\instaspin_foc\boards*.
2. Create a copy of the *boostxldrv8301_revB* folder in the same directory and rename it to *tida00913*.
3. Navigate to the folder: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\modules\hal\boards*.
4. Create a copy of the *boostxldrv8301_revB* folder in the same directory and rename it to *tida00913*.
5. Copy the five sources files as provided with the TIDA-00913 software package into the *tida00913* folder. The project folders are as follows:
   (a) Copy *user.h* and *user_j5.h* to the following directory: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\solutions\instaspin_foc\boards\tida00913\f28x\f2806xF\src*. Note that this action replaces or overwrites the original files.
   (b) Copy *hal.c* and *hal.h* to the following directory: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\modules\hal\boards\tida00913\f28x\f2806x\src*. Note that this action replaces or overwrites the original files.
   (c) Copy *proj_lab02a-tida00913.c* to the following directory: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\solutions\instaspin_foc\src*.

3.4.2 Set up TIDA-00913 Board Specific Project With Code Composer Studio™ (CCS) Software

1. Open the CCS software, choose TIDA-00913 as the new workspace, and import the *tida00913* projects from:
   C:\TI\MOTORWARE\motorware_1_01_00_16\sw\solutions\instaspin_foc\boards\tida00913\f28x\f2806xF\projects\ccs5.
2. Make the *proj_lab02a* project active.
3. In the *CCS Project* explorer for *proj_lab02a* select the *proj_lab02a.c* C:/ source file and exclude this from the build.
4. Add the file to the project and browse to the *proj_lab02a-tida00913.c* file in the following folder: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\solutions\instaspin_foc\src*. In the dialog window, add the option for adding *proj_lab02a-tida00913.c* as per Figure 19 and click the *OK* button.

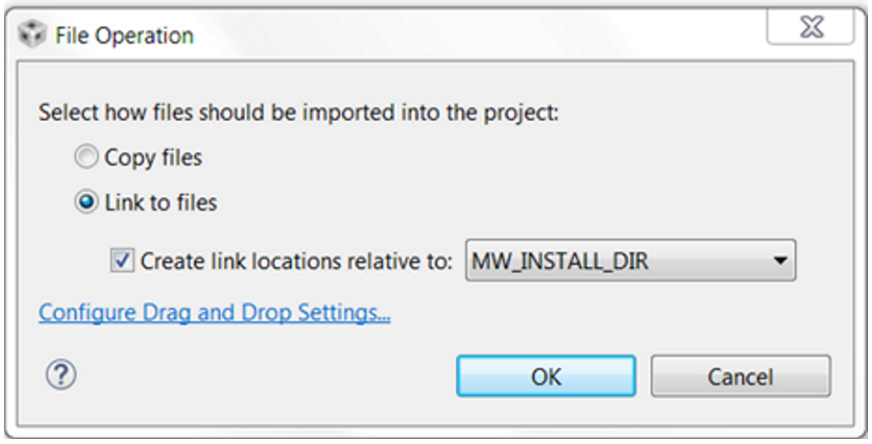


Figure 19. Dialog Window for Step 4

5. In the CCS Project explorer, open the properties of the *proj_lab02* project.
   (a) In the *File* menu, navigate to "Resources" → "Linked Resources", and in the dialog window click the tab on the right for linked resources, as Figure 20 shows:

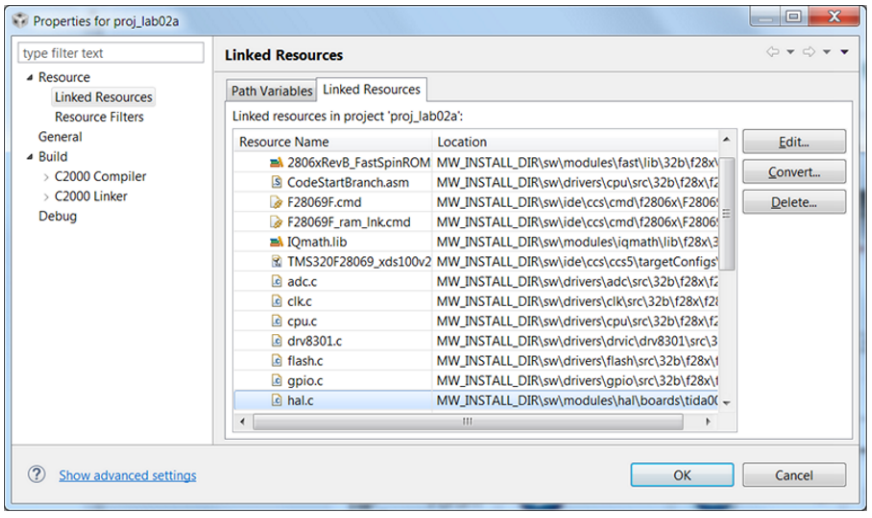


Figure 20. Dialog Window for Step 5a

(b) Select the *hal.c* file (in the "Resource Name" column) and edit the existing link (in the "Location" column) with the new link to the tida00913 project: *MW_INSTALL_DIR\sw\modules\hal\boards\tida00913\f28x\f2806x\src\hal.c*, as Figure 21 shows:

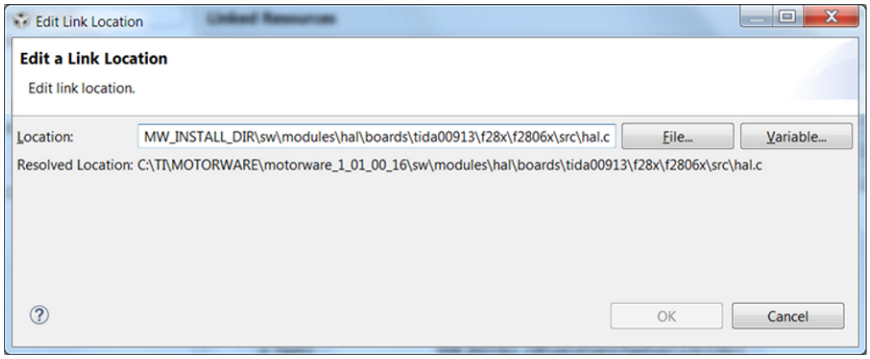


Figure 21. Dialog Window for Step 5b

(c) Click the *OK* button to close the dialog window.

6. In the CCS Project explorer open the properties of the *proj_lab02* project.

(a) In the *File* menu, navigate to "Build" → "C2000 Compiler" → "Include Options" to view the following options in Figure 22:

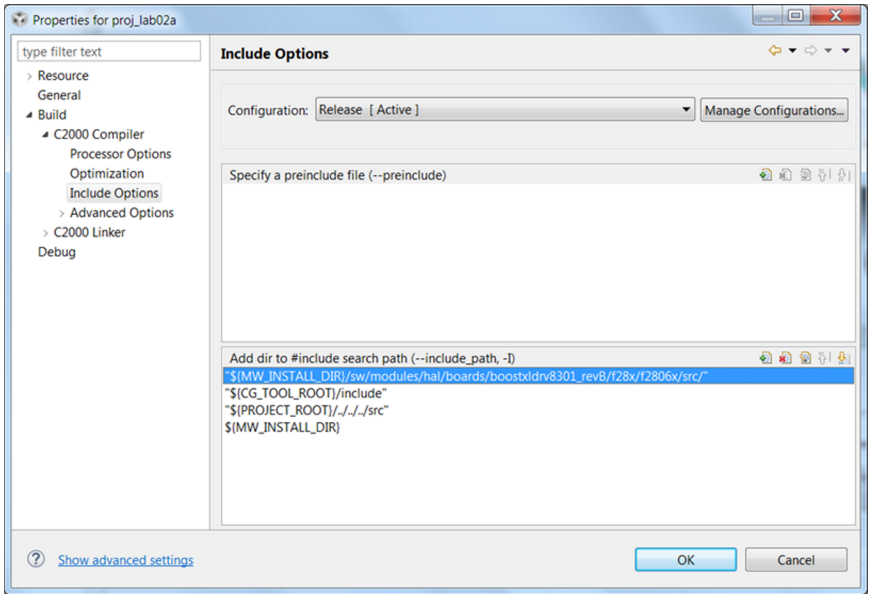


Figure 22. Dialog Window for Step 6a

(b) Select the path highlighted *${MW_INSTALL_DIR}* and change this to *${MW_INSTALL_DIR}/sw/modules/hal/boards/tida00913/f28x/f2806x/src/* as Figure 23 shows:

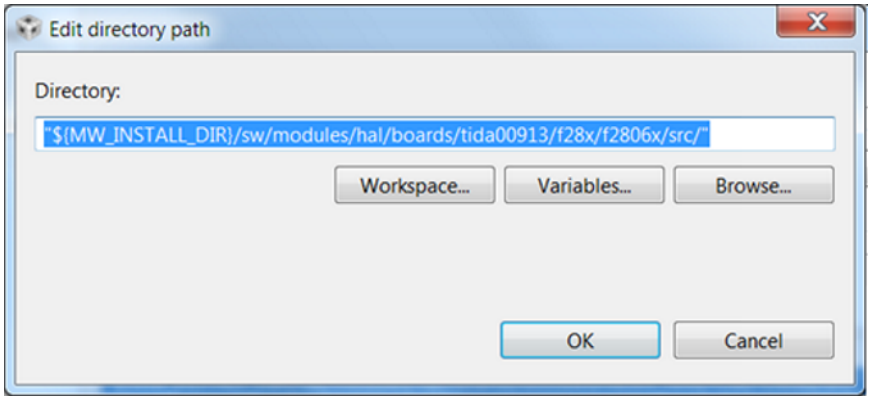


Figure 23. Dialog Window for Step 6b

(c) Click the *OK* button to close the properties window.

3.4.3 Compile and Run TIDA-00913 Project Example

1. Compile the *proj_lab02a-tida00913* project and download to the TMS329F28069F target processor on the InstaSPIN-MOTION LaunchPad.
2. Open the document *InstaSPIN Projects and Labs User's Guide* from: *C:\TI\MOTORWARE\motorware_1_01_00_16\docs\labs\instaspin_labs*.
3. Navigate to the *Lab 2a* project using InstaSPIN for the first time out of ROM on page 27 in the *InstaSPIN Projects and Labs User's Guide* (located in *C:\TI\MOTORWARE\motorware_1_01_00_16\docs\labs\instaspin_labs*) and follow the instructions to identify and run the motor.

The default motor defined in the tida00913 project is the Teknic M-2310P-LN-04K. See the *InstaSPIN Projects and Labs User's Guide* when using other motors.

4 Testing and Results

Table 9 lists the key test equipment. The following subsections descriptions and pictures of the test setup for specific tests.

Table 9. Key Test Equipment

DESCRIPTION	PART NUMBER
High-speed oscilloscope	Tektronix TDS784C
Single-ended probes	Tektronix P6139A
High-speed oscilloscope	Tektronix MDO4104-B3
Differential probes	Tektronix TPD0500
Single-ended probes	Tektronix TPP1000
Power analyzer	Tektronix PA4000
Isolated current probe	Tektronix TCP0030
Multimeter	Agilent 34401A, Fluke 207
Thermal camera	Fluke TI40
Adjustable power supply	Knuerr-Heinzinger Polaris 125-5
Adjustable power supply	TDK-Lamda Genesys GEN 100-33
C2000 MCU LaunchPad	Texas Instruments LAUNCHXL-F28069M
Low-voltage servo motor (48 V, 7 A)	Teknic M-2310P-LN-04K
Low-inductance high-speed brushless multirotor motor	Quanum MT Series 2208 1800KV

The focus of the tests was to measure the performance of the in-line 5-mΩ shunt-based non-isolated phase current sensing using the INA240A1 current sense amplifier with PWM rejection.

For specific test details on the 48-V/10-A GaN inverter switch node and thermal performance, see the TIDA-00909 TI Design.

4.1 Power Management and System Power-up and Power-Down

4.1.1 Power-up and Power-Down of 5- and 3.3-V Rails

The focus of this test was to validate the onboard 5- and 3.3-V power supplies and measure the typical current consumption of the 3.3- and 5-V rails. For these tests, the C2000 LaunchPad was not powered from the TIDA-00913 design. Due to the high step-down ratio of 48:5 (48-V input to 5-V output), the voltage ripple at the 5-V rail was also validated. Two measurements were performed for this test (see Figure 24 and Figure 25).

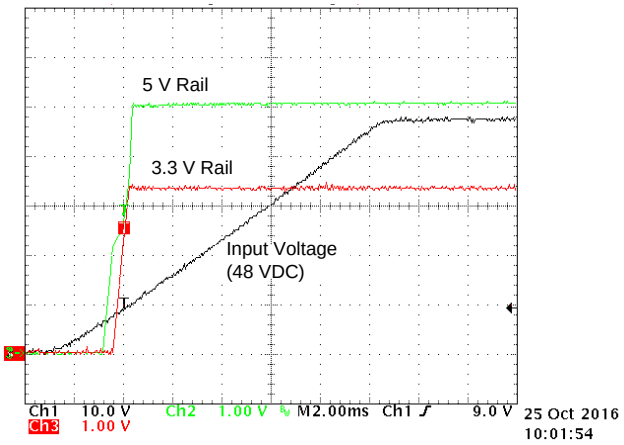


Figure 24. System Power-up (48-V Input, 5-V Rail, and 3.3-V Rail)

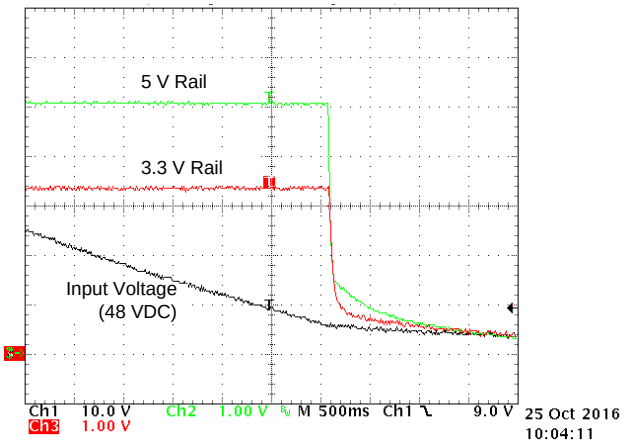


Figure 25. System Power Down (48-V Input, 5-V Rail, and 3.3-V Rail)

The UVLO of the LM5018 is set to 7.5 V. After the input voltage reaches the UVLO threshold, the LM5018 turns on and the 5-V output voltage rise. After the 5 V reaches 3.3 V, the LDO turns on. The slight delay in the ramp up is due to the peak current limit feature of the LM5018 to charge the large 3.3-V bulk capacitor of 100-µF at the output 3.3-V LDO output.

4.1.2 Power-up of INA240 Phase Current Output Voltage

The focus of this test was to validate the INA240 current sense amplifier output voltages (phase current I_A, I_B, and I_C) during power-up. The TIDA-00913 board was tested standalone without a motor and without a host processor connected. Figure 26 shows the phase current output voltage I_A, I_B, and I_C at the interface connector J1-14, J1-16, and J1-18 during VDC power-up, until the 3.3-V rail. All three phases currents I_A, I_B, and I_C track during power-up and power-down and settle at the mid bias voltage of 1.65 V, corresponding to a zero phase current.

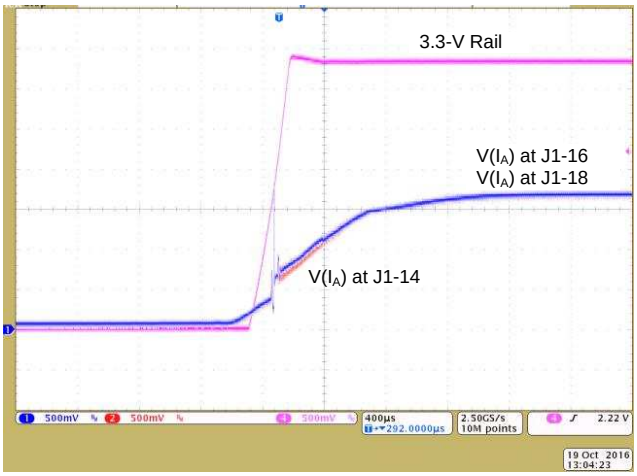


Figure 26. Phase Voltage V_A, V_B, V_C (Connector J3) During 48-V Power-up

4.1.3 5-V and 3.3-V Rails and Supply Current

The AC ripple of the 5-V rail remains well below 20 mVpp in light-load and typical load conditions, including the C2000 InstaSPIN-MOTION LaunchPad (see Figure 27 and Figure 28). See typical load currents in Section 4.2.

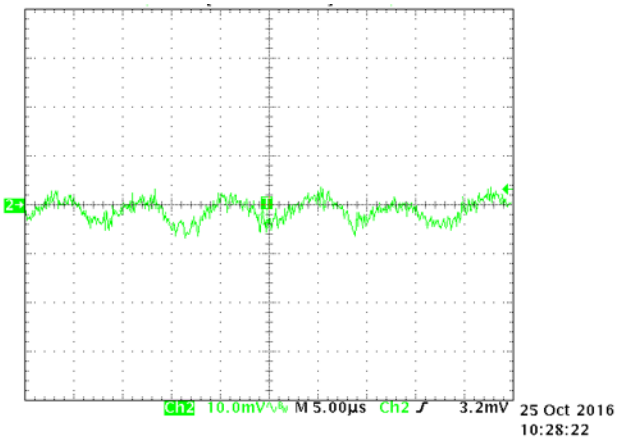


Figure 27. 5-V Ripple at Nominal Load (12 mA)

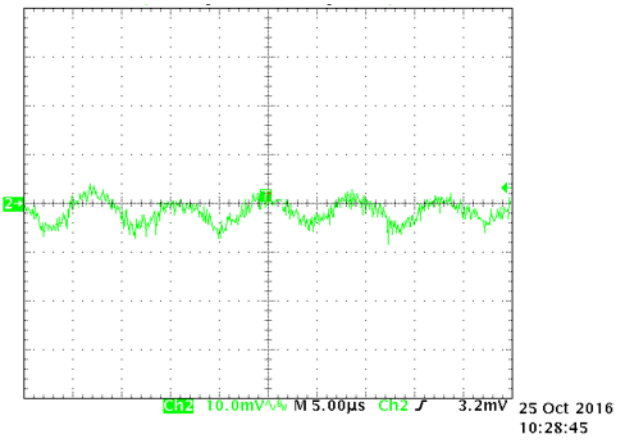


Figure 28. 5-V Ripple at 167-mA Load Current Powering C2000 LaunchPad Tool

Table 10. TIDA-00913 Total Current Consumption at 5 V and 3.3 V for 40-kHz and 100-kHz PWM

SUPPLY RAIL	CURRENT AT 40-kHz PWM	CURRENT AT 100-kHz PWM
3.3 V	7.8 mA	7.8 mA
5 VSection 2.1.2	12 mA	13.7 mA

The 5-V load current can be split into subcircuits as Table 11 shows:

Table 11. Current Consumption at 5-V Split into Subcircuits

SUBCIRCUITS DRIVEN BY 5-V RAIL	CURRENT AT 40-kHz PWM	CURRENT AT 100-kHz PWM
3.3-V rail (input to LDO U7)	7.8 mA	7.8 mA
5-V LED (D5)	2 mA	2 mA
REF3333 (U10)	0.1 mA	0.1 mA
LMG5200 (U1, U2, U3)	0.7 mA, 0.7 mA, 0.7 mA	1.26 mA, 1.26 mA, 1.26 mA

The 3.3-V load current is independent of the PWM switching frequency and can be split into subcircuits as Table 12 shows:

Table 12. Current Consumption at 3.3-V Split into Subcircuits

SUBCIRCUITS DRIVEN BY 5-V RAIL	CURRENT
3.3-V LED (D6)	1.5 mA
TMP302 (U10)	< 100 µA
SN74AVC8T245 (U4)	≈ 1 mA (driving 6× 10-k pulldown resistors)
INA240 (U8, U9, U11)	1.8 mA, 1.8 mA, 1.8 mA

In the typical use case, the TIDA-00913 device provides the 3.3-V supply rail to also power the LaunchPad. This configuration ensures proper sequencing of the 3.3-V rail on the LaunchPad as well as on the TIDA-00913 device. With the F28069M LaunchPad running the TIDA-00913 InstaSPIN-FOC firmware example, the additional current drawn by the LaunchPad was 155 mA at the 3.3-V rail. This result yields a total of 163 mA drawn from the 3.3-V rail.

The losses in the 3.3-V LDO are around 277 mW, which yields a maximum junction temperature of 99ºC at an 85ºC ambient temperature, based on the WSON package junction-to-ambient thermal resistance of 50.3ºC/W. Assuming a maximum load current of 300 mA, the maximum junction temperature is estimated to be 111ºC at an 85ºC ambient temperature.

4.2 Phase Current Sensing

The 5-mΩ current shunt is connected to the switch node of the LMG5200 GaN half-bridge power module and the differential input of the INA240 current sense amplifier. Therefore it is important to validate the common mode transient voltage in order to characterize the INA240. Unlike Si-FET, the LMG5200 has a much better switching performance and common mode voltage transients are in the range of 25 to 50 V/ns.

For more details and test results on the GaN inverter switching performance and switch node rise and fall times, see the TIDA-00909 TI Design.

The common-mode voltage transient seen at the INA240 is therefore much higher compared to using Si-FETs. Therefore, testing with GaN FETs is a higher challenge for in-line current sense amplifiers and the following test result outline the excellent performance of the INA240 at these high common-mode transients.

For the test, the optional EMI filter was connected between the TIDA-00913 motor-terminal output and the phase input of the Teknic low-voltage servo motor as the load.

The C2000 MCU was configured to generate a three-phase space vector with a complementary PWM with 100-kHz switching frequency and 12.5-ns deadband. The PWM duty cycle per phase was configured to drive the corresponding phase current I_A with $I_B = I_C = –0.5\ I_A$.

The LMG5200 switch node voltage was measured at the LMG5200 SW pin (pin 8), which is referenced to the PGND through close to the LMG5200 PGND pin (pin 9), as Figure 29 shows.

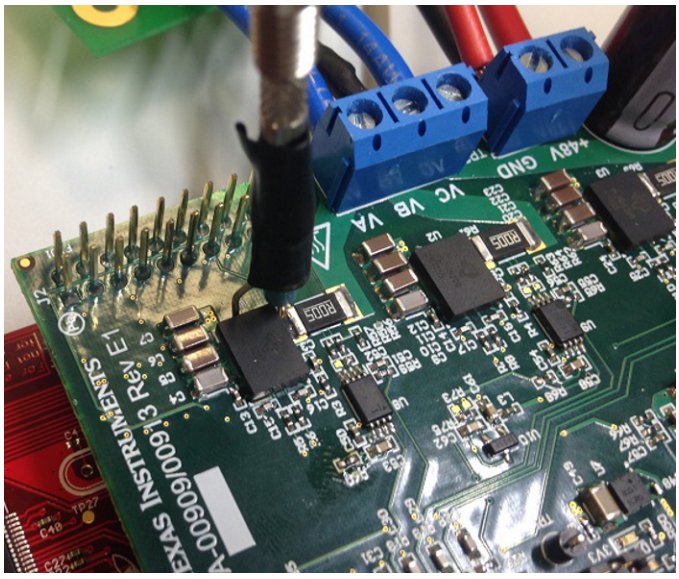


Figure 29. Test Setup for LMG5200 Switch Node Measurement (Pin SW to PGND) With Single-Ended Probe

4.2.1 Phase Current Shunt Common-Mode Voltage Transients

The following figures outline the phase (switch node) voltage transient from 0 to 48-V and vice versa, for hard and soft switching of the upper or lower GaN FET, depending on the phase current direction. Only phase A is shown; the other phases B and C had the same performance. The maximum common-mode transient voltage is in the range of 50 V/ns. The 12.5-ns PWM dead band can be well identified during the transition.

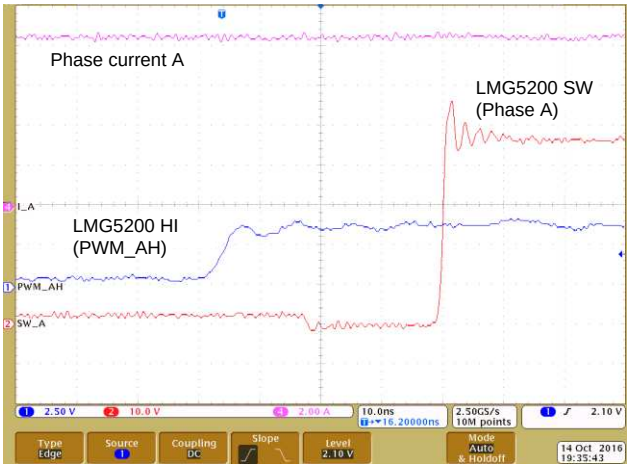


Figure 30. Phase A Rising SW, Phase Current, and LMG5200 PWM (HI) at 48 V/10 A

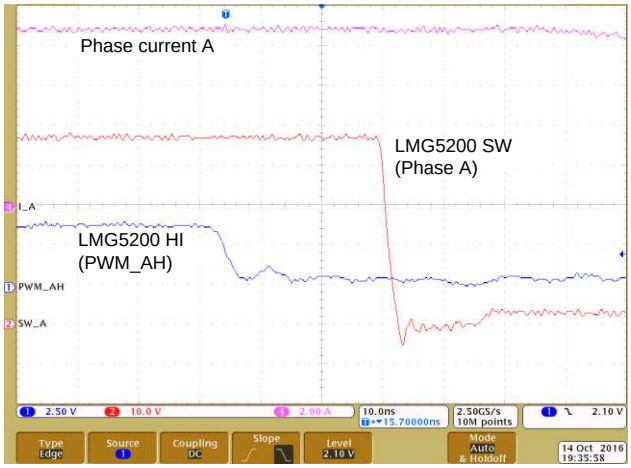


Figure 31. Phase A Falling SW, Phase Current, and LMG5200 PWM (HI) at 48 V/10 A

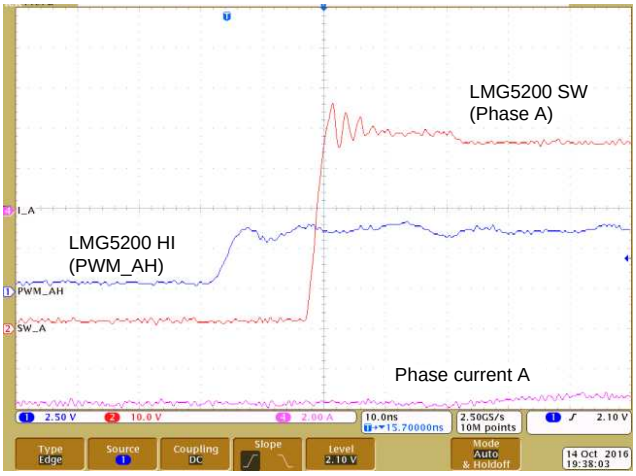


Figure 32. Phase A Rising SW, Phase Current, and LMG5200 PWM (HI) at 48 V/–10 A

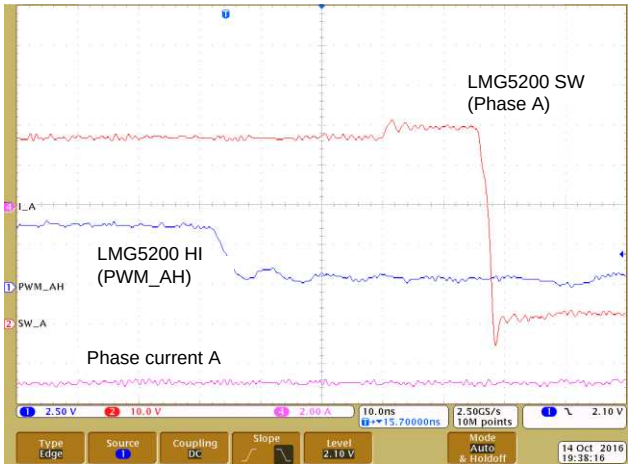


Figure 33. Phase A Falling SW, Phase Current, and LMG5200 PWM (HI) at 48 V/–10 A

4.2.2 Phase Current Transfer Function

Figure 34 shows the transfer function of phase current through the 5-mΩ shunt resistor versus the output voltage of the INA240. The output voltage equals 1.65 V, when the phase current is zero. Note that the output voltage is inverted versus the motor phase for optimized layout.

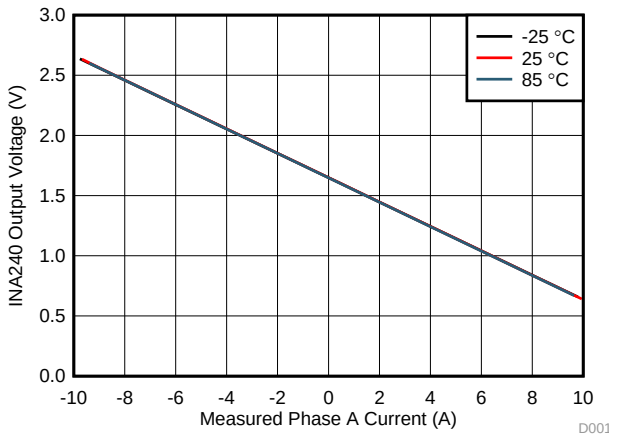


Figure 34. Phase-A Rising SW, Phase Current, and LMG5200 PWM (HI) at 48 V and 1 A

4.2.3 Phase Current Accuracy

The focus of this test is to measure the DC accuracy of the INA240A1 with 5 mΩ and the INA240 with a 20-V/V gain at –25°C, 25°C, and 85°C ambient temperature and 48-V DC bus voltage. The load used was the Teknic low-voltage servo motor.

The full-scale phase current range is –16.5 to 16.5 A, the nominal phase current range (safe operating area of the three-phase inverter) is –10 to 10 A.

The test at 85°C ambient and phase currents greater than 3.5-V DC up to 10-A DC was done within a few seconds for each step to ensure that the junction temperature of each of the three LMG5200 half-bridge power modules did not exceed 125°C.

The phase currents I_A, I_B, and I_C were measured with a precision multimeter in series to the motor phases and compared against the output voltage of the corresponding current sense amplifier INA240 measured with another precision multimeter at the interface connector J1, respectively. One phase was tested at a time. Figure 35 shows the test setup principle.

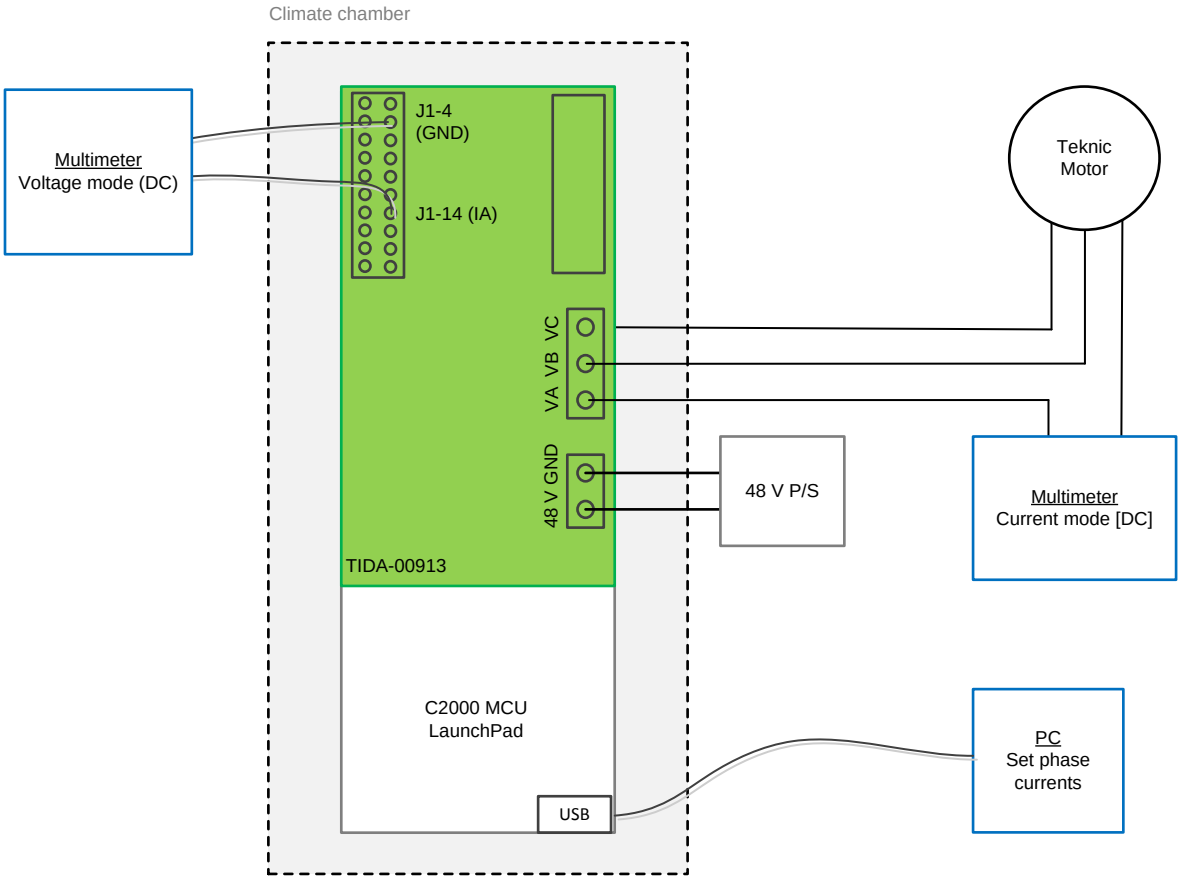


Figure 35. Test Setup Principle (Phase A Test) With C2000 MCU LaunchPad to Configure Phase Current

Figure 36 shows the climate chamber used in this test.

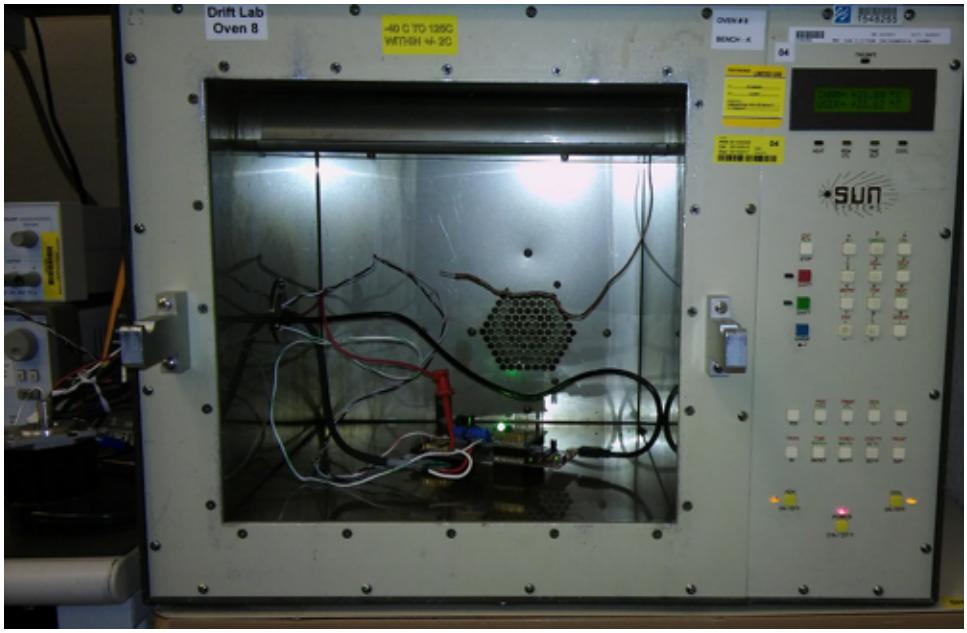


Figure 36. Test Setup Picture With Climate Chamber

Measurements were done with DC values. The C2000 was configured to generate a three-phase PWM sinusoidal voltage with configurable amplitude, frequency, and phase. For the accuracy test, the frequency was set to 0 Hz, and the amplitude and phase was adjusted to drive the corresponding phase currents in 1-A steps. For example, for phase A, the relation between the three phase currents was $I_A = –0.5 \times I_C = –0.5 \times I_C$.

Figure 37 shows the uncalibrated error of the phase currents I_A, I_B, and I_C at –25°C, 25°C, and 85°C, respectively.

Note that the major impact on gain tolerance is from the 5-mΩ shunt resistor (CRE2512 High Power Current Sense Chip). The resistance tolerance is ±1% and the temperature coefficient is 50 ppm/°C. The INA240A1 has a gain tolerance of 0.2% and a gain drift of 50 ppm/°C.

The absolute error remains within ±0.17 A, with respect to the full scale input current range from –16.5 to 16.5 A.

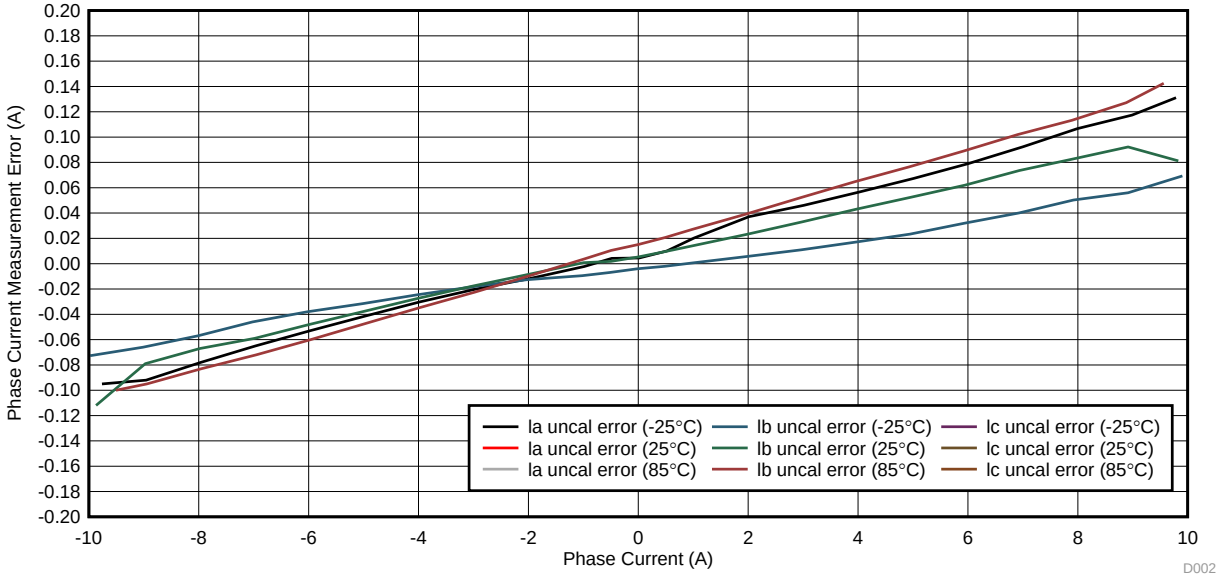


Figure 37. Absolute (Uncalibrated) Error of Phase Current I_A, I_B, and I_C at –25°C, 25°C, and 85°C

The following three figures outline the phase current measurement error with a one-time calibration of offset and gain at 25°C.

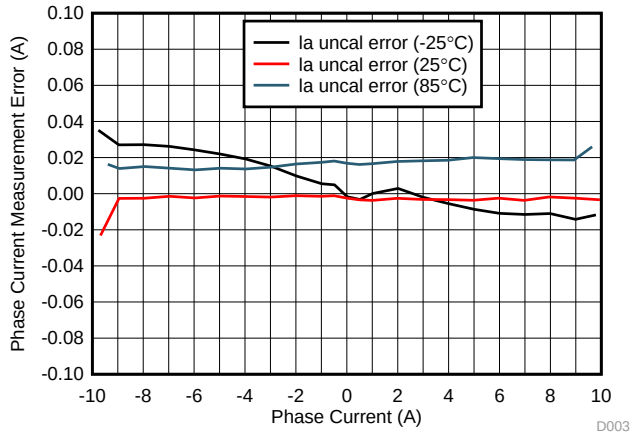


Figure 38. Absolute (Calibrated) Error of Phase Current I_A at –25°C, 25°C, and 85°C

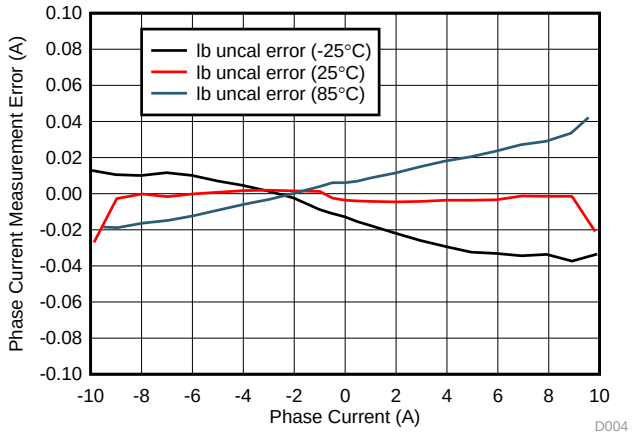


Figure 39. Absolute (Calibrated) Error of Phase Current I_B at –25°C, 25°C, and 85°C

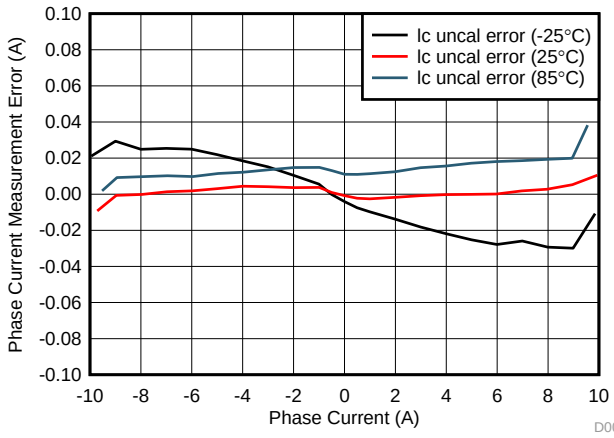


Figure 40. Absolute (Calibrated) Error of Phase Current I_C at –25°C, 25°C, and 85°C

Figure 41 shows calibrated and uncalibrated phase A current error comparison. The absolute uncalibrated error remains below ±0.5% over the entire temperature range from –25°C to 85°C. The absolute calibrated error (one-time calibration at 25°C) remains below ±0.1% over the entire temperature range from –25°C to 85°C.

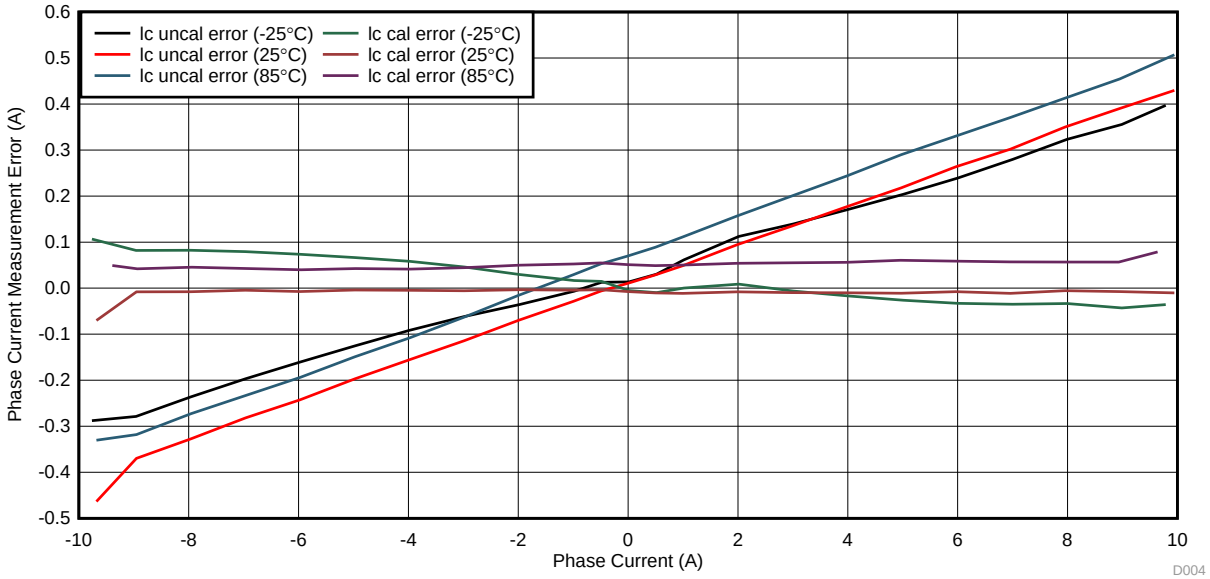


Figure 41. Absolute Calibrated and Uncalibrated Error in % of Phase Current I_A at –25°C, 25°C, and 85°C

4.2.4 Phase Current Transient Response

The focus of this test is to evaluate the common-mode transient rejection of the INA240 due to PWM switching with a 5-mΩ shunt connected to the INA240 with a 20 V/V gain and no RF low-pass filter at the INA240 differential input.

The load is a Teknic low-voltage synchronous servo motor. The test has been done at a 7-A_{RMS} phase current with a 10-Hz frequency with 48-V DC and 40-kHz PWM.

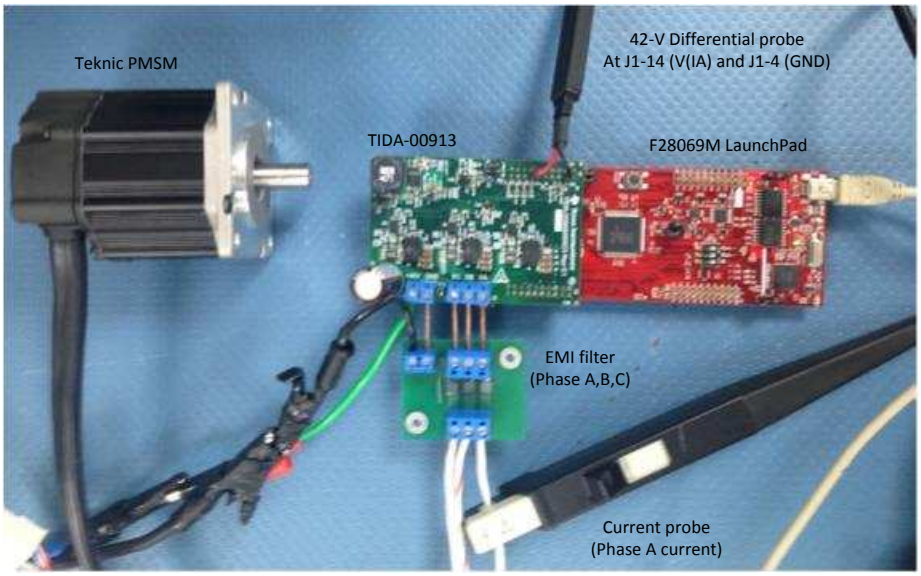


Figure 42. Test Setup for Transient Phase Current Output Voltage Measurement

All three-phase current output voltages showed the same transient response, the following figures show the transient response measured at maximum positive amplitude (10 A), zero crossing and maximum negative amplitude (–10 A) of the phase current I_A. Note that the phase current at the INA240 is inverted for optimized PCB layout in this TI Design.

Figure 43 to Figure 45 show the DC-link voltage AC ripple measured at the 220-µF bulk capacitor with a 24-V and 48-V DC input. The PWM switching frequency was set to 40 kHz. The AC ripple voltage remains below 400 mVpp.

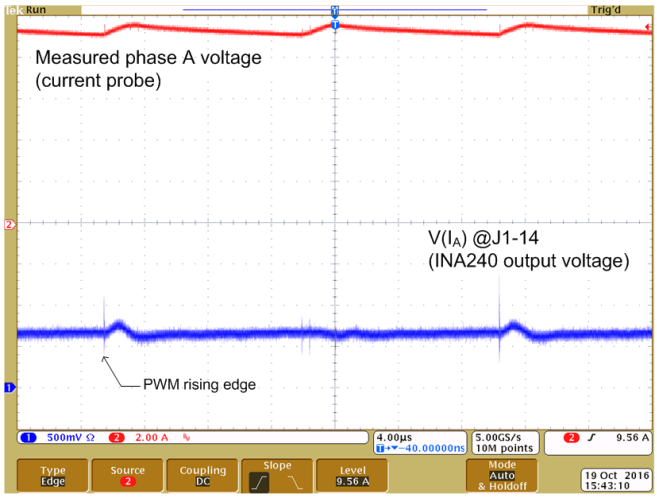


Figure 43. Phase Current I_A Output Voltage at J1-14 at 40-kHz PWM and 48-V DC Bus Voltage 10 A

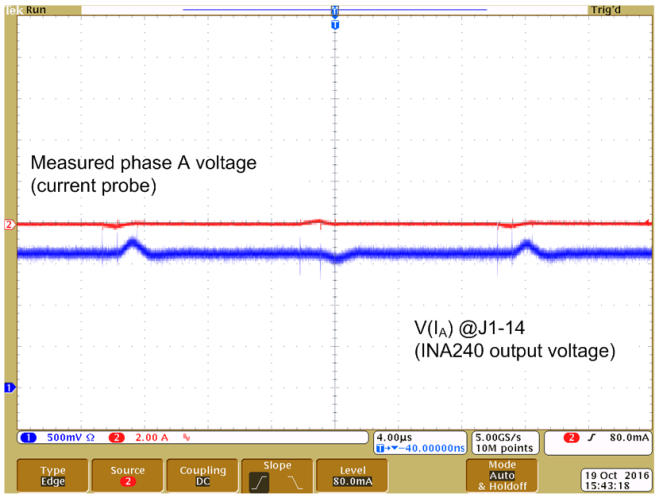


Figure 44. Phase Current I_A Output Voltage at J1-14 at 40-kHz PWM and 48-V DC Bus Voltage 0 A

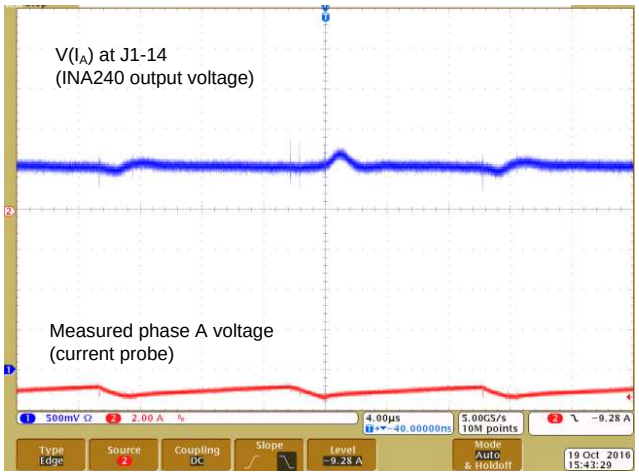


Figure 45. Phase Current I_A Output Voltage at J1-14 at 40-kHz PWM and 48-V DC Bus Voltage –10 A

The following four scope plots show the measured with a single ended probe at the interface J1-14 (phase I_A output voltage scaled from 0 to 3.3 V) and the common-mode phase voltage to PGND at the phase current shunt. Note that the common-mode transients are extremely high due to use of fast switching GaN power modules with 20 to 50 V/ns. Therefore, impulse noise is coupled into GND during PWM switching of the measured and adjacent phases.

The figures outline the excellent common-mode rejection of the INA240 and the output settles in around 2 µs even after a very high transient of around 48 V/ns and maximum load current of 10 A. Even at maximum current of 10 A, the overshoot at the INA240 output remains below 150 mV, equivalent to 1.5 A. This is less than 4.5% versus the full scale range of 33 A (–16.5 to 16.5 A) and outlines the excellent performance of the INA240 PWM rejection.

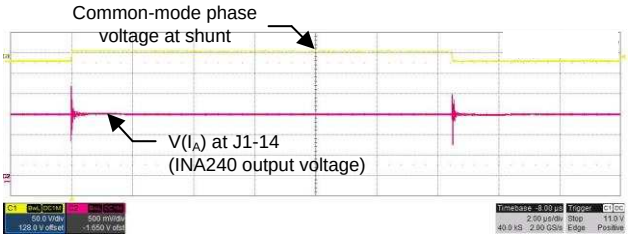


Figure 46. Phase Current I_A Output Voltage at J1-14 at 40-kHz PWM, 0 A, and 24-V DC Bus Voltage

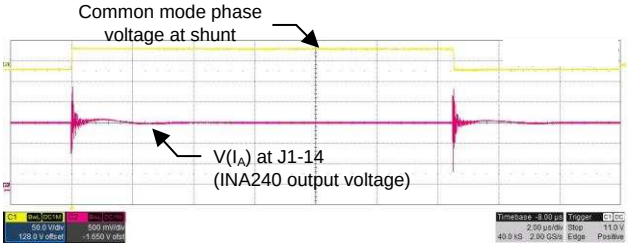


Figure 47. Phase Current I_A Output Voltage at J1-14 at 40-kHz PWM, 0 A, and 48-V DC Bus Voltage

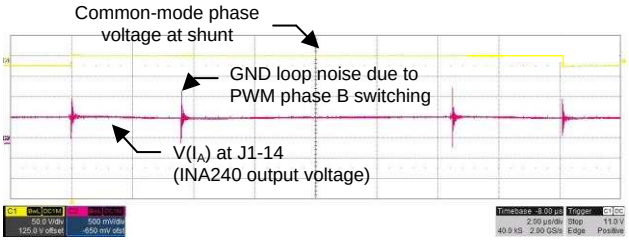


Figure 48. Phase Current I_A Output Voltage at J1-14 at 40-kHz PWM, 10 A, and 24-V DC Bus Voltage

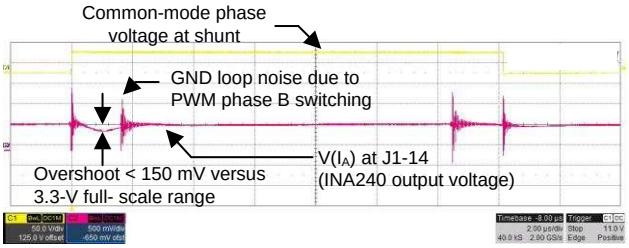


Figure 49. Phase Current I_A Output Voltage at J1-14 at 40-kHz PWM, 10 A, and 48-V DC Bus Voltage

The following measurement was done with the C2000 MCU embedded 12-bit ADC capturing the phase current output voltage over one half PWM cycle. The ADC sample trigger was shifted by one CPU cycle (12.5 ns) respectively to get an interleaved sample representation of the phase current output voltage over one half PWM period. For that test, the phase current I_A was set to 5-A DC, to measure during the hard-switching transition of the rising phase A switched voltage, which had the highest common-mode transient voltage of 48 V/2 ns. Phase currents I_B and I_C were set to –2.5-A DC. A blanking time of around 2.5 µs after the PWM switching is recommended prior to sampling the analog output voltage of the INA240 to ensure the output voltage has settled back to the sensed phase current.

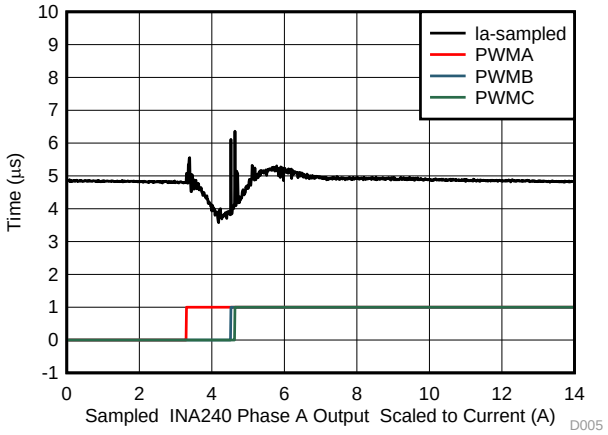


Figure 50. Phase Current I_A at 5-A DC Sampling Interleaved With C2000 MCU Over one Half PWM Cycle at 48-V DC Bus Voltage

4.2.5 Continuous Output Current Safe Operating Area

Figure 51 shows the maximum three-phase AC current for the TIDA-00913 design at 40-kHz and 100-kHz PWM switching frequency with natural convection.

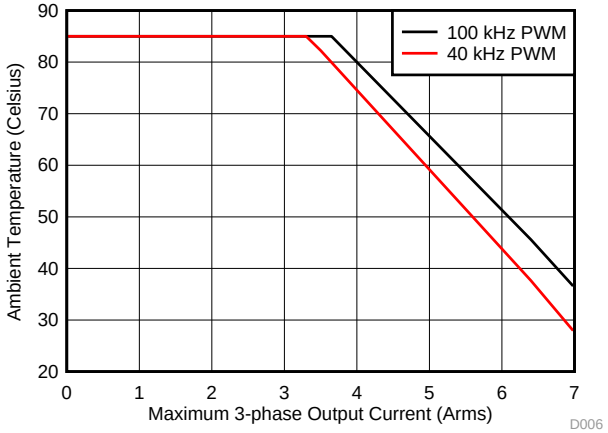


Figure 51. Safe Operating Area With Natural Convection

4.3 Phase Voltage and DC Bus Voltage Sensing

The focus of this test is to measure the DC-link voltage and the AC phase-to-phase voltage like seen in a speed-variable drive. For this test, a sinusoidal space vector PWM (40-kHz) with a 2-V_{RMS} amplitude and 10-Hz frequency was generated and the corresponding filtered phase voltage V_A at the interface pin J1-8 and the DC-link input voltage VDC at interface pin J1-6 was captured with the C2000 MCU embedded 12-bit ADC. Based on the resistor divider ratio of 24.7 [(100 kΩ + 4.22 kΩ) / 4.22 kΩ] the measured input DC voltage was 1.95 V × 26.7 = 48.1 V.

Figure 52 shows the captured results.

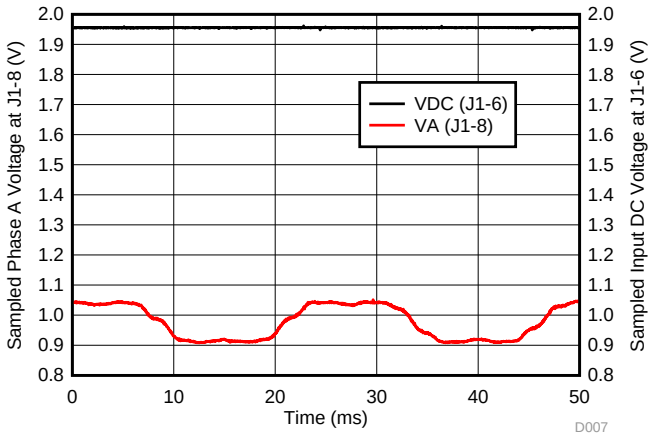


Figure 52. Test Setup for Inverter Efficiency Analysis

4.4 System Test With High-Speed Synchronous Motors

4.4.1 High-Speed BLDC Motor for Drones

The following tests have been performed with a low-inductance, high-speed BLDC motor, such as that used with drones. The motor was driven with sinusoidally-impressed phase currents with 2 V_{RMS} of amplitude and a 1000-Hz frequency. The PWM switching frequency was set to 100 kHz. The test has been done with an optional EMI output filter as the test setup in Figure 53 shows. The scope probes were connected to the phase V_C motor terminal and the filtered-phase V_C output after the EMI output filter was referenced to GND. A current probe was used to measure the phase current I_C.

The electric parameters of the low-inductance BLDC motor stator are:

- R_S = 0.05 Ω, L_S = 4.1 µH, I_{MAX} = 4.5 A_{RMS}

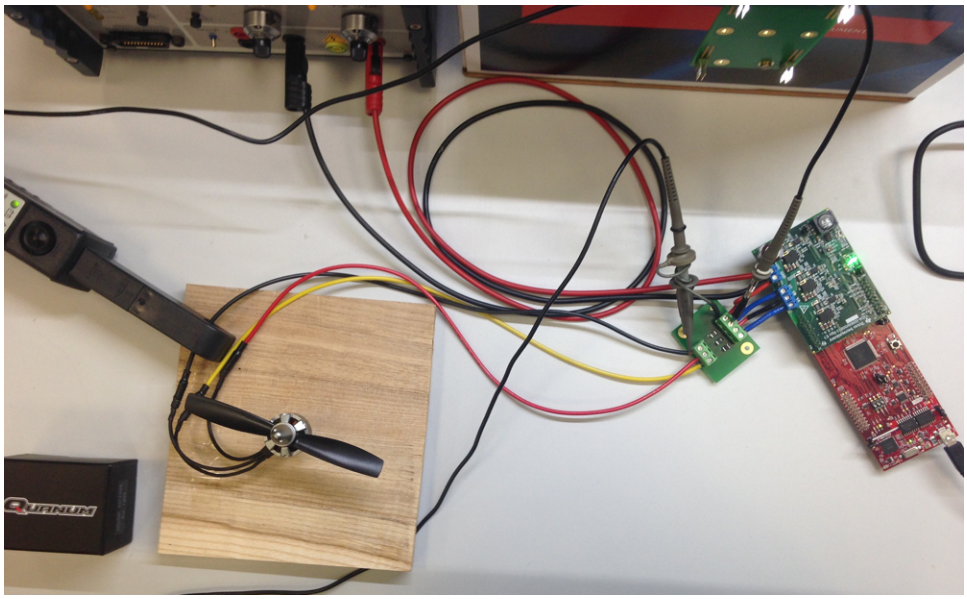


Figure 53. Test Setup Image With Oscilloscope Probe Points

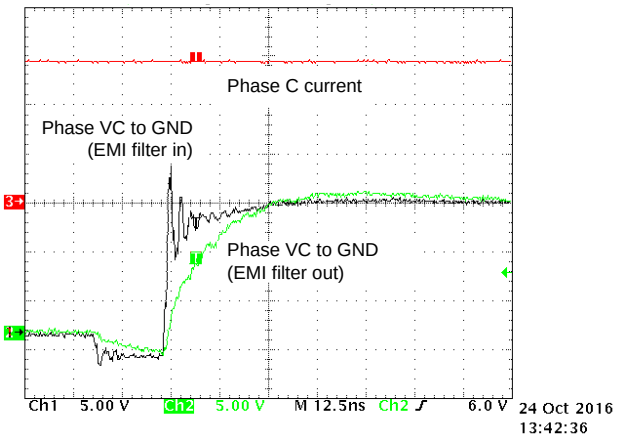


Figure 54. Phase Voltage V_C, $V_{C\text{-}EMI}$, and Phase Current I_C at 100-kHz PWM With ESC PMSM

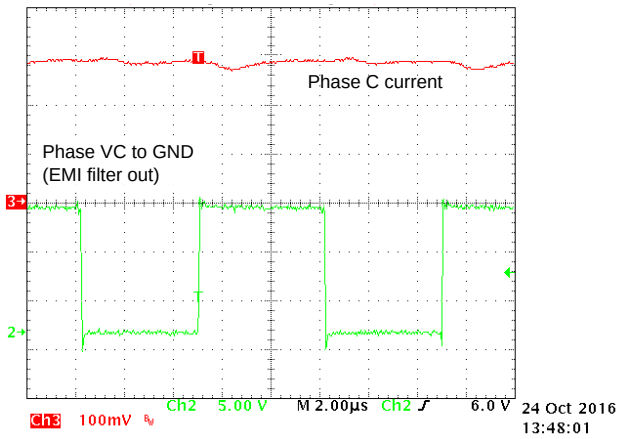


Figure 55. Zoom-in of Figure 54 to Show I_C Phase Current Ripple

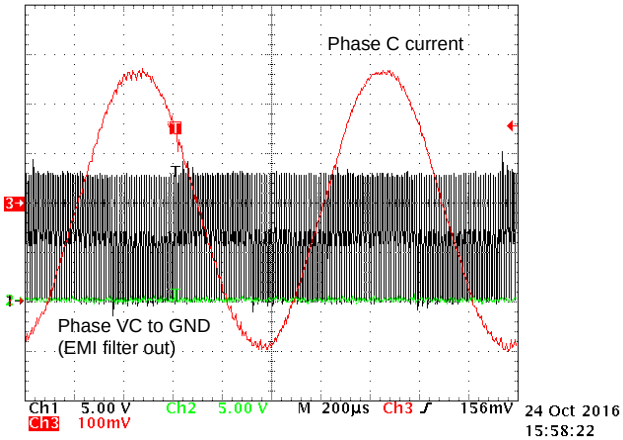


Figure 56. Zoom-out of Figure 54 to Show Phase Current I_C Period

As expected with the EMI LCR low-pass filter, the rise time of the transient phase voltage referenced to GND is reduced to around 25 ns.

Due to the high PWM frequency, the BLDC motor phase-current ripple at 100-kHz PWM is reduced to ±100 mA.

To validate the TIDA-00913 phase current sensing and phase voltage feedback network, the corresponding voltages for I_C (pin J1-18) and V_C (pin J1-12) were measured with the C2000 MCU-embedded 12-bit ADC center aligned to the 100-kHz PWM. The values shown represent the measured voltage at the corresponding interface pins for I_C (pin J1-18) and V_C (pin J1-12). Note that the output voltage of the phase current sense amplifier is inverted and has a 1.65-V offset. Applying the correct scaling factor $I_{A\text{-}PEAK} = (V(I_A) – 1.65\ V) \times 10\ A/V = (1.935\ V – 1.65\ V) \times 10\ A/V = 2.85\ A_{PEAK}$ (2 V_{RMS}).

The following figures show all three corresponding voltages for phase currents I_A (pin J1-14), I_B (pin J1-16), and I_C (pin J1-18).

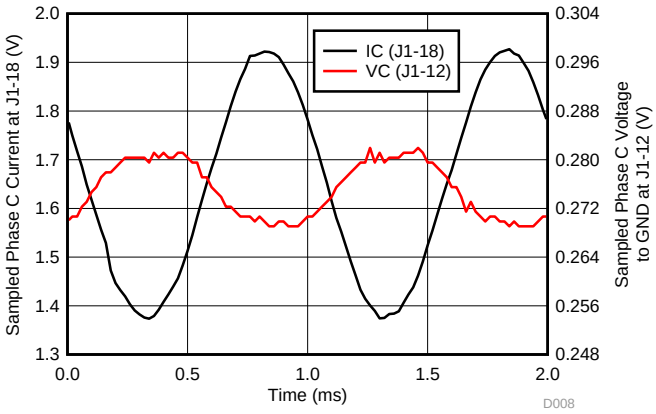


Figure 57. Phase Current I_C Output Voltage and V_C Phase-to-GND Voltage Sampled With C2000 MCU Center-Aligned at 100-kHz PWM

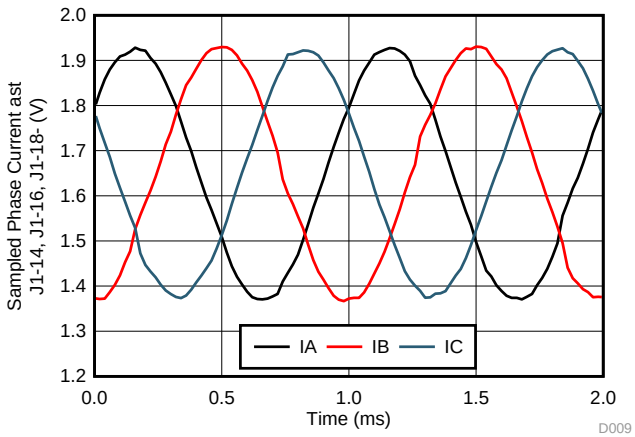


Figure 58. Phase Currents I_A, I_B, and I_C Output Voltage Sampled With C2000 MCU Center-Aligned at 100-kHz PWM

4.4.2 Low-Voltage Servo Motor (Teknic)

The following tests have been performed with a low-voltage synchronous servo motor Teknic M-2310P-LN-04K (four pole pairs), which may be used with servo drives. The motor was driven with sinusoidally-impressed phase currents with 2 V_{RMS} of amplitude and 100-Hz frequency. The PWM switching frequency was set to 40 kHz. The test has been done with an optional EMI output filter as previously shown. The scope probes were connected to the phase V_C motor terminal and the filtered phase V_C output after the EMI output filter was referenced to GND. A current probe was used to measure the phase current I_C.

The Teknic M-2310P-LN-04K synchronous motor stator electric parameters are:

- R_S = 0.363 Ω, L_S = 160 µH, I_{MAX} = 7 A_{RMS}

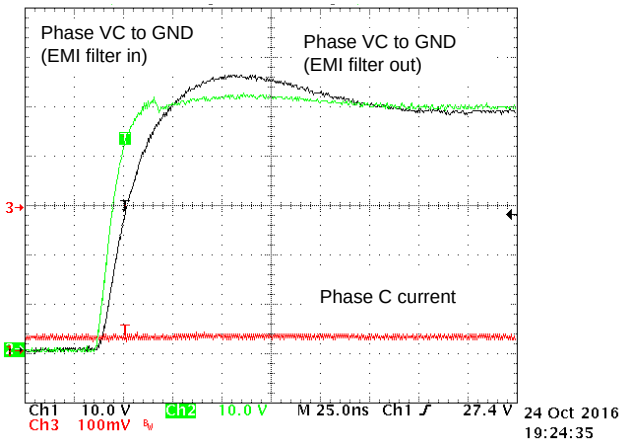


Figure 59. V_C at EMI Input and EMI Output Filter and Phase Current I_C at 40-kHz PWM With PMSM

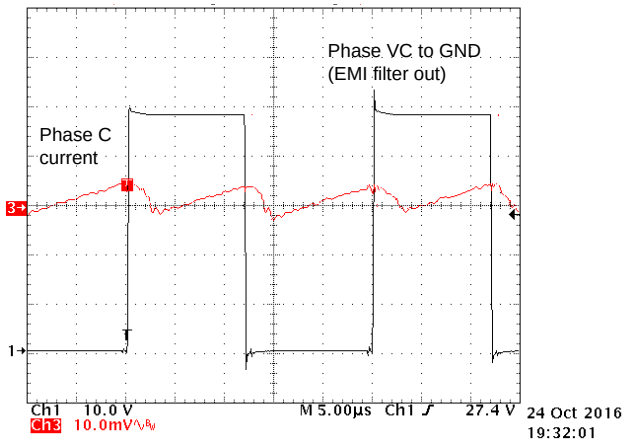


Figure 60. Zoom-in of Figure 59 to Show I_C Phase Current Ripple

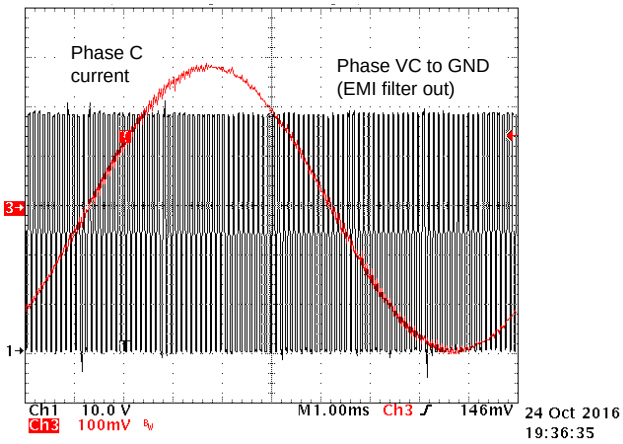


Figure 61. Zoom-out of Figure 59 to Show Phase Current I_C Period

Figure 62 and Figure 63 show all three corresponding phase voltages sampled at the TIDA-00913 interface J1-6, J1-8, and J1-10, as well as the equivalent voltages of the phase currents I_A (pin J1-14), I_B (pin J1-16), and I_C (pin J1-18). A peak voltage of 1.935 V equals a phase current of (1.935 V – 1.65 V) × 10 = 2.85 V_{PEAK} or 2 V_{RMS}.

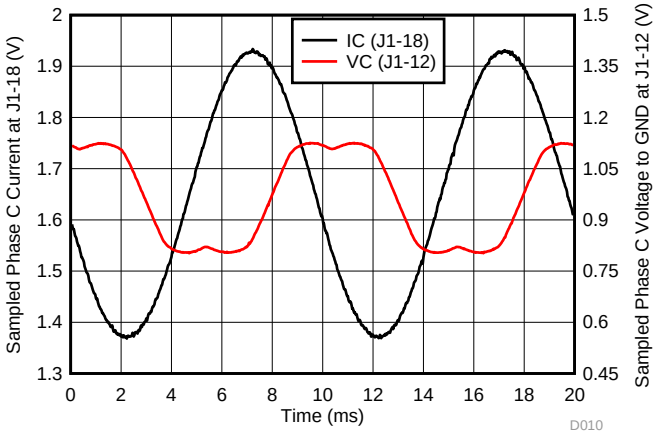


Figure 62. Phase Voltages V_A, V_B, and V_C Output Voltage Sampled With C2000 MCU Center-Aligned at 40-kHz PWM

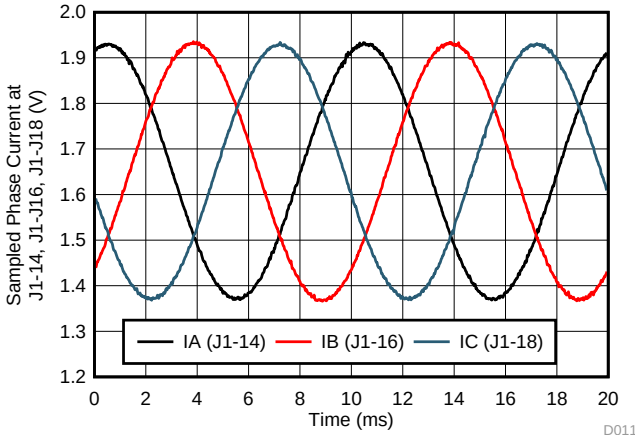


Figure 63. Phase Currents I_A, I_B, and I_C Output Voltage Sampled With C2000 MCU Center-Aligned at 40-kHz PWM

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00913.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00913.

5.3 PCB Layout Recommendations

For layout recommendations of the LMG5200, see the TIDA-00909 design.

Careful layout is an integral part of the phase current sensing circuit design. Kevin connection must be adopted to minimize the parasitic resistance in the measurement path (see Figure 64).

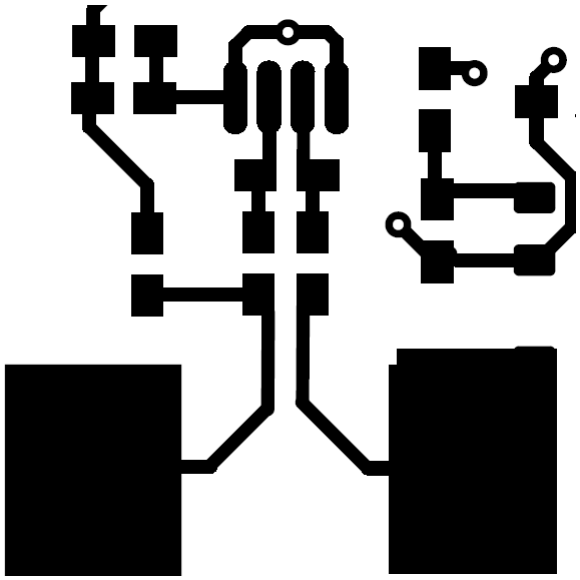


Figure 64. Shunt With Kelvin Connection to INA240 Inputs

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00913.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00913.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00913.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00913.

6 Software Files

To download the software files, see the design files at TIDA-00913.

7 Related Documentation

1. Texas Instruments, *Layout Considerations for LMG5200 GaN Power Stage*, LMG5200 Application Report (SNVA729)
2. Texas Instruments, *Optimizing GaN Performance with an Integrated Driver*, White Paper (SLYY085)
3. Texas Instruments, *GaN FET Module Performance Advantage over Silicon*, White Paper (SLYY071)
4. Texas Instruments, *Gallium Nitride (GaN) Solutions*, Overview Page (www.ti.com/gan)
5. Texas Instruments, *REF33xx 3.9-µA, SC70-3, SOT-23-3, and UQFN-8, 30-ppm/ºC Drift Voltage Reference,*, REF33xx Datasheet (SBOS392)
6. Texas Instruments, *48-V, 10-A, High-Frequency PWM, 3-Phase GaN Inverter Reference Design for High-Speed Motor Drives*, TIDA-00909 Design Guide (TIDUCE7)
7. Texas Instruments, *LP3869x/-Q1 500-mA Low-Dropout CMOS Linear Regulators Stable With Ceramic Output Capacitors,*, LP3869x/LP3869x-Q1 Datasheet (SNVS321)
8. Texas Instruments, *WEBENCH® Design Center*, Overview Page (www.ti.com/webench)
9. Texas Instruments, *TINA-TI Simulation Software*, Overview Page (www.ti.com/tina-ti)
10. Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DC-DC Converters,* AN-2162 Application Report (SNVA489)
11. Texas Instruments, *TI InstaSPIN™ Motor Control Solutions*, Overview Page (www.ti.com/ww/en/mcu/instaspin/)
12. Texas Instruments, *MotorWare™ Software*, MotorWare Tool Folder (www.ti.com/tool/motorware)
13. Texas Instruments, *Low Voltage Servo Motor - Low voltage servo (encoder) motor and wiring harness*, LVSERVOMTR Tool Folder (www.ti.com/tool/lvservomtr)
14. DYS, *Quanum MT Series 2208 1800KV Brushless Multirotor Motor* (www.dys.hk)
15. Texas Instruments, *Current Sensing for Inline Motor-Control Applications*, Application Report (SBOA172)
16. Texas Instruments, *Low-Drift, Precision, In-Line Motor Current Measurements With Enhanced PWM Rejection*, TI Tech Note (SBOA160)

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8 Terminology

GaN— Gallium nitride

HEMT— High-electron mobility transistor

9 About the Authors

MARTIN STAEBLER is a system architect in the Industrial Systems-Motor Drive team at Texas Instruments, where he is responsible for specifying and developing reference designs for industrial drives.

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9.1 Recognition

The author would like to recognize the excellent contributions from **PAWAN NAYAK** and **KRISTEN MOGENSEN** on the TIDA-00913 schematics and layout capture, the TIDA-00913 test software development, and the TIDA-00913 design test and validation.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2016) to A Revision	Page
• Changed language and images to fit current style guide	1
• Added TIDA-00909 design guide (TIDUCE7) to Section 7	42
• Added AN-2162 application report (SNVA489) to Section 7	42
• Added current sensing application report (SBOA172) to Section 7	42
• Added TI tech note (SBOA160) to Section 7	42

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