TI Designs

48-V, 10-A, High-Frequency PWM, 3-Phase GaN Inverter Reference Design for High-Speed Motor Drives

Description

Low-voltage, high-speed drives and low-inductance brushless motors require higher inverter switching frequencies in the range of 40 kHz to 100 kHz to minimize losses and torque ripple in the motor. The TIDA-00909 reference design achieves this by using a three-phase inverter with three 80 V, 10-A half-bridge GaN power modules (LMG5200) and uses shunt-based phase-current sensing. Gallium nitride (GaN) transistors can switch much faster than silicon field-effect transistors (FETs) and integrating the GaN FET and driver in the same package reduces parasitic inductances and optimizes switching performance to reduce losses, thus allowing the designer to downsize or eliminate the heatsink. The TIDA-00909 offers a TI BoosterPack™ Plug-in Module with a compatible interface to connect to a C2000™ MCU LaunchPad™ Development Kit for easy performance evaluation.

Resources

TIDA-00909	Design Folder
LMG5200	Product Folder
INA240	Product Folder
REF3333	Product Folder
LM5018	Product Folder
TMP302	Product Folder
TIDA-00913	Design Folder
InstaSPIN™-MOTION LaunchPad™	Tools Folder

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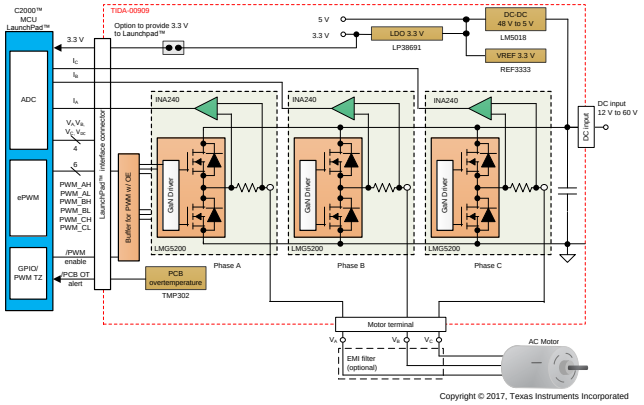
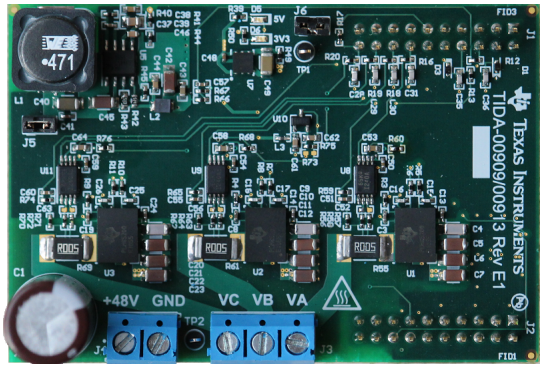
Features

- Three-Phase GaN Inverter With Wide-Input Voltage Range 12 V to 60 V and 7 A_{RMS} per 10-A Peak Output Current; Tested up to 100-kHz PWM
- GaN Power Stage With Greatly-Reduced Switching Losses Allows High PWM Switching Frequencies With Peak Efficiency up to 98.5% at 100-kHz PWM
- LMG5200 GaN Half-Bridge Power Stage Simplifies PCB Layout and Reduces Parasitic Inductances for Optimized Switching Performance; Less than 2-ns Rise and Fall Time
- Very-Low Switch Node Voltage Overshoot and Undershoot With Very-Low 12.5-ns Deadband Minimizes Phase-Voltage Ringing and reduces Phase-Voltage Distortions and EMI
- Precision Shunt-Based, Phase-Current Sensing With High Accuracy (0.1%)
- TI BoosterPack™ Compatible Interface With 3.3-V I/O for Easy Performance Evaluation With C2000™ MCU LaunchPad™ Development Kit

Applications

- Servo Drives and Motion Control
- Computer Numerical Control (CNC) Drives
- Manufacturing Robots
- Service Robots
- Non-Military Drones





1 System Overview

1.1 System Description

Low-voltage brushless AC or DC motors with low stator inductance and high-speed brushless AC or DC motors such as those used in precision applications like servo drives, CNC machines and service robots, or non-military drones require higher inverter switching frequencies in the range of 40 kHz to 100 kHz to minimize losses and torque ripple within the motor or to avoid electromagnetic interference such as with ultrasonic sensors.

The phase current ripple is inversely proportional to the pulse width modulation (PWM) switching frequency. The phase current ripple contributes to motor losses, which reduce the efficiency of the motor and increase the temperature of the motor. These losses are especially present in motor-integrated power electronics such as 48-V servo drives or 48-V, battery-operated, multi-axis drives used service robots, where any additional motor losses limit the maximum power of the device over the rated operating temperature range.

For precision servo drives, which require high position accuracy, a torque ripple can have a negative impact on statics position accuracy. The motor phase-current ripple must be reduced to reduce the torque ripple for a given motor, which can be achieved by increasing the inverter PWM switching frequency.

Non-military drones, such as quadcopters, typically employ four high-speed synchronous motors to drive the propeller speed. Ultrasonic sensors are often used for collision avoidance, landing assist, and operate up to 40 kHz and force the inverter switching frequency to 40 kHz and above.

Alternatively, the inverter losses increase with the switching frequency. With a traditional low-voltage 48-V Si-FET inverter, the switching losses at 40-kHz PWM may already be significantly higher than the conduction losses and hence dominate the overall power losses. A larger heat sink is required to dissipate the excess heat; however, this increases system cost, weight, and space.

The solution to the problem is to use GaN FETs, which have several advantages over Si-FETs. Table 1 shows an overview.

Table 1. Comparison of Silicon MOSFET and TI GaN FET (HEMT)

PARAMETER	Si-FET	TI GaN (HEMT)	COMMENTS
Device structure	Vertical	Lateral	The TI GaN FET and driver are in the same package, which reduces parasitic inductances and optimizes switching performance
Rds,on, area metric	> 10 mΩ-cm2	5 mΩ-cm2 to 8 mΩ-cm2	Lower conduction losses
SGate charge QG	≈4 nC-Ω	≈1 nC-Ω to 1.5 nC-Ω	Reduces gate driver losses and enables faster switching, lower switching losses, and lower deadband distortions
Output charge QOSS	≈25 nC-Ω	≈5 nC-Ω	Lower output capacitance enables faster switching speeds and reduces switch charging losses
Reverse recovery QRR	≈2 µC-Ω to 15µC-Ω	—	Zero reverse-recovery enables efficient half-bridge inverters and reduces or eliminates ringing in hard switching

Gallium nitride (GaN) transistors can switch much faster than silicon MOSFETs, which allows the potential to achieve lower switching losses. However, at high slew rates, certain package types can limit GaN FET switching performance. Integrating the GaN FET and driver in the same package reduces parasitic inductances and optimizes switching performance. For more details refer to the *Gallium Nitride (GaN) Solutions* overview page [4] and the REF33xx Datasheet [5].

The TIDA-00909 TI Design realizes a B6 inverter topology with three 80-V, 10-A half-bridge GaN power modules LMG5200. The LMG5200 device integrates the driver and two 80-V GaN FETs in a 6×8-mm QFN package, which is optimized for extremely-low-gate loop and power loop impedance [4]. The inputs are 3-V complementary metal-oxide-semiconductor (CMOS) and 5-V transistor-transistor logic (TTL) compatible and can be directly interfaced to a host processor like a C2000™ MCU. Figure 1 shows a simplified block diagram.

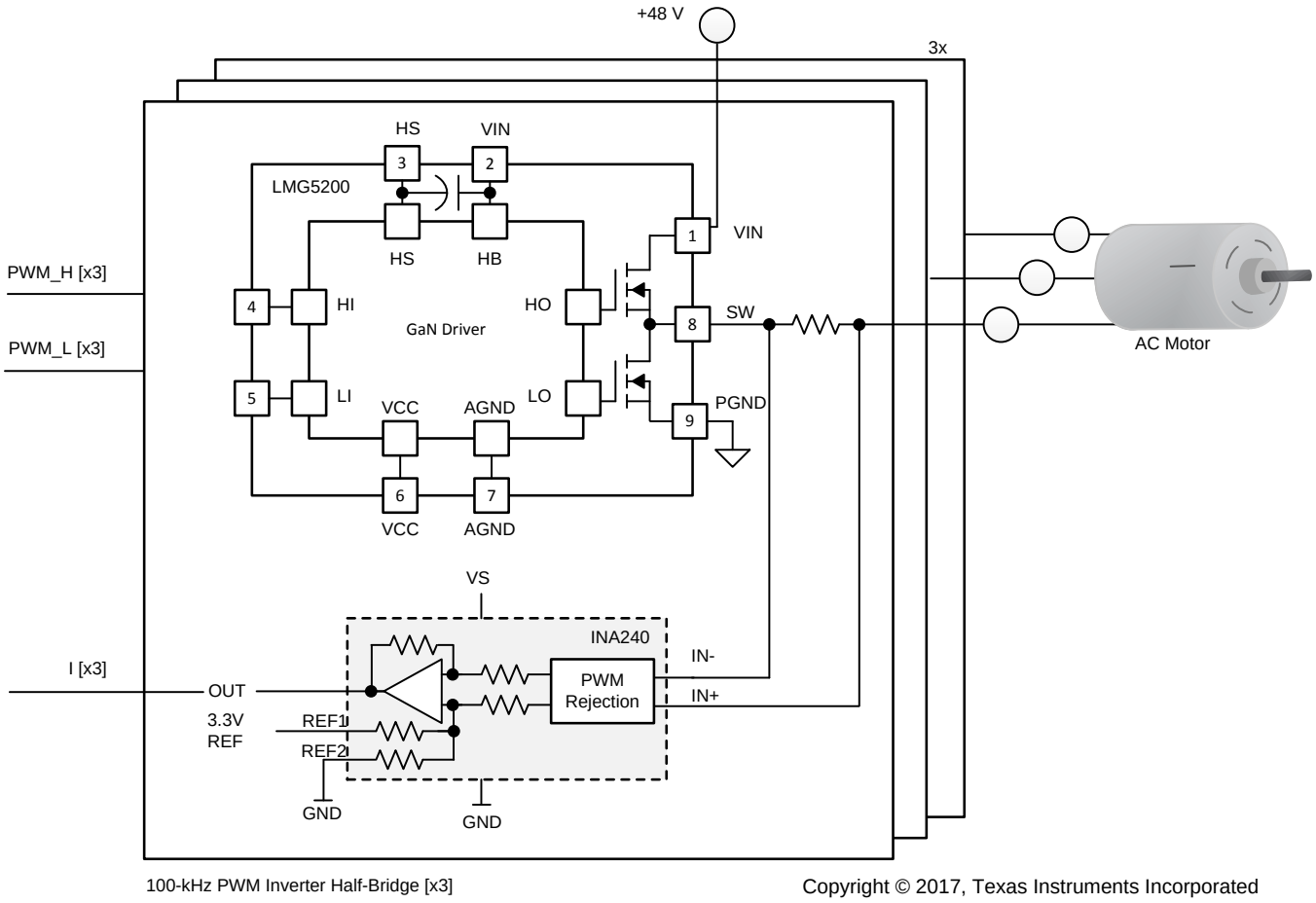


Figure 1. TIDA-00909 Three-Phase Inverter Topology

For precision phase-current measurements with high linearity, the TIDA-00909 TI Design employs a phase current shunt and a differential, precision current-sense amplifier INA240 with a high common mode and high-AC common-mode transient immunity. This high common-mode transient immunity is due to the integrated PWM rejection from the INA240 device. For more details on non-isolated, precision phase-current sensing refer to the TIDA-00913 reference design [6].

Onboard power management provides a 5-V rail to supply the LMG5200 gate driver and 3.3-V band-gap reference as well as a 3.3-V rail for the INA240 current sense amplifiers and temperature switch.

The TIDA-00909 offers a TI BoosterPack™ Plug-in Module, which is a compatible interface to connect to a C2000 MCU LaunchPad™ Development Kit for easy performance evaluation.

1.2 Key System-Level Specifications

Table 2 provides the key specifications of the TIDA-00909 high-switching frequency, three-phase GaN inverter reference design. The TIDA-00909 design is compliant to the TI BoosterPack 40-pin standard (www.ti.com/byob).

The TIDA-00909 board can be directly connected to a C2000 LaunchPad to either the first 40-pin instance (J1–J3 and J4–J2) or the second 40-pin instance (J5–J7 and J8–J6). A jumper option is provided on the TIDA-00909 to power the LaunchPad with 3.3 V. Table 3 and Table 4 introduce the TIDA-00909 pin assignment.

Table 2. Three-Phase Inverter Key Specifications

PARAMETER	TYPICAL VALUE	COMMENTS
DC input voltage	48 V (12 V to 60 V)	80-V absolute max
Maximum three-phase output current	$7A_{RMS}$ (10-A peak) per phase	Refer to Figure 62 for maximum three-phase output current versus ambient temperature with natural convection
Maximum input power	400 W (at 48 V)	—
Power FET type	GaN technology	Half-bridge power module with integrated high-side and low-side gate drivers (LMG5200)
PWM switching frequency	40 kHz to 100 KHz	—
PWM deadband	12.5 ns	—
Maximum efficiency at 100-kHz PWM	98.5%	At 400-W input power
Phase currents sense and amplifier	5-mΩ shunt per INA240	Differential, non-isolated current sense amplifier with 20 V/V and enhanced PWM rejection (INA240)(1).
Phase current maximum range	±16.5 A	Scaled to 0 V to 3.3 V; inverted with 1.65-V bias
Phase current accuracy (–25°C to 85°C)	±0.5% (uncalibrated), ±0.1% (calibrated)	Over nominal range ±10 A; one-time calibration of offset and gain at 25ºC
EMI input and output filter	External	—
PCB layer stack	Four-layer, 70-µm copper	—
PCB size	53.4 mm × 78.9 mm	Dimensions in mil: 2105 mil × 3107 mil
Temperature range	–40ºC to 85ºC	Refer to Figure 62 for maximum three-phase output current versus ambient temperature with natural convection
PCB overtemperature alert	> 85ºC	Configurable from 70ºC to 85ºC (TMP302B)
Interface-to-host processor	TI BoosterPack™ compatible	Refer to Table 3 and Table 4 for pin assignment
3.3-V supply current for LaunchPad™	300 mA or 500 mA (max), see Section 2.2	Jumper option (J3) to provide 3.3-V supply for C2000™ MCU LaunchPad™

(1) Inverted phase current output voltage for optimized layout

Table 3. Interface Specification – Header J1

PIN	SIGNAL	I/O (3.3 V)	PIN	SIGNAL	I/O (3.3 V)
J1-1	3.3-V supply (optional)	O or NC (jumper selectable)	J1-2	NC	—
J1-3	NC	—	J1-4	GND	GND
J1-5	NC	—	J1-6	VDC	O (0 V to 3.3 V)(1)
J1-7	NC	—	J1-8	VA	O (0 V to 3.3 V)(1)
J1-9	NC	—	J1-10	VB	O (0 V to 3.3 V)(1)
J1-11	VREF	O (3.3 V, 10 ppm)	J1-12	VC	O (0 V to 3.3 V)(1)
J1-13	NC	—	J1-14	IA	O (0 V to 3.3 V)
J1-15	NC	—	J1-16	IB	O (0 V to 3.3 V)
J1-17	NC	—	J1-18	IC	O (0 V to 3.3 V)
J1-19	NC	—	J1-20	VREF	O (3.3 V, 10 ppm/K)

(1) Overvoltage protection with Schottky diodes ensures output voltage remains below 3.6 V

Table 4. Interface Specification – Header J2

PIN	SIGNAL	I/O (3.3 V)	PIN	SIGNAL	I/O (3.3 V)
J2-1	PWM A (high-side)	I (10k PD)	J2-2	GND	GND
J2-3	PWM A (low-side)	I (10k PD)	J2-4	NC	—
J2-5	PWM B (high-side)	I (10k PD)	J2-6	NC	—
J2-7	PWM B (low-side)	I (10k PD)	J2-8	NC	—
J2-9	PWM C (high-side)	I (10k PD)	J2-10	NC	—
J2-11	PWM C (low-side)	I (10k PD)	J2-12	NC	—
J2-13	/PCB OT alert	O (open drain, 10k PU)	J2-14	NC	—
J2-15	NC	—	J2-16	/PWM enable (active low)	I (10k PU)
J2-17	NC	—	J2-18	NC	—
J2-19	NC	—	J2-20	NC	—

1.3 Block Diagram

Figure 2 shows the system block diagram of the three-phase GaN inverter with the TIDA-00909 device indicated in the red-dotted box.

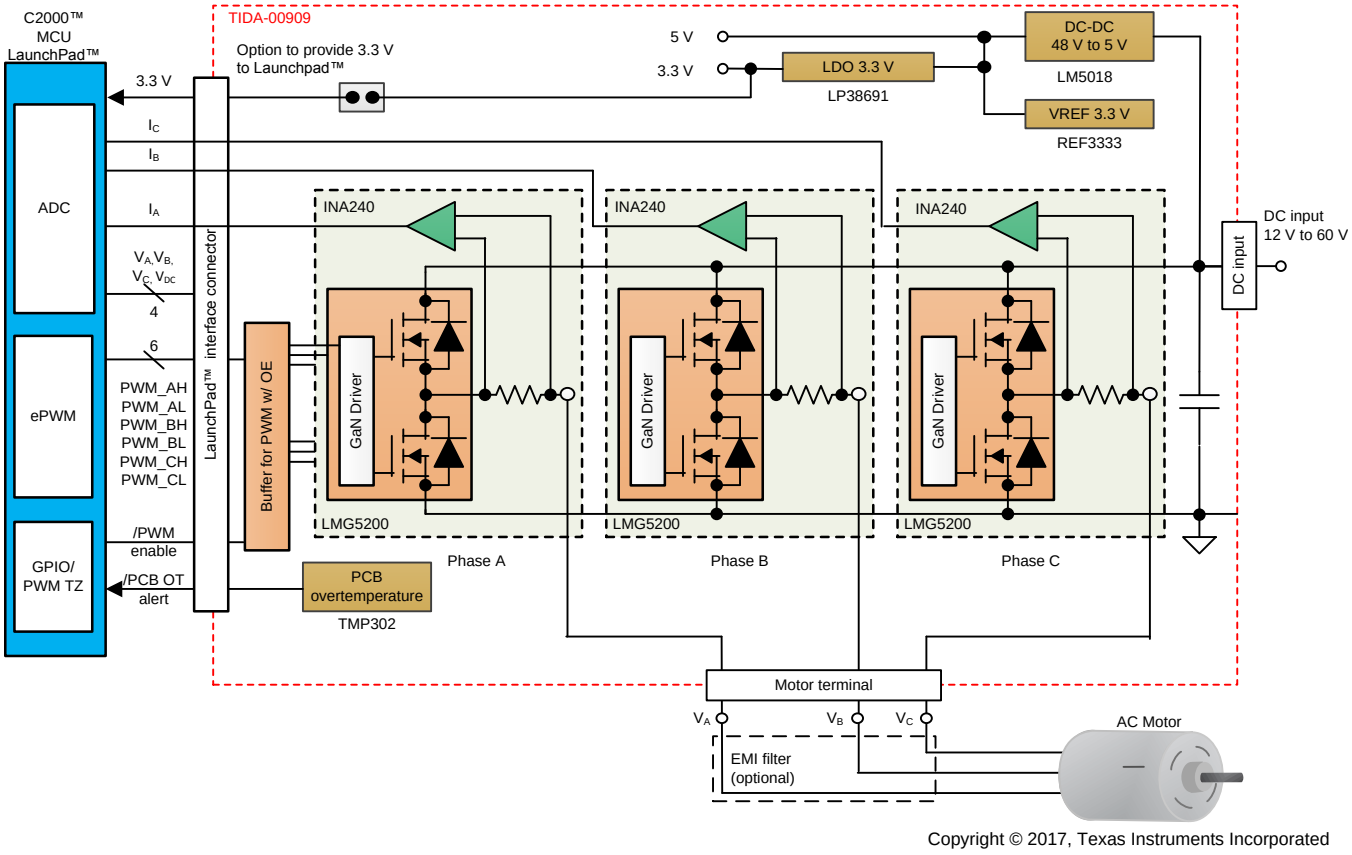


Figure 2. TIDA-00909 Block Diagram

The TIDA-00909 three-phase inverter accepts input DC voltages from 12-V to 60-V DC, the nominal DC input voltage is 48 V. LM5018, a wide-input voltage range DC-DC converter, generates the 5-V rail to supply the LMG5200 gate driver and the 3.3-V band-gap reference and a 3.3-V low-dropout regulator (LDO) supplies the current sense amplifier, input buffer, and temperature switch.

Each of the three inverter half-bridges employ an integrated 80-V, 10-A GaN half-bridge module (LMG5200), a 5-mΩ phase current shunt, and a differential current sense amplifier (INA240) with a gain of 20 V/V and a midpoint voltage of 1.65 V, which is set by the 3.3-V reference (VREF3333). A temperature switch monitors the printed-circuit board (PCB) temperature close to the GaN power module.

The TIDA-00909 interface connector-to-host processor provides the PWM high- and low-side input signals, the phase current sense amplifier output voltage, and the scaled, low-pass filtered phase voltage for each of the three phases. The PWM signals are buffered. A PWM enable signal (active low) allows the host processor to enable and disable all three complementary PWM signals simultaneously through the onboard buffer. The interface connector also provides the scaled DC-link voltage as well as a PCB overtemperature alert (active low).

The three-phase motor is connected to the three-phase motor terminal. An optional electromagnetic interference (EMI) filter can be added for slew rate reduction, as explained in Section 2.1.3.

The C2000 MCU LaunchPad with the TMS320F28069M device is connected to the TIDA-00909 device and implements a sensorless, speed-variable, field-oriented control of a synchronous motor using the InstaSPIN-FOC™ software. A binary example firmware for the TMS320F28069M device on the InstaSPIN-MOTION™ LaunchPad has been provided to evaluate the TIDA-00909 design with a 48-V low-voltage servo motor (http://www.ti.com/tool/lvservomtr).

1.4 Highlighted Products

The TIDA-000909 reference design features the following key devices from Texas Instruments.

1.4.1 LMG5200

The LMG5200 80-V GaN half-bridge power stage provides an integrated power stage solution using enhancement-mode Gallium Nitride (GaN) FETs. The device consists of two GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration, as Figure 3 shows.

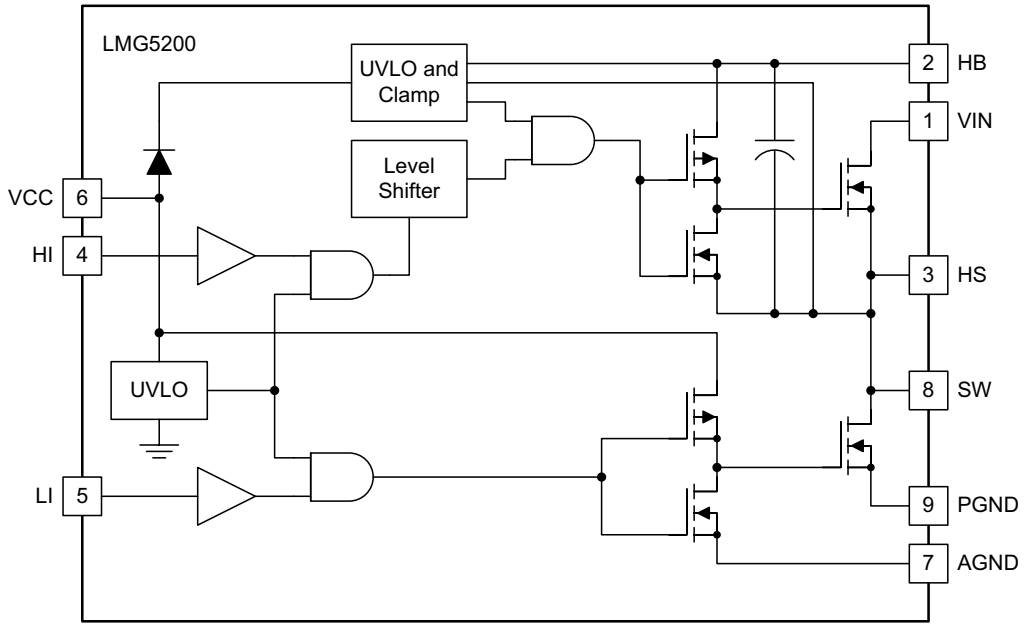


Figure 3. LMG5200 Functional Block Diagram

GaN FETs provide significant advantages for power conversion as they have near-zero reverse recovery and very-small input capacitance CISS. The LMG5200 is mounted on a completely bond-wire-free package platform with minimized package parasitic elements. The LMG5200 device is available in a 6×8×2-mm lead free package and can be easily mounted on PCBs. The LMG5200 reduces the board requirements for maintaining clearance and creepage requirements for medium-voltage GaN applications while minimizing the loop inductances to ensure fast switching. The LMG5200 is specified over the extended operating temperature range (–40°C to +125°C).

Table 5 lists the features and benefits of the LMG5200 device.

Table 5. LMG5200 Features and Benefits

FEATURES	BENEFITS
Integrated high-side and low-side GaN driver and 80-V GaN FETs; 14-mΩ devices for 10-A DC operation	Enables up to 60-V DC, three-phase inverter with 7-A_{RMS} phase current at 100-kHz high-switching frequency for low inductance and high-speed drives
Integrated 80-V, 14 -mΩ, GaN FETs and GaN driver with completely bond-wire-free package	Minimized package parasitic elements enable ultra-fast switching for reduced switching losses to reduce or eliminate heatsink
GaN FETs have zero reverse recovery (third quadrant operation) and very-small input capacitance CISS	Reduce or eliminates ringing in hard switching, which reduces EMI; very low overshoot and undershoot allows higher nominal DC-link voltage than Si-FET for same max rated voltage
Excellent propagation delay matching (2-ns FETs)	Enables ultra-low deadband per half-bridge for major reduction of switching losses in three-phase inverter applications
Independent high-side and low-side TTL inputs	Direct PWM interface to 3.3-V MCU
Single 5-V gate driver supply with bootstrap voltage clamping and undervoltage lockout	Ease power management; UVLO ensures simultaneous shutdown of high-side and low-side GaN FET in case of gate driver undervoltage
LMG5200 optimized pinout	Simple PCB layout with minimum inductance for reduced switching losses

1.4.2 INA240

The INA240 is a voltage-output, current-sense amplifier with enhanced PWM rejection which can sense drops across shunt resistors over a wide common-mode voltage range from –4 V to 80 V, independent of the supply voltage. (see Figure 4) Enhanced PWM rejection provides high levels of suppression for large common-mode transients (ΔV/Δt) in systems that use pulse-width modulation (PWM) signals such as three-phase inverters in motor drives. This feature allows for accurate current measurements without large transients and associated recovery ripple on the output voltage.

This device operates from a single 2.7-V to 5.5-V power supply, drawing a maximum of 2.4 mA of supply current. Four fixed gains are available: 20 V/V, 50 V/V, 100 V/V, and 200 V/V. The low offset of the zero-drift architecture enables current sensing with maximum drops across the shunt as low as 10-mV full-scale. All versions are specified over the extended operating temperature range (–40°C to +125°C), and are offered in an 8-pin TSSOP package.

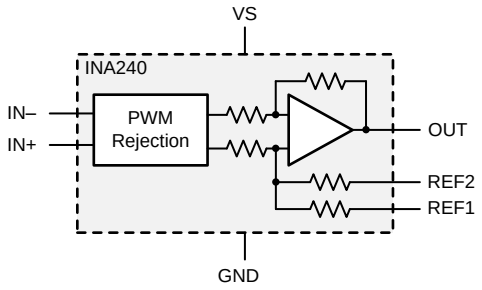


Figure 4. INA240 Functional Block Diagram

Table 6 lists the features and benefits of the INA240 amplifier.

Table 6. INA240 Features and Benefits

FEATURES	BENEFITS
Fast-transient, common-mode, voltage input filtering (enhanced PWM rejection) and high AC CMRR: 93 dB at 50 kHz and 132-dB DC CMRR	Enables non-isolated, shunt-based, precision-phase-current measurement with three-phase inverters with a high-switching frequency of 40 kHz and above
Wide common-mode input voltage range: –4 V to 80 V	Provides sufficient headroom for transient overvoltage and undervoltage in three-phase inverters with 48-V to 60-V DC link voltage
Low offset voltage (V_{OS} = ±25 µV) and low gain error (0.2%)	Low offset and gain error enables accurate current sensing without calibration
Low offset voltage drift (0.25 µV/°C) and gain error drift (2.5 ppm/°C)	Ultra-low offset and gain error drift allows highly-accurate current sensing over entire temperature range without temperature-dependent calibration
400-kHz signal bandwidth	High signal bandwidth supports low-latency phase current measurement of high-speed motors as well as low latency detection of high-current transients such as during a short-circuit event
Integrated output, midpoint voltage, reference voltage divider	Allows using an external ADC reference to set the INA240 midpoint voltage to half of the ADC reference voltage, which eliminates any offset generated by the ADC reference voltage drift
Integrated precision-gain-setting resistors	Very-low offset drift, easier PCB layout, and reduced BOM

1.4.3 LM5018/LM5017

The LM5018 is a 100-V, 300-mA synchronous step-down regulator with integrated high-side and low-side MOSFETs. The LM5018 device is available in WSON-8 and HSOP PowerPAD™-8 plastic integrated circuit packages. The LM5017 is a drop-in compatible version for a 600-mA supply current.

Table 7 lists the features and benefits of the LM5018 regulator.

Table 7. LM5018 Features and Benefits

FEATURES	BENEFITS
Wide 7.5-V to 100-V input range	Allows use for point-of-load for three-phase inverters with wide-input DC-link voltage from 12 V to 80 V
Integrated 100-V high-side and low-side switches	Reduced BOM cost, easier layout
Constant on-time (COT) control scheme employed in the LM5018	No loop compensation required, provides excellent transient response, and enables very-high step-down ratios, such as 48 V to 5 V used in the TIDA-00909 design
Integrated peak-current limit circuit and thermal shutdown	Protects against overload conditions

For more information on each of these devices, see their respective product folders at www.ti.com or click on the links for the product folders on the first page of this reference design under the *Resources* section.

2 System Design Theory

2.1 Three-Phase GaN Inverter Power Stage

The three-phase GaN inverter is realized with three LMG5200 GaN half-bridge power modules. A bulk capacitor of 220 uF is used to buffer the 48-V DC input. The PCB employs two separated ground planes: the power ground (PGND) and the logic or analog ground (GND). Both ground planes are connected in a star configuration through a net tie and two optional 0-Ω resistors to minimize the crosstalk of high-switching frequency currents in the power ground plane into the logic plane.

2.1.1 LMG5200 GaN Half-Bridge Power Stage

The LMG5200 80-V GaN half-bridge power stage provides an integrated and easy-to-use power stage solution using enhancement-mode Gallium Nitride (GaN) FETs. The device consists of two GaN FETs driven by one high-frequency GaN FET driver in a half-bridge configuration. GaN FETs provide significant advantages for power conversion as they have near-zero reverse recovery and very small input capacitance CISS. The LMG5200 is mounted on a completely bond-wire-free package platform with minimized package parasitic elements. The PCB space is further reduced due to high integration and the fact that only a few additional passive components are required. Figure 5 shows the schematic of one half-bridge.

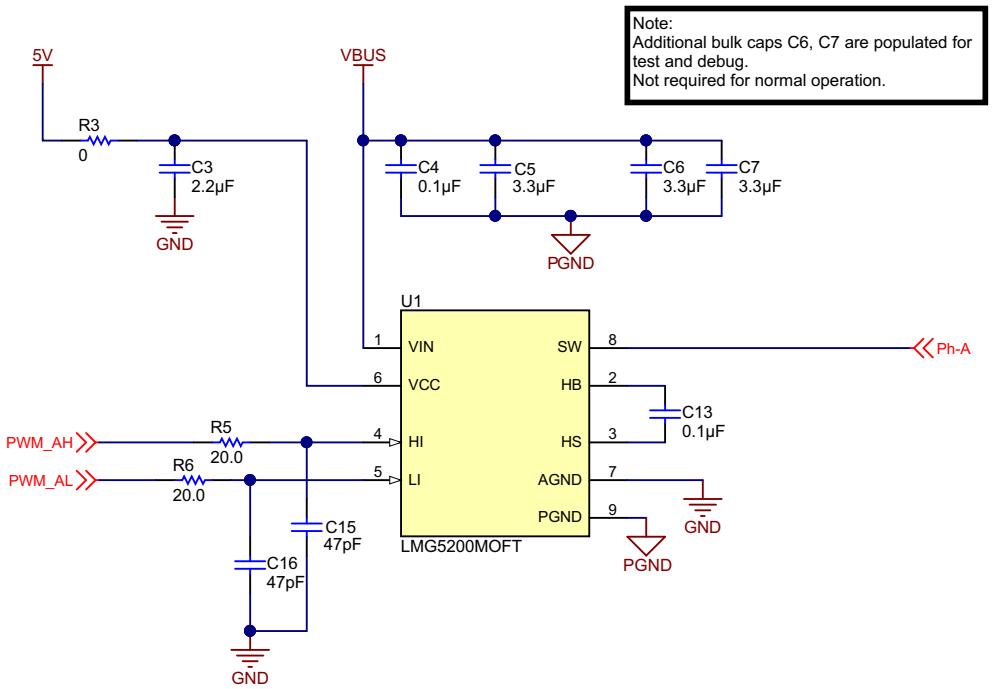


Figure 5. Schematic of Half-Bride Power Stage for Phase A

Due to the high integration of the LMG5200 power stage, very few passive components are required. The 48-V DC-link voltage is connected between the LMG5200 VIN pin and referenced to the power ground (PGND) pin. Local ceramic bypass capacitors C4 (100 nF) and C5, C6, and C7 (each 3.3 uF) are placed in parallel close between the VIN and PGND pins to minimize loop inductance. C6 and C7 are optional and not required for normal operation, as the *Test Results* outline in Section 4.2.3. The *Layout Recommendations* in Section 5.3.1 outline the optimized layout for low EMI.

The LMG5200 integrated gate driver is supplied with 5 V. A 2.2-uF ceramic bypass capacitor C3 is placed close to the VCC pin and AGND pin. The series resistor R3 has been placed for testing and debugging such as current consumption measurement and was set to 0 Ω for the final board. Sequencing is not required for the 5 V at V_{CC} and the 48 V at V_{IN}, neither during the power up or power down of the input DC voltage.

The complementary PWM signals for the high-side and low-side switch from the MCU are low-pass filtered with R5/C14 and R6/C16 and reject high-frequency impulse noise to avoid false switching. The 100-n ceramic bootstrap capacitor C13 is placed close to the HB (high-side, gate-driver bootstrap rail) and HS (high-side, GaN-FET source connection) pins. The SW (switch node) pin is connected to the motor phase-A terminal through a series inline shunt for phase current sensing, which Section 2.2 outlines.

2.1.2 Power-Stage PCB Overtemperature Switch

To sense an overtemperature event with the PCB power stage, the TMP302 family of temperature switch devices has been selected as it offers trip-point accuracy of ±0.2°C from +40°C to +125° and pin-selectable trip points from 55°C to 125°C in 5°C steps with an optional 5°C or 10°C hysteresis. The TMP302B micro-package temperature switch has been chosen and placed closed to the LMG5200 half-bridge module (see the schematic in Figure 6). The TMP302B switch is configured to trip above 85°C by pulling up the TMP302B TRIPSET0 and TRIPSET1 pins to 3.3 V. The hysteresis is set to 5°C by pulling the HYSTSET pin down to GND. The /OT pin is an open-drain and has a 10-k pullup to 3.3 V. An overtemperature event is indicated through the /OT pin set low. The TMP302B switch is connected to the 3.3-V rail and logic GND, but placed very close to the power ground plane of the phase-A half-bridge.

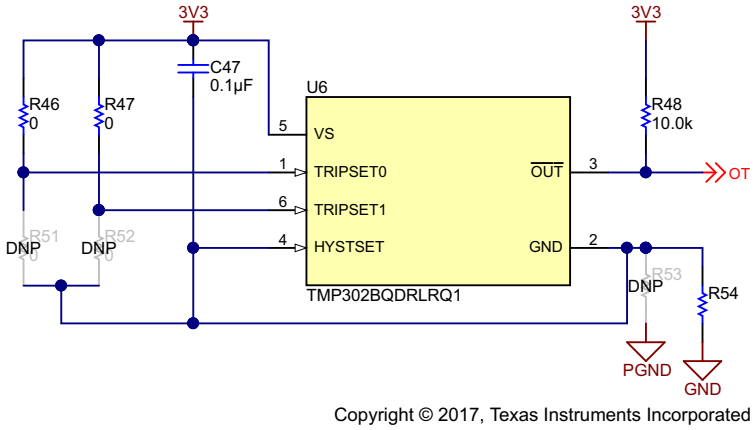


Figure 6. Schematic of 85ºC PCB Temperature Switch

2.1.3 Optional Output LCR EMI Filter

Phase voltage transients higher than specified for the corresponding motor may deteriorate the winding insulation. Typical motor isolation ratings are below 10 kV/µs. Due to the very-high slew rate of the TIDA-00909 GaN inverter of around 50 V/ns, an output LCR EMI filter may be added in series to each phase terminal to reduce the slew rate at the motor phase terminals, respectively. Figure 7 shows the topology of the output LCR filter applicable to each phase.

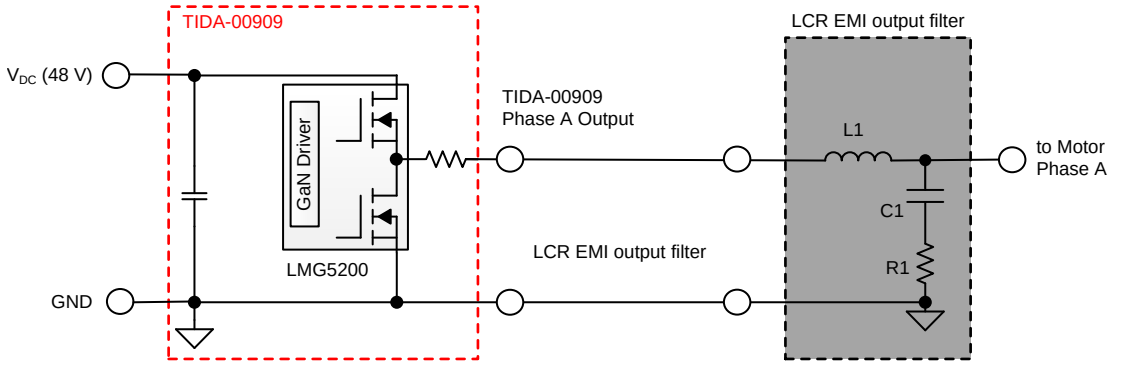


Figure 7. Output LCR Filter Topology

The EMI LCR filter components have been calculated based on the nominal specification of the inverter:

- DC-link voltage (V DC): 48 V
- Peak phase current (I_{PEAK}): 10 A
- Minimum PWM on-time and off-time (t_{ON-MIN}): 100 ns
- GaN inverter slew rate: ≈50 V/ns
- Slew rate at motor terminals (dV/dt): ≈5 V/ns

In the first step the capacitor C1, L1, and R1 were roughly approximated per Equation 1 to Equation 3:

$$C1 \geq \frac{I_{PEAK}}{dV / dt} \approx 2\ nF \tag{1}$$

$$L1 \leq \left(\frac{t_{ON-MIN}}{2 \times \pi} \right)^2 \times \frac{1}{C1} \approx 138\ nH \tag{2}$$

$$R1 \geq \sqrt{\frac{L1}{C1}} \approx 8.3\ \Omega \tag{3}$$

In the second step the components were optimized with TINA-TI™ Spice simulation software while also considering the availability of suitable inductors in the 100-nH range. Figure 8 shows a TINA-TI Spice simulation with the selected passive components:
L1 = 120 nH, R1= 12.5 Ω, and C1 = 3.3 pF.

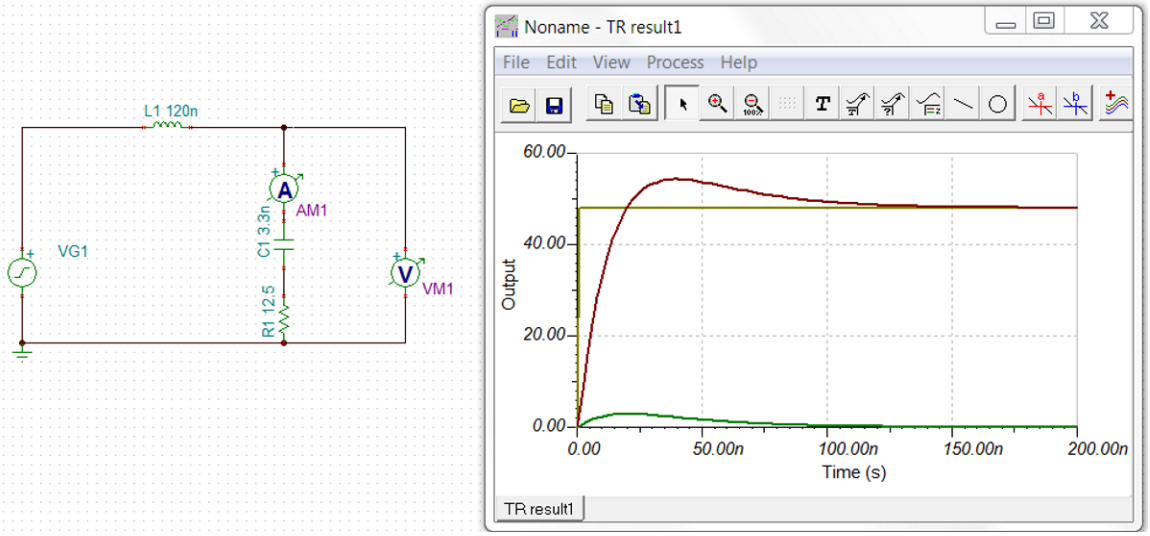


Figure 8. TINA-TI™ Spice Simulation of EMI Output Filter

The peak current through the damping resistors R1 is around 4 A and the power dissipation at 100-kHz PWM is around 150 mW. Figure 9 shows the schematic and Table 8 shows the bill of materials (BOM).

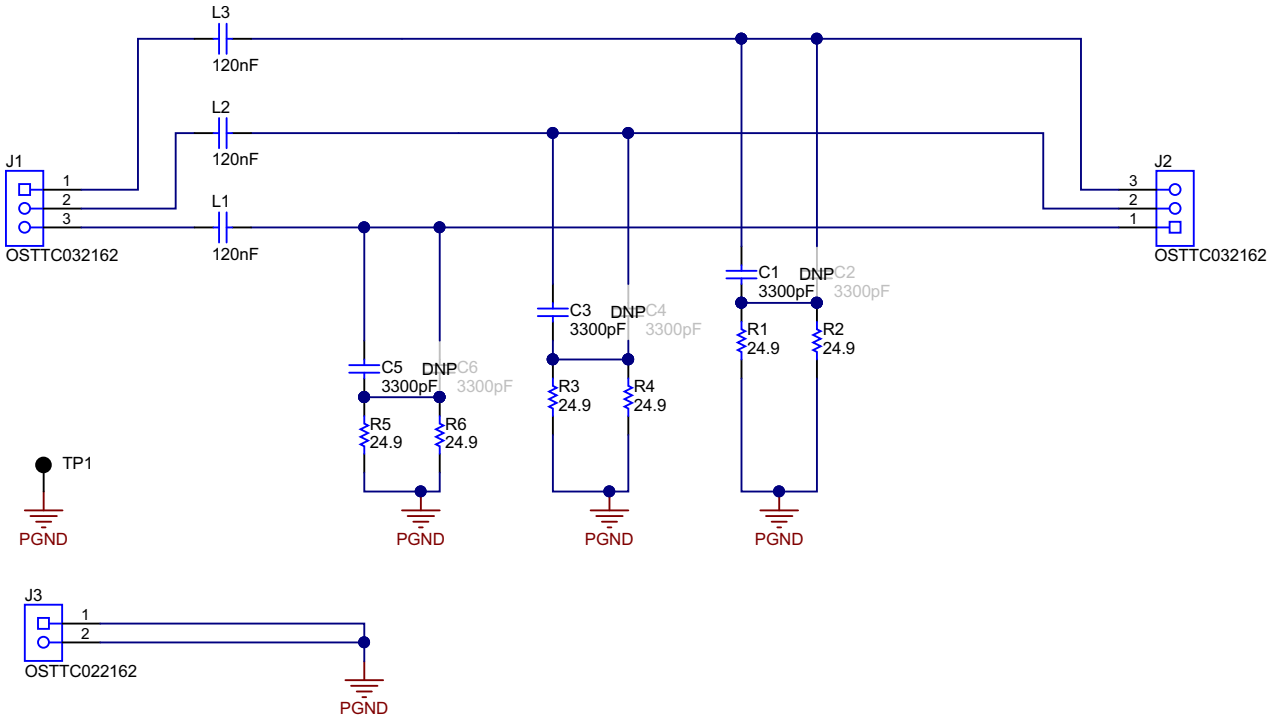


Figure 9. Schematic of Three-Phase LCR EMI Output Filter

Table 8. BOM of Three-Phase LCR EMI Output Filter

DESIGNATOR	VALUE	PART NUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
L1, L2, L3	56 Ω at 100 MHz	74279223560	Wurth Elektronik	WE-MPSB EMI Multilayer Power Suppression Bead	1612 (4.06 mm × 3.05 mm)
R1, R2, R3, R4, R5, R6	24.9 Ω	—	±5%	—	0805
C1, C3, C5	3300 pF, 100 V	—	As low as possible	CAP, CERM, ± 5%, X7R	0805

2.2 In-Line Shunt Precision-Phase Current Sensing With INA240

The phase current in each phase is measured inline through a 5-mΩ shunt, for example R55 for phase A, as Figure 10 shows. R55 is directly connected to the switch node output (SW pin) of the LMG5200 device. The shunt is connected through a Kelvin connection and optional, differential RC low-pass filter (R57, R56, and C52) to the differential inputs IN+ and IN– of the INA240A1 device. In this design, the low-pass filter is not required and the two series resistors have been selected as 0 Ω and the capacitor C52 has not been populated on all three phases. The INA240A1 device has a fixed gain of 20 V/V. To convert the bipolar input voltage across the shunt into a unipolar output voltage that is suitable for an ADC with a 3.3-V input voltage range, the mid voltage of the INA240A1 (U8) is set to 1.65 V. To achieve this conversion, a precision, low-drift 3.3-V reference REF3333 is connected through an optional RC low-pass filter (R60 and C53) to the REF1 pin. The REF2 pin is connected to GND. In the default setting of the TIDA-00909 design, the low-pass filter is not used and R60 is set to 0 Ω, which is the same on the other two phases. An internal, precision divide-by-2 function in the INA240 device creates a precision, ultra-low drift, 1.65-V bias voltage at the INA240 OUT pin. The transfer function can be calculated as per Equation 4:

$$IA[V] = \left(-IL_A[A] \times 5\,m\Omega\right) \times 20\left[\frac{V}{V}\right] + 1.65\ V \quad (4)$$

Note that the phase current direction is actually inverted for the purposes of having an optimized layout. The maximum phase current range is from –16.5 A to 16.5 A. The corresponding output voltage ranges from 0 V to 3.3 V with 1.65 V representing a 0-A phase current.

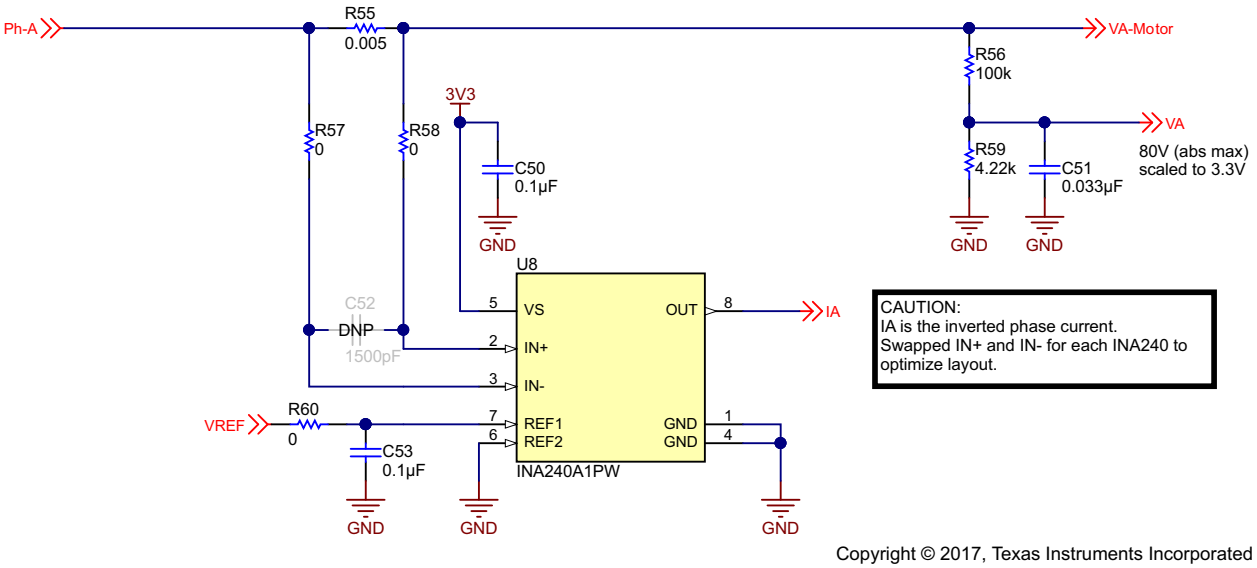


Figure 10. Schematic of Inline Phase-Current Sense Solution for Phase A

For more details on designing with the INA240 device, refer to the TIDA-00913 TI Design [6].

2.3 Phase Voltage and DC Input Voltage Sensing

The phase voltage for each phase and the DC link voltage, which is equal to the input voltage, are sensed through a resistor divider. Figure 11 shows an example of this for the DC-link voltage (R56, R59) with a low-pass filter (C51) to attenuate the PWM carrier frequency. The phase voltage is scaled to 3.3 V, assuming an absolute maximum voltage of 80 V according to Equation 5:

$$VA[V] = V\_A[V] \times \frac{1}{24.7} \tag{5}$$

The cut-off frequency (f – 3 dB) of the low-pass filter has been set to 1 kHz, which provides around 32 dB of attenuation to reject a 40-kHz PWM carrier frequency and 40 dB for a 100-kHz PWM carrier frequency. The DC-link voltage is sensed through the same resistor divider (see Figure 11) and low-pass filter to ensure all voltages have the same transient response and delay.

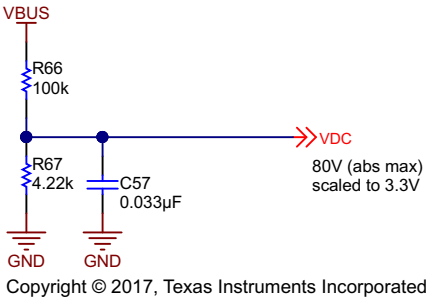


Figure 11. Schematic of DC-Link Voltage Sense

2.4 Interface-to-Host MCU

The interface-to-host processor, such as the C2000™ MCU, is compliant to a 3.3-V I/O and provides all the required signals like the complementary PWM signals for phase A, B, and C; a PWM trip and disable signal; as well as accurate phase current, phase voltage, and DC-link voltage feedback to control the three-phase GaN inverter. Additional feedback signals, like the overtemperature trip (/OT), further help to protect the three-phase GaN power stage.

To allow quick and easy evaluation with a C2000 MCU, the TIDA-00909 host-processor interface headers are TI BoosterPack compatible. The TIDA-00909 fits both upper and lower headers of an 80-pin C2000 MCU LaunchPad, like the LAUNCHXL-F28069M. Additionally, the TIDA-00909 host interface offers the option to provide the 3.3-V rail to power the C2000 LaunchPad, too. This option ensures proper power-up sequencing of the entire system. The details of the pin assignment are outlined in Section 1.2 in Table 3 and Table 4, respectively.

Figure 12 shows the schematic of the host port interface.

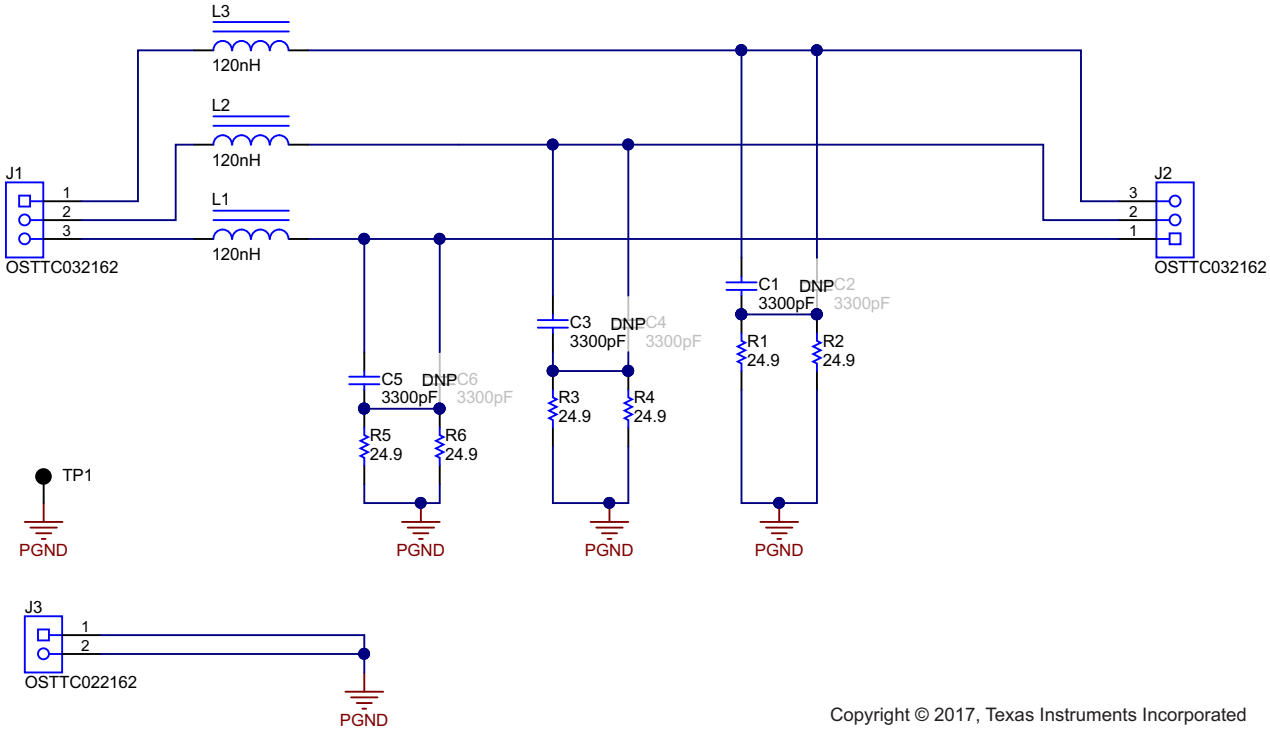


Figure 12. Schematic of Host Interface Connectors J1 and J2

All eight analog feedback signals (I^A, I_B, I_C, V_A, V_B, V_C, V_{DC}, and V_{REF}) include an RF filter with a high enough capacitor of 2200 pF to drive the switched-capacitor ADC input embedded in the C2000 MCU. The capacitors are a magnitude of 1000 larger than the integrated switched capacitor in the ADC of a C2000 Piccolo MCU. This magnitude properly ensures that the input signals settle to 0.1% or better, even during short sampling periods of less than 100 ns without requiring an additional buffer amplifier. The phase voltage and DC-link voltage signals have additional Schottky diodes clamped to 3.3 V to ensure the ADC input voltage remains below 3.6 V, even if a voltage higher than the 80-V input has been accidently applied to the TIDA-00909.

The complementary PWM signals are buffered through the SN74AVC8T245 8-bit dual-supply bus transceiver. During power-up, the output of the bus transceiver remains high impedance due to the 10-k pullup (R30) at the /OE pin. All PWM input and output pins on either side of the SN74AVC8T245 transceiver have pulldown resistors. These pulldown resistors ensure that the PWM signals remain low and the LMG5200 remains off if no host processor is connected or the PWM pins of the host processor are high impedance during power up or power down.

2.5 Power Management

The onboard power management consists of an EMI input filter, a wide-input voltage DC-DC buck converter to generate the 5-V rail, and an LDO for the 3.3-V rail.

2.5.1 EMI Input Filter

An input filter is used to reduce the input voltage ripple accordingly. The design follows the *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* application report [10]. In the case of the TIDA-00909 design, this input filter consists of a PI-filter (π) with the cutoff frequency around 1/10th of the switching frequency of the DC-DC converters to have 40 dB of attenuation at the DC-DC converter switching frequency of around 150 kHz. The inductor L2 is set to 33 µH, which yields a capacitor value of 3.3 µF for C42 (see Equation 6).

$$fc = \frac{1}{2 \times \pi \times \sqrt{L2 \times C42}} \quad (6)$$

2.5.2 48-V to 5-V DC-DC Converter

The DC-DC buck converter has been designed for a nominal input voltage range from 12 V to 60 V with an input voltage capability of at least 80 V. The output voltage is set to 5 V. The DC-DC buck-converter feedback circuit has been designed for minimum output voltage ripple and at least 400 mA of output current. The power supply has been entirely designed using WEBENCH® Power Designer [8], using the following parameter specifications in Table 9:

Table 9. DC-DC Buck Converter Parameter

PARAMETER	TYPICAL VALUE	MIN AND MAX VALUES
DC-link voltage	48 V	10 V or 80 V
Output voltage	5 V	±5%
Output voltage ripple	< 50m Vpp	As low as possible
Output current	50 mA	≥ 300 mA
Temperature range	–40.85°C (125°C)	—

Using these settings, the LM5018 is the device chosen to fit the design specification. To meet the minimum ripple, the WEBENCH output ripple option for “Low O/P Ripple Solution” has been selected for the design. Figure 13 shows the proposed WEBENCH recommendation using these settings:

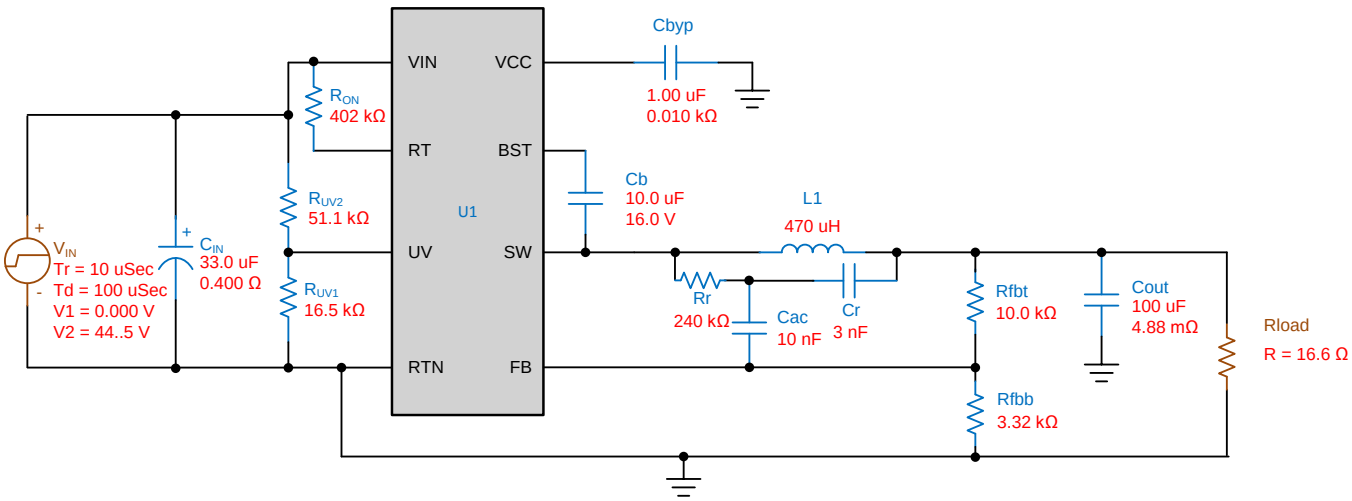


Figure 13. WEBENCH® Schematics Proposal for 48-V to 5-V Power Supply With Minimum Output Voltage Ripple

Minor changes to the WEBENCH proposals have been made in the final schematics of the TIDA-00909 design. Figure 14 shows the final passive components. Some examples of these minor changes are: An inductor L1 with higher saturation current was chosen to allow higher output current out to 600 mA by replacing the LM5018 device with the LM5017 if required. The feedback filter R40, C38, and C39 help minimize the ripple on the 5-V output rail. The undervoltage-lockout (UVLO) was set to 7.35 V by setting R43 to 100 k and R45 to 20 k and the hysteresis was set to 2 V. For details on calculating all passive components, refer to the LM5018 datasheet.

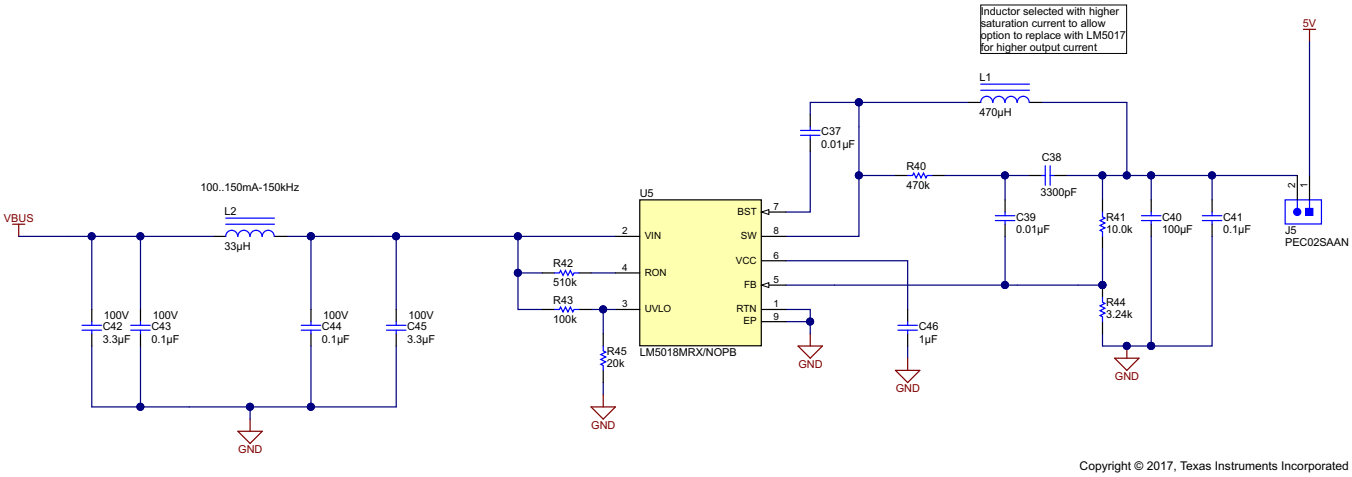


Figure 14. 48-V to 5-V DC-DC Buck Converter With Input EMI Filter

2.5.3 3.3-V Rail

For the 3.3-V rail, an LDO with at least 300-mA output current capability and high-input ripple rejection at 100 kHz was chosen (see Figure 15). The LP38691 device meets these requirements. The output bulk capacitor of 100 uF was chosen for high ripple rejection at 100 kHz, which is close to the switching frequency of the 5-V input. With the 100-µF capacitor, the ripple rejection of the LP38691 device was increased to 50 dB at 100 kHz. The jumper J6, when populated, provides the 3.3-V rail of the TIDA-00909 to also power the C2000 LaunchPad. The maximum load current is 300 mA.

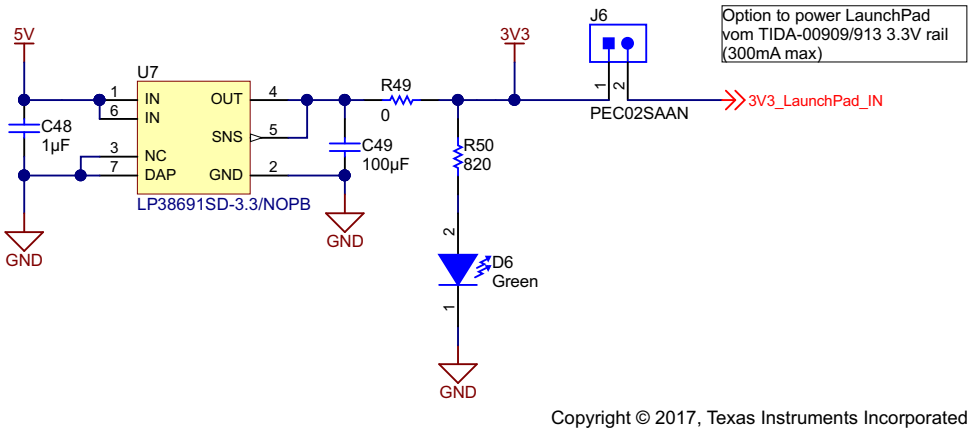


Figure 15. 5-V to 3.3-V LDO

3 Getting Started Hardware and Software

3.1 TIDA-00909 PCB Overview

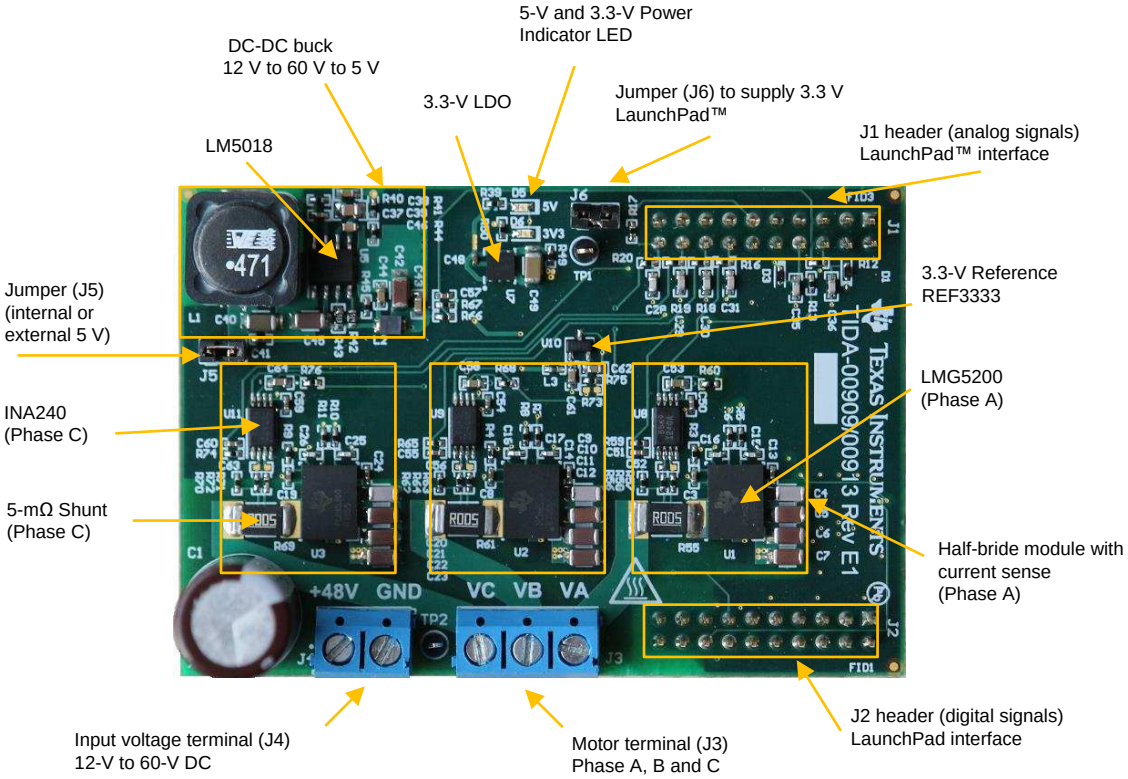


Figure 16. TIDA-00909 PCB – Top View

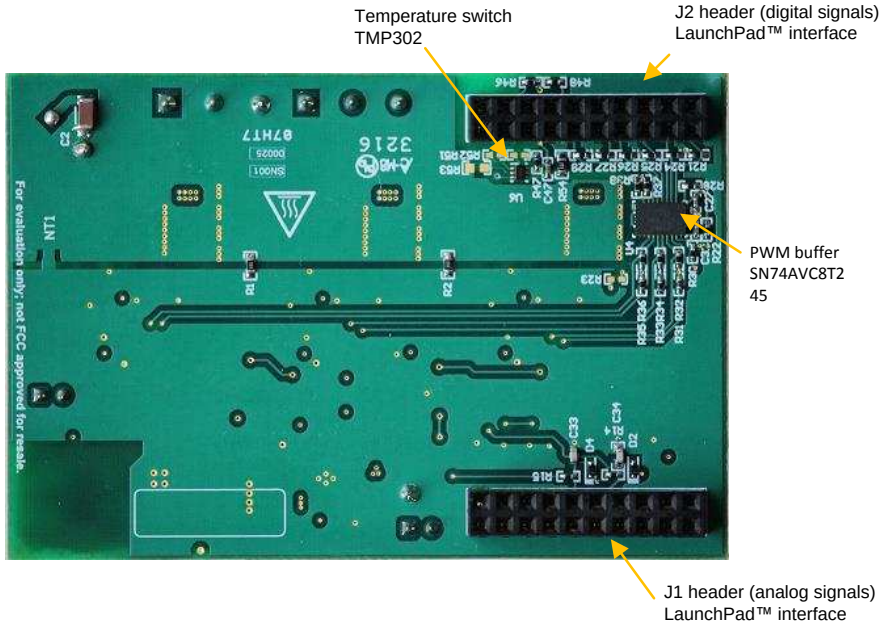


Figure 17. TIDA-00909 PCB – Bottom View

3.2 TIDA-00909 Jumper Settings

The TIDA-00909 employs two jumpers: The jumper J5 allows using an external 5-V supply, if desired. The default setting is J5 populated to use the onboard 5-V supply. The jumper J6, when populated, provides 3.3 V to the J1-1 interface pin to supply to the C2000 LaunchPad with 3.3 V. The maximum continuous current is 300 mA.

Table 10 shows the TIDA-00909 jumper settings.

Table 10. TIDA-00909 Jumper Settings

JUMPER	FUNCTION	POPULATED	NOT POPULATED
J5	5-V supply	Onboard (default)	External 5 V
J6	3.3-V supply at J1-1 interface connector to LaunchPad™	3.3 V (default)	Not connected

CAUTION

When the jumper J3 is populated, ensure that the C2000 LaunchPad is not powered through a USB. To ensure this, remove the JP1 and JP2 jumpers on the C2000 InstaSPIN-MOTION LaunchPad.

3.3 Interface to C2000™ InstaSPIN-MOTION™ LaunchPad™

The TIDA-00909 interface specification is compliant to the TI BoosterPack standard. Refer to the pin assignment in Table 3 and Table 4 in Section 1.2. The TIDA-00909 board can either be connected to the C2000 InstaSPIN-MOTION LaunchPad headers J1 through J3 and J2 through J4 or to the extended headers J5 through J7 and J6 through J8.

CAUTION

- When connecting the TIDA-00909 to the LaunchPad, pay attention that the bottom-side solder joints do not connect to the additional jumpers and headers of the LaunchPad.
- The phase current I_A, I_B, and I_C equivalent output voltage at connectors J1-14, J1-16, and J1-18 is inverted versus the DRV8301 BoosterPack.
- When J6 is populated so that TIDA-00909 provides the 3.3 V to supply the LaunchPad, ensure that the LaunchPad is not powered from a USB. To ensure this, remove the JP1 and JP2 jumpers on the InstaSPIN-MOTION LaunchPad, as Figure 18 shows.

The following Figure 18 shows the TIDA-00909 connected to the InstaSPIN-MOTION LaunchPad headers J5 through J7 and J6 through J8. Note that the TIDA-00909 powers the LaunchPad, therefore TIDA-00909 J6 is populated and the jumpers JP1 and JP2 on the LaunchPad are not populated.

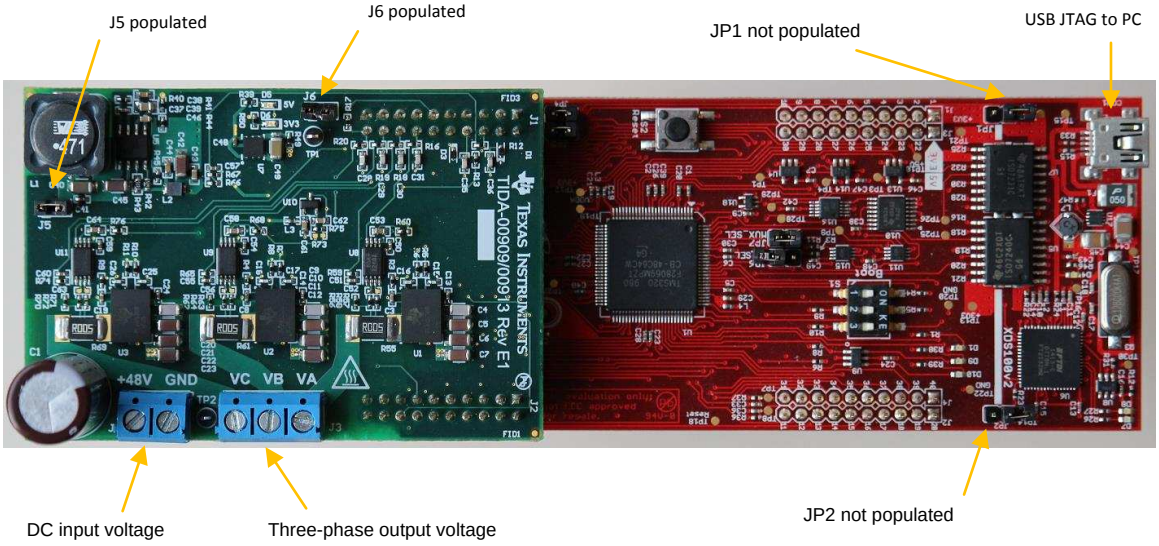


Figure 18. TIDA-00909 PCB – Bottom View

Connect the DC power supply (12 V to 60 V, 48-V nominal) to the DC input voltage connector (J4) and the three-phase motor to the three-phase output voltage connector (J3). Validate that the three-phase motor can handle the high slew rates of the phase voltages during PWM switching; otherwise, consider using a low-pass LCR filter to reduce the slew rate of the phase voltage according to the requirements of the motor.

3.4 InstaSPIN-FOC™ Example Project for Teknic Servo Motor M-2310P-LN-04K

The software example is created for the InstaSPIN-MOTION LaunchPad using headers J5/J7 and J6/J8. Ensure the TIDA-00909 board is connected to the InstaSPIN-MOTION LaunchPad as the preceding Figure 18 shows.

Be sure to install the Texas Instrument's MotorWare™ software package revision 1.01.00.16 in the default install path *C:\ti\MOTORWARE\motorware_1_01_00_16*.

Unzip the TIDA-00909 software package for the example to the *C:\ti\tida-00909* folder.

Follow the next steps in Section 3.4.1 to create an InstaSPIN-FOC project example for the TIDA-00909 hardware connected to the InstaSPIN-MOTION LaunchPad.

3.4.1 Set up TIDA-00909 Board Specific Project Folders in MotorWare™ Software

1. Navigate to folder: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\solutions\instaspin_foc\boards*.
2. Create a copy of the *boostxldrv8301_revB* folder in the same directory and rename it to *tida00909*.
3. Navigate to the folder: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\modules\hal\boards*.
4. Create a copy of the *boostxldrv8301_revB* folder in the same directory and rename it to *tida00909*.
5. Copy the five sources files as provided with the TIDA-00909 software package into the *tida00909* folder. The project folders are as follows:
   (a) Copy *user.h* and *user_j5.h* to the following directory: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\solutions\instaspin_foc\boards\tida00909\f28x\f2806xF\src*. Note that this action replaces or overwrites the original files.
   (b) Copy *hal.c* and *hal.h* to the following directory: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\modules\hal\boards\tida00909\f28x\f2806x\src*. Note that this action replaces or overwrites the original files.
   (c) Copy *proj_lab02a-tida00909.c* to the following directory: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\solutions\instaspin_foc\src*.

3.4.2 Set up TIDA-00909 Board Specific Project With Code Composer Studio™ (CCS) Software

1. Open the Code Composer Studio™ (CCS) software, choose TIDA-00909 as the new workspace, and import the *tida00909* projects from: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\solutions\instaspin_foc\boards\tida00909\f28x\f2806xF\projects\ccs5*.
2. Make the *proj_lab02a* project active.
3. In the *CCS Project* explorer for *proj_lab02a* select the *proj_lab02a.c* C:/ source file and exclude this from the build.
4. Add the file to the project and browse to the *proj_lab02a-tida00909.c* file in the following folder: *C:\TI\MOTORWARE\motorware_1_01_00_16\sw\solutions\instaspin_foc\src*. In the dialog window, add the option for adding *proj_lab02a-tida00909.c* as per Figure 19 and click the *OK* button.

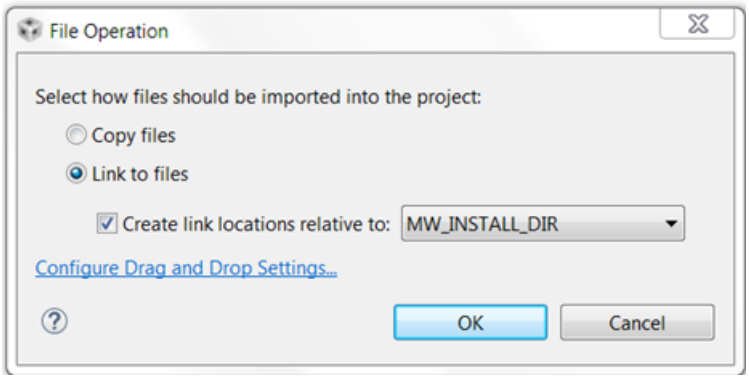


Figure 19. Dialog Window for Step 4

5. In the CCS Project explorer, open the properties of the *proj_lab02* project.
   (a) In the *File* menu, navigate to "Resources" → "Linked Resources", and in the dialog window click the tab on the right for linked resources, as Figure 20 shows:

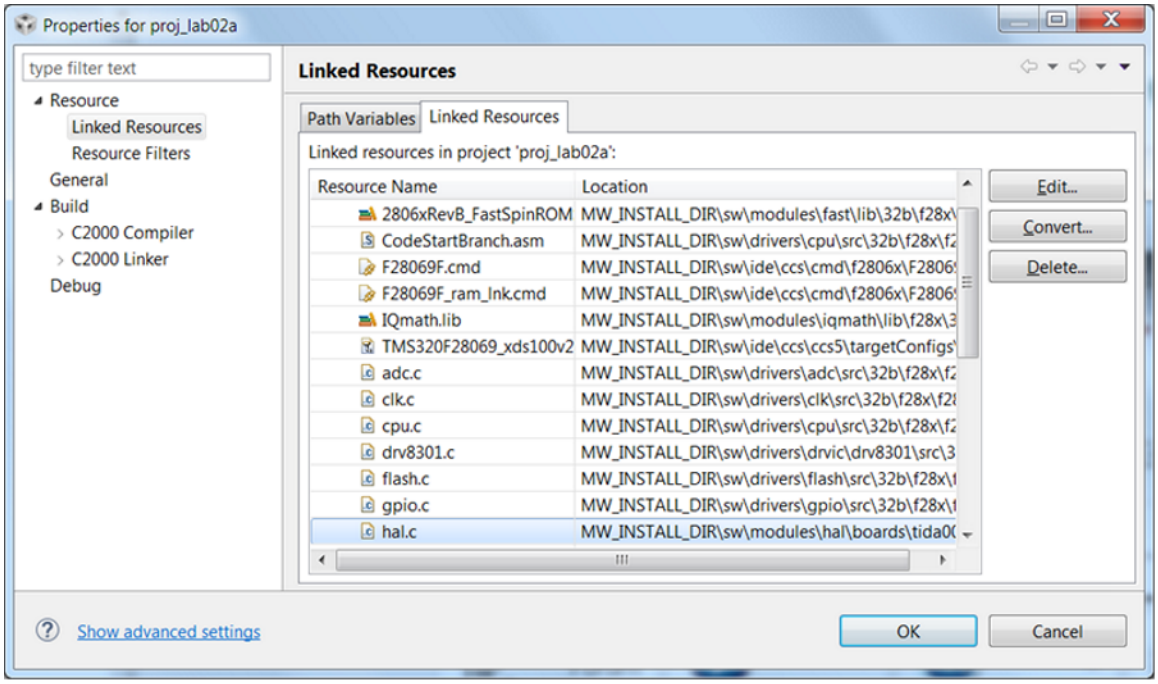


Figure 20. Dialog Window for Step 5-a

(b) Select the *hal.c* file (in the "Resource Name" column) and edit the existing link (in the "Location" column) with the new link to the tida00909 project: *MW_INSTALL_DIR\sw\modules\hal\boards\tida00909\f28x\f2806x\src\hal.c*, as Figure 21 shows:

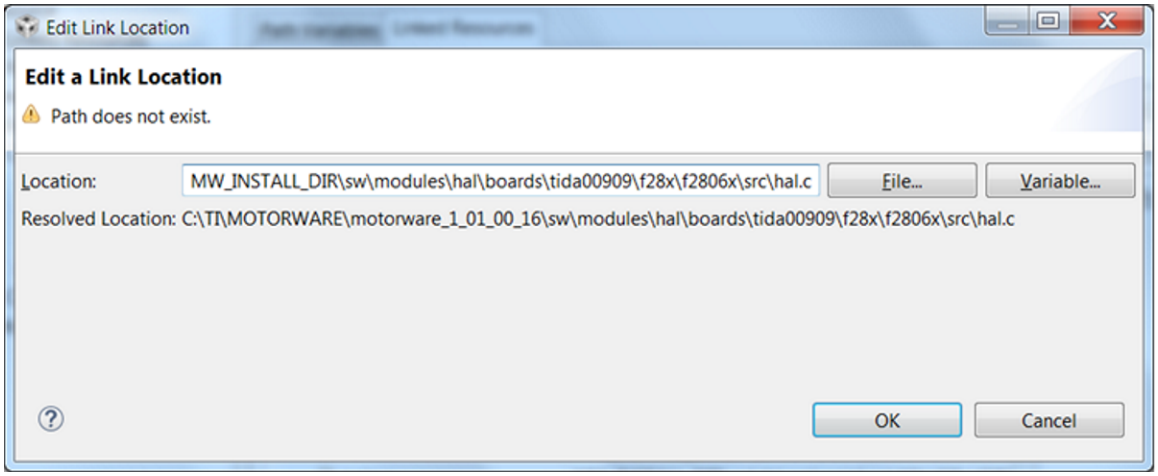


Figure 21. Dialog Window for Step 5-b

(c) Click the *OK* button to close the dialog window.

6. In the CCS Project explorer open the properties of the *proj_lab02* project.

(a) In the *File* menu, navigate to "Build" → "C2000 Compiler" → "Include Options" to view the following options in Figure 22:

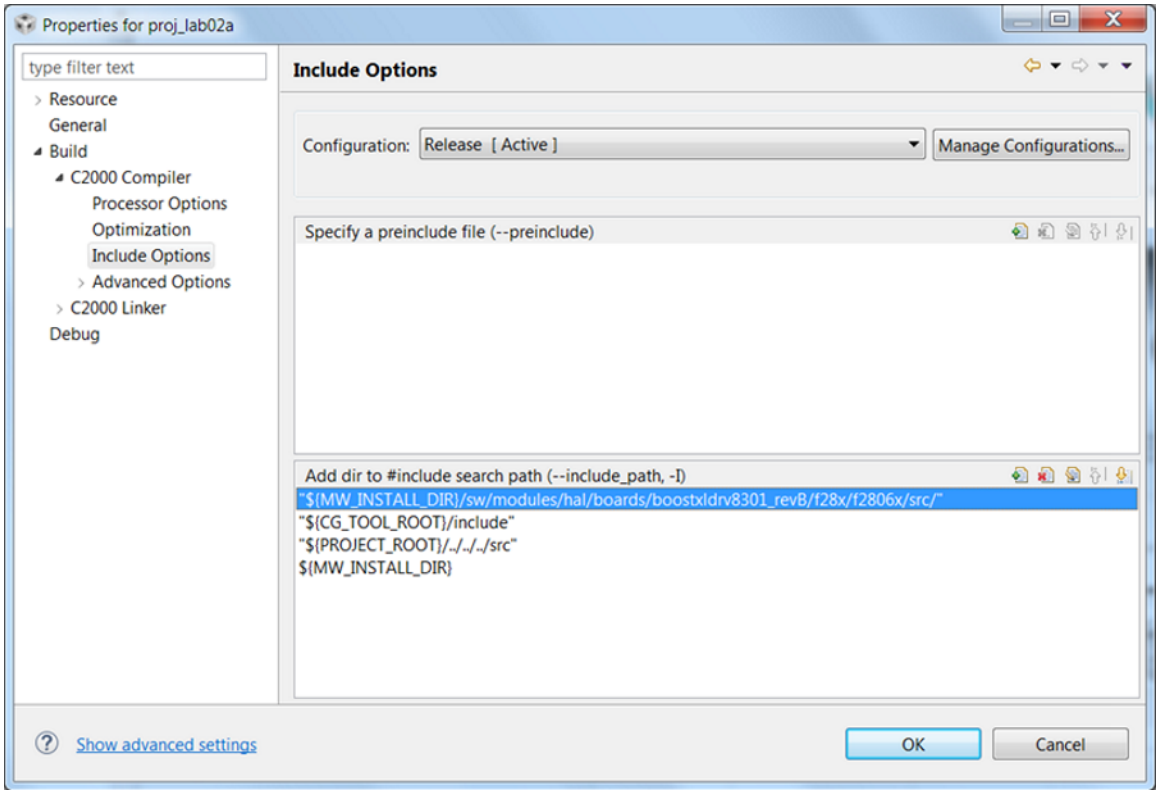


Figure 22. Dialog Window for Step 6-a

(b) Select the path highlighted *${MW_INSTALL_DIR}* and change this to *${MW_INSTALL_DIR}/sw/modules/hal/boards/tida00909/f28x/f2806x/src/* as Figure 23 shows:

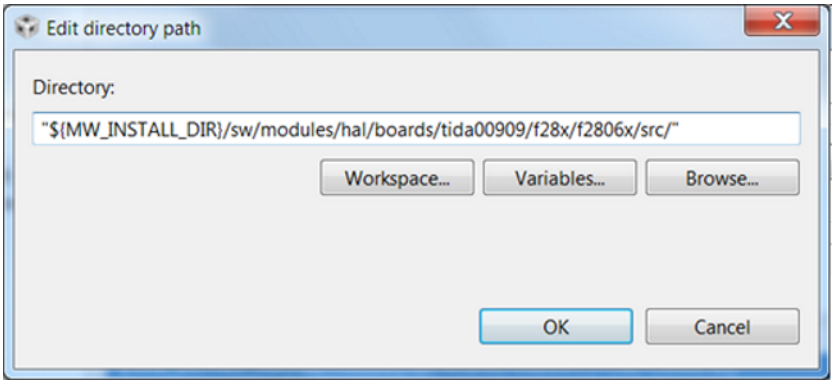


Figure 23. Dialog Window for Step 6-b

(c) Click the *OK* button to close the properties window.

3.4.3 Compile and Run TIDA-00909 Project Example

1. Compile the *proj_lab02a-tida00909* project and download to the TMS329F28069F target processor on the InstaSPIN-MOTION LaunchPad.
2. Open the InstaSPIN Projects document and Labs User's Guide from: *C:\TI\MOTORWARE\motorware_1_01_00_16\docs\labs\instaspin_labs*.
3. Navigate to the *Lab 2a* project using InstaSPIN for the first time out of ROM on page 27 in the *InstaSPIN Projects and Labs User's Guide* (located in *C:\TI\MOTORWARE\motorware_1_01_00_16\docs\labs\instaspin_labs*) and follow the instructions to identify and run the motor.

The default motor defined in the tida00909 project is the Teknic M-2310P-LN-04K. Refer to the *InstaSPIN Projects and Labs User's Guide* when using other motors.

4 Testing and Results

Table 11 lists the key test equipment. Description and pictures of the test setup for specific tests are provided in the section of the corresponding test results.

Table 11. Key Test Equipment

DESCRIPTION	PART NUMBER
High-speed oscilloscope	Tektronix TDS784C
Single-ended probes	Tektronix P6139A
High-speed oscilloscope	Tektronix MDO4104-B3
Differential probes	Tektronix TPD0500
Single-ended probes	Tektronix TPP1000
Power analyzer	Tektronix PA4000
Isolated current probe	Tektronix TCP0030
Multimeter	Agilent 34401A, Fluke 207
Thermal camera	Fluke TI40
Adjustable power supply	Knuerr-Heinzinger Polaris 125-5
Adjustable power supply	TDK-Lamda Genesys GEN 100-33
C2000™ MCU LaunchPad™	Texas Instruments LAUNCHXL-F28069M
Low-voltage servo motor (48 V, 7 A)	Teknic M-2310P-LN-04K
Low-inductance high-speed brushless multirotor motor	Quanum MT Series 2208 1800KV

For detailed test results on the in-line, shunt-based phase-current sensing, refer to the TIDA-00913 TI Design [6].

4.1 Power Management and System Power-Up and Power-Down

4.1.1 System Power up and Power Down Cycling

The focus of this test is to validate the motor-terminal output voltages (phase voltage V_A, V_B, and V_C) during power up and power down of the 48-V DC supply input. The TIDA-00909 board was tested standalone without a motor and without a host processor connected. Figure 24 shows the motor terminal phases V_A, V_B, and V_C during power up of the V DC until it reaches 48 V. Figure 25 shows the power down. All three phases V_A, V_B, and V_C track during power up and power down, so there is no differential phase-to-phase voltage, which would drive current into the motor.

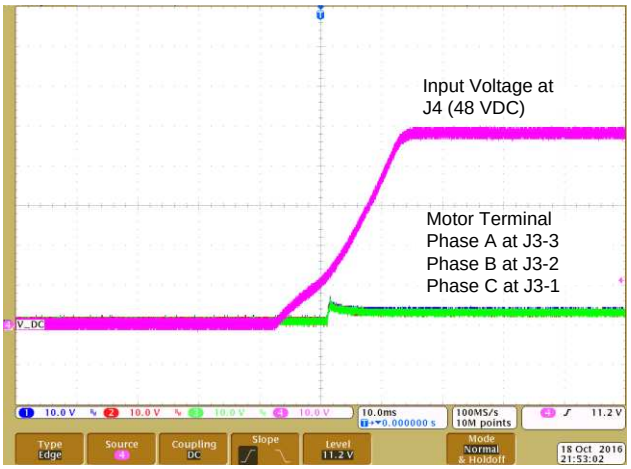


Figure 24. TIDA-00909 Phase Voltage V_A, V_B, V_C (Connector J3) During 48-V Power up

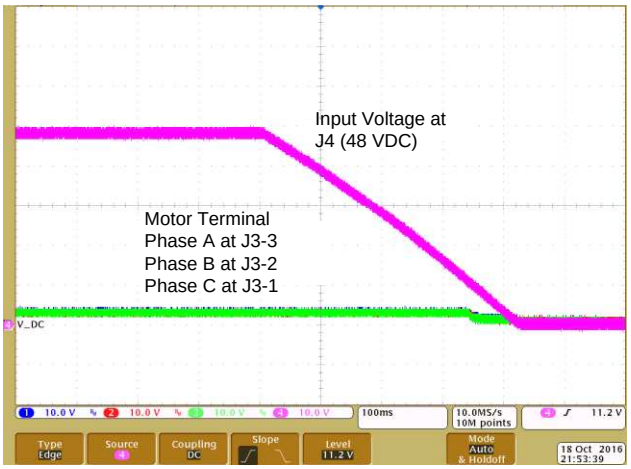


Figure 25. TIDA-00909 Phase Voltage V_A, V_B, V_C (Connector J3) During 48-V Power Down

4.1.2 Power up and Power Down of 5-V and 3.3-V Rails

The focus of this test was to validate the onboard 5-V and 3.3-V power supplies and measure the typical current consumption of the 3.3-V and 5-V rails. For these tests, the C2000 LaunchPad was not powered from the TIDA-00909. Due to the high step-down ratio 48:5 (48-V input to 5-V output), the voltage ripple at the 5-V rail was also validated. Two measurements were performed for this test (see Figure 26 and Figure 27).

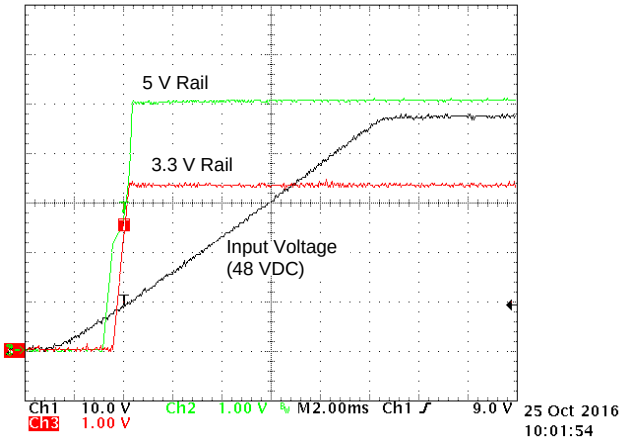


Figure 26. TIDA-00909 System Power up (48-V Input, 5-V Rail, and 3.3-V Rail)

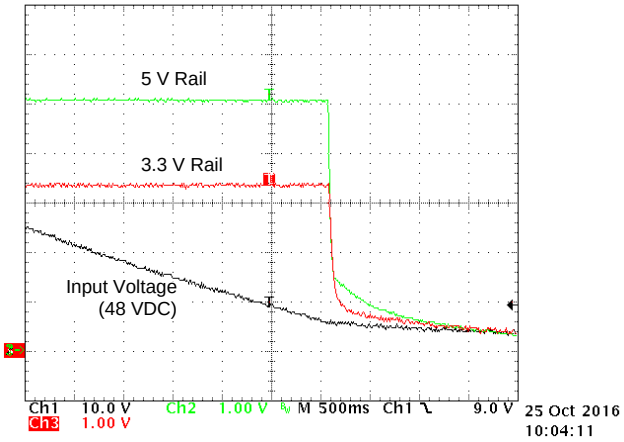


Figure 27. TIDA-00909 System Power Down (48-V Input, 5-V rail, and 3.3-V Rail)

The UVLO of the LM5018 device is set to 7.5 V. After the input of the LM5018 device reaches the UVLO threshold, the output of the LM5018 device turns the 5-V rail ON. As soon as the 5-V rail reaches 3 V, the LDO turns ON. The slight delay in the ramp-up of the 5-V rail is due to the peak current limit feature of the LM5018 to charge the large 3.3-V bulk capacitor of 100 µF at the 3.3-V LDO output.

4.1.3 5-V and 3.3-V Rails and Supply Current

The AC ripple of the 5-V rail remains well below 20 mVpp in light-load and typical load conditions, including the C2000 InstaSPIN-MOTION LaunchPad (see Figure 28 and Figure 29). Refer to typical load currents in the following Section 4.2.

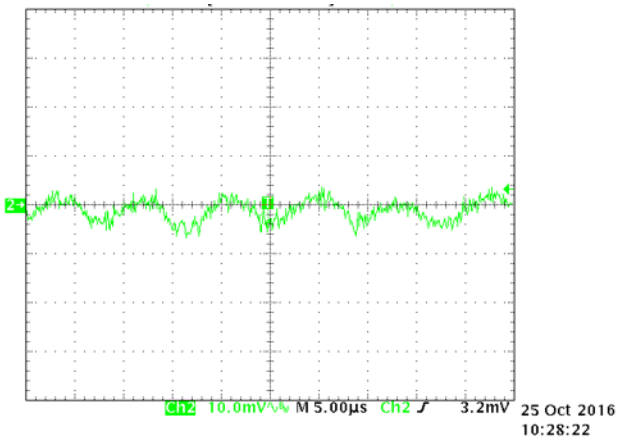


Figure 28. TIDA-00909 5-V Ripple at Nominal Load (12 mA)

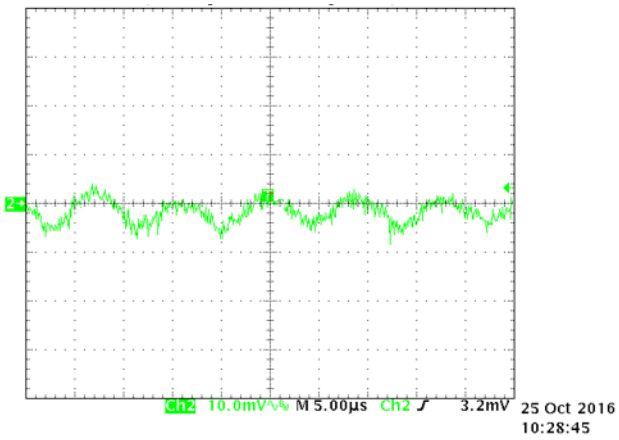


Figure 29. TIDA-00909 5-V Ripple at 167-mA Load Current Powering C2000™ LaunchPad™ Tool

Table 12. TIDA-00909 Total Current Consumption at 5 V and 3.3 V for 40-kHz and 100-kHz PWM

SUPPLY RAIL	CURRENT AT 40-kHz PWM	CURRENT AT 100-kHz PWM
3.3 V	7.8 mA	7.8 mA
5 V(1)	12 mA	13.7 mA

(1) Because the 3.3-V rail is derived from the 5-V rail through the LDO, the 5-V current includes the 3.3-V load current, too.

The 5-V load current can be split into subcircuits as the following Table 13 shows:

Table 13. Current Consumption at 5-V Split into Subcircuits

SUBCIRCUITS DRIVEN BY 5-V RAIL	CURRENT AT 40-kHz PWM	CURRENT AT 100-kHz PWM
3.3-V rail (input to LDO U7)	7.8 mA	7.8 mA
5-V LED (D5)	2 mA	2 mA
REF3333 (U10)	0.1 mA	0.1 mA
LMG5200 (U1, U2, U3)	0.7 mA, 0.7 mA, 0.7 mA	1.26 mA, 1.26 mA, 1.26 mA

The 3.3-V load current is independent of the PWM switching frequency and can be split into subcircuits as the following Table 14 shows:

Table 14. Current Consumption at 3.3-V Split into Subcircuits

SUB-CIRCUITS DRIVEN BY 5-V RAIL	CURRENT
3.3-V LED (D6)	1.5 mA
TMP302 (U10)	< 100 µA
SN74AVC8T245 (U4)	≈1 mA (driving 6x 10-k pulldown resistors)
INA240 (U8, U9, U11)	1.8 mA, 1.8 mA, 1.8 mA

In the typical use case, the TIDA-00909 device provides the 3.3-V supply rail to also power the LaunchPad. This configuration ensures proper sequencing of the 3.3-V rail on the LaunchPad as well as on the TIDA-00909 device. With the F28069M LaunchPad running the TIDA-00909 InstaSPIN-FOC firmware example, the additional current drawn by the LaunchPad was 155 mA at the 3.3-V rail. This result yields a total of 163 mA drawn from the 3.3-V rail.

The losses in the 3.3-V LDO are around 277 mW, which yields a maximum junction temperature of 99ºC at an 85ºC ambient temperature, based on the WSON package junction-to-ambient thermal resistance of 50.3ºC/W. Assuming a maximum load current of 300 mA, the maximum junction temperature is estimated to be 111ºC at an 85ºC ambient temperature.

4.2 Switch Node Voltage of GaN Inverter Half-Bridge Module

The focus of this test was to validate the transient response of the switch node voltage of the GaN inverter at 24 V and 48 V at low and maximum phase currents. The other objective of the test was to validate the capacity or amount of local bypass capacitors at each of the LMG5200 GaN power modules.

For the test, the optional EMI filter was connected between the TIDA-00909 motor-terminal output and the phase input of the Teknic low-voltage servo motor as the load.

The C2000 MCU was configured to generate a three-phase space vector with a complementary PWM with 100-kHz switching frequency and 12.5-ns deadband. The PWM duty cycle per phase was configured to drive the corresponding phase current I_A with $I_B = I_C = –0.5\ I_A$.

The LMG5200 switch node voltage was measured at the LMG5200 SW pin (pin 8) which is referenced to the PGND via close to the LMG5200 PGND pin (pin 9), as Figure 30 shows.

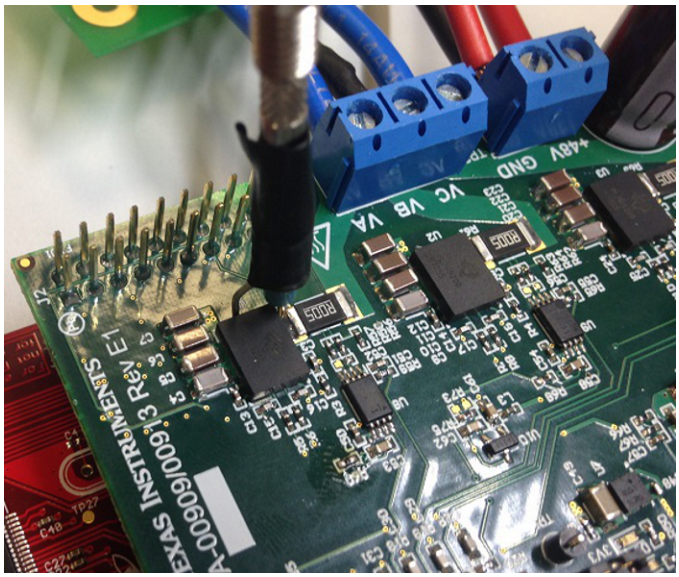


Figure 30. Test Setup for LMG5200 Switch Node Measurement (Pin SW to PGND) With Single-Ended Probe

Another objective of the test was to validate the required bypass capacity of the DC-bypass capacitors across the LMG5200 V_{IN} and PGND (see Figure 31 and Figure 32).

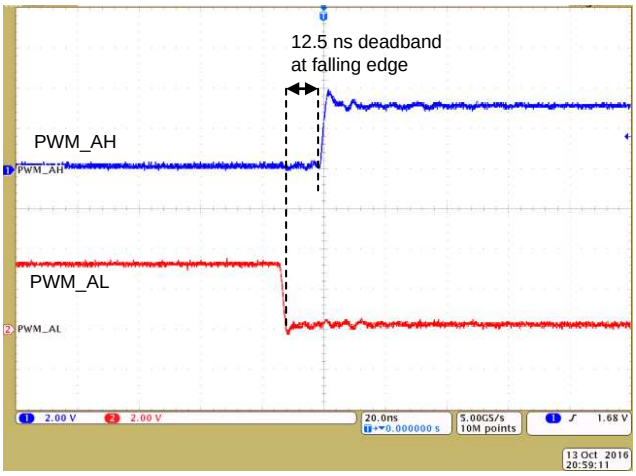


Figure 31. Rising Edge PWM A (H/L) at J2-1 and J2-3

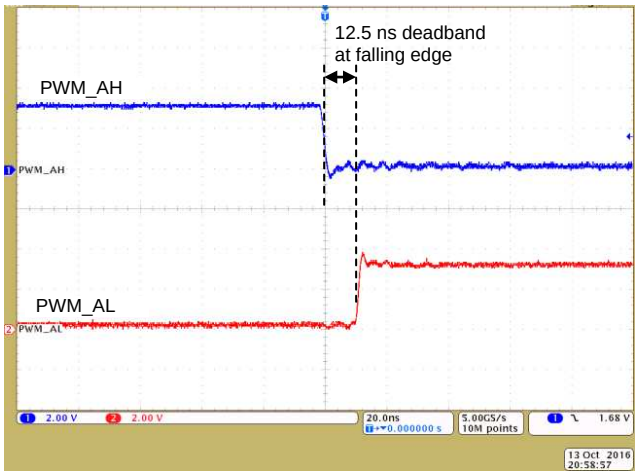


Figure 32. Falling Edge PWM A (H/L) at J2-1 and J2-3

4.2.1 24-V DC Link Voltage

The following figures outline the SW transient voltage at hard-switching and soft-switching. The LMG52000 propagation delay, as well as the 12.5-ns PWM deadband, are easy to identify.

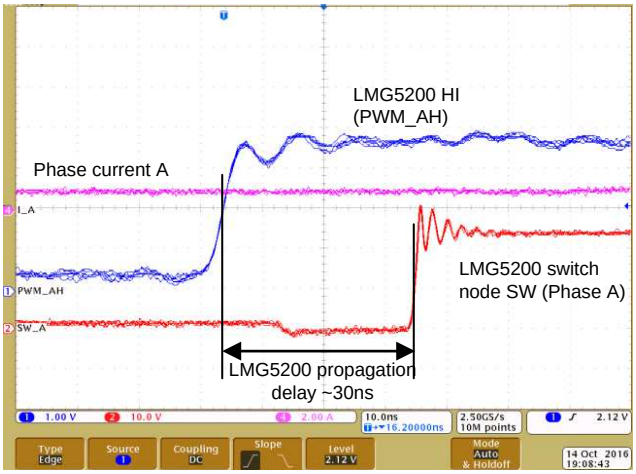


Figure 33. Phase-A Rising SW, Phase Current, and LMG5200 PWM (HI) at 24 V and 1 A

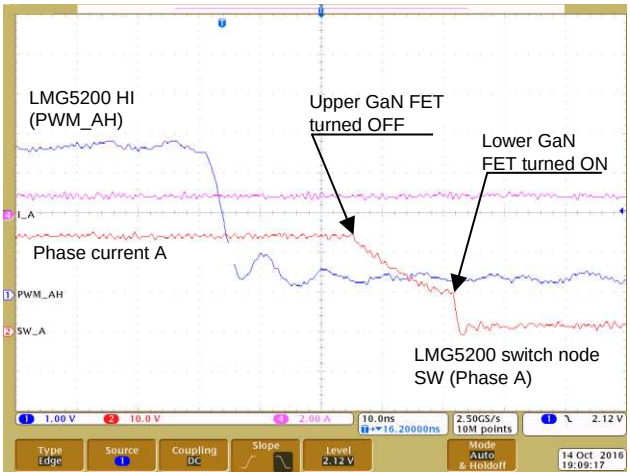


Figure 34. Phase-A Falling Switch Node (SW), Phase Current, and LMG5200 PWM (HI) at 24 V and 1 A

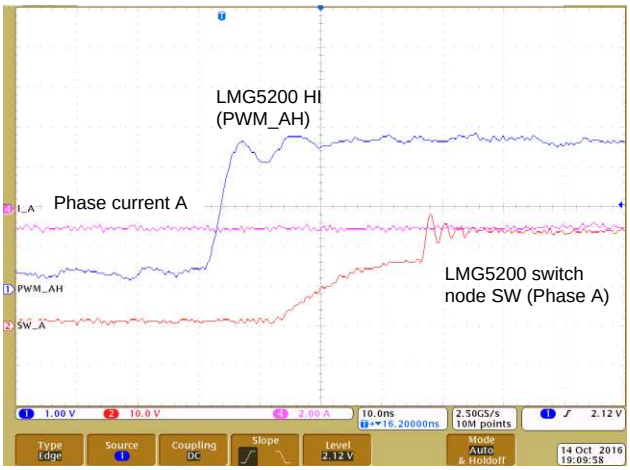


Figure 35. Phase-A Rising SW, Phase Current, and LMG5200 PWM (HI) at 24 V and –1 A

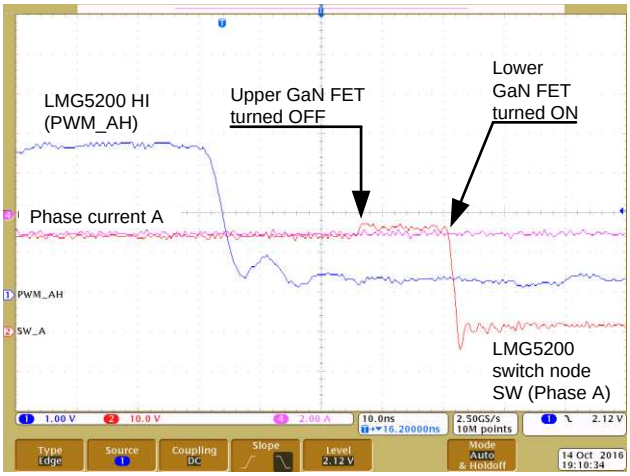


Figure 36. Phase-A Falling SW, Phase Current, and LMG5200 PWM (HI) at 24 V and –1 A

4.2.2 48-V DC Link Voltage

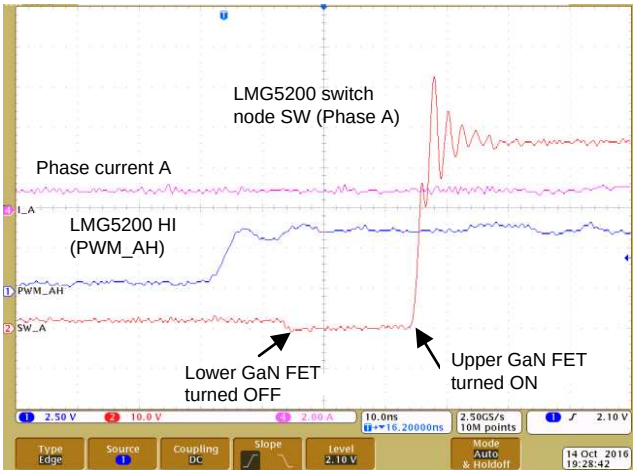


Figure 37. Phase-A Rising SW, Phase Current, and LMG5200 PWM (HI) at 48 V and 1 A

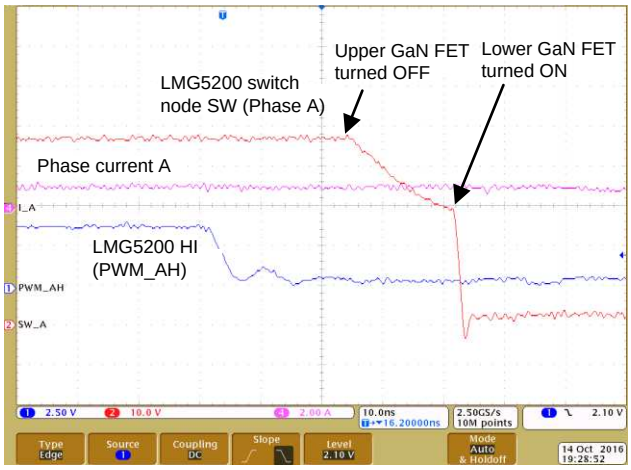


Figure 38. Phase-A Falling SW, Phase Current, and LMG5200 PWM (HI) at 48 V and 1 A

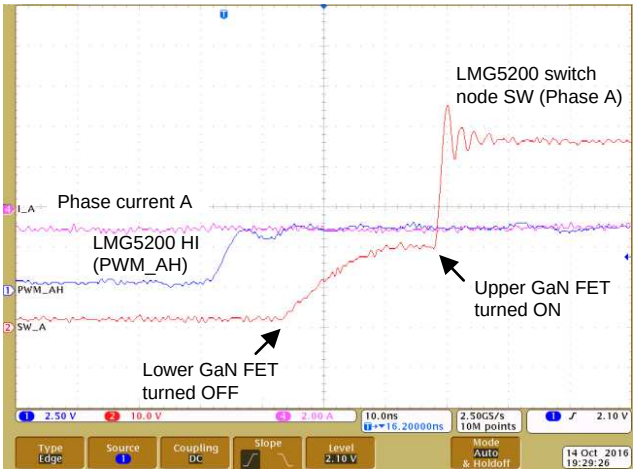


Figure 39. .Phase-A Rising SW, Phase Current, and LMG5200 PWM (HI) at 48 V and –1 A

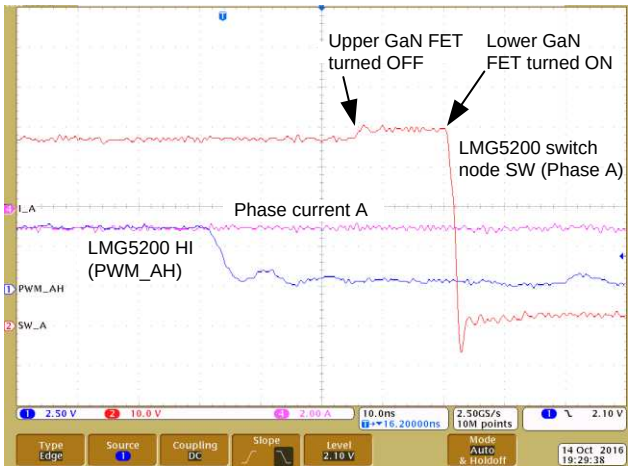


Figure 40. Phase-A Falling SW, Phase Current, and LMG5200 PWM (HI) at 48 V and –1 A

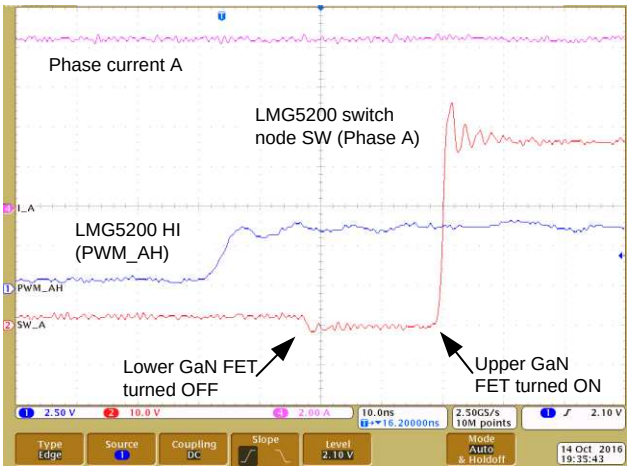


Figure 41. Phase-A Rising SW, Phase Current, and LMG5200 PWM (HI) at 48 V and 10 A

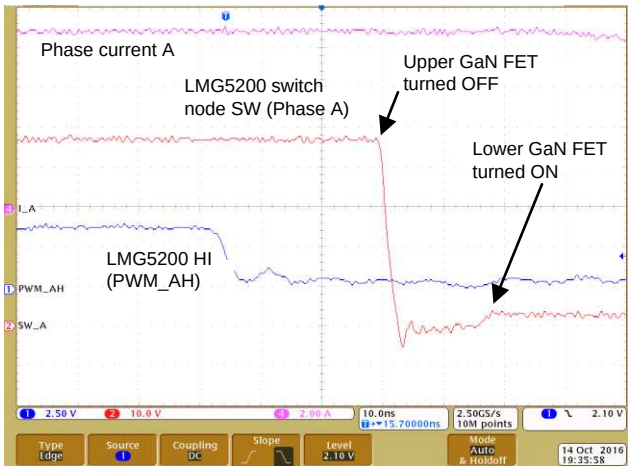


Figure 42. Phase-A Falling SW, Phase Current, and LMG5200 PWM (HI) at 48 V and 10 A

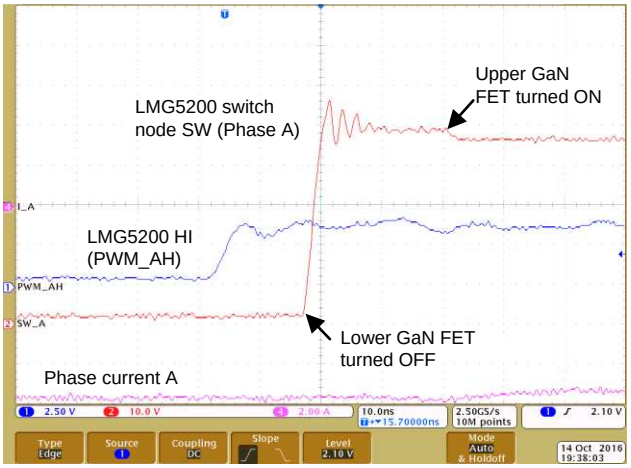


Figure 43. Phase-A Rising SW, Phase Current, and LMG5200 PWM (HI) at 48 V and –10 A

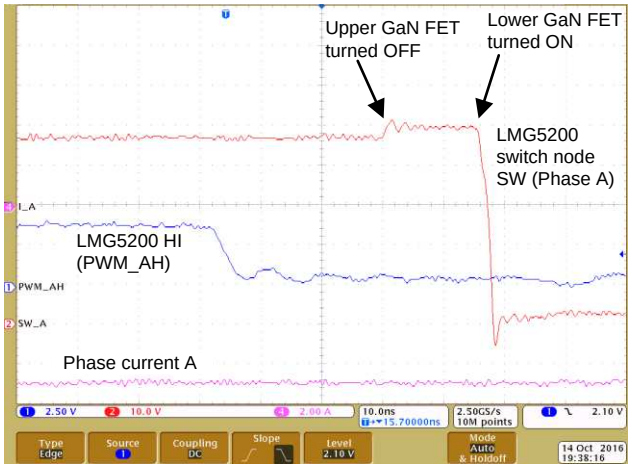


Figure 44. Phase-A Falling SW, Phase Current, and LMG5200 PWM (HI) at 48 V and –10 A

Figure 45 and Figure 46 show zoomed-in images of the hard-switching switch-node transition (both edges):

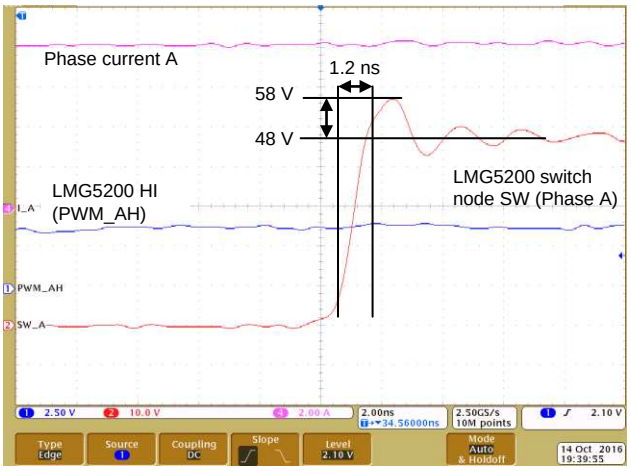


Figure 45. Phase-A Rising SW, Phase Current, and LMG5200 PWM (HI) at 48 V and 10 A

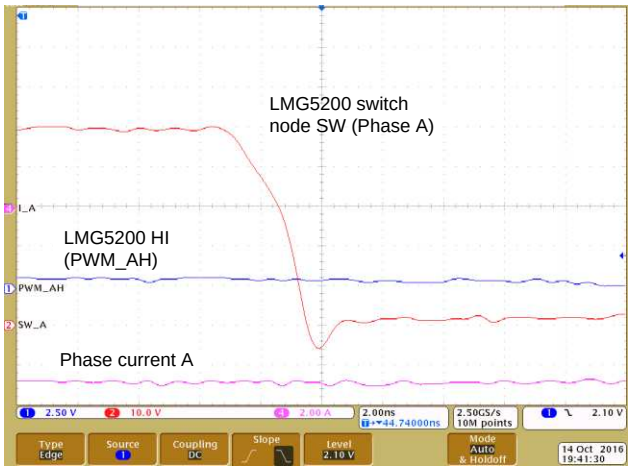


Figure 46. Phase-A Falling SW, Phase Current, and LMG5200 PWM (HI) at 48 V and –10 A

4.2.3 48-V DC Link Voltage With Reduced Bypass Caps

For this test the local bypass capacitors at the LMG5200 device were reduced to a single 3.3-µF, 100-V ceramic capacitor in parallel to one 100-nF, 100-V ceramic capacitor, as the following Figure 47 shows for phase A (U1). C6 and C7 were removed for this test.

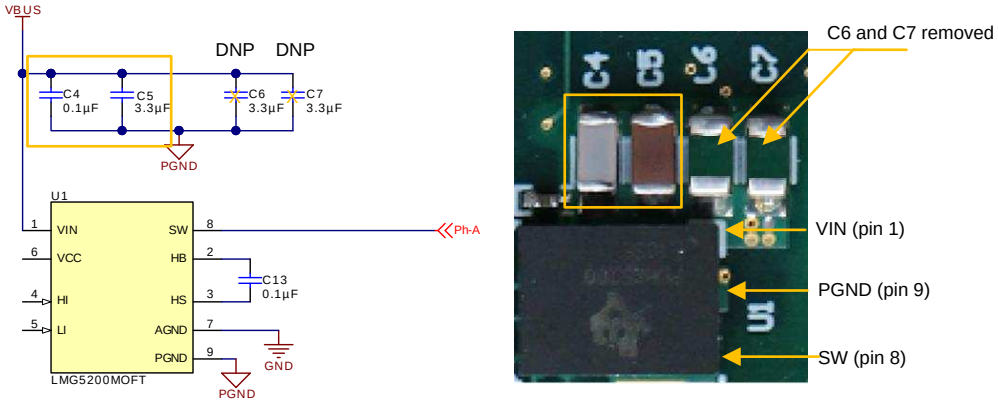


Figure 47. LMG5200 (U1) With Reduced Local-Bypass Caps

The following measurements outline the hard-switching transition at a 48-V DC-link voltage with reduced bypass capacitors, as demonstrated in the preceding Figure 47.

The measurable impact is insignificant and affirms that the bypass capacitors at each LMG5200 device can be reduced as shown in Figure 47.

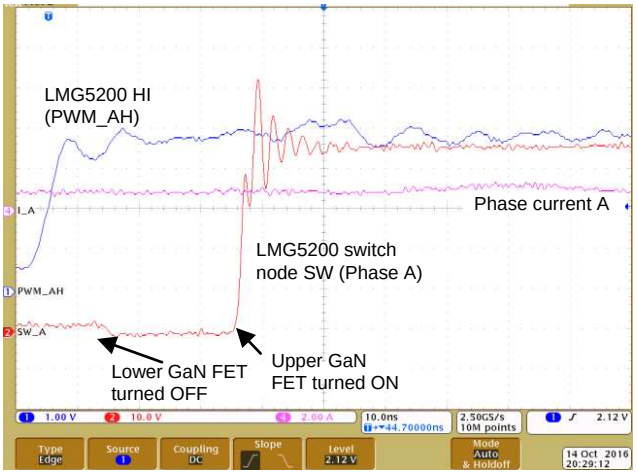


Figure 48. Phase-A Rising SW, Phase Current, and LMG5200 PWM (HI) at 48 V and 1 A

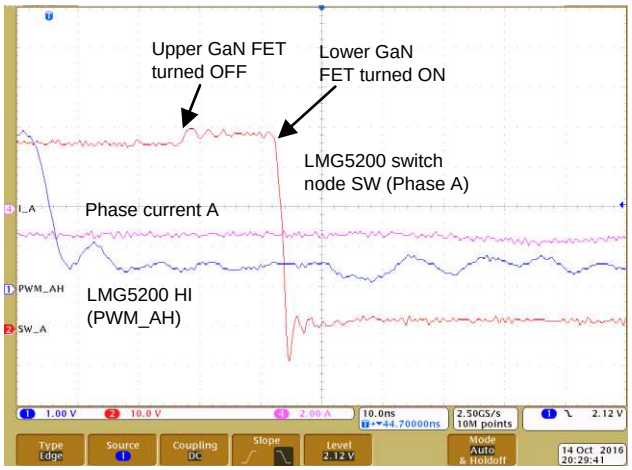


Figure 49. Phase-A Falling SW, Phase Current, and LMG5200 PWM (HI) at 48 V and –1 A

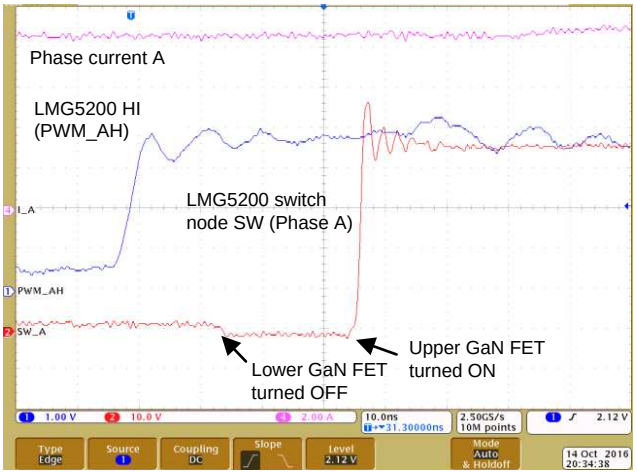


Figure 50. Phase-A Rising SW, Phase Current, and LMG5200 PWM (HI) at 48 V and 10 A

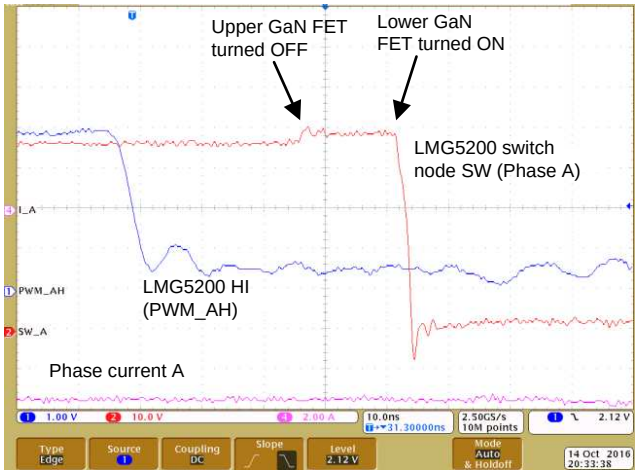


Figure 51. Phase-A Falling SW, Phase Current, and LMG5200 PWM (HI) at 48 V and –10 A

Figure 52 shows a zoomed-in image of the hard-switching switch-node transition:

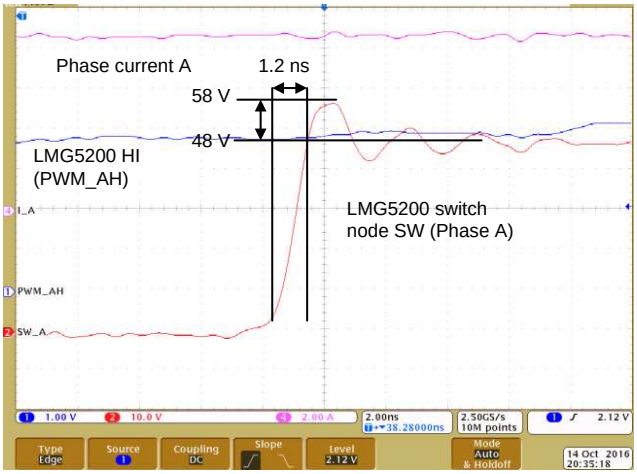


Figure 52. Phase-A Rising SW, Phase Current, and LMG5200 PWM (HI) at 48 V and 10 A

4.2.4 DC-Link Voltage Ripple at Maximum Load Current

The following Figure 53 and Figure 54 show the DC-link voltage AC ripple measured at the 220-µF bulk capacitor with a 24-V and 48-V DC input. The PWM switching frequency was set to 40 kHz. The AC ripple voltage remains below 400 mVpp.

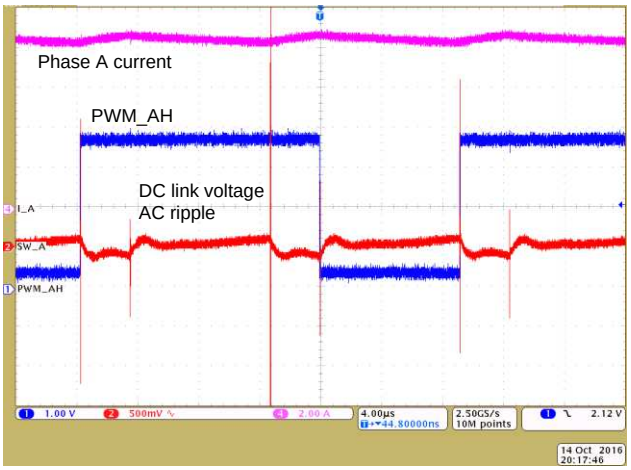


Figure 53. DC-Link Voltage AC Ripple at 24-V DC, 40-kHz PWM, I_A = 10 A, I_B = I_C = –5 A

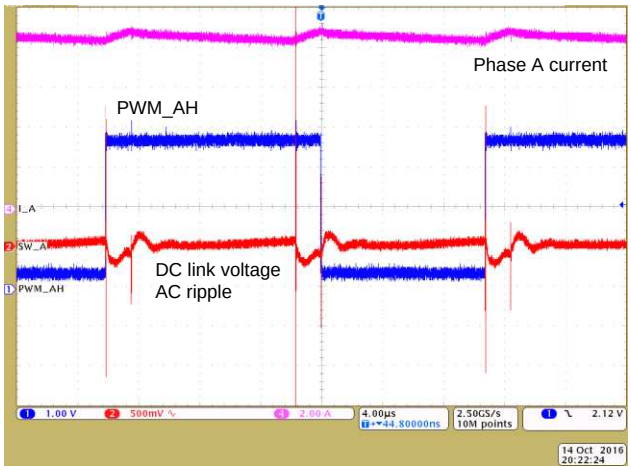


Figure 54. DC-Link Voltage AC Ripple at 48-V DC, 40-kHz PWM, I_A = 10 A, I_B = I_C = –5 A

4.3 Inverter Efficiency and Thermal Characteristic

4.3.1 Efficiency Measurements

The efficiency testing was performed at a 27ºC lab temperature using a Tektronix PA4000 Power Analyzer. The TIDA-00909 device was powered with a 48-V DC and a Teknic low-voltage servo motor was used as the load. The motor was run at a zero load torque due to lack of a dynamometer. The test software implemented on the C2000 LaunchPad was configured for closed-loop current control and generated the corresponding PWM to drive an impressed three-phase AC current at a 10-Hz frequency with configurable amplitude. The PWM carrier frequency was set to either 40 Hz or 100 kHz. During the efficiency testing, a fan with a linear airflow of 3.2 m/s was used to ensure almost constant board temperature of the TIDA-00909 device independent of the load current. Figure 55 shows an image of the test setup.

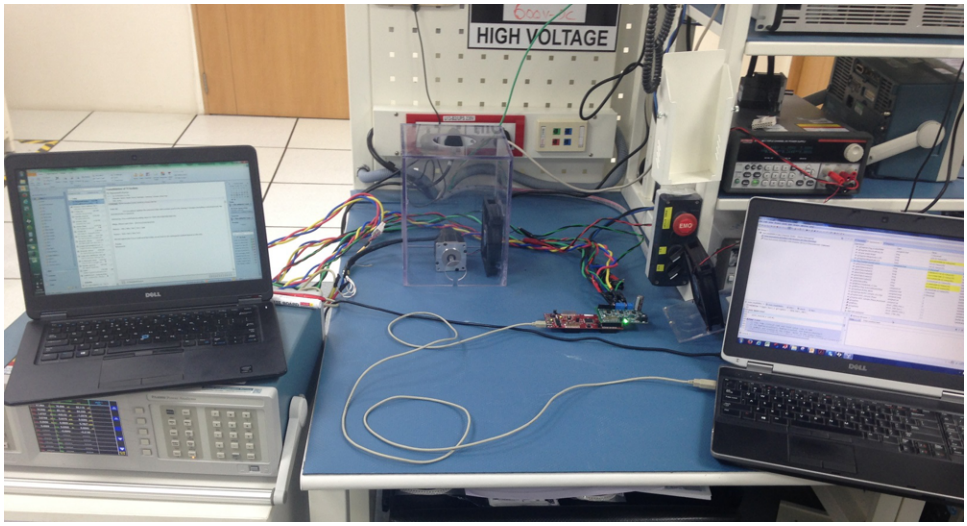


Figure 55. TIDA-00909 Test Setup for Inverter Efficiency Analysis

The following Figure 56 shows the TIDA-00909 power losses versus the three-phase motor load current in A_{RMS}. Note that these numbers do not include the power losses of the C2000 LaunchPad.

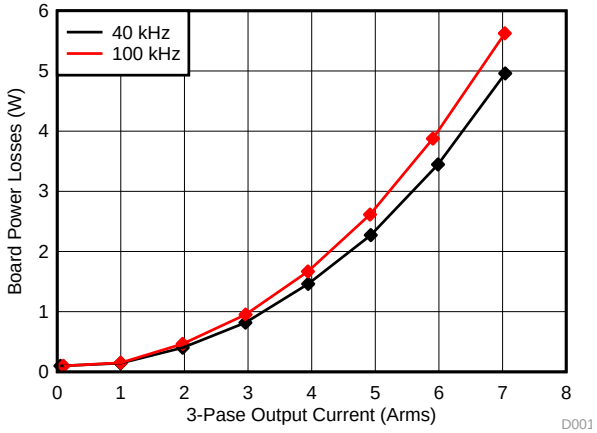


Figure 56. TIDA-00909 Board Losses at 48-V Input versus Three-Phase Output Current

The TIDA-00909 board power losses at the maximum load current of $7A_{RMS}$ were 4.95 W at a 40-kHz PWM and 5.65 W at a 100-kHz PWM. The TIDA-00909 power losses are dominated by the losses in the GaN FETs (LMG5200) and the losses in the 5-mΩ shunt resistors.

The efficiency with an output power of 83 W while driving the Teknic servo motor was 94.3% at a 40-kHz PWM and 93.6% at a 100-kHz PWM. The theoretical maximum efficiency at a 48-V, 400-W maximum input power with a phase-to-phase voltage of $34\text{-}V_{RMS}$ (space vector PWM) at a $7\text{-}A_{RMS}$ phase current would be 98.7% at a 40-kHz PWM and 98.5% at a 100-kHz PWM.

4.3.2 Thermal Analysis and SOA

The thermal analysis of the design was performed at a 27ºC lab temperature with a 48-V DC input with a 40-kHz PWM and 100-kHz PWM with the low-voltage servo motor driven with sinusoidal phase currents at a 50% load current (3.6 A_{RMS}, 5-A peak) and 100% load current (7 A_{RMS}, 10-A peak). This test did not use a heatsink or fan. Figure 57 shows an image of the test setup.

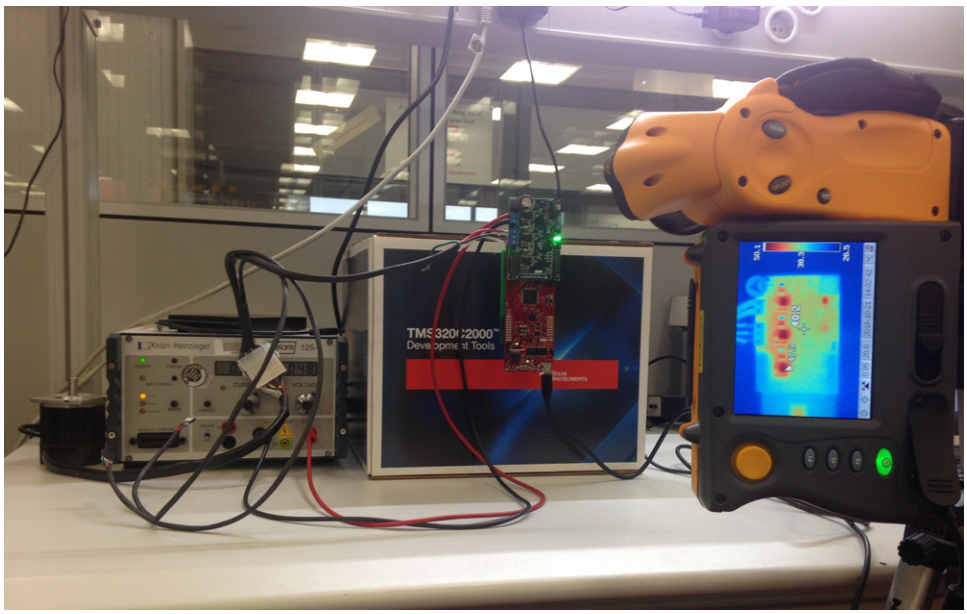


Figure 57. TIDA-00909 Test Setup for Thermal Analysis

The following figures show pictures of the thermal tests at a 27ºC ambient temperature with 50% and 100% load current with either a 40-kHz or 100-kHz PWM switching frequency.

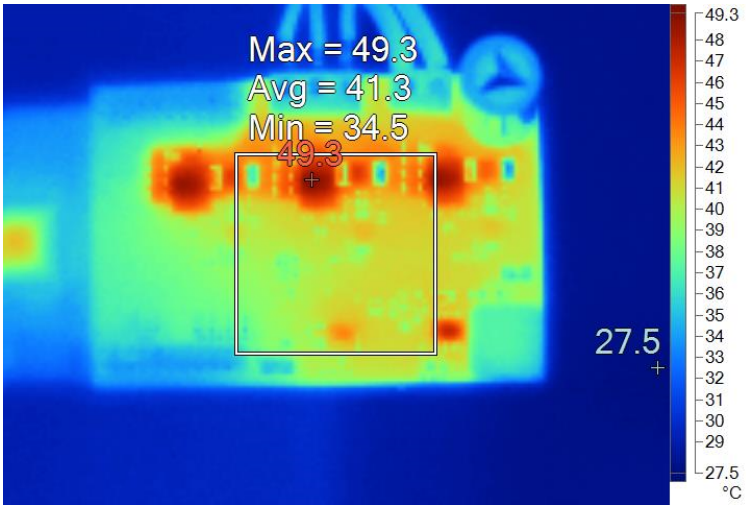


Figure 58. Thermal Image of TIDA-00909 at 50% Load Current (3.6 A_{RMS}) at 40-kHz PWM

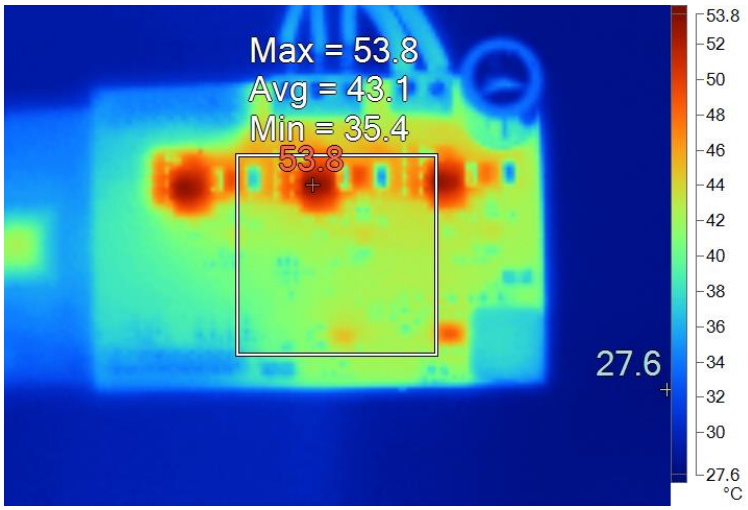


Figure 59. Thermal Image of TIDA-00909 at 50% Load Current (3.6 A_{RMS}) at 100-kHz PWM

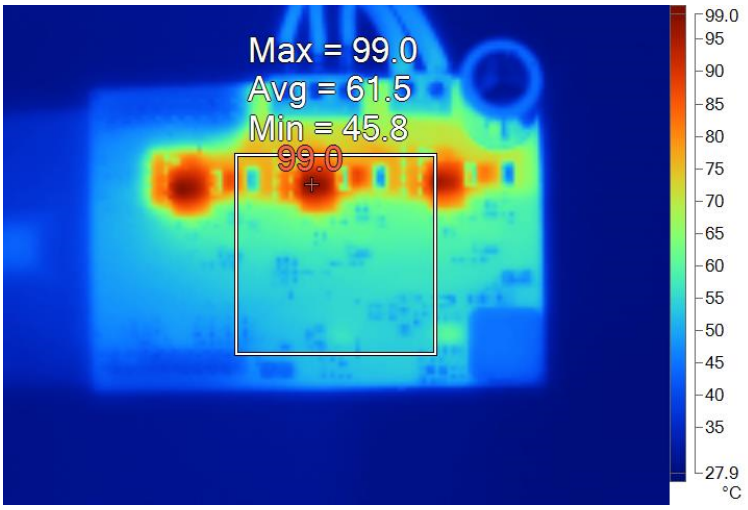


Figure 60. Thermal Image of TIDA-00909 at 100% Load Current (7 A_{RMS}) at 40-kHz PWM

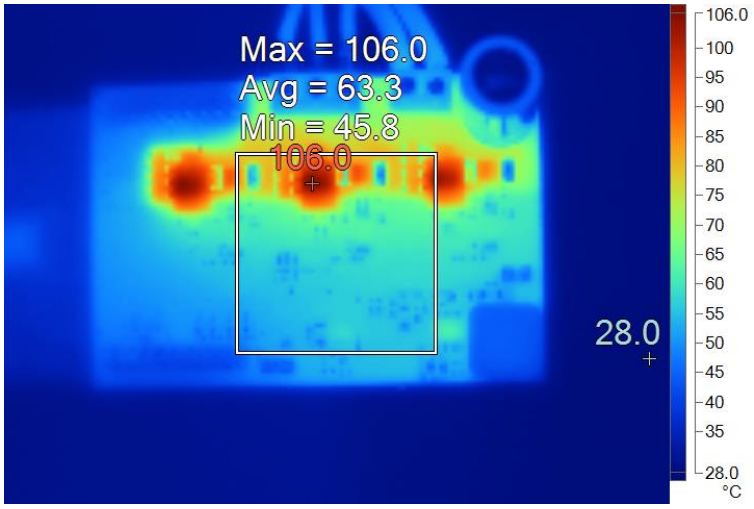


Figure 61. Thermal Image of TIDA-00909 at 100% Load Current (7 A_{RMS}) at 100-kHz PWM

The LMG5200 maximum junction temperature at the maximum load is estimated based on the power losses of the LMG5200 at 1.3 W at a 40-kHz PWM and at 1.53 W at a 100-kHz PWM. The worst-case junction temperature of the LMG5200 at a 100-kHz PWM switching frequency would be 124ºC, assuming that all of the LMG5200 power losses are dissipated through the top-side package.

Figure 62 shows the estimated safe operating area for the TIDA-00909 with only natural convection.

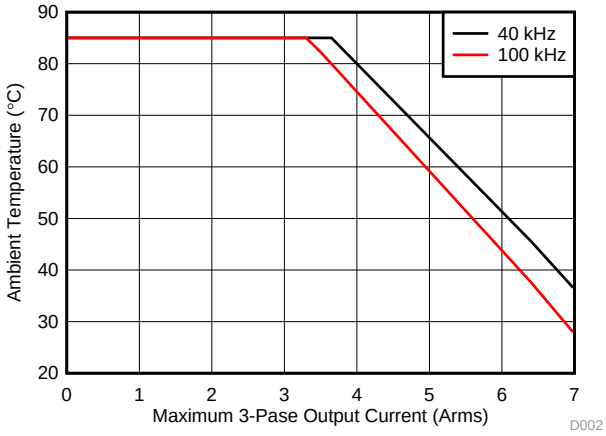


Figure 62. Safe Operating Area of TIDA-00909 With Natural Convection

4.4 System Test With High-Speed Synchronous Motors

4.4.1 High-Speed BLDC Motor for Drones

The following tests have been performed with a low-inductance, high-speed brushless DC motor, such as that used with drones. The motor was driven with sinusoidally-impressed phase currents with 2 V_{RMS} of amplitude and 1000-Hz frequency. The PWM switching frequency was set to 100 kHz. The test has been done with an optional EMI output filter as the test setup in Figure 63 shows. The scope probes were connected to the phase VC motor terminal and the filtered-phase VC output after the EMI output filter was referenced to GND. A current probe was used to measure the phase current IC.

The electric parameters of the low-inductance brushless DC (BLDC) motor stator are:
R_S = 0.05 Ω, L_S = 4.1 µH, I_{MAX} = 4.5 A_{RMS}.

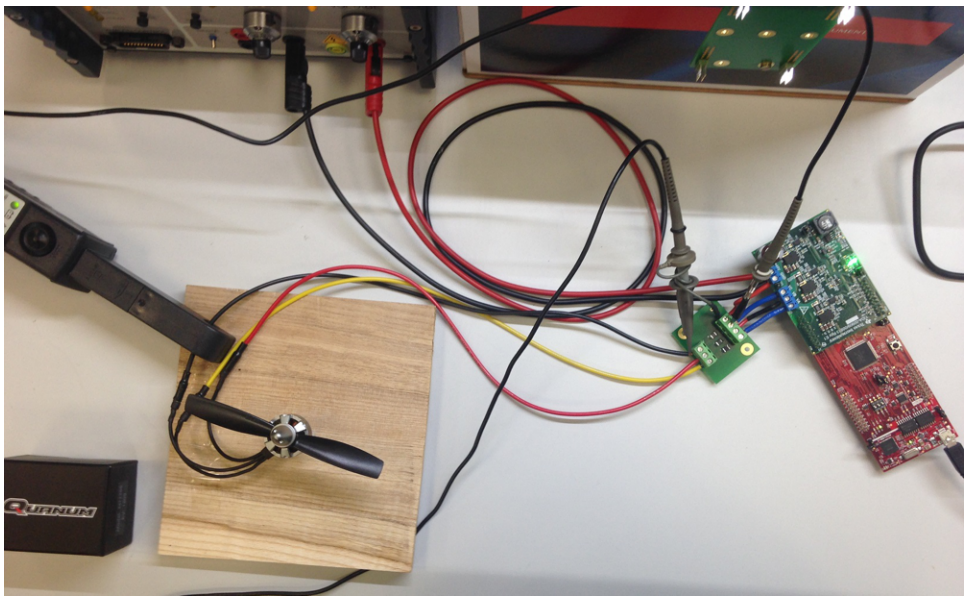


Figure 63. Test Setup Image With Oscilloscope Probe Points

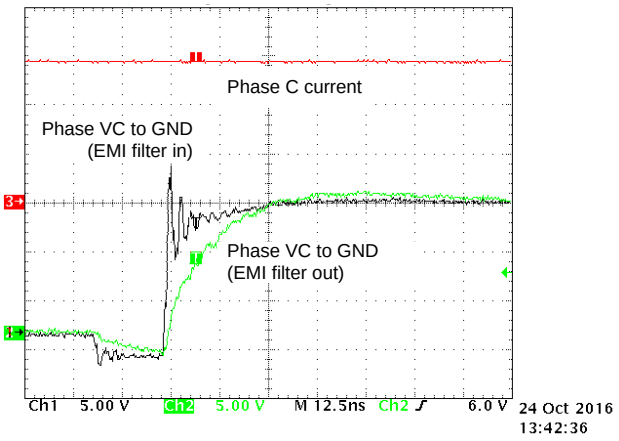


Figure 64. Phase Voltage V_C, $V_{C\text{-}EMI}$, and Phase Current I_C at 100-kHz PWM With ESC PMSM

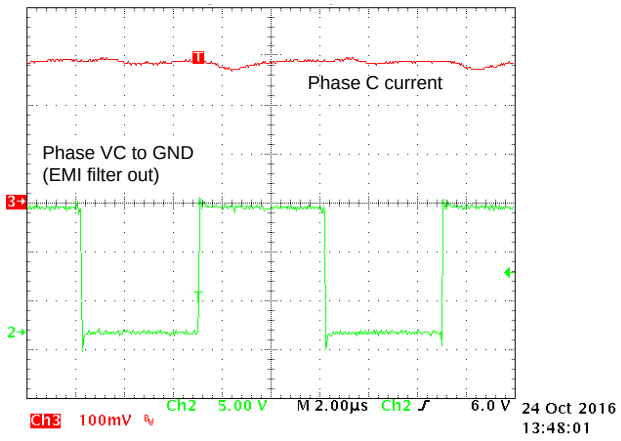


Figure 65. Zoom-in of Figure 64 to Show I_C Phase Current Ripple

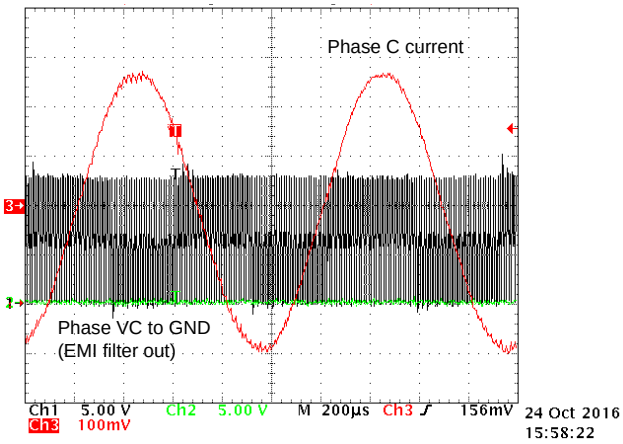


Figure 66. Zoom-out of Figure 64 to Show Phase Current I_C Period

As expected with the EMI LCR low-pass filter, the rise time of the transient phase voltage referenced to GND is reduced to around 25 ns.

Due to the high PWM frequency, the BLDC motor phase-current ripple at 100-kHz PWM is reduced to ±100 mA.

To validate the TIDA-00909 phase current sensing and phase voltage feedback network, the corresponding voltages for I_C (pin J1-18) and V_C (pin J1-12) were measured with the C2000 MCU-embedded 12-bit ADC center aligned to the 100-kHz PWM. The values shown represent the measured voltage at the corresponding interface pins for I_C (pin J1-18) and V_C (pin J1-12). Note that the output voltage of the phase current sense amplifier is inverted and has a 1.65-V offset. Applying the correct scaling factor $I_{A\text{-}PEAK} = (V(I_A) – 1.65\ V) \times 10\ A/V = (1.935\ V – 1.65\ V) \times 10\ A/V = 2.85\ A_{PEAK}$ (2 V_{RMS}).

The following figures show all three corresponding voltages for phase currents I_A (pin J1-14), I_B (pin J1-16), and I_C (pin J1-18).

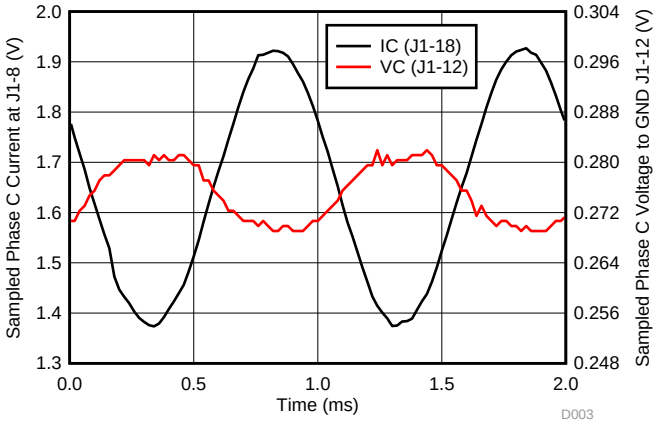


Figure 67. Phase Current I_C Output Voltage and V_C Phase-to-GND Voltage Sampled With C2000™ MCU Center-Aligned at 100-kHz PWM

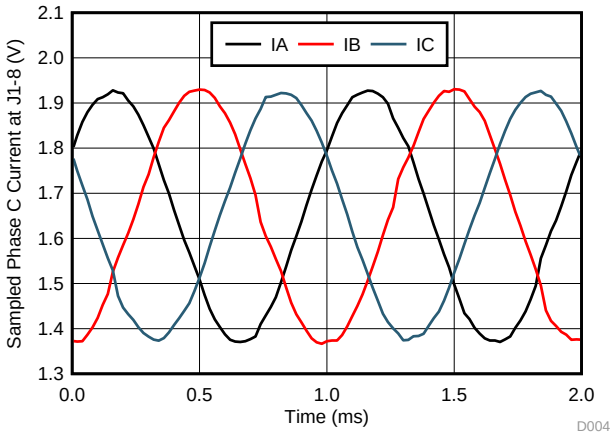


Figure 68. Phase Currents I_A, I_B, and I_C Output Voltage Sampled With C2000™ MCU Center-Aligned at 100-kHz PWM

4.4.2 Low-Voltage Servo Motor (Teknic)

The following tests have been performed with a low-voltage synchronous servo motor Teknic M-2310P-LN-04K (four pole pairs), which may be used with servo drives. The motor was driven with sinusoidally-impressed phase currents with 2 V_{RMS} of amplitude and 100-Hz frequency. The PWM switching frequency was set to 40 kHz. The test has been done with an optional EMI output filter as previously shown. The scope probes were connected to the phase VC motor terminal and the filtered phase VC output after the EMI output filter was referenced to GND. A current probe was used to measure the phase current IC.

The Teknic M-2310P-LN-04K synchronous motor stator electric parameters are:
R_S = 0.363 Ω, L_S = 160 µH, I_{MAX} = 7 A_{RMS}

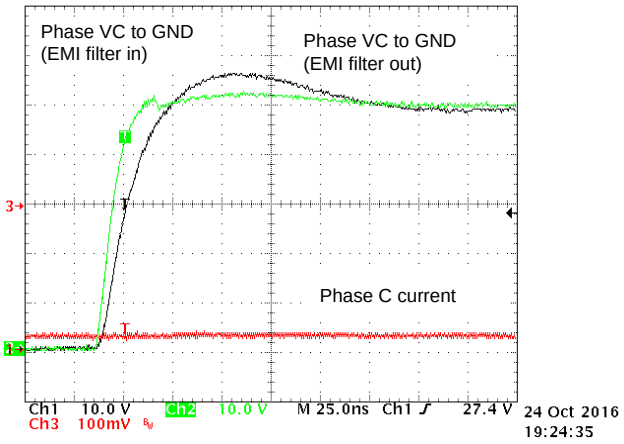


Figure 69. V_C at EMI Input and EMI Output Filter and Phase Current I_C at 40-kHz PWM With PMSM

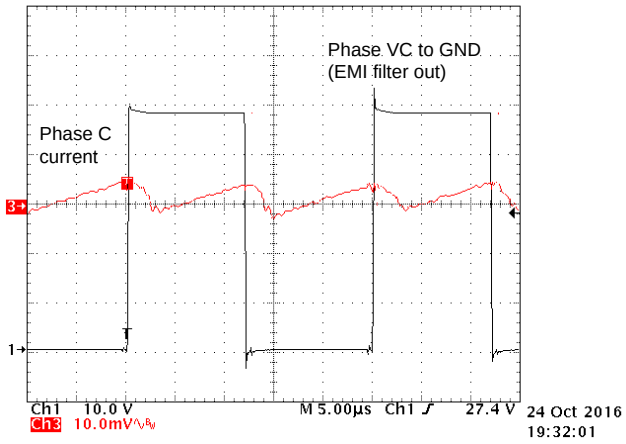


Figure 70. Zoom-in of Figure 69 to Show I_C Phase Current Ripple

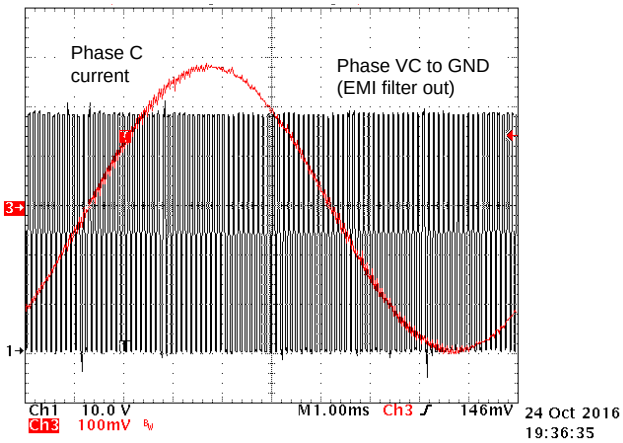


Figure 71. Zoom-out of Figure 69 to Show Phase Current I_C Period

The following Figure 72 and Figure 73 show all three corresponding phase voltages sampled at the TIDA-00909 interface J1-6, J1-8, and J1-10, as well as the equivalent voltages of the phase currents I_A (pin J1-14), I_B (pin J1-16), and I_C (pin J1-18). A peak voltage of 1.935 V equals a phase current of (1.935 V – 1.65 V) × 10 = 2.85 V_{PEAK} or 2 V_{RMS}.

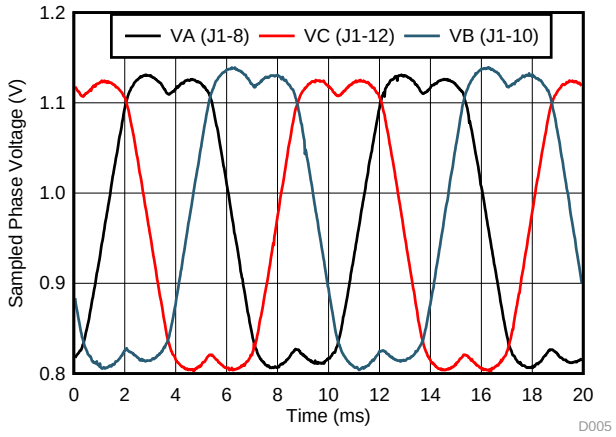


Figure 72. Phase Voltages V_A, V_B, and V_C Output Voltage Sampled With C2000™ MCU Center-Aligned at 40-kHz PWM

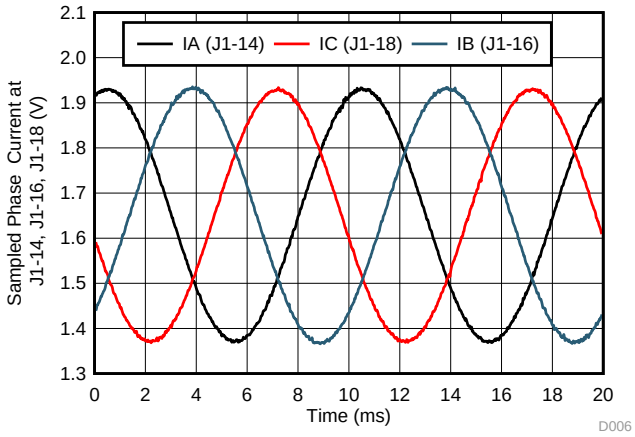


Figure 73. Phase Currents I_A, I_B, and I_C Output Voltage Sampled With C2000™ MCU Center-Aligned at 40-kHz PWM

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00909.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00909.

5.3 PCB Layout

5.3.1 Layout Recommendations

The layout for the LMG5200 in the TIDA-00909 PCB followed the guidelines referenced in the *Layout Considerations for LMG5200 GaN Power Stage* application report [1].

The power-loop parasitic impedance is minimized by having a small return path (layer 2 below the LMG5200) to the input capacitor (between VIN and PGND) and directly underneath the first layer (see Figure 74). The loop inductance is reduced due to inductance cancellation as the return current is directly underneath and flowing in the opposite direction. Another crucial guideline is that the VCC capacitor and the bootstrap capacitor be placed as close to the device as possible and in the first layer. Carefully consider the AGND connection of the LMG5200 device, as it should not be directly connected to PGND so that PGND noise does not directly shift AGND and cause spurious switching events due to noise injected in HI and LI signals. See the ground cut between the PGND layer and GND layer in Figure 74.

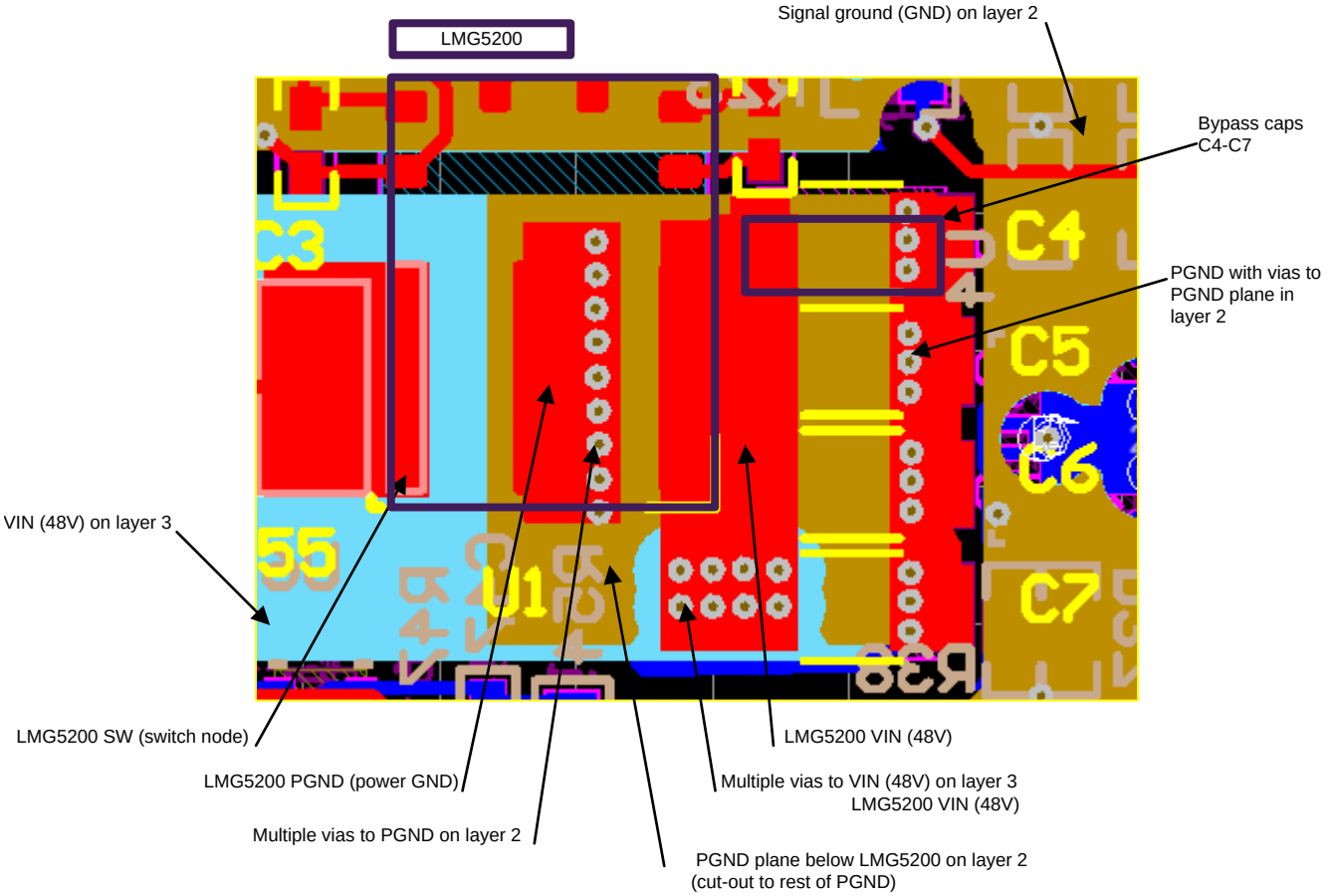


Figure 74. LMG5200 Optimized Layout With Local Bypass Caps

5.3.2 Layer Plots

To download the layer plots, see the design files at TIDA-00909.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00909.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00909.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00909.

6 Software Files

To download the software files, see software files at TIDA-00909.

7 Related Documentation

1. Texas Instruments, *Layout Considerations for LMG5200 GaN Power Stage*, LMG5200 Application Report (SNVA729)
2. Texas Instruments, *Optimizing GaN Performance with an Integrated Driver*, White Paper (SLYY085)
3. Texas Instruments, *GaN FET Module Performance Advantage over Silicon*, White Paper (SLYY071)
4. Texas Instruments, *Gallium Nitride (GaN) Solutions*, Overview Page (www.ti.com/gan)
5. Texas Instruments, *REF33xx 3.9-µA, SC70-3, SOT-23-3, and UQFN-8, 30-ppm/ºC Drift Voltage Reference,*, REF33xx Datasheet (SBOS392)
6. Texas Instruments, *48V 3-Phase Inverter with Shunt-based In-line Motor Phase Current Sensing Reference Design, TIDA-00913 Reference Design*, TIDA-00913 Reference Design (TIDUCE8)
7. Texas Instruments, *LP3869x/-Q1 500-mA Low-Dropout CMOS Linear Regulators Stable With Ceramic Output Capacitors,*, LP3869x/-Q1 Datasheet (SNVS321)
8. Texas Instruments, *WEBENCH® Design Center*, Overview Page (www.ti.com/webench)
9. Texas Instruments, *TINA-TI Simulation Software*, Overview Page (www.ti.com/tina-ti)
10. Texas Instruments, *AN-2162 Simple Success With Conducted EMI From DC-DC Converters,* AN-2162 Application Report (SNVA489)
11. Texas Instruments, *TI InstaSPIN™ Motor Control Solutions*, Overview Page (www.ti.com/ww/en/mcu/instaspin/)
12. Texas Instruments, *MotorWare™ Software*, MOTORWARE Tool Folder (www.ti.com/tool/motorware)
13. Texas Instruments, *Low Voltage Servo Motor - Low voltage servo (encoder) motor and wiring harness*, LVSERVOMTR Tool Folder (www.ti.com/tool/lvservomtr)
14. DYS, *Quanum MT Series 2208 1800KV Brushless Multirotor Motor ,*, (www.dys.hk)

7.1 Trademarks

8 Terminology

GaN— Gallium Nitride

HEMT— High-electron mobility transistor

9 About the Author

MARTIN STAEBLER is a system architect in the Industrial Systems-Motor Drive team at Texas Instruments, where he is responsible for specifying and developing reference designs for industrial drives.

10 Recognition

The author would like to recognize the excellent contribution from **GUANG ZHOU**, **PAWAN NAYAK**, **KRISTEN MOGENSEN**, **PAL BOELE**, and **ALBERTO DORONZO** on the TIDA-00909 schematics and layout capture, the TIDA-00909 test software development, and the TIDA-00909 design test and validation.

Revision History A

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (Nov 2016) to A Revision	Page
• Changed document by converting to .XML format	1

Revision History B

Changes from A Revision (February 2017) to B Revision	Page
• Changed *Figure 12* to updated schematic with values of "120 nH" instead of "120 nF"	14

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