TI Designs

Electronically Commutated Motor Reference Design for HVAC Blowers With Low BOM Cost

Description

The TIDA-01353 reference design is a discrete MOSFET based three-phase inverter for driving brushless DC (BLDC) motors rated up to 375 W in HVAC blower applications using a sensorless, trapezoidal control method. The cycle-by-cycle overcurrent protection feature protects the power stage from overcurrent, and the board can work up to 85°C ambient. This TI Design is a tested, ready-to-use hardware and software platform for the speed control of high-voltage BLDC motors using sensorless trapezoidal control.

Resources

TIDA-01353	Design Folder
MSP430F5132	Product Folder
UCC27714	Product Folder
TLV316	Product Folder
UCC28881	Product Folder
LP2985-33	Product Folder
LMT84LP	Product Folder
TPD1E10B06	Product Folder
InstaSPIN	Product Folder

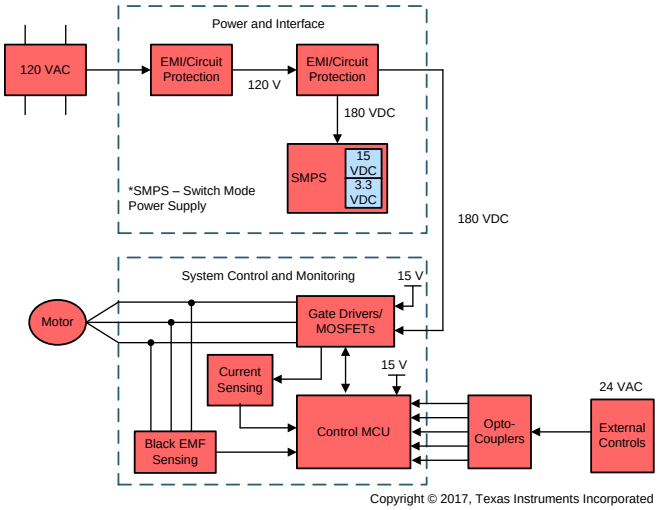
TI E2E™ Community — ASK Our E2E Experts

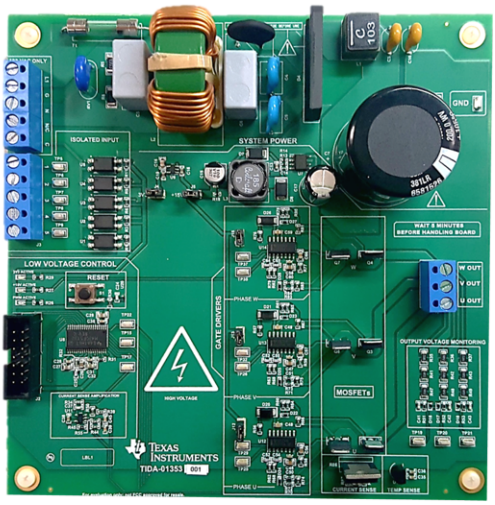
Features

- Onboard Temperature Sensing
- Optocoupling for Circuit Isolation
- Sensorless Motor Control
- Current Sensing Using Single Shunt Resistor on DC Bus
- Sensorless Trapezoidal Control Using the TI InstaSPIN-BLDC BEMF Integration Method
- Low BOM Cost, High-Efficiency ECM Motor Controller
- Five Preset Motor Speeds

Applications

- Appliances
- Building Automation
- Motor Drives
- Brushless DC Drives
- HVAC Motor Control





1 System Overview

1.1 System Description

Any HVAC system in the world has a blower motor. This integral component is responsible for moving air from the return through the evaporator coil or heating elements and through the supply vents. For years, the most popular choice for a blower motor was a permanent split capacitor motor, or PSC. Used primarily in a single-phase HVAC system, the PSC motor substitutes the third leg of the motor with a capacitor, introducing an offset phase of 90 degrees. However clever this may be, the design suffers from one main drawback—efficiency.

The TIDA-01353 is a three-phase inverter drive based on discrete MOSFETs, which drive an electronically commutated motor, or ECM, rated at 115-V AC and ½ horsepower. This TI Design uses the sensorless, trapezoidal control method and has higher efficiency than the common PSC motor.

The motor winding current sensing is done using a single shunt resistor on the DC Bus return with an external, low-power, high-bandwidth operational amplifier. The cycle-by-cycle overcurrent protection feature protects the power stage from large current spikes and is achieved through the integrated, high-speed high-precision comparator and programmable reference, which is a built-in feature of the MSP430F5132. This TI Design can work in ambient temperatures up to 85°C and at a 375-W power rating.

This TI Design also integrates isolation for the preset speed controls through the use of optocoupler isolation ICs. These couplers accept the 24-V AC control signals from the air handler control circuit board, allowing for a seamless transition between preexisting motor controller modules and this TI Design for testing purposes.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS			DETAILS
Motor	6-pole, single phase, ½ HP			—
Input voltage	115 V ±10%, 1-phase AC, 50/60 Hz			See Section 1.5.1
DC link voltage	163.5-V DC (typical)			See Section 3.2
Rated input power	375 W			See Section 1.5.1
Control method	Sensorless trapezoidal			See Section 2.2.3
Inverter switching frequency	20 kHz			See Section 1.5.3
Motor electrical frequency	Min	Nom	Max	See Section 1.5.3
	30 Hz	—	53 Hz	
Feedback signals	Three motor winding voltages, DC bus voltage, low-side DC bus current			See Section 1.5.6 through Section 1.5.8
Protections	Cycle-by-cycle current			See Section 1.5.5 through Section 1.5.8
	Input undervoltage			
	Over temperature			
Operating ambient	–20°C to 85°C			—
Isolated control input	24-V AC ± 20%			See Section 1.5.9

1.3 Block Diagram

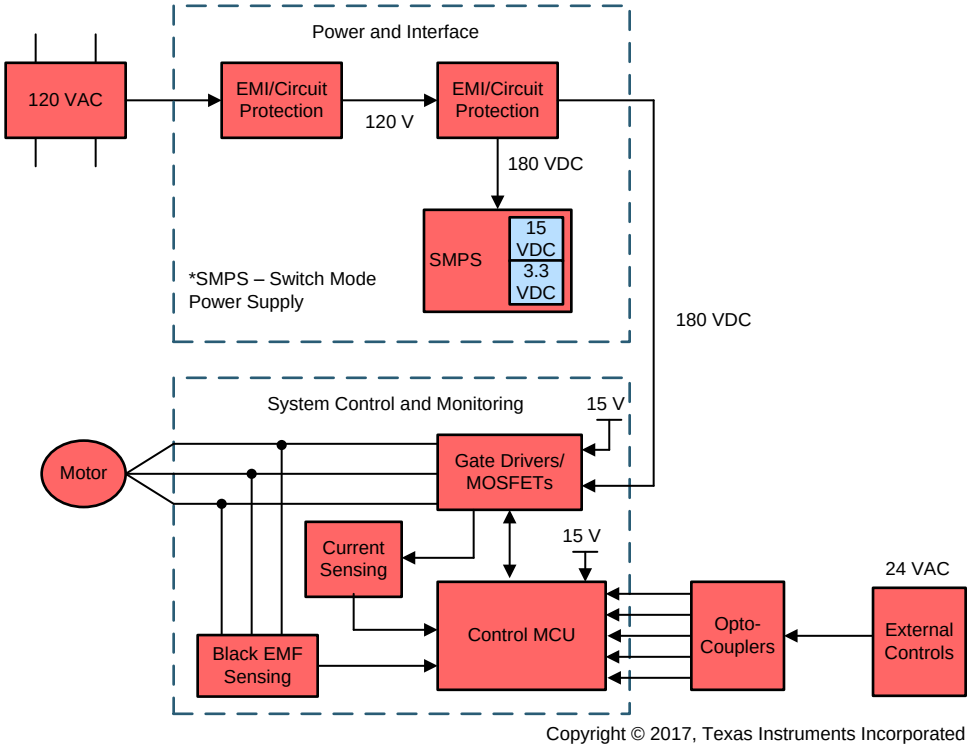


Figure 1. TIDA-01353 Block Diagram

1.4 Highlighted Products

The following subsections describe the key features for selecting the devices for this reference design. Find the complete details of the highlighted devices in their respective product datasheets.

1.4.1 MSP430F5132

The TI MSP430™ family of ultra-low-power MCUs consists of several devices featuring different sets of peripherals targeted for various applications. The architecture is combined with five low-power modes. The device features a powerful 16-bit reduced instruction set computing (RISC) CPU, 16-bit registers, and constant generators that contribute to the maximum code efficiency. The digitally controlled oscillator (DCO) allows the devices to wake up from low-power modes to active mode in less than 5 μs.

The MSP430F51x2 series are microcontroller configurations with two 16-bit high-resolution timers, two universal serial communication interfaces (USCIs) USCI_A0 and USCI_B0, a 32-bit hardware multiplier, a high-performance 10-bit 200-ksps analog-to-digital converter (ADC), an on-chip comparator, a three-channel direct memory access (DMA), 5-V tolerant I/Os, and up to 29 I/O pins. The timer event control module connects different timer modules to each other and routes the external signals to the timer modules. The device is capable of working up to a system frequency of 25 MHz. The operating temperature of the device is –40°C to 85°C. Figure 2 shows the functional block diagram of the MSP430F5132.

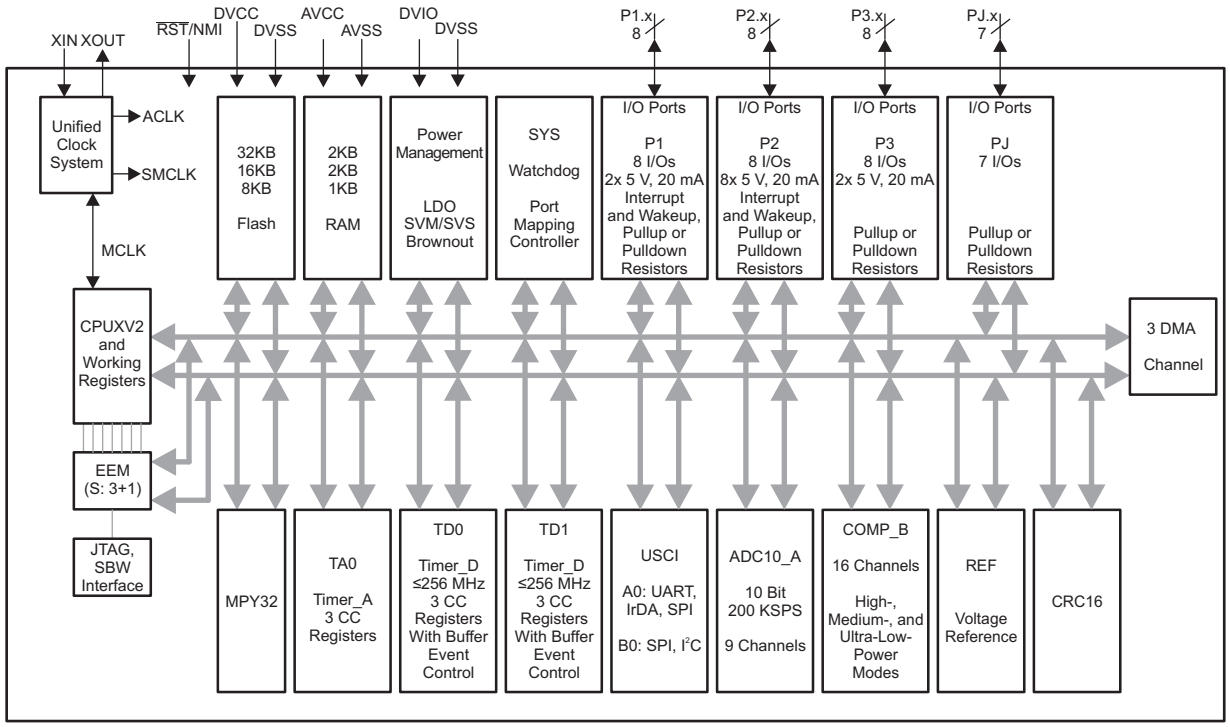


Figure 2. MSP430F5132 Functional Block Diagram

1.4.2 UCC27714

The UCC27714 is a 600-V, high-side, low-side gate driver with a 4-A source and 4-A sink current capability with the purpose of driving power MOSFETs. The device comprises one ground-referenced channel (LO) and one floating channel (HO). The HO is designed to operate with bootstrap supplies. The device features an excellent robustness and noise immunity with the capability to maintain operational logic at negative voltages of up to –8-V DC on the HS pin (at VDD = 12 V). The device features the industry best-in-class input propagation delays and delay matching between both channels with the purpose of minimizing pulse distortion in high-frequency switching applications. Each channel is controlled by its respective input pins (HI and LI), allowing full and independent flexibility to control the on and off state of the output.

The UCC27714 device output stage features a unique architecture on the pullup structure, which delivers the highest peak-source current when it is most required during the Miller plateau region of the power-switch turnon transition (when the power switch drain or collector voltage experiences dv/dt). The UCC27714 includes protection features at which point the outputs are held LOW when inputs are floating or when the minimum pulse-width specification of the input is not met. The driver inputs are complementary metal-oxide semiconductor (CMOS) compatible and transistor-transistor logic (TTL) compatible for easy interfacing with both digital power controllers and analog controllers.

The UCC27714 driver includes an enable and disable function to enable the output gate signals. The device accepts a bias supply with a wide input range from 10 to 20 V and offers undervoltage lockout (UVLO) protection for both the VCC and HB bias supply pins. The UCC27714 is available in an SOIC-14 package and rated to operate from –40°C to 125°C. Figure 3 shows a typical setup using the UCC27714.

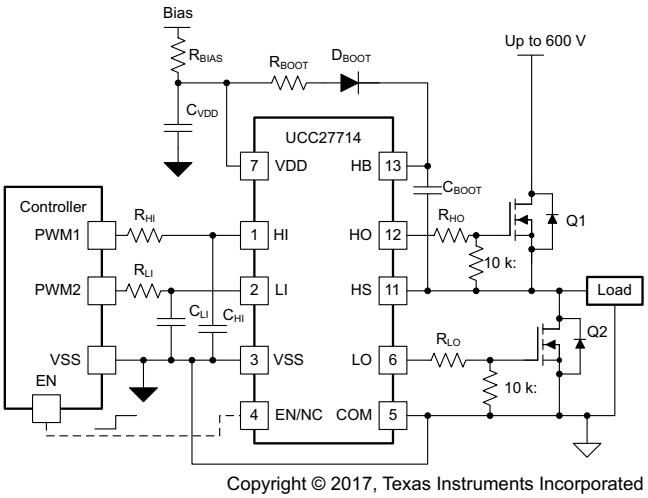


Figure 3. UCC27714 Application Schematic

1.4.3 TLV316

The TLV316 is a family of low-power, rail-to-rail input and output operational amplifiers. These devices operate from 1.8 to 5.5 V, are unity-gain stable, and are suitable for a wide range of general-purpose applications. The class AB output stage is capable of driving ≤10-kΩ loads connected to any point between V+ and ground. The input common-mode voltage range includes both rails and allows the TLVx316 to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications, and makes them suitable for driving sampling ADCs.

The TLV316 features a 10-MHz bandwidth and 6-V/μs slew rate with only a 400-μA supply current per channel, providing good AC performance at very-low power consumption. DC applications are well served with a very-low input noise voltage of 12 nV/√Hz at 1 kHz, low input bias current (5 pA), and an input offset voltage of 0.5 mV (typical).

1.4.4 UCC28881

The UCC28881 integrates a controller and a 700-V power MOSFET into one monolithic device. The device also integrates a high-voltage current source, enabling start up and operation directly from the rectified mains voltage. The UCC28881 is the same family device as the UCC28880 and it provides higher power handling capability.

The low-quiescent current of the device enables excellent efficiency. The device is suitable for non-isolated AC-to-DC low-side buck and buck-boost configurations with level-shifted direct feedback, but also more traditional high-side buck, buck-boost, and low-power flyback converters with low standby power can be built using a minimum number of external components.

The device generates its own internal low-voltage supply (5 V referenced to the device's ground, GND) from the integrated high-voltage current source. The PWM signal generation is based on a maximum constant on-time, minimum off-time concept, with the triggering of the on-pulse depending on the feedback voltage level. Each on-pulse is followed by a minimum off-time to ensure that the power MOSFET is not continuously driven in an on-state. The PWM signal is AND-gated with the signal from a current limit circuit. No internal clock is required, as the switching of the power MOSFET is load dependent. A special protection mechanism is included to avoid runaway of the inductor current when the converter operates with the output shorted or in other abnormal conditions that can lead to an uncontrolled increase of the inductor current. This special protection feature keeps the MOSFET current at a safe operating level. The device is also protected from other fault conditions with thermal shutdown, UVLO, and soft-start features.

Features:

- Integrated 14-Ω, 700-V power MOSFET
- Integrated high-voltage current source for internal device bias power
- Integrated current sense
- Internal soft start
- Self-biased switcher (start up and operation directly from rectified mains voltage)
- Supports buck, buck-boost and flyback topologies
- <100-μA device quiescent current
- Robust current protection during load short circuit
- Protection:
  - Current limit
  - Overload and output short circuit
  - Over temperature

Figure 4 shows the functional block diagram of the UCC28881.

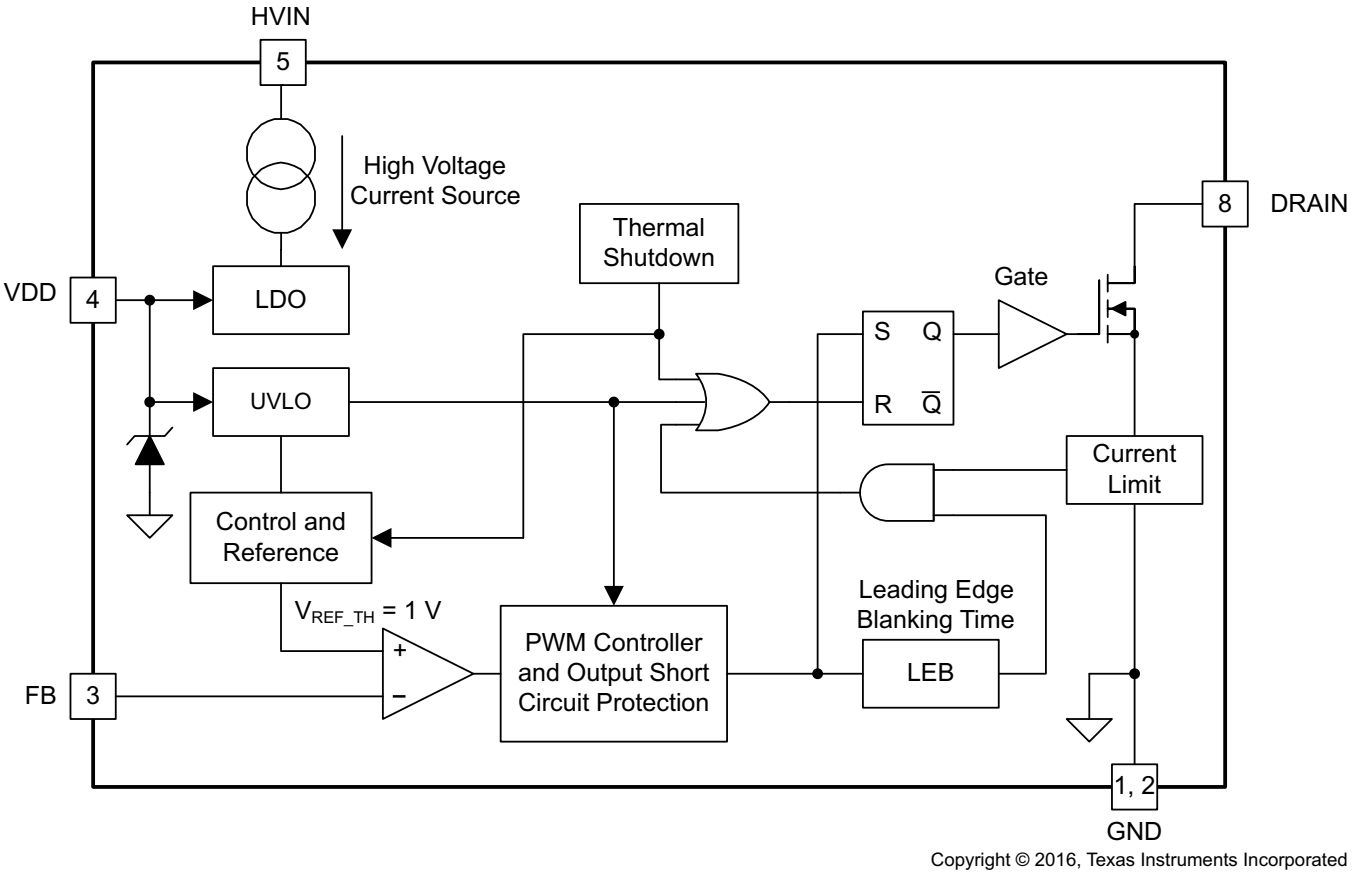


Figure 4. UCC28881 Functional Block Diagram

1.4.5 LP2985-33

The LP2985 family of fixed-output, low-dropout regulators offers exceptional, cost-effective performance for both portable and non-portable applications. Available in voltages of 1.8 V, 2.5 V, 2.8 V, 2.9 V, 3 V, 3.1 V, 3.3 V, 5 V, and 10 V, the family has an output tolerance of 1% for the A version (1.5% for the non-A version) and is capable of delivering a 150-mA continuous load current. The device includes standard regulator features such as overcurrent and over-temperature protection.

Features:

- Output tolerance:
  - 1% (A Grade)
  - 1.5% (Standard Grade)
- Ultra-low dropout, typically:
  - 280 mV at full load of 150 mA
  - 7 mV at 1 mA
- Wide V_{IN} range: 16 V max
- Low I_Q: 850 μA at full load at 150 mA
- Shutdown current: 0.01 μA typ
- Low noise: 30 μV_{RMS} with 10-nF bypass capacitor
- Stable with low-ESR capacitors, including ceramic
- Overcurrent and thermal protection
- High peak-current capability
- ESD protection exceeds JESD 22:
  - 2000-V human-body model (A114-A)
  - 200-V machine model (A115-A)

1.4.6 LMT84

The LMT84/LMT84-Q1 are precision CMOS integrated-circuit temperature sensors with an analog output voltage that is linearly and inversely proportional to temperature. Its features make it suitable for many general temperature sensing applications. It can operate down to a 1.5-V supply with 5.4-μA power consumption, making it ideal for battery powered devices. Package options including a through-hole TO-92 package allows the LMT84 to be mounted onboard, off-board, to a heat sink, or on multiple unique locations in the same application. A class-AB output structure gives the LMT84/LMT84-Q1 strong output source and sink current capability that can directly drive up to 1.1-nF capacitive loads. This means it is well suited to drive an ADC sample-and-hold input with its transient load requirements. It has accuracy specified in the operating range of −50°C to 150°C. The accuracy, 3-lead package options, and other features also make the LMT84/LMT84-Q1 an alternative to thermistors.

Features:

- Low 1.5-V operation
- Very accurate: ±0.4°C typical
- Wide temperature range: –50°C to 150°C
- Low 5.4-μA quiescent current
- Average sensor gain: –5.5 mV/°C
- Output is short-circuit protected
- Push-pull output with ±50-μA drive capability

1.4.7 TPD1E10B06

The TPD1E10B06 device is a single-channel electrostatic discharge (ESD) transient voltage suppression (TVS) diode in a small 0402 package. This TVS protection product offers ±30-kV contact ESD, ±30-kV IEC air-gap protection, and has an ESD clamp circuit with a back-to-back TVS diode for bipolar or bidirectional signal support. The 12-pF line capacitance of this ESD protection diode is suitable for a wide range of applications supporting data rates up to 400 Mbps. The 0402 package is an industry standard and is convenient for component placement in space-saving applications. The TPD1E10B06 devices are characterized for operation over a temperature range of –40°C to 125°C.

1.4.8 InstaSPIN-BLDC Solution

Targeted at low-cost BLDC applications, InstaSPIN-BLDC is a sensorless control technique based on the premise that "simple is better". In field tests with over 50 different motor types, InstaSPIN-BLDC was able to get each motor up and running in less than 20 seconds. The InstaSPIN-BLDC does not require any knowledge about motor parameters to work and only needs to adjust a single tuning value.

Unlike other sensorless BLDC control techniques based on BEMF zero-cross timing, InstaSPIN-BLDC monitors the motor's flux to determine when to commutate the motor. With the help of a free GUI (see Figure 5), the user can watch the flux signal in a plot window and set the "Flux Threshold" slider to specify at what flux level the motor should be commutated. Optimal commutation can be verified by observing the phase voltage and current waveforms, which are also displayed.

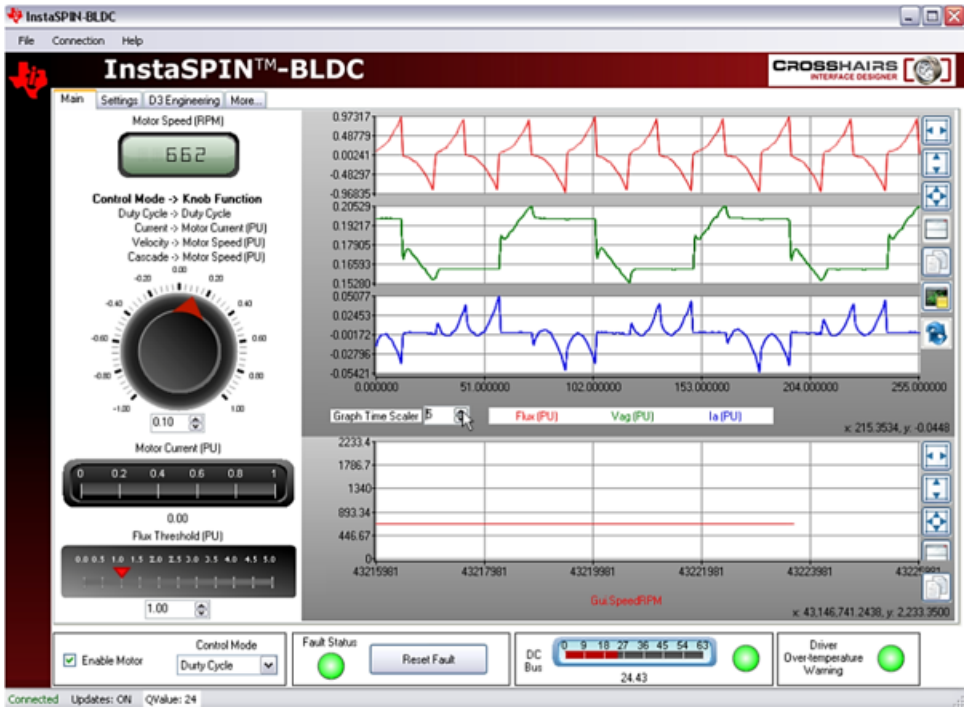


Figure 5. InstaSPIN-BLDC Graphical Interface

In addition to its ability to work with just about any BLDC motor, InstaSPIN-BLDC has demonstrated incredible resilience to speed transient perturbations. With zero-cross timing, the user is always using *past* information to predict *future* commutation events. However, InstaSPIN-BLDC monitors a real-time flux waveform to determine the appropriate time to commutate. Abrupt speed changes will be reflected in the flux waveform in real time, so it will still cross the specified threshold value at exactly the right time to commutate.

Using flux for commutation versus BEMF zero-cross timing also enables more stable operation at lower speeds. Unlike the flux signal, the BEMF signal amplitude diminishes at lower speeds, resulting in poor signal-to-noise performance. InstaSPIN-BLDC enables smoother operation at low speeds and provides more reliable motor starting, even under heavy loads.

1.5 System Design Theory

The following sections outline the design theory for the selection and implementation of devices into the TIDA-01353.

1.5.1 115-V AC Rectification and EMI Protected Circuit Design Theory

The AC-DC power stage is shown in Figure 6. The connection port is set up identical to the ECM motor controller port for ease of testing. The common is the output port for the control signal 24-V AC inputs. The other input/output ports are for the hot, neutral, and earth ground connections.

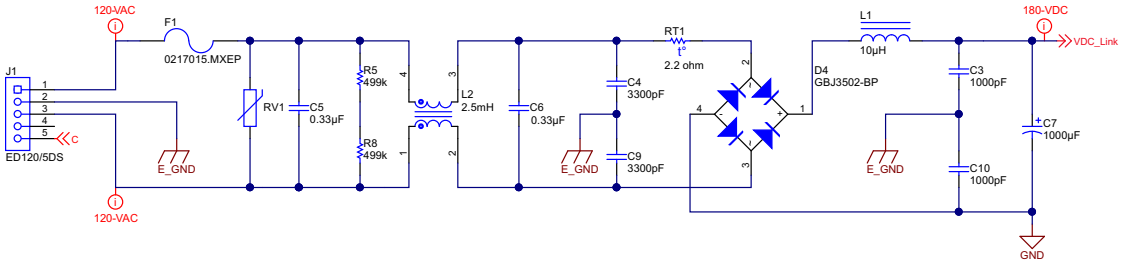


Figure 6. TIDA-01353 Rectification and EMI Protection Circuit

This TI Design also incorporates a 15-A 250-V AC rated fuse to prevent damage to the board in case of overcurrent. The RV1 metal oxide varistor (MOV), rated for 275-V_{RMS}, is also used for surge protection. Both 499-kΩ resistors are used as the discharge resistive network for capacitors C5 and C6, and are rated for 400 V. The rectification bridge is rated for 200 V at 35 A, leaving plenty of room for a sufficient safety factor. L2 is a common-mode filter. To limit the inrush current of the bulk DC capacitors, an inrush current limiter RT1 is provided. D4 is the full bridge rectifier. L1 is the DC choke provided for meeting the line harmonic standard. C7 is the electrolytic capacitor at the DC bus.

The AC-DC subsection of the design has been designed with the DC bus capacitor and necessary filters for conducted emission, surge, and EFT protection as per the standard EN55014. Figure 7 shows the simulation output of the design using the listed circuit parameters.

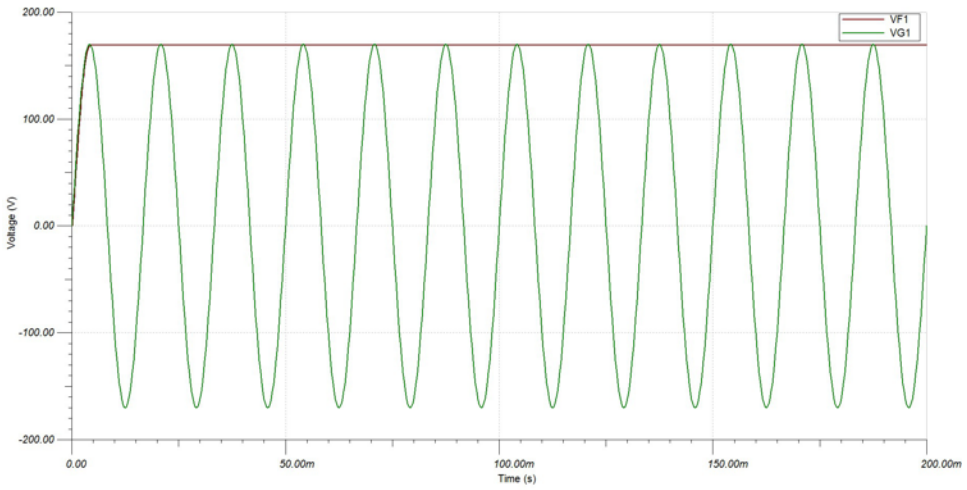


Figure 7. Rectification and EMI Protection Circuit Simulation Output

To reduce the voltage ripple of the DC output, calculate the bulk capacitor or DC link capacitor value. This helps ensure that a sufficient hold up time is provided, during which the regulated supply continues to provide the regulated voltage output in the event of a short lapse in AC voltage supply. The following arithmetic is used to properly fit the circuit with an appropriately sized DC bus capacitor.

The input voltage to this system is rated at 115-V AC at 60 Hz. For a DC ripple of 10%, the peak-to-peak DC voltage ripple is:

$$\Delta V_{DC} = \left(115 \times \sqrt{2}\right) \times 0.10 = 16.3 \text{ V} \quad (1)$$

This gives a maximum DC bus voltage of 178.9 V and a minimum of 146.3 V. The discharge time of the capacitor can be calculated by setting the instantaneous AC input voltage equal to the minimum value of the DC bus voltage ripple, as Equation 2 shows.

$$V_m \sin\theta = 146.3 \quad (2)$$

where V_m is the amplitude of the input voltage as shown in Figure 8.

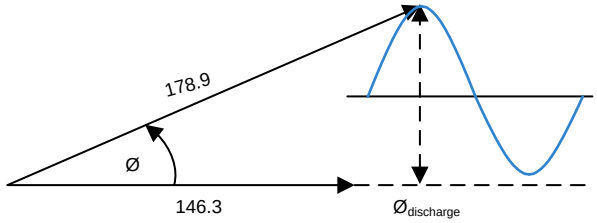


Figure 8. Capacitor Discharge Plot

Substituting V_m = 178.9 in Equation 1 results in 178.9 sin θ = 146.3, which leads to θ = 0.9575 radians. Therefore, the total electrical angle during the capacitor discharging period is:

$$\theta_{discharge} = \frac{\pi}{2} + 0.9575 = 2.5283 \text{ rad}$$

The electrical angle can be expressed in terms of the angular electrical frequency (ω) and time (t) as Equation 3 shows:

$$\theta = \varpi t \quad (3)$$

where ω can be expressed in electrical frequency as:

$$\varpi = 2\pi f \quad (4)$$

For a 60-Hz AC supply, ω = 2π × 60 = 376.99 rad/s; therefore, the discharge time of the capacitor is:

$$t_{discharge} = \frac{\theta_{discharge}}{\varpi} = 6.71 \text{ ms} \quad (5)$$

The average DC bus voltage is:

$$V_{DC\_ACVG} = 178.9 - \frac{\Delta V_{DC}}{2} = 170.75 \text{ V}$$

By taking the power consumption of the motor to be:

$$HP_{Rated} \times \frac{\text{Watts}}{HP_{Rated}} \quad (6)$$

where the rated horsepower of the motor is ½ hp and the ratio of watts per horsepower is 745.7 W for every 1 horsepower. Calculate the power required for the motor as:

$$\frac{1}{2} \times 745.7 = 372.85 \text{ Watts}$$

The average DC link current at 373 W is:

$$I_{DC} = \frac{P_{DC}}{V_{DC\_AVG}} = \frac{373 \text{ Watts}}{170.75} = 2.19 \text{ A} \quad (7)$$

Therefore, the required capacitance value C can be calculated by:

$$C \geq I_{DC} \times \frac{\Delta t}{\Delta V_{DC}} \quad (8)$$

where $\Delta t = t_{discharge} = 6.71$ ms. By substituting the values of I_{DC}, Δt, and ΔV_{DC} in Equation 8, the user can obtain the value for the required DC bus capacitor:
$C \geq 902\ \mu F$

In this TI Design, a 1000-µF electrolytic capacitor is used as the DC bus capacitor, rated for a maximum current ripple of 2.8 A.

1.5.2 Low-Voltage Supply Design Theory

In order to provide a suitable voltage level with sufficient current to the low-voltage components of this reference design, the UCC28881 and TPS7A4201 are used to create the 15-V and 3.3-V power supplies, respectively. The following sections outline the design theory used for the TIDA-01353 design.

1.5.2.1 UCC28881 Design Theory

In this TI Design, the UCC28881 is used to reduce the voltage from the DC bus to 15 V for the gate driver and inverter gate voltages. The design specifications are shown in Table 2.

Table 2. Buck Converter Design Parameters

DESCRIPTION	MIN	NOM	MAX	UNITS
V_{IN}	146.3	—	178.9	V
V_{OUT}	14.25	15	15.75	V
I_{OUT}	0.045	0.05	0.055	A
η	70%	85%	100%	—

1.5.2.1.1 Regulator Capacitor Selection

Capacitor C_{VDD} acts as the decoupling capacitor and storage capacitor for the internal regulator. A 100-nF, 400-V rated ceramic capacitor is enough for proper operation of the device's internal LDO.

1.5.2.1.2 Output Capacitor Selection

The value of the output capacitor impacts the output ripple, depending on the combination of the capacitor value and equivalent series resistor (R_{ESR}). A larger capacitor value also has an impact on the start-up time. For a typical application, the capacitor value can start from 47 µF to hundreds of µF. A guide for sizing the capacitor value can be calculated using the following equations:

$$C_L > 20 \times \frac{I_{LIMIT} - I_{OUT}}{f_{sw(max)} \times \Delta V_{OUT}} \quad (9)$$

$$R_{ESR} < \frac{\Delta V_{OUT}}{I_{LIMIT}} \quad (10)$$

Note that both C_L and R_{ESR} contribute to output voltage ripple. A first pass capacitance value can be selected and the contribution of C_L and R_{ESR} to the output voltage ripple can be evaluated. If the total ripple is too high, the capacitance value has to increase or R_{ESR} value must be reduced. The formula that calculates C_L is based on the assumption that the converter operates in burst of 20 switching cycles. The number of bursts per cycle could be different; the formula for C_L is a first approximation.

1.5.2.1.3 Pre-Load Resistor Selection

The pre-load resistor connected at the output is required for the high-side buck topology. Unlike low-side buck topology, the output voltage is directly sensed, in high-side buck topology the output is sampled and estimated. At no-load condition, because the feedback loop runs with its own time constant, the buck converter operates with a fixed minimum switching frequency. Select the pre-load resistor or using a Zener diode to prevent output voltage goes too high at no-load condition.

A simple Zener diode would be a good choice without going through the calculation. Besides the simplifying the calculation, the Zener diode does not consumes power at heavy load condition, which helps to improve the converter heavy-load efficiency.

A simple resistor can also be used to limit the output voltage at no load condition. However, this resistor connects to the output all the time and it reduces the full-load efficiency. The pre-load resistor can be calculated based on Equation 11 or based on experiments. In this equation, the V_{MAX} is allowed maximum output voltage and V_{REG} is the regulated output voltage.

$$R_L = \frac{4 \times V_{MAX}^2 \times (V_{MAX} - V_{REG})}{V_{MAX} + V_{REG}} \times \frac{C_{FB} \times (R_{FB1} + R_{FB1})}{L_1 \times I_{LIMIT}^2} \tag{11}$$

In this TI Design, the pre-load resistor is 15 kΩ with a power dissipation of 63 mW at the full rated load.

1.5.2.1.4 Inductor Selection

The following are the initial calculations used for the selection of the inductor used with the UCC2881.

Half of the peak-to-peak ripple current at full load is:

$$\Delta I_L = 2 \times (I_{Limit} - I_{OUT}) \tag{12}$$

When operating in DCM, the peak-to-peak current ripple is the peak current of the device. The average MOSFET conduction minimum duty cycle at continuous conduction mode (CCM) is:

$$D_{MIN} = \frac{V_{OUT} + V_D}{V_{IN(MAX)} - V_D} \tag{13}$$

If the converter operates in DCM:

$$D_{MIN} = 2 \times \frac{I_{OUT}}{I_{Limit}} \times \frac{V_{OUT} + V_D}{V_{IN(MAX)} - V_D} \tag{14}$$

The maximum allowed switching frequency at $V_{IN(max)}$ and full load is defined as:

$$F_{SW\_VIN(max)} = \frac{D_{MIN}}{t_{ON\_TO}} \tag{15}$$

where t_{ON_TO} is the inductor current runaway protection time threshold, at 450 ns. The switching frequency has a maximum value limit of $f_{SW(max)}$.

The worst case is I_{LIMIT} = 315 mA, but assuming ΔI_L = 530 mA, the converter works in DCM ($\Delta I_L > I_{LIMIT}$); therefore, based on V_{OUT} = 15 V, V_d = 0.5 V and $V_{IN(max)}$ = 180 V.

$$D_{MIN} = 2 \times \frac{0.05}{0.315} \times \frac{15 + 0.5}{180 - 0.5} = 2.74\%$$

The maximum allowed switching frequency is 61 kHz because the calculated value is below it.

$$F_{SW\_VIN(max)} = \frac{D_{MIN}}{t_{ON\_TO}} = 61\,kHz > f_{SW(max)} = 62\,kHz$$

The duty cycle does not force the MOSFET on time to go below t_{ON_TO}. If $D_{MIN}/T_{ON\_TO} < f_{SW(max)}$, the switching frequency is reduced by current runaway protection and the maximum average switching frequency is lower than $f_{SW(max)}$, the converter cannot support full load. The minimum inductance value satisfies both the following conditions:

$$L > \frac{V_{OUT} + V_d}{\Delta I_L \times F_{SW\_VIN(max)}} = 0.479\,mH \quad (16)$$

$$L > \frac{V_{IN(max)} + V_d}{I_{LIMIT}} \times t_{ON\_TO} = \frac{180.5\,V}{315\,mA} \times 450\,ns = 0.258\,mH \quad (17)$$

In this TI Design, 0.479 mH is selected as the minimum standard value that satisfies Equation 16 and Equation 17. The TIDA-01353 uses a 1.8-mH inductor, roughly four times the minimum required inductance.

1.5.2.1.5 Feedback Path and Load Resistor Selection

In low-side buck converter applications, the output voltage is always sensed by the FB pin and the UCC28881 internal controller can turn on the MOSFET on V_{OUT}. In high-side buck converter applications, the information on the output voltage value is stored on C_{FB} capacitor. This information is not updated in real time. The information on C_{FB} capacitor is updated just after the MOSFET turnoff event. When the MOSFET is turned off, the inductor current forces the freewheeling diode (D8 in Figure 9) to turn on and the GND pin of the UCC28881 goes negative at $-V_{d8}$ (where V_{d8} is the forward drop voltage of diode D8) with respect to the negative terminal of bulk capacitor . When D8 is on, through diode D7, the C_{FB} capacitor is charged at $V_{OUT} - V_{d4} + V_{d8}$. Set the output voltage regulation level using Equation 18.

$$\frac{R_{FB1}}{R_{FB2}} = \frac{V_{OUT(\tau)} - V_{d7} - V_{d8} - V_{FB\_TH}}{V_{FB\_TH}} \cong \frac{V_{OUT(\tau)} - V_{FB\_TH}}{V_{FB\_TH}} \quad (18)$$

where:

- V_{FB_TH} is the FB pin reference voltage
- V_{OUT_T} is the target output voltage
- R_{FB1}, R_{FB2} is the resistance of the resistor divider connected with FB pin (see Figure 9)
- The capacitor C_{FB} after D8 is discharged with a time constant that is $\tau_{FB} = C_{FB} \times (R_{FB1} + R_{FB2})$

Select the time constant τ_{FB}, given in Equation 19.

$$\tau_{FB} = V_{FB} \times (R_{FB1} + R_{FB2}) = 0.1 \times C_L \times R_{LOAD} \quad (19)$$

where R_{LOAD} is the full load resistor value.

The time constant selection leads to a slight output-voltage increase in no-load or light-load conditions. In order to reduce the output-voltage increase, increase τ_{FB}. The drawback of increasing τ_{FB} is t in high-load conditions V_{OUT} could drop.

Because of the nature of sample and hold of output voltage feedback, the feedback loop components need some adjustment after the initial design. The larger time constant of the feedback components leads to a lower no-load switching frequency. As the results, the no-load standby power and light-load voltage regulation are improved. Because of a larger time constant at a heavier load, the load regulation starts to get worse. On the contrast, decreasing the time constant makes the heavy load regulation better but increases the no-load standby power and makes the light-load voltage regulation worse. Some trade-off is required to make the regulation and standby power.

The complete buck converter configuration is shown along with simulation data representing the efficiency and power dissipation for three separate values. The efficiency is 85% at the full current output of 100 mA to the load. The power dissipation at the full load current is 275 mW for the buck converter.

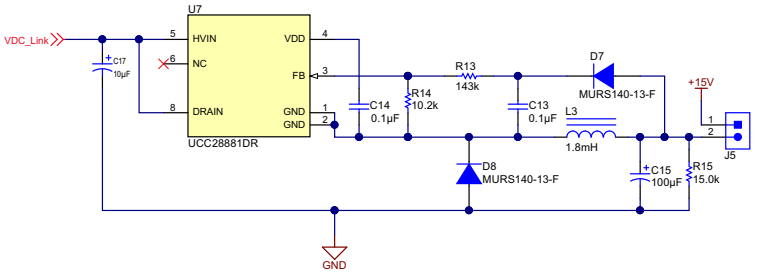


Figure 9. TIDA-01353 Buck Converter Configuration

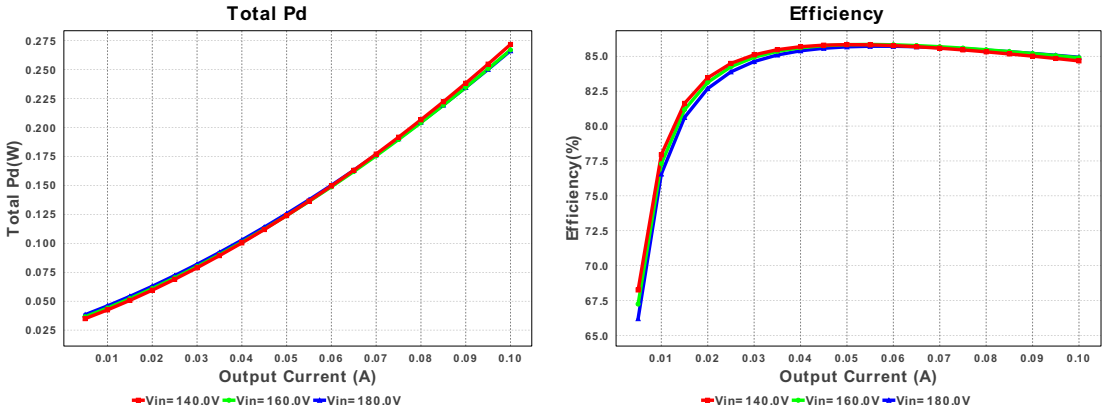


Figure 10. Buck Converter Simulation Output (Power Dissipation and Efficiency)

1.5.2.2 LP2985-33 Application and Design Theory

The LP2985-33 has a fixed output voltage of 3.3 V and the ability to deliver up to 150 mA. The typical application schematic for the device is shown in Figure 11.

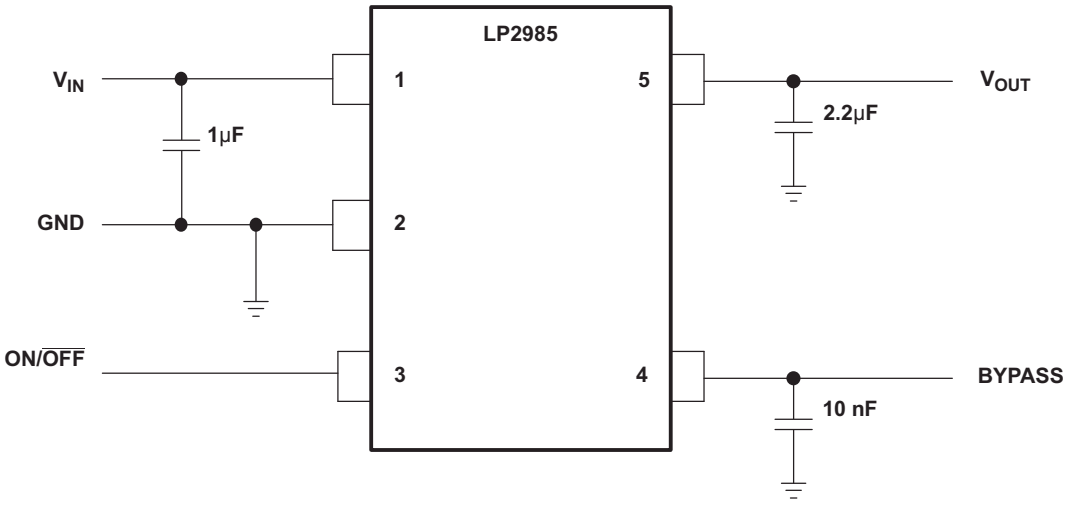


Figure 11. LP2985-33 Application Schematic

1.5.2.2.1 Input Capacitor Selection

A minimum value of 1 μF (over the entire operating temperature range) is required at the input of the LP2985. In addition, this input capacitor should be located within 1 cm of the input pin and connected to a clean analog ground. There are no equivalent series resistance (ESR) requirements for this capacitor, and the capacitance can be increased without limit.

1.5.2.2.2 Output Capacitor Selection

As an advantage over other regulators, the LP2985 permits the use of low-ESR capacitors at the output, including ceramic capacitors that can have an ESR as low as 5 mΩ. Tantalum and film capacitors also can be used if size and cost are not issues. The output capacitor also should be located within 1 cm of the output pin and be returned to a clean analog ground.

As with other PNP LDOs, stability conditions require the output capacitor to have a minimum capacitance and an ESR that falls within a certain range (minimum C_{OUT}: 2.2 μF; can be increased without limit to improve transient response stability margin).

It is critical that both the minimum capacitance and ESR requirement be met over the entire operating temperature range. Depending on the type of capacitors used, both these parameters can vary significantly with temperature.

1.5.2.2.3 Noise Bypass Capacitor Selection

The LP2985 allows for low-noise performance with the use of a bypass capacitor that is connected to the internal band-gap reference through the BYPASS pin. This high-impedance band-gap circuitry is biased in the microamp range and, thus, cannot be loaded significantly, otherwise, its output—and, correspondingly, the output of the regulator—changes. Thus, for best output accuracy, DC leakage current through C_{BYPASS} should be minimized as much as possible and never should exceed 100 nA.

A 10-nF capacitor is recommended for C_{BYPASS}. Ceramic and film capacitors are well suited for this purpose.

1.5.2.2.4 LDO Simulation Performance

For this LDO, the power dissipation is around 0.6 W at full-load conditions. Figure 12 shows the simulation data for the LM2985-33 from no load to full load.

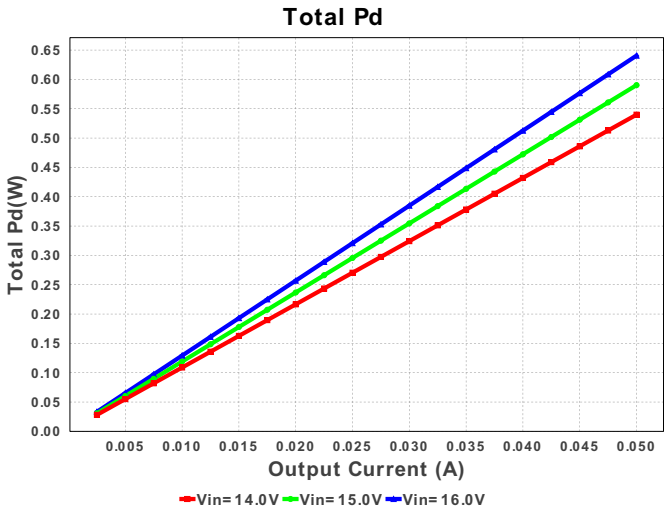


Figure 12. LP2985 Power Dissipation Simulation Results

Table 3 shows the values of some key parameters of the LDO simulation. The total power output is 165 mW with an output voltage ripple of 4.4 mV peak to peak.

Table 3. LDO Simulation Results

PARAMETER	VALUE	UNITS
P_{OUT}	165.0	W
Steady state efficiency	20.5%	—
$V_{OUT\ P-P}$	4.4	mV
V_{OUT} tolerance	4.0%	—

1.5.3 Gate Driver Design Theory

The UCC27714 is used in this TI Design to drive the MOSFETs of the motor controller. Typically with any logic based gate driver, the output PWM signal will be 3.3 V. The UCC27714 provides level shifting functionality to boost the 3.3-V signal to the specified gate-drive voltage in order to fully turn on the power device and reduce conduction loss.

Gate drivers effectively combine both the level-shifting and buffer-drive functions. Gate drivers also find other needs such as minimizing the effect of high-frequency switching noise by locating the high-current driver physically close to the power switch, driving gate-drive transformers and controlling floating power-device gates, reducing power dissipation and thermal stress in controllers by moving gate charge power losses from the controller into the driver.

Figure 13 shows a single instance of the device with properly parameterized passive component selection for this application. The methods for obtaining these values can be found in the following sections.

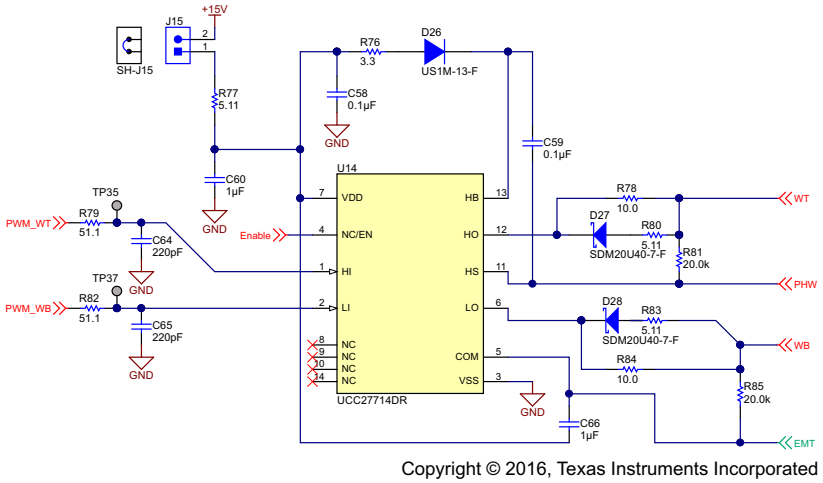


Figure 13. TIDA-01353 Application of UCC27714 Half-Bridge Gate Driver

1.5.3.1 HI and LI Low-Pass Filter Components

A RC filter must be added between PWM controller and input pin of the UCC27714 to filter the high frequency noise, namely R_{HI} / C_{HI} and R_{LI} / C_{LI}. From the UCC27714 datasheet, find the recommended value of the RC filter is:

$R_{HI} = R_{LI} = 51\ \Omega$

$C_{HI} = C_{LI} = 220$ pF

1.5.3.2 Boost Capacitor (C_{BOOT})

The boost capacitor should be sized to have more than enough energy to drive the gate of the MOSFET high, without depleting the boot capacitor more than 10%. A good rule of thumb is size C_{BOOT} to be at least 10 times; as large as the equivalent MOSFET gate capacitance (C_g). C_g will have to be calculated based on the voltage driving the high-side MOSFET's gate (V_{GS}) and knowing the MOSFET's gate charge (Q_g). V_{GS} is approximately the bias voltage supplied to V_{DD} less the forward voltage drop of the boost diode (V_{DBOOT}). In this TI Design, the estimated V_{GS} was 13.3 V.

The MOSFET used in this example had a specified Q_g of 25 nC.

$$V_{GS} \approx V_{DD} - V_{DBOOT} = 15\ V - 1.7\ V = 13.3\ V \tag{20}$$

Once C_g is estimated C_{BOOST} should be sized to be at least 10 times larger than C_g.

$$C_g = \frac{Q_g}{V_{GS}} = \frac{25\ ns}{13.3} \approx 1.9\ nF \tag{21}$$

$$C_{BOOST} \geq 10 \times C_g = 19\ nF \tag{22}$$

For this TI Design, a 100-nF capacitor was chosen for the boost capacitor.

$$C_{BOOST} = C_{59} = 100\ nF$$

1.5.3.3 V_{DD} Bypass or Holdup Capacitor and R_{Bias}

The VDD capacitor (C_{VDD}) should be chosen to be at least 10 times larger than C_{BOOST}. For this TI Design example, a 1-µF capacitor was selected. C53 is the V_{DD} capacitor.

$$C_{VDD} \geq 10 \times C_{BOOST} = 1\ \mu F$$

Under the condition when the output of the UCC27714 has no load and $V_{DD/HB-HS}$ ramps up quickly, the HO/LO has am error logic spike even HI/LI is in low condition. If the $V_{DD/HB-HS}$ ramp-up time from 0 to 15 V is less than 50 µs (or, if the ramp-up slew rate of $V_{DD/HB-HS}$ is larger than 300 V/ms), there is a risk of hitting this phenomenon. A 5-Ω resistor R_{bias} series with bias supply and V_{DD} pin is recommended to make the V_{DD} ramp up time larger than 50 µs. In Figure 13, the 5.11-Ω resistor is used as the R_{bias} resistor

1.5.3.4 Estimating Boost Diode Power Dissipation

Estimate boost diode power dissipation (P_{DBOOT}) based on switching frequency, diode forward voltage drop, and gate driver switching frequency (f_{SW}). For this example, the switching frequency is set to 10 kHz. The estimated power loss for the boost diode is given in Equation 23.

$$P_{DBOOT} = \frac{1}{2} Q_g \times f_{sw} \times V_{DBOOT} = \frac{1}{2} \times 25\ nC \times 10\ kHz \times 1.7\ V \approx 0.2\ mW \tag{23}$$

1.5.3.5 Boost Diode Current Limiting Resistor (R_{BOOT})

Resistor R_{BOOT} is selected to limit the current in D_{BOOT} and limit the ramp-up slew rate of voltage of HB-HS. It is recommended when using the UCC27714 that R_{BOOT} is between 2 and 10 Ω. For this TI Design, a current limiting resistor of 3.3 Ω is used. The peak boost diode current ($I_{DBOOTPK}$) is limited to roughly 4 A.

$$R_{BOOT} = 3.3\ \Omega$$

$$I_{DBOOT_{PK}} = \frac{VDD - V_{DBOOT}}{R_{BOOT}} = \frac{15\ V - 1.7\ V}{3.3\ \Omega} \approx 4.03\ A \tag{24}$$

1.5.3.6 Bootstrap Diode

The voltage seen by the bootstrap diode will be same as the full DC bus voltage (in this case around 165-V DC). The bootstrap diode voltage rating must be greater than the DC bus rail voltage. It must be a fast recovery diode to minimize the recovery charge and hence charge fed from the bootstrap capacitor to the 15-V VDD supply.

The diode should be able to carry a pulsed peak current of 4.03 A. However, the average current is much smaller and is dependent on the switching frequency and the gate charge requirement of the high-side MOSFET. This reference design uses a 1000-V, 1-A, fast recovery diode.

1.5.3.7 Gate Resistor R_{HO} and R_{LO}

The gate resistors are sized to reduce ringing caused by parasitic inductances and capacitances and also to limit the current coming out of the gate driver. From the UCC27714 datasheet:

- LO, HO output pulldown resistance: $R_{HOL} = R_{LOL} = 1.45\ \Omega$
- LO, HO output pullup resistance: $R_{HOH} = R_{LOH} = 3.75\Omega$

The reference design uses different gate resistors to turn on and turn off the MOSFET. The external gate resistors used are:

- The high-side turnon gate resistance, $R_{HO\_ON} = 10\ \Omega$
- The parallel combination of the resistors R78 and R80 form the turnoff equivalent resistance.
- The high-side turnoff gate resistance, $R_{HO\_OFF} = 3.38\ \Omega$ (10 Ω and 5.11 Ω in parallel).
- The low-side turnon gate resistance, $R_{LO\_ON} = 10\ \Omega$.
- The high-side turnon gate resistance, $R_{LO\_OFF} = 3.38\ \Omega$.

To calculate the maximum HO drive current (I_{HO_DR}):

$$I_{HO\_DR} = \frac{V_{DD} - V_{DBOOT}}{R_{HO\_ON} - R_{HOH}} = \frac{15\ V - 0.55\ V}{10\ \Omega + 3.75\ \Omega} \approx 1.05\ A \quad (25)$$

To calculate the maximum HO sink current (I_{HO_SK}):

$$I_{HO\_SK} = \frac{V_{DD} - V_{DBOOT}}{R_{HO\_OFF} - R_{HOL}} = \frac{15\ V - 0.55\ V}{3.38\ \Omega + 1.45\ \Omega} \approx 3\ A \quad (26)$$

To calculate the maximum LO drive current (I_{LO_DR}):

$$I_{LO\_DR} = \frac{V_{DD}}{R_{LO\_ON} - R_{LOH}} = \frac{15\ V}{10\ \Omega + 3.75\ \Omega} \approx 1.09\ A \quad (27)$$

To calculate the maximum LO sink current (I_{LO_SK}):

$$I_{LO\_SK} = \frac{V_{DD}}{R_{LO\_OFF} - R_{LOL}} = \frac{15\ V}{3.38\ \Omega + 1.45\ \Omega} \approx 3\ A \quad (28)$$

1.5.3.8 Estimating UCC27714 Power Losses

Power dissipation of the gate driver has two portions as shown in Equation 29:

$$P = P_{DC} + P_{SW} \tag{29}$$

The static power dissipation due to quiescent current is calculated as:

$$P_{QC} = \left(I_{QDD} + I_{QBS}\right) \times V_{DD} \tag{30}$$

where I_{QDD} is the quiescent current for the driver.

The quiescent current is the current consumed by the device to bias all internal circuits such as the input stage, reference voltage, logic circuits, protection circuits, and any current associated with switching of internal devices when the driver output changes state (such as charging and discharging of parasitic capacitances, parasitic shoot-through). The UCC27714 features very low quiescent currents (less than 1.1 mA). In practice, this is the power consumed by driver when its output is disconnected from the gate of power switch.

The power dissipated in the gate driver package during switching (PSW) depends on the following factors:

- Gate charge required of the power device (usually a function of the drive voltage V_G, which is very close to input bias supply voltage VDD due to low V_{OH} drop-out)
- Switching frequency
- Use of external gate resistors

To turn on a MOSFET, the sufficient gate charge must be provided by the gate driver. The energy required to supply the gate charge is calculated as:

$$E_G = \frac{Q_G \times V_{GS}}{2}$$

where V_{GS} is the gate voltage supplied by the gate driver across the gate and source of the MOSFET.

If the MOSFET is switching at a frequency $f_{SW,}$ then the gate power supplied by the gate driving during the turnon of the MOSFET is calculated as:

$$P_{G(on)} = \frac{Q_G \times V_{GS} \times f_{SW}}{2} \tag{31}$$

The same energy is dissipated when the MOSFET turns off as well. Therefore, the total gate power required to turn on and off one MOSFET is:

$$P_G = Q_G \times V_{GS} \times f_{SW} \tag{32}$$

In BLDC trapezoidal control, only the upper MOSFET is switched using PWM. The lower MOSFET is continuously ON for 120° electrical. Both upper and lower MOSFETs are ON only for one third of the electrical cycle. Therefore, the gate power required for the upper MOSFET is:

$$P_{GH} = \frac{Q_G \times V_{GS} \times f_{SW}}{3} \tag{33}$$

The gate power required for the lower MOSFET can be calculated based on the electrical frequency of the inverter output voltage and current. The electrical frequency of the motor winding voltage at 1050 RPM for a 6-pole motor is approximately 53 Hz. The lower MOSFET is switched ON and OFF once in every electrical frequency.

$$P_{GL} = Q_G \times V_{GS} \times f_{ele}$$

The total power loss in a single UCC27714 device is:

$$P_{UCC27714} \approx \left(V_{DD} \times I_{QDD} + I_{QBS}\right) + \left(\frac{1}{3} \times Q_G \times V_{GS} \times f_{SW}\right) + \left(Q_G \times V_{GS} \times f_{ele}\right) \tag{34}$$

which yields a loss of 16 mW per IC. This TI Design uses three separate instances of the UCC27714, making the total gate drive power loss 47 mW.

1.5.4 Inverter Design Theory

The inverter in this design is used to spin the BLDC motor through six transistors and the rectified input voltage from the DC bus. The output of these three lines goes directly to the motor through the J16 terminal block. The inverter section must be capable of withstanding the DC bus voltage calculated in previous sections, roughly 180-V DC; high-voltage capacity transistors are therefore required in this inverter design.

The layout and minimization of trace length with respect to the power section is critical to reduce the switching voltage spikes across the MOSFETs. Furthermore, placing local decoupling capacitors close to each leg of the inverter can minimize the voltage spikes as well. C61, C62, and C63 are provided for decoupling and are placed very close to each leg of the inverter.

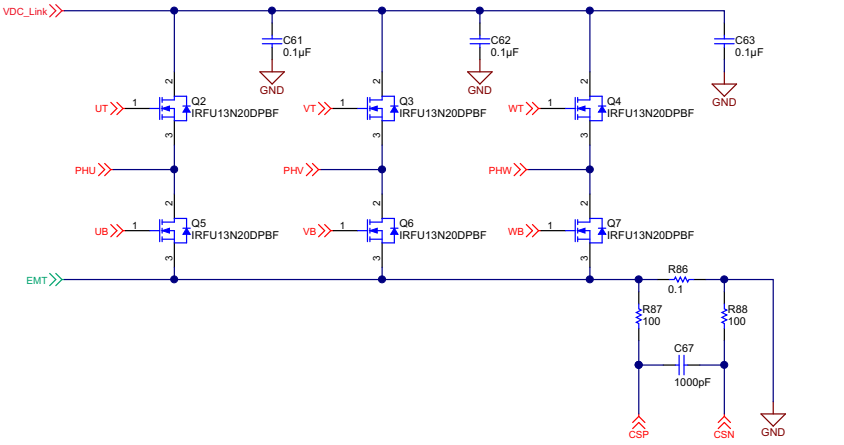


Figure 14. Inverter MOSFET Schematic

For the design's inverter design, there is a choice between power MOSFETs and insulated-gate bipolar transistors (IGBT). For this application, the MOSFET is used due to the output switching characteristics, conduction characteristics, and voltage controllability. These devices have the advantage with respect to ease of control. These devices are suitable for switching frequencies above 20 kHz, as well as for applications involving moderate voltage levels, that is 200 V.

For each of the six MOSFETs shown in Figure 14, the gate voltage is provided by the HI and LO gate driver outputs of the UCC27714. The voltage applied to each gate is 15 V with a current output limited at 4 A. These particular transistors have a source-to-drain voltage rating of 200 V and a maximum ID of 13 A. The static drain-to-source on-resistance $R_{DS(on)}$ is rated at 0.235 Ω.

1.5.5 Heat Sink Temperature Sensor Circuit

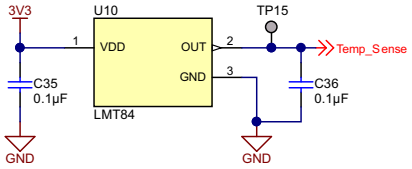


Figure 15. TIDA-01353 Application of LMT84

The LMT84 is used in this TI Design to monitor the heat sinks of the inverter transistors. This data is fed into an ADC port of the MSP430 for comparison. The capacitors are used to reduce noise coupling. A series output resistor can be added for capacitive loads greater than 1100 pF. Table 4 shows the recommended resistance value for three separate capacitance ranges. In this particular case, the input capacitance of the ADC pin of the MSP430F5132 is 3.5 pF, well below the load limit.

Table 4. LMT84 RS Requirement for Capacitive Loads

C_{LOAD}	MINIMUM R_S
1.1 to 99 nF	3 kΩ
100 to 999 nF	1.5 kΩ
1 µF	800 Ω

The voltage and ADC digital output readings are converted to a temperature value in Celsius using Equation 35:

$$\text{Temperature}\left(^{\circ}\text{C}\right) = \frac{5.506 - \sqrt{\left(-5.506\right)^2 + 4 \times 0.00176 \times \left(870.6 - V_{TEMP}\left(\text{mV}\right)\right)}}{2 \times \left(0.00176\right)} + 30 \quad (35)$$

where the V_{TEMP} is the value in millivolts obtained from the ADC. This parabolic equation is an approximation of the transfer table listed in the LMT84 datasheet and the accuracy of the equation degrades slightly at the temperature range extremes.

The MSP430F5132 has a 10-bit ADC, therefore the voltage gain per LSB is approximated as:

$$\frac{3.3\ \text{V} - 0\ \text{V}}{1024} = 3.22\ \frac{\text{mV}}{\text{LSB}}$$

This value can be multiplied by the LSB value from the ADC to find the value of V_{TEMP} in Equation 35. Note that the LSB values acquired from the LMT84 output are inversely proportional to the sensed temperatures they represent.

Due to the intrinsic behavior of an NMOS/PMOS rail-to-rail buffer, a slight shift in the output can occur when the supply voltage is ramped over the operating range of the device. The location of the shift is determined by the relative levels of V_{DD} and V_{OUT}. The shift typically occurs when $V_{DD} - V_{OUT} = 1.0$ V. This slight shift (a few millivolts) takes place over a wide change (approximately 200 mV) in V_{DD} or V_{OUT}. Because the shift takes place over a wide temperature change of 5°C to 20°C, V_{OUT} is always monotonic.

1.5.6 Motor Voltage Feedback Circuit Design Theory

For the sensorless motor control, the voltage of each leg of the inverter needs to be fed into the MSP430. The firmware can then measure the motor phase voltage directly instead of estimating the value. The firmware works on the back electro-motive force (BEMF) integration technique. The algorithm derives the motor BEMF by sensing the winding voltages of the non-energized phase. The measured winding voltage overrides on half of the DC bus voltage (V_{DC} / 2) during the PWM ON time of the energized phases. Therefore, the BEMF is derived by subtracting (V_{DC} / 2) from the sensed winding voltages. The algorithm assumes the same scaling in the winding voltage and DC bus voltage (V_{DC}) sensing network. Therefore, it is important to maintain the exact same scaling configuration for the BEMF voltage-sensing circuits and V_{DC} sensing circuit.

Each motor leg has a maximum voltage value equal to the DC bus voltage, about 180-V DC. The MSP430F5132 can accept voltage levels up to 3.3 V on any ADC pin; therefore, the voltage must be reduced to an acceptable working level. This is done through the use of a voltage divider network, which incrementally brings the voltage down to a safe operating range for the MSP430, as shown in Figure 16.

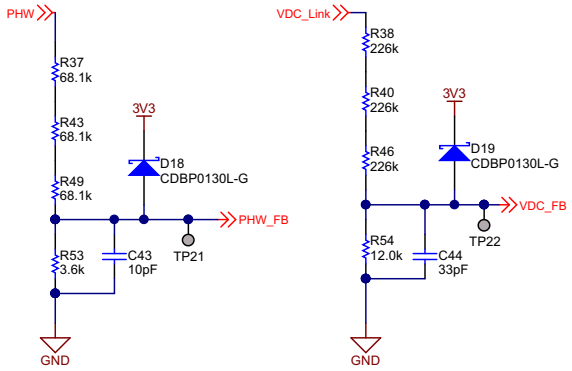


Figure 16. TIDA-01353 Voltage Sensing Schematic

The maximum voltage seen at the MCU is:

$$\text{PHW} \times \left(\frac{3.6\,\text{k}\Omega}{3.6\,\text{k}\Omega + 68.1\,\text{k}\Omega + 68.1\,\text{k}\Omega + 68.1\,\text{k}\Omega} \right) \tag{36}$$

Substituting the maximum voltage for PHW, 178.9-V DC, the output voltage is calculated as 3.098 V at its highest value. For an additional safety factor, a protection clamp diode is integrated into the design. The remaining two legs of the motor output are identical with respect to the calculated values. For the VDC input, the resistor values are slightly higher, allowing a 3.130-V signal input to the ADC. These resistor values are increased in value in order to reduce the standby current of VDC when the motor is not operating.

1.5.7 MSP430F5132 MCU Integration

Figure 17 shows the schematic for configuring the MSP430F5132 MCU. The MSP430 MCU generates a core supply voltage, which is internally regulated and denoted as VCORE. A suitable decoupling capacitor must be connected to the VCORE pin. The datasheet recommends using a decoupling capacitor with a value of 470 nF (SLAS619). A capacitor tolerance of ±20% or better is required. The VCORE pin is only for internal device usage. Do not apply any external DC load or voltage to this pin.

The datasheet specifies a capacitor ratio of 10 between the DVCC (digital power supply) and VCORE pins. TI recommends using a 4.7-µF capacitor (minimum) at the DVCC pin. The TIDA-01353 reference design uses a 10-µF capacitor at the DVCC pin. A 0.1-µF capacitor has been added to obtain the best performance at a high frequency. The same 10- and 0.1-µF decoupling capacitors are provided at the digital IO power supply pin (DVIO) and analog power supply pin (AVCC).

The Timer_D of the MCU is used for PWM generation. The TD1.0 instance of the MCU and the corresponding pins are mapped to the high-side switch PWM. The TIDA-01353 reference design uses unipolar, trapezoidal BLDC control with only the high-side switches switching at a high frequency. The low-side switches switch at the electrical frequency of the motor current, which is much lower. Gate control of the lower MOSFETs is possible using the general purpose input and output (GPIO) pins of the MCU. All of the feedback voltages including the DC bus voltage, three winding voltages, current sense amplifier output, and temperature sensor output are interfaced to the 10-bit successive approximation (SAR) ADC channels of the MCU.

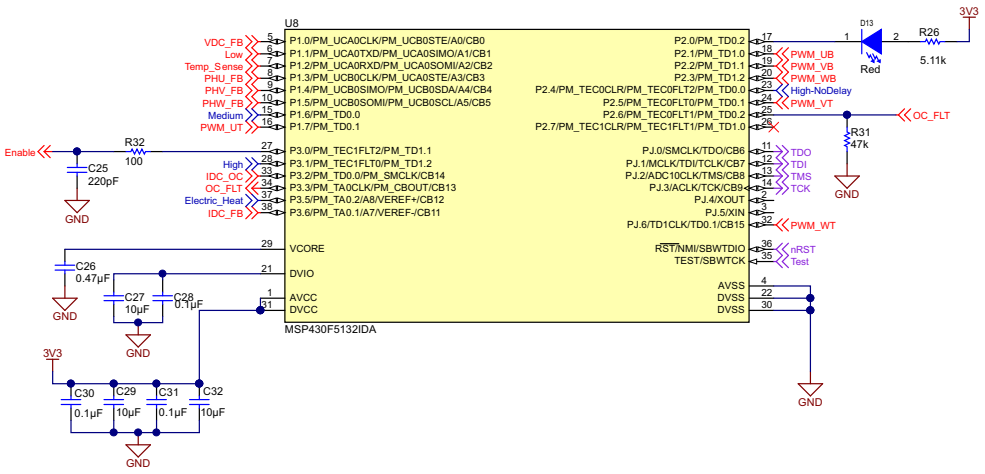


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Figure 17. MSP430F5132 Setup Schematic

1.5.7.1 Overcurrent Protection With MSP430F5132

The comparator_B (Comp_B) is an analog voltage comparator and features the following:

- Inverting and non-inverting terminal input multiplexer
- Software-selectable RC filter for the comparator output
- Interrupt capability
- Selectable reference voltage generator, voltage hysteresis generator
- Ultra-low-power comparator mode

The comparator compares the analog voltages at the non-inverting (+) and inverting (–) input terminals. If the non-inverting terminal is more positive than the inverting terminal, the comparator output CBOUT is high. The comparator can be switched ON or OFF using the control bit CBON. The output of the comparator can be used with or without internal filtering. When the control bit CBF is set, the output is filtered with an on-chip RC filter. The delay of the filter can be adjusted in four different steps. Selecting the output filter can reduce errors associated with comparator oscillation. The comparator features a high-precision reference voltage level, low offset voltage, and high speed. The CBRSEL (reference select) bit in the CBCTL2 register can be configured to obtain different thresholds. The reference voltages available are 1.5 V, 2.0 V, and 2.5 V.

1.5.7.2 Timer Event Control Module

The Timer Event Control (TEC) module is the interface between the timer modules and the external events. The TEC and Timer_D modules are connected through internal signals. The TEC module contains the control registers to configure the routing between the timer modules. The TEC module also has the enable register bits, interrupt enable, and interrupt flags for external event inputs.

The TEC module features include:

- Enabling of internal and external clear signals
- Routing of internal signals (between Timer_D instances) and external clear signals
- Support of external fault input signals
- Interrupt vector generation of external fault and clear signals
- Generating feedback signals to the timer capture and compare channels to affect the timer outputs

In the TIDA-01353 reference design, the COMPB module and TEC module are used together for current limit operation. The output of the current sense amplifier is connected to the non-inverting terminal of the comparator through the input channel 14 (CB14), as Figure 17 shows. The inverting input of the comparator is internally connected to the programmable voltage reference. The output of the comparator CBOUT is externally routed to the external fault event pin TECxFLT1 of the TEC module. Whenever the current sense amplifier output exceeds the voltage reference of the comparator, the output CBOUT and TECxFLT1 goes high, which initiates an event in the TEC module. The TEC module is programmed to disable the Timer_D output PWM during this event. This programmed function means that CBOUT goes high when the motor hits an overcurrent condition and can disable the Timer_D output (as Figure 18 shows) if CBOUT is connected to a TECxFLT input pin. When CBOUT goes low, the Timer_D output is then allowed to resume normal operation.

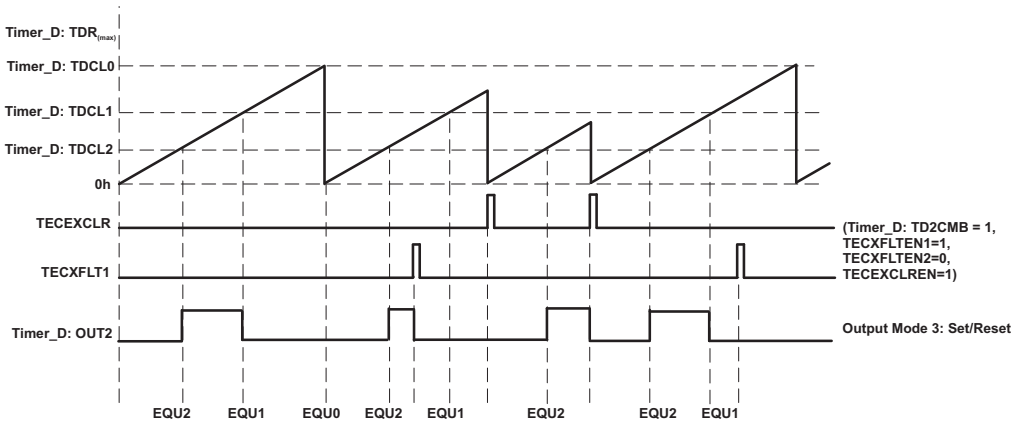

Figure 18. MSP430F5132 Timer D Diagram

1.5.8 Current Sense Amplifier Design Theory

Current sensing and amplification are used for two main purposes in this TI Design. First, the current sensing is sent into the ADC input of the MSP430 to execute any current or torque control algorithms. Second, the current sensing is sent to the MSP430's onboard comparator module for cycle-by-cycle current limiting. In order to select the right current sensing resistor and op-amp gain, the maximum current at the lower leg of the inverter must be calculated. The peak current is calculated as:

$$I_{Peak} = I_{RMS} \times \sqrt{2} \times I_{Ripple} \tag{37}$$

Substituting in the values of the motor used in this TI Design:

- I_{RMS}= 6.5 A
- I_{Ripple} = IRMS ±10%

This yields a peak current at 10.08 A for the inverter current sensing resistor. Now that the maximum current peak that will be seen by the shunt resistor has been calculated, the appropriate gain of the amplifier can be calculated along with the resistor values needed to achieve this gain.

The maximum current seen is be around 10 A, but if the current swings to the opposite polarity, it can cause issues with the sense amplifier. When this negative current induces a negative voltage on the op amp, there is a recovery delay. This charge accumulation requires time to dissipate before the amplifier will function correctly again. In order to account for this event, the voltage levels are shifted up to prevent the voltage from going negative.

In this application, the differential amplifier is used with an added voltage reference value that will bias the current reference input signal to a higher voltage, while also providing amplification. The target conditions are:

- V_{OUT} = 2.5 V when the current is at 10 A
- V_{OUT} = 0.1 V when the current is at –(10 A)

To find the slope of this voltage shift, Equation 38 can be set up with the given values:

$$\begin{pmatrix} 2.5\ V = m \times (10\ A) + b \\ 0.1\ V = m \times (-10\ A) + b \end{pmatrix} \tag{38}$$

Next, the lower equation in Equation 38 is multiplied throughout by –1, yielding Equation 39:

$$\begin{pmatrix} 2.5\ V = m \times (10\ A) + b \\ -0.1\ V = m \times (10\ A) - b \end{pmatrix} \tag{39}$$

Simplifying the system of equations yields Equation 40:

$$2.4\ V = m \times 20\ A \tag{40}$$

Solving for m gives a gain value of 1.2 V/V and results in a b value of 1.3 V, the offset voltage. To calculate the resistor values for the differential circuit, the following method and circuit layout is used.

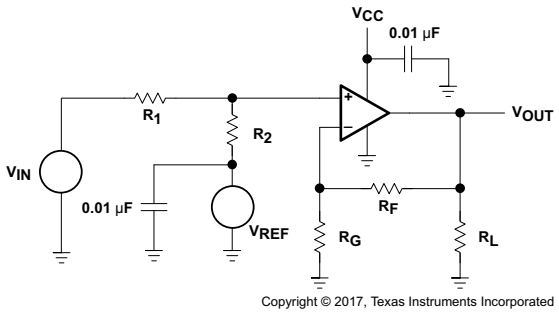

Figure 19. Current Sense Amplifier Setup

The circuit can be written out using a simple voltage divider rule and super positioning. This yields Equation 41:

$$V_{OUT} = V_{IN}\left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_2}{R_1 + R_2}\right) + V_{REF}\left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_1}{R_1 + R_2}\right) \quad (41)$$

Equating the previously calculated coefficients yields Equation 42 and Equation 43:

$$m = \left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_2}{R_1 + R_2}\right) \quad (42)$$

$$b = V_{REF}\left(\frac{R_F + R_G}{R_G}\right)\left(\frac{R_1}{R_1 + R_2}\right) \quad (43)$$

Now the values of R_1 and R_2 can be calculated using the following relationship. A reference voltage source is left out of the design as a space and cost savings measure, and it sacrifices noise performance, accuracy, and stability performance. Cost is an important specification, but the V_{CC} supply must be specified well enough to do the job.

$$\left(\frac{R_F + R_G}{R_G}\right) = m\left(\frac{R_1 + R_2}{R_2}\right) = \frac{b}{V_{CC}}\left(\frac{R_1 + R_2}{R_2}\right) \quad (44)$$

This yields the relationship $R_1 = 0.3283\ R_2$.

The selected resistance values of R_1 and R_2 are:

- $R_1 = 3.3\ k\Omega$
- $R_2 = 10.0\ k\Omega$

Next, the chosen resistor values for R1 and R2 are substituted into Equation 44 for the ratio of R_G and R_F. This yields the ratio $R_F = 0.594\ R_G$.

For this TI Design, the chosen resistance values are chosen to be:

- $R_F = 8.87\ k\Omega$
- $R_G = 14.9\ k\Omega$

Lastly, the shunt resistor value must be calculated based on the given values for the slope and offset voltage. Using the slope intercept form with the calculated values yields:

$$2.5 = 1.2 \times 10\ \alpha + 1.3 \quad (45)$$

where α is the resistance value of the shunt resistor. Solving the shunt resistor value is 0.1 Ω for this TI Design. The dissipation through this resistor is:

$$P_D = I_{RMS}^2\ R_{SHUNT} = (6.5\ A)^2 \times 0.1 = 4.225\ Watts \quad (46)$$

For this design, a 20-W, 0.1-Ω resistor is used for current sensing.

The following simulation output verifies the correct output of the current sense amplifier based on the current across the shunt resistor.

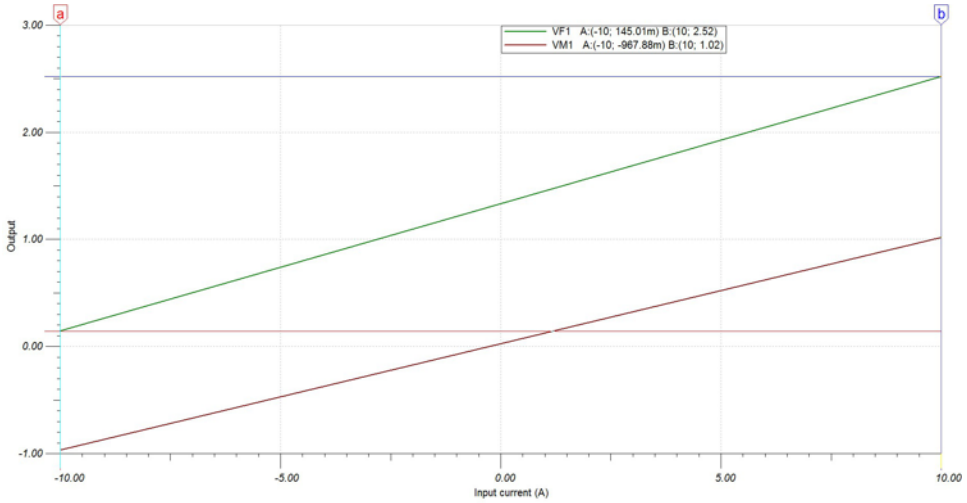

Figure 20. Current Sense DC Sweep Simulation Results

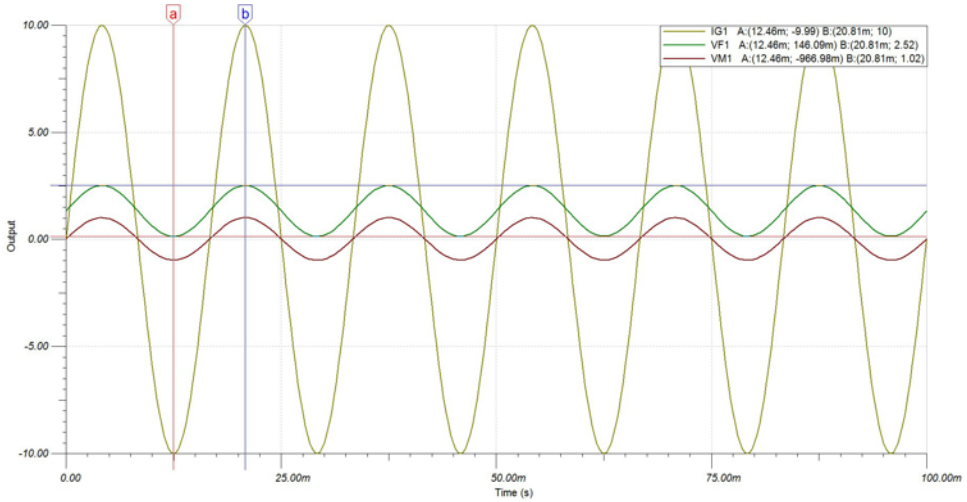

Figure 21. Current Sense Transient Simulation Results

The comparator compares the analog voltages at the non-inverting (+) and inverting (–) input terminals. If the non-inverting terminal is more positive than the inverting terminal, the comparator output CBOUT is high. The comparator can be switched ON or OFF using the control bit CBON. The output of the comparator can be used with or without internal filtering. When the control bit CBF is set, the output is filtered with an on-chip RC filter. The delay of the filter can be adjusted in four different steps. Selecting the output filter can reduce errors associated with comparator oscillation. The comparator features a high-precision reference voltage level, low offset voltage, and high speed. The CBRSEL (reference select) bit in the CBCTL2 register can be configured to obtain different thresholds. The reference voltages available are 1.5 V, 2.0 V, and 2.5 V.

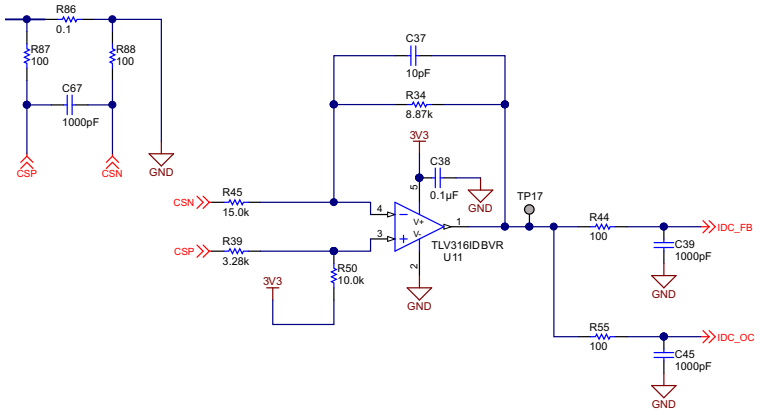

Figure 22. TIDA-01353 Current Sense Amplification Schematic

1.5.9 Optocoupler Isolation Circuit Design Theory

The TIDA-01353 reference design incorporates isolation circuitry between the 24-V AC control signals and the internal logic of the design. Five LTV-817S optocouplers are used as the interface between these two signals. This configuration is shown in Figure 23. Each of the signal pins correspond to a specific speed or setting. These parameters are shown in Table 5.

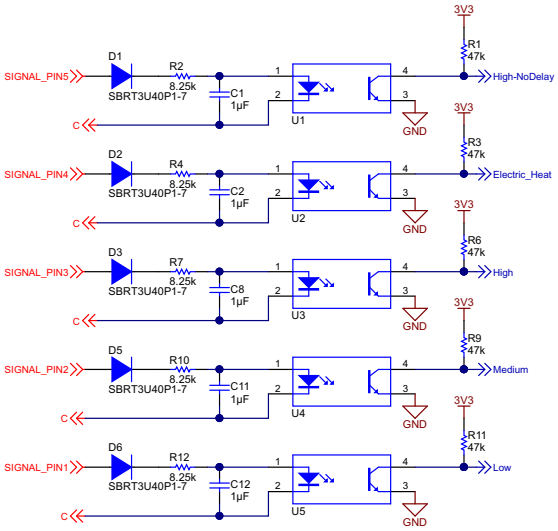

Figure 23. Optocoupler Isolation Schematic

Table 5. Optocoupler Header Pin Function

24-V AC SIGNAL PIN	INTERNAL FUNCTION		MCU INPUT LOCATION
SIGNAL_PIN1	Low fan speed	90-second delay	PJ.0
SIGNAL_PIN2	Medium fan speed	90-second delay	PJ.1
SIGNAL_PIN3	High fan speed	90-second delay	PJ.2
SIGNAL_PIN4	Electric heat	No delay	PJ.3
SIGNAL_PIN5	High fan speed	No delay	PJ.4

The LTV-817 has a maximum forward diode current of 50 mA and a maximum forward voltage of 1.4 V. In order to avoid potential damage and provide a more consistent input signal to the MCU, the 24-V signal is conditioned before entering the isolation interface. The 24-V AC has a maximum DC voltage level ±20% for transformer voltage fluctuations of:

$$V_{DC(MAX)} = \left(24\sqrt{2}\right) \times (1 + 0.20) = 40.73 \text{ VDC} \tag{47}$$

Considering the voltage drop across the diode, the voltage is:

$$40.73 - 0.7 = 40.03 \text{ VDC}$$

In order to ensure the current levels stay within the bounds of the optocoupler specifications, a series resistance is added along with a capacitor to reduce the ripple from the AC source. In order to have a target current input < 5 mA considering a ±20% tolerance, the resistance value is:

$$\frac{40.029 \text{ V}}{0.005 \text{ A}} = 8005.8 \ \Omega \tag{48}$$

In this application, pick a resistance value close to this target value at 8.25 kΩ, giving a maximum current input to the optocoupler of 4.44 mA.

Similarly, the input to the MSP430F5132 has a maximum current tolerance of 2 mA at any I/O pin. The optocoupler current transfer ratio, defined as:

$$\text{CTR} = \frac{I_C}{I_F} \times 100\% \tag{49}$$

where:

- I_C is the collector current, rated for a maximum of 50 mA
- I_F is the forward current, also rated for a maximum of 50 mA

This rating has a maximum at 600% for the LTV-817, reducing the current output to the MCU down to 0.33 mA. Taking this into consideration, along with the desired pullup resistor network layout, the maximum current from the 3.3-V power supply into the MCU is 70.2 µA with a 47-kΩ pullup resistor, well below the limits of the MCU.

2 Getting Started Hardware and Firmware

2.1 Getting Started Hardware

The following sections outline how the board should be configured to test the TIDA-01353 reference design. Use caution when working with high voltage, and do not to make contact with the board during operation.

2.1.1 Setting up the TIDA-01353 Board

Take extra precaution to ensure the following connections are correct before applying power to the board. J1 is the header for the main line voltage. The hot wire is connected to the L1 terminal, and the neutral wire is connected to the N terminal. The Earth ground is located at the terminal labeled G. Terminal position 4 has no connection and is therefore labeled with an N/C. The last terminal pin on header J1 is the common wire for the 24-V AC from the air handler control circuit board. Figure 24 shows the correct wiring of the board to a 120-V AC power outlet. The terminal block is rated for 300 V and 15 A.

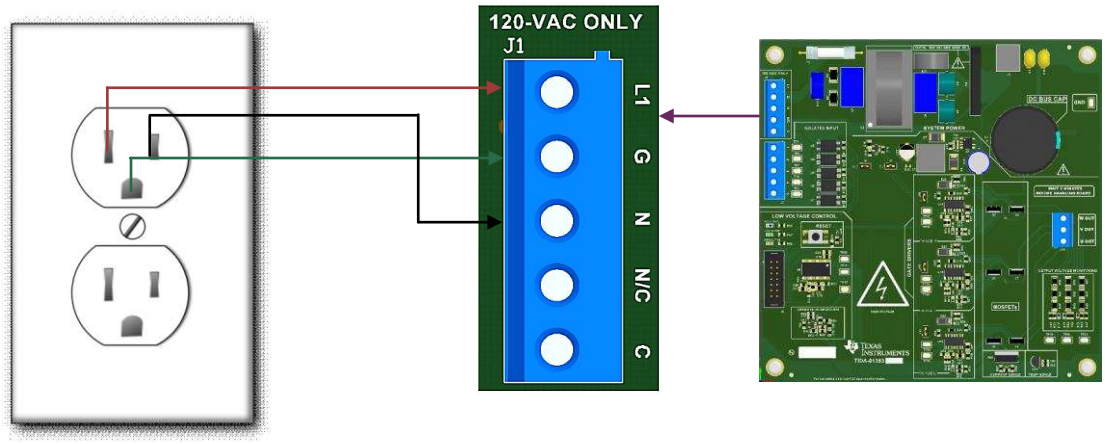

Figure 24. 120-V AC Power Outlet Board Connection Example

CAUTION

For the control signals, there should only be one 24-V AC signal connected to the board at a time. See Section 1.5.9 for further details with respect to the control signal terminal. The 24-V signal should only be tied to J3 terminals to prevent damage to the board. As with the previous connection, do not apply power until all wiring has been properly connected to the TIDA-01353 board.

For this TI Design, the motor chassis is shown in Figure 25. As seen in Figure 25, the three connectors (U,V,W) are wired to the red, blue, and yellow wire of the socket connector of the motor, respectively. Nte that the wire gauge should be 18 AWG at a minimum. After completing the connection, ensure there are no exposed wires, which can create a potential shock hazard.

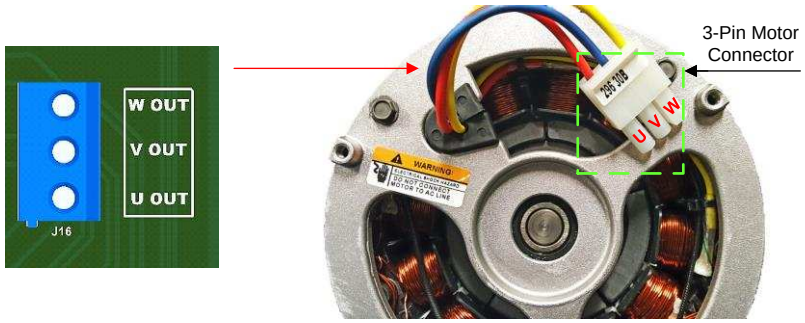

Figure 25. ECM Connection to TIDA-01353

2.1.2 Programming the MSP430

Programming the MSP430F5132 is done by means of a 4-Wire JTAG. The 14-pin connector diagram is shown in Figure 26 for the 4-wire JTAG programming. J1 at pin 4 is connected to the internal 3.3-V supply to provide power to the JTAG interface.

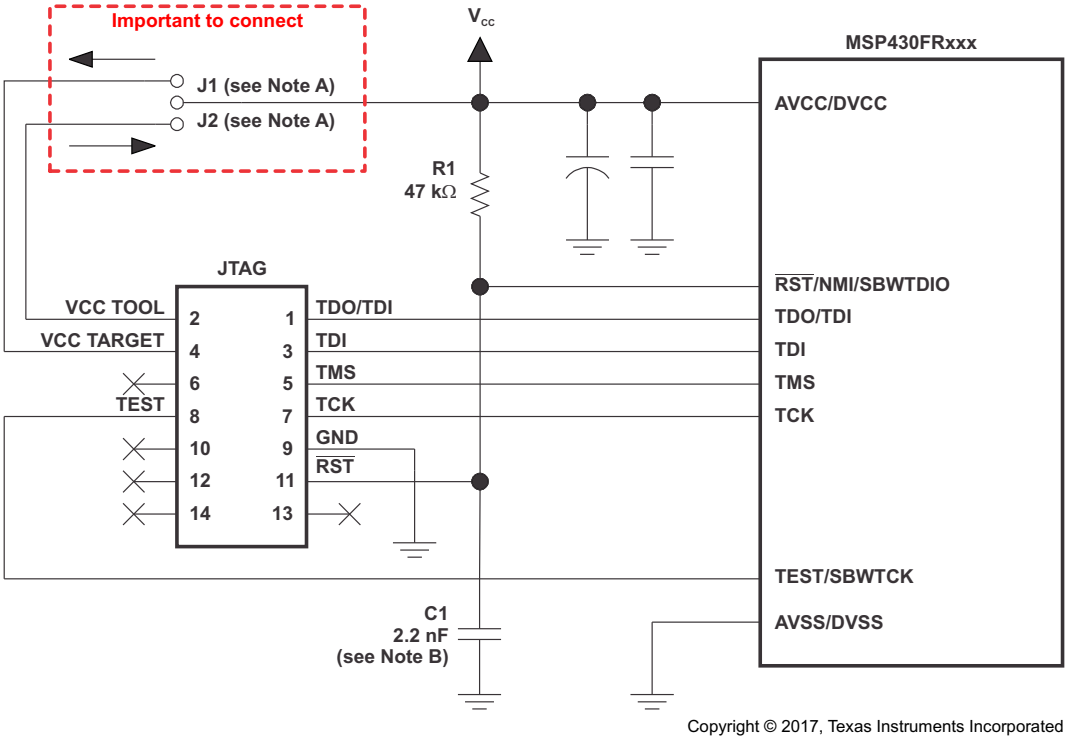

Figure 26. Programming of MSP430 With 4-Wire JTAG

Follow these steps to program the MSP430F5132:

1. Switch off the mains input to the board. Wait for the DC bus voltage stored on the DC bus capacitor to ramp down to zero. A safe practice is to wait at least 5 minutes before handling the board after a 120-V AC supply voltage is removed from the system.
2. Apply a 3.3-V power source from a supply to connector J4 and the common of the power supply to the GND pin on the board. The 3.3-V LED should become active when correctly connected.

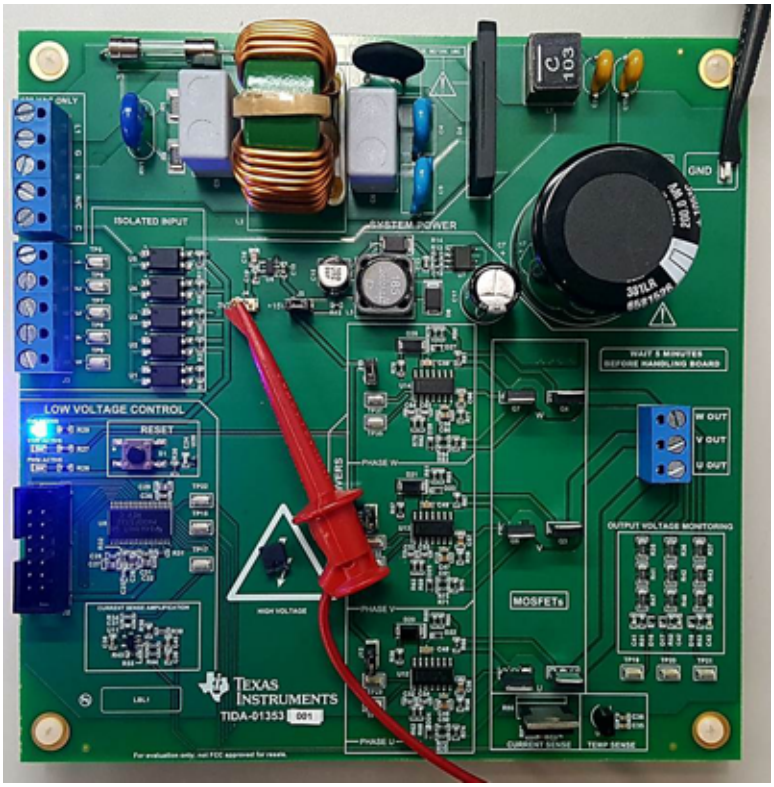

Figure 27. 3.3-V Connection for MSP430F5132 JTAG Programming

3. After turning ON the supply, connect the programming connector from the programmer.
4. Open Code Composer Studio™ (CCS), then build and debug the program to program the code to MSP430F5132.

WARNING

Failure to allow the DC bus capacitor to fully discharge can result in serious injury or death. Exercise extreme caution when operating the board.

2.2 Getting Started Firmware

TI's InstaSPIN-BLDC™ is the core of this software implementation. Section 2.2.1 provides details for implementing an InstaSPIN-BLDC solution, and subsequent Section 2.2.2 and Section 2.2.3 outline the complete implementation of the software.

2.2.1 InstaSPIN-BLDC

InstaSPIN-BLDC is one of TI's key flagship motor control technology targeted for cost sensitive sensorless BLDC applications. This sensorless technique uses traditional trapezoidal or 120° commutation and monitors motor flux by integrating BEMF of non-energized phase to determine the commutation instances. For certain markets such as fans, pumps, blowers, and so on, all which do not require a fast dynamic torque response, InstaSPIN-BLDC implementation is the right way to meet low-cost requirements.

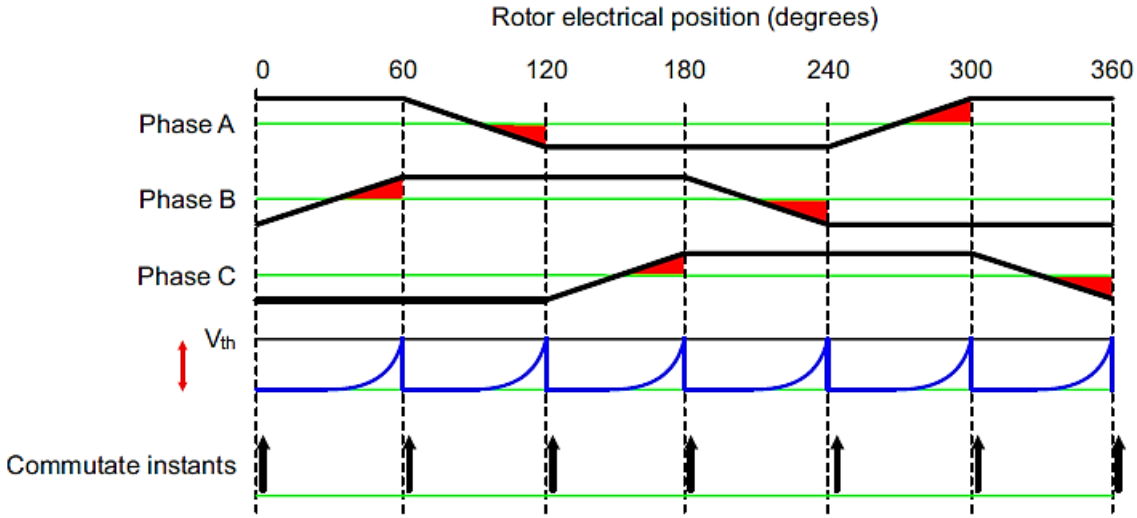

Figure 28. Implementation of Two-Quadrant Uni-Polar PWM

For any trapezoidal control of a BLDC motor, for each 60 electrical degrees, only two inverter legs are active and deliver the power to motor while third inverter leg is kept in high impedance state by switching off both high-side and low-side switches. For a uni-polar two-quadrant drive (see Figure 28), PWM is applied only to the high-side switch of one active leg while the low-side switch of other active leg is kept ON continuously for one 60 electrical degree.

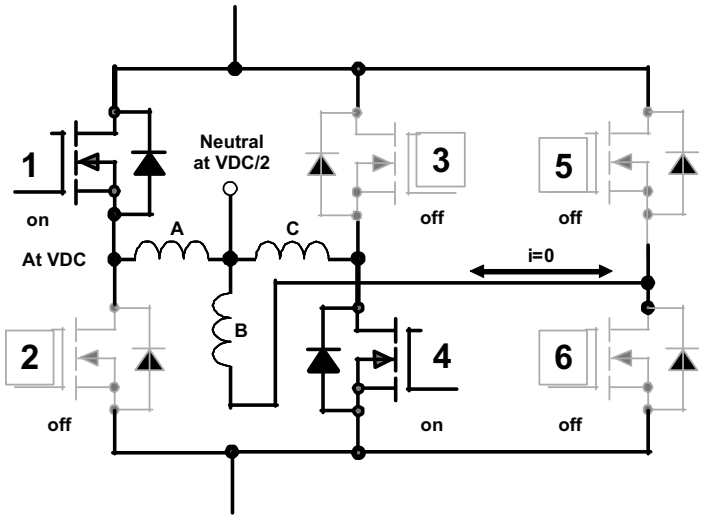

Figure 29. Motor Neutral Voltage During PWM ON

The InstaSPIN-BLDC method requires precise sensing of BEMF of open phase of the motor to determine the commutation instant. As shown in Figure 29, for the first 60-degree interval, PWM is applied only to the phase-A top switch. In the phase-C bottom switch is continuously ON, BEMF of open phase B is rising and can be measured and integrated to determine the commutation instant. During the ON-time of the PWM pulse, with top switch of phase-A connected to VDC and the bottom switch of phase-C connected to GND, motor neutral terminal potential rises to VDC/2 with respect to GND, and BEMF of phase-B appears at VDC/2 level above GND. By capturing the absolute value of voltage across phase-B during PWM on pulse and subtracting it with VDC/2, actual value of motor BEMF can be derived.

2.2.1.1 Tuning the Motor With Proper Flux Threshold

The commutation instance is derived by integrating the BEMF of non-energized phase (obtained during each PWM on pulse) and comparing the integrated value to pre-defined threshold. The threshold is in fact equivalent to flux of the motor because it is compared with the integrated value of the BEMF. The value of the flux threshold depends upon the motor BEMF constant; therefore, this value needs to be tuned for each motor for commutation. For tuning purposes, usually an oscilloscope is used to see the symmetry of the motor input voltages or motor phase current. See Figure 30 for the different flux threshold values. These scope shots show the motor input voltage and a current waveform for one phase.

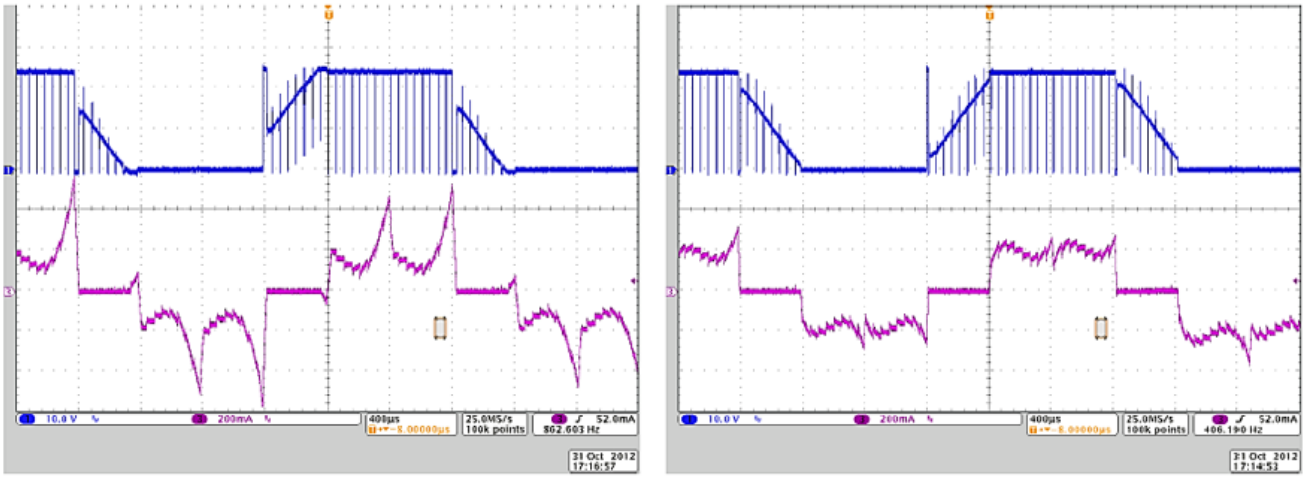

Figure 30. High versus Optimized Flux Threshold Waveforms

2.2.2 System Features

The TIDA-01353 firmware offers the following features and user controllable parameters:

- Trapezoidal sensorless control of the BLDC motor using BEMF integration method
- Open loop control to accelerate the motor to a certain speed so that there is enough BEMF for sensing and then moving to closed loop control, which integrates the BEMF to commutating motor winding current switching at the exact position
- The sensorless control code that can be customized based on the target motor
- Overcurrent protection using internal comparator of the MSP430F5132

Table 6. MSP430F5132 Usage Summary

PARAMETER	VALUE
Target controller	MSP430F5132
PWM frequency	20-kHz PWM (default), programmable for higher and lower frequencies
PWM mode	Asymmetrical with no dead band
Interrupts	CPU Timer D1: Implements 20-kHz ISR execution rate
	ADC interrupt
Peripherals used	TIMER D1.0 for motor control PWM
	ADC-A0: DC bus voltage sense
	ADC-A2: Temperature sense
	ADC- A3, A4, A5: Motor winding voltage sensing
	COMP B: Comparator for current limit protection
	TEC0FLT1: Overcurrent limit fault input

2.2.3 Customizing the Reference Code

To modify the sensorless code, the end user must have CCS and the MSP430F5132 configuration files installed. This section describes the different user adjustable parameters and how to select an optimized value for a specific application. Start by loading the project into CCS and locating the parameters.

1. Open CCS and load the reference project "TIDA-01353_Sensorless_BLDC_V1.0". Note if this project is zipped it must be extracted.
2. Select the file "main.c". At the top of the file are some parameters that can be optimized, which are included as the configuration variables. Figure 31 shows these parameters:

```
unsigned int INTEGRATION_CONSTANT =300;
unsigned char START_UP_DUTY = 1;//%
unsigned char START_UP_MAX_DUTY= 4;//%
unsigned char INCREMENTAL_DUTY = 1;//%
unsigned char INCREMENTAL_TIME = 80;//
unsigned int WAIT_TIME = 50000;//
unsigned char SPEED_DUTY_MAX = 80;//%
unsigned char SPEED_UTY_MIN = 30;//%
unsigned char SPEED_RAMP_CYCLES = 5;
unsigned int MAX_DUTYCYCLE =  768 ;
unsigned int Velocity_Ramp = 5000;
```

Figure 31. Optimization Capable Variables

2.2.3.1 PWM_PERIOD

The PWM_PERIOD is used to set the value in TimerD capture/compare register 0. Because TimeD is used as the PWM generator, this value specifies at what timer count the timer generates an interrupt and restarts from zero. TimerD is initialized to operate at 25 MHz; see Equation 50 for calculating the PWM frequency. The TIMERD PWM is configured in UP Mode.

$$\text{PWM Frequency}\,(\text{Hz}) = \frac{25\,\text{MHz}}{((\text{PWM\_PERIOD}) - 1)} \tag{50}$$

For example, here PWM_PERIOD = 1251, therefore:

$$\text{PWM Frequency}\,(\text{Hz}) = \frac{25\,\text{MHz}}{(1252 - 1)} = 20\,\text{kHz}$$

2.2.3.2 MAX_DUTY_CYCLE

MAX_DUTY_CYCLE sets the maximum threshold the input duty cycle command is allowed to. Every time the input is read, the duty cycle input command is compared to MAX_DUTY_CYCLE, and if it exceeds it, the target duty cycle is set to MAX_DUTY_CYCLE. This number is relative to the PWM period.

2.2.3.3 MIN_DUTY_CYCLE

MIN_DUTY_CYCLE sets the minimum duty cycle that can be applied to the motor.

2.2.3.4 BEMF_THRESHOLD

BEMF_THRESHOLD is the only parameter that needs to be measured on the motor. Follow these steps to calculate this parameter:

1. Verify the motor is not connected to the board.
2. Use an oscilloscope to capture the differential voltage waveform between any two phases.
3. Measure the amplitude and frequency of the BEMF (see Figure 32).
4. Calculate the BEMF constant (K_e) parameter by using Equation 51. Note that the BEMF constant used is the phase-to-phase value.

$$K_e\left(\frac{V}{\text{Hz}}\right) = \frac{\text{Amplitude}\,(V)}{\text{Frequency}\,(\text{Hz})} \tag{51}$$

where

- T = Time period of the BEMF waveform
- Frequency (Hz) = 1/T

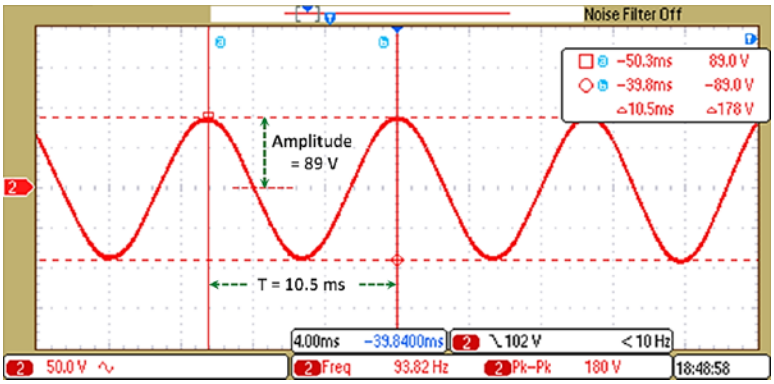

Figure 32. BEMF Oscilloscope Output

Figure 33 shows the BEMF integration zones in the motor winding voltage waveform. The center tap voltage is VDC/2. The BEMF integration starts when the winding voltage of the non-switching phase crosses the center tap and continues until the integrated value reached the BEMF threshold.

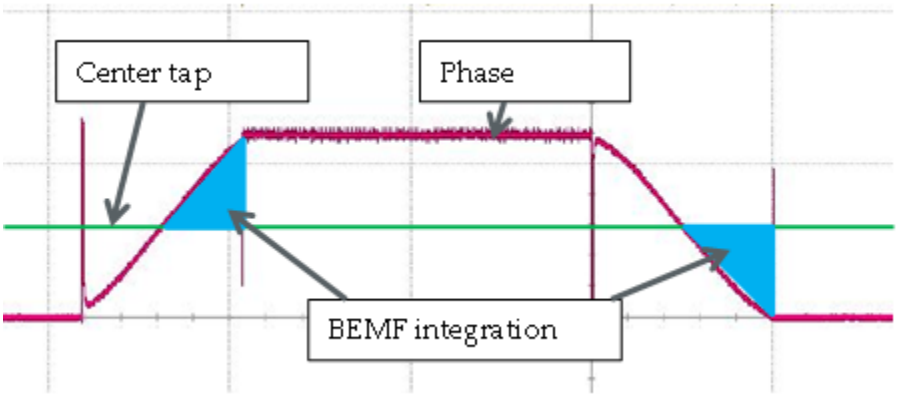

Figure 33. Phase Voltage Waveform Showing BEMF Integration Zones

Figure 34 explains how to calculate the BEMF threshold using the BEMF constant of the motor. The calculations are given in Equation 52 through Equation 55.

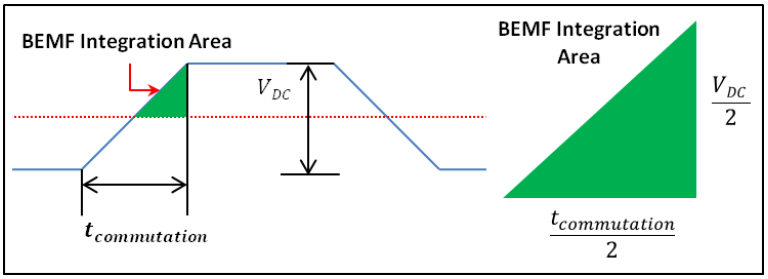

Figure 34. BEMF Integration Area

In the MCU, the ADC samples in every PWM cycle. The PWM time period = (1 / PWM frequency) ≈ 50 µ.

The full-scale output of a 10-bit ADC = 1024 discrete values with a full-scale input voltage of 3.3 V. Therefore, the ADC reading for any winding voltage of V_{ph} can be expressed as:

$$\text{BEMF ADC Reading} = \frac{V_{ph} \times 3.6}{450 + 3.6} \times \frac{1024}{3.3} = 2.24627 \times V_{ph} \quad (52)$$

From Figure 34, the maximum phase-to-phase BEMF (V_{ph}) is V DC. The $T_{commutation}$ is the time period between two commutation instances:

$$T_{commutation} = \frac{T}{6}$$

Using the previously calculated BEMF constant K_e, $T_{commutation}$ can be calculated as:

$$T_{commutation} = \frac{K_e}{6 \times \text{BEMF Amplitude}} = \frac{K_e}{6 \times V_{DC}} \quad (53)$$

Next, from Figure 34, the BEMF integration area is:

$$\text{BEMF integration area} = \frac{1}{2} \times \frac{2.24627\ V_{DC}}{2} \times \frac{T_{commutation}}{2} \quad (54)$$

where VDC is multiplied by the ADC reading scale factor. Additionally, the ADC samples the BEMF in each PWM cycle every 50 µs. Substituting this value into the denominator of Equation 54 and substituting $T_{commutation}$ with Equation 53, the BEMF_THRESHOLD can be calculated as:

$$\text{EMF Threshold} = \frac{k_e \times 2.24627}{6 \times 8 \times 50\ us} = k_e \left(\frac{V}{Hz} \right) \times 936 \quad (55)$$

The parameter required in the reference code is a scaled version of the K_e in V/Hz. To scale the K_e to the needed BEMF_THRESHOLD value, multiply K_e by 936. This value is the threshold of the integrated BEMF measured from the center tap zero crossing by the ADC. If this number is not correct for the specific motor, it may not run as expected.

For advanced control, this value can be adjusted as a lead angle adjustment. If the value is set lower than the measured number, the control will commutate earlier. If the parameter is set greater than the calculated threshold, the commutation event will be delayed.

2.2.3.5 START_UP_DUTY

The first open loop control duty cycle is fixed to the START_UP_DUTY parameter. This is used to align the motor to a particular position. This number can be adjusted for a specific motor to control how much current is used during startup. This number is related to the PWM period.

2.2.3.6 START_UP_DUTY_MAX

During open loop control startup, the START_UP_DUTY parameter is gradually increased to START_UP_DUTY_MAX to complete the alignment of the motor to the start position. This number is related to the PWM period.

NOTE: To tune the software parameters for your motor, BEMF_THRESHOLD and START_UP_DUTY are the key parameters to start with.

To change the direction of rotation of the motor, interchange any two motor winding connections to the board.

2.2.3.7 Overcurrent Limit

The MSP430F5132 has an integrated comparator and timer event control module, which can be configured to implement the current limit.

The CBRSEL (reference select) bit in the CBCTL2 register can be configured to get different thresholds. The reference voltages available are 1.5 V, 2.0 V, and 2.5 V. See Section 1.5.8 for more details.

2.2.4 Running the Project in CCS

To run this project in CCS:

1. Install CCS using the CCS Installation.
2. Import the project "TIDA-01353_sensor_based_BLDC_V1.0".
3. Read through Section 2.2.3 to tune the control for the specific motor.
4. Power up the board and connect the JTAG connector to the board.
5. Build and debug the modified project to download the code to the MSP430F5132.

3 Testing and Results

The following sections outline the testing of TIDA-01353 along with the results for each test.

3.1 UCC27714 Functionality Testing

The UCC27714 gate driver receives the PWM signals from the MSP430 MCU and the corresponding gate drive voltages are generated. Figure 35 shows the low-side and high-side output from the UCC27714. In BLDC trapezoidal control, only the high side is modulated and is switching at 20 kHz in the 120-degree ON period. The low side is continuously ON for 120 degrees.

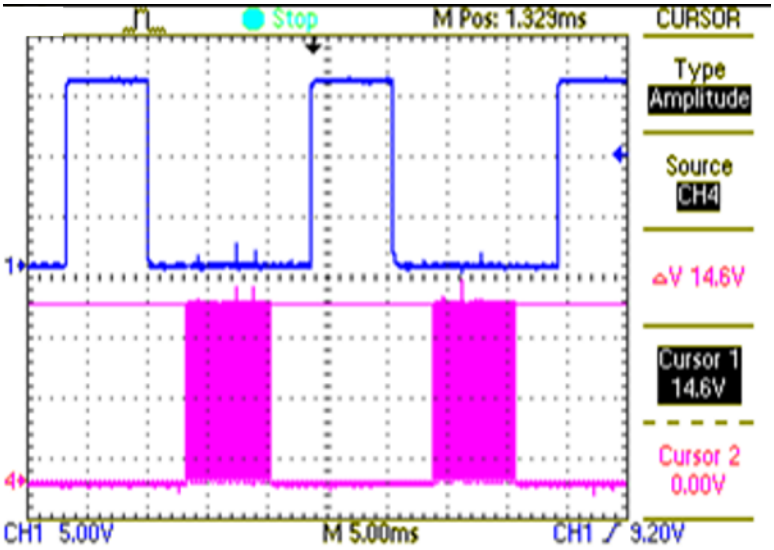

Figure 35. High-Side and Low-Side PWM Input to UCC27714

Figure 36 shows the low-side signal input and the corresponding low-side output of one UCC27714 measured across the gate-to-source voltage (V_{GS}) of the MOSFET. The low-side gate output from the UCC27714 swings between ground and V_{CC} of the UCC27714.

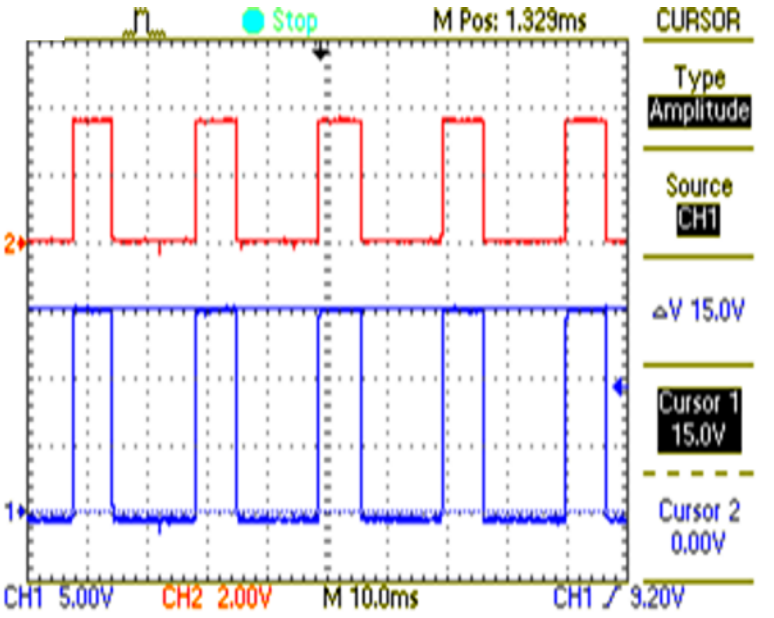

Figure 36. V_{GS} of Low-Side MOSFET and PWM From MCU

Figure 37 shows the high-side signal input and the corresponding high-side output of the UCC27714 measured across the gate-to-source voltage (V_{GS}) of the MOSFET. The gate-to-source voltage is equal to V_{CC} of the UCC27714 minus the drop across the bootstrap diode of the high-side driver in the UCC27714. The waveforms reveal that the V_{GS} is approximately 14.6 V.

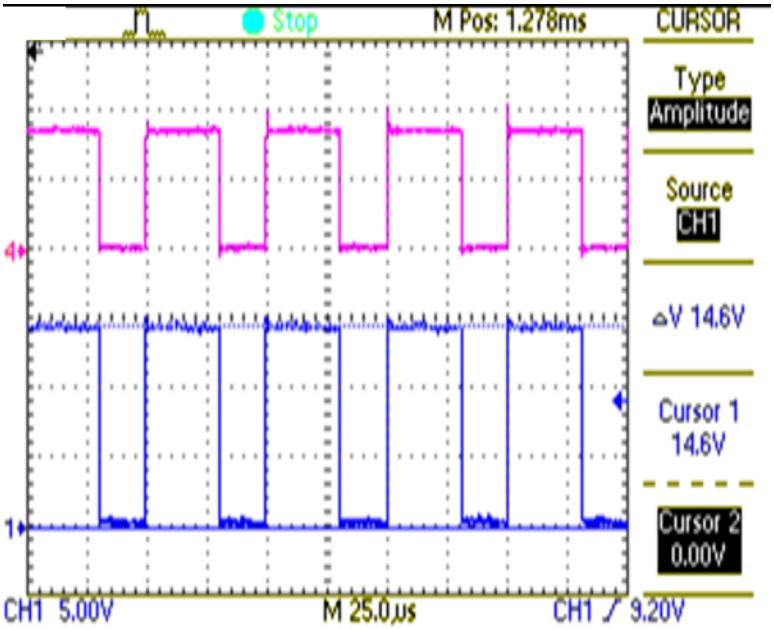

Figure 37. V_{GS} of High-Side MOSFET and PWM From MCU

3.2 Power Supply Testing

The power supply provides the main voltage and current requirements to each of the devices on the board, in addition to the motor phases. For this testing, the voltage is reduced to avoid high-voltage conditions on the oscilloscope probes. A signal generator is used to provide the simulated input source of the design. The signal is a 60-Hz, 10-V peak-to-peak sinusoid. The setup is shown in Figure 38. The input is attached to the L1 terminal and the signal generator ground is tied to the N terminal.

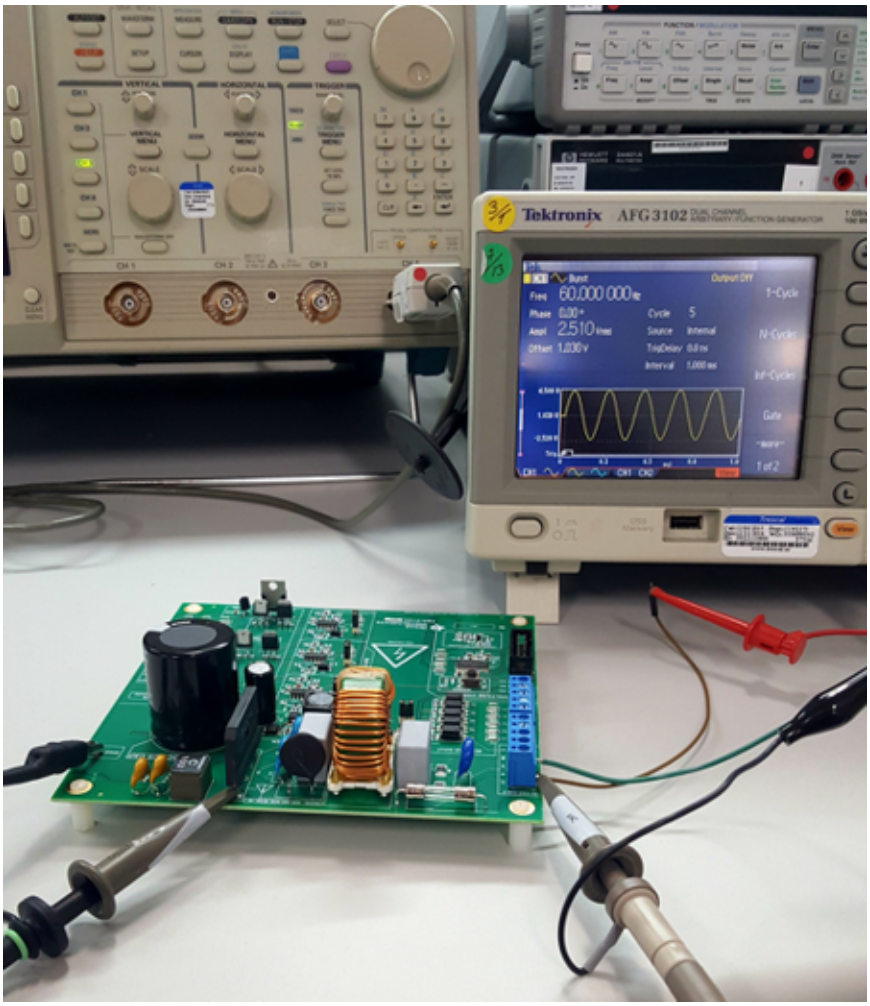

Figure 38. Main Power Supply Testing Setup

The voltage of the signal generator is set to 10 V_{p-p} and applied to the L1 and N terminals of the circuit once all other connections have been made. As shown in Figure 39, the DC_Link ripple for this circuit is approximately 0.219 V_{p-p}. With an input of 10 V, this makes the ripple of 2.19%.

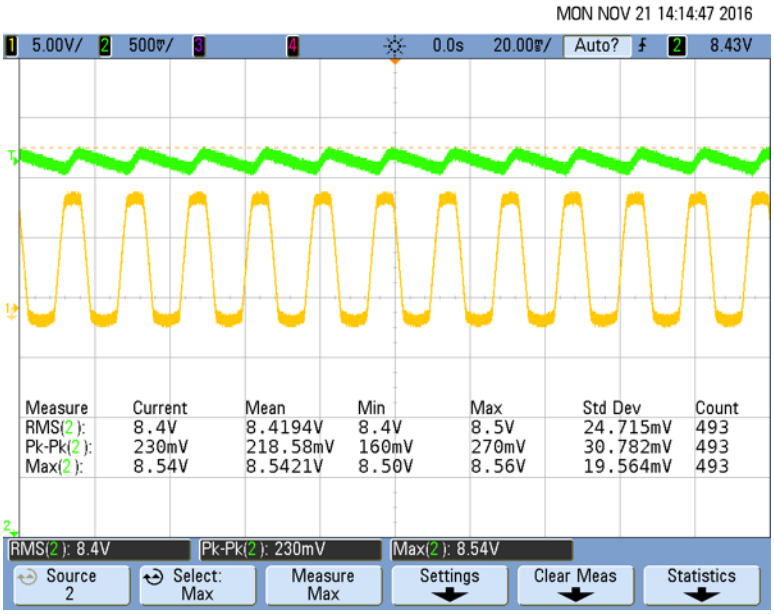

Figure 39. 10 Vp-p Input and DC_Link Voltage Output

Table 7 also shows key testing parameters of the power supply and their respective values.

WARNING

The full-scale DC voltage value at the DC_Link should only be acquired and tested by a professional, as this creates a serious shock hazard to the user. Any unintended contact with the high voltage sections of the board can cause serious harm or death.

Table 7. Main Power Supply Key Test Parameters

PARAMETER	VALUE	UNITS
Average DC_Link voltage (120-V AC input)	163.5000	VDC
Signal generator input	10.0000	V_{p-p}
DC_Link voltage ripple (10-V input)	219.0000	mV_{p-p}
UCC28881 output voltage (25-V DC input)	13.7180	VDC
LM2985-33 output voltage (25-V DC input)	3.3170	VDC

3.3 Optocoupling Isolation Testing

To test the optocoupling circuitry, an external 3.3-V DC power source is connected to the outgoing terminal pin of the 3.3-V jumper. This source powers the MSP430F5132 for speed control interrupts.

Next, a transformer is attached to the circuit to simulate the control signal sent from the air handler's main control board. The common is attached to the terminal block connection labeled "C" and the other wire is tied into the "1" terminal of the control signal block. The wiring is done and checked for safety before any voltage is applied to the transformer.

Last, the oscilloscope is connected to the circuit in order to characterize the behavior of the optocouplers. Figure 40 shows the setup for the control signal isolation circuitry. Verify all connections before applying power to any connection on the board.

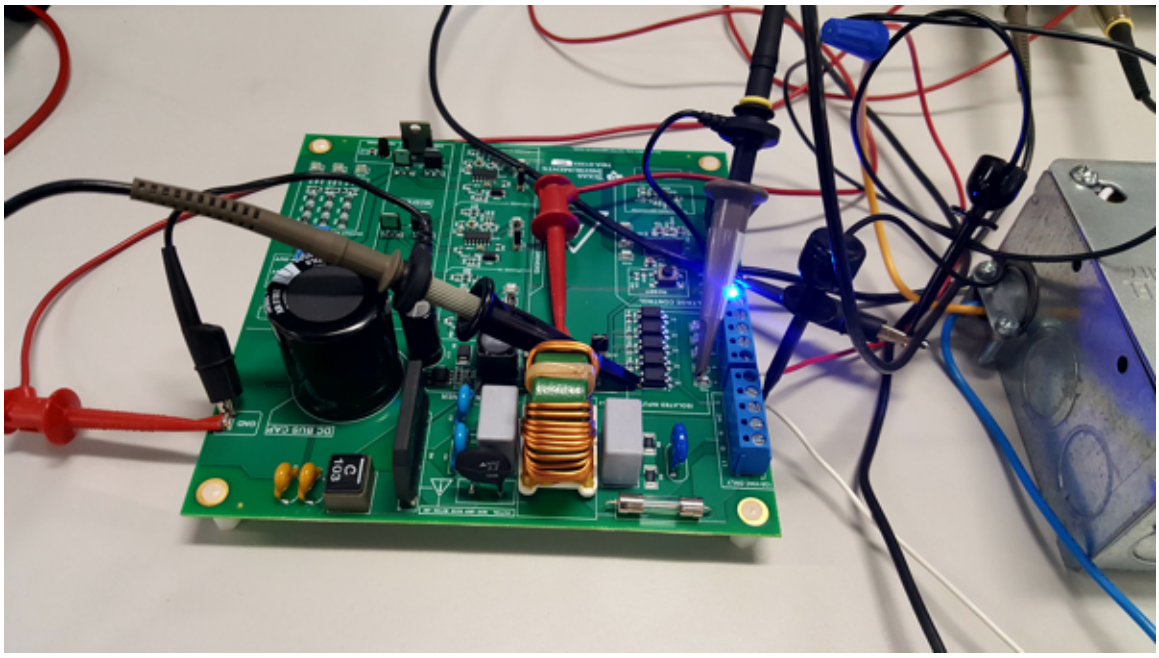

Figure 40. 24-V AC Control Signal Optocoupler Test Setup

CAUTION

Two separate oscilloscopes are used in the test shown in Figure 40 to keep the grounds of each power source isolated from the other. Damage may occur if the oscilloscope is used to read both signals simultaneously.

Figure 41 shows the oscilloscope results for the control board side of the circuit. The voltage level has an RMS value of 26.373 V with a peak value of 39.9 V. This voltage source is used to drive the internal optical circuitry to turn on the transistor. The sinusoidal input signal creates a pulsed signal on the input to the MCU.

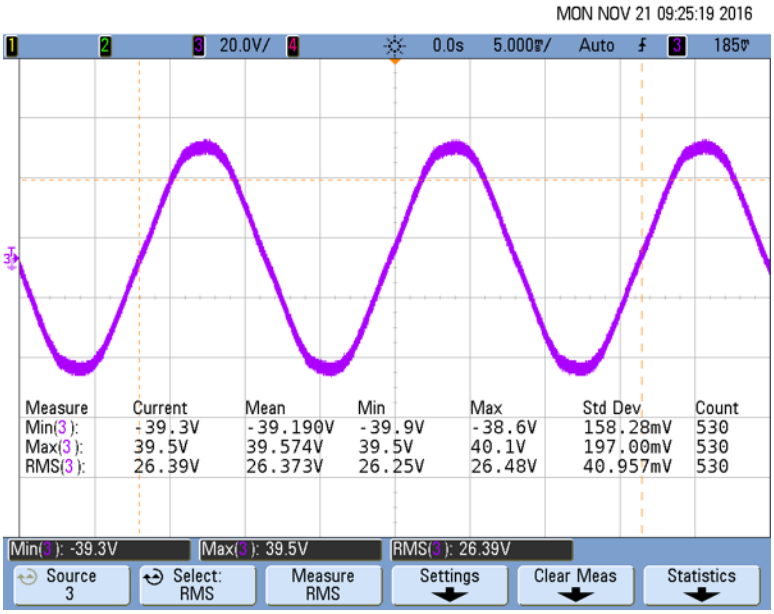

Figure 41. 24-V AC Transformer Optocoupler Input

The transistor of the optocoupler is turned "on" once the threshold voltage of the transistor is reached. Figure 42 shows the output of the optocoupler into the MSP430F5132. This rectified wave has a minimum value of 581 mV and an RMS voltage of 943 mV, and has a synchronous frequency with that of the 24-V AC air handler input signal. Once the signal drops below a preset threshold on the input of the MCU, the speed assigned to that specific input pin can begin execution. In this test, the voltage drops from a DC value of 3.3 V to an AC signal with an average maximum voltage of 1.15 V over roughly 1.5k samples. In the event of a no control signal, the pulsed output of the optocoupler stops and the voltage returns to the 3.3 V provided by the pullup resistor network. This simulates the control board relaying to the ECM motor that the temperature requirement on the thermostat has been reached. If the fan is on "AUTO" it shuts off. If the fan is on, it remains running regardless of the cooling or heating cycle.

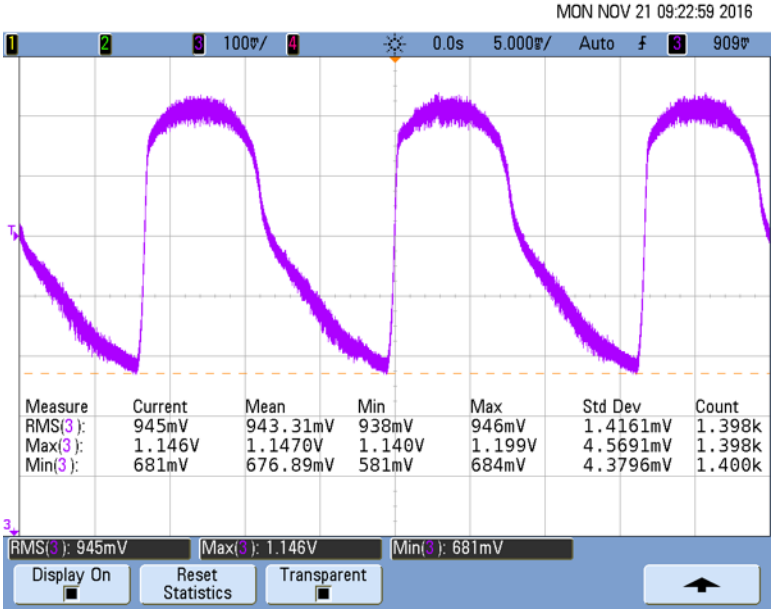

Figure 42. MCU Speed Setting Input From Optocoupler

3.4 Overcurrent Protection Testing

The reference design uses the TLV316 op amp configured as a differential amplifier to sense the winding current. The high bandwidth of the TLV316 is suitable choice for motor current sensing and protection applications. Figure 43 shows the winding current and the output of the TLV316. As can be confirmed by the output, the high bandwidth of the amplifier helps in tracking the DC bus current properly.

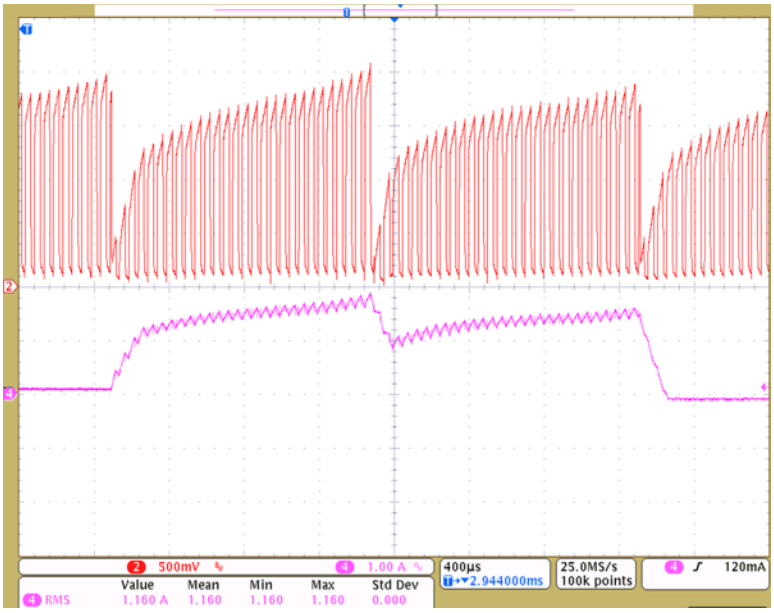

Figure 43. Motor Winding Current and Current Sense Amplifier Output

As previously mentioned, the threshold voltage of the MCU is set to 2.5 V and the current limit is set at ±10 A. To test and verify simply and safely with respect to functionality, the comparator value is set to 1.5 V with an overcurrent at 1.25 A. Figure 44 shows the current limit operation in action. The PWM is turning off immediately when the comparator output goes high.

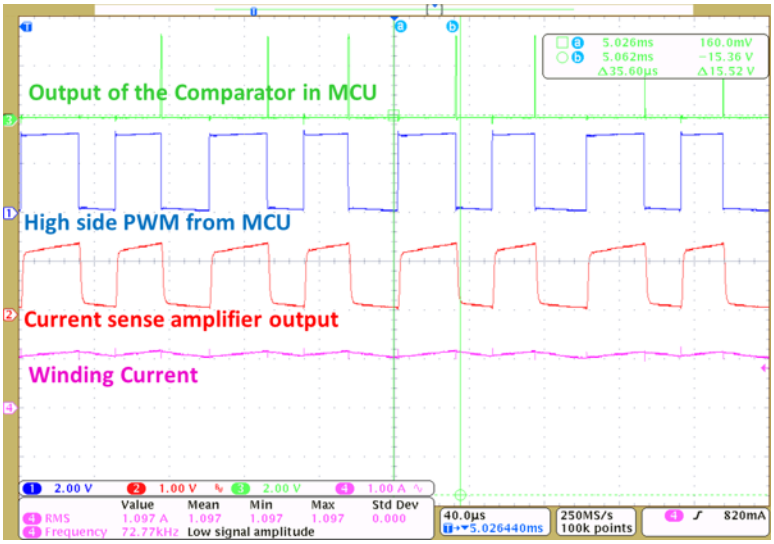

Figure 44. Cycle-By-Cycle Current Limit Showing the PWM Shutdown With Comparator Output of MSP430F5132

Figure 45 shows the response time of the current limit action of the design. The response time from the comparator output going high to PWM shut down event is approximately 100 ns.

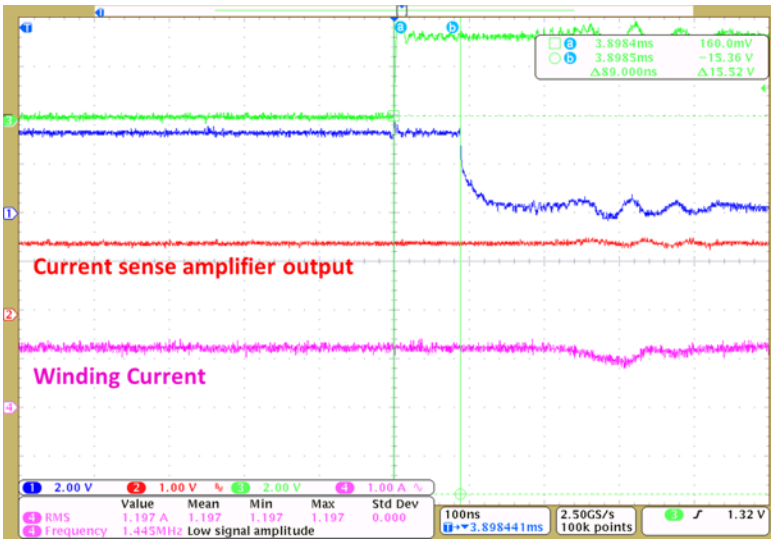

Figure 45. Response Time From Comparator Goes High To PWM Shutdown

3.5 Effect of Motor Inductance on BEMF Sampling

The motor inductance greatly influences the BEMF sampling. The winding inductance causes oscillations with any existing parasitic capacitance on the board. Figure 46 shows the oscillations in the winding voltage of the non-switching phase. This is important in sampling the winding voltage.

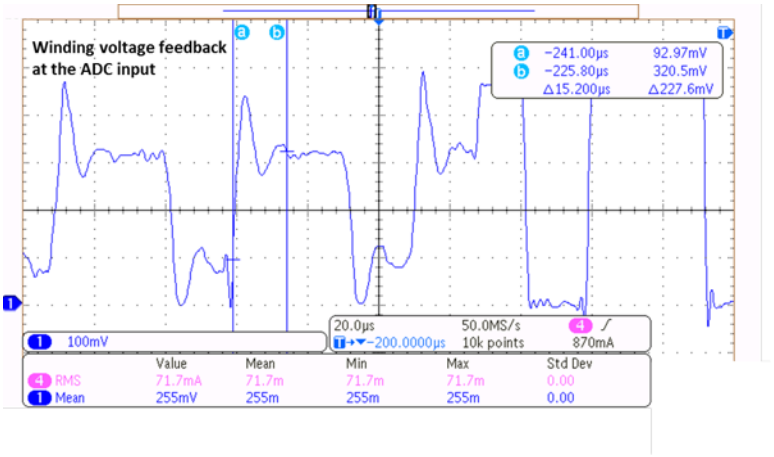

Figure 46. Oscillations in Winding Voltage Feedback for High-Inductance Motor

The best sampling point is at the mid of the PWM on period, where the oscillations are damping down. At low duty cycles, the sampling point can be moved towards 75% of the PWM on period. Figure 47 shows the winding voltage of the non-switching phase in a low inductance motor. When the motor inductance is very low, the oscillations are small and are getting damped out very soon. Therefore, the ADC sampling can be done at even 25% of the PWM on period.

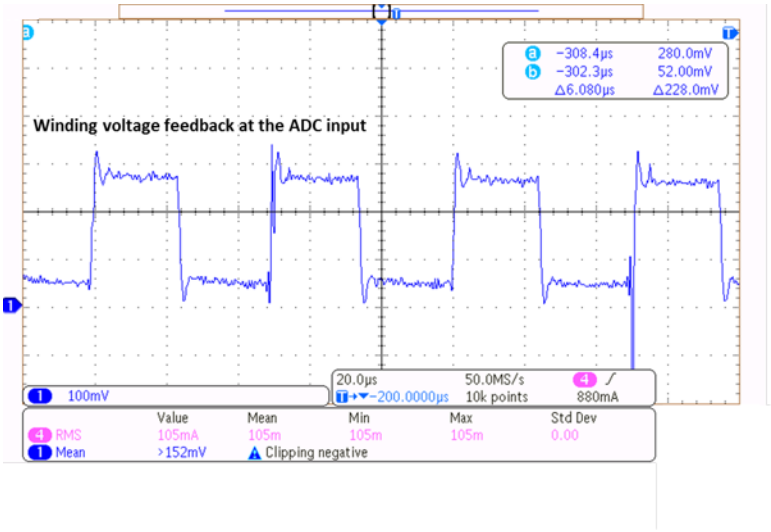

Figure 47. Oscillations in Winding Voltage Feedback for Low inductance Motor

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-01353.

4.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-01353.

4.3 PCB Layout Recommendations

A careful PCB layout is critical and extremely important in a fast-switching circuit to provide appropriate device operation and design robustness. As with all switching power supplies, attention to detail in the layout can save much time in troubleshooting later on.

4.3.1 UCC28881 Layout Guidelines

The VDD pin provides a regulated 5-V output, but it is not intended as a supply for external load. Do not supply VDD pin with external voltage source (for example, the auxiliary winding of flyback converter). Always keep GND pin 1 and GND pin 2 connected together with the shortest possible connection. Additional layout guidelines are as follows:

- In both buck and buck-boost low-side configurations, minimize the copper area of the switching node DRAIN to reduce EMI.
- Similarly, minimize the copper area of the FB pin to reduce coupling to feedback path. Also minimize loop CL, Q1, and RFB1 to reduce coupling to feedback path.
- In high-side buck and buck-boost, the GND, VDD and FB pins are all part of the switching node, so optimize the copper area connected with these pins. A large copper area allows better thermal management, but it causes more common-mode EMI noise. Use the minimum copper area that is required to handle the thermal dissipation.
- Keep a minimum distance between the 700-V coated traces, which is 1.41 mm (60 mils).

4.3.2 LP2985-33 Layout Guidelines

- Bypass the input pin to ground with a bypass-capacitor.
- The optimum placement of the bypass capacitor is closest to the VIN of the device and GND of the system. Minimize the loop area formed by the bypass-capacitor connection, the VIN pin, and the GND pin of the system.
- To operate at a full-rated load, use wide trace lengths to eliminate IR drop and heat dissipation.

4.3.3 UCC27714 Layout Guidelines

- Place the UCC27714 as close as possible to the MOSFETs in order to minimize the length of high-current traces between the HO/LO and the gate of MOSFETs.
- Use a 5-Ω resistor series with bias supply and VDD pin.
- Place the VDD capacitor (C_VDD) and VHB capacitor (CBS) as close as possible to the pins of the UCC27714.
- Use a 2- to 5-Ω resistor series with bootstrap diode to limit bootstrap current.
- Use an RC filter with 5.1 to 51 Ω and 220 pF for HI/LI.
- Separate power traces and signal traces, such as output and input signals.

4.3.4 TLV316 Layout Guidelines

For the best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and the operational amplifier. Bypass capacitors reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of the circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are typically devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques* (SLOA089).
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicularly is much better than crossing in parallel with the noisy trace.
- Place the external components as close to the device as possible. Keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.

4.4 Altium Files

To download the Altium project files, see the design files at TIDA-01353.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-01353.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-01353.

4.7 Software Files

To download the software files, see the design files at TIDA-01353.

5 Related Documentation

1. Texas Instruments, *MSP430F51x2 and MSP430F51x1 Mixed Signal Microcontrollers*, MSP430F5132 Datasheet (SLAS619)
2. Texas Instruments, *UCC27714 High-Speed, 600-V High-Side Low-Side Gate Driver with 4-A Peak Output*, UCC27714 Datasheet (SLUSBY6)
3. Texas Instruments, *Sensorless Trapezoidal Control of BLDC Motors*, Application Report (SPRABQ7)
4. Texas Instruments, *UCC28881 700-V, 225-mA Low Quiescent Current Off-Line Converter*, UCC28881 Datasheet (SLUSC36)
5. Texas Instruments, *Op Amps for Everyone*, Design Reference (SLOD006)
6. Texas Instruments, *Analog Temperature Sensors with Class-AB Output*, LMT84 Datasheet (SNIS167)
7. Texas Instruments, *230-V/250-W, Hi-η Sensorless Brushless DC Motor Drive With 30% Reduced Bulk Capacitor Reference Design*, TIDA-00472 Design Guide (TIDUAR7)
8. Texas Instruments, WEBENCH Design Center (http://www.ti.com/webench)

5.1 Trademarks

6 Terminology

PWM— Pulse width modulation

BLDC— Brushless DC motor

MCU— Microcontroller unit

MOSFET— Metal–oxide–semiconductor field-effect transistor

IGBT— Insulated gate bipolar transistor

ESD— Electrostatic discharge

RPM— Rotation per minute

RMS— Root mean square

7 About the Author

BRIAN DEMPSEY is a systems designer at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Brian brings to this role his extensive experience in HVAC systems, along with his experience with mixed signal systems. Brian earned his bachelor of science in electrical engineering (BSEE) from Texas A&M University in College Station, TX. Brian is a member of the Institute of Electrical and Electronics Engineers (IEEE).

Revision A History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2016) to A Revision	Page
• Changed language and images to fit current style guide	1

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