TI Designs

12-Bit, 20-MSPS Data Acquisition Reference Design for Digitizers

Description

This reference design utilizes the ADS4122 ADC along with OPA656 and THS4541 amplifiers to develop a 12-bit, 20-MSPS digitizer for the BeagleBone Cape form factor. This expansion board interfaces with the BeagleBone Black development platform, which is a low-cost, open source, community-supported environment based on the ARM® Cortex®-A8 processor. This design shows a cost-effective and low-power data acquisition system (DAQ) that provides an alternative to FPGA-based systems and features a single-ended, high-impedance input that can be used in a wide number of applications including portable instrumentation and digitizers.

Resources

TIDA-00942	Design Folder
ADS4122	Product Folder
OPA656	Product Folder
THS4541	Product Folder
Sitara™ AM335x	Product Folder

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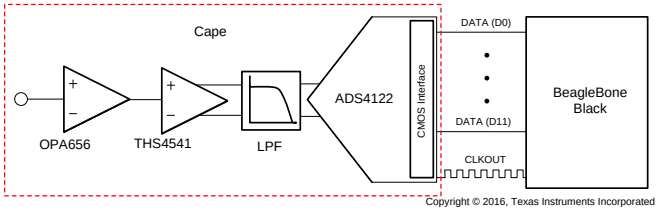
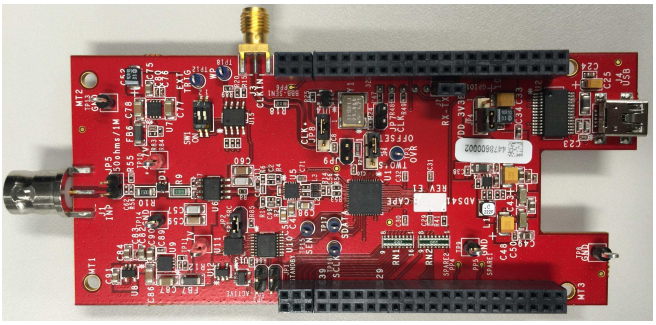
Features

- Single-Ended-to-Differential Digitizer Reference Design Using OPA656 and THS4541
- DC-Coupled Signal Path (0 MHz to 9 MHz)
- Low-Power Operation (330 mW)
- 2-V_{P-P} Input Voltage Range
- Option to Choose Between 50-Ω or 1-MΩ Input Impedance
- Available, Onboard 20-MHz Crystal Oscillator Option for External Clocking
- Low System Cost; BeagleBone Black (BBB) Sitara™ Processor Reduces System Cost Over FPGA-Based Solutions.

Applications

- Portable Instrumentation
- Low-Power Data Acquisition
- Industrial Sensor Data Analyzers
- Oscilloscopes





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1 System Overview

1.1 System Description

This design demonstrates a low-power, 20-MSPS digitizer signal-chain based on the ADS4122 ADC and BeagleBone Black (BBB) development platform. This design includes an OPA656 high-input impedance buffer, THS4541 single-ended-to- differential converter, antialiasing filtering, and digital interfacing.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATIONS
Input signal voltage range	2-V_{P-P}
Resolution	12-bit
Sample rate	20 MSPS
Input signal bandwidth	9 MHz
Power consumption	330 mW
Output data rate	20 MSPS
Supply voltage	5 V (USB bus or externally powered)

1.3 Block Diagram

Figure 1 shows the block diagram for the reference design which is composed of a high-input impedance junction gate field-effect transistor (JFET) input buffer (OPA656), single-ended-to-differential converter (THS4541), second-order 9-MHz low-pass antialiasing filter, and 12-bit 20-MSPS ADS4122 analog-to-digital converter (ADC) . The parallel CMOS output of the ADC is connected to the BeagleBone Black through the cape interface connectors. Section 2 describes these components in more detail.

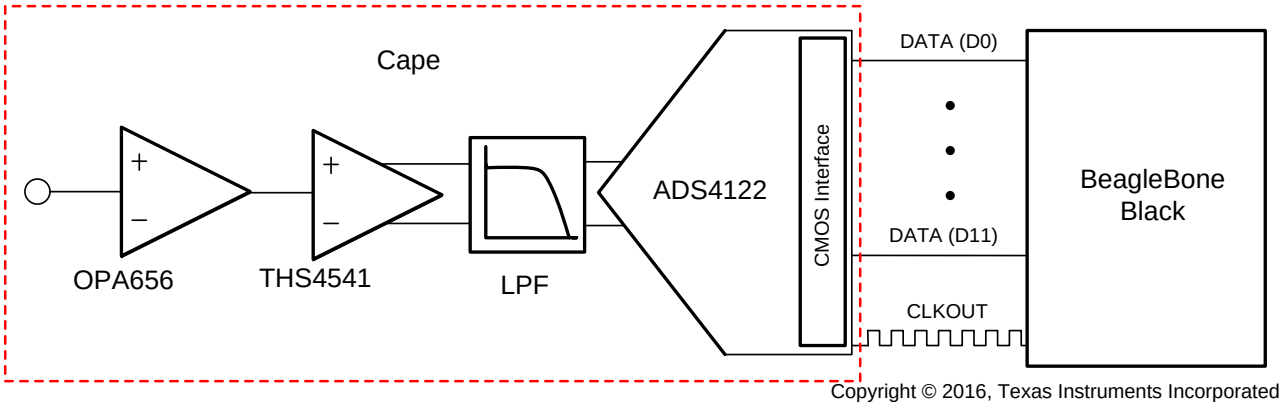

Figure 1. TIDA-00942 Block Diagram

1.4 Highlighted Products

1.4.1 ADS4122

ADS4122 is member of the ADS41xx family of ADCs. These devices provide high dynamic performance while consuming extremely low power at a 1.8-V supply. ADS4122 ADCs have fine gain options that can be used to improve spurious-free dynamic range (SFDR) performance at lower full-scale input ranges, especially at high input frequencies. The ADS4122 includes a DC offset correction loop that can be used to cancel the ADC offset. At lower sampling rates, the ADC automatically operates at a scaled-down power mode without any loss in performance, which makes it suitable for low-power applications.

1.4.2 OPA656

The OPA656 is a wideband, unity-gain stable, voltage-feedback operational amplifier with a JFET-input stage to offer an ultra-high dynamic-range amplifier for ADC buffering and transimpedance applications. The device provides extremely low DC error and provides high precision in optical applications. The high unity-gain stable bandwidth and JFET input allows exceptional performance in high-speed, low-noise applications.

1.4.3 THS4541

THS4541 is low-power, voltage-feedback, fully differential amplifier (FDA) with an input common-mode range below the negative rail and rail-to-rail output. The amplifier has been designed for low-power data acquisition systems where high density is critical in a high-performance ADC. The THS4541 features the negative-rail input required when interfacing a DC-coupled, ground-centered source signal. This negative-rail input, with rail-to-rail output, allows for easy interface between single-ended, ground-referenced, bipolar signals.

2 System Design Theory

This reference design demonstrates the implementation of a low-cost, low-power, data capture solution, which can be used in industrial sensor measurement systems. This fully self-contained BeagleBone Black cape houses an optimized analog front-end (AFE) signal chain and ADC.

2.1 Design Theory

The AFE for this cape design combines a high-impedance input buffer, single-ended-to-differential converter, and a 9-MHz second-order low-pass Bessel filter.

Two main parameters must be considered for the AFE design:

- Allowed maximum analog input voltage for the ADC is 2-V_{P-P}
- Targeted bandwidth for First Nyquist operation is 10 MHz

Based on these requirements, the acceptable input signal can be 2-V_{P-P}. In this design, the OPA656 device is set up to accept ±1 V and design it with a gain of 1.8 V/V. This setting provides 3.6-V_{P-P} to the fully-differential amplifier stage, which will be brought down to 1.8-V_{P-P}, max input for the ADC. The 2-V_{P-P} (0-dBFS) input voltage is brought down to1.8-V_{P-P} (–1-dBFS) to prevent saturation of the ADC.

Figure 2 shows the circuit diagram from the OPA656 input buffer, which is operated in a non-inverting configuration with a gain of +1.8 V/V. The input impedance is jumper-selectable between 1 MΩ or 50 Ω and has an overdrive protection clamp based on the BAV99 diode pair, which can clamp transients up to ±50 V. The 150 Ω between the input and diode pair limits the current into the diodes and is followed by an additional 50 Ω, which ensures that most clamped transient current flows through the external diodes and not the OPA656 electrostatic discharge (ESD) cells. The combined response of the input circuit as shown in Figure 3 serves to limit the bandwidth to 100 MHz, which limits high-frequency noise.

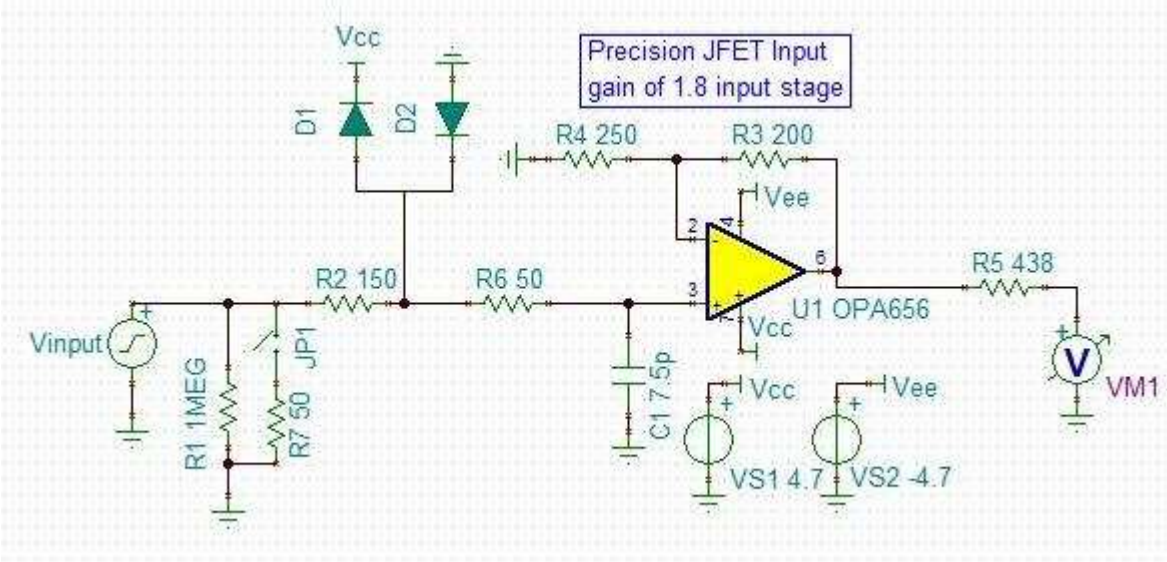

Figure 2. Circuit for Input Buffer Stage (OPA656)

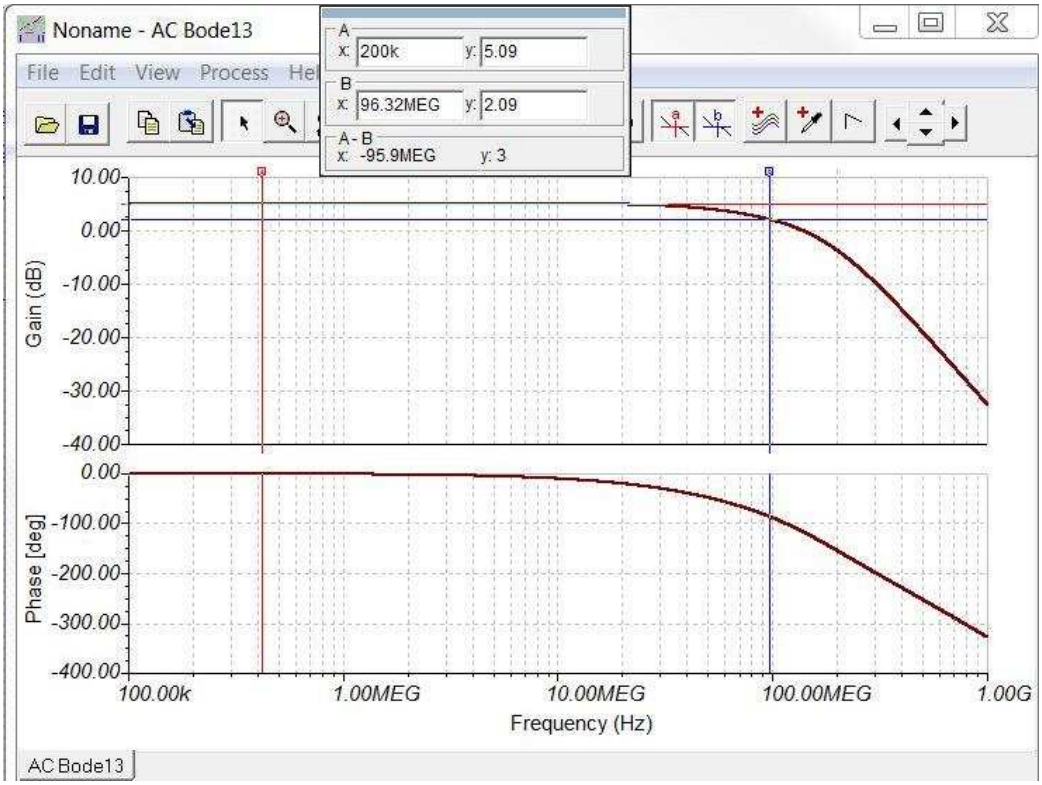

Figure 3. Frequency Response of Input Buffer Stage (OPA656)

As Figure 4 shows, the output of the OPA656 device is converted from single-ended to differential by the THS4541 fully differential amplifier (FDA). This amplifier also acts as a second-order, multi-feedback (MFB) based low-pass filter with a cutoff frequency of 13 MHz. To achieve the required 1.8-V_{P-P} signal level at the ADC input, the combined response of the FDA and following, passive low-pass filter must have a –6 dB gain. A –5 dB is implemented in the FDA with the remaining 1 dB coming from the passive filter. Figure 5 shows the combined frequency response of the FDA and MFB low-pass filter. For more information on how to design the active filter stage, refer to the *Design Methodology for MFB filters in ADC Interface Applications* report [1].

A second-order low-pass RLC filter is implemented right before the input of the ADC and after the single-ended-to-differential stage amplifier. The low-pass filter has been designed to have a cutoff frequency of 7.24 MHz and insertion loss of –1dB. For detailed information on how to design the passive filter see the *RLC Filter Design for ADC Interface Applications* report [2].

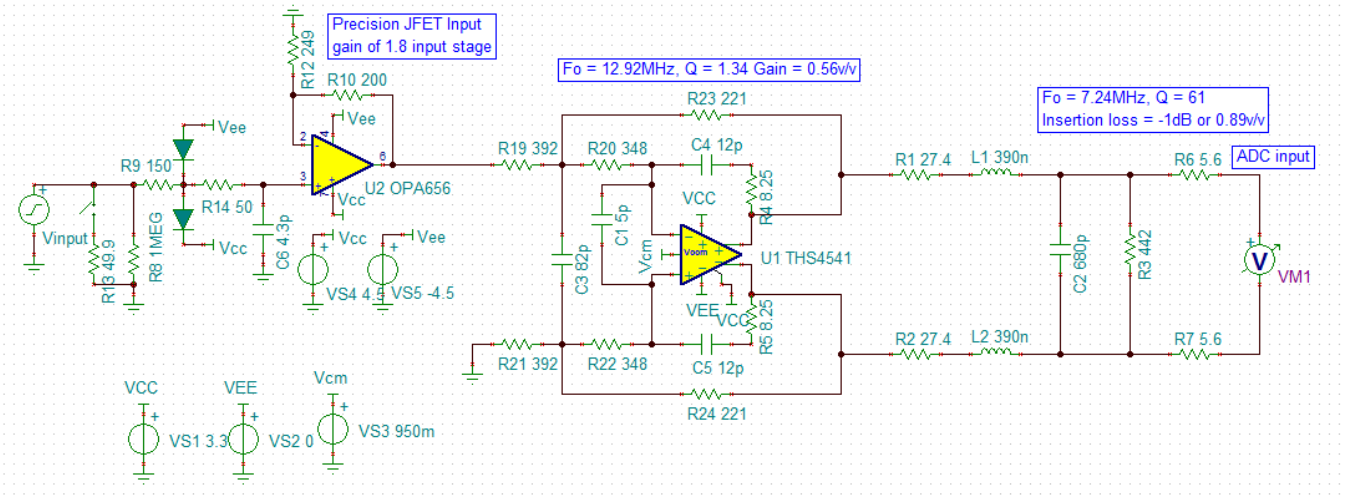

Figure 4. Input Circuit With OPA656, THS4541, and Low-pass Filter

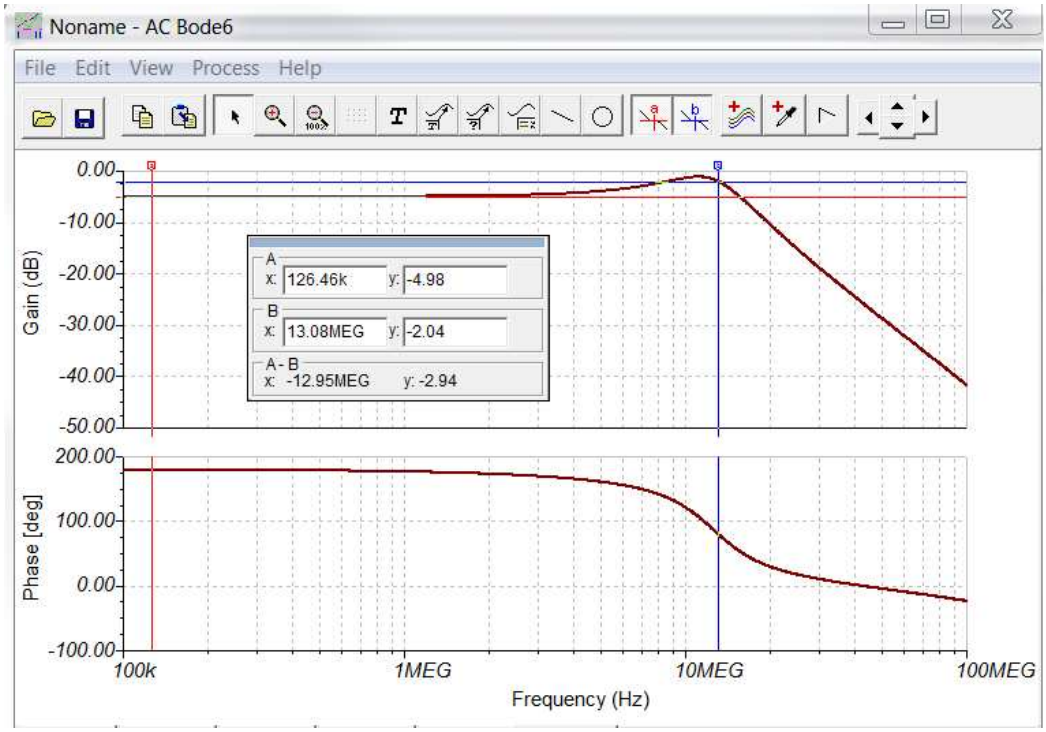

Figure 5. Frequency Response of FDA (THS4541) and MFB Low-pass Filter

Figure 6 shows the overall frequency response of the input buffer stage, FDA with MFB low-pass filter, and RLC low-pass filter.

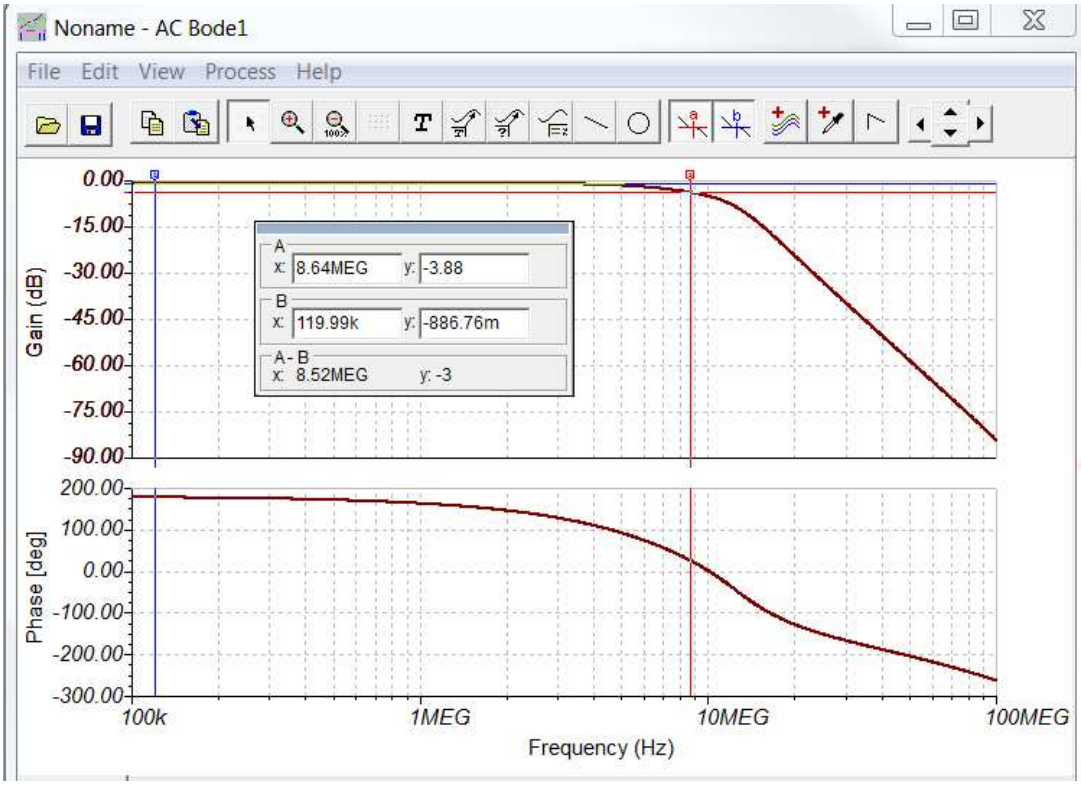

Figure 6. Frequency Response of Input Circuit

3 Getting Started Hardware and Software

3.1 Hardware

Figure 7 shows the cape board plugs on top of the BBB. By default, all the jumpers on the cape board have been set up to make the cape board function without any register configuration from the BBB. By default, the cape board utilizes the onboard 20-MHz oscillator to clock the ADC. An option also exists to provide an external clock through connector J3. If an external clock is desired, the jumper JP8 must be moved from pin 1-2 to pin 2-3, and jumper JP9 must be installed.

By default, the cape board has been designed to provide a 1-MΩ termination with an optional 50-Ω input resistance for a 50-Ω source. The input resistance can be selected by installing (50 Ω) and uninstalling (1 MΩ) jumper JP5 on the board.

The cape draws its power from the BBB, which can either be powered by the USB 5 V or the DC input jack. By default, the cape has been set up to draw power from the VDD_5V pin (jumper JP4 at pin 1-2). If powering the BBB through USB, then the cape board must be configured to draw power from SYS_5V pin (JP4 at pin 2-3).

The ADS4122 device on the cape board can be configured through either onboard jumpers or through the serial peripheral interface (SPI). By default, the ADC is setup to be configured through jumpers. To control ADS4122 using ADS4122 software graphical user interface (GUI), install the jumper JP3 (SPI-ACTIVE) and remove the jumper JP2 (SPI-SRC). An option also exists to configure the ADC using SPI signals from the BBB. To control the ADC using a BBB, the designer must install both the jumper JP3 (SPI-ACTIVE) and JP2 (SPI-SRC).

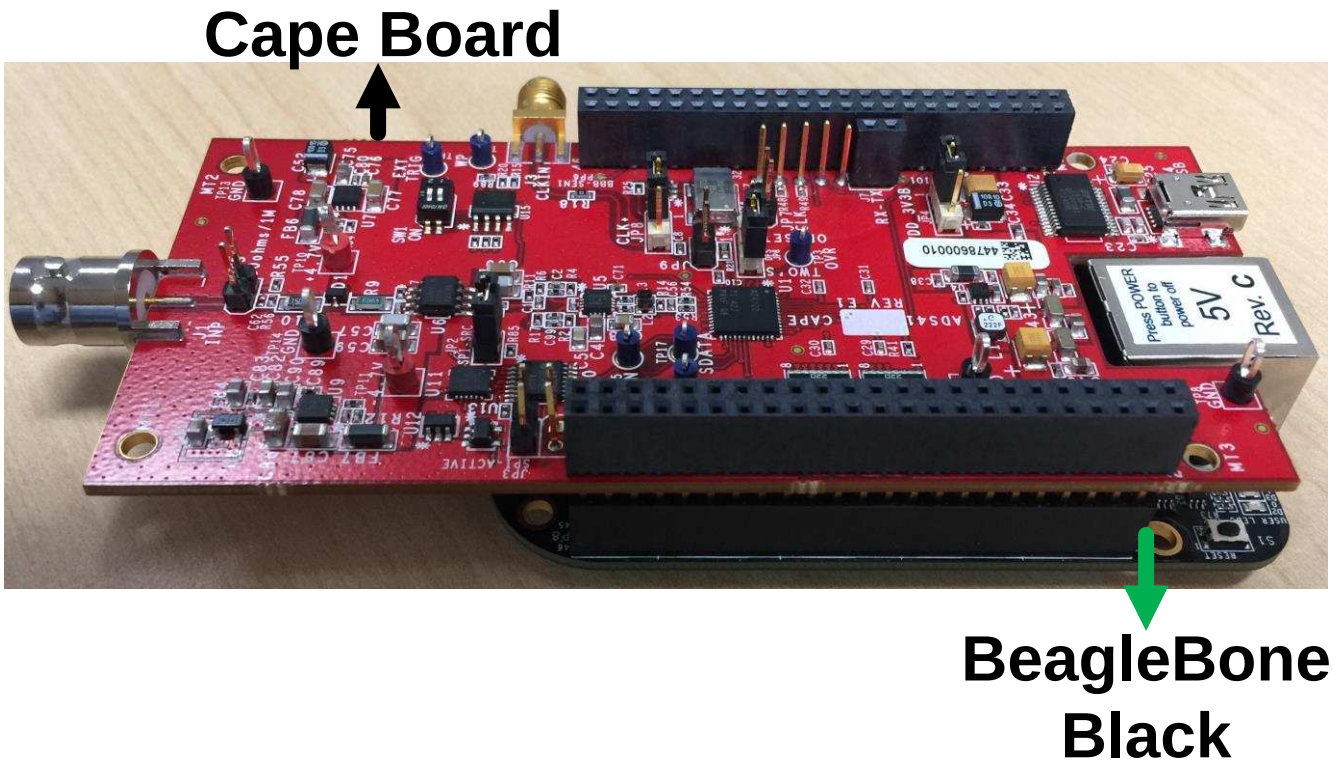

Figure 7. Stacked view of cape and BeagleBone Black

3.2 Software

3.2.1 ADS4122 GUI

The ADS4122 GUI is used to configure the ADC. Refer to the ADS4122 tool folder at http://www.ti.com/tool/ads4122evm for a detailed description on how to use the GUI.

3.2.2 HSDC Pro GUI

HSDC Pro software is used to analyze the digital data captured by the BBB. Refer to the HSDC Pro tool folder at http://www.ti.com/tool/dataconverterpro-sw for a detailed description on how to use the GUI.

3.2.3 BeagleBone Black Data Capture Application

A BeagleBone Black is used to capture data from the ADC. The main processor of the device is the Sitara AM335x, which has a separate co-processor called the Programmable Real-Time Unit Subsystem and Industrial Communication Subsystem (PRU-ICSS) that directly connects to the ADC output. The programmable PRU-ICSS captures 12-bit samples every clock cycle from the ADC and buffers the data into internal memory. The Cortex-A8 on the AM335x then moves the data into its own allocated memory and finally creates a text file of the data samples in its file system. Then access the data file through USB or serial port and run post processing. For further information, contact the Sitara applications team on the Sitara processor E2E forum.

4 Testing and Results

In this section a variety of measurements have been performed to demonstrate the performance of the cape board and describe the process. The cape board is plugged **into** the BeagleBone Black, which captures the data generated by the ADC. The data is analyzed using the HSDC Pro software. Performance measurements have been made on filtered input signals connected to the BNC connector (J1) on the cape.

Figure 8 shows the frequency domain performance of the cape board. A fast Fourier transform (FFT) was performed on a 1-MHz, –1-dBFS input signal. The resulting SNR is 70.5 dB and the SFDR is 71 dB.

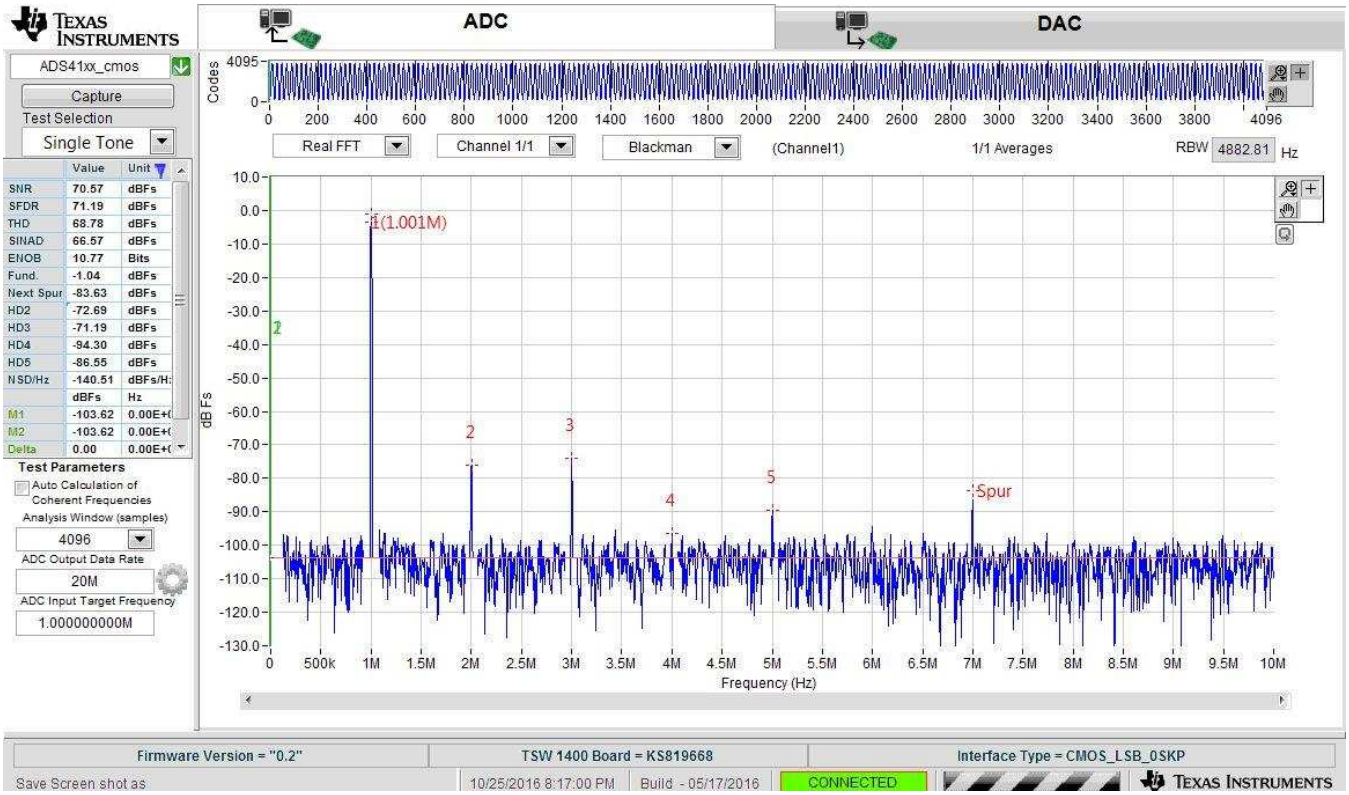

Figure 8. FFT 1-MHz –1-dBFS Input Signal

Figure 9 and Figure 10 show the results when a 100-KHz and 1-MHz, ±1-V square wave has been applied at the input of cape board.

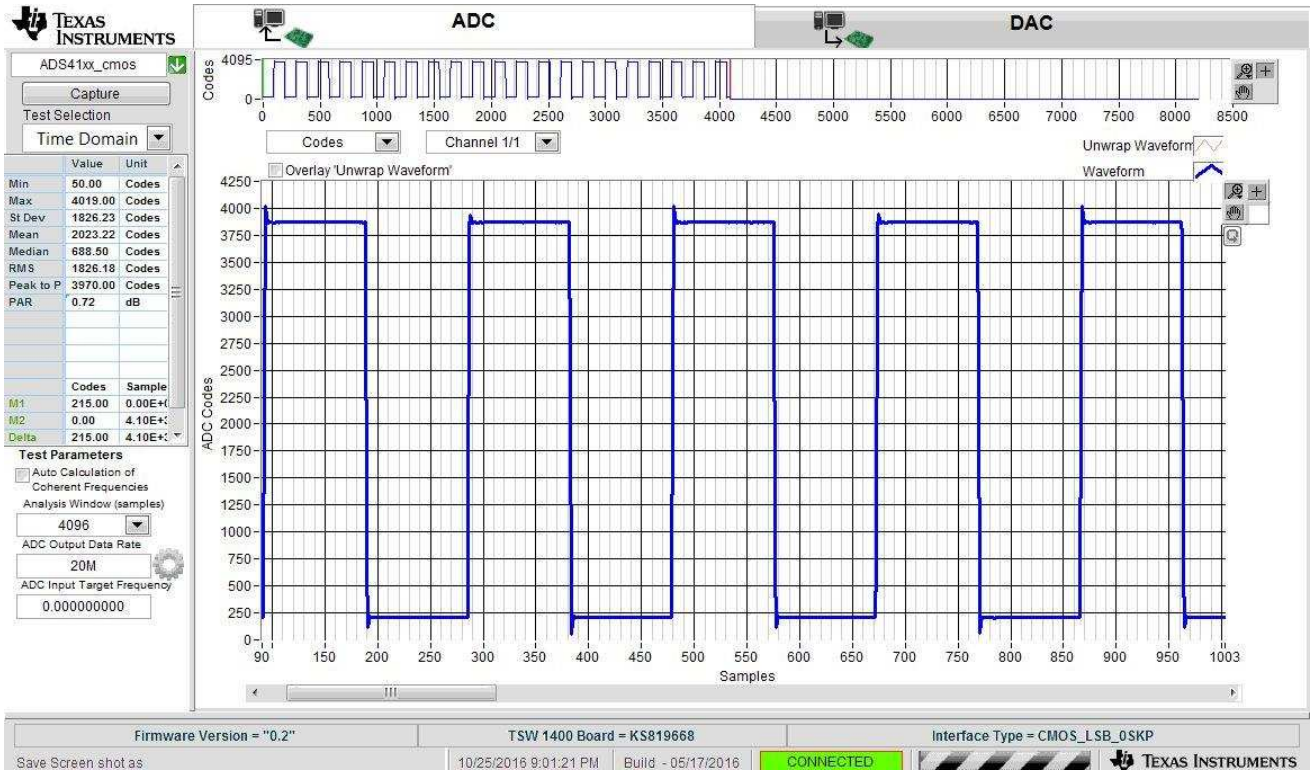

Figure 9. 100-KHz Square Wave Input

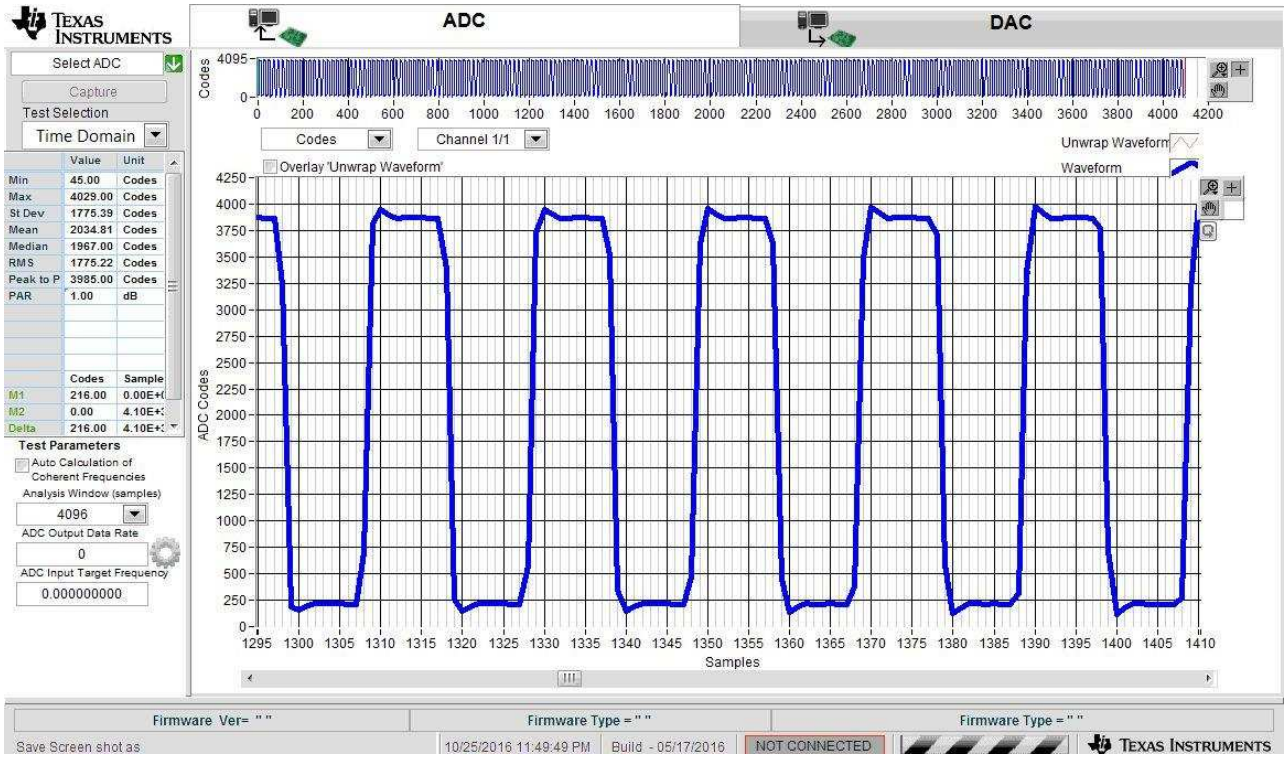

Figure 10. 1-MHz Square Wave Input

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00942.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00942.

5.3 PCB Layout Recommendations

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00942.

5.4 Gerber Files

To download the Gerber files, see the design files at TIDA-00942.

5.5 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00942.

6 Software Files

To download the software files, see the design files at TIDA-00942.

7 References

1. Texas Instruments, *Design Methodology for MFB Filters in ADC Interface Applications*, Application Report (SBOA114)
2. Texas Instruments, *RLC Filter Design for ADC Interface Applications*, Application Report (SBAA108)

8 About the Author

NEERAJ GILL is a part of the applications team in the high speed catalog converters group at the Texas Instruments. Neeraj received his BSEE from University of New Hampshire in 2011 and then his Masters in Electrical Engineering also from University of New Hampshire in 2013.

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