TI Designs

TIDA-00887: Automotive Dual-Port 2.4 A USB Hub Reference Design with Short-to-Battery Protection

The TIDA-00887 is comprised of a two-port USB 2.0 hub with short-to-battery (STB) and short-circuit protection on both downstream ports provided by the TPD3S716-Q1. Both downstream ports are configured either as a custom divider mode or a dedicated charging port (DCP) provided by the TUSB4020BI-Q1 USB2.0 hub if no upstream device is connected. When an upstream is connected, the TUSB4020 hub will support charging via CDP. The ports automatically switch between divider mode, CDP mode, and DCP mode depending on the portable devices connected in order to provide the fastest charging rate to the connected device.

Resources

TIDA-00887	Design Folder
TPD3S716-Q1	Product Folder
TUSB4020BI	Product Folder
TPS7A4533	Product Folder
TPS74801	Product Folder
LMR14050	Product Folder

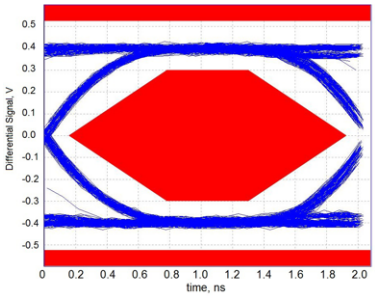
TI E2E™ Community — ASK Our E2E Experts

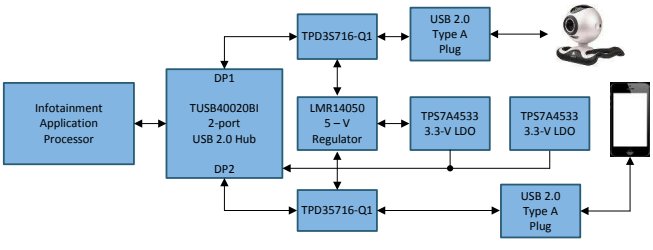
Features

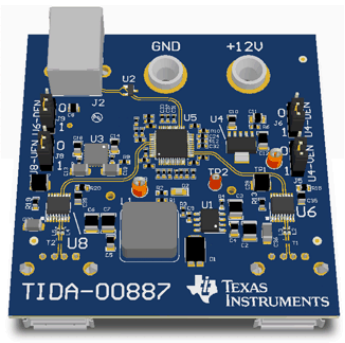
- Fully functional USB Hub with short-to-battery protection and BC1.2 charge detection
- Supports USB 2.0 High-Speed Data Rates
- Short-to-Battery Protection (up to 18 V) on V_{BUS_CON}, VD+, VD-
- Short-to-Ground Protection on V_{BUS_CON} for both downstream ports
- Adjustable Overcurrent Protection Current Limit up to 2.4 A
- IEC 61000-4-2 (Level 4) and ISO 10605 system level ESD protection at VBUS_CON, VD+, VD-

Applications

- Remote USB 2.0 Ports Where Short-to-Battery (STB) is a Concern
  - Media Connection Modules
  - Head Units With Remote USB Ports
  - Rear Seat Entertainment







An IMPORTANT NOTICE at the end of this TI reference design addresses authorized use, intellectual property matters and other important disclaimers and information.

1 System Overview

1.1 System Description

The TIDA-00887 is a two port automotive USB hub reference design with additional functions key to the automotive USB hub design. This board features integrated charge detection, current limiting up to 2.4-A, short-to-battery protection, and ESD protection on both downstream ports. The upstream port may be connected to a head unit's downstream port to provide a data path for attached peripheral devices.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
STB response time	TPD3S716-Q1 shuts off in 2 µs to protect the system from up to 18-V STB	See Section 1.4.1
ESD protection	±8-kV contact and ±15-kV air-gap per IEC 61000-4-2	See Section 1.4.1
Overcurrent protection	TPD3S716-Q1 limits current on V_{BUS} up to 2.4 A	See Section 1.4.1

1.3 Block Diagram

This automotive USB 2.0 hub with STB protection has two downstream ports (DPs). Each DP is protected by the TPD3S716-Q1. An external 12-V DC power supply provides power to the USB 2.0 hub circuitry through a step-down (buck) regulator, the LMR14050-Q1, which steps down the 12-V to provide a 5-V rail for the two low-dropout regulators (LDOs) and V_{BUS} for the TPD3S716-Q1s to supply the DPs. The LDO TPS7A4533 provides the 3.3-V rail, and the LDO TPS74801-Q1 provides the 1.1-V rail. The upstream port (UP) data lines are protected against ESD by the TPD2E2U06-Q1.

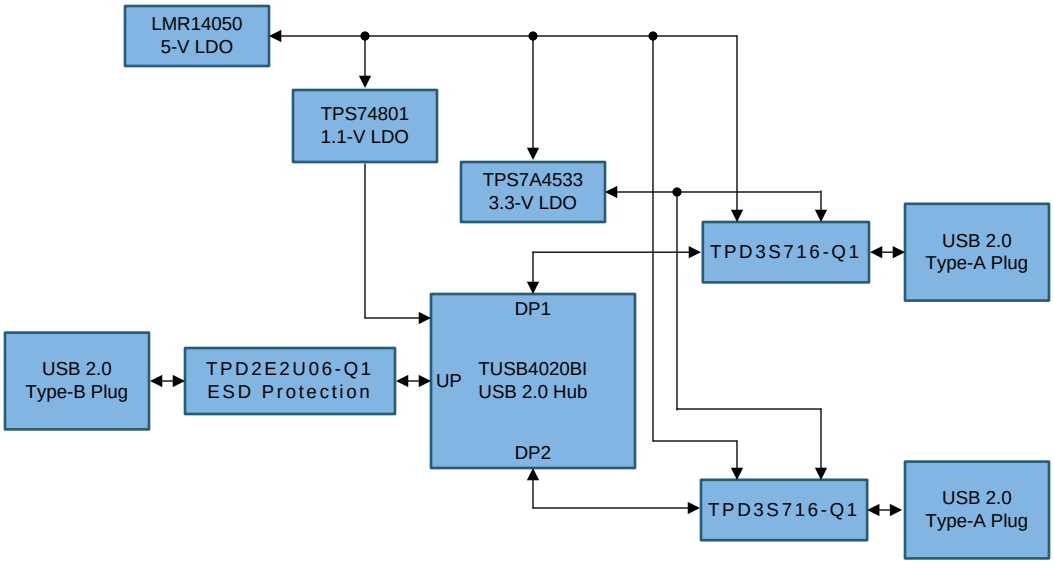


Figure 1. Block Diagram

1.3.1 LMR14050-Q1

- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40 to 125°C ambient operating temperature range
  - Device HBM ESD classification level H1C
  - Device CDM ESD classification level C4A
- 4- to 40-V input range
- 5-A continuous output current
- Ultra-low 40-µA operating quiescent current
- 90-mΩ high-side MOSFET
- Minimum switch-on time: 75 ns
- Adjustable switching frequency from 200 kHz to 2.5 MHz
- Frequency synchronization to the external clock
- Spread-spectrum option for reduced electromagnetic interference
- Internal compensation for ease of use
- High-duty cycle operation supported
- Precision-enable input
- 1-µA shutdown current
- External soft-start
- Thermal, overvoltage, and short protection
- 8-Pin HSOIC with PowerPAD™ Package

1.3.2 TPS7A4533

- Optimized for fast transient response
- Output current: 1.5 A
- High output voltage accuracy: 1% at 25°C
- Dropout voltage: 300 mV
- Low noise: 35 μV_{RMS} (10 Hz to 100 kHz)
- High ripple rejection: 68 dB at 1 kHz
- 1-mA quiescent current
- Controlled quiescent current in dropout
- Less than 1-µA quiescent current in shutdown
- Stable with 10-µF ceramic output capacitor
- Reverse-battery protection
- Reverse-current protection

1.3.3 TPS74801-Q1

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
  - Device temperature grade 1: –40 to 125°C ambient operating temperature range
  - Device HBM ESD classification level H2
  - Device HBM ESD classification level C4B
- V_{OUT} Range: 0.8 to 3.6 V
- Ultra-low V_{IN} Range: 0.8 to 5.5 V
- V_{BIAS} Range 2.7 to 5.5 V
- Low dropout: 60-mV typ at 1.5 A, V_{BIAS} = 5 V
- 2% accuracy over line, load, and temperature

- Programmable soft-start provides linear-voltage startup
- V_{BIAS} Permits Low V_{IN} operation with good transient response
- Stable with any output capacitor ≥ 2.2 µF
- Available in small 3-mm × 3-mm × 1-mm SON-10, and 5 × 5 QFN-20 Packages

1.3.4 TPD2E2U06-Q1

- IEC 61000-4-2 level 4 ESD protection
  - ±25-kV contact discharge
  - ±30-kV air-gap discharge
- ISO 10605 (330 pF, 330 Ω) ESD protection
  - ±20-kV contact discharge
  - ±25-kV air-gap discharge
- IO capacitance of 1.5 pF (typ)
- DC breakdown voltage 6.5 V (minimum)
- Ultra-low leakage current of 10 nA (maximum) and 0.1 nA (typ)
- Low ESD clamping voltage
- Industrial temperature range: –40°C to +125°C
- Easy routing DBZ and DCK packages

1.4 Highlighted Products

1.4.1 TPD3S716-Q1

The TPD3S716-Q1 is a single-chip solution for short-to-battery, short-circuit, and ESD protection with an adjustable current-limit for the USB connector's V_{BUS} and data lines in automotive applications. The integrated data switches provide 1 GHz bandwidth for minimal signal degradation while simultaneously providing 18-V short-to-battery protection.

The STB protection protects against shorts up to 18 V, in both hot-plug and DC events. The over-voltage protection reacts very quickly, shutting off the switches and protecting the upstream transceiver from harmful voltage and current spikes. The integrated ESD protection provides system-level IEC 61000-4-2 Level 4 protection. The adjustable overcurrent protection automatically limits current to 2.4 A, allowing support for charging USB BC1.2, USB Type-C 5V/1.5A, and proprietary charging schemes up to 2.4 A. The separate enable pins for data and V_{BUS} allow for both host and client or OTG mode.

Key features:

- AEC-Q100 qualified (grade 1)
  - –40 to 125°C operating temperature range
- STB protection, up to 18 V, on V_{BUS_CON}, VD+, VD–
- Short-to-ground protection on V_{BUS_CON}
- Short-to-bus protection on VD+, VD–
- ESD protection on V_{BUS_CON}, VD+, VD–
  - ±8 kV contact discharge (IEC 61000-4-2)
  - ±15 kV air-gap discharge (IEC 61000-4-2)
- Low R_{ON} nFET V_{BUS} Switch
- High-speed data switches
- Hiccup current limit
  - Adjustable up to 2.4 A
- Independent V_{BUS} and data enable pins for configuring both host and Client or USB On-The-Go mode
- Fault output signal
- Thermal shutdown feature

- 16-pin DBQ package (3.9 mm × 4.94 mm)
- STB response time of 2 µs (Typ) for V_{BUS}, and 200 ns for the data path

1.5 TUSB4020BI-Q1

The TUSB4020BI-Q1 is a two-port USB 2.0 hub. It provides USB high-speed/full-speed connections on the UP, and provides high-speed, full-speed, or low-speed connections on the two DPs. When the UP is connected to an electrical environment that supports high-speed and full-speed/low-speed connections, high-speed and full-speed/low-speed USB connectivity is enabled on the DPs. When the UP is connected to an electrical environment that only supports full-speed/low-speed connections, high-speed connectivity is disabled on the DPs. Battery charging support includes both divider mode and DCP.

Key features:

- Two-port USB 2.0 hub
- USB 2.0 hub features:
  - Multi-transaction translator (MTT) hub: two transaction translators
  - Four asynchronous endpoint buffers per transaction translator
- Per port or ganged power switching, and overcurrent notification inputs
- One-time programmable (OTP) ROM, serial EEPROM, or I^2C or SMBus slave interface for custom configurations:
  - Vendor ID (VID) and product ID (PID)
  - Port customization
  - Manufacturer and product strings (not by OTP ROM)
  - Serial number (not by OTP ROM)
- Application feature selection using terminal selection, EEPROM or I^2C or SMBus slave interface
- Provides 128-bit universally unique identifier (UUID)
- Supports onboard and in-system OTP or EEPROM programming through the USB 2.0 UP
- Single clock input, 24-MHz crystal or oscillator
- No special driver requirements (works seamlessly on any operating system with USB stack support)
- 48-pin HTQFP package (PHP)

2 System Design Theory

The TIDA-00887 two-port automotive USB 2.0 hub with STB and short-circuit protection highlights the TPD3S716-Q1 and provides USB 2.0 DP protection against STB, short-circuit, IEC 61000-4-2 ESD Level 4, and overcurrent. Battery charging support includes both divider and dedicated charging port (DCP) modes. The DCP mode is compliant with the Chinese Telecommunications Industry Standard YD/T 1591-2009.

2.1 Downstream Ports

Figure 2 shows two TPD3S716-Q1s (U6 and U8) connected to the TUSB4020BI-Q1 downstream data lines, which follows the data sheet guidelines of the TPD3S716-Q1.

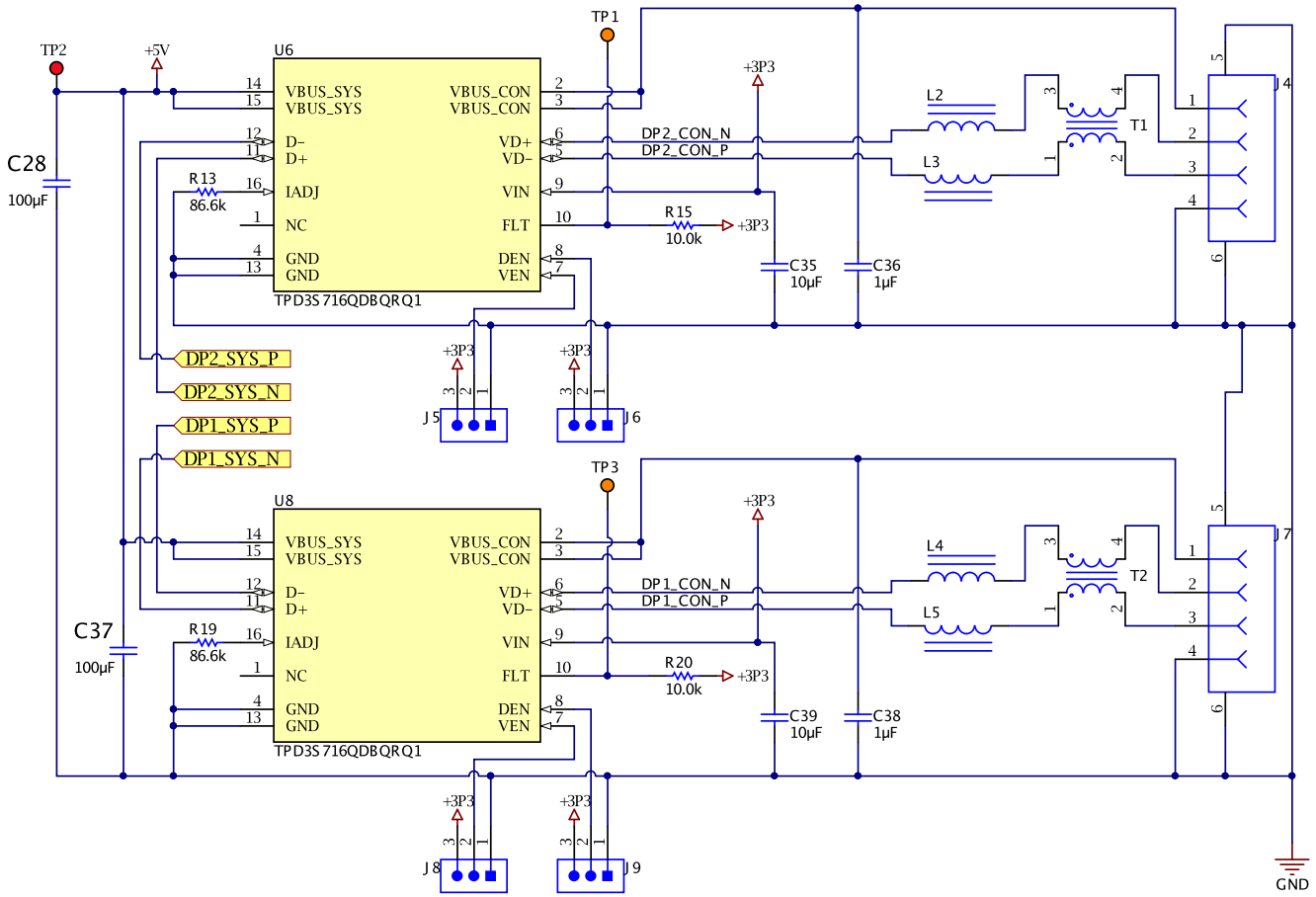


Figure 2. TPD3S716-Q1 Protecting Downstream Ports

2.2 TUSB4020BI-Q1

The TUSB4020BI-Q1 is a two-port USB 2.0-compliant hub device. The device provides high-speed and full-speed connections on the UP. The TUSB4020BI-Q1 also supports high, full, or low-speed connections on the DPs. When the UP connects to an environment that supports only full and low-speed connections, high-speed is disabled on the DPs. The hub's individual port power switching is not used due to the TPD3S716-Q1 overcurrent limiter, which provides the two-port protection scheme. The USB 2.0 hub is configured with the de-assertion of RESET.

Figure 3, shows the TUSB4020BI-Q1 (U5) configuration. Only connected pins are shown.

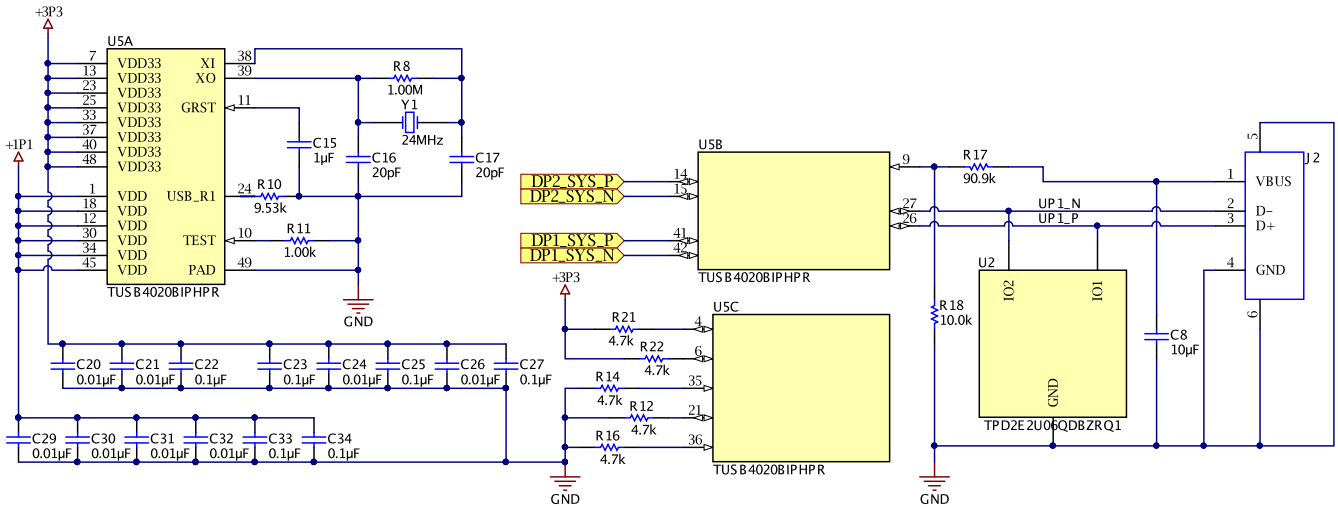


Figure 3. TUSB4020BI-Q1 Schematic

2.3 LMR14050-Q1

Figure 4 shows the LMR14050-Q1 (U1) configured for a 5-V output capable of 3.5 A. An 18-V external AC-DC converter supplies the input power. The 5-V output rail supplies the 3.3-V LDO TPS7A4533 and 1.1-V LDO TPS74801. An LED diode (D3) indicates when the power rail becomes active.

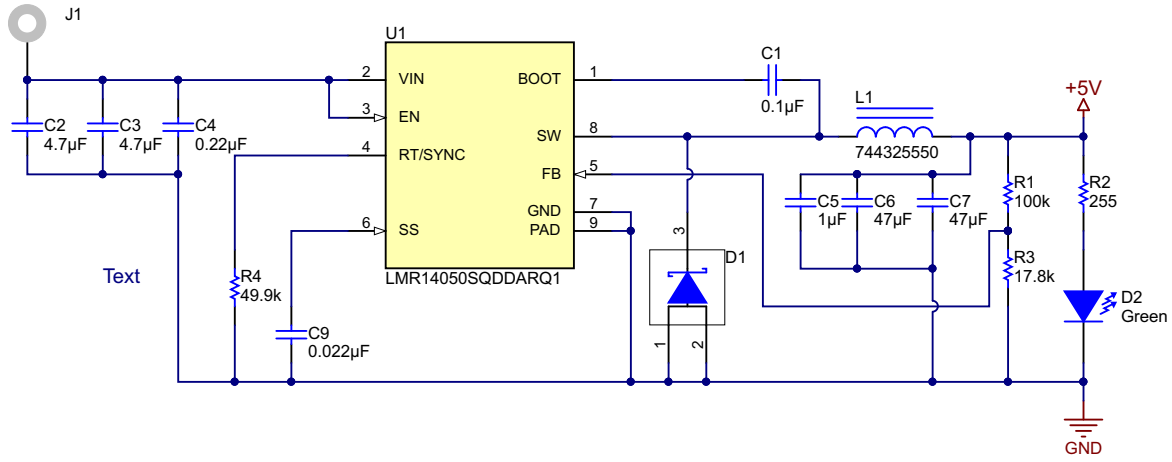


Figure 4. LMR14050 Step Down (Buck) Regulator Schematic

2.3.1 Output Voltage Selection

The internal voltage reference produces a precise 0.75-V (typical) voltage reference over the operating temperature range. The output voltage is set by a resistor divider from the output voltage to the FB pin. It is recommended to use divider resistors with 1% tolerance or better, and a temperature coefficient of 100 ppm or less. Select the high-side resistor R_{FBT} (R2) for the desired divider current, and use Equation 1 to calculate low-side R_{FBB} (R3). Larger value divider resistors are good for efficiency at light load. However, if the values are too high the regulator is more susceptible to noise, and voltage errors from the FB input current may become noticeable. R_{FBB} in the range from 10 to 100 kΩ are recommended for most applications.

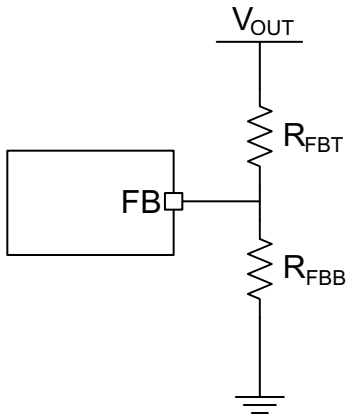


Figure 5. Output Voltage Setting

$$R_{FBB} = 0.75 / V_{OUT} – .75 \times R_{FBT} \quad (1)$$

Choosing R_{FBT} = 100 kΩ and V_{OUT} = 5 V, gets R_{FBB} = 17,647Ω. Choose a standard value of 17.8 kΩ.

2.3.2 Switching Frequency

For a desired frequency, use Equation 2 to calculate the required value for R_T (R1).

$$R_T(K\Omega) = 42904 \times f_{sw}(kHZ)^{-1.088} \quad (2)$$

This design uses a switching frequency of 500 kHz. For 500 kHz, the calculated R_T is 49.66 kΩ, and a standard value of 49.9 kΩ can be used to set the switching frequency at 500 kHz.

2.3.3 Output Inductor Selection

The most critical parameters for the inductor are the inductance, saturation current, and the RMS current. The inductance is based on the desired peak-to-peak ripple current, Δi_L. Because the ripple current increases with the input voltage, the maximum input voltage is always used to calculate the minimum inductance, L_{MIN}. Use Equation 4 to calculate the minimum value of the output inductor. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. A reasonable value of K_{IND} should be 20 to 40%. During an instantaneous short or overcurrent operation event, the RMS and peak inductor current can be high. The inductor current rating should be higher than the current limit.

$$\Delta i_L = V_{OUT} \times (V_{IN\_MAX} – V_{OUT}) / V_{IN\_MAX} \times L \times f_{SW} \quad (3)$$

$$L_{MIN} = V_{IN\_MAX} – V_{OUT} / I_{OUT} \times K_{IND} \times V_{OUT} / V_{IN\_MAX} \times f_{SW} \quad (4)$$

In general, it is preferable to choose lower inductance when switching power supplies because it usually corresponds to a faster transient response, smaller DCR, and reduced size for more compact designs. However, too low of an inductance can generate too large of an inductor current ripple where overcurrent protection at the full load could be falsely triggered. Lower inductance also generates more conduction loss because the RMS current is slightly higher. Larger inductor current ripple also implies larger output voltage ripple with the same output capacitors. With peak current mode control, it is not recommended to have too small of an inductor current ripple. A larger peak current ripple improves the comparator signal-to-noise ratio. For this design example, choose K_{IND} = 0.4, the minimum inductor value is calculated to be 6.12 µH, and the nearest standard value above that is chosen 6.5 µH. Use a standard 6.5-µH ferrite inductor (L1) with a capability of 5-A RMS current and 7-A saturation current.

2.3.4 Output Capacitor Selection

The output capacitor(s), C_{OUT} (C5, C6, C7), should be carefully chosen because they directly affect the steady-state output voltage ripple, loop stability, and the voltage overshoot and undershoot during load current transients. The output ripple is essentially composed of two parts. One part is caused by the inductor current ripple going through the equivalent series resistance (ESR) of the output capacitors:

$$\Delta V_{OUT\_ESR} = \Delta i_L \times ESR = K_{IND} \times I_{OUT} \times ESR \quad (5)$$

The other part is caused by the inductor current ripple charging and discharging the output capacitors:

$$V_{OUT\_C} = \Delta i_L / 8 \times f_{SW} \times C_{OUT} = K_{IND} \times I_{OUT} / 8 \times f_{SW} \times C_{OUT} \quad (6)$$

The two components in the voltage ripple are not in phase, so the actual peak-to-peak ripple is smaller than the sum of the two peaks. Output capacitance is usually limited by transient performance specifications if the system requires tight voltage regulation with the presence of large current steps and fast slew rate. When a fast large load increase happens, output capacitors provide the required charge before the inductor current can slew up to the appropriate level. The regulator's control loop usually needs three or more clock cycles to respond to the output voltage droop. The output capacitance must be large enough to supply the current difference for the three clock cycles to maintain the output voltage within the specified range.

Equation 7 shows the minimum output capacitance needed for a specified output undershoot. When a sudden large load decrease happens, the output capacitors absorb energy stored in the inductor. The catch diode can't sink current so the energy stored in the inductor results in an output voltage overshoot. Equation 8 calculates the minimum capacitance required to keep the voltage overshoot within a specified range.

$$C_{OUT} > 3 \times (I_{OH} - I_{OL}) / (f_{SW} \times V_{US}) \quad (7)$$

$$C_{OUT} > I^2_{OH} - I^2_{OL} / (V_{OUT} - V_{OS})^2 - V^2\_{OUT} \quad (8)$$

where:

- K_{IND} = ripple ratio of the inductor ripple current (ΔiL / IOUT)
- I_{OL} = low-level output current during load transient
- I_{OH} = high-level output current during load transient
- V_{US} = target output-voltage undershoot
- V_{OS} = target output-voltage overshoot

For this design example, the target output ripple is 50 mV. Presuppose $\Delta V_{OUT\_ESR} = \Delta V_{OUT\_C}$ = 50-mV, and chose K_{IND} = 0.4. Equation 5 yields ESR no larger than 35.7 mΩ and Equation 6 yields C_{OUT} no smaller than 7 µF. For the target over and undershoot range of this design, $V_{US} = V_{OS}$ = 5% × V_{OUT} = 250 mV. The C_{OUT} can be calculated to be no smaller than 75.6 µF and 30.8 µF by Equation 7 and Equation 8 respectively. In summary, the most stringent criteria for the output capacitor is 75.6 µF. Two 47-µF, 16-V, X7R ceramic capacitors (C6 and C7) with 5-mΩ ESR are used in parallel. A 1-µF, X7R, capacitor (C5) is also used for high-frequency filtering, placed as close as possible to the device pins.

2.3.5 Schottky Diode Selection

The preferred breakdown voltage rating of the diode is 25% higher than the maximum input voltage. The current rating for the diode should be equal to the maximum output current for the best reliability in most applications. In cases where the input voltage is much greater than the output voltage, the average diode current is lower. In this case it is possible to use a diode with a lower average current rating, approximately (1-*D*) × I_{OUT}, however the peak current rating should be higher than the maximum load current. A 4 to 5-A rated diode is a good starting point. For this design example, a 5-A, 60-V Schottky diode (D1) was chosen.

2.3.6 Input Capacitor Selection

The LMR14050-Q1 device requires high-frequency input decoupling capacitor(s) and a bulk-input capacitor, depending on the application. The typical recommended value for the high-frequency decoupling capacitor is from 4.7 to 10 µF. A high-quality ceramic capacitor, type X5R or X7R, with a sufficient voltage rating is recommended. To compensate the derating of ceramic capacitors, a voltage rating of twice the maximum input voltage is recommended. Additionally, some bulk capacitance can be required especially if the LMR14050-Q1 circuit is not located within approximately 5 cm from the input voltage source. This capacitor is used to provide damping to the voltage spike due to the lead inductance of the cable or the trace. For this design, two 4.7-µF, X7R ceramic capacitors (C2 and C3) rated for 50 V are used. A 0.22-µF, X7R ceramic capacitor (C4) rated for 50 V is also used for high-frequency filtering, which is placed as close as possible to the device pins.

2.3.7 Bootstrap Capacitor Selection

Every LMR14050-Q1 design requires a bootstrap capacitor, CBOOT (C1). The recommended capacitor is 0.1 µF and rated 16 V or higher, which are the values used in this design. The bootstrap capacitor is located between the SW pin and the BOOT pin. The bootstrap capacitor must be a high-quality ceramic type with an X7R or X5R grade dielectric for temperature stability. This design uses X7R.

2.4 TPS7A4533

Figure 6 shows the TPS7A4533 (U4) configured in this design. The LMR14050-Q1 supplies the V_{IN}. V_{OUT} is the VDD33 supply rail for the USB 2.0 hub TUSB4020BI-Q1 and the TPD3S716-Q1.

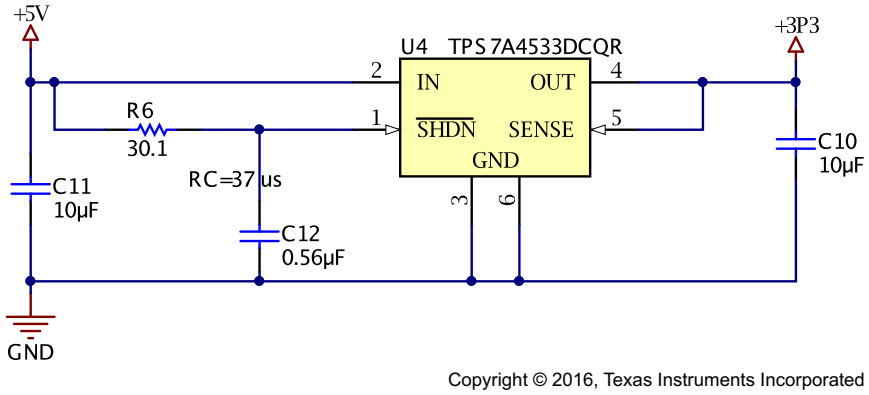


Figure 6. TPS7A4533 3.3-V Low Dropout Regulator Schematic

2.4.1 Start-up Timing

The USB 2.0 hub TUSB4020BI-Q1 requires that the VDD33 supply (TPS704533 in this design) be stable at least 10-µs before the VDD supply (TPS74801-Q1 in this design) powers on. To accomplish this, an RC circuit (R6 and C12) adds a 37-µs startup delay to the $\overline{\text{SHDN}}$ pin with the VDD33 supply and a 66-µs startup delay for the VDD supply. The difference of 29 µs meets this requirement.

2.4.2 Output Capacitor Selection

Extra consideration must be given for the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behaviors over temperature and applied voltage. The most common dielectrics used are Z5U, Y5V, X5R, and X7R. The Z5U and Y5V dielectrics are good for providing high capacitances in a small package, but exhibit strong voltage and temperature coefficients. When used with a 5-V regulator, a 10-µF Y5V capacitor can exhibit an effective value as low as 1 µF to 2 µF over the operating temperature range. The X5R and X7R dielectrics result in more stable characteristics and are more suitable for use as the output capacitor. The X7R type has better stability across temperature, while the X5R is less expensive and is available in higher values. This design uses a 10-µF capacitor (C10) with an X5R rating.

2.5 TPS78401-Q1

Figure 7 shows the TPS78401-Q1 (U3) configured in this design. The LMR14050-Q1 supplies the IN voltage-supply pin. The OUT pin is the VDD supply rail for the USB 2.0 hub TUSB4020BI-Q1.

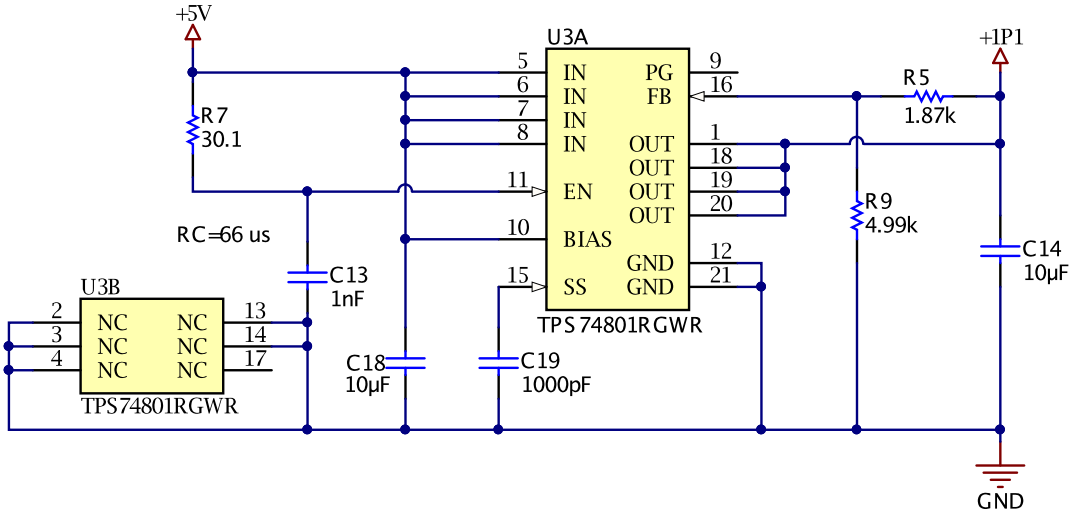


Figure 7. TPS78401-Q1 1.1-V Low Dropout Regulator Schematic

2.5.1 Output Voltage Selection

For an output voltage of 1.1 V, the resistor divider (R5 and R9) on the FB pin was set by Equation 9 where R9 should be ≤ 4.99 kΩ. A value for R9 of 4.99 kΩ was chosen to minimize the FB pin input current. This yields a value of 1.87 kΩ for R5.

$$V_{OUT} = 0.8 \times (1 + R_5 / R_9) \quad (9)$$

2.5.2 Input, Output, and Bias Capacitor Requirements

The device is designed to be stable for all available types and values of output capacitors ≥ 2.2 µF. The device is also stable with multiple capacitors in parallel, which can be of any type or value. The capacitance required on the IN and BIAS pins strongly depends on the input supply source impedance. To counteract any inductance in the input, the minimum recommended capacitor for V_{IN} and V_{BIAS} is 1 µF. If V_{IN} and V_{BIAS} are connected to the same supply, the recommended minimum capacitor for V_{BIAS} is 4.7 µF. Good quality, low ESR capacitors should be used on the input, ceramic X5R and X7R capacitors are preferred. These capacitors should be placed as close to the pins as possible for optimum performance. For this design, C_{OUT} (C14) is a 10-µF capacitor with an X5R rating. Because the IN and BIAS pins are connected to the same supply, C_{IN} (C18) is a 22-µF capacitor with an X5R rating.

2.5.3 Programmable Soft-Start

The TPS74801-Q1 features a programmable, monotonic, voltage-controlled soft-start that is set with an external capacitor (CSS, or C19). This feature is important for many applications because it eliminates power-up initialization problems when powering FPGAs, DSPs, or other processors. The controlled voltage ramp of the output also reduces peak inrush current during start-up, minimizing start-up transient events to the input power bus. To achieve a linear and monotonic soft-start, the TPS74801-Q1 error amplifier tracks the voltage ramp of the external soft-start capacitor until the voltage exceeds the internal reference. The soft-start ramp time depends on the soft-start charging current (ISS), soft-start capacitance (CSS), and the internal reference voltage (VREF), and can be calculated using Equation 10:

$$t_{SS} = (V_{REF} \times C_{SS}) / I_{SS} \quad (10)$$

where:

- V_{REF} = 0.8 V
- I_{SS} = 440 nA

This design uses a C_{SS} (C19) of 1000 pF for t_{SS} = 1.82 ms. This measure, along with the 66-µs RC (R7 and C13) circuit on the EN pin, ensures the VDD stabilizes after VDD33 for the TUSB4020BI-Q1 timing requirement.

3 Getting Started Hardware

- Connect the board to a +12V power supply and GND through the in-board banana jacks.
- The board should power on automatically; verify that the board is receiving power by checking if the LED is illuminated.
- To check port functionality, confirm that VEN and DEN jumpers are enabled for the port being tested.
- Connect USB peripheral device through a USB cable to the J4 and J7 USB ports to validate DCP charging functionality.
- To verify USB data functionality, connect the upstream USB port (J2) to a PC through USB Type-A to Type-B cable.

4 Testing and Results

4.1 Short-to-Battery

Once a voltage above the V_{OVP} threshold is detected by the device, the TPD3S716-Q1 shuts off all FETs and asserts a fault on the $\overline{FLT}$ pin. When the excessive voltage is removed, the device automatically re-enables and the $\overline{FLT}$ de-asserts.

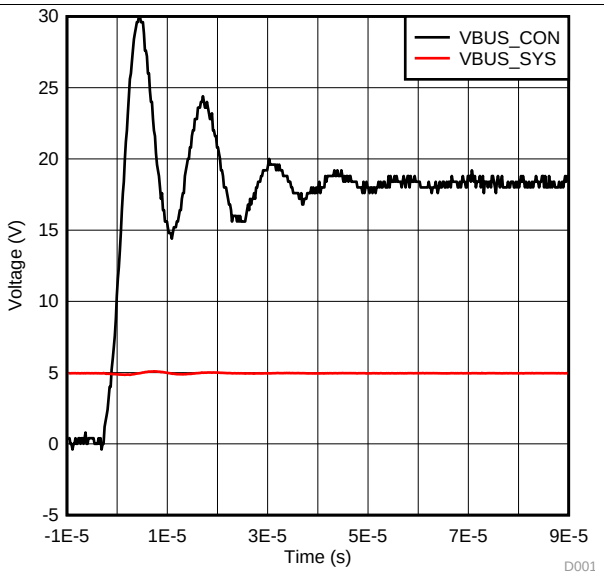


Figure 8. 18-V STB to DP1 V_{BUS}

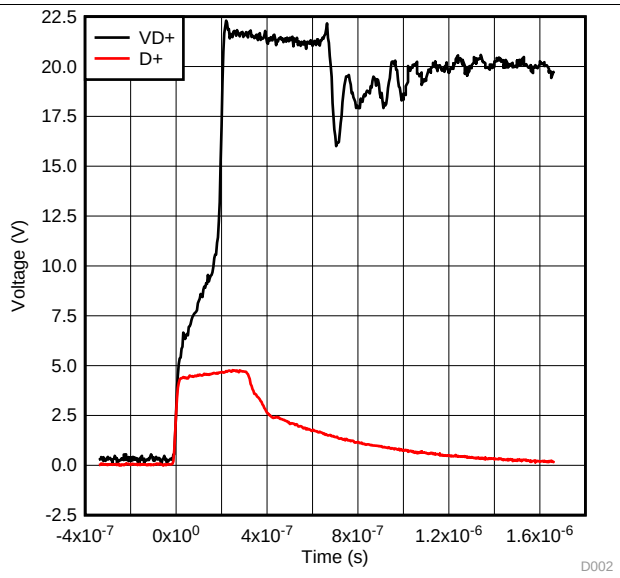


Figure 9. 18-V STB to USB Data Lines

4.2 IEC 61000-4-2 ±8-kV Clamping Waveforms on USB Data Lines

The protected pins (VBUS_CON, VD+, VD-) are tested to pass the IEC 61000-4-2 ESD standard up to level 4 ESD protection. Additionally, these pins are tested against ISO 10605 with the 330-pF and 330-Ω equivalent network. This guarantees passing at least ±8-kV contact discharge and ±15-kV air-gap discharge according to both standards.

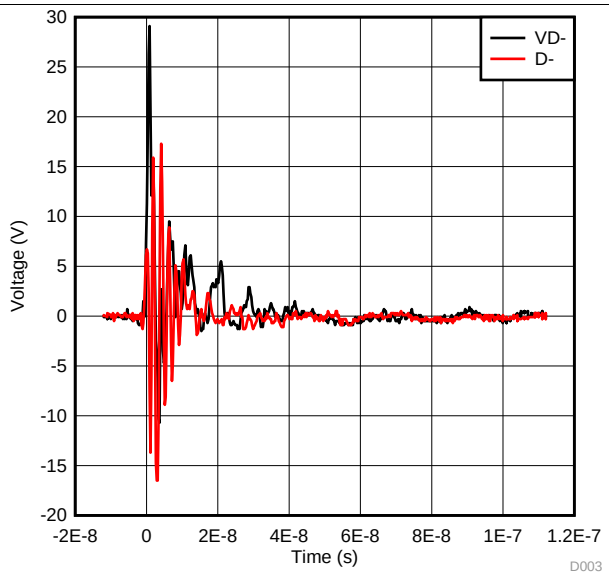


Figure 10. +8-kV IEC 61000-4-2 ESD Clamping

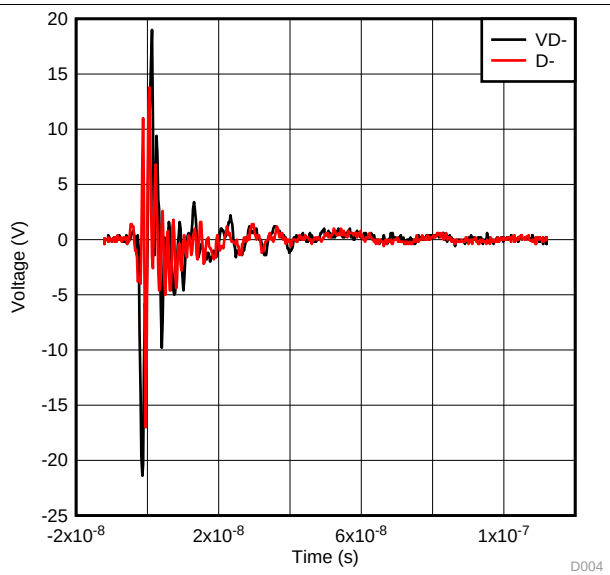


Figure 11. -8-kV IEC 61000-4-2 ESD Clamping

4.3 Short to Ground

When a voltage on VBUS_CON is detected as too low (below the V_{SHRT} threshold) after the device is enabled, the device enters a short-circuit protection mode and asserts the $\overline{FLT}$. The device sources the I_{SHRT} current until it detects the voltage rising above the V_{SHRT} threshold. Then the device resumes standard operating mode and de-asserts $\overline{FLT}$.

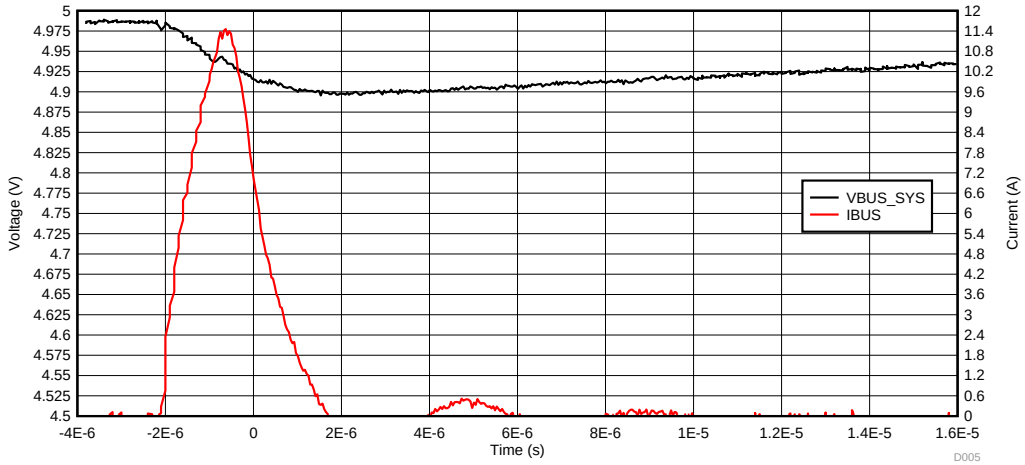


Figure 12. Short to Ground on V_{BUS}

4.4 USB 2.0 High-Speed Downstream Near-End Eye Diagram

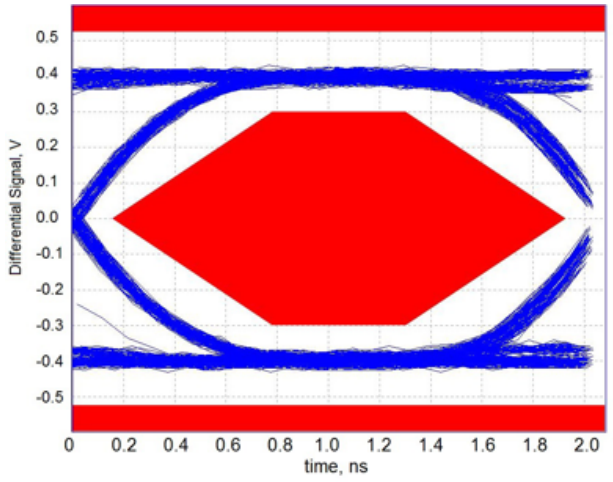


Figure 13. TIDA-00887 USB 2.0 DP1 Eye Diagram

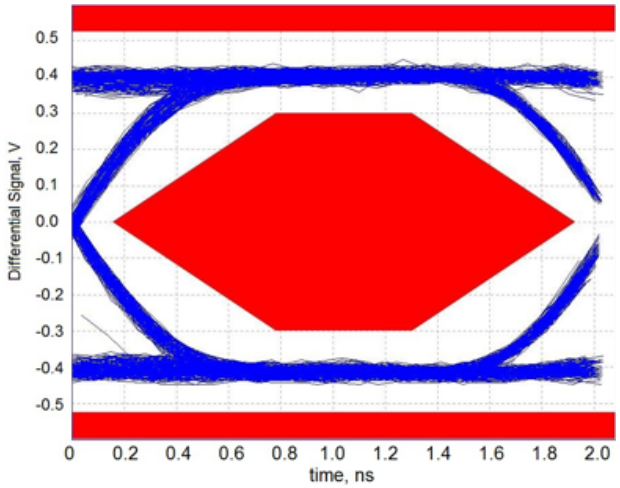


Figure 14. TIDA-00887 USB 2.0 DP2 Eye Diagram

5 Design Files

5.1 Schematics

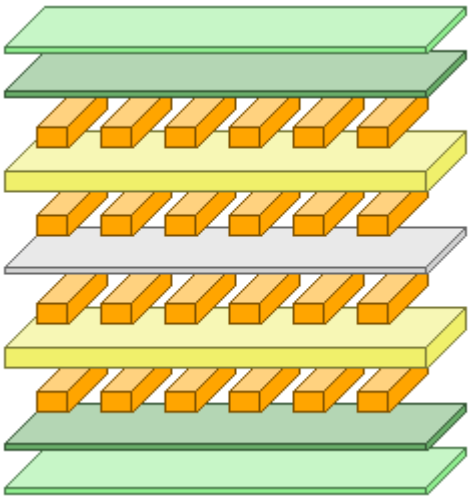
To download the schematics for each board, see the design files at: TIDA-00887.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00887.

5.3 Printed Circuit Board (PCB) Layout Recommendations

TIDA-00887 is a four-layer PCB. The board thickness is 0.062 inches. Figure 15 shows the PCB stack-up. The core material for dielectric 1 and dielectric 3 is FR-408HR.



Top Overlay	
Top Solder	0.4 mils
Top Layer	1.417 mils
Dielectric 1	5.5 mils
GND	1.417 mils
Dielectric 2	44.532 mils
3p3V	1.417 mils
Dielectric 3	5.5 mils
Bottom Layer	1.417 mils
Bottom Solder	0.4 mils
Bottom Overlay	

Figure 15. TIDA-00887 PCB Stack-Up

Route all USB 2.0 lines as controlled impedance, high-speed differential pairs. Minimize the use of VIAs and 90° corners in the routing of the high-speed lines. Assure the high-speed lines reference a solid ground plane and the plane is void of cuts and splits to prevent impedance discontinuities. ESD connection points must be placed in line with the high-speed signal traces to reduce reflections caused by routing discontinuities.

5.3.1 Layout Prints

To download the layer plots, see the design files at TIDA-00887.

5.4 Layout Guidelines

5.4.1 TPD3S716-Q1

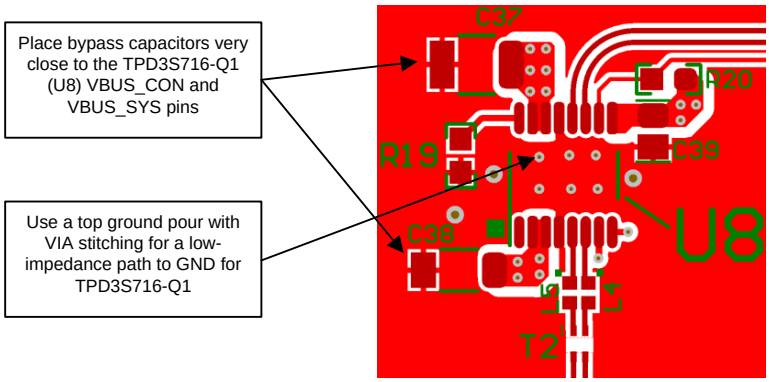


Figure 16. TPD3S716-Q1

5.4.2 LMR14050-Q1 (U5)

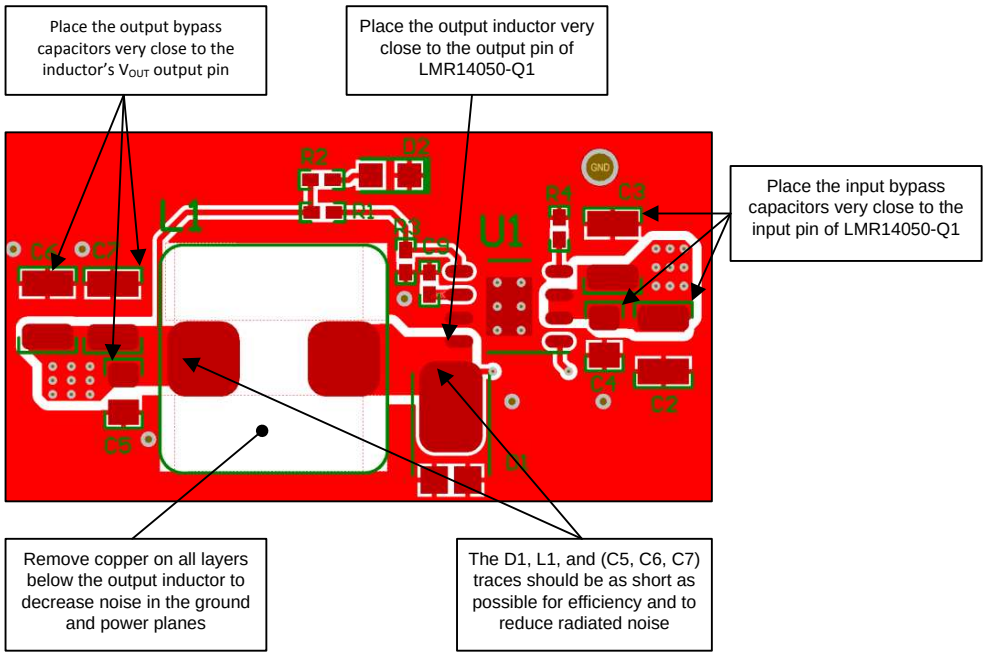


Figure 17. LMR14050-Q1 (U1)

5.4.3 TPS7A4533 (U6)

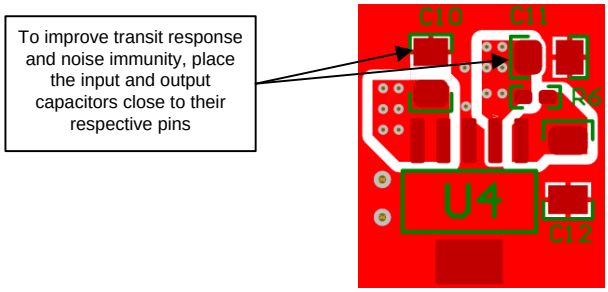


Figure 18. TPS7A4533 (U4)

5.4.4 TPS74801 (U7)

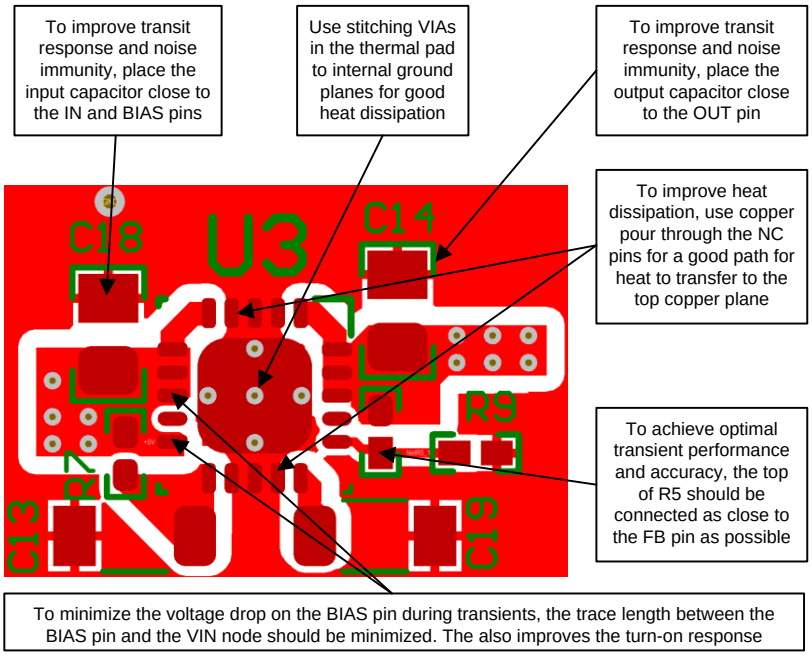


Figure 19. TPS74801 (U3)

5.4.5 TUSB4020BI-Q1 (U4)

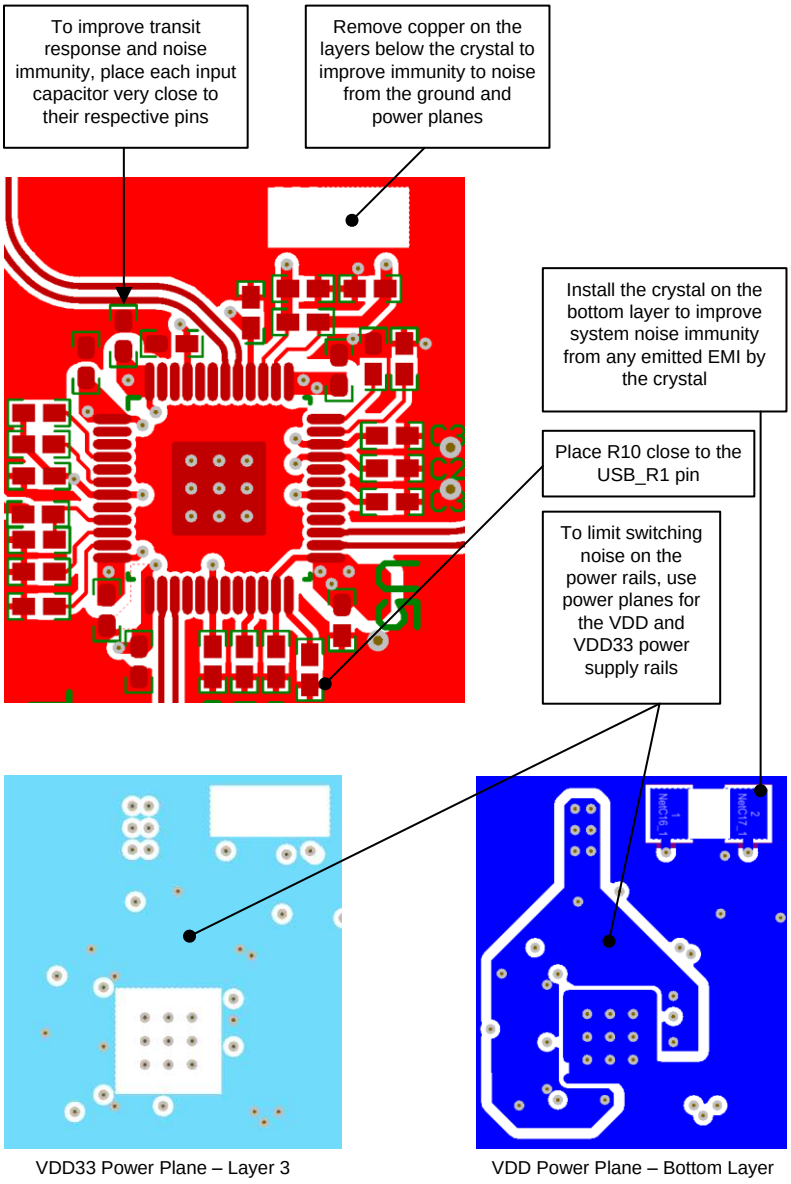


Figure 20. TUSB4020BI-Q1 (U5)

5.5 Altium Project

To download the Altium project files, see the design files at TIDA-00887.

5.6 Gerber Files

To download the Gerber files, see the design files at TIDA-00887.

5.7 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00887.

6 Related Documentation

1. Texas Instruments, *Designing USB for Short-to-battery Tolerance in Automotive Environments*, (SLLY019)
2. Texas Instruments, *ESD Protection Layout Guide*, Application Report (SLVA680)
3. Texas Instruments, *LDO Noise Demystified*, Application Report (SLAA412)
4. Texas Instruments, *WEBENCH® Design Center*, (http://www.ti.com/webench)

6.1 Trademarks

7 Terminology

- DCP – Dedicated charging port
- DP – Downstream port
- STB – Short-to-battery
- UP – Upstream port

IMPORTANT NOTICE FOR TI REFERENCE DESIGNS

Texas Instruments Incorporated ('TI") reference designs are solely intended to assist designers ("Designer(s)") who are developing systems that incorporate TI products. TI has not conducted any testing other than that specifically described in the published documentation for a particular reference design.

TI's provision of reference designs and any other technical, applications or design advice, quality characterization, reliability data or other information or services does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such reference designs or other items.

TI reserves the right to make corrections, enhancements, improvements and other changes to its reference designs and other items.

Designer understands and agrees that Designer remains responsible for using its independent analysis, evaluation and judgment in designing Designer's systems and products, and has full and exclusive responsibility to assure the safety of its products and compliance of its products (and of all TI products used in or for such Designer's products) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to its applications, it has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any systems that include TI products, Designer will thoroughly test such systems and the functionality of such TI products as used in such systems. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

Designers are authorized to use, copy and modify any individual TI reference design only in connection with the development of end products that include the TI product(s) identified in that reference design. HOWEVER, NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of the reference design or other items described above may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI REFERENCE DESIGNS AND OTHER ITEMS DESCRIBED ABOVE ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNERS AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS AS DESCRIBED IN A TI REFERENCE DESIGN OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF THE REFERENCE DESIGNS OR USE OF THE REFERENCE DESIGNS, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

TI's standard terms of sale for semiconductor products (http://www.ti.com/sc/docs/stdterms.htm) apply to the sale of packaged integrated circuit products. Additional terms may apply to the use or sale of other types of TI products and services.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265