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TI Precision Designs
20-Bit, 1-MSPS, 4-Ch Small-Form Factor Design for Test and Measurement Applications Reference Design

TI Designs – Precision

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Design Resources

TIPD211	All Design Files
ADS8900B	Product folder
OPA625/2625	Product folder
REF5050	Product folder
REF6050	Product folder
ADS8881	Product folder
TINA-TI™	SPICE simulator

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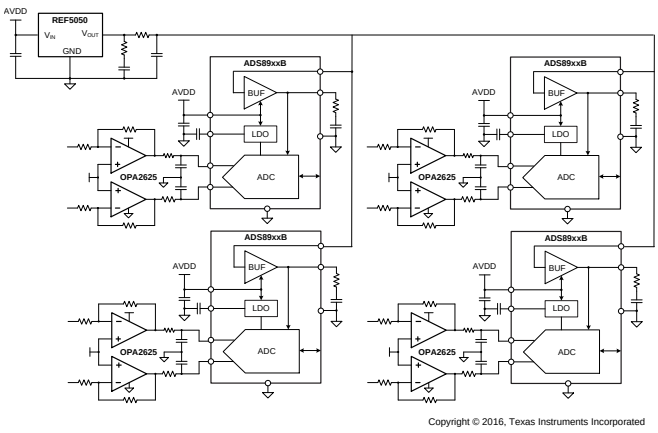
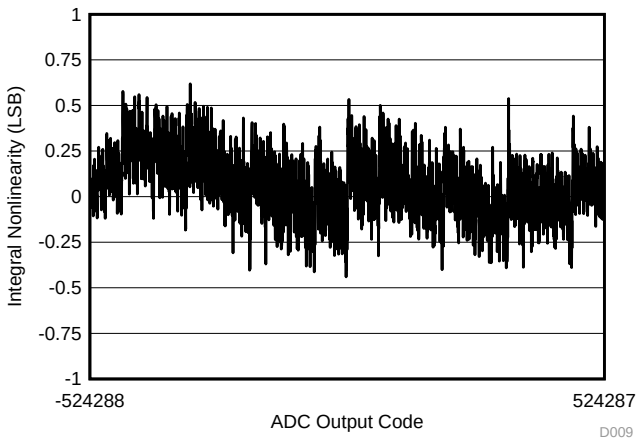
Circuit Description

End equipment such as mixed-signal SoC testers, memory testers, battery testers, liquid-crystal display (LCD) testers, benchtop equipment, high-density digital cards, high-density power cards, x-ray, MRI, and so forth require multiple, fast, simultaneous-sampling channels with excellent DC and AC performance but at low power and in small board spaces. The proposed solution in this design uses high-performance SAR ADCs (ADS8900B), precision amplifiers (OPA2625), and a precision voltage reference (REF5050).

Features

- 20-Bit, 1-MSPS, Four-Channel Simultaneous Sampling Data Acquisition System
- 20-Bit NMC DNL; ±1-ppm INL Linearity Performance for Each Channel
- 102.5-dB SNR, 125-dB THD With 2-kHz Sine Wave Input on Each Channel
- > 110-dB Channel-to-Channel Isolation
- Tested Circuit Guide; Includes Getting Started Guide





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1 Key System Specifications

The primary goal for this TI Precision Design is to create a data acquisition system that delivers four high-speed, simultaneous sampling channels with 20-bit precision performance and low channel-to-channel interference in a small printed-circuit board (PCB) area and with low power consumption.

The design goals and performance is summarized in Table 1.

Table 1. Design Goal vs Measured Performance

PARAMETER	GOAL	MEASURED
ADC sample rate	1 MSPS	1 MSPS
No. of channels	Four, simultaneous sampling	Four, simultaneous sampling
Linearity	20-bit NMC, < ±1.5 ppm INL	20-bit NMC, ±0.75 ppm INL
Noise performance 10-V_{P-P} differential input signal of 2 kHz	> 102 dB SNR	102.5 dB
Distortion	< –120 dB	–125 dB
Channel-to-channel isolation	> 100 dB	> 110 dB
Power supply	< 5.5-V analog, 3.3 V I/O	5.3-V analog, 3.3 V I/O
Power consumption	< 250 mW	210 mW
PCB size (analog blocks)	< 75 sq. cm	< 60 sq. cm

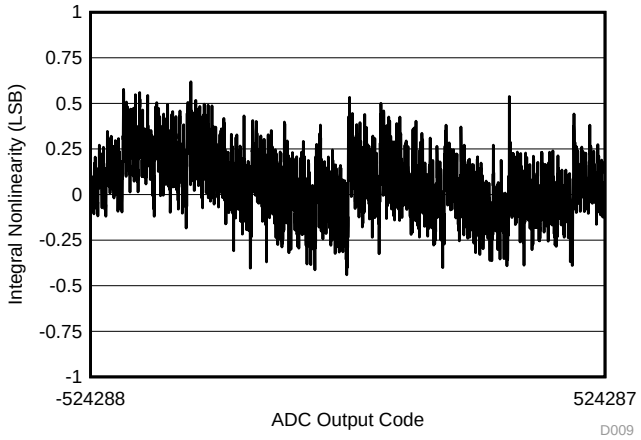

Figure 1. Linearity Plot
20-bit NMC DNL, ±0.75-ppm INL

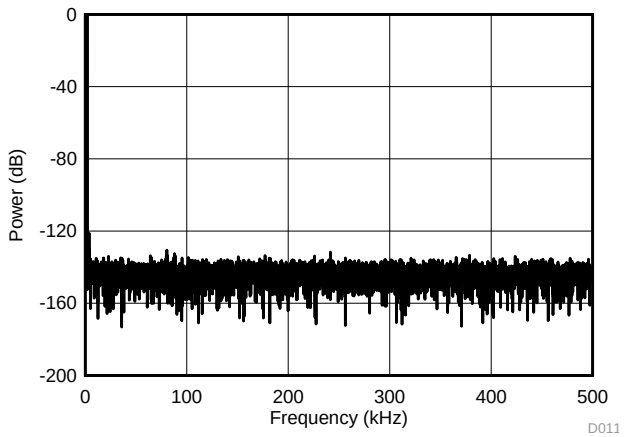

Figure 2. FFT Plot
102.5-dB SNR –125-dB THD

2 System Description

End equipment such as mixed-signal system-on-a-chip (SoC) testers, memory testers, battery testers, LCD testers, benchtop equipment, high density digital cards, high density power cards, x-ray, MRI, and so forth require multiple, fast, simultaneous-sampling channels with excellent DC and AC performance but at low power and in small board spaces.

The design uses the ADS8900B precision SAR ADC, the REF5050 low-drift reference source, and the OPA2625 precision driver amplifier.

3 Block Diagram

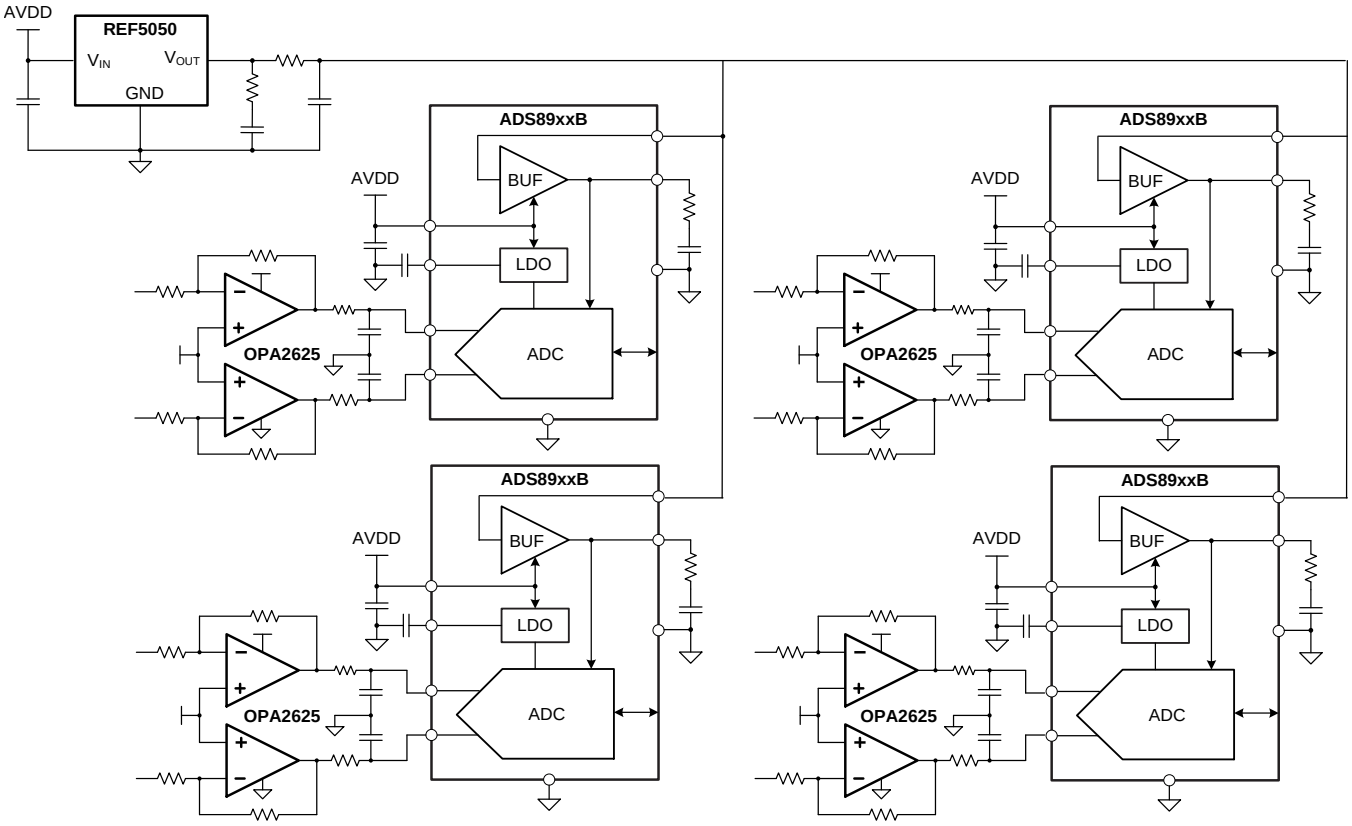

Figure 3. TIPD211 Block Diagram

4 Problem Statement

Figure 4 shows a typical block diagram highlighting the major blocks of a data acquisition system with a single SAR ADC (from an analog design perspective).

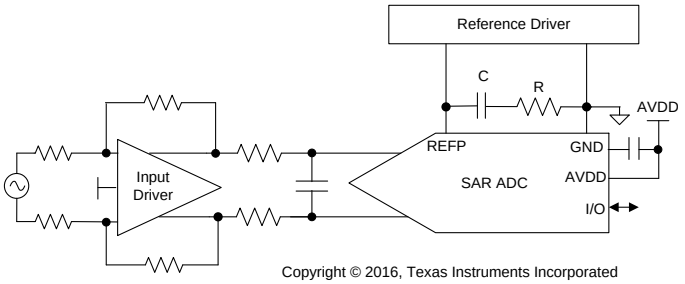

Figure 4. Major Blocks of DAQ—Single SAR ADC

For a system employing multiple, simultaneously-sampling SAR ADCs, the user can share the power supply and then simply duplicate the input driver and reference driver circuit for each SAR ADC, as shown in Figure 5.

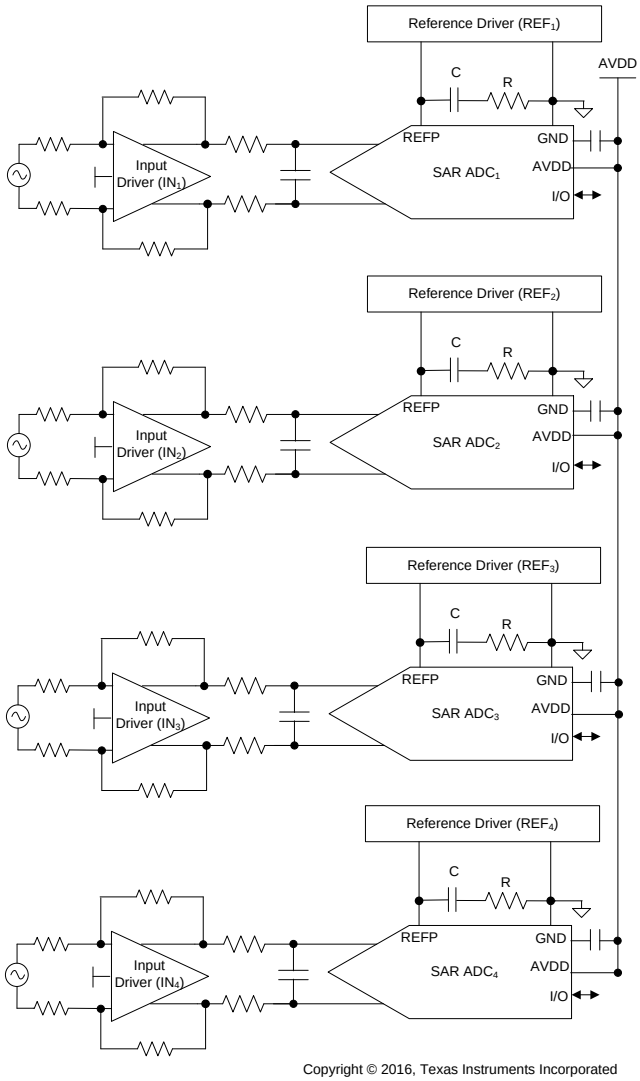

Figure 5. Major Blocks of DAQ—Four SAR ADCs

From an analog design perspective, the three major design blocks in any data acquisition system (DAQ) are the power supply, the input driver circuit, and the reference driver circuit.

1. *Power Supply*: Any noise in the power supply of the system can couple to the ADC output through the ADC power supply terminals, or the ADC input terminals (through the input driver supply path), or the ADC reference terminals (through the reference driver circuit supply path), or through all of them. To achieve the targeted rejection to any noise on the power supply, TI recommends to power the entire analog block with a very low-noise linear regulator. By carefully considering the component selection and layout, the power supply section can be common for the entire system.
2. *Input Driver Circuit*: Keeping the input driver circuit for each SAR ADC channel completely independent from the other channels eliminates one major potential source of channel-to-channel interference. This setup also allows the user to design the analog front-end (AFE) circuit of each channel, as per the characteristics of the input signal provided on that channel. For example:
   - TIDU012 demonstrates how to design an *18-Bit Data Acquisition (DAQ) Block Optimized for 1-μs Full-Scale Step Response* by pairing the ADS8881 SAR ADC with the OPA350 precision amplifier.
   - SLAU515 demonstrates how to design an *18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Distortion and Noise* by pairing the same ADS8881 SAR ADC with the THS4521 fully differential amplifier.
   - SLAU513 demonstrates how to design an *18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Powe*r by pairing the same ADS8881 SAR ADC with the low power OPA320 amplifier.
   - SLAU514 demonstrates how to design an *18-Bit, 10kSPS Data Acquisition (DAQ) Block Optimized for Ultra Low Power < 1 mW* by pairing the same ADS8881 SAR ADC with the ultra-low-power OPA2333 amplifier.
3. *Reference Driver*: The reference driver circuit to the SAR ADC must provide low drift and very accurate voltage for the ADC conversion process and support the dynamic charge requirements of the SAR ADC without limiting the noise and linearity performance at the system level. Keeping the reference driver circuit for each SAR ADC channel completely independent from the other channels helps to improve the channel-to-channel isolation; however, such a solution also results in the following characteristics:
   - On every power up, the initial values of REF_1, REF_2, REF_3, and REF_4 may be different from each other, which leads to gain error mismatch between the four channels.
   - The temperature drift of REF_1, REF_2, REF_3, and REF_4 can be kept low by selecting the appropriate components; however, this temperature drift does not correlate between the four channels.
   - Four independent reference circuits increase the bill-of-materials (BOM) and add to the power consumption and PCB area.

NOTE: The goal of this design is to optimize the reference driver circuit to achieve:
- *Excellent channel-to-channel isolation and excellent channel-to-channel gain matching*
- *Low and correlated temperature drift within channels*
- *Low power, smaller PCB size, and smaller BOM*

5 Theory of Operation

The two primary design considerations to maximize the performance of a high-resolution SAR ADC are the input driver and the reference driver. Figure 6 shows a block diagram comprising the critical analog circuit blocks, which must be carefully designed to achieve the design specifications. The figure also includes the most important specifications for each individual analog block and in the order of design priority. This order is important because the design criteria for each block is dependent on the desired system performance as well as the input signal type.

This design systematically approaches the design of each analog circuit block to achieve an 20-bit low noise and distortion data acquisition system.

The following design steps must be followed to meet the performance goals of this design:

- *Step 1:* Selection of SAR ADC to meet the resolution, linearity, noise, distortion, and throughput requirements
- *Step 2:* Design of the charge kickback filter to maintain amplifier stability and achieve low noise and low distortion.
- *Step 3:* Selection of input driver amplifier and its configuration to achieve extremely low distortion
- *Step 4:* Design a high-precision reference driver circuit, whichprovides the required value of V_{REF} with a low offset, drift, and noise contributions.

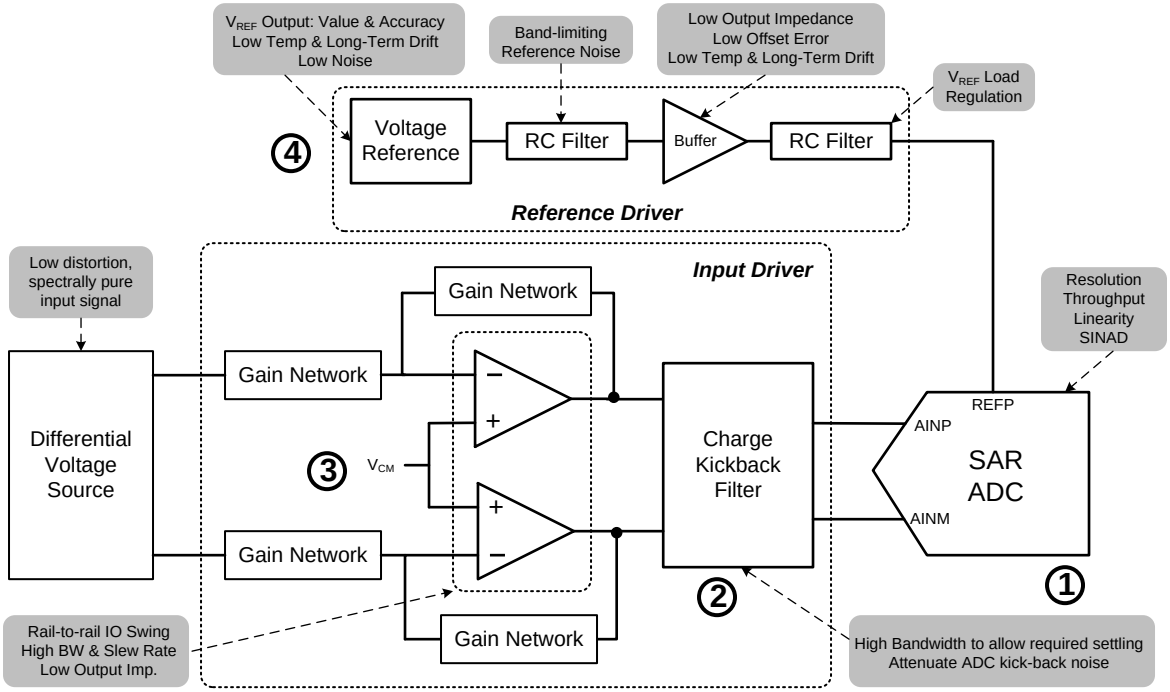

Figure 6. Block Diagram Highlighting Primary Design Criteria for DAQ Block

5.1 Step 1—SAR ADC selection

As detailed in Section 2, the SAR ADC selected for this design must have a minimum of 20 bits of resolution and must support a throughput of 1-MSPS. Another imperative is that the selected SAR ADC must have linearity, noise, distortion, and power consumption specifications that meet or exceed the system level specifications.

5.2 Step 2—Low-Distortion Charge Kickback Filter Design

Figure 7 shows the input circuit of a typical SAR ADC. During the acquisition phase, the SW switch closes and connects the sampling capacitor (C_{SH}) to the input driver circuit. This action introduces a transient on the input pins of the SAR ADC. An ideal amplifier with 0 Ω of output impedance and infinite current drive can settle this transient in zero time. For a real amplifier with non-zero output impedance and finite drive strength, this switched capacitor load may create stability issues.

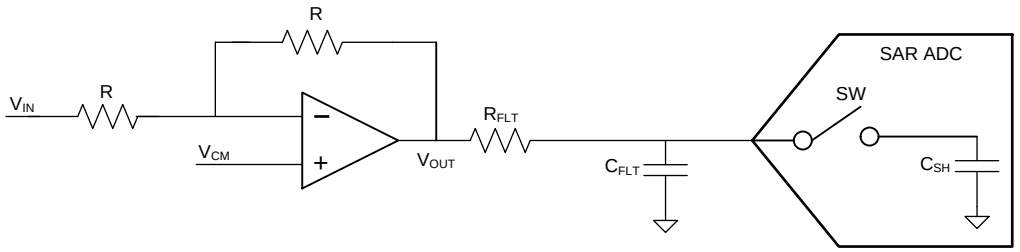

Figure 7. Input Sample and Hold Circuit for Typical SAR ADC

The RC charge kickback filter helps address these issues. The capacitor C_{FLT} helps reduce the sampling charge-kickback at the ADC input and provides a charge bucket to quickly charge the input capacitor C_{SH} during the sampling process.

When SW closes, the worst-case voltage difference between the sampling capacitor (C_{SH}) and the filter capacitor (C_{FLT}) is the full-scale input range supported by the SAR ADC (that is, V_{REF}). The charge required for the ADC sampling capacitor is given by Equation 1 :

$$Q_{SH} = C_{SH} \times V_{REF} \tag{1}$$

As a general rule, the value of the capacitor C_{FLT} must be selected such that it provides this charge without dropping its voltage by more than 5% (see Equation 2):

$$Q_{FLT} = C_{FLT} \times \Delta V_{FLT} \leq C_{FLT} \times (0.05 \times V_{REF}) \tag{2}$$

By the principle of charge conservation, the charge required by the sampling capacitor must be equal to the charge provided by the filter capacitor. Using this principle, derive the following Equation 3:

$$Q_{SH} = Q_{FLT}$$

$$\rightarrow C_{FLT} \times (0.05 \times V_{REF}) \geq C_{SH} \times V_{REF}$$

$$\rightarrow C_{FLT} \geq 20 \times C_{SH} \tag{3}$$

At this point, understanding the trade-offs involved in selecting the values of C_{FLT} and R_{FLT} is important. A higher value of C_{FLT} provides better attenuation against the kickback noise when the sampling switch closes. However, C_{FLT} cannot be made arbitrarily large because it may then degrade the phase margin of the driving amplifier, and even make it unstable.

The series resistor R_{FLT} functions as an isolation resistor, which helps stabilize the driving amplifier, as explained in *Operational Amplifier Stability - Parts 1-11* [2]. A higher value of R_{FLT} is helpful from the perspective of amplifier stability, but this higher source impedance increases the non-linear input impedance of the SAR ADC and thus introduces distortion. Use the following Equation 4 as a general rule:

$$R_{FLT} < \frac{R_{SWITCH}}{20} \tag{4}$$

If the output impedance of the driving amplifier is equal to R_O, its stability can be analyzed by evaluating the effect of R_{FLT} and C_{FLT} on the amplifier open-loop gain (A_{OL}) response. As shown in Figure 8, the closed-loop response of the amplifier for a gain of 1 is denoted as A_{CL} and the unity-gain bandwidth is denoted as f_{CL}.

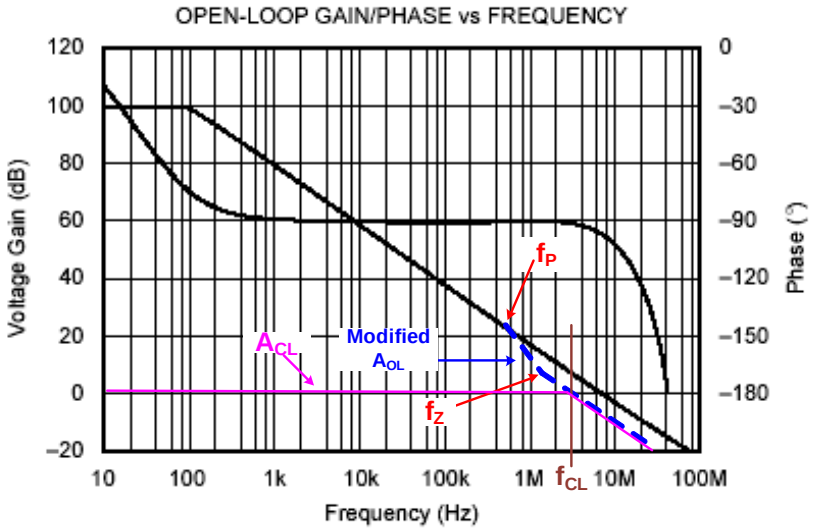

Figure 8. Analyzing Effect of RC-Filter on Op Amp Stability Using A_{OL} Response

The combination of R_O, R_{FLT}, and C_{FLT} introduces one pole, f_P, and one zero, f_Z, as the open-loop response of the amplifier shows, for which the corner frequencies are given in Equation 5 and Equation 6, respectively:

$$f_P = \frac{1}{2\pi(R_O + R_{FLT})C_{FLT}} \quad (5)$$

$$f_Z = \frac{1}{2\pi R_{FLT} C_{FLT}} \quad (6)$$

To ensure that the phase change from the zero negates the phase change that the pole initiates, the frequency distance between the pole and zero must be less than or equal to one decade, as Equation 7 shows.

$$\log\left(\frac{f_Z}{f_P}\right) \leq 1 \quad (7)$$

From Equation 7, the minimum value of R_{FLT} can be derived as:

$$R_{FLT} \geq \frac{R_O}{9} \quad (8)$$

In the interest of stability, the effects of f_Z must occur at a frequency lower than the closed-loop gain bandwidth of the amplifier (f_{CL}). This requirement is in regard for the stability of the amplifier circuit; the closure rate between the open-loop and closed-loop gain curves must not be greater than 20 dB/decade. To account for the fabrication process variations associated with the amplifier performance, a good practice is to choose f_Z such that the closed-loop gain bandwidth of the amplifier, f_{CL}, is at least twice the frequency of the zero, as Equation 9 shows.

$$\frac{f_{CL}}{f_Z} \geq 2 \quad (9)$$

Much of this discussion and subsequent results described in Section 6.3.2 and Figure 29 and which relate to op amp stability have been detailed in [2].

5.3 Step 3—Low-Distortion Input Driver Design

When designing a very low distortion data acquisition block, understanding the sources of nonlinearity is important. In a data acquisition system, every analog and mixed signal component can potentially introduce a non-linearity, which results in distortion. Ideally, the designer prefers that the distortion specification of the system is only limited by the total harmonic distortion (THD) specification of the SAR ADC. To achieve this specification, the distortion specification of the input driver circuit must be negligible compared to the THD specification of the SAR ADC.

As a general rule, if the input driver circuit has been designed to have a 10-dB lower distortion specification than the THD specification of the SAR ADC, then the input driver circuit does not degrade the system level THD specification by more than 0.5 dB (see Equation 10).

$$THD_{AMP} < THD_{ADC} - 10\ dB \tag{10}$$

When an amplifier has been used with negative feedback, the non-linearity (NL) is divided by the loop gain (Aβ), as shown in Equation 11 and Figure 9.

$$V_{OUT} = \frac{V_{IN} \times A}{1 + A\beta} + \frac{NL}{1 + A\beta} \tag{11}$$

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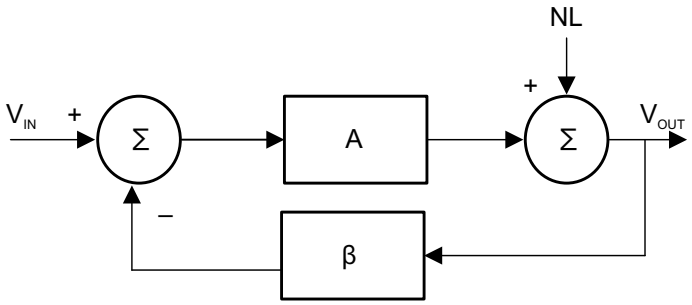

Figure 9. Analyzing Effect of RC-Filter on Op Amp Stability Using A_{CL} Response

The open-loop gain (A) of the amplifier is a function of frequency and typically degrades at –20 dB per decade. This reduction of open-loop gain at higher frequencies causes the THD to degrade at high frequencies. Therefore, to maintain a low THD at higher frequencies, choosing an amplifier with high gain bandwidth product (GBW) is important. This selection ensures that there is sufficient loop gain available at higher input frequencies to maintain the minimum required THD specification.

Most amplifier data sheets specify the THD plus noise (THD+N) as a measured specification. Understanding that in some amplifiers the noise dominates the THD+N specification is important; however, the designer can calculate the THD specification of the amplifier alone based on the second and third harmonic distortion (HD2 and HD3 respectively) using Equation 12.

$$THD(dB) = 10\log\left(10^{\frac{HD2}{10}} + 10^{\frac{HD3}{10}}\right) \tag{12}$$

The distortion from the input driver, however, is not limited to the amplifier distortion specification but also to the amplifier configuration. The input driver can be configured either in an inverting or a non-inverting configuration, as Figure 10 shows.

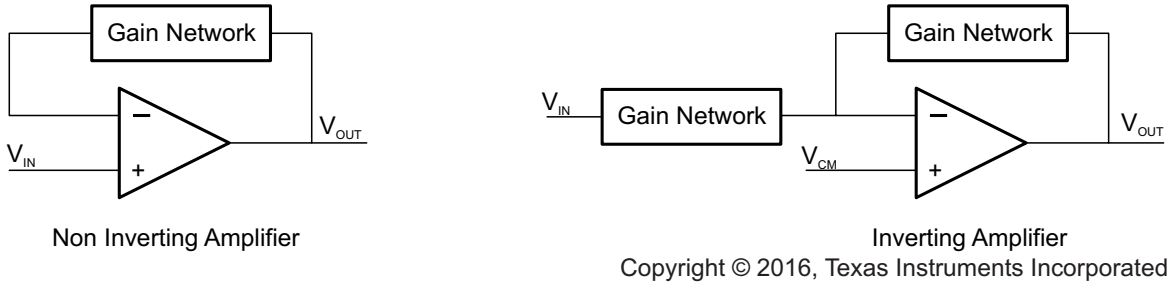

Figure 10. Non-Inverting and Inverting Amplifier Configurations

The common mode of the input driver in a non-inverting configuration follows the input signal. This action adds a constraint on the input amplifier to have rail-to-rail inputs to allow full-scale input signals. Furthermore, the movement of the common mode of the input amplifier introduces additional common-mode dependent distortion at the output of the amplifier. In comparison, in the inverting configuration the common mode is fixed and thus does not require rail-to-rail inputs and also does not introduce any additional common-mode dependent distortion. Therefore, in this design the input driver amplifier has been configured in an inverting amplifier configuration.

For more information regarding the input driver design, visit the TI training portal for *TI Precision Labs - Op Amps*: https://training.ti.com/ti-precision-labs-op-amps.

A high-performance 20-bit, 1-MSPS SAR ADC has a typical signal-to-noise raitio (SNR) specification of >100 dB for a 2-kHz input signal and a V_{REF} = 5 V. To maintain the superior dynamic performance of this ADC, the effect of noise from the front-end circuit has been analyzed in this section. This analysis provides a bound for the maximum noise, which the input driver circuit can have without degrading the system SNR. Based on the maximum noise, an appropriate input amplifier and feedback resistors can be selected for the design.

The input driver in an inverting configuration requires input and feedback. This architectural choice has a significant impact on the noise analysis. Considering the circuit in Figure 11, which is an amplifier in an inverting configuration with two resistors, the user can calculate the noise separately from each of the resistors and the op-amp voltage noise. Each source has its own contribution to the noise at the amplifier output. Noise referred to the input (RTI) is simply the noise referred to the output (RTO) divided by the noise gain of the amplifier.

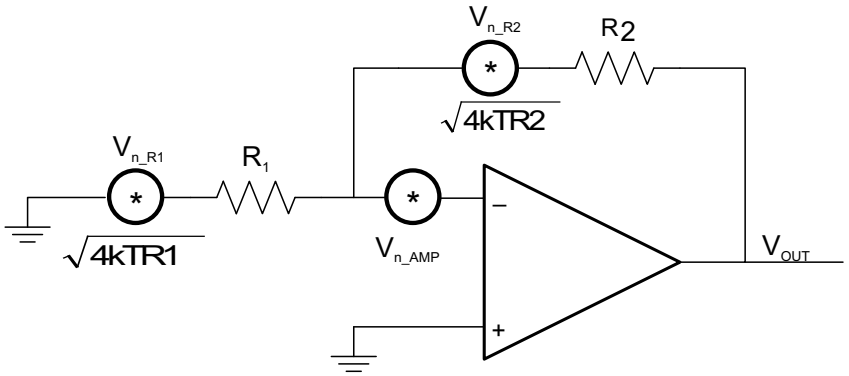

Figure 11. Noise Contributing in Inverting Amplifier

By only considering the voltage noise and not current noise, the RTI noise can be calculated using equation Equation 13

$$V_{n\_AMP\_RTI\_RMS} = \sqrt{1.57 \times BW_{FLT}} \times \sqrt{V_{n\_AMP}{}^2 + 4kTR_1\left[\frac{R_2}{R_1 + R_2}\right]^2 + 4kTR_2\left[\frac{R_1}{R_1 + R_2}\right]^2}$$

$$V_{n\_AMP\_RTO\_RMS} = NG \times V_{n\_AMP\_RTI\_RMS} \quad (13)$$

To calculate the RMS noise, the voltage noise density must be integrated over the anti-aliasing filter bandwidth. For an RC-filter, the effective bandwidth is equal to π / 2 or 1.57 times the 3-dB cutoff frequency. One observation is that the thermal noise of the resistor contributes significantly to RTO noise. In an inverting configuration, the noise gain (NG) is given by Equation 14.

$$NG = 1 + \frac{R_2}{R_1} \quad (14)$$

For equal resistors ($R_1 = R_2 = R$), the noise gain becomes 2 V/V and Equation 13 modifies to Equation 15.

$$V_{n\_AMP\_RTI\_RMS} = \sqrt{1.57 \times BW_{FLT}} \times \sqrt{V_{n\_AMP}{}^2 + 4kT\frac{R}{2}}$$

$$V_{n\_AMP\_RTO\_RMS} = 2 \times \sqrt{1.57 \times BW_{FLT}} \times \sqrt{V_{n\_AMP}{}^2 + 4kT\frac{R}{2}} \quad (15)$$

For any SAR ADC with a differential input, the topology shown in Figure 12 is required.

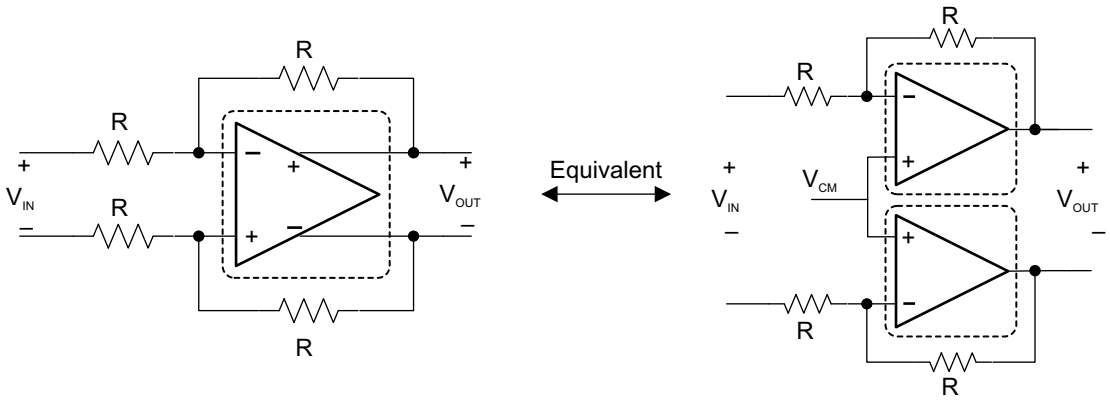

Figure 12. Fully Differential Amplifier Configuration

Both the single-ended amplifiers are identical; so, by using law of superposition, the noise of the fully differential amplifier can be calculated as Equation 16:

$$V_{n\_DIFF\_AMP\_RTO\_RMS} = \sqrt{\left(V_{n\_AMP\_RTO\_RMS}\right)^2 + \left(V_{n\_AMP\_RTO\_RMS}\right)^2}$$

$$V_{n\_DIFF\_AMP\_RTO\_RMS} = \sqrt{2} \times \left(V_{n\_AMP\_RTO\_RMS}\right)$$

$$V_{n\_DIFF\_AMP\_RTO\_RMS} = 2 \times \sqrt{1.57 \times BW_{FLT}} \times \sqrt{2 \times V_{n\_AMP}{}^2 + 4kTR} \quad (16)$$

Therefore, to achieve a lower noise, maintaining the feedback resistors as low as possible is important. However, low value feedback resistors increase the system power consumption and also require amplifiers with a high output current drive. In practice, a trade-off is required between system noise and power.

Now considering an ADC with an input dynamic range of V_{FSR}, the input referred noise can be calculated from the specified value of SNR in the data sheet by using the following Equation 17:

$$V_{n\_ADC\_RMS} = \frac{V_{FSR}}{2\sqrt{2} \times 10^{\frac{SNR(db)}{20}}} \quad (17)$$

So, the total noise contribution from the total data acquisition system can be calculated as Equation 18 shows:

$$V_{n\_TOT\_RMS} = \sqrt{V_{n\_DIFF\_AMP\_RTO\_RMS}^2 + V_{n\_ADC\_RMS}^2} \quad (18)$$

To achieve a minimum specified SNR from the system (SNR_{SYS}), the maximum total RMS noise from the block must be able to meet the requirement in Equation 19:

$$V_{n\_TOT\_RMS} \leq \frac{V_{FSR}}{2\sqrt{2} \times 10^{\frac{SNR_{SYS}\ (dB)}{20}}} \quad (19)$$

The preceding Equation 16 shows that the voltage noise of the amplifier and the thermal noise of the resistors have been integrated over the filter bandwidth. To limit the total integrated noise, the inverting configuration can be modified to an inverting low-pass filter (as shown in Figure 13) by placing an additional filter capacitor (C_{FB}) in parallel with the feedback resistor (R).

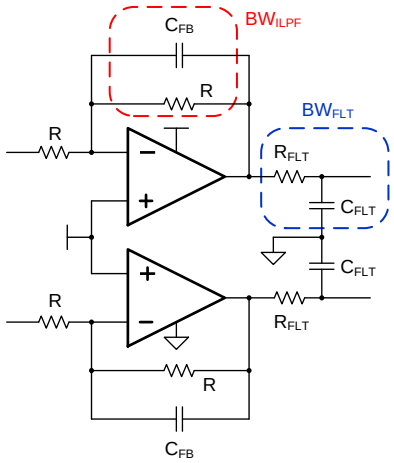

Figure 13. Inverting Low Pass Filter Configuration

The value of the C_{FB} must be such that the closed-loop response of the amplifier does not start affecting the harmonic frequencies. As a general rule, select the cutoff frequency as follows in Equation 20:

$$BW_{ILPF} > 10 \times \text{highest harmonic frequency of interest} \quad (20)$$

The feedback capacitor has been selected as a COG type with a higher voltage rating to counter the effect of capacitance variation with voltage leading to distortion.

5.4 Step 4—Reference Driver Design

External voltage reference circuits are used in a data acquisition system if there is no internal reference in the ADC or if the accuracy of the internal reference is not sufficient to meet the performance goals of the system. These circuits must provide a low-drift, low-noise, and accurate voltage for the ADC reference input. However, the output broadband noise of most references can be in the order of a few 100 μV_{RMS}, which degrades the noise and linearity performance of precision ADCs, for which the typical noise is in the order of tens of μV_{RMS}. So, to optimize the ADC performance, the output of the voltage reference must be appropriately filtered and buffered.

Figure 14 shows the basic circuit diagram for the reference driver circuit for precision ADCs.

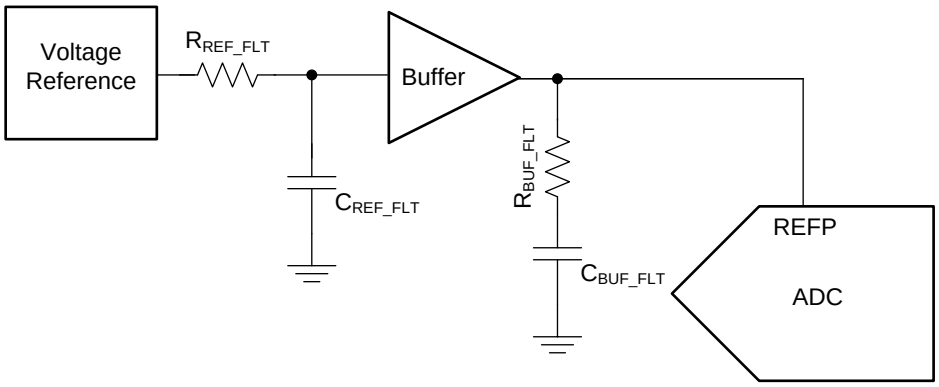

Figure 14. Simplified Schematic of Reference Driver Circuit

The reference noise can be divided into two major categories:

- Low frequency, peak-to-peak flicker or 1/f noise (V_{1/f_REF_P-P}) from 0.1 Hz to 10 Hz
- Higher frequency broadband noise, generally specified as a noise spectral density ($e_{n\_REF\_RMS}$) over a wide range of frequency

The broadband output noise from the reference circuit is band-limited by the 3-dB cutoff frequency (f_{REF_3dB}) of an RC filter at the output. So, the primary objective for the filter design is to keep the bandwidth low enough such that the intrinsic noise from the reference does not degrade the performance of the ADC. For a high-precision ADC with an input dynamic range of V_{FSR}, the root-mean-square (RMS) value of an input-referred noise can be calculated from the specified value of SNR in the data sheet by using Equation 21:

$$V_{n\_ADC\_RMS} = \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)} \tag{21}$$

As a general rule, the total integrated noise from the reference ($V_{n\_REF\_RMS}$) must be kept at least one-third of the ADC noise to prevent any degradation in the system performance, as Equation 22 shows:

$$V_{n\_REF\_RMS} \leq \frac{V_{n\_ADC\_RMS}}{3} \tag{22}$$

For an RC filter, the effective noise bandwidth is equal to the product of π / 2 or 1.57 times the –3-dB cutoff frequency. The value of total noise contribution from the reference circuit, $V_{n\_REF\_RMS}$, is calculated by the root-sum-square (RSS) of the flicker noise and broadband noise, as Equation 23 shows:

$$V_{n\_REF\_RMS} = \sqrt{\left(\frac{V_{1/f\_REF\_pp}}{6.6}\right)^2 + e_{n\_REF\_RMS}^2 \times \frac{\pi}{2} \times f_{REF\_3dB}} \tag{23}$$

Substituting Equation 21 and Equation 23 in Equation 22 results in the following Equation 24:

$$\sqrt{\left(\frac{V_{1/f\_REF\_pp}}{6.6}\right)^2 + e_{n\_REF\_RMS}^2 \times \frac{\pi}{2} \times f_{REF\_3dB}} \le \frac{1}{3} \times \frac{V_{FSR}}{2\sqrt{2}} \times 10^{-\left(\frac{SNR(dB)}{20}\right)} \quad (24)$$

The variation in the broadband noise density of the voltage reference ranges from 100 nV / $\sqrt{Hz}$ to 10000 nV / $\sqrt{Hz}$, depending on the reference type and power consumption. In general, the reference noise is inversely proportional to the quiescent current (I_{Q_REF}). Because broadband noise density is not always included in the voltage reference data sheet, Equation 25 provides an approximation of the noise density for band-gap reference circuits:

$$e_{n\_REF\_RMS} \approx \frac{10000\ nV}{\sqrt{Hz}} \times \frac{1}{\sqrt{2 \times I_{Q\_REF}\ (\text{in } \mu A)}} \quad (25)$$

Equation 25 has been derived on the basis of the measured characteristic between the output noise density and quiescent current of several TI reference circuits, as Figure 15 shows.

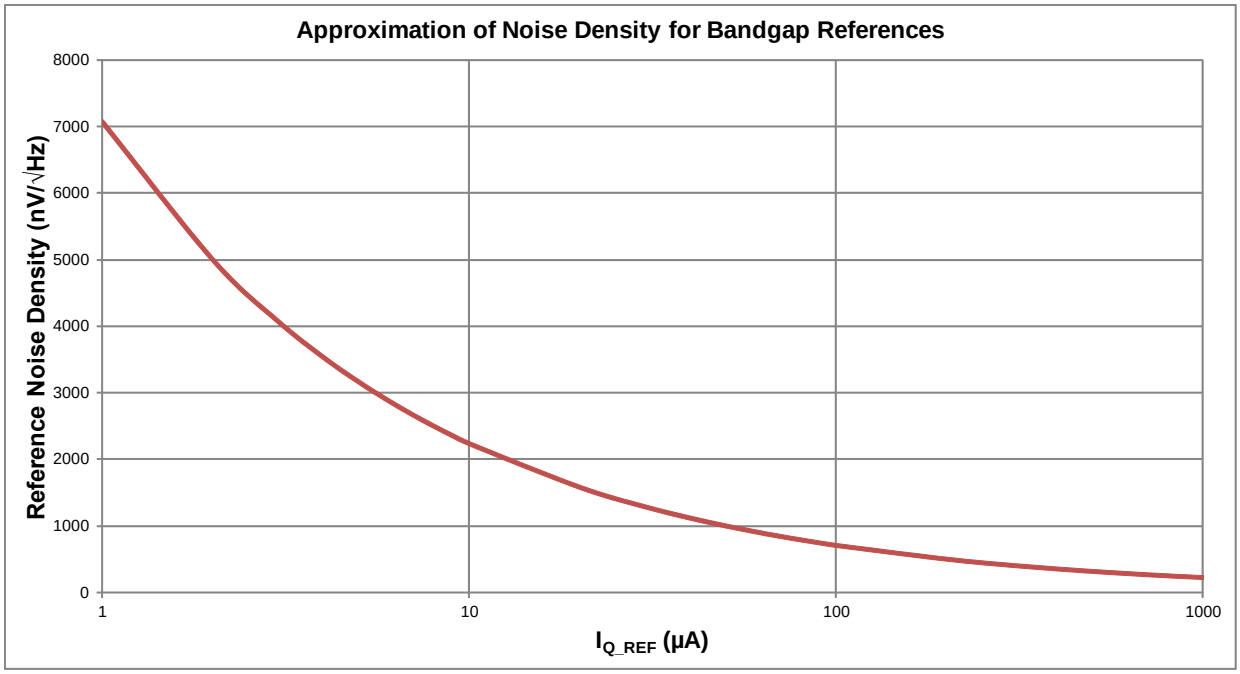

Figure 15. Characteristic Curve—Reference Noise vs Current

Using Equation 24 and Equation 25, the maximum limit for f_{REF_3dB} can be derived as Equation 26 shows:

$$f_{REF\_3dB} \le \frac{2 \times I_{Q\_REF}(\mu A)}{\left(10000\ nV / \sqrt{Hz}\right)^2} \times \frac{2}{\pi} \times \left[\frac{1}{9} \times \frac{V_{FSR}^2}{8} \times 10^{-\frac{SNR(dB)}{10}} - \left(\frac{V_{1/f\_REF\_pp}}{6.6}\right)^2\right] \quad (26)$$

The value of the capacitor for the RC-filter must be kept higher than 100 nF to keep the thermal noise lower than 0.2 μV_{RMS}. Using the selected value for C_{REF_FLT} and f_{REF_3dB}, the value of R_{REF_FLT} can be calculated using Equation 26, as Equation 27 shows:

$$R_{REF\_FLT} = \frac{1}{2\pi f_{REF\_3dB} \times C_{REF\_FLT}} \quad (27)$$

After the noise of the reference block has been band-limited, the next important step is to ensure that the reference can drive the dynamic load posed by the ADC reference input. The reference buffer must regulate the voltage such that ΔV_{REF} stays within a 1-LSB error at the start of each conversion. This requirement necessitates the use of a capacitor (C_{BUF_FLT}) at the output of the buffer amplifier to drive the ADC reference pin.

For an ADC with resolution N, the difference in V_{REF} between two conversions is calculated by Equation 28:

$$\Delta V_{REF} \leq \frac{V_{REF}}{2^N} \tag{28}$$

If the total charge consumed during each conversion is Q_{REF}, then C_{BUF_FLT} can be calculated using Equation 29:

$$C_{BUF\_FLT} = \frac{Q_{REF}}{\Delta V_{REF}} = \frac{Q_{REF} \times 2^N}{V_{REF}} \tag{29}$$

The average value of Q_{REF} can be calculated from the maximum ADC conversion time (T_{CONV_MAX}) and the average value of reference input current (I_{REF}) specified in the ADC data sheet, as Equation 30 shows:

$$Q_{REF} = I_{REF} \times T_{CONV\_MAX} \tag{30}$$

The combination of Equation 28, Equation 29, and Equation 30 yields the expression for the minimum value of C_{BUF_FLT}, as derived in Equation 31:

$$C_{BUF\_FLT} = \frac{I_{REF} \times T_{CONV\_MAX} \times 2^N}{V_{REF}} \tag{31}$$

The capacitor values (C_{BUF_FLT}) derived from this equation are high enough to make the driving amplifier unstable, so TI recommends to use a series resistor, R_{BUF_FLT}, to isolate the amplifier output and make it more stable.

The value of R_{BUF_FLT} is dependent on the output impedance of the driving amplifier as well as on the signal frequency. Typical values of R_{BUF_FLT} range between 0.1 Ω to 2 Ω and the exact value can be found by using simulations from a Simulation Program with Integrated Circuit Emphasis (SPICE). TI recommends to use the smallest possible values for R_{BUF_FLT} to avoid any voltage spikes at the reference pin, which can potentially affect the conversion accuracy.

After designing the appropriate passive filter for band-limiting the noise of the reference circuit, the next step is to select an appropriate amplifier for use as a reference buffer. The key specifications to consider when selecting an appropriate amplifier for the reference buffer are:

- *Open-loop output impedance*: It is important to keep this open-loop output impedance as low as possible because the ADC draws current from the reference pin during conversion and the resultant drop in reference voltage is directly proportional to the output impedance of the driving buffer.
- *Input offset*: The initial input offset must be minimized to ensure that the reference voltage driving the ADC is very accurate.
- *Offset drift*: The offset temperature drift of the reference buffer must be as low as possible to make sure that the reference voltage for the ADC does not change significantly over the operating temperature range.

Texas Instruments' unique REF6050 precision reference offers an elegant solution for this requirement. The REF6050 integrates a precision, low-noise, low-drift bandgap source with a high-bandwidth, low-output impedance drive buffer, which is suitable for driving the reference pin of high precision 18-bit SAR ADCs such as the ADS8881 (see Figure 16).

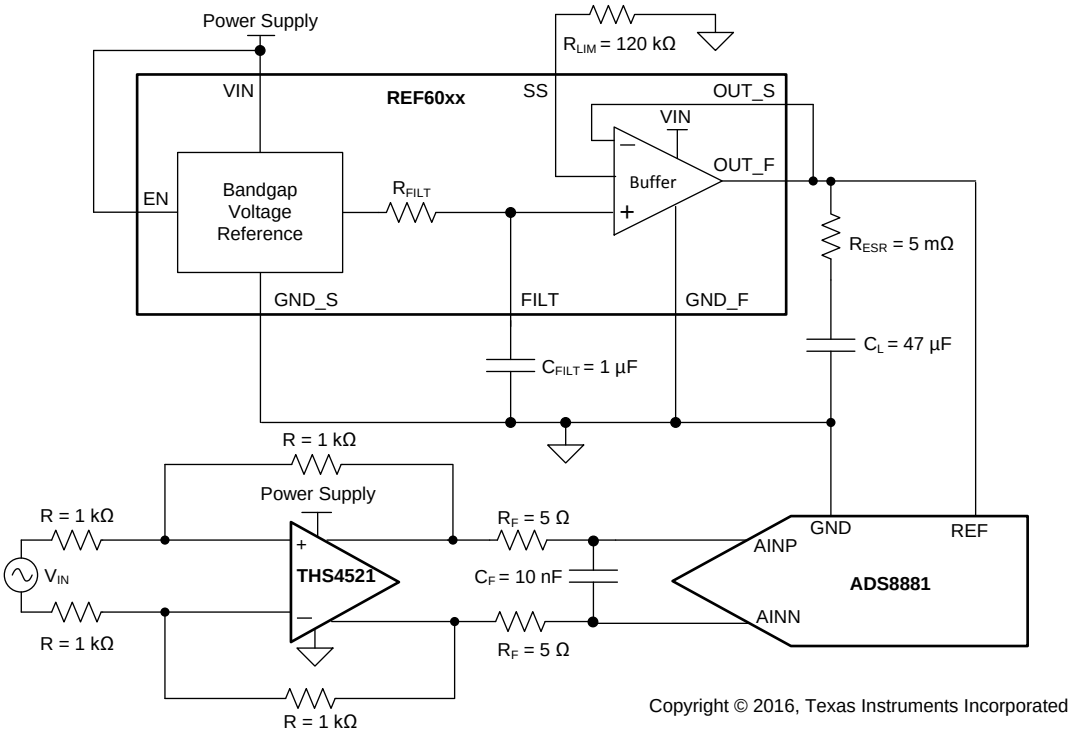

Figure 16. ADS8881 + REF6050 solution

Refer the Applications and Implementation Section of the REF6050 datasheet for more details.

In a system employing four SAR ADCs, it is very tempting to share one REF6050 output across all four SAR ADCs as shown in Figure 17.

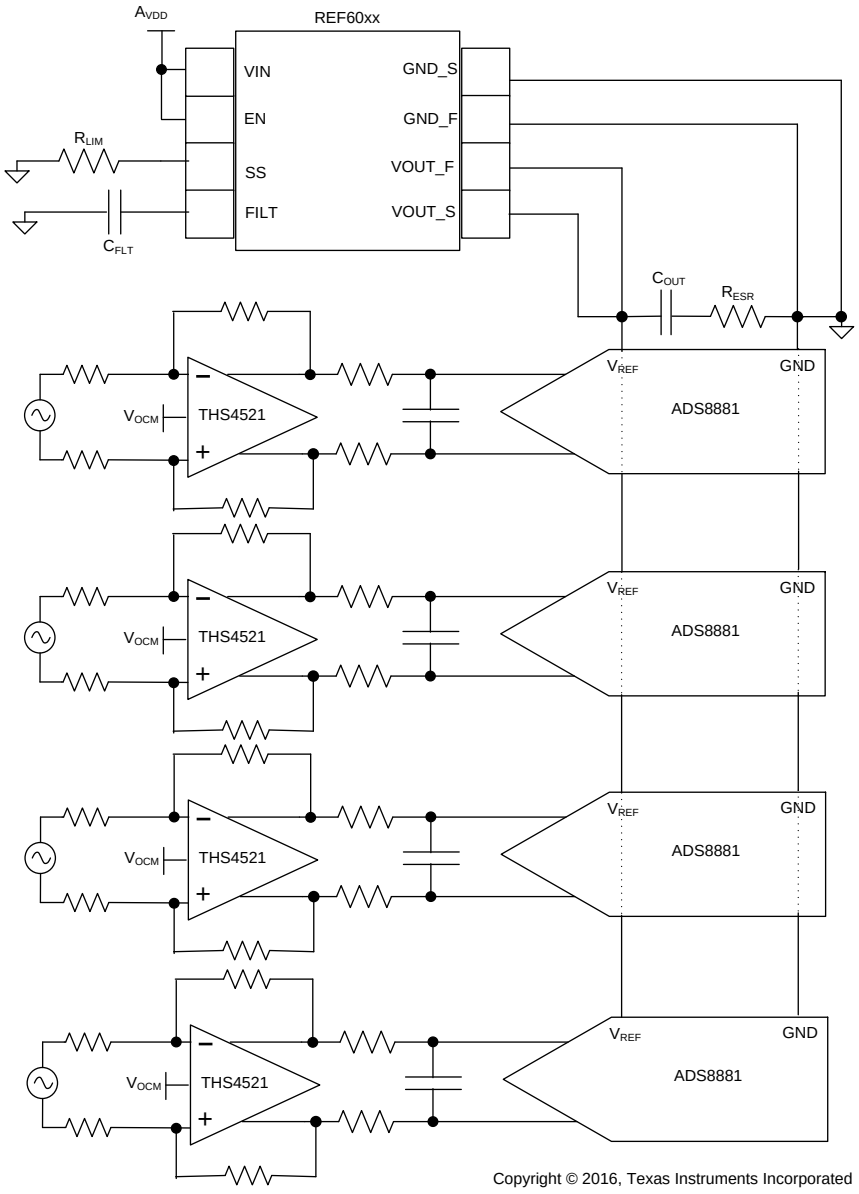

Figure 17. Single REF60xx, Single RC with 4x SAR ADCs

However, the dynamic charge requirement of the reference pin of each ADC is a function of the input voltage provided on the analog input pins of that particular ADC. If C_{REFBUF} and R_{ESR} are shared by the four ADCs, then any settling error in the common reference path introduced due to activity on one of the channels will also disturb the other channels, thereby resulting in channel-to-channel interference errors. For these reasons, it is imperative to provide a separate pair of C_{REFBUF} and R_{ESR} for each individual SAR ADC (see Figure 18).

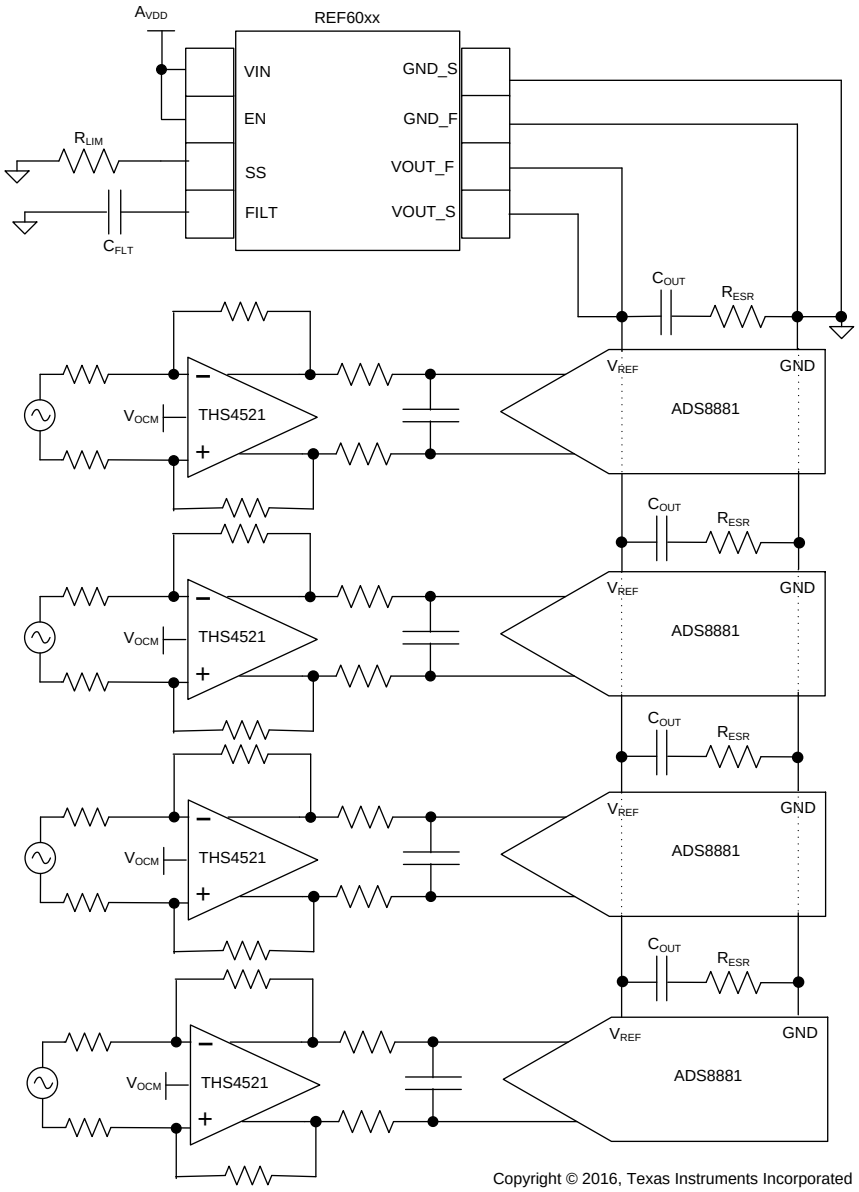

Figure 18. Single REF60xx, 4x RC With 4x SAR ADCs

With this arrangement, the individual C_{REFBUF} values remain the same as indicated by Equation 31. However, the common reference buffer (inside REF6050) is now driving all four capacitors and is now expected to support four times the output current. This is outside the specifications of REF6050.

Figure 19 shows one REF6050 used per SAR ADC.

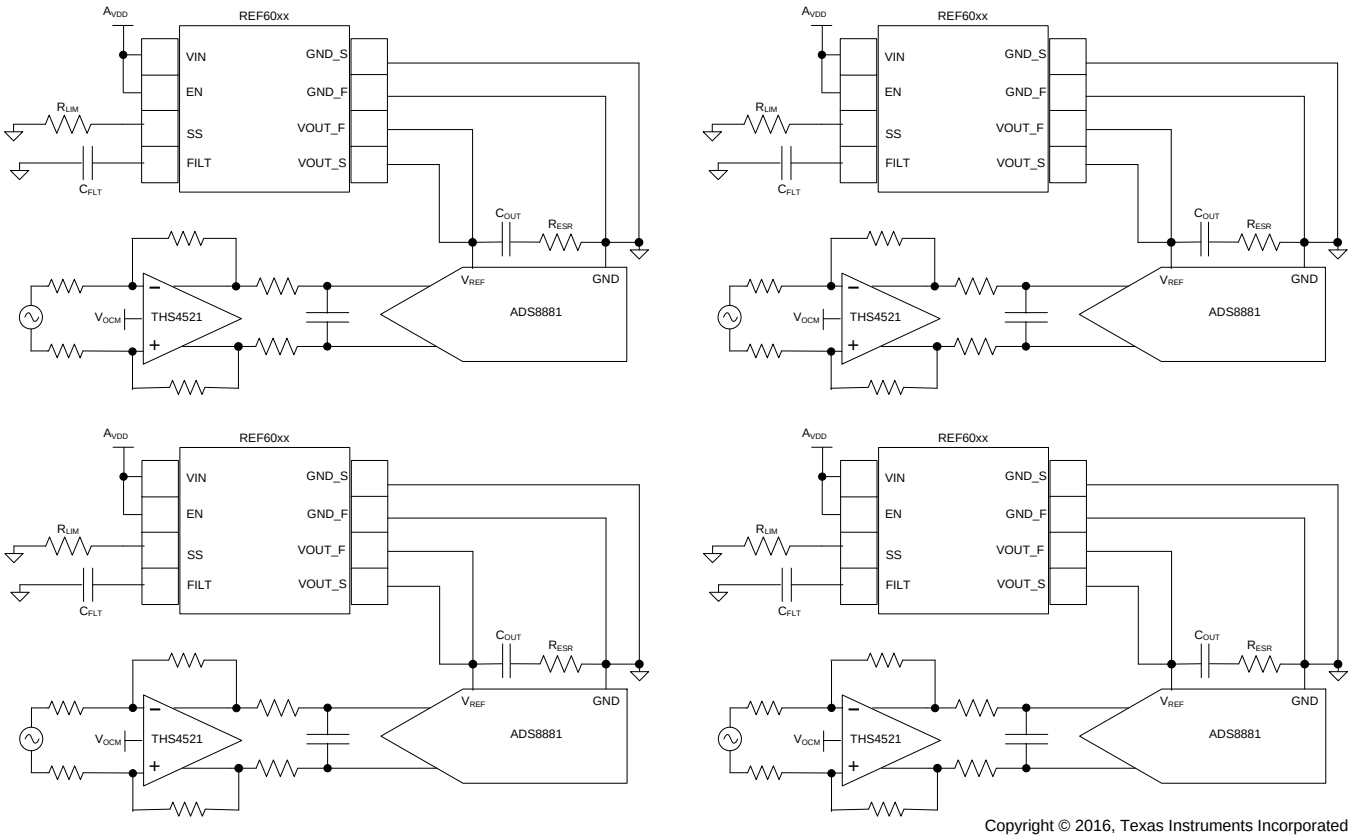

Figure 19. 1x REF60xx and 1x RC Per SAR ADC

However, this configuration has following limitations:

- On every power up, the initial values of the four REF6050 devices may be different from each other, which leads to again error mismatch between the four channels.
- The temperature drift of the four REF6050 devices is very low; however, this temperature drift does not correlate between the four channels.
- Four independent reference circuits increase the bill-of-materials (BOM) and add to the power consumption and PCB area.

Figure 20 shows a optimum reference solution with a single reference source followed by individual, discrete, external reference buffer for each SAR ADC.

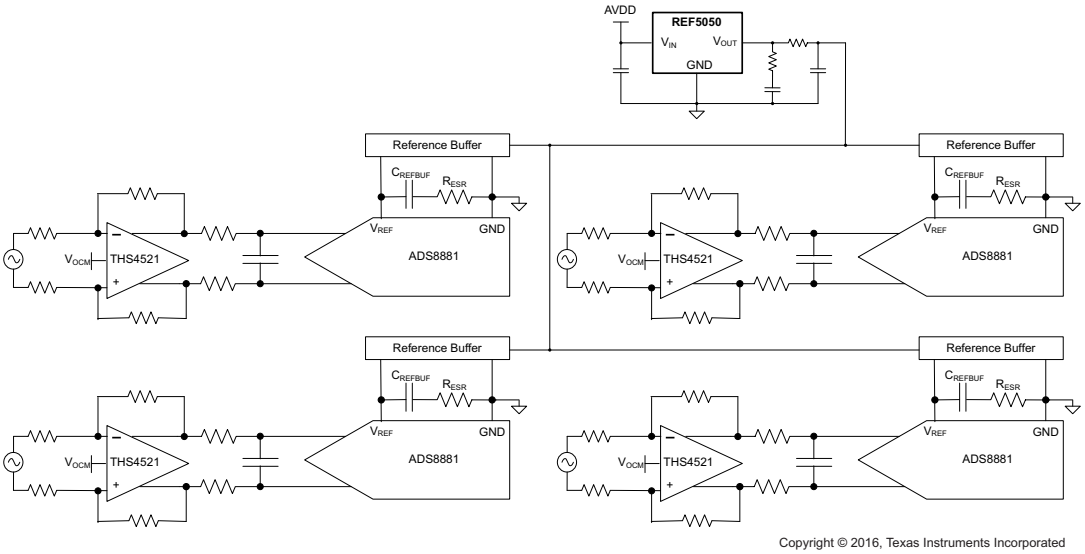

Figure 20. Individual External Reference Buffer Per ADC

The reference buffer can be realized using a single amplifier having high bandwidth, low open-loop output impedance, low offset, and low drift specifications as shown in Figure 21 or by using a composite amplifier circuit as shown in Figure 22.

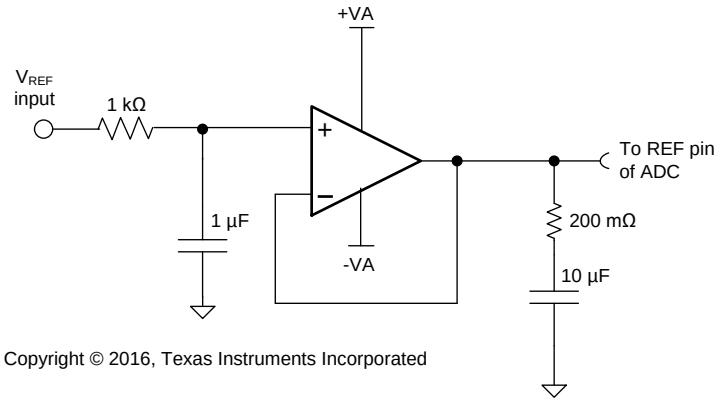

Figure 21. Single Amplifier Implementation

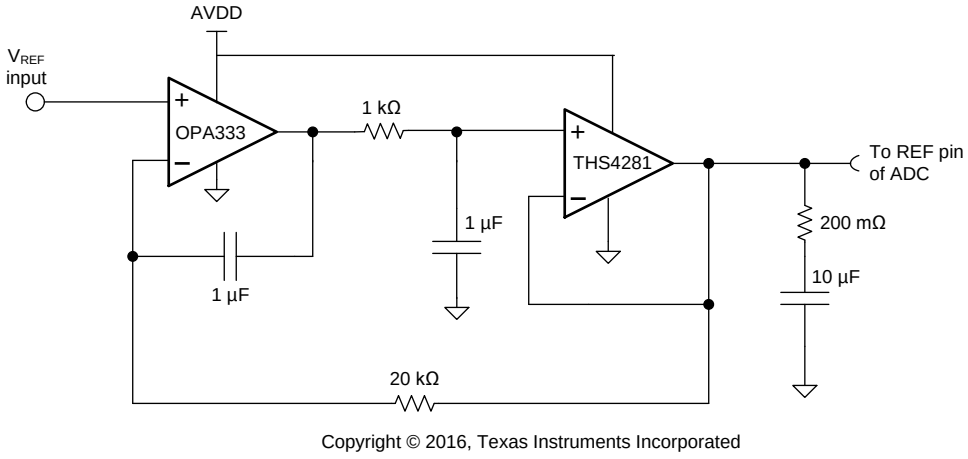

Figure 22. Composite Amplifier Implementation

The topology shown in Figure 21 generally results in using an amplifier with high quiescent current and high-output headroom requirements. The topology shown in Figure 22 achieves the rated performance with a greatly reduced power consumption, but with a much higher component count (refer to *TIPD115: 18-Bit, 1-MSPS Data Acquisition (DAQ) Block Optimized for Lowest Distortion and Noise* for details of design).

If the reference buffer is integrated within the SAR ADC, the design simplifies to:

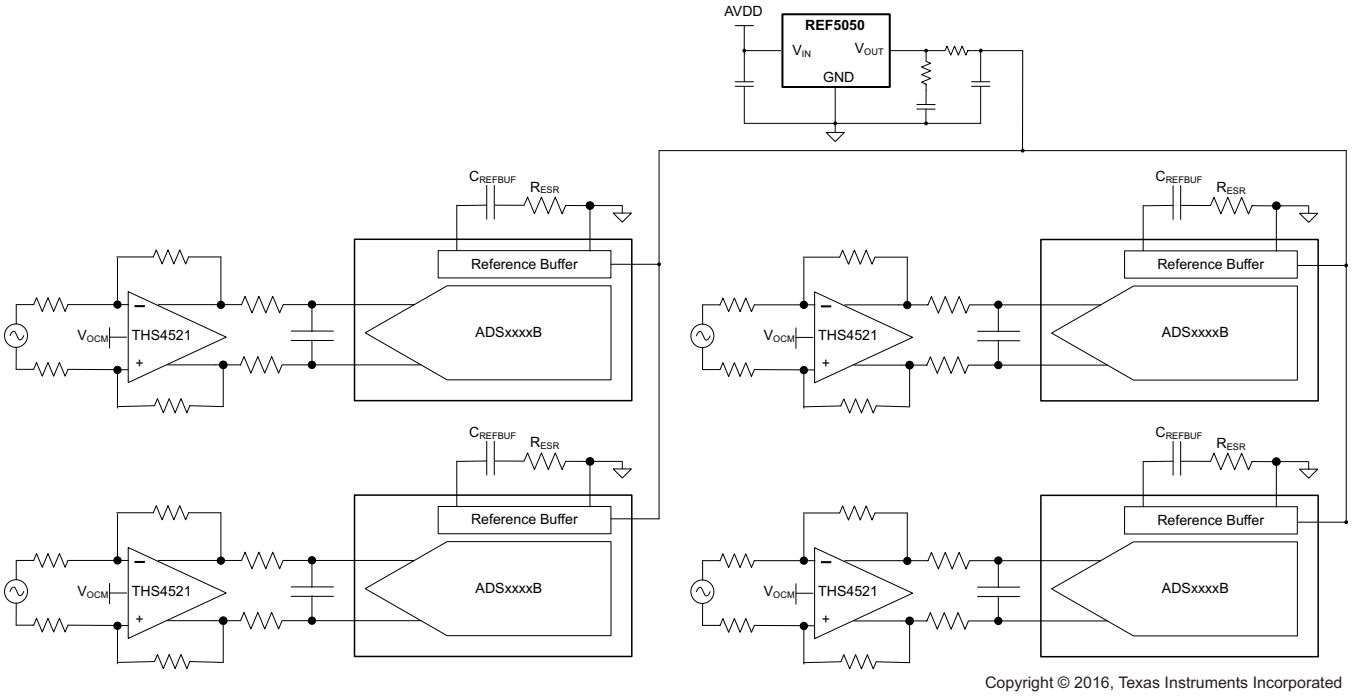

Figure 23. Simplified Design With Reference Buffer Integrated Within SAR ADC

6 Component Selection

The primary goal of this TI Precision Design is to create a data acquisition system that delivers four high-speed, simultaneous sampling channels with 20-bit precision performance and low channel-to-channel interference in a small PCB area and with low power consumption.

6.1 SAR ADC Selection

As shown in Figure 20, having an individual reference buffer per ADC is essential to achieve the performance specifications of the SAR ADC and also to limit the channel-to-channel interference. An SAR ADC with an integrated reference buffer eliminates a major design challenge and also helps to reduce the PCB size.

The Texas Instruments' ADS8900B integrates this reference buffer and the SAR ADC in one package and all the performance specifications are at the full-chip level (a combination of the SAR ADC and the internal reference buffer). As Table 2 shows, the ADS8900B device meets or exceeds all the design requirements:

Table 2. Comparison of Design Goal and Measured Performance

PARAMETER	DESIGN REQUIREMENT	ADS8900B SPECIFICATION
ADC sample rate	1-MSPS	1-MSPS
Resolution	20 bits	20 bits
Linearity	20-bit NMC, < ±1.5-ppm INL	20-bit NMC, ±1-ppm INL (typ)
Noise performance	> 102 dB SNR	104.5 dB (typ)
Distortion	< –120 dB	–125 dB (typ)
Power supply	< 5.5-V analog, 3.3-V I/O	Single analog supply, RVDD (3 V to 5.5 V), Separate I/O supply, DVDD (1.65 V to 5.5 V)
Power consumption	Low	21 mW at 1 MSPS (Including internal reference buffer and LDO)
PCB size	Minimum	4.0 mm × 4.0 mm, QFN Integrated reference buffer and LDO

By implementing the ADS8900B SAR ADC, the design block diagram simplifies to the following Figure 24:

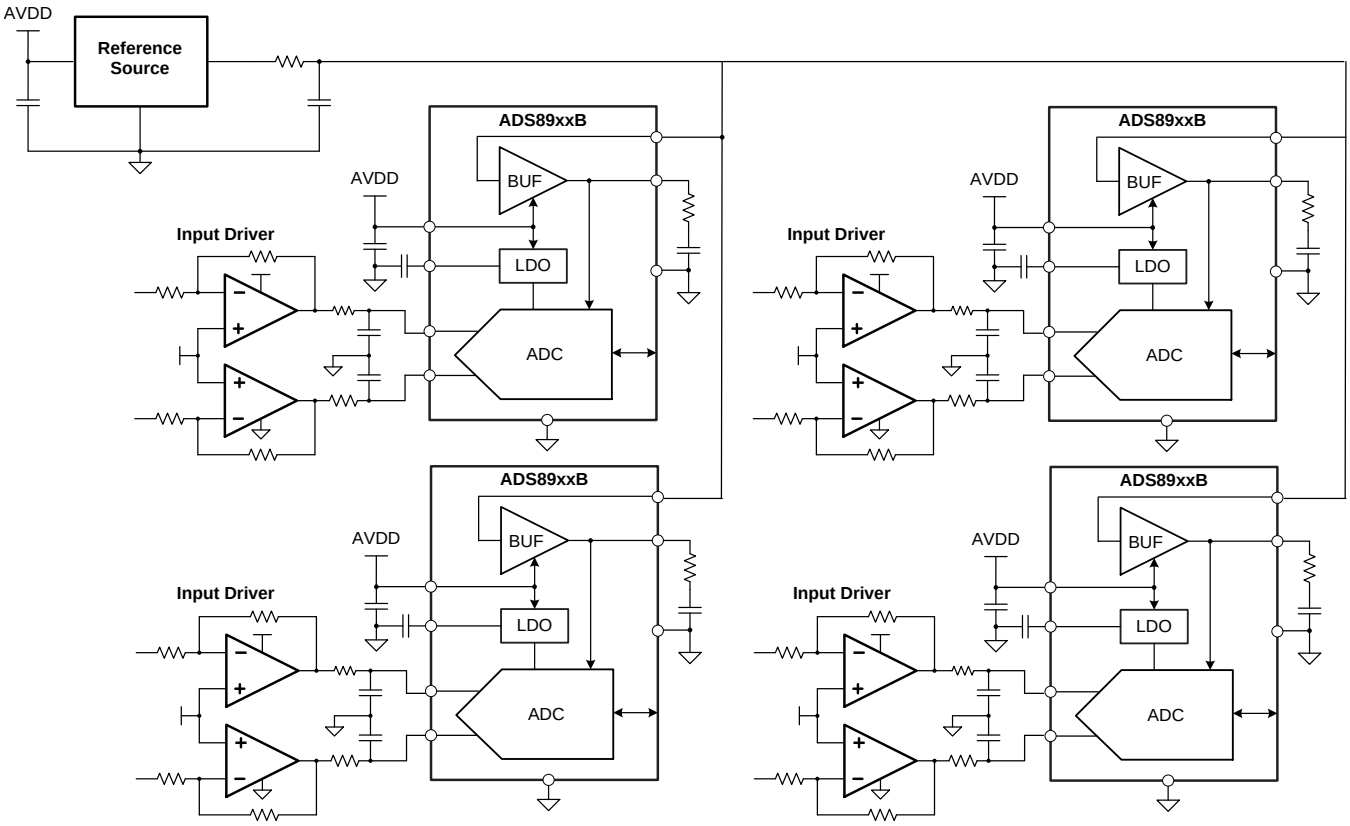

Figure 24. System Block Diagram Using 4x ADS8900B

To achieve the rated performance of the ADS8900B, this design uses C_{REFBUF} of 22 µF and R_{ESR} of 1 Ω, as specifed in the ADS8900B data sheet.

6.2 Reference Selection

After integrating the reference buffer inside the ADS8900B, the reference component selection narrows down to the selection of the reference source and the selection of the passive components.

6.2.1 Reference Source Selection

The reference source must provide a low-drift, low-noise, and accurate voltage for ADC conversion process. Table 3 shows the specifications of the REF5050 device from TI.

Table 3. Key specifications of REF5050

PARAMETER	DATA SHEET SPECIFICATION
Power supply	Up to 18 V
Output voltage	5 V
Initial accuracy	± 0.05 %
Output voltage noise (0.1 Hz to 10 Hz)	3 μV_{pp}/V
Temperature drift	3 ppm/°C (Max)

As Figure 25 shows, this design uses C_L of 10-µF and an ESR of 0.1 Ω for lower noise and easy power up.

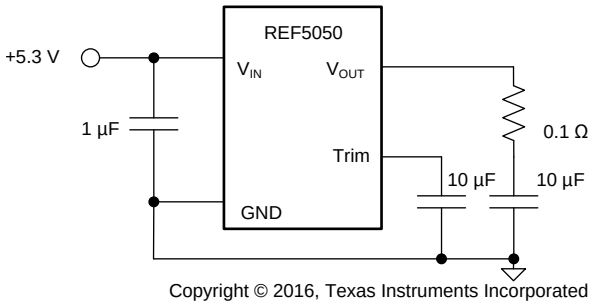

Figure 25. REF5050 and Associated Components

6.2.2 Passive Components Selection

As Section 5.4 details, the noise from the reference source must be bandwidth limited by designing a low-pass RC filter at the reference source output. According to Equation 26, the maximum value of the 3-dB bandwidth for this filter can be calculated as shown in Equation 32:

$$f_{REF\_3dB} \leq \frac{2 \times I_{Q\_REF}(uA)}{(10000\ nV/\sqrt{Hz})^2} \times \frac{2}{\pi} \times \left[\frac{1}{9} \times \frac{V_{FSR}{}^2}{8} \times 10^{\frac{SNR(dB)}{10}} - \left(\frac{V_{1/f\_REF\_pp}}{6.6}\right)^2\right]$$

$$f_{REF\_3dB} \leq 562Hz \tag{32}$$

Select C_{REF_FLT} = 10 µF to keep the thermal noise of the capacitor at a low value. The minimum value of R_{REF_FLT} can be calculated using Equation 27 as:

$$R_{REF\_FLT} \geq \frac{1}{2\pi \times 562 \times 10 \times 10^{-6}} = 28\ \Omega \tag{33}$$

As shown in Figure 26, this design uses R_{REF_FLT} = 1 kΩ to further reduce the bandwidth of the filter so that the broadband noise contribution from the reference is negligible.

With C_{REF_FLT} = 10 µF and R_{REF_FLT} = 1 kΩ, the reference filter bandwidth is:

$$f_{REF\_3dB} = \frac{1}{2 \times \pi \times R_{REF\_FLT} \times C_{REF\_FLT}} = 16Hz \tag{34}$$

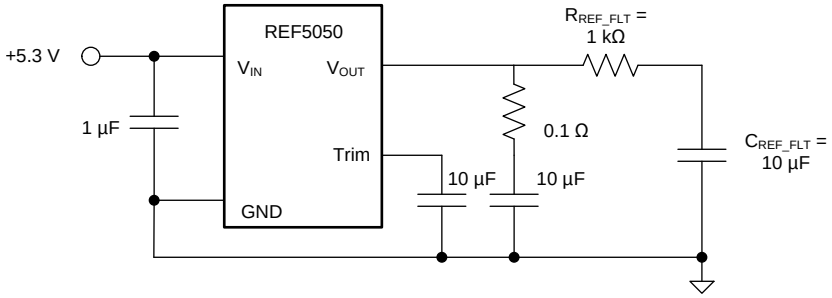

Figure 26. Reference RC Filter

6.3 Component Selection for Input Driver Circuit

6.3.1 RC-Filter Passive Components Selection

The critical passive components for this design are the resistor (R_{FLT}) and capacitor (C_{FLT}) for the charge kickback filter at the input of the ADC. The tolerance of the selected resistor must be < 1%. The COG (NPO) capacitors are appropriate for this application because of their high Q, low temperature coefficient, and stable electrical characteristics under varying voltages, frequencies, and times.

As explained in Equation 4:

$$R_{FLT} < \frac{R_{SWITCH}}{20} \tag{35}$$

From the datasheet of ADS8900B, R_{SH} = 50 Ω; therefore:

$$R_{FLT} < 2.5\Omega \tag{36}$$

Choose R_{FLT} = 2.2 Ω.

As explained in Section 5.2:

$$R_{FLT} \geq \frac{R_O}{9} \tag{37}$$

To meet both criteria, choose amplifier with output impedance less than the calculated value in Equation 38 at 2-kHz:

$$R_o \leq 2.2 \times 9 = 19.8\Omega \tag{38}$$

As explained in Section 5.2:

$$C_{FLT} \geq 20 \times C_{SH} \tag{39}$$

From the data sheet of the ADS8900B device, C_{SH} = 60 pF, therefore:

$$C_{FLT} \geq 1.2nF \tag{40}$$

To limit the broadband noise contribution, this design uses C_{FLT} = 10 nF.

Therefore the bandwidth of the charge kickback filter is:

$$BW_{FLT} = \frac{1}{2 \times \pi \times R_{FLT} \times C_{FLT}} = 7.2MHz \tag{41}$$

Figure 27 shows the charge kickback filter for this design.

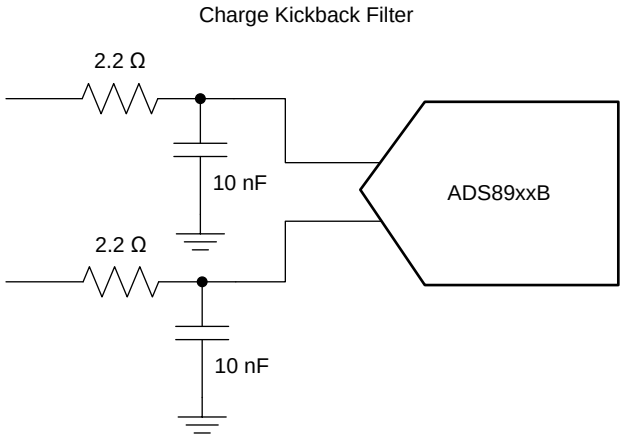

Figure 27. Charge Kickback Filter

6.3.2 Amplifier Selection

As Equation 42 shows, a system level SNR specification of 102 dB translates an RMS noise specification of 28.1 µV.

$$V_{n\_TOT\_RMS} = \frac{V_{FSR}}{\left(2 \times \sqrt{2} \times 10^{\left(\frac{SNR_{SYSTEM}}{20}\right)}\right)} = 28.1\mu V \tag{42}$$

From the ADS8900B data sheet:

$$V_{n\_ADC\_RMS} = \frac{V_{FSR}}{\left(2 \times \sqrt{2} \times 10^{\left(\frac{SNR_{ADC}}{20}\right)}\right)} = 21\mu V \tag{43}$$

Therefore:

$$V_{n\_DIFF\_AMP\_RTO\_RMS} < \sqrt{(V_{n\_TOT\_RMS}{}^2 - V_{n\_ADC\_RMS}{}^2)} < 18.7\mu V \tag{44}$$

But:

$$V_{n\_DIFF\_AMP\_RTO\_RMS} = 2 \times \sqrt{1.57 \times BW_{FLT}} \times \sqrt{2 \times V_{n\_AMP}^2 + 4kTR} \tag{45}$$

With the selected charge kickback filter, to reduce $V_{n\_DIFF\_AMP\_RTO\_RMS}$, select an amplifier with a lower noise density (V_{n_AMP}), use a lower value resistors (R), or both. However, lower value resistors result in higher power consumption. To keep the power consumption optimum, this design uses R = 1 kΩ. :

The design uses an OPA2625 as the input driver amplifier. Table 4 shows key specifications of the OPA2625.

Table 4. Key Specifications of OPA2625

PARAMETER	DATA SHEET SPECIFICATION
Power supply	Up to 5.5 V
THD	< –130 dB
Slew rate	45 V/µs
Voltage noise	3.2 nV/√Hz
Output Impedance	9 Ω

With OPA2625, R = 1 kΩ, and BW_{FLT} = 7.2 MHz, the noise contribution of the input driver circuit is calculated in Equation 46:

$$V_{n\_DIFF\_AMP\_RTO\_RMS} = 2 \times \sqrt{1.57 \times BW_{FLT}} \times \sqrt{2 \times V_{n\_AMP}^2 + 4kTR} = 36\ \mu V \tag{46}$$

The input driver circuit noise is higher than calculated in Equation 44. The input driver is modified to operate in an inverting low-pass filter configuration to reduce the bandwidth and in effect the input driver noise contribution.

For this design, select C_{FB} = 1 nF. Therefore, the effective bandwidth (for integrated noise) is:

$$BW_{ILPF} = \frac{1}{2 \times \pi \times R \times C_{FB}} = 160kHz \tag{47}$$

Substitute the value to get: Equation 48:

$$V_{n\_DIFF\_AMP\_RTO\_RMS} = 2 \times \sqrt{1.57 \times BW_{ILPF}} \times \sqrt{2 \times V_{n\_AMP}{}^2 + 4kTR} = 6.1\mu V \tag{48}$$

Figure 28 shows the complete design with component values.

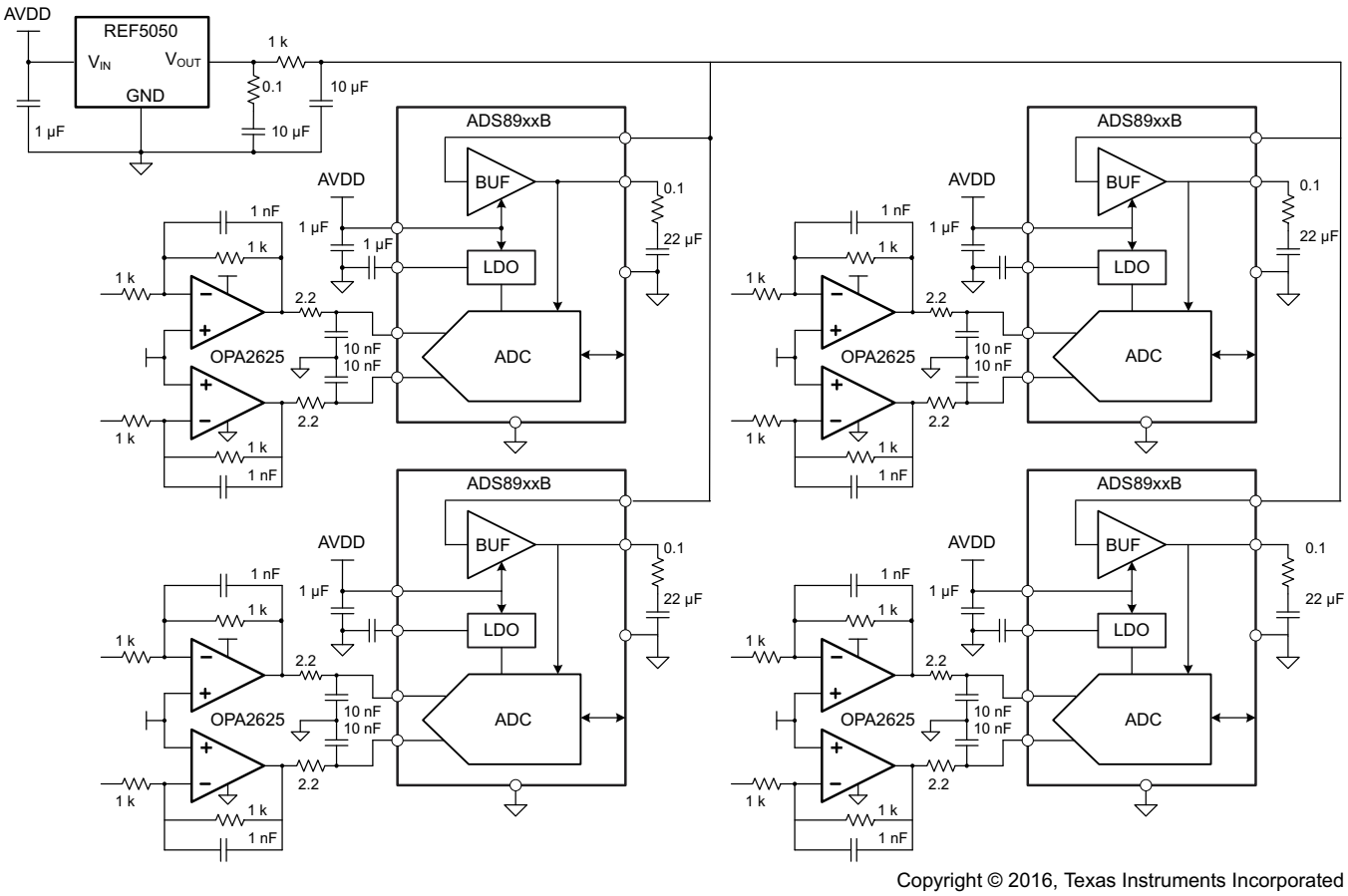

Figure 28. Design Details

7 Simulation

Figure 29 shows the TINA-TI schematic for the design.

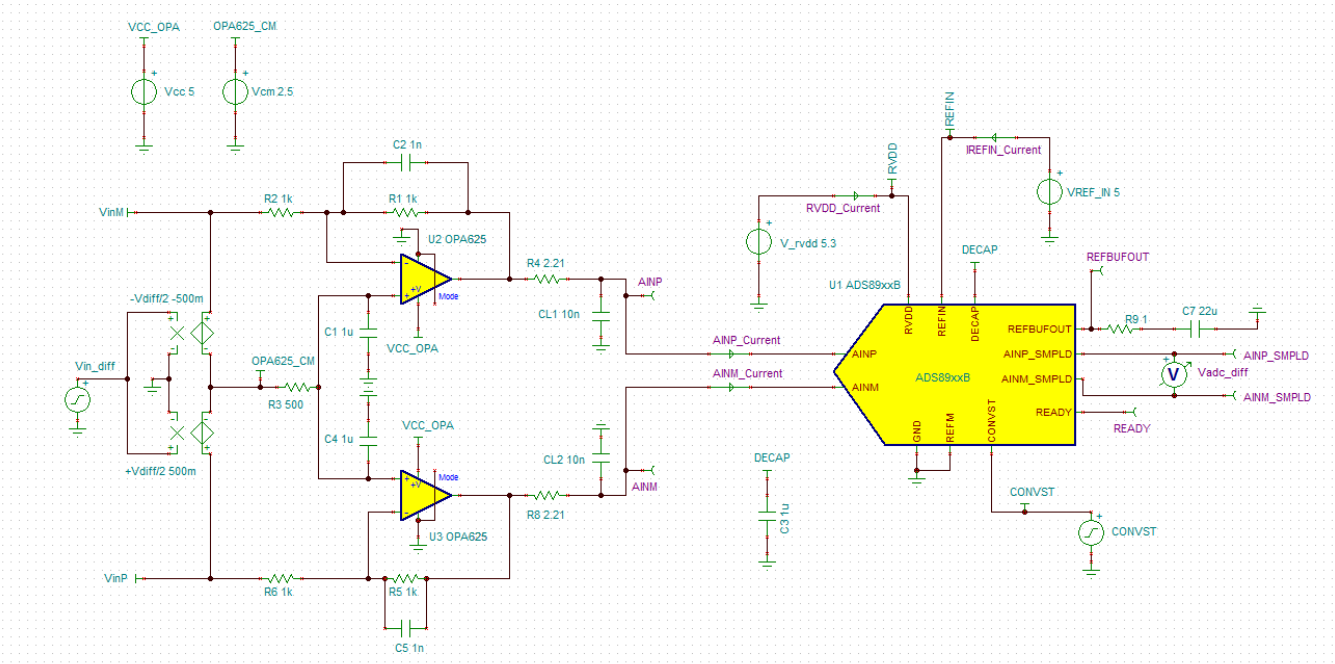

Figure 29. TINA-TI™ Schematic for Design

The input driver circuit is simulated for stability, noise, and transient settling. The reference circuit is simulated for settling.

7.1 Stability Analysis of Input Driver Circuit

To check the stability of the input driver circuit, a step input of 2 V is applied to the inputs and the output waveforms are monitored.

The output settles to the final value and does not show any oscillations. The designed circuit is stable for a step input and does not introduce unwanted signal. Figure 30 shows the resultant output waveform for the step input.

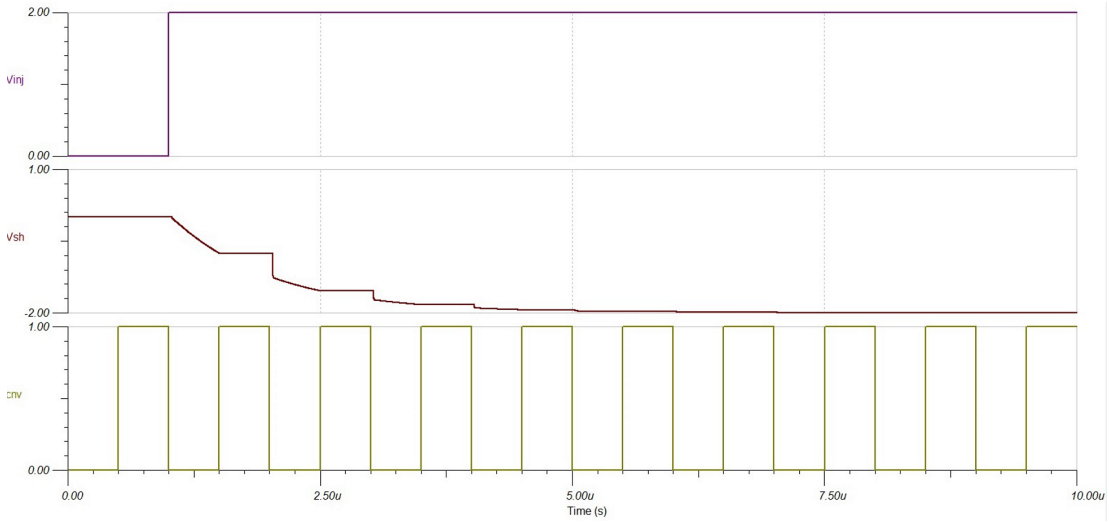

Figure 30. Input Settling for Step Input

7.2 Noise Analysis of Input Driver Circuit

Figure 31 shows the TINA-TI™ schematic used to simulate the integrated RMS noise of the input driver.

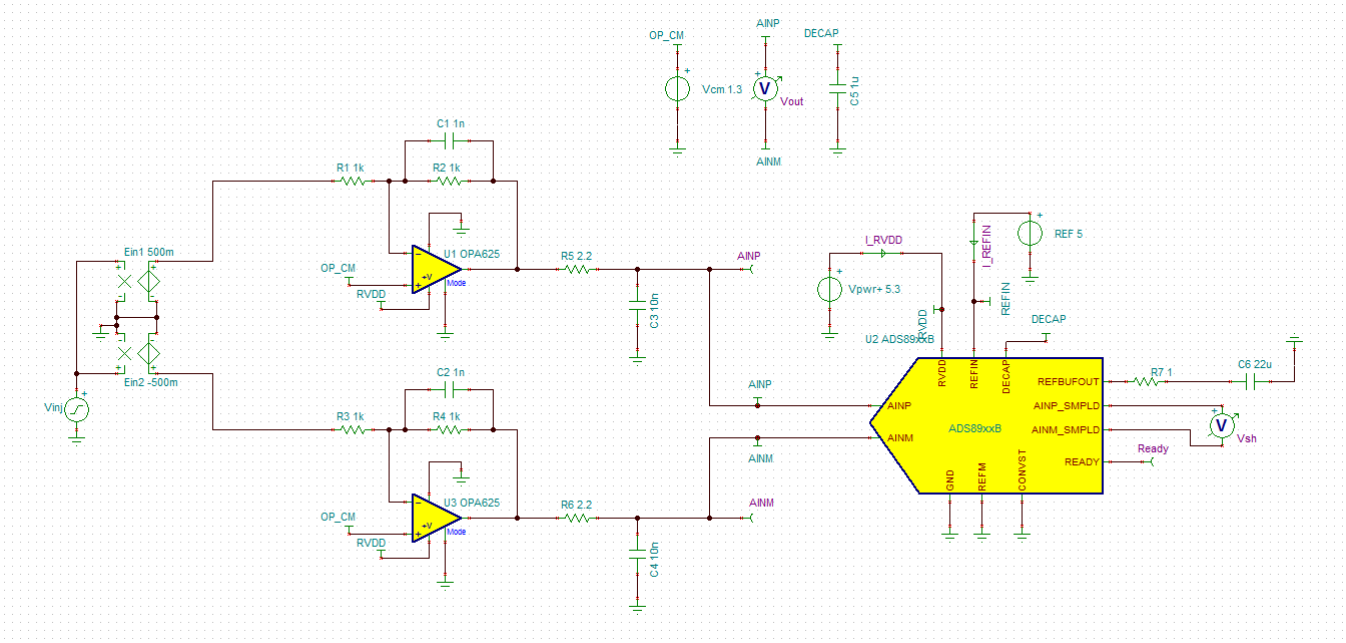

Figure 31. Schematic for Input Driver Noise Analysis

Ideally, to calculate the referred-to-output (RTO) noise from the input driver, the voltage noise density curve must be integrated to infinity. For a realistic approximation of the RTO noise; integration to a decade beyond the bandwidth of the system is sufficient. Figure 32 shows that the simulated integrated noise from the fully differential amplifier input driver referred to the output is 15 μV_{RMS}, which meets the design requirements.

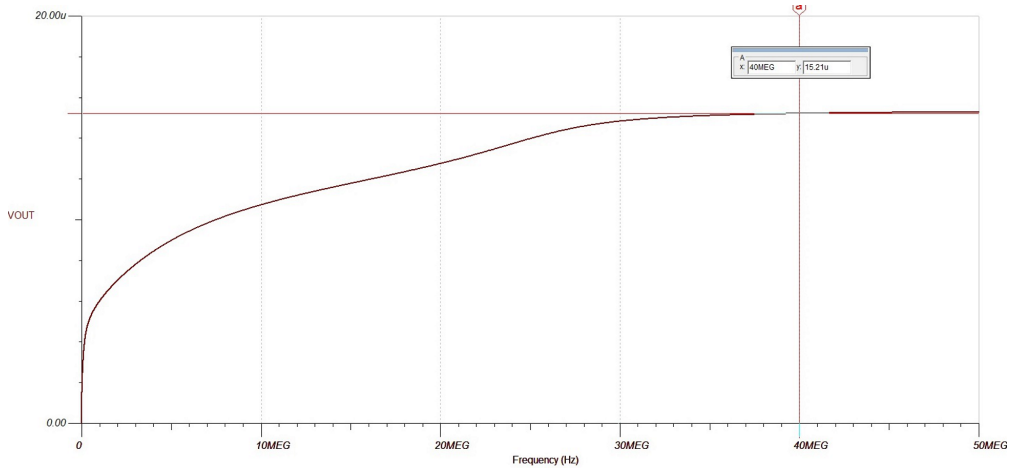

Figure 32. Integrated RMS Noise for Input Driver

7.3 Transient Analysis of Input Driver Circuit

The TINA-TI™ schematic shown in Figure 29 is used to check the accurate settling of the sine-wave signal at the inputs of the ADC during sampling phase. The simulated time-domain response for the circuit is shown in Figure 33 and Figure 34.

Figure 33 shows one cycle of a 10-kHz sine-wave with an amplitude of ±4.9 V applied at the differential inputs of the ADS8900B. In these figures, the signal *Vin* represents the actual input signal at the differential inputs of the ADC and the signal *Vsh* shows the output of the ADCs input sample-and-hold circuit, as explained in Section 5.2. Figure 34 shows the same waveform zoomed-in on time scale for more details. The curves are collated together to show that the sampled signal accurately tracks the input signals during sampling and stays on hold when the ADC is converting.

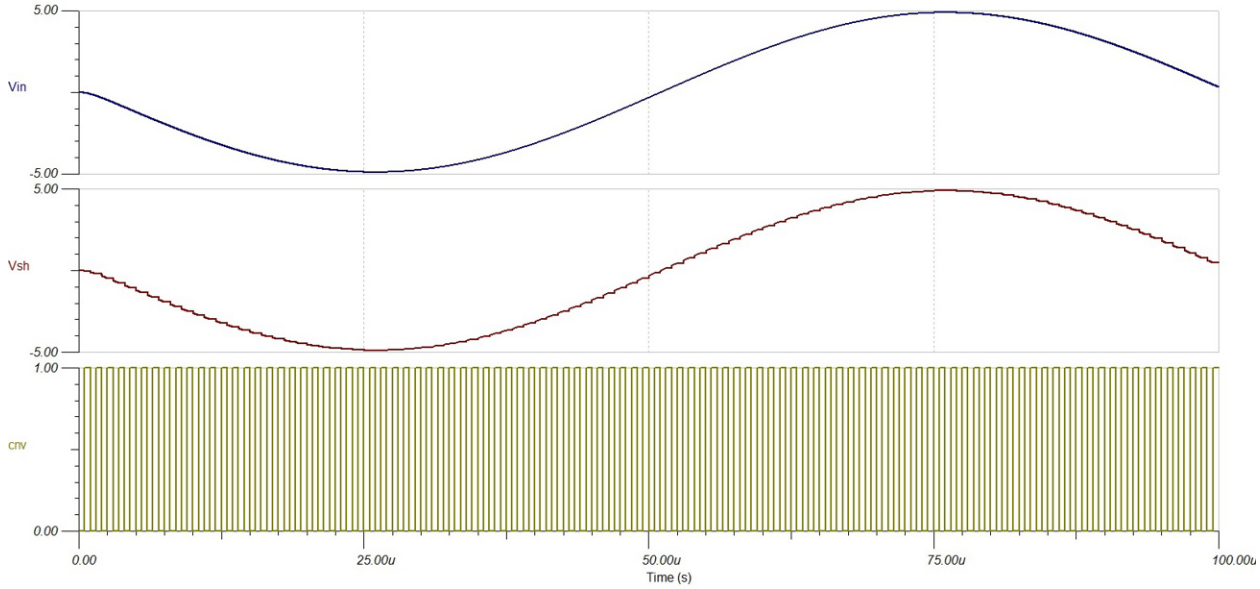

Figure 33. Digitization of Input Sine-Wave Showing ADC Sample and Hold

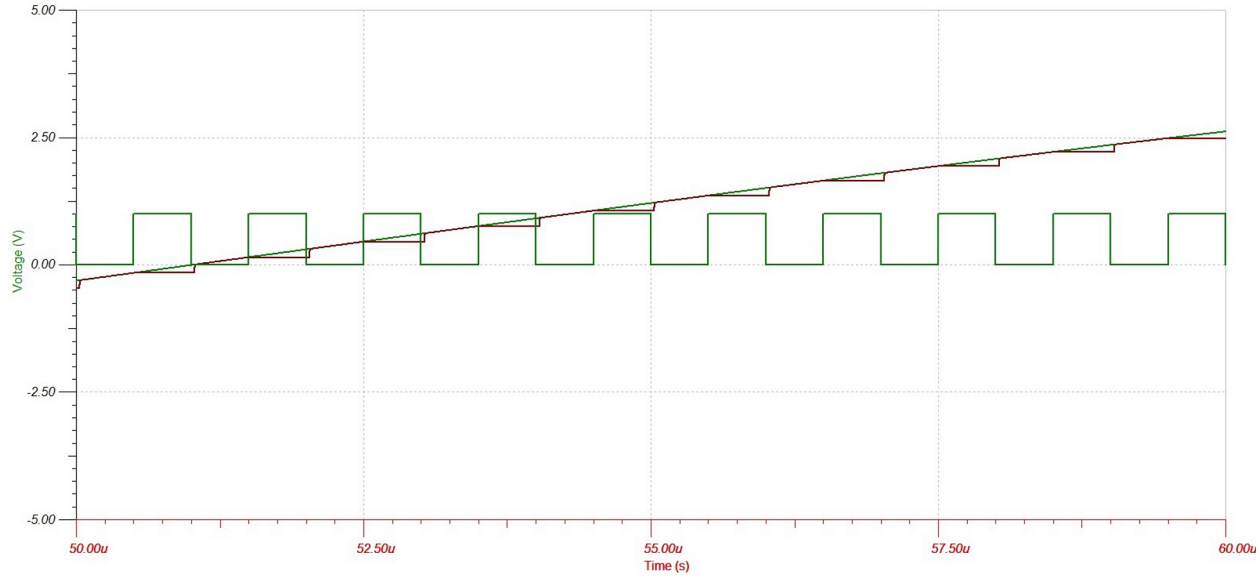

Figure 34. Digitization of Input Sine-Wave Showing ADC Sample and Hold—Zoomed

7.4 Settling Response of ADC Reference Input

The TINA-TI™ schematic shown in Figure 29 is used to check the settling of the reference buffer output (REFBUFOUT) of the ADS8900B. As explained in Section 5.4, to maintain the overall system performance, the voltage at the REFBUFOUT pin must settle to less than one LSB of the ADS8900B ADC.

For V_{REF} = 5 V, one LSB of ADS8900B is equal to 9.5 μV. According to the transient simulation plot that shows, the error in the voltage at the REFBUFOUT pin between two successive conversions is ΔV_{REF} = 61 nV, which is significantly less than one LSB (9.5 μV). This result validates that the reference voltage has settled to the sufficient accuracy to maintain the performance of this design.

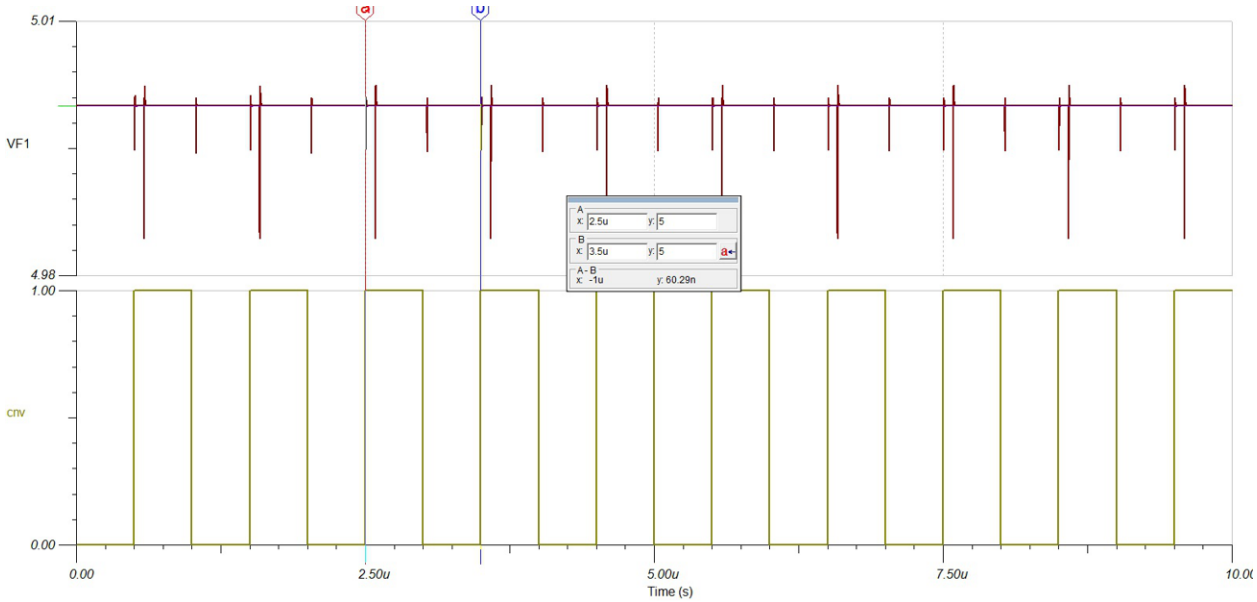

Figure 35. ADC Reference Settling

8 Test Results

This section lists the measurement results for the verification of this design. To measure the channel-to-channel interference and isolation, all measurements were carried out with two setups. The first setup comprises only a single ADS8900B SAR ADC converting its analog input while the other three ADS8900B devices are kept in sampling mode (thereby not presenting any load to the REF5050 device). The second setup comprises all four ADS8900B SAR ADCs simultaneously sampling and converting the analog inputs.

Comparing several different figures of merit for noise shows that the simultaneous sampling system and the single-channel system have similar noise performance. These results show that the system noise performance was not impacted by adding multiple channels and simultaneous sampling.

8.1 DC Noise Measurement

All ADC circuits suffer from some amount of inherent broadband noise contributed by the internal resistors, capacitors, and other circuitry, which is referred to the inputs of the ADC. The front-end driver circuit also contributes some noise to the system, which can also be referred to the ADC inputs. The cumulative noise, often referred to as the *input-referred noise* of the ADC, has a significant impact on the overall system performance.

The most common way to characterize this noise is to use a constant DC voltage as the input signal, collect a large number of ADC output codes, plot a histogram of the output codes, and analyze the distribution characteristics.

Gaussian distribution of output codes in the histogram usually indicates a properly designed system with no missing codes. Alternatively, an output code distribution with large peaks and valleys (distinctly non-Gaussian) probably indicates significant differential nonlinearity (DNL) errors at the system level. These nonlinearity errors can come from insufficient power supply decoupling, improper ground connections, other poor PCB layout effects, and so on. TI recommends to further validate these observations with a single-tone fast Fourier transform (FFT) test and a linearity test.

In this design, the analysis was performed for these two setups and at three different DC input values:

1. $V_{DIFF} = V_{INP} – V_{INM} = 0$; $V_{CM} = V_{REF} / 2$
2. $V_{DIFF} = V_{INP} – V_{INM} = + V_{REF} – \Delta V$; $V_{CM} = V_{REF} / 2$
3. $V_{DIFF} = V_{INP} – V_{INM} = – V_{REF} + \Delta V$; $V_{CM} = V_{REF} / 2$

The following plots show the results:

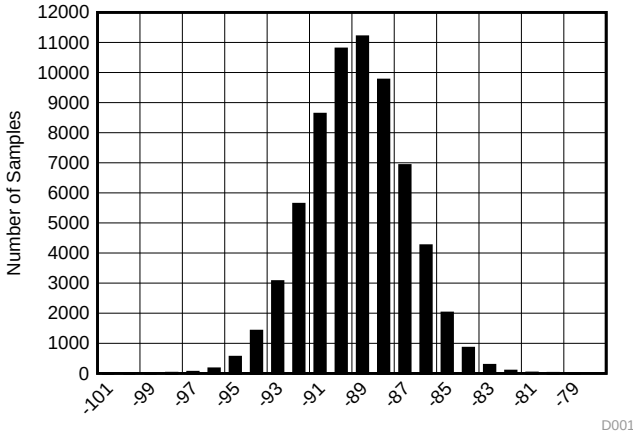

Figure 36. For 0-V (Diff) Input—Single ADC Converting Mean Code = –89 σ = 2.30

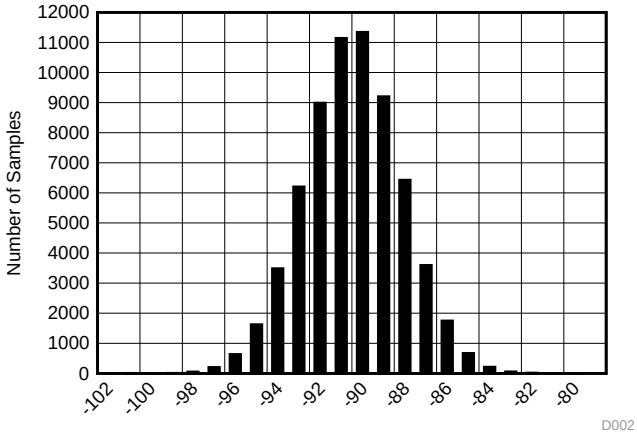

Figure 37. For 0-V (Diff) Input—All Four ADCs Converting Mean Code = –90 σ = 2.29

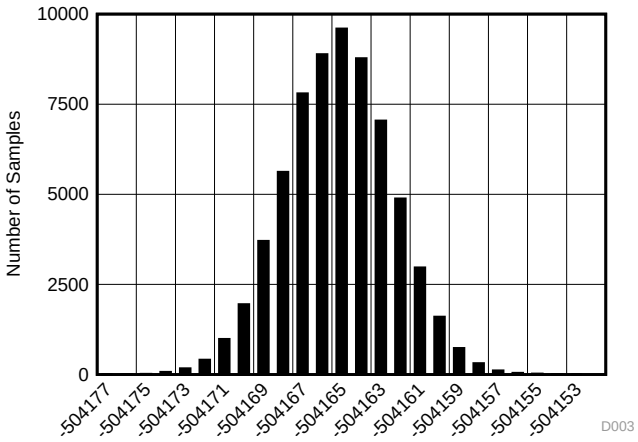

Figure 38. For –4.8-V (Diff) Input—Single ADC Converting
Mean Code = –504165 σ = 2.73

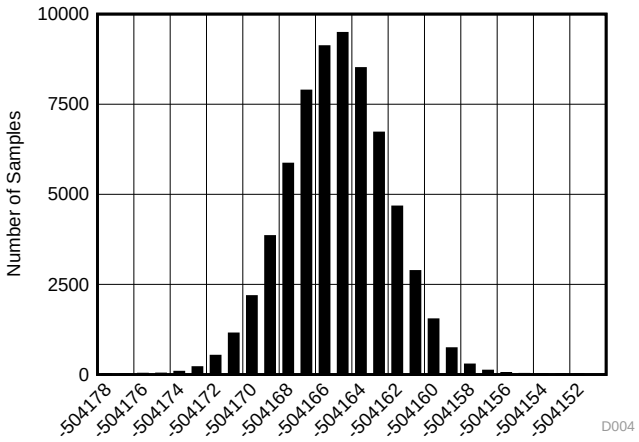

Figure 39. For –4.8-V (Diff) Input—All Four ADCs Converting
Mean Code = –504165 σ = 2.76

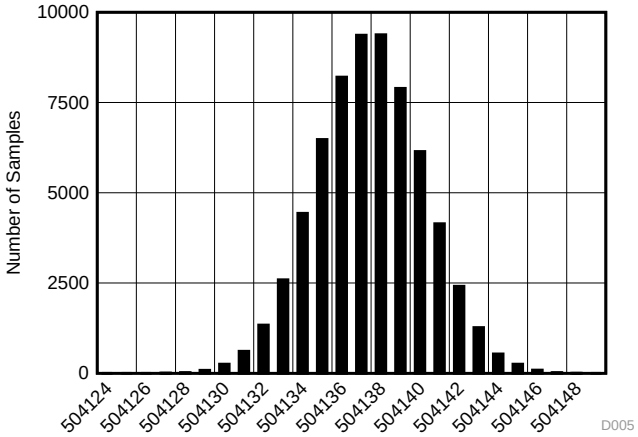

Figure 40. For 4.8-V (Diff) Input—Single ADC Converting
Mean Code = 504137 σ = 2.76

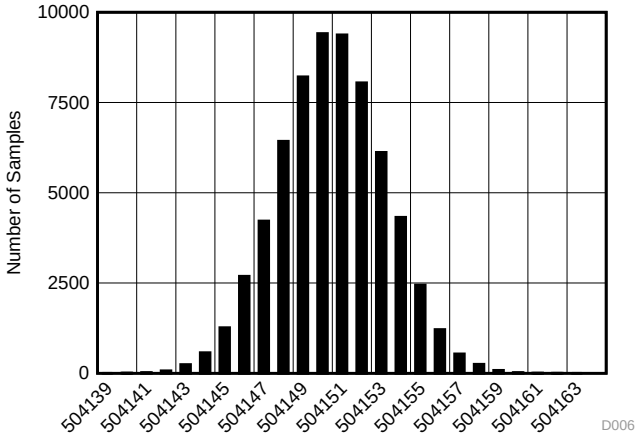

Figure 41. For 4.8-V (Diff) Input—All Four ADCs Converting
Mean Code = 504150 σ = 2.74

As the plots show, the output code distribution is close to Gaussian. Every ADC channel meets the ADS8900B data sheet specifications. The mean output code and the standard deviation of output code for the monitored channel is not affected by the operation of the three other channels.

In conclusion, the design exhibits excellent noise performance and channel-to-channel isolation.

8.2 Single-Tone FFT Analysis and Crosstalk Analysis

In this test, a spectrally pure 2-kHz full-scale tone was applied to the system and the FFT of the output codes were plotted to analyze the noise and distortion performance of the system.

The measurement was performed for two setup conditions:

1. A single ADS8900B converting a full-scale signal of 2 kHz; the other three ADS8900B devices are in sampling mode
2. A single ADS8900B converting a full-scale signal of 2 kHz; the other three ADS8900B devices convert a full-scale signal of 17 kHz

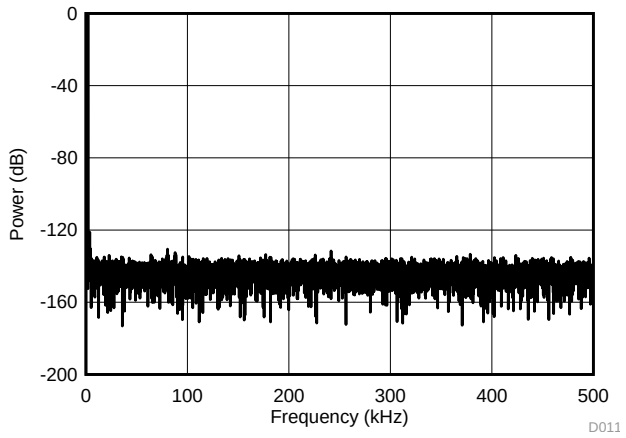

Figure 42. FFT Plot—Single ADC Converting SNR = 102.5 dB THD = –125 dB

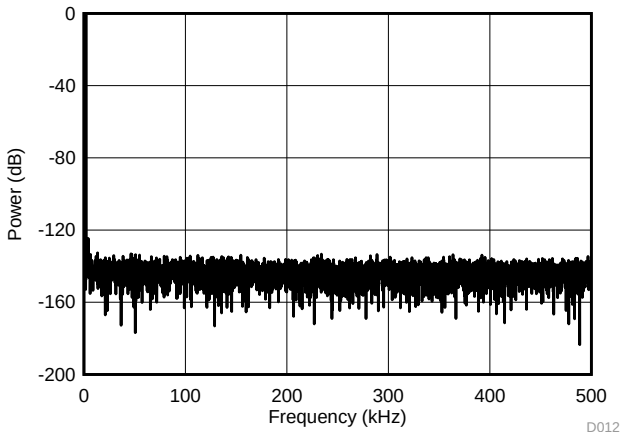

Figure 43. FFT Plot—All Four ADCs Converting SNR = 102.5 dB THD = –125 dB

With the first setup, the results show that the design meets the performance goals of the system and delivers 102.5 dB SNR and –125 dB THD performance.

With the second setup, the results show that the design delivers the exact same performance for the channel being monitored. As a measure of the channel-to-channel isolation, analyze the spectral content around the 17-kHz tone (aggressor). Figure 43 shows that the design delivers channel-to-channel isolation > 110 dB.

Therefore, the other three ADS8900B SAR ADCs that share the REF5050 reference source and operate simultaneously at a full throughput have no adverse effect on the operation and performance of the ADS8900B SAR ADC under test.

In conclusion, the design delivers better than 102-dB SNR, which is better than –125-dB THD and better than 110-dB channel-to-channel isolation.

8.3 System Linearity Measurement

The system level linearity is tested using the histogram method with a sine wave input signal. The measurement was performed for the two setup conditions from Section 8.2.

1. A single ADS8900B device converts a full-scale signal of 2 kHz; the other three ADS8900B devices are in sampling mode
2. A single ADS8900B device converts a full-scale signal of 2 kHz; the other three ADS8900B devices convert a full-scale signal of 17 kHz

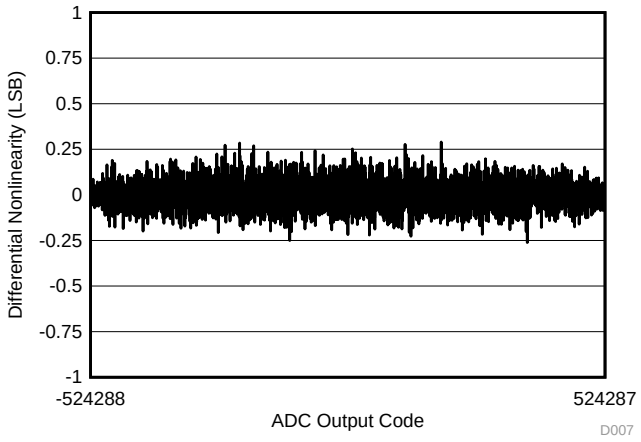

Figure 44. DNL—Single ADC Converting DNL < ± 0.3 ppm

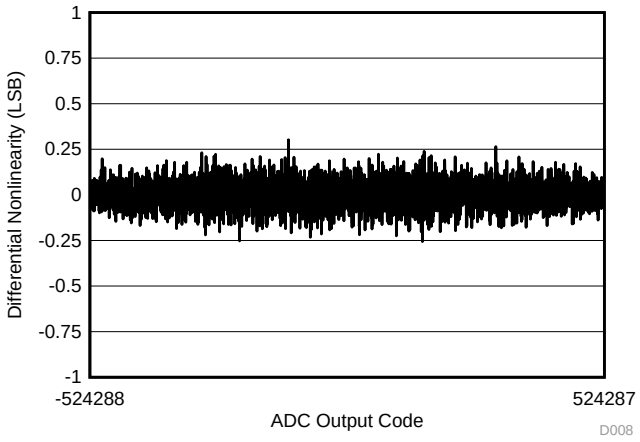

Figure 45. DNL—All Four ADCs Converting DNL < ± 0.3 ppm

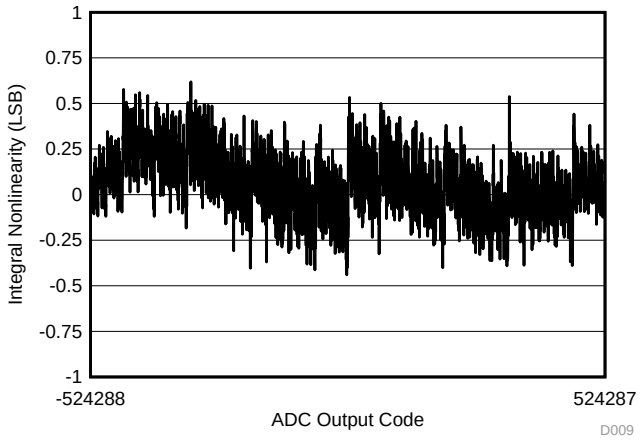

Figure 46. INL—Single ADC Converting INL < ± 0.75 ppm

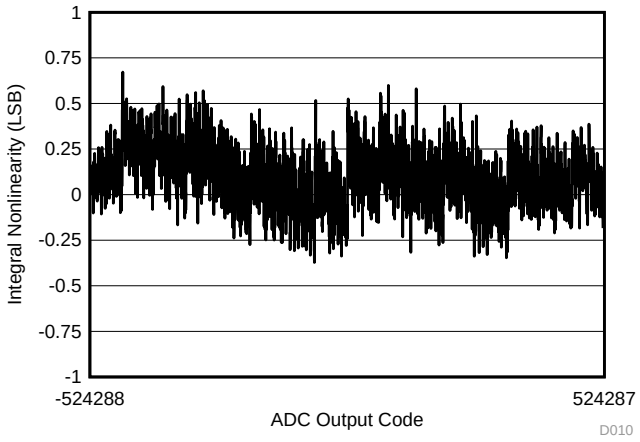

Figure 47. INL—All Four ADCs Converting INL < ± 0.75 ppm

With the first setup, the results show that the design meets the performance goals of the system and delivers an 20-bit NMC DNL and less than ±1-ppm INL at a 20-bit resolution.

With the second setup, the results show that the design delivers the exact same performance for the channel being monitored.

In conclusion, ***the design delivers a 20-bit NMC DNL and better than a ±1-ppm INL at a 20-bit resolution and with excellent channel-to-channel isolation***.

Table 5 summarizes the design goals and performance.

Table 5. Design Goal vs Measured Performance

PARAMETER	GOAL	MEASURED
ADC sample rate	1 MSPS	1 MSPS
No. of channels	Four, simultaneous sampling	Four, simultaneous sampling
Linearity	20-bit NMC, < ±1.5-ppm INL	20-bit NMC, ±1-ppm INL
Noise performance 10-V_{P-P} differential input signal of 2 kHz	> 102 dB SNR	102.5 dB
Distortion	< –120 dB	–125 dB
Channel-to-channel isolation	> 100 dB	> 110 dB
Power supply	< 5.5-V analog, 3.3-V I/O	5.3-V analog, 3.3-V I/O
Power consumption	< 250 mW	210 mW
PCB size (analog blocks)	< 75 sq. cm	< 60 sq. cm

9 Modifications

The ADS8900B comes from a family of pin-to-pin compatible family of 20-/18-/16-bit SAR ADCs with three throughput options, 1 MSPS/500 KSPS/ 250 KSPS, at each resolution. The components selected for this design are also applicable for all other part number within the product family.

Table 6 summarizes the test results obtained with all the part numbers.

Table 6. Measured Performance With ADS89xxB

PARAMETER	ADS8900B	ADS8902B	ADS8904B	ADS8910B	ADS8912B	ADS8914B	ADS8920B	ADS8922B	ADS8924B
Resolution	20	20	20	18	18	18	16	16	16
ADC sample rate	1 MSPS	500 KSPS	250 KSPS	1 MSPS	500 KSPS	250 KSPS	1 MSPS	500 KSPS	250 KSPS
No. of channels	4-ch, Simultaneous								
Linearity	±1 ppm	±1 ppm	±1 ppm	±0.3 LSB at 18 bit	±0.3 LSB at 18 bit	±0.3 LSB at 18 bit	±0.2 LSB at 16 bit	±0.2 LSB at 16 bit	±0.2 LSB at 16 bit
Noise performance 10-V_{P-P} (differential) 2 kHz	102.5 dB	102.5 dB	102.5 dB	101.2 dB	101.2 dB	101.2 dB	96.5 dB	96.5 dB	96.5 dB
Distortion	–125 dB	–125 dB	–125 dB	–125 dB	–125 dB	–125 dB	–125 dB	–125 dB	–125 dB
Channel-to-channel isolation	> 110 dB	> 110 dB	> 110 dB	> 110 dB	> 110 dB	> 110 dB	> 110 dB	> 110 dB	> 110 dB
Power supply	5.3-V analog, 3.3-V I/O								
Power consumption	210 mW								
PCB size (analog blocks)	< 60 sq. cm								

10 Design Files

10.1 Schematics

To download the schematics, see the design files at TIPD211.

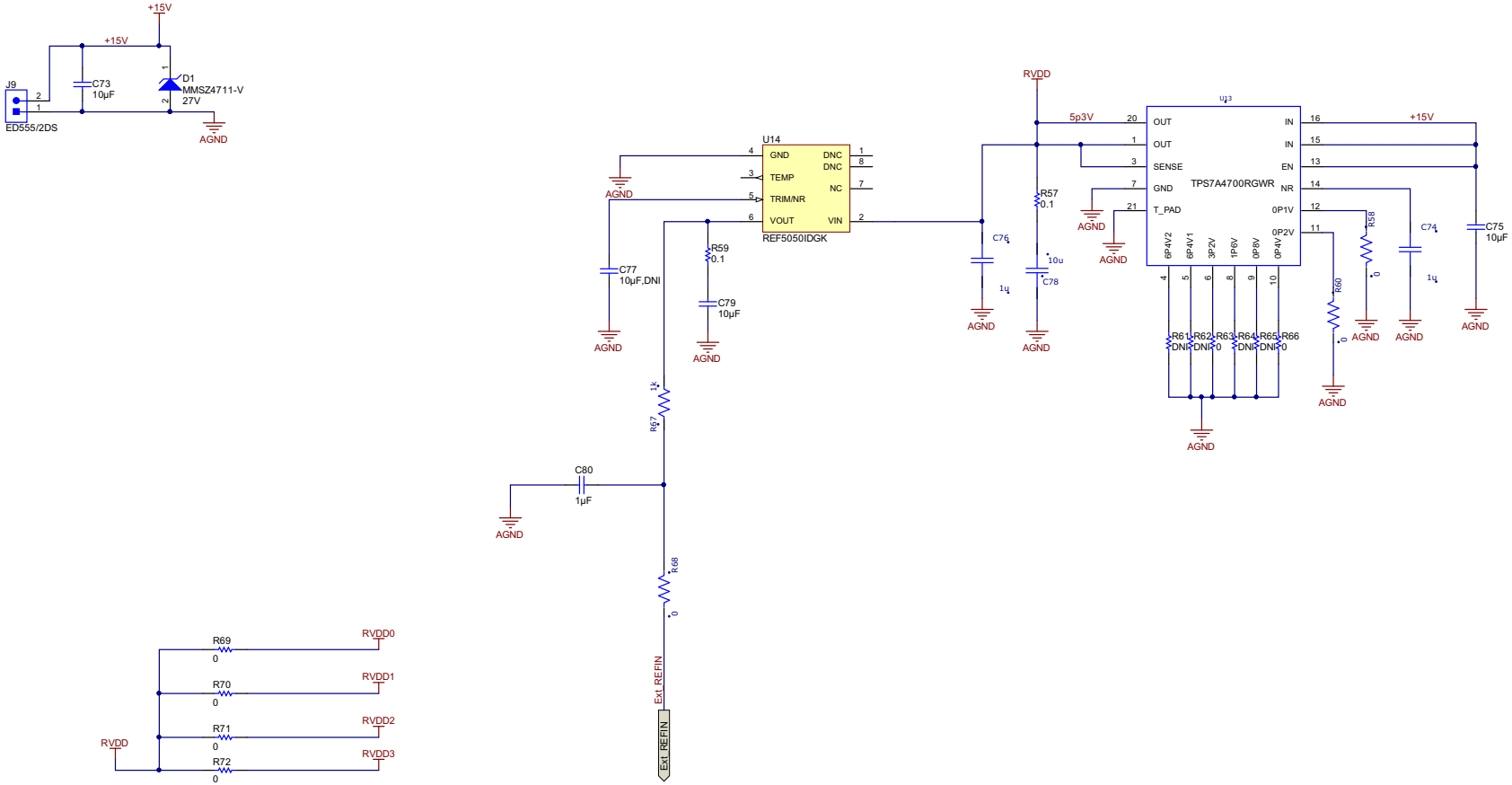

Figure 48. Reference and Power Supply Schematic

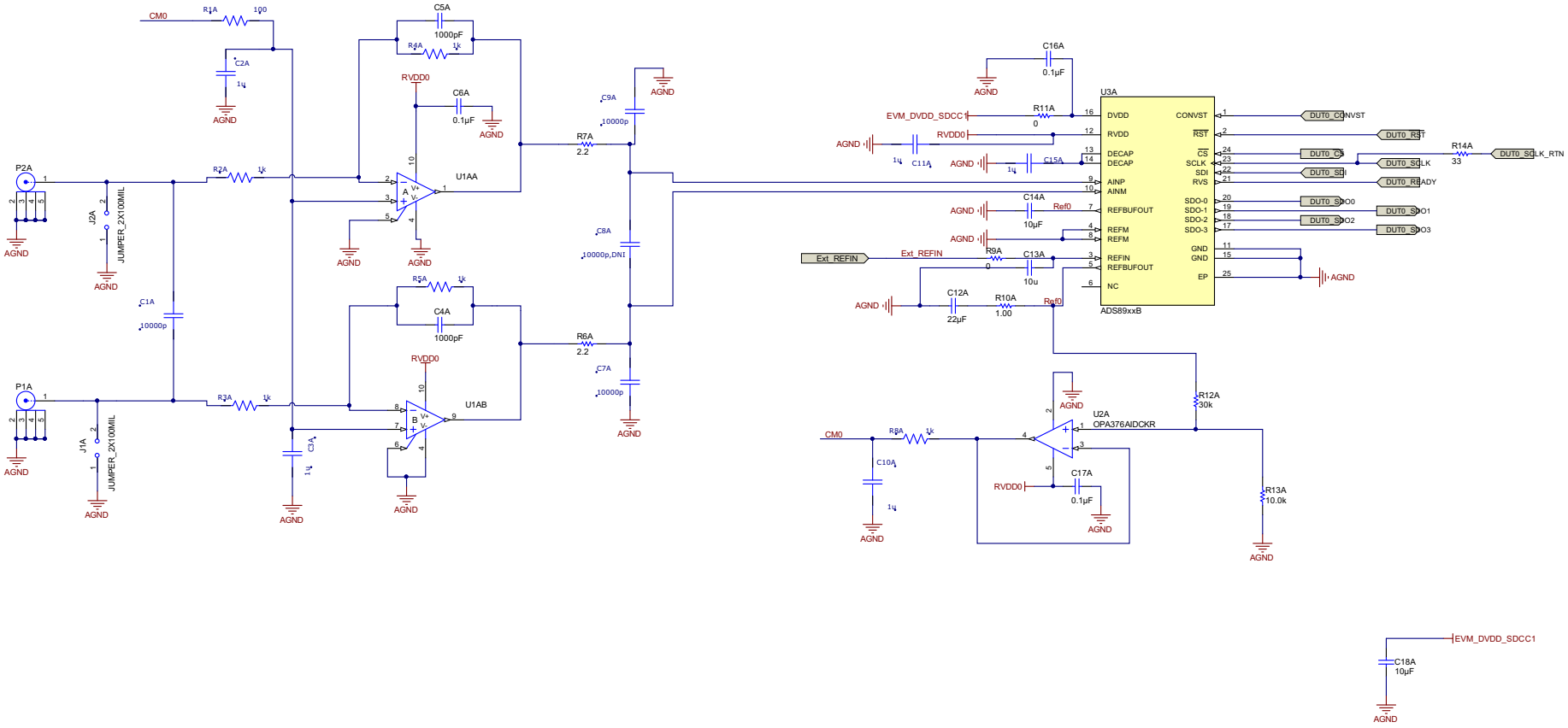

Figure 49. Ch0 Input and Reference Schematic

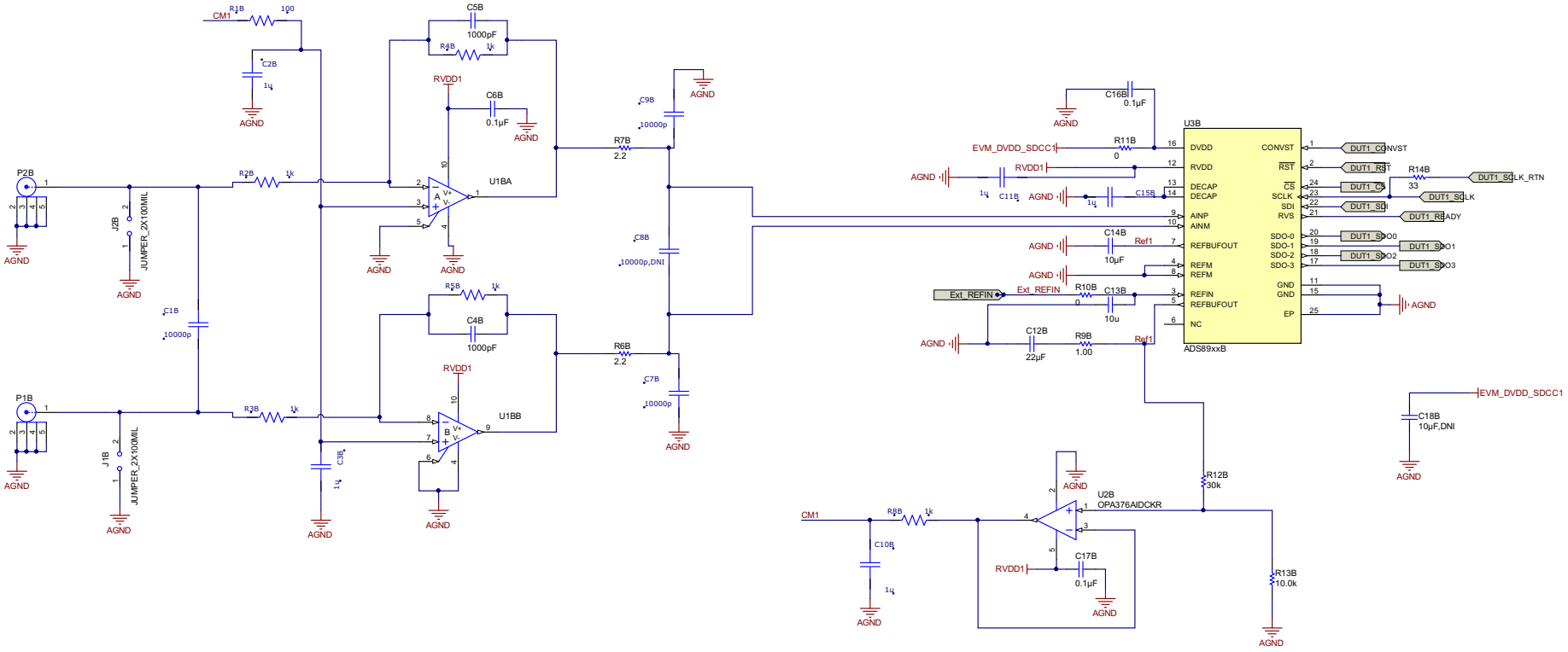

Figure 50. Ch1 Input and Reference Schematic

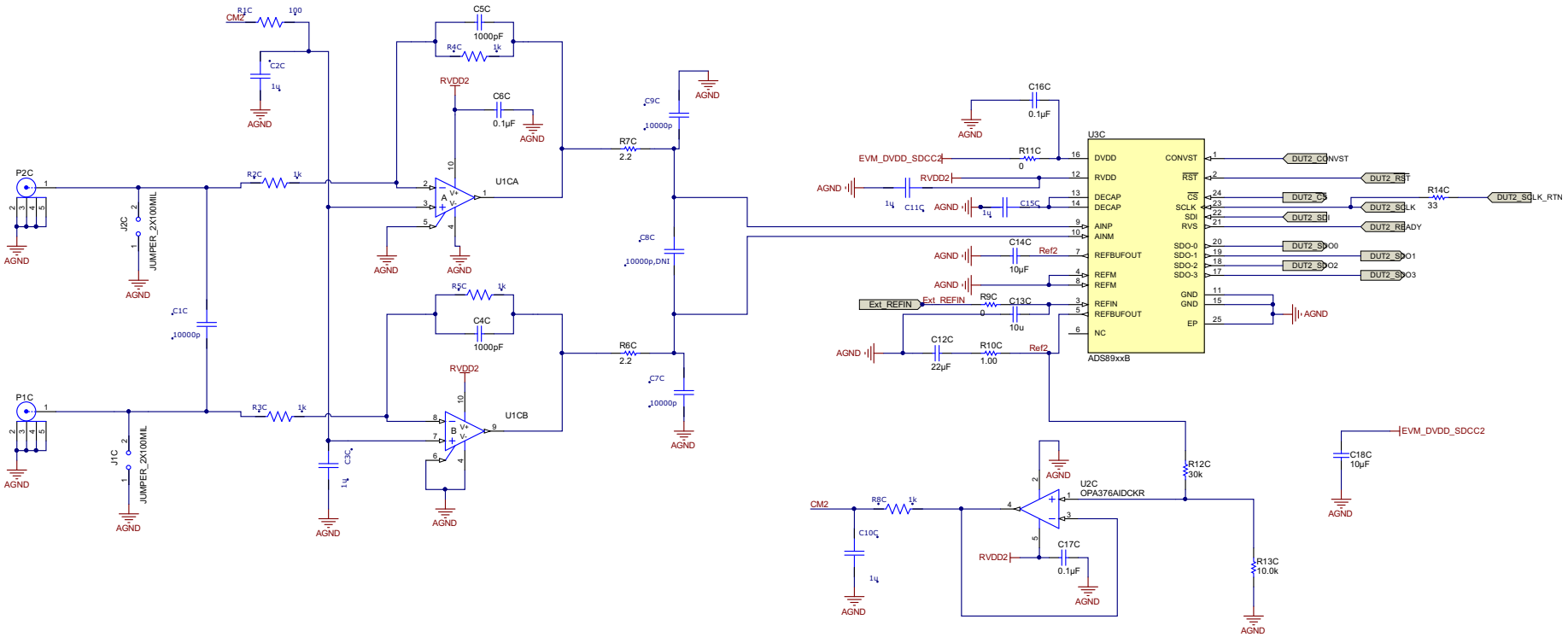

Figure 51. Ch2 Input and Reference Schematic

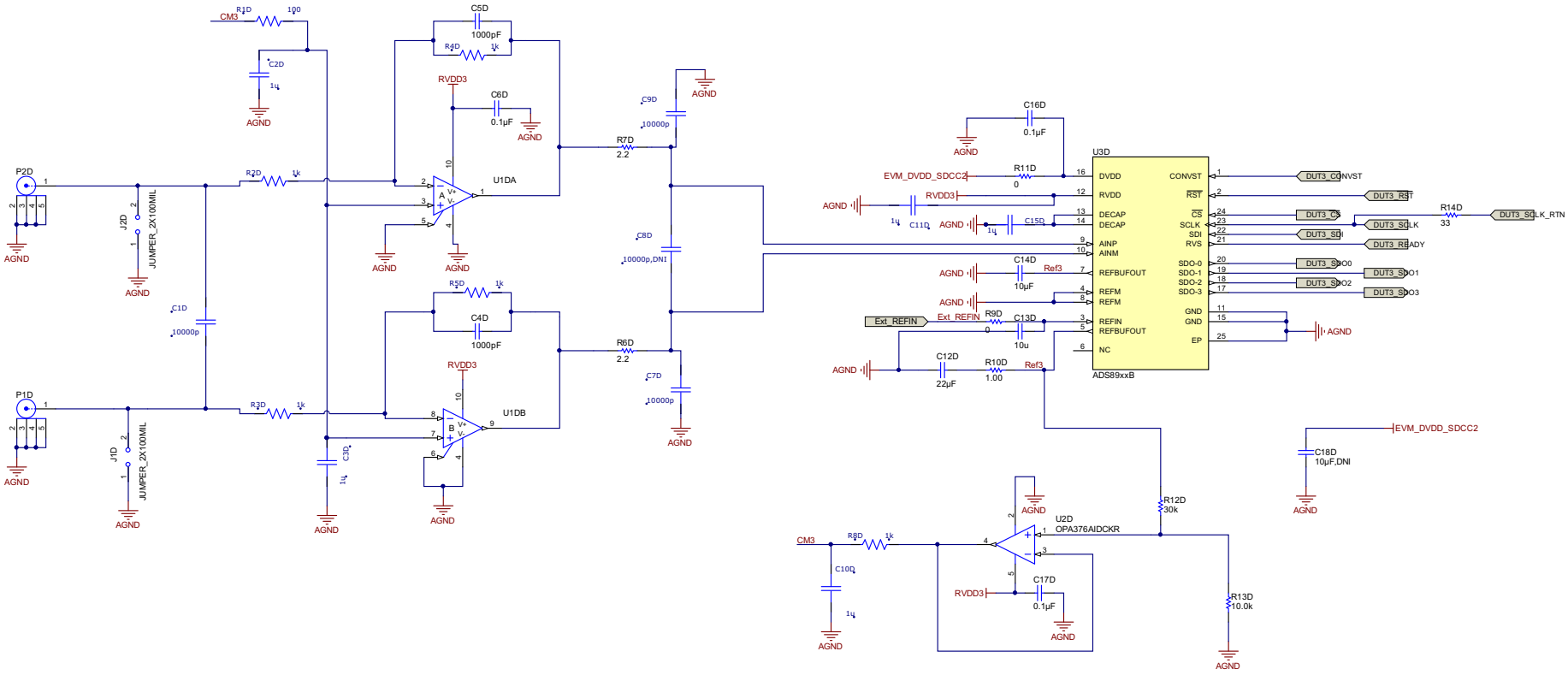

Figure 52. Ch3 Input and Reference Schematic

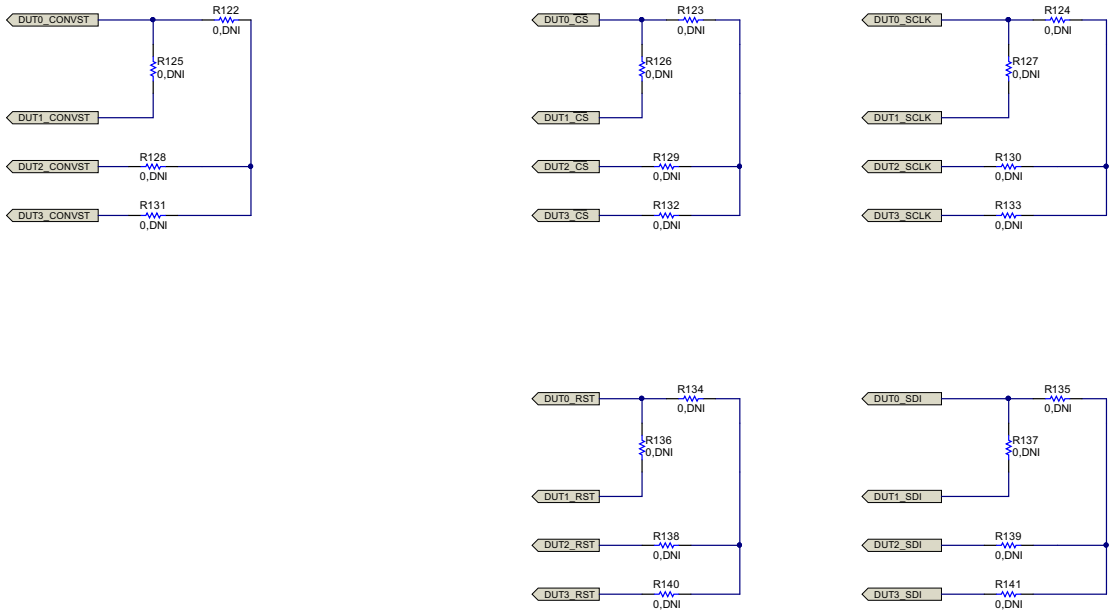

Figure 53. Digital Control Schematic

10.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIPD211.

10.3 PCB Layout Recommendations

The most important considerations to make when designing the PCB layout for this DAQ block are as follows:

- The recommended 1-Ω equivalent series resistance (ESR) and 22-uF ceramic decoupling capacitor on the REFBUFOUT pins must be placed as close to the REFBUFOUT and REFM pins as possible.
- The REFBUFOUT and REFP pins of the ADC must be connected with a local plane to minimize the trace inductances that can adversely affect the reference settling or may even lead to instability.
- The input driver circuit, comprising the OPA2625, must be located as close as possible to the inputs of the ADC to minimize loop area, thus making the layout more robust against electromagnetic interference (EMI) and radio frequency interference (RFI).
- Similarly, the resistors and capacitor of the anti-aliasing filter at the inputs of the ADC must be kept close together and close to the inputs of the ADC to minimize the loop area.
- The traces feeding the differential input voltage from the source up to the differential inputs of the ADC must be kept symmetrical without any sharp turns.

View the complete PCB layout for this design at TIPD211.

10.3.1 Layout Prints

To download the layout prints, see the design files at TIPD211.

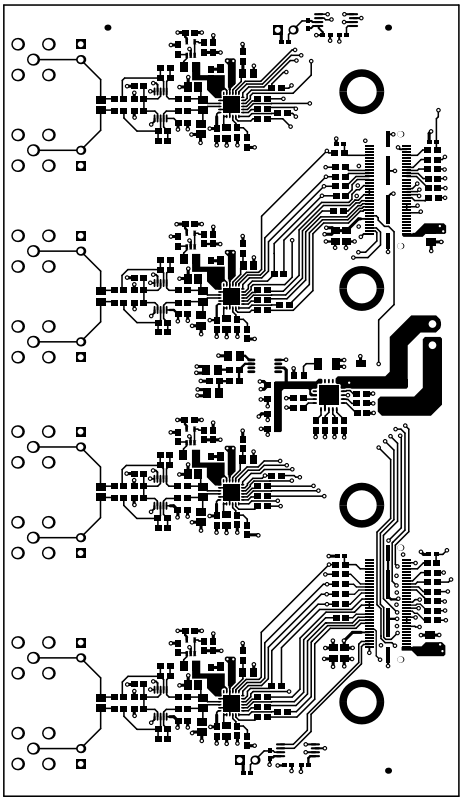

Figure 54. Top Layer

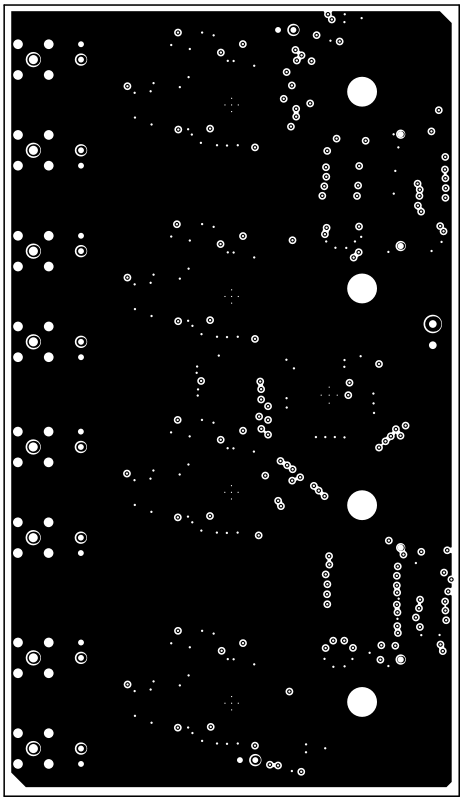

Figure 55. L2 GND

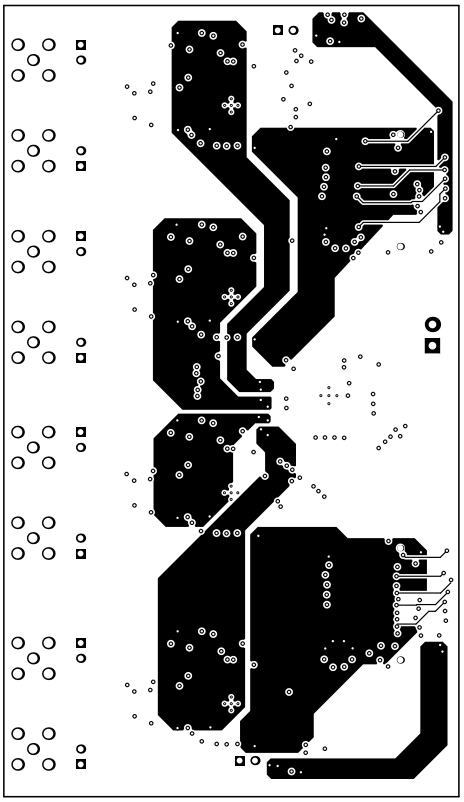

Figure 56. L3 PWR

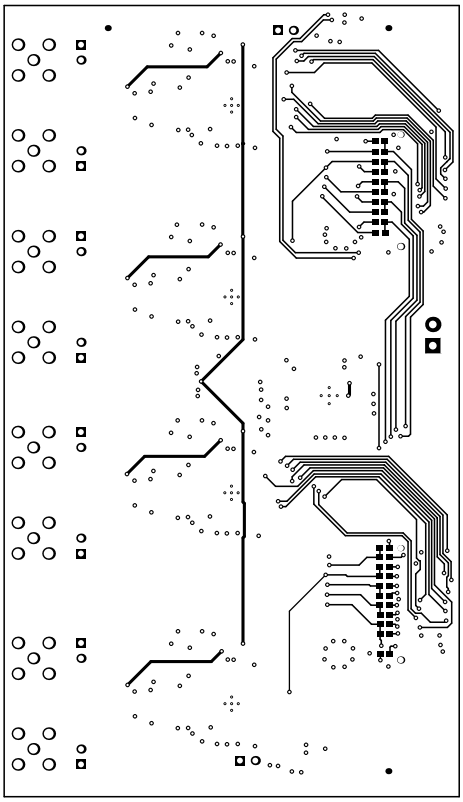

Figure 57. Bottom Layer

11 References

1. Texas Instruments, *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise*, TIPD115 TI Precision Design (SLAU515)
2. Green, Tim; *Operational Amplifier Stability - Parts 1-11*, November 2008: http://www.en-genius.net/site/zones/acquisitionZONE/technical_notes/acqt_050712
3. Texas Instruments, *18-Bit Data Acquisition (DAQ) Block Optimized for 1-µs Full-Scale Step Response*, TIPD112 TI Precision Design (TIDU012)

12 About the Author

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Revision History B

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from A Revision (November 2016) to B Revision **Page**

- Added *Features* subsection 1

Revision History A

Changes from Original (July 2016) to A Revision **Page**

- Changed title from *18-Bit, ,1-MSPS, 4-Ch Small Form Factor Design for Test and Measurement Applications Reference Design* to *20-Bit, 1-MSPS, 4-Ch Small-Form Factor Design for Test and Measurement Applications Reference Design* .. 1
- Changed from ADS8910B device to ADS8900B device 1
- Changed from ADS8910B device to ADS8900B device 1
- Changed plot on landing page to updated figure with different results 1
- Changed *linearity* goal from "18-bit NMC" to "20-bit NMC" 2
- Changed *linearity* goal from "< ±1 LSB INL" to "< ±1.5 ppm INL" 2
- Changed *linearity* measurement from "18-bit NMC" to "20-bit NMC" 2
- Changed *linearity* measurement from "±0.3 LSB INL" to "±0.75 ppm INL" 2
- Changed *Noise performance* goal from "> 100 dB" to "> 102 dB" 2
- Changed *Noise performance* measurement from "101.2 dB" to "102.5 dB" 2
- Changed data plot set and caption from "Linearity Plot 18-bit NMC DNL < ±0.5 LSB" to "Linearity Plot 20-bit NMC DNL, ±0.75 ppm-INL" 2
- Changed caption from "FFT Plot 101.2-dB SNR –123.9-dB THD" to "FFT Plot 102.5-dB SNR –125-dB THD" 2
- Changed from ADS8910B device to ADS8900B device 3
- Changed value from "18-bit low noise" to "20-bit low noise" 6
- Changed value from "18 bits of resolution" to "20 bits of resolution" 6
- Changed Equation 3 to updated equation 7
- Changed value from "18-bit, 1-MSPS SAR ADC" to "20-bit, 1-MSPS SAR ADC"" 10
- Changed Equation 29 to updated equation 15
- Changed value from "18-bit precision performance" to "20-bit precision performance" 22
- Changed from ADS8910B device to ADS8900B device 22
- Changed from ADS8910B device to ADS8900B device 22
- Changed from ADS8910B device to ADS8900B device 22
- Changed *Resolution* design requirement from "18 bits" to "20 bits" 22
- Changed Resolution ADS8900B specification from "18 bits" to "20 bits" 22
- Changed *linearity* design requirement from "18-bit NMC" to "20-bit NMC" 22
- Changed *linearity* design requirement from "< ±1 LSB INL" to "< ±1.5-ppm INL" 22
- Changed *linearity* ADS8900B specification from "18-bit NMC" to "20-bit NMC" 22
- Changed *linearity* ADS8900B specification from "±0.5 LSB INL (typ)" to "±1-ppm INL (typ)" 22
- Changed *Noise performance* design requirement from "> 100 db SNR" to "> 102 db SNR" 22
- Changed from ADS8910B device to ADS8900B device 23
- Changed caption from "System Block Diagram Using 4x ADS8910B" to "System Block Diagram Using 4x ADS8900B" 23
- Changed from ADS8910B device to ADS8900B device 23
- Changed from ADS8910B device to ADS8900B device 23
- Changed Equation 32 to updated equation 24
- Changed Equation 33 to updated equation 24
- Changed from ADS8910B device to ADS8900B device 25
- Changed text from "The output impedance of the OPA2625 device depends on the frequency of operation. The output impedance for the OPA2625 device at a 2-kHz frequency is 9 Ω, therefore:" to "To meet both criteria, choose amplifier with output impedance less than the calculated value in Equation 38 at 2-kHz:" 25
- Changed Equation 38 to updated equation 25

- Changed from ADS8910B device to ADS8900B device 25
- Changed image to updated Figure 27 25
- Changed Equation 42 to updated equation 26
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