## *TI Designs*
# *Power Over Ethernet® (PoE) for Connected IoT*

TEXAS INSTRUMENTS

## Design Overview

This design integrates TI PoE solution with TM4C129x high performance microcontroller to enable customers to develop applications for IoT in a small form factor board. The ability to derive power over existing network cabling combined with intelligence to gather, process and exchange data with the cloud increases the value of the end application.

## Design Resources

| | |
|---|---|
| TIDM-TM4C129POE | Design Folder |
| TM4C129ENCPDT | Product Folder |
| TPS23753A | Product Folder |
| TPD2E2U06 | Product Folder |
| TLV431A | Product Folder |
| | Product Folder |

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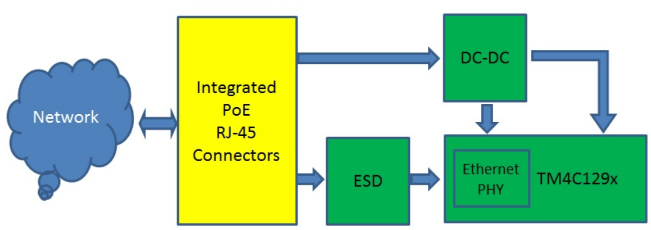
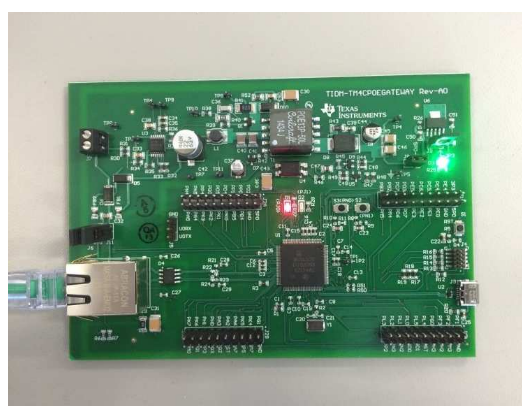
## Design Features

- Small Form Factor Board Measuring 4.95” × 3.45” With TM4C129ENCPDT Microcontroller Featuring Integrated Ethernet® PHY and MAC.
- Integrated RJ45, Transformer and Diode Bridge for PoE Power Stage for Lower BOM Cost.
- 7 W Isolated Output From the Fly-Back Converter, With Provision for Both 5 V and 3.3 V Output Power Rails.
- Optional Power Header to Supply External DC Power From an UPS in Case of a Network Power Failure.
- Dual BoosterPack™ Headers to Prototype End Applications With a Wide Range of BoosterPacks™ From TI and Third-Party.
- TivaWare Examples for Crypto Connected LaunchPad™ May be Run With Minimum Modifications for Evaluation.

## Featured Applications

- Factory Automation and Control
- IoT Cloud Gateway
- Camera Surveillance
- Access Control
- Information Kiosks



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# 1 System Description

The TM4C129x family of microcontrollers from TI that feature an integrated Ethernet® PHY and MAC with cryptographic modules and a large number of serial interfaces for control and sensor data acquisition. When integrated with PoE solutions from TI, the TM4C129x adds a layer of intelligence at the remote node. The TM4C129x allows customers to leverage their existing network to not only communicate and control devices securely with the PoE solution, but also deliver power, reducing the system cost in IoT space, and adding value to their products. The design files include Schematics, Bill of Materials (BOM), Layer Plots, Altium Files, and Gerber Files.

## *1.1 TM4C129ENCDT*

The TM4C129ENCPDT is a 120 MHz high-performance microcontroller with 1 MB on-chip Flash and 256 KB on-chip SRAM. The TM4C129ENCPDT microcontroller also features an integrated Ethernet MAC + PHY for connected applications and cryptographic modules of AES, DES and SHA for encryption, decryption and authentication. The device has high bandwidth interfaces such as Memory Controller and a High Speed USB2.0 digital interface. With integration of a number of low to mid speed serial, up to 4MSPS 12-bit ADC and motion control peripherals it makes for a unique solution for a variety of applications ranging from industrial communication equipment's to Smart Energy and Smart Grid applications.

Figure 1 shows the TM4C129ENCPDT microcontroller high-level block diagram.

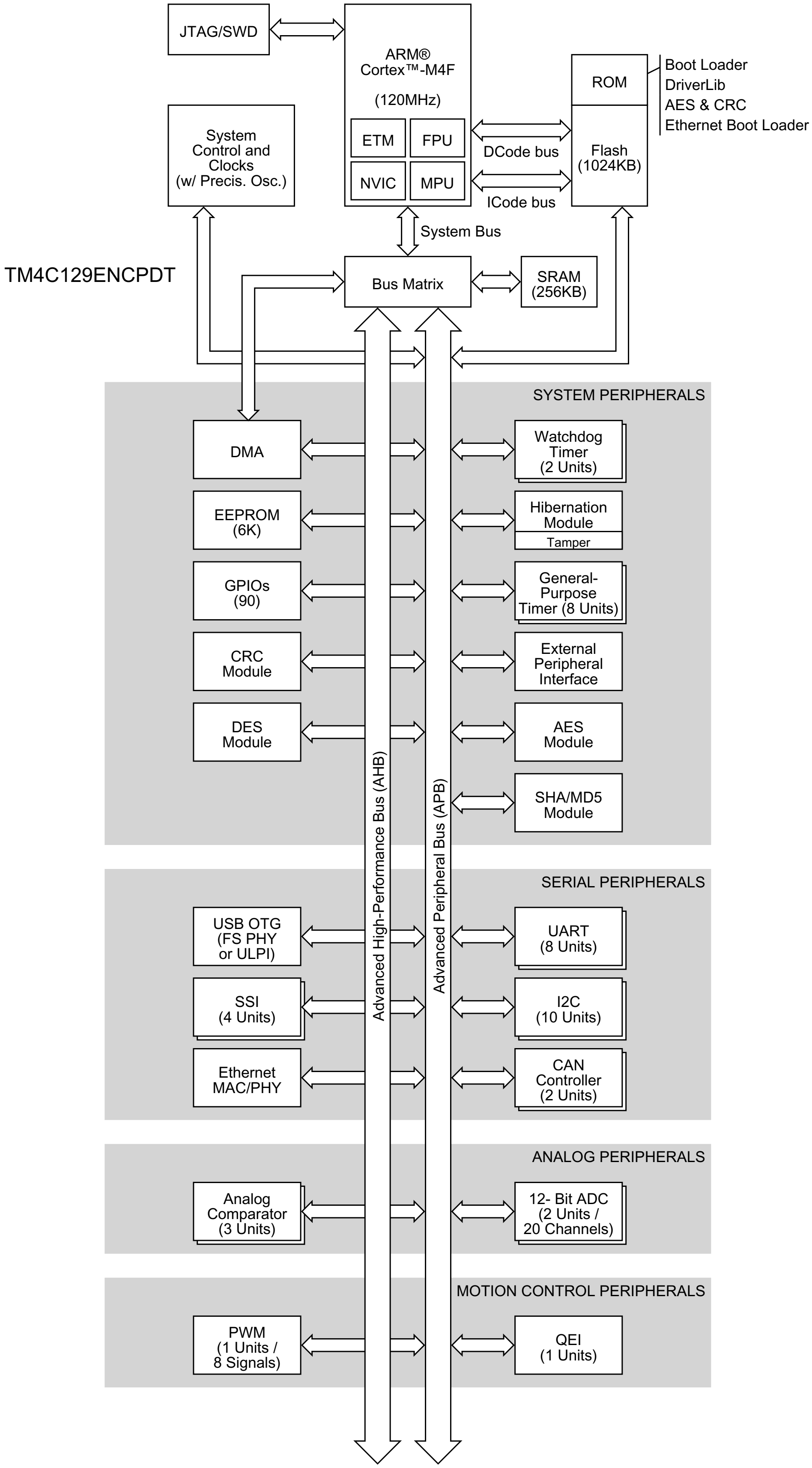


**Figure 1. TM4C129ENCPDT Microcontroller High-Level Block Diagram**

### 1.2 TPS23753A

The TPS23753A is a combined Power over Ethernet (PoE) Powered Device (PD) interface and current-mode DC-DC controller optimized specifically for isolated converter designs. The PoE implementation supports the IEEE 802.3at standard as a 13-W, type 1 PD. The requirements for an IEEE 802.3at type 1 device are a superset of IEEE 802.3-2008 (originally IEEE 802.3af). The DC-DC controller features a bootstrap start-up mechanism with an internal current source, which provides the advantages of cycling overload fault protection without the constant power loss of a pull-up resistor.

## 2 Block Diagram

Figure 2 shows the power over Ethernet (PoE) for connected IoT block diagram.

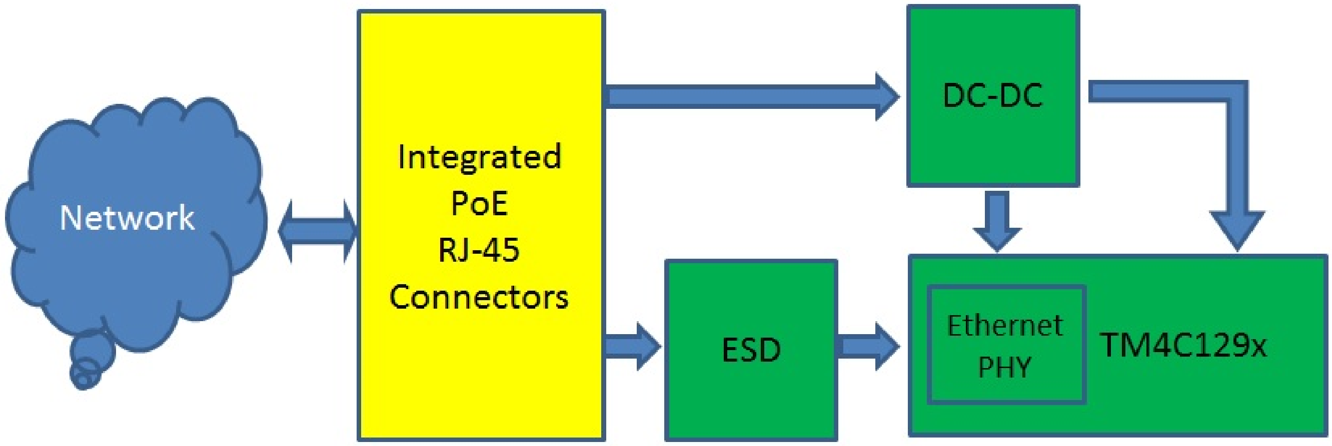


**Figure 2. Power Over Ethernet (PoE) for Connected IoT Block Diagram**

# 3 Getting Started Hardware

This design is a plug and play system and little user intervention is required for either supplying or managing any control I/O's for power to the device.

## 3.1 Test Points, Connectors, Jumpers, Switches, and LEDs

This section gives details about the connectors, test points, and the jumpers that are available on the design for debug, probe, and flexibility of evaluation.

Table 1 lists the test points.

**Table 1. Test Points**

| DESIGNATOR | DESCRIPTION |
|---|---|
| TP1 | TM4C129ENCPDT 1.2 V Core Voltage Test Point |
| TP2 | DC/DC Converter Return |
| TP3 | PoE Input, Low Side |
| TP4 | DC/DC Converter Output Voltage |
| TP5 | Digital Ground |
| TP6 | DC/DC Converter Bias Supply |
| TP7 | DC/DC Converter Return |
| TP8 | Drain Terminal of the Primary-Side Switching MOSFET |
| TP9 | Bias Voltage Regulator |
| TP10 | Gate Driver for the Primary-Side Switching MOSFET |
| TP11 | Control Loop Input to the Pulse Width Modulator |

Table 2 lists the connectors and jumpers.

**Table 2. Connectors and Jumpers**

| DESIGNATOR | DESCRIPTION |
|---|---|
| J1A | BoosterPack™ Header |
| J1B | BoosterPack Header |
| J2A | BoosterPack Header |
| J2B | BoosterPack Header |
| J3 | USB Header |
| J4 | JTAG Debug Header |
| J5 | UART Header for Debug COM Port |
| J6 | Integrated RJ45 Connector, Transformer and Rectifier Diode |
| J7 | External Adapter Input Connector |
| J8 | 5 V Output Jumper |
| J9 | 3.3 volt output jumper |
| J10 | PoE Input Low Side From the RJ45 Jack |
| J11 | PoE Input High Side From the RJ45 Jack |

## 3.2 Power-Up

There are four potential sources of power in this design:

- The primary power is through the Ethernet RJ45 (J6). The user must ensure that a Switch or Hub being used is a PoE PSE equipment.
- The user may power the design by using the external adapter input connector (J7) through a 12V DC power supply.
- The user may power the design from a 5-V DC power supply, by removing the header (J8) and applying 5-V input to Pin-1 of J8.

**NOTE:** GND from the external power supply must be connected to TP5.

- The user may power the design from a 3.3-V DC power supply, by removing the header (J9) and applying 3.3V input to Pin-1 of J9.

**NOTE:** GND from the external power supply must be connected to TP5. In this configuration, the 5 V is not available on the BoosterPack headers.

## 3.3 Connecting a Debugger

To be able to download an application to the TM4C129ENCPDT microcontroller, the header J4 is provided. This header is a 10-pin 50 mil spacing connector and is compliant to the ARM™ Cortex 10-pin JTAG standard. In case the debugger does not have an ARM Cortex 10-pin header, a small adapter board may be required, and is easily available with most manufacturers of debug pods.

# 4 Getting Started Firmware

There is no specific software required for the design. The user may import examples from TivaWare for EK-TM4C129EXL Crypto Connected Launchpad and run the same as is for the design. However, there are some changes that are required to make the examples work on the design as the BoosterPack headers are slightly different from the EK-TM4C129EXL Crypto Connected LaunchPad.

## 4.1 BoosterPack Head Compatibility

Table 3 summarizes the difference in pinout on the BoosterPack headers.

**Table 3. BoosterPack Header Compatibility, Table A**

| EK-TM4C129EXL HEADER X8 | PORT PIN NAME | TIDM-TM4C129POE HEADER J1A | PORT PIN NAME |
|---|---|---|---|
| 1 | 3.3 V | 1 | 3.3 V |
| 2 | 5 V | 2 | 5 V |
| 3 | PE4 | 3 | PE4 |
| 4 | GND | 4 | GND |
| 5 | PC4 | 5 | PC4 |
| 6 | PE0 | 6 | PE0 |
| 7 | PC5 | 7 | PC5 |
| 8 | PE1 | 8 | PE1 |
| 9 | PC6 | 9 | PC6 |
| 10 | PE2 | 10 | PE2 |
| 11 | PE5 | 11 | PE5 |
| 12 | PE3 | 12 | PE3 |
| 13 | PD3 | 13 | PD3 |
| 14 | PD7 | 14 | PD7 |
| 15 | PA7 | 15 | PC7 |
| 16 | PA6 | 16 | PD6 |
| 17 | PB2 | 17 | PB2 |
| 18 | PM4 | 18 | PM4 |
| 19 | PB3 | 19 | PB3 |
| 20 | PM5 | 20 | PM5 |

Table 4 lists the BoosterPack header compatibility, table B.

**Table 4. BoosterPack Header Compatibility, Table B**

| EK-TM4C129EXL HEADER X9 | PORT PIN NAME | TIDM-TM4C129POE HEADER J1B | PORT PIN NAME |
|---|---|---|---|
| 1 | PF1 | 1 | PF1 |
| 2 | GND | 2 | GND |
| 3 | PF2 | 3 | PF2 |
| 4 | PM3 | 4 | PM3 |
| 5 | PF3 | 5 | PF3 |
| 6 | PH2 | 6 | PH2 |
| 7 | PG0 | 7 | PG0 |
| 8 | PH3 | 8 | PH3 |
| 9 | PL4 | 9 | PL4 |
| 10 | RST_N | 10 | RST_N |
| 11 | PL5 | 11 | PL5 |
| 12 | PD1 | 12 | PD1 |
| 13 | PL0 | 13 | PL0 |
| 14 | PD0 | 14 | PDO |
| 15 | PF1 | 15 | PF1 |
| 16 | PN2 | 16 | PN2 |
| 17 | PL2 | 17 | PL2 |
| 18 | PN3 | 18 | PN3 |
| 19 | Pl3 | 19 | PL3 |
| 20 | PP2 | 20 | PP2 |

Table 5 lists the BoosterPack header compatibility, Table C.

**Table 5. BoosterPack Header Compatibility, Table C**

| EK-TM4C129EXL HEADER X6 | PORT PIN NAME | TIDM-TM4C129POE HEADER J2A | PORT PIN NAME |
|---|---|---|---|
| 1 | 3.3 V | 1 | 3.3 V |
| 2 | 5 V | 2 | 5 V |
| 3 | PD2 | 3 | PD2 |
| 4 | GND | 4 | GND |
| 5 | PP0 | 5 | PP0 |
| 6 | PB4 | 6 | PB4 |
| 7 | PP1 | 7 | PP1 |
| 8 | PB5 | 8 | PB5 |
| 9 | PD4 | 9 | PD4 |
| 10 | PK0 | 10 | PK0 |
| 11 | PD5 | 11 | PD5 |
| 12 | PK1 | 12 | PK1 |
| 13 | PQ0 | 13 | PQ0 |
| 14 | PK2 | 14 | PK2 |
| 15 | PP4 | 15 | PP4 |
| 16 | PK3 | 16 | PK3 |
| 17 | PN5 | 17 | PN5 |
| 18 | PA4 | 18 | PA4 |
| 19 | PN4 | 19 | PN4 |
| 20 | PA5 | 20 | PA5 |

Table 6 lists the BoosterPack header compatibility, Table D.

**Table 6. BoosterPack Header Compatibility, Table D**

| EK-TM4C129EXL HEADER X7 | PORT PIN NAME | TIDM-TM4C129POE HEADER J2B | PORT PIN NAME |
|---|---|---|---|
| 1 | PG1 | 1 | PG1 |
| 2 | GND | 2 | GND |
| 3 | PK4 | 3 | PK4 |
| 4 | PM7 | 4 | PM7 |
| 5 | PK5 | 5 | PK5 |
| 6 | PP5 | 6 | PP5 |
| 7 | PM0 | 7 | PA6 |
| 8 | PA7 | 8 | PA7 |
| 9 | PM1 | 9 | PA2 |
| 10 | RST_N | 10 | RST_N |
| 11 | PM2 | 11 | PA3 |
| 12 | PQ2 | 12 | PQ2 |
| 13 | PH0 | 13 | PH0 |
| 14 | PQ3 | 14 | PQ3 |
| 15 | PH1 | 15 | PH1 |
| 16 | PP3 | 16 | PP3 |
| 17 | PK6 | 17 | PK6 |
| 18 | PQ1 | 18 | PQ1 |
| 19 | PK7 | 19 | PK7 |
| 20 | PM6 | 20 | PM0 |

## 5 Test Data

The following section gives details of the electrical tests that have been done on the design for PoE power front end.

### 5.1 Startup

The 5V and 3.3V output voltage startup waveforms are shown in Figure 3 with no external load and a 48V- input at J6.

CH1 (5Vout): 1V/div; CH2 (3.3Vout): 1V/div; 1ms/div

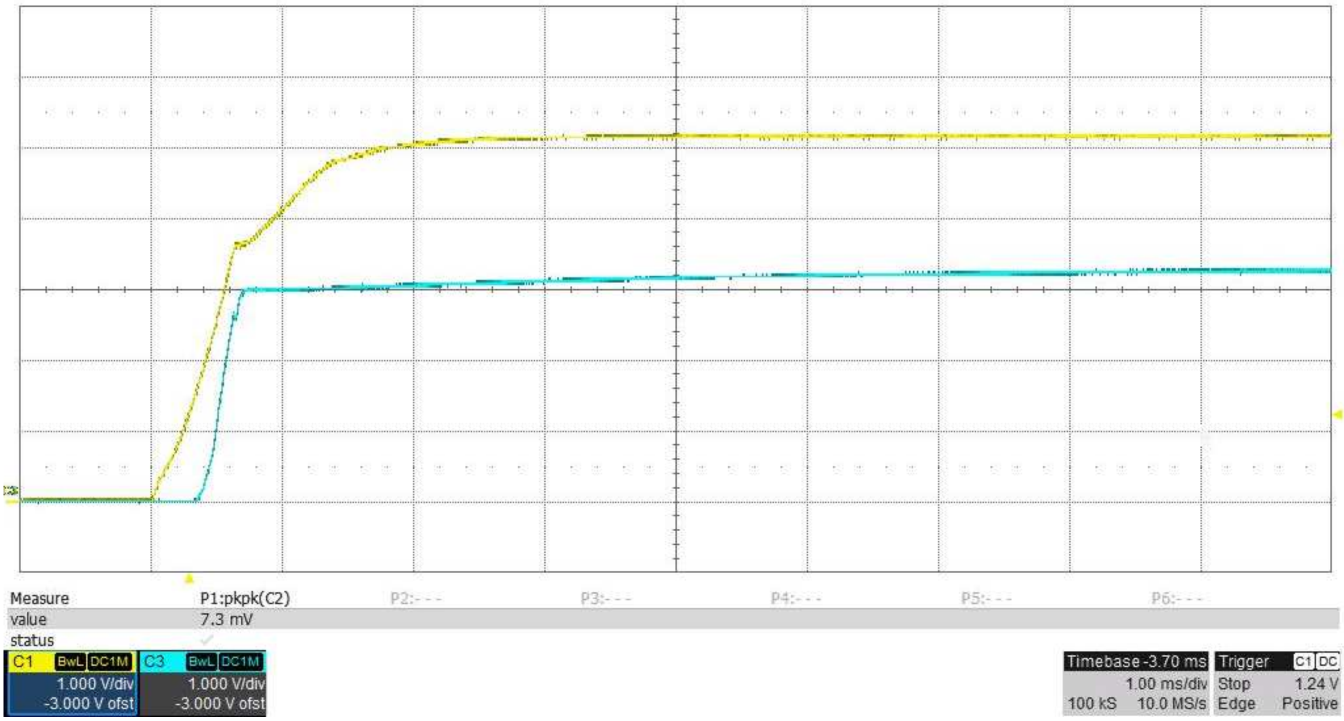


**Figure 3. Start-Up Under No Load**

The 5 V and 3.3-V output voltage startup waveforms are shown in Figure 4 with a 160-mA external load and 48-V input at J6.

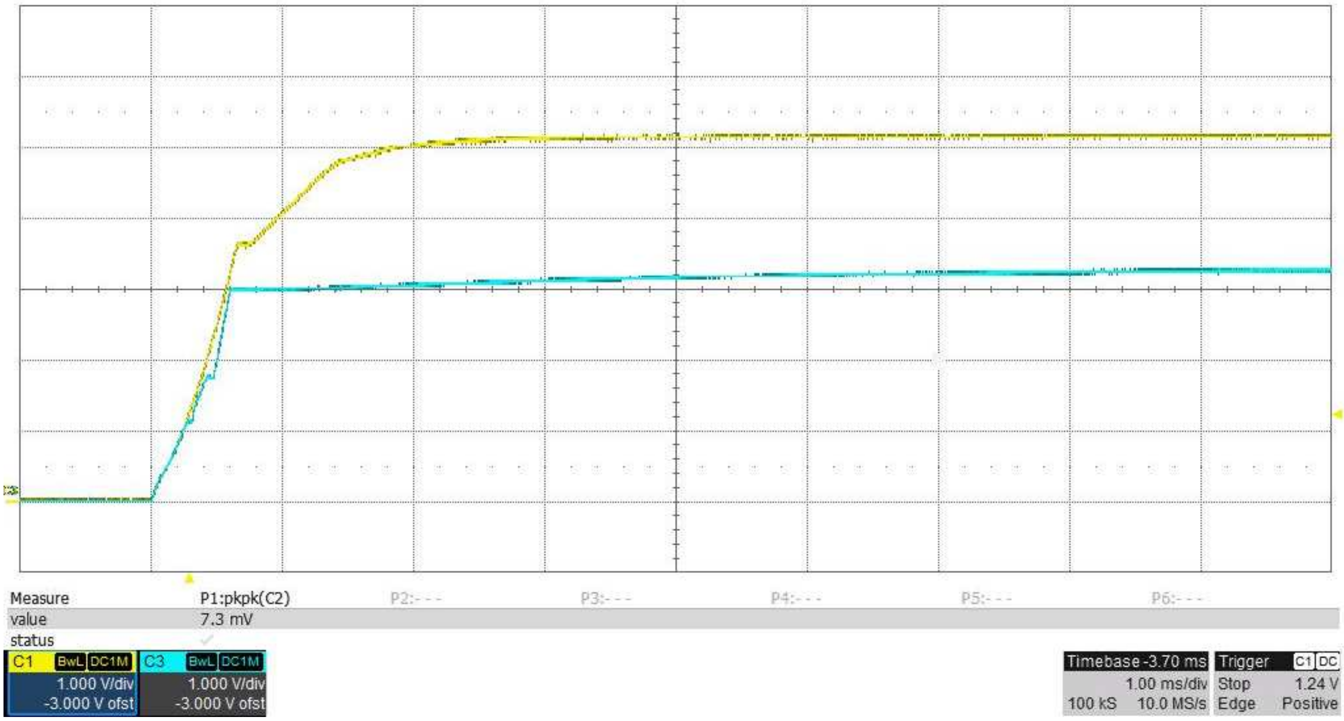


**Figure 4. Start-Up Under Load Conditions**

## 5.2 Efficiency

The converter efficiency is shown in Figure 5 with a 48-V input at J6. Jumper J8 has been removed and all loading is on the 5-V output.

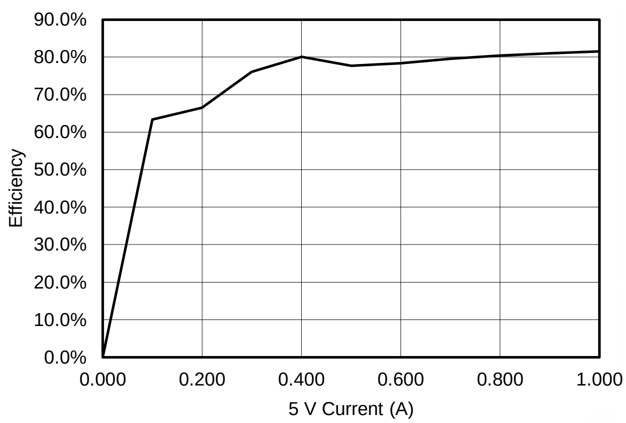


**Figure 5. Efficiency Chart**

## 5.3 Output Ripple Voltage

The 5-V output ripple voltage is shown in Figure 6, measured across C46. The 5-V output is loaded by the 3.3-V LDO (approximately 90 mA plus an external 160 mA load on the 5 V. (20 mV ÷ DIV, 2 us ÷ DIV).

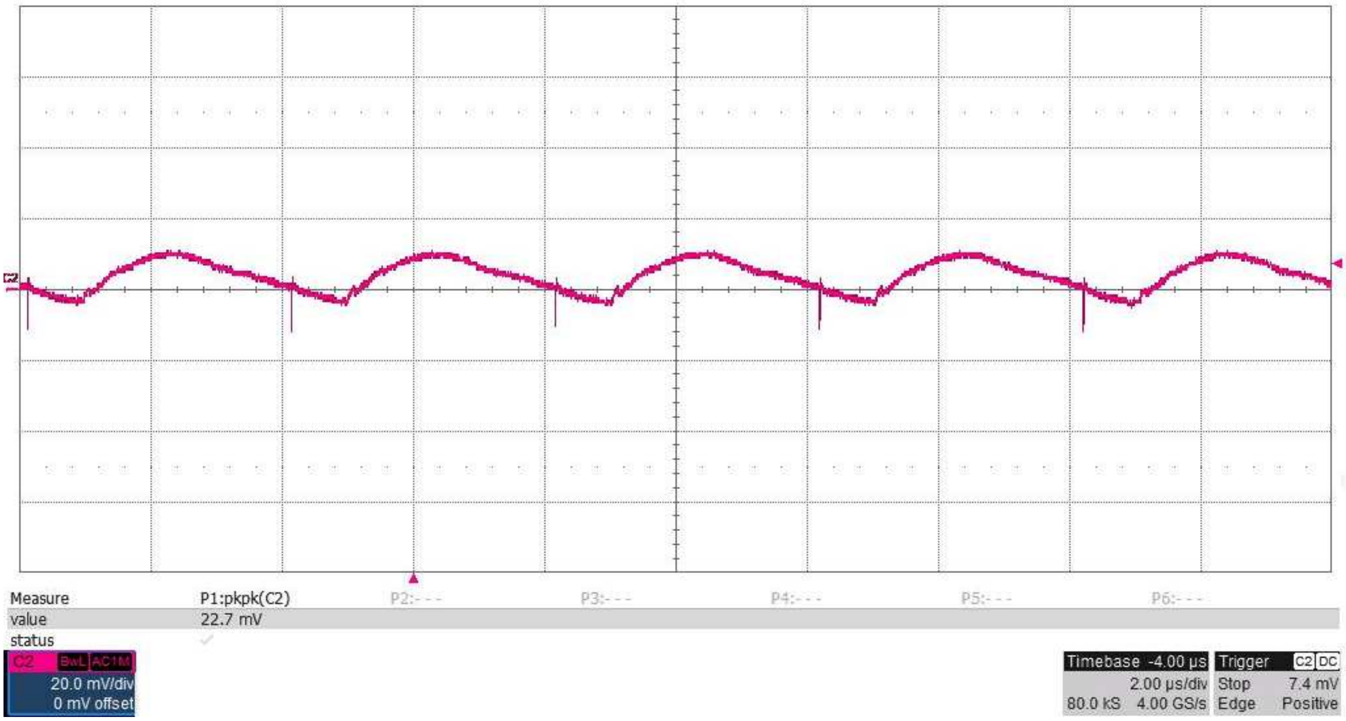


**Figure 6. Ripple Voltage on a 5-V Load**

The 3.3-V output ripple voltage is shown in Figure 7, measured across C52. There is a load on the 3.3 V that repeats approximately every 60 ms, resulting in the noise shown in Figure 7. (20 mV ÷ DIV, 100 uS ÷ DIV)

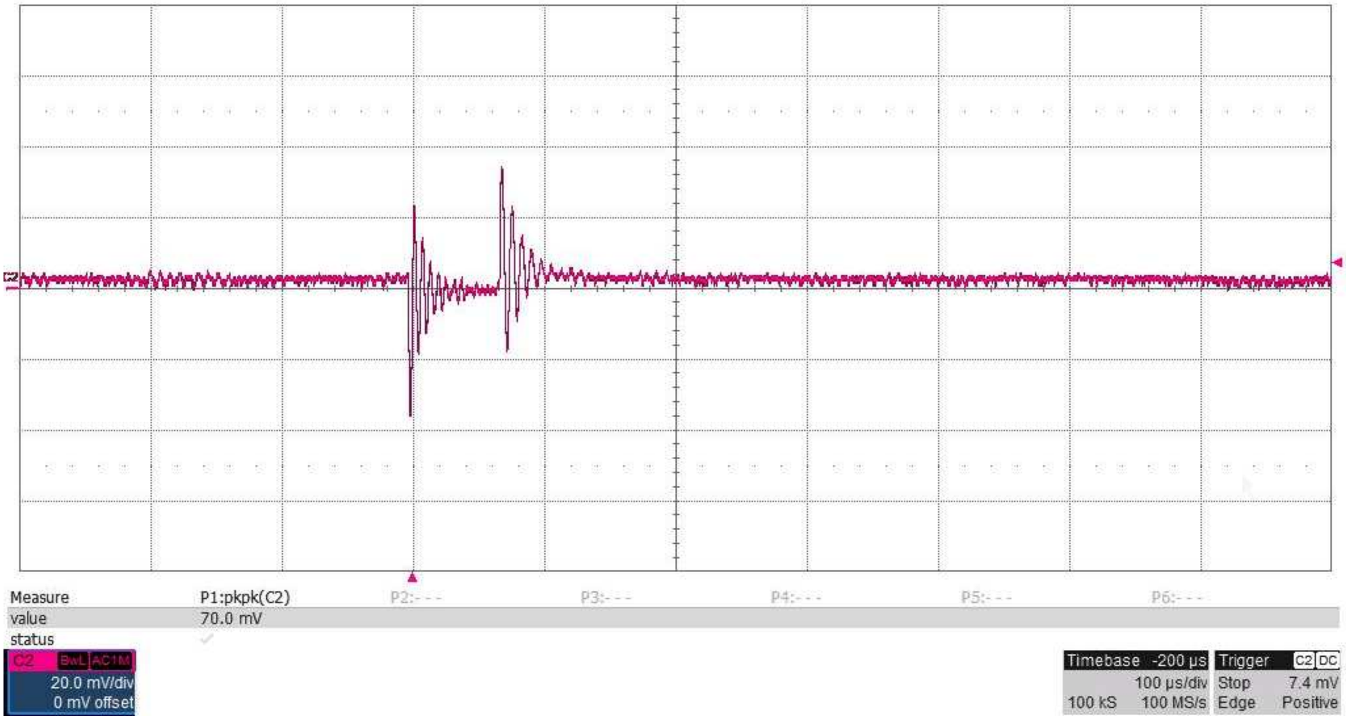


**Figure 7. Ripple Voltage on a 3.3-V Load**

## *5.4 Load Transients*

Figure 8 shows the 5-V output voltage response (AC-coupled) to a load current step from 90 mA to 250 mA. The 90 mA load is the LDO with an external 160 mA load step applied. (50mV ÷ DIV, 100 mA ÷ DIV, 1 msec ÷ DIV, 25 mA ÷ usec slew rate).

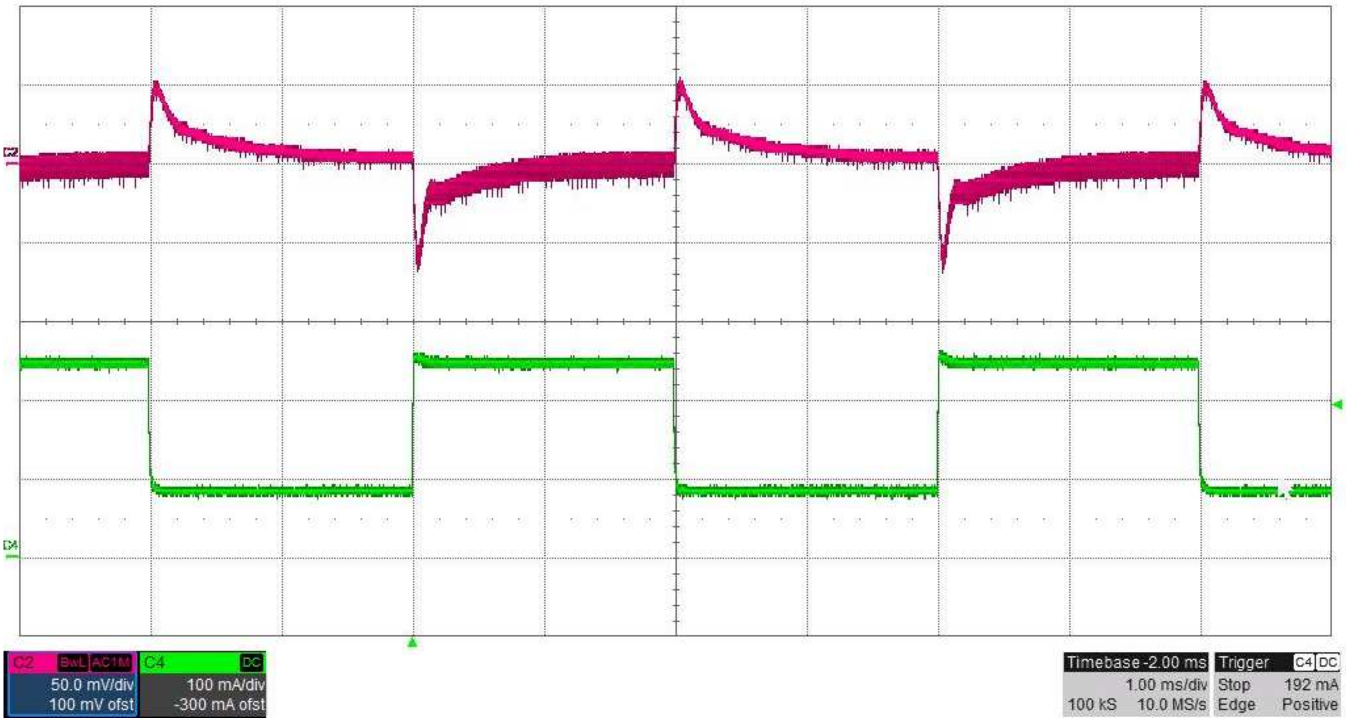


**Figure 8. Load Transients on 5 V Output**

### 5.5 Switching Waveforms

Figure 9 shows the drain voltage of Q1 with respect to GNDX. The input voltage is 48-V and the 5-V output is loaded with the 3.3 V-LDO (90 mA) plus and external 160-mA load. (20V ÷ div, 2 usec ÷ div).

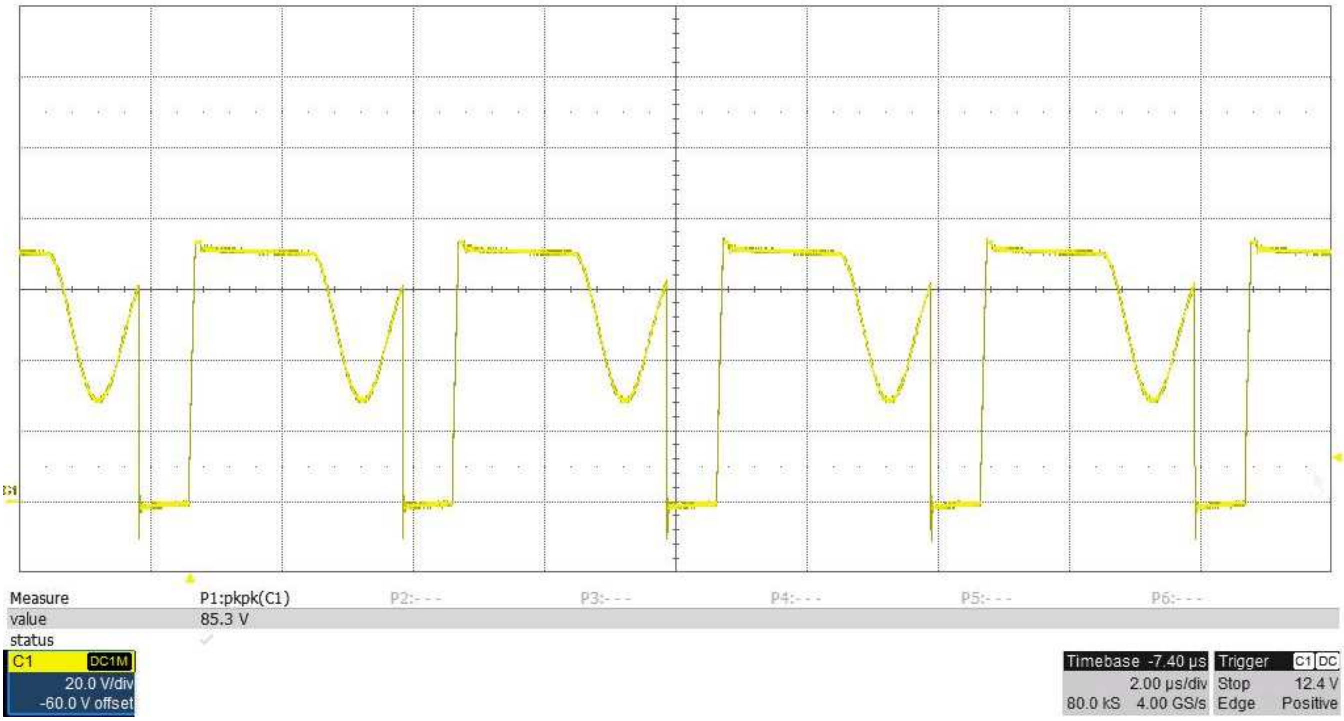


**Figure 9. Switching Waveforms for Q1**

Figure 10 shows the anode voltage of D8 with respect to GND. The input voltage is 48 V and the 5-V output is loaded with the 3.3-V LDO (90 mA) plus and external 160-mA load. (10 V ÷ div, 2 usec ÷ div).

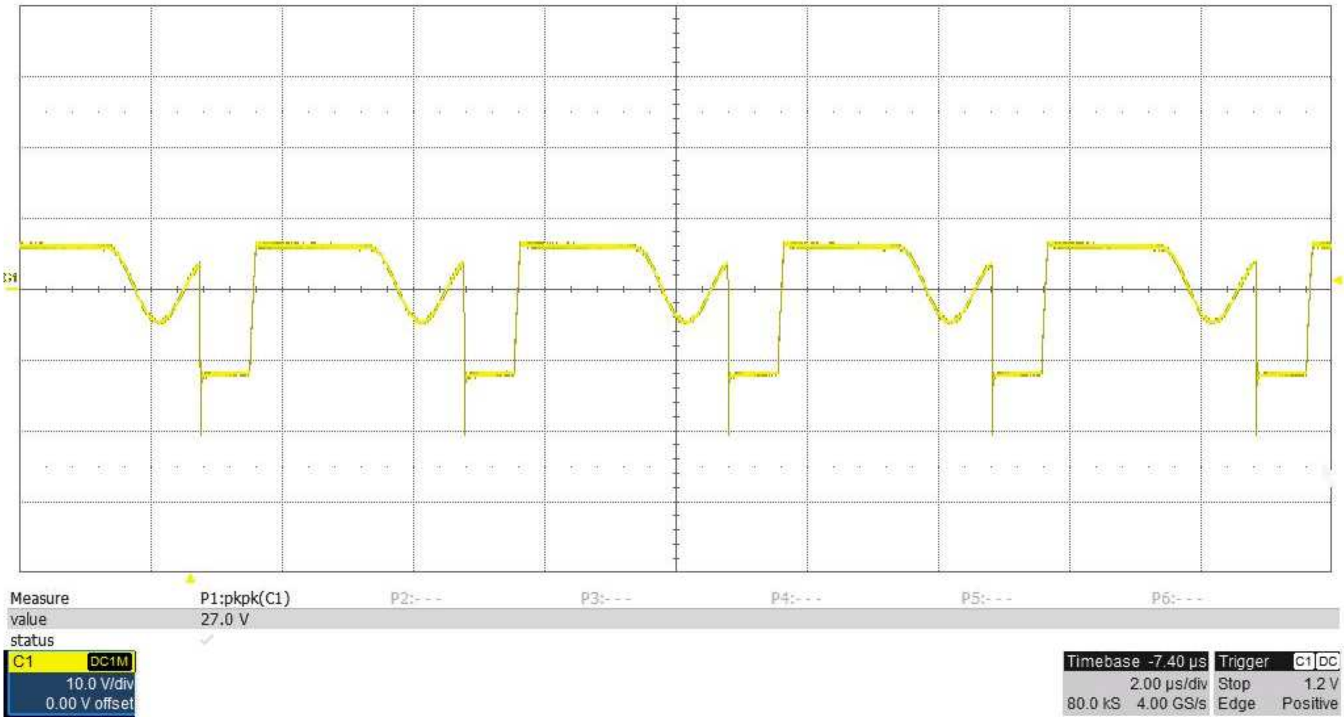


**Figure 10. Switching Waveform for D8**

### 5.6 Control Loop Gain Stability

Figure 11 shows the converter's loop gain and phase margin. The 5V is loaded with the 3.3-V LDO (90 mA) plus a 160-mA external load. The input is 48 V at J6.

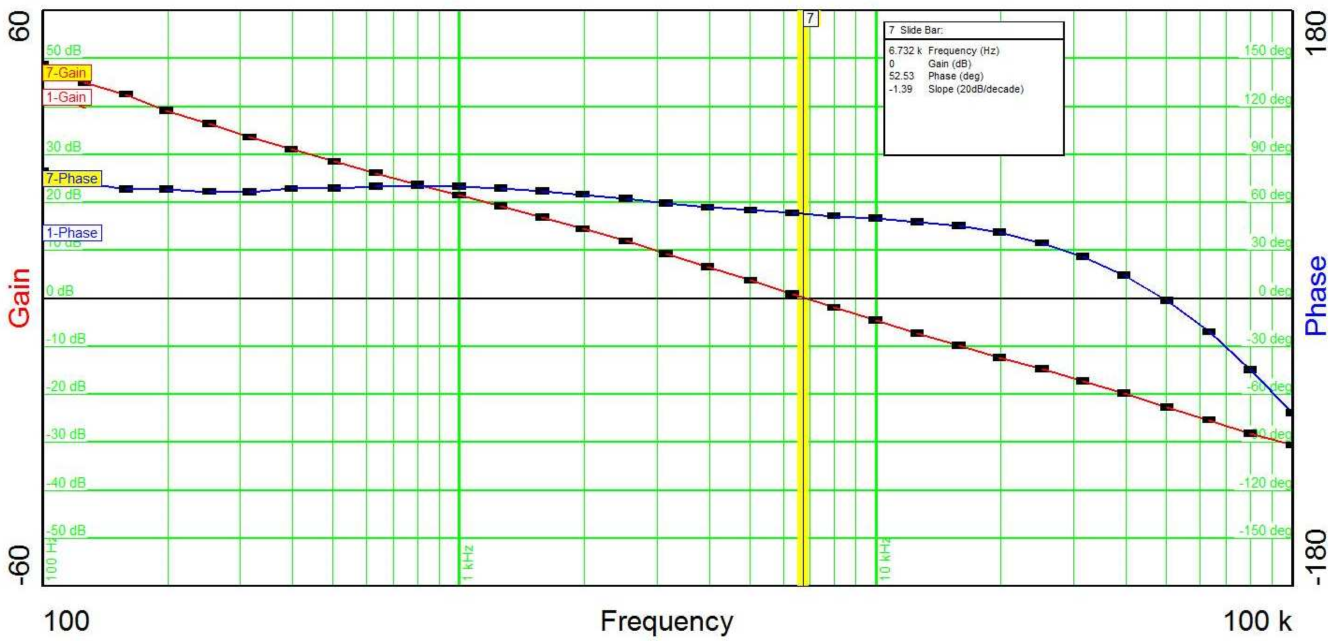


**Figure 11. Control Loop Gain Stability**

# 6 Design Files

## 6.1 Schematics

To download the schematics, see the design files at TIDM-TM4C129POE..

Figure 12 shows the schematic for the microcontroller section.

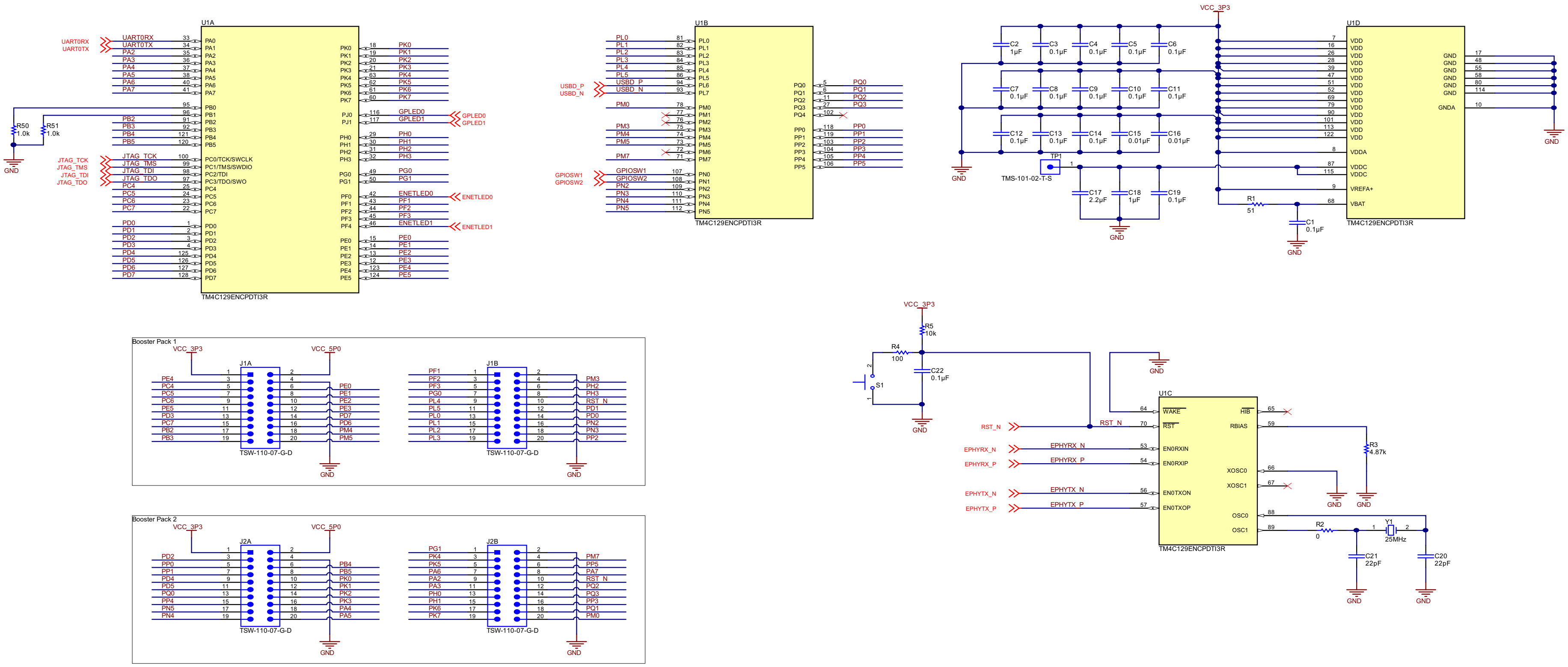



**Figure 12. Schematic for the Microcontroller Section**

[Figure 13](#) shows the schematic for the connector section.

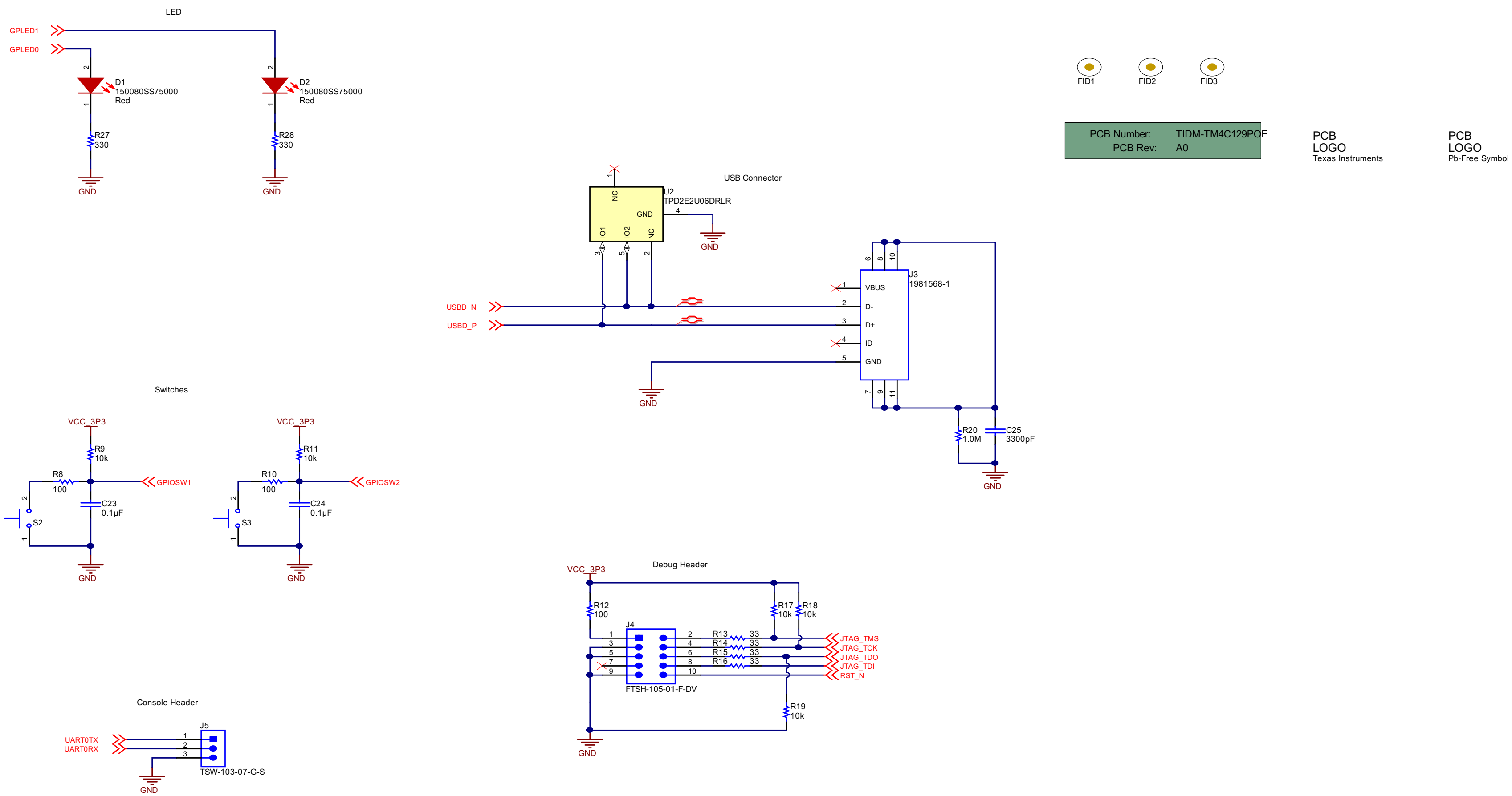




**Figure 13. Schematic for the Connector Section**

Figure 14 shows the schematic for the Ethernet section.

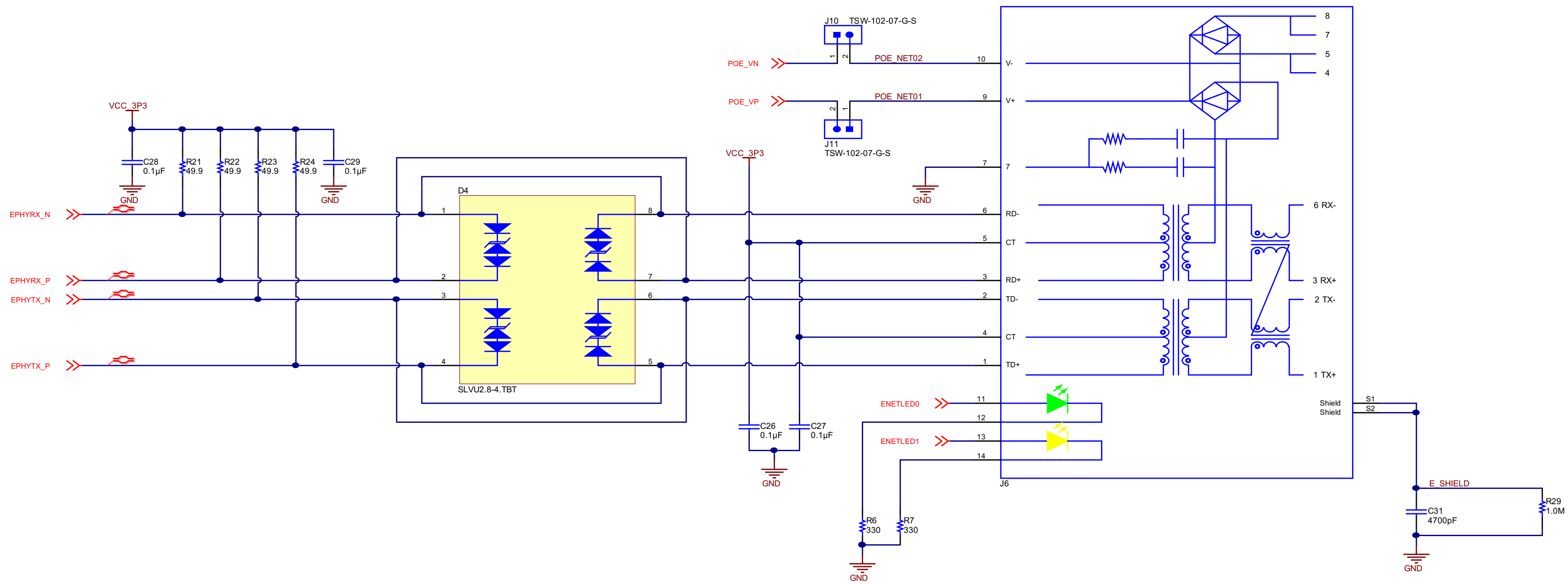




**Figure 14. Schematic for the Ethernet Section**

Figure 15 shows the schematic for the power stage section.

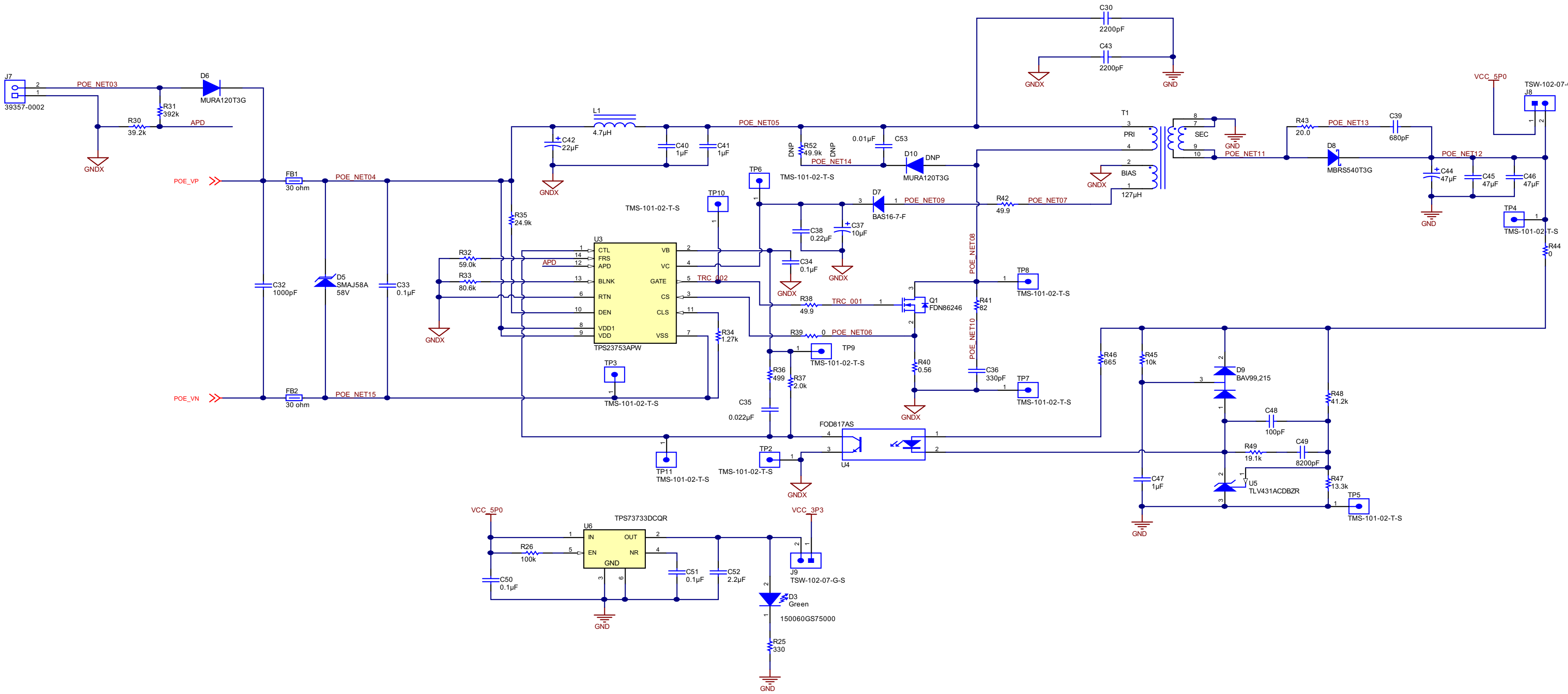



**Figure 15. Schematic for the Power Stage Section**

## 6.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDM-TM4C129POE..

### 6.3 PCB Layout Recommendations

An important consideration when doing the layout is the trace width for Ethernet and USB signals. The Ethernet and USB interfaces have critical differential impedance requirements. Both Ethernet signal pairs must be routed as a 100 Ω ± 10% differential pair on the top layer of the PCB with a ground plane as a reference. The USB signal pair must be routed as a 90 Ω ±10% differential pair on the top layer of the PCB with a ground plane as a reference.

The most optimal solution is if the PCB fab house may adjust the stack up and provide for controlled dielectric. The designer must use the PCB tools to set the spacing and width of the traces to get close to the target characteristic impedance. The PCB fab house may then adjust the trace space and width to their specific materials and process.

During the PCB layout, if the PCB fab house has a predefined layer stack up for low cost process, the user must ascertain the layer stack up information. Then use this information in PCB tools to get the optimum trace width. The design files have used a low cost variant with the following PCB stack up for four layer PCB's.

Figure 16 shows the PCB layer stack up for TIDM-TM4C129POE.

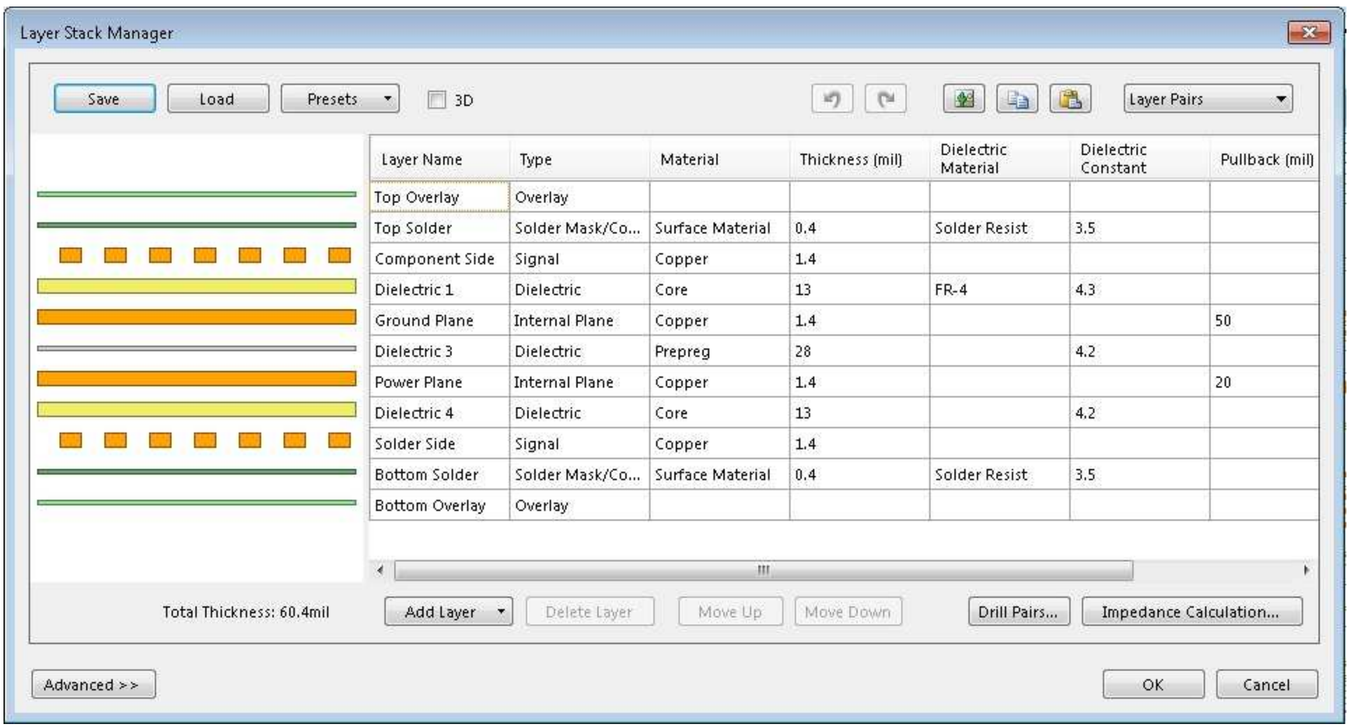


**Figure 16. PCB Layer Stack Up for TIDM-TM4C129POE**

When the data shown in Figure 16 is entered into the PCB tool, the trace width and space for Ethernet and USB signals are computed are listed in Table 7. The most important parameter is the ZDIFF which must be within ±10% tolerance.

**Table 7. Differential Signals Trace Information**

| TRACE WIDTH (mil) | TRACE THICKNESS (mil) | TRACE HEIGHT (mil) | TRACE SPACING (mil) | $E_R$ | $Z_{DIFF}$ | $Z_O$ |
|---|---|---|---|---|---|---|
| 10 | 0.4 | 15.8 | 5 | 4.2 | 109.476 | 84.766 |
| 12.8 | 0.4 | 15.8 | 5 | 4.2 | 99.336 | 76.915 |

### *6.4 Altium Project*

To download the Altium project files, see the design files at TIDM-TM4C129POE.

### *6.5 Layout Guidelines*

To download the layout guidelines, see the design files at TIDM-TM4C129POE.

#### 6.5.1 Layout Prints

To download the layout prints for each board, see the design files at TIDM-TM4C129POE.

### *6.6 Gerber Files*

To download the Gerber files, see the design files at TIDM-TM4C129POE.

### *6.7 Assembly Drawings*

To download the assembly drawings, see the design files at TIDM-TM4C129POE.

## 7 Software Files

To download the software files, see the design files at TIDM-TM4C129POE.

## 8 References

1. *System Design Guidelines for the TM4C129x Family of Tiva™ C Series Microcontrollers* (SPMA056).
2. Saturn PCB Design Toolkit.

## 9 About the Author

**AMIT ASHARA** is an Application Engineer and Member Group Technical Staff at TI, where he works on developing applications for TM4C12x family of high performance microcontrollers. Amit brings to this role his extensive experience in high-speed digital and microcontroller system-level design expertise. Amit earned his Bachelor of Engineering (BE) from University of Pune, India.

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