TI Designs

Thermal Protection of IGBT Modules for HEV and EV Traction Inverters Reference Design

Description

This reference design is a temperature sensing solution for IGBT thermal protection in hybrid electric vehicle and electric vehicle (HEV and EV) traction-inverter systems. The solution monitors the IGBT temperature through the NTC thermistor that is integrated inside of the IGBT module and provides thermal shutdown to the IGBT gate drivers once the NTC thermistor temperature rises above the programmed threshold. The design includes the IGBT isolated gate drivers, NTC signal conditioning, I^2C interface and isolation, and a load resistor that enables the system to run independently under high power ratings.

Resources

TIDA-00794	Design Folder
ISO5852S	Product Folder
ADS1015-Q1	Product Folder
LM5160-Q1	Product Folder
TPS57140-Q1	Product Folder
MSP-EXP430F5529LP	Tools Folder

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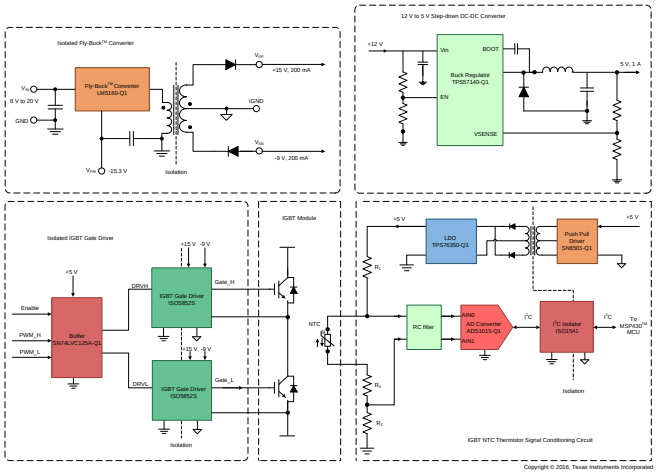
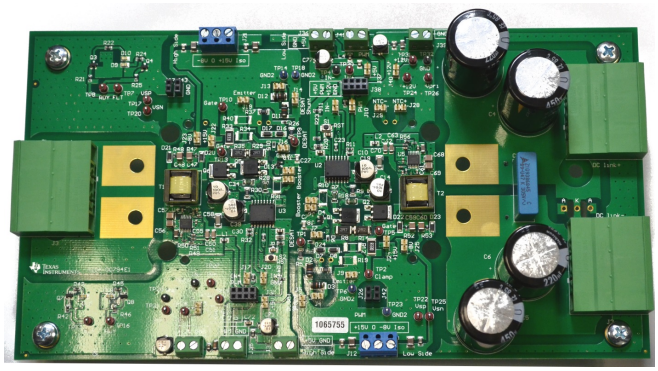
Features

- Designed for Traction Inverters With Rated Current up to 300 A and DC Bus Voltage up to 400 V
- An IGBT Half-Bridge Evaluation Platform That Includes Gate Driver, Isolation, NTC Signal Conditioning Circuit, Interface to MCU, and Load Resistor
- Push-Pull Current Boost at Gate Driver That Enables 10-A Source and 10-A Sink Peak Gate Currents
- One Multichannel ADC and one Isolation IC for Conditioning Multi NTCs in Inverter System
- 8-kV Reinforced Isolation and CMTI Greater Than 50 kV/µs

Applications

- HEV and EV Traction Inverters
- Variable Speed Motor Drives
- Solar Inverters





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1 System Overview

1.1 System Description

The IGBT modules in the HEV and EV traction inverter are carrying currents as high as 300 A, and the DC bus voltage up to 400 V, where temperature monitoring is a key criterion for overload protection. Integration of NTC (Negative Temperature Coefficient) thermistor with the IGBT modules is mostly adopted for the IGBT temperature sensing. Figure 1 shows one typical NTC temperature characteristic (see [1]). The resistance decreases flatly from 15 kΩ to 150 Ω with respect to the increase of the temperature from 0°C to 150°C. The NTC is designed for detection of long-term overload conditions. The NTC is not suitable for overtemperature protection during short-term failures such as short circuits.

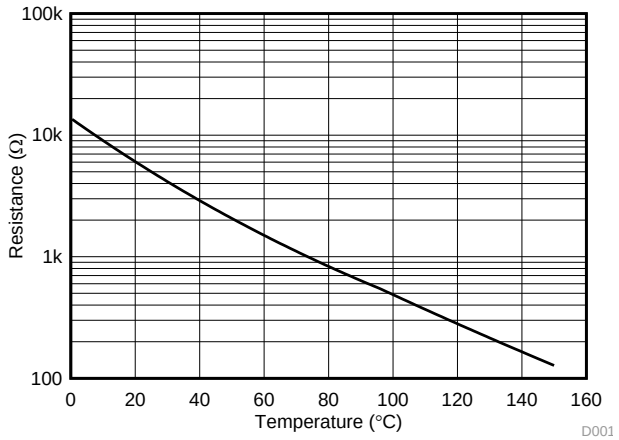


Figure 1. Resistance – Temperature Characteristic of NTC Inside Infineon Module

The TIDA-00794 reference design is a full temperature sensing solution for the IGBT modules in HEV and EV traction-inverter systems. It monitors the IGBT substrate temperature by signal conditioning the NTC thermistor that is integrated with the IGBT modules. It provides the thermal shutdown by disabling the IGBT gate drivers once the NTC thermistor temperature rises above the high temperature threshold, avoiding overheating of the IGBT module. The design includes the IGBT isolated gate drivers, isolated IGBT bias power, I^2C isolation, NTC signal conditioner, load resistor, and an I^2C interface to the MCU that enables the system to run independently under high power without requiring redundancy equipment.

The TIDA-00794 system consists of:

- The IGBT gate driver subsystem
- NTC signal conditioning subsystem
- MSP430™ LaunchPad™ Development Kit for controlling the IGBT and monitoring the temperature

The implemented IGBT module is Infineon FS300R07ME4_B11. There are two IGBTs inside of the package and they are connected in a half-bridge configuration. The NTC thermistor is mounted in proximity to the silicon chips to achieve a close thermal coupling. Two isolated IGBT gate drivers drive the high side and the low side IGBTs. The MSP430 sends the pulse-width modulation (PWM) signals to the gate driver. One multichannel ADC and one isolation IC are used for signal conditioning multi NTCs in the inverter. A 4-k V_{PEAK} isolation is applied between the NTC and the MSP430 MCU according to UL1577 and IEC60747-5-2 standards. The MSP430F5529 LaunchPad (MSP-EXP430F5529LP) is the center MCU that sends the PWM signals and provides the shutdown signal to the IGBT module. The MSP430 monitors the IGBT substrate temperature through I^2C communication with the ADS1015-Q1 analog-to-digital converter (ADC).

1.2 Key System Specifications

Table 1 provides the key system specifications and which sections to read for more information.

Table 1. Key System Specifications

FEATURE	PARAMETER	SPECIFICATION	DETAILS
DC link Power Stage	Input Voltage	400-V maximum	Section 1.5.1
	IGBT Power Module	Infineon FS300R07ME4_B11	
	Input DC current rating	40 A	
	DC bus Capacitors	880 µF at 450 V	
	Switching Frequency	30 kHz (maximum)	Section 1.5.5.3
IGBT gate driver	Isolation	12.8 kV_{PK} Surge	Section 1.5.5
		5.7 kV_{RMS} Isolation	
		8000 V_{PK} V_{IOTM} (transient)	
		2121 V_{PK} V_{IORM} (working voltage)	
	CMTI	120 kV/µs (typical)	
		and 100 kV/µs (minimum)	
	Protection	IGBT DESAT detection	
		Gate driver primary and secondary side power under voltage lockout	
		Active miller clamp	
		Safety input current limiting	
	Interface	PWM, FAULT, RESET, ENABLE, READY, and FAULT	
	Output current	2.5-A source	
		5-A sink	
	Push-pull current boost	10-A source	Section 1.5.5.4
		10-A sink	
IGBT Bias power	Input voltage	8 V to 20 V	Section 1.5.2
	Output	+15 V, 200 mA	
		–9 V, 200 mA	
	Transformer dielectric	2.5 kV for 1 minute	Section 1.5.2.2
		2.5 kV-surge	
NTC signal conditioning	Signal excitation	Resistive divider	Section 1.5.4
	I^2C isolation	2500-V working voltage	
		4242-V transient	
		4000-V surge	
	CMTI	50 kV/µs	
	Data sampling rate	3.3 k per second	
	Isolated Power Supply	+5 V, 150 mA	
	Transformer dielectric	2.5 kV for 1 minute	Section 1.5.4.1
		3.125-kV surge	

1.3 Block Diagram

The TIDA-00794 system consists of the IGBT gate driver subsystem and the NTC signal-conditioning system. Figure 2 and Figure 3 shows the block diagrams of the two subsystems. The implemented part numbers are shown in the diagrams.

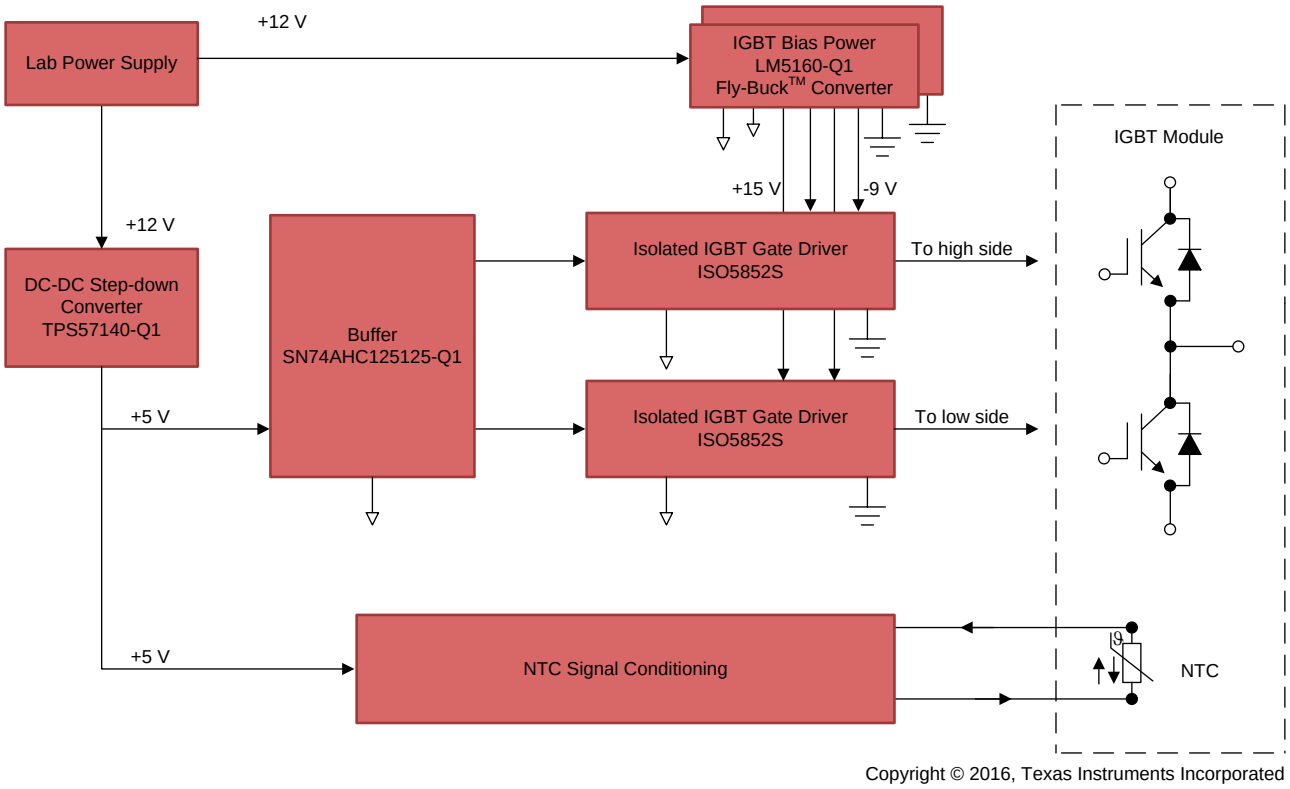


Figure 2. IGBT Gate Driver Subsystem

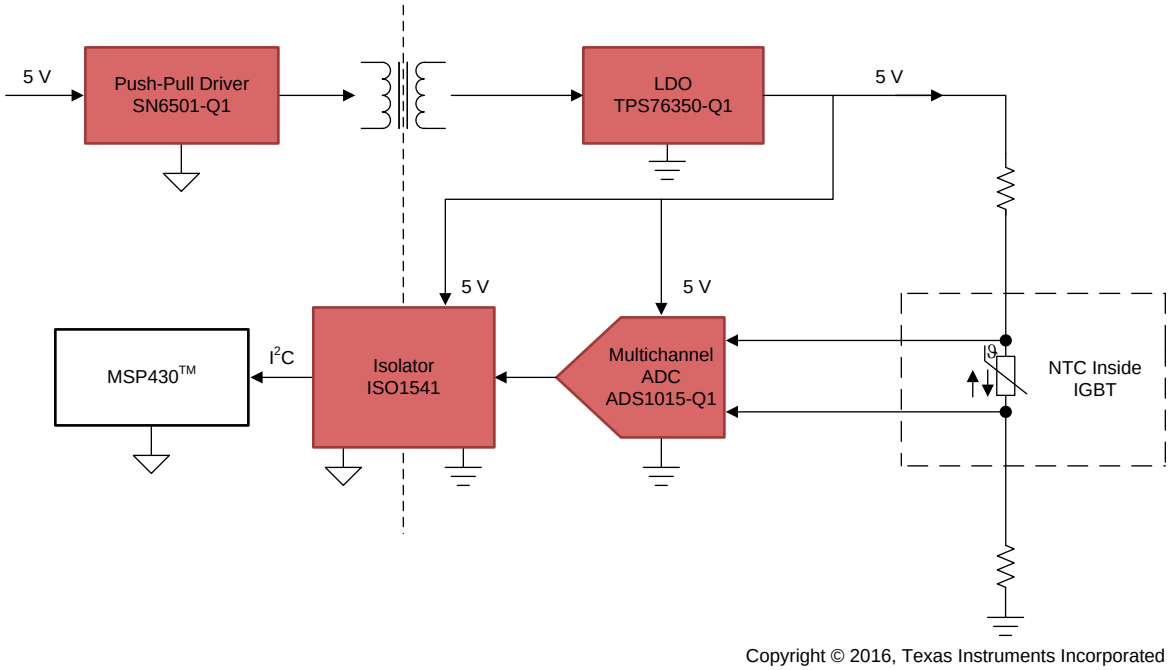


Figure 3. NTC Signal Conditioning Subsystem

The TIDA-00794 consists of four primary circuit blocks, shown in Figure 4.

- Isolated Fly-Buck™ converter (based on LM5160-Q1)
- 12-V to 5-V step-down DC-DC converter (based on TPS57140-Q1)
- Isolated IGBT gate driver (based on ISO5852S)
- NTC thermistor-signal conditioning circuit (based on SN6505-Q1, TPS76350-Q1, ADS1015-Q1, and ISO1541)

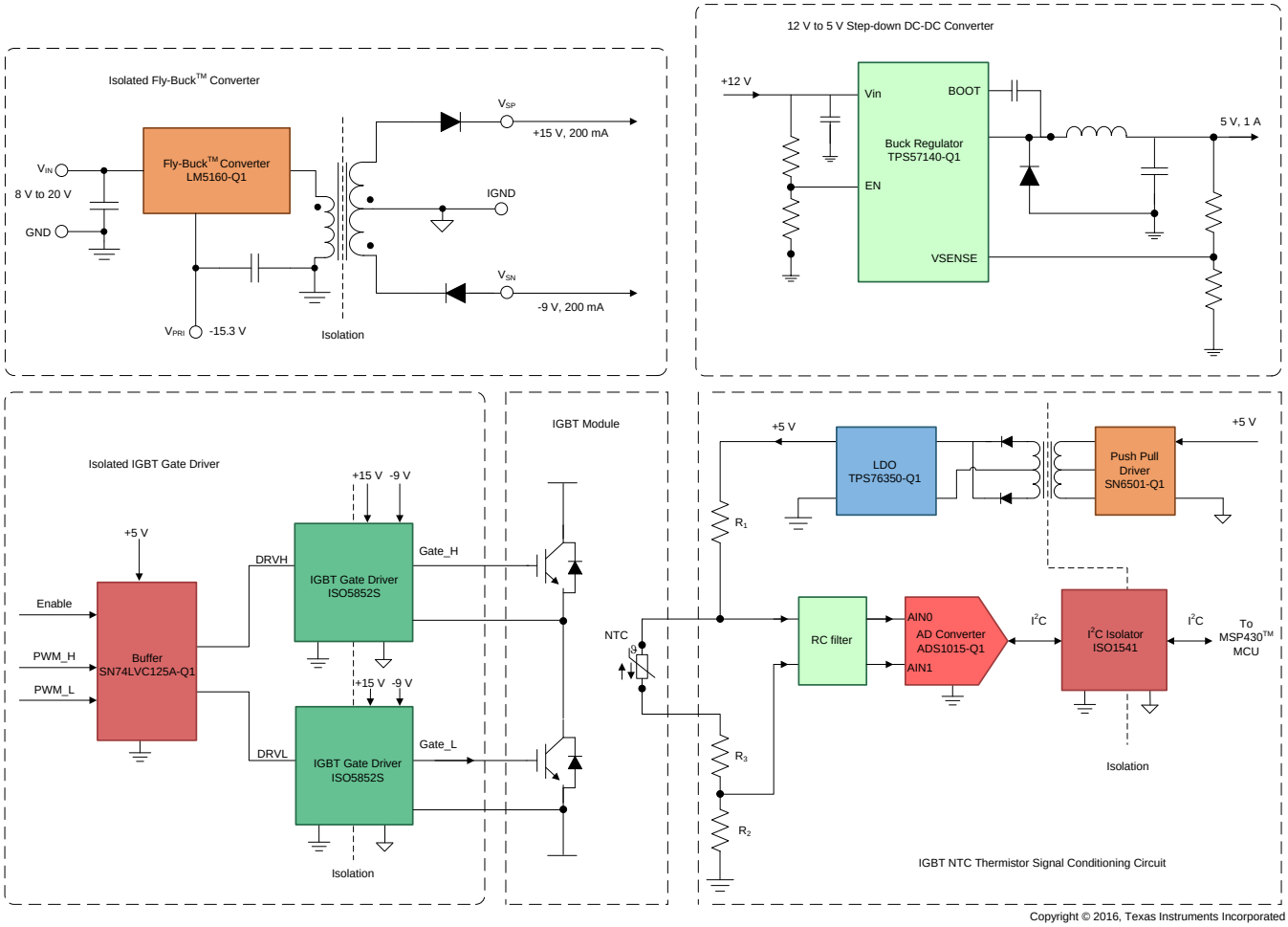


Figure 4. TIDa-00794 Block Diagrams

Figure 5 shows the TIDA-00794 system structure. The heat sink is at the bottom. The IGBT gate driver board is on top of the IGBT module.

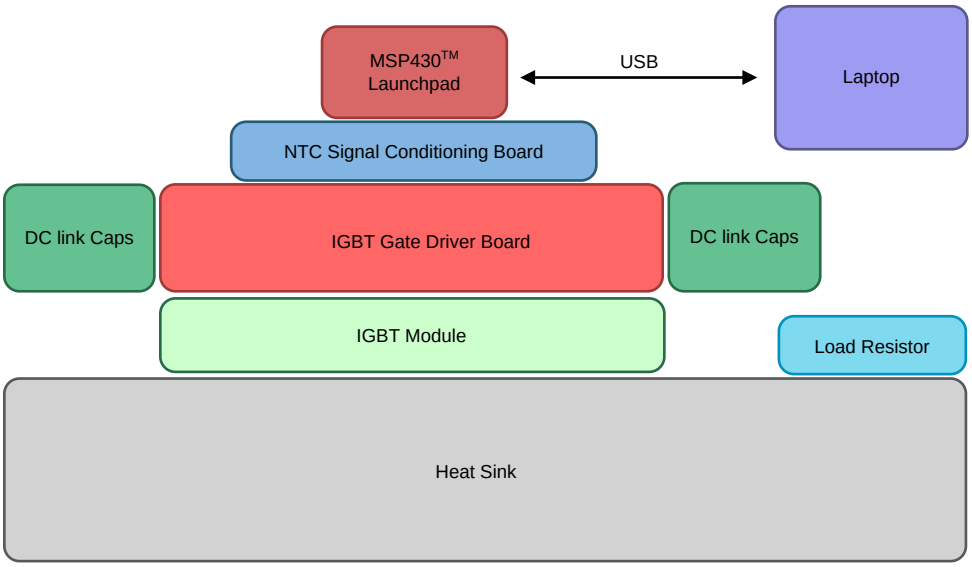


Figure 5. TIDA-00794 System Structure

1.4 Highlighted Products

1.4.1 ISO5852S

Figure 6 shows the diagram of the ISO5852S device. The ISO5852S device is a reinforced, isolated gate driver that is capable of driving a 1200-V IGBT module with current ratings from 50 A to 200 A. The device offers:

- Highest isolation ratings in the industry
  - 5.7 kV_{RMS} V_{ISO}
  - 8000-V_{PK} V_{IOTM} transient
  - 2121-V_{PK} V_{IORM} working voltage
- Split outputs
- OUTH (2.5 A) and OUTL (5 A)
- 12.8-kV_{PK} surge
- 120-kV/µs CMTI (typical)
- 100-kV/µs (minimum)

The device also includes the Miller clamp, soft turnoff, UVLO, DESAT detect, fault feedback, and ready-status feedback features.

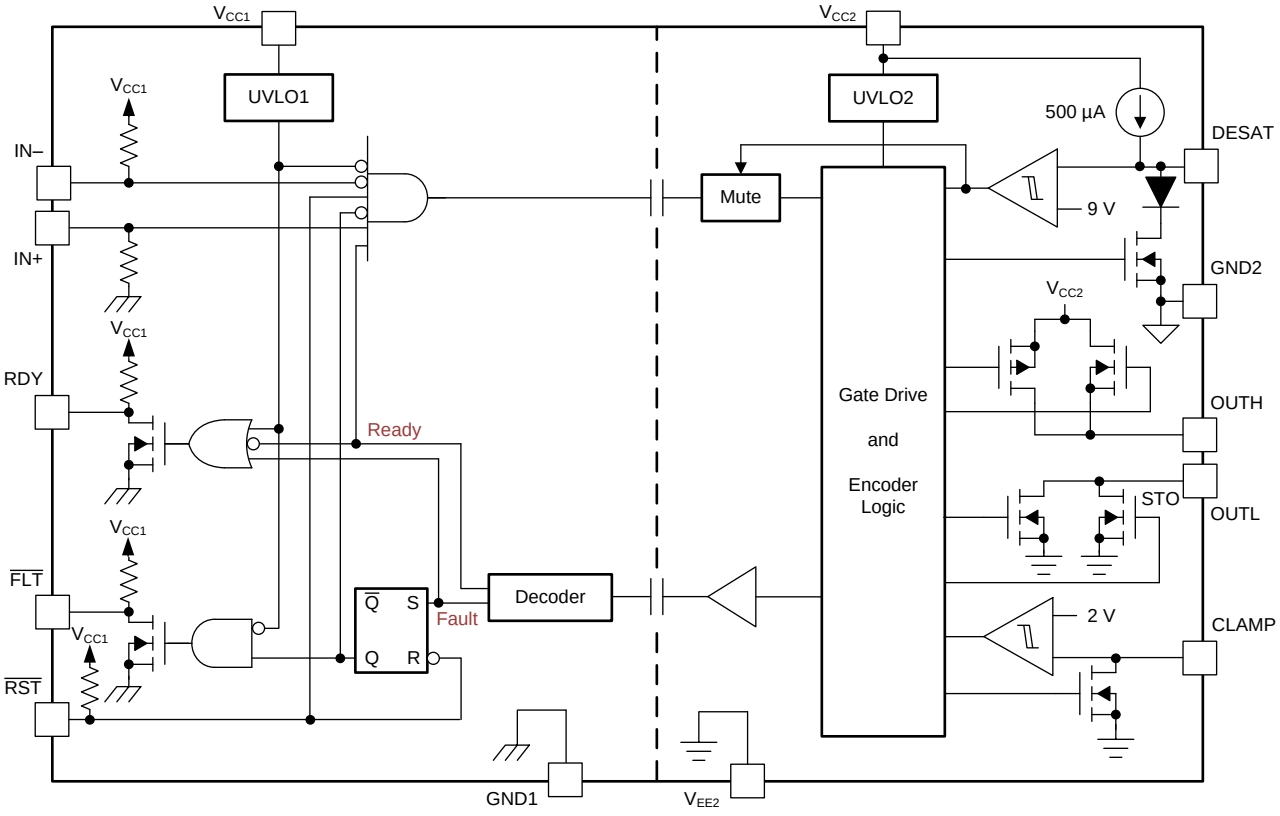


Figure 6. ISO5852S Block Diagram

1.4.2 ADS1015-Q1

Figure 7 shows the ADS1015-Q1 block diagram. The ADS1015-Q1 device is a 4-channel precision ADC with 12 bits resolution and an internal programmable gain amplifier (PGA). The ADS1015-Q1 can perform conversions at rates up to 3.3-k samples per second (ksps) with full scale at ±4.096 V/PGA. The ADS1015 family also uses an I^{2}C-compatible serial interface and operates from a single power supply ranging from 2.0 V to 5.5 V. The device offers conversion rates up to 3.3-ksps while consuming only 150 µA of supply current and operating down to 2.0 V.

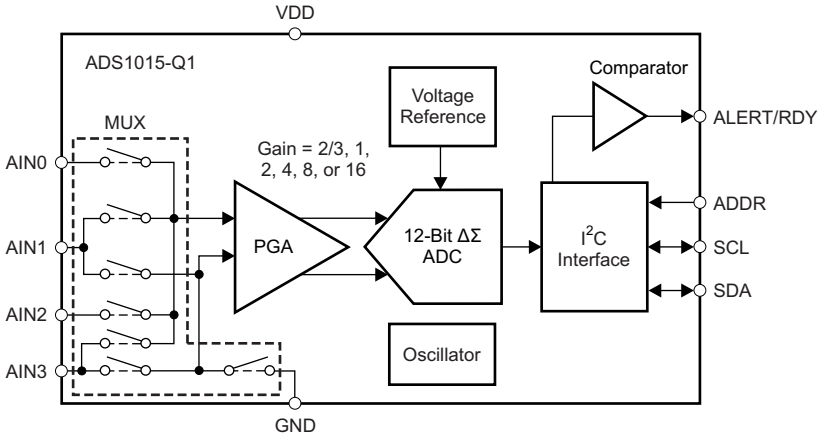


Figure 7. ADS1015-Q1 Block Diagram

1.4.3 LM5160-Q1

Figure 8 shows the LM5160-Q1 block diagram. The LM5160-Q1 device is the highest power synchronous step-down regulator in the industry that also supports TI Fly-Buck topology for delivering isolated bias supplies up to 15 W with no optoisolator. The integrated 1.5-A ultra-low on resistance synchronous MOSFETs of the LM6150-Q1 help extend TI Fly-Buck enabled devices to address higher bias power needs in industrial and automotive applications.

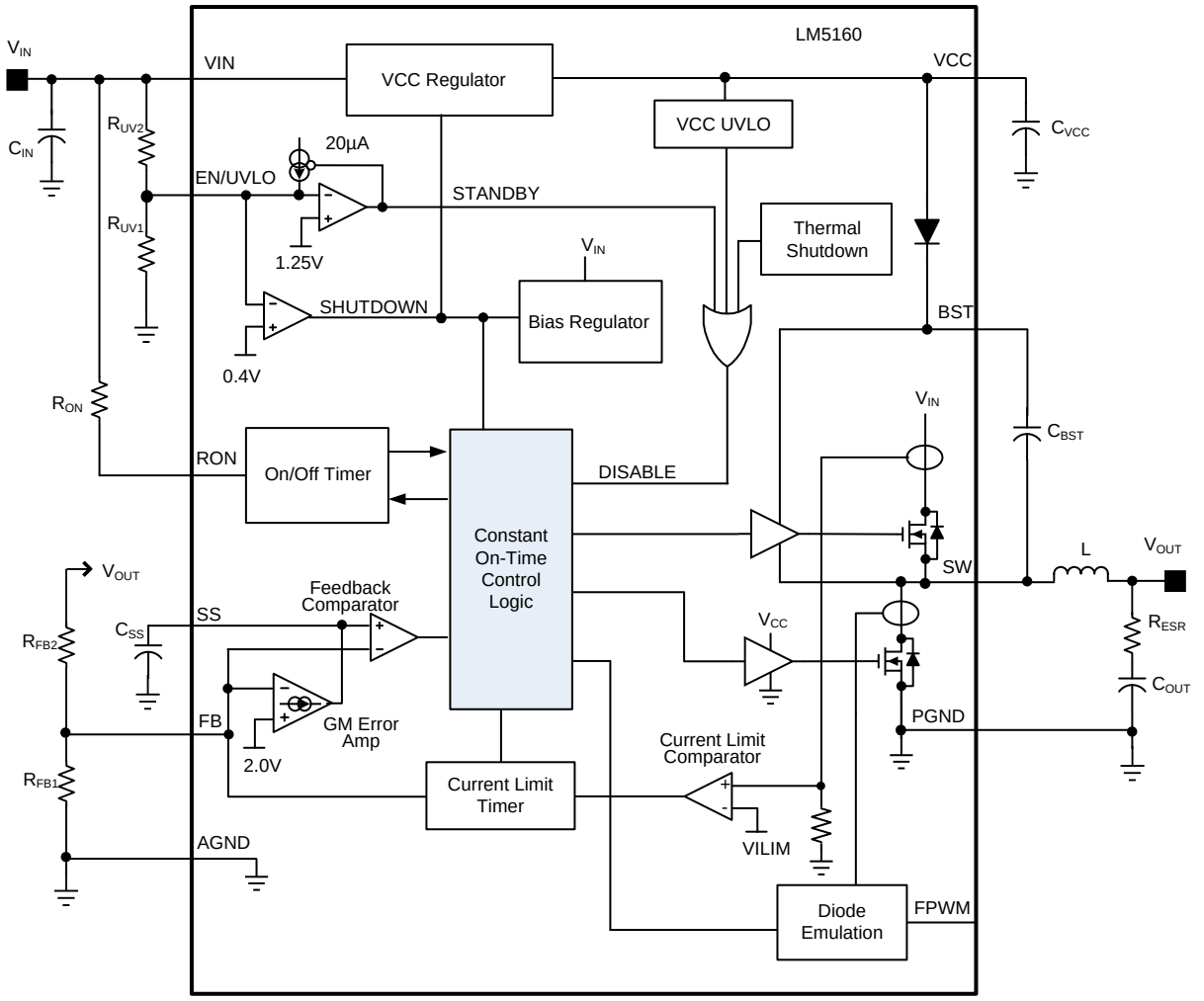


Figure 8. LM5160-Q1 Block Diagram

1.4.4 TPS57140-Q1

Figure 9 shows the TPs57140-Q1 block diagram. The TPS57140-Q1 device is a 42-V, 1.5-A step-down regulator with an integrated high-side MOSFET. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the no load, regulated output supply current to 116 µA. Using the enable pin, shutdown supply current is reduced to 1.5 µA.

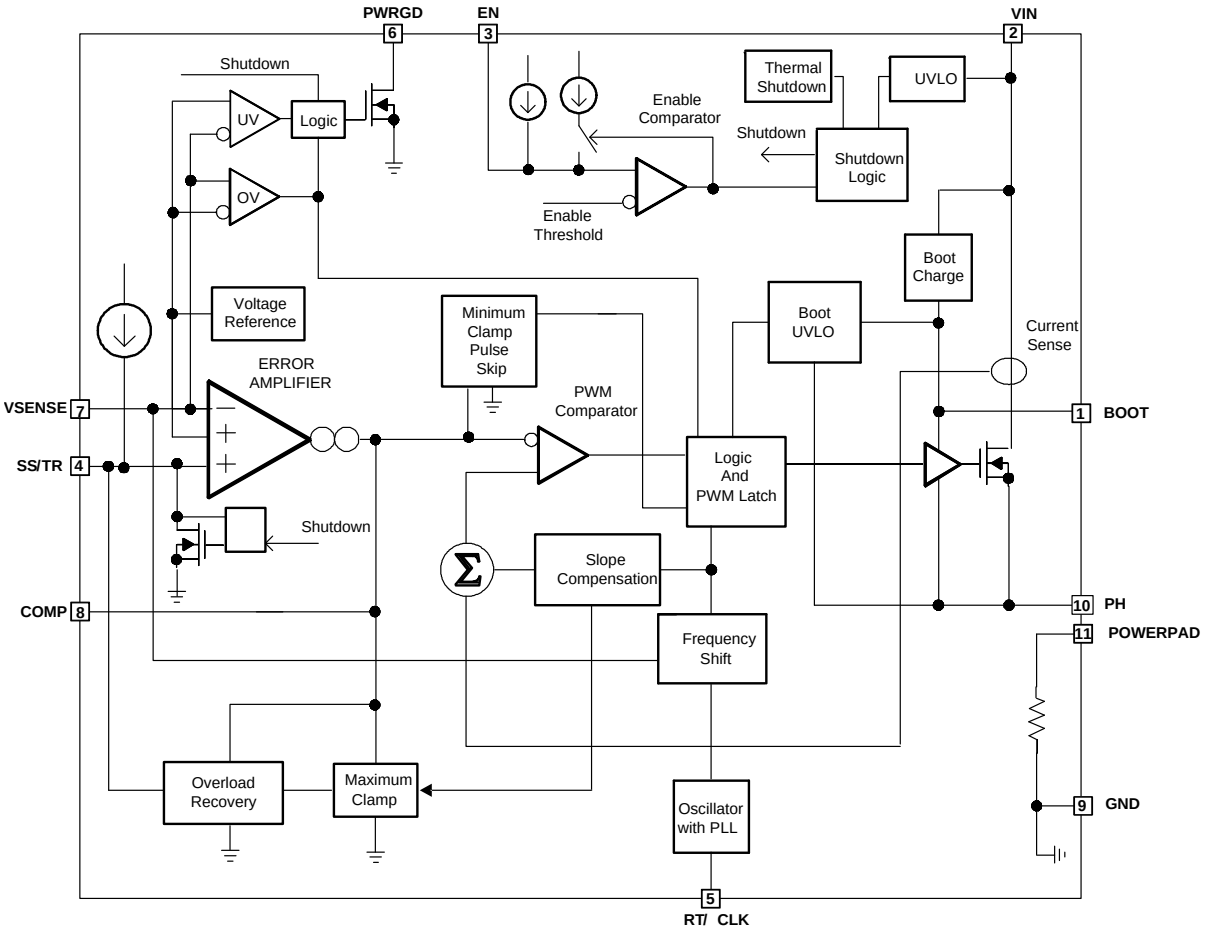


Figure 9. TPS57140-Q1 Block Diagram

1.4.5 TPS76350-Q1

Figure 9 shows the TPS76350-Q1 block diagram. The TPS76350-Q1 LDO offers the benefits of low-dropout voltage, low-power operation, and miniaturized packaging. These regulators feature low dropout voltages and quiescent currents compared to conventional LDO regulators. The TPS763xx devices are ideal for cost-sensitive designs and for applications where board space is at a premium because they are offered in a 5-terminal, small outline integrated-circuit SOT-23 package.

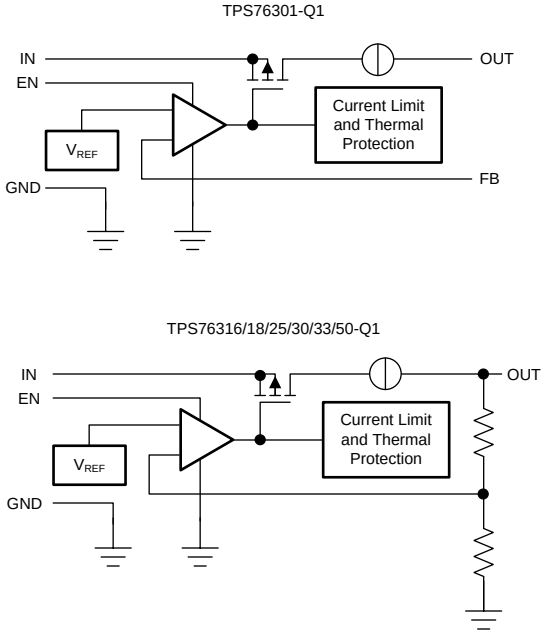


Figure 10. TPS76350-Q1 Block Diagram

1.4.6 SN6501-Q1

Figure 11 shows the SN6501-Q1 block diagram. The SN6501-Q1 device is a monolithic oscillator and power-driver designed for small form factor, isolated power supplies in isolated interface applications. The device drives a low-profile, center-tapped transformer primary from a 3.3 V or 5 V DC power supply, has a 350-mA output drive, thermal shutdown and soft start features, and switches at 410 kHz. The secondary can be wound to provide any isolated voltage based on transformer turns ratio.

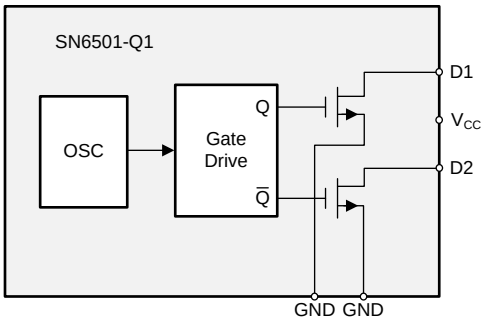


Figure 11. SN6501-Q1 Block Diagram

1.4.7 ISO1541

Figure 12 shows the ISO1541 block diagram. The ISO1541 device is a low-power, bidirectional isolator that is compatible with I^2C interfaces. The device has logic input and output buffers separated by TI capacitive isolation technology using a silicon-dioxide (SiO2) barrier. When used in conjunction with isolated power supplies, these devices block high voltages, isolate grounds, and prevent noise currents from entering the local ground and interfering with or damaging sensitive circuitry.

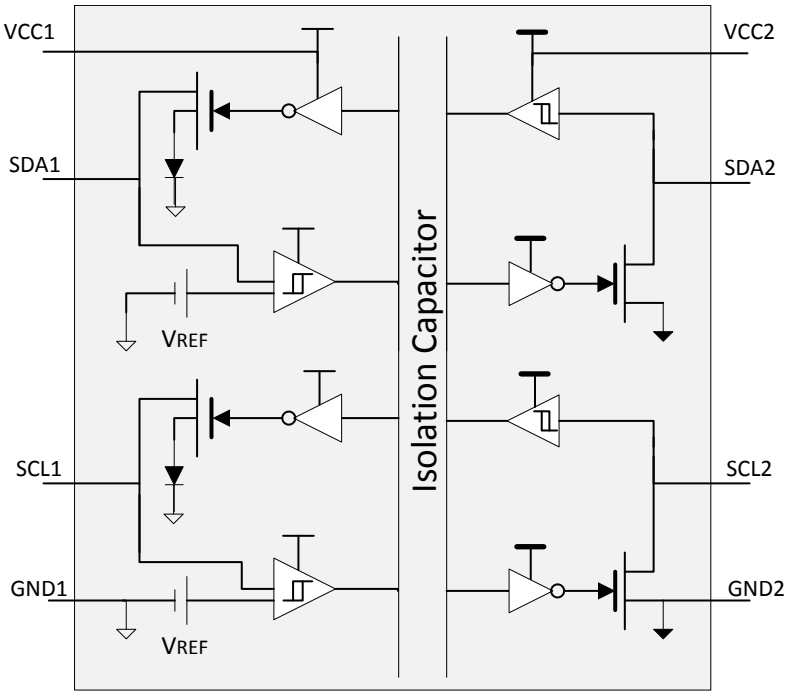


Figure 12. ISO1541 Block Diagram

1.5 System Design Theory

1.5.1 DC Link Power Stage

Figure 13 shows the schematic of the DC link power stage. Power diode D1 (IEW100E60) is for reverse polarity protection. A total of 880-µF capacitance (with 220 µF each) has been implemented. Two film capacitors (C1 and C2) are implemented for suppressing high frequency voltage spikes. Specifications of the power stage are shown in the following list:

- DC link voltage: 400-V maximum
- Resistor load: 22-Ω, 150-W chassis-mount resistor
- IGBT module: Infineon FS300R07ME4_B11
- Electrolytic capacitors: 220 µF, 450 V

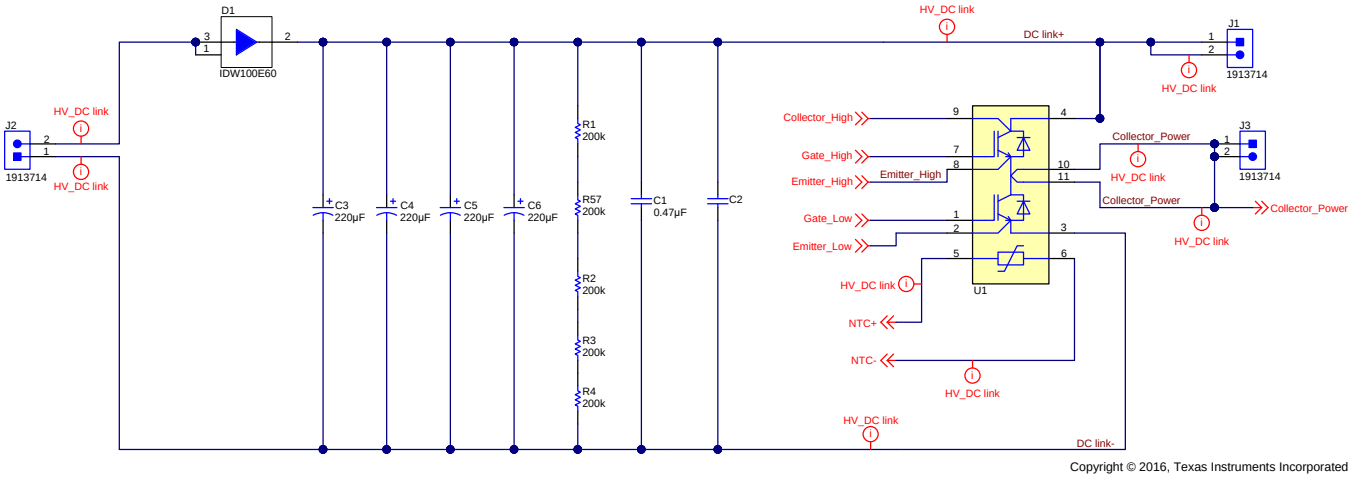


Figure 13. Schematic of Power Stage

Use Equation 1, Equation 2, Equation 3, Equation 4, and Equation 5 to calculate the main parameters.

Use Equation 1 to calculate and set the voltage ripple on the DC link (ΔV_{DC}) during operation.

$$\Delta V_{DC} = 400\ V \times 5\% = 20\ V \tag{1}$$

Use Equation 2 to estimate the required maximum DC link capacitance (C_{DC_MAX}).

$$C_{DC\_MAX} = \frac{i \times \Delta t}{\Delta V_{DC}} = \frac{i \times \frac{1}{F_{SW\_MIN}}}{\Delta V_{DC}} = \frac{200\ A \times (1/10\ kHz)}{20\ V} = 1000\ \mu F \tag{2}$$

where

- i is the normal operating current through the IGBT
- F_{SW_MIN} is the minimum switching frequency of the IGBT

Use Equation 3 and Equation 4 to calculate the short-circuit current of the IGBT (I_{SHORT}).

$$R_{DS\_ON} = \frac{V_{CESAT}}{I_{CESAT}} = \frac{1.75\ V}{300\ A} = 0.0058\ \Omega \tag{3}$$

$$I_{SHORT} = \frac{V_{DESAT}}{R_{DS\_ON}} = \frac{9\ V}{0.0058\ \Omega} = 1.551\,kA \tag{4}$$

where

- R_{DS_ON} is the channel resistance while IGBT is turned on
- V_{CESAT} is the collector-emitter saturation voltage
- I_{CESAT} is the collector-emitter saturation current
- V_{DESAT} is the desaturation voltage of the ISO5852S
- I_{SHORT} is the short-circuit current

Consider a short-circuit period of 6 µs and use Equation 5 to calculate the required DC link capacitance for a short-circuit test.

$$C_{DC\_SHORT} = \frac{I_{SHORT} \times \Delta t}{\Delta V_{DC}} = \frac{1551\,A \times 6\ \mu s}{20\ V} = 465.3\ \mu F \tag{5}$$

TI recommends implementing a total capacitance of 880 µF with four 220-µF electrolytic capacitors connected in parallel on the DC bus.

1.5.2 Isolated Fly-Buck™ Converter

Isolated power supplies are required for the gate driver bias power to turn on and turn off the IGBT gate. The power rails are connected to the secondary side of the IGBT gate driver. The Fly-Buck converter based on the LM5160-Q1 is implemented because it is cost-effective, easy-to-design, and has good flexibility [2]. The LM5160-Q1 can handle a wide voltage input (V_{IN}) range of 65 V that is important for this application.

The positive voltage of +15 V is generated to turn on the IGBT, and the negative voltage of –9 V is generated to turn off the IGBT. The voltages should be steady as they affect the switching speed. The negative rail holds the IGBT gate-emitter voltage below the threshold, preventing parasitic turn-ons induced by the Miller effect.

Figure 14 shows the schematic of the isolated Fly-Buck converter. The 15-V and –9-V voltages are obtained through the center-tapped transformer that can provide better voltage balance and regulation. In this configuration, the two rails can handle loads separately and the voltages do not collapse.

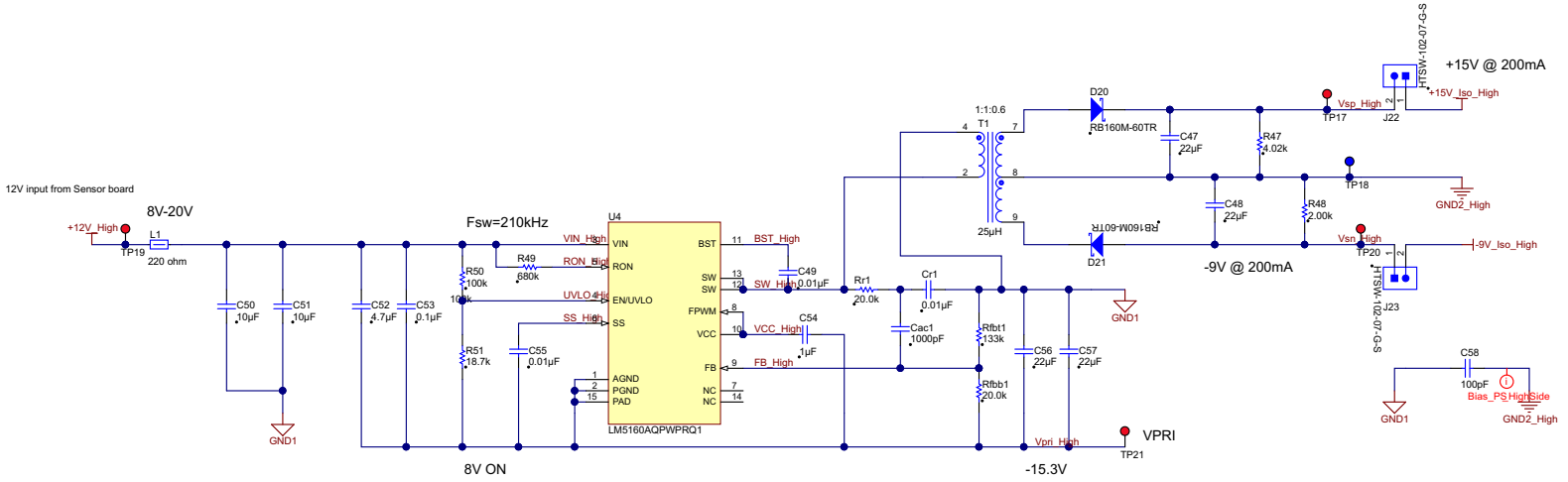


Figure 14. Schematic of Isolated Fly-Buck™ Converter

1.5.2.1 Power Requirement

The power that a Fly-Buck converter can give must be larger than the power dissipation in the IGBT gate driver circuit. Power dissipates in the gate driver circuit, the IGBT gate resistor, and any resistor in the gate drive when switching the IGBT on and off. IGBTs are switched at up to 30 kHz. Use Equation 6 to calculate power dissipation (P).

$$\begin{aligned} P &= P_{DC} + P_{SW} + P_{CG} \\ &= I_Q \times V_{DD} + \Delta V \times Q_G \times F_{SW} + \frac{1}{2} \times C_{IES} \times \Delta V^2 \\ &= 4.5\ \text{mA} \times 5\ \text{V} + 24\ \text{V} \times 3.3\ \mu\text{C} \times 30\ \text{kHz} + \frac{1}{2} \times 18.5\ \text{nF} \times 24^2 \\ &= 0.225 + 2.376 + 0.00533 = 2.6\ \text{W} \end{aligned} \tag{6}$$

where

- I_Q is the quiescent current of ISO5852S
- V_{DD} is the voltage applied to the primary side of the IS)5852S
- • C_{IES} is the input capacitance of the IGBT
- F_{SW} is the switching frequency
- ΔV is the voltage swing from turnon to turnoff at the IGBT

The isolated Fly-Buck converter power-supply specifications are provided in Table 2.

Table 2. Isolated Fly-Buck™ Converter Specifications

PARAMETER	SPECIFICATION
V_{IN}	8 V to 20 V
V_{OUT}	+15 V, –9-V dual isolated outputs
Output Ripple	±10%
I_{OUT}	+15 V at 200 mA, –9 V at 200 mA
Switching Frequency	210 kHz
P_{OUT}	4.8 W

1.5.2.2 Transformer Design

The turn ratio of the transformer is equal to the secondary-to-primary voltage ratio. The secondary windings are split into generating the positive and negative rails. The primary regulation voltage is set at –15.3 V.

Use Equation 7 to calculate the turn ratio of the primary-to-secondary positive rail (N_{PS_POS}).

$$N_{PS\_POS} = \frac{N_{PRI}}{N_{SEC\_POSITIVE}} = \frac{15.3\ \text{V}}{15\ \text{V}} = 1.02:1 \tag{7}$$

where

- N_{PRI} is the number of turns at the primary side
- $N_{SEC\_POSITIVE}$ is the number of turns at the secondary side of the +15-V rail

Use Equation 8 to calculate the turn ratio of the primary-to-secondary negative rail (N_{PS_NEG}).

$$N_{PS\_NEG} = \frac{N_{PRI}}{N_{SEC\_NEGATATIVE}} = \frac{15.3\ \text{V}}{9\ \text{V}} = 1.7:1 \tag{8}$$

where

- $N_{SEC\_NEGATIVE}$ is the number of turns at the secondary side of the –9-V rail

The primary side inductance determines the peak current flowing into the device switch. The LM5160-Q1 has a switch-current limit of 2.5 A. Consider the efficiency of 80% at 200-mA full load and use Equation 9 and Equation 10 to calculate the average current at the primary side (I_{PR_AVG}).

$$P_{IN} = \frac{P_{OUT}}{\eta} = \frac{4.8\ W}{0.8\ W} = 6\ W \tag{9}$$

$$I_{PRI\_AVG} = \frac{P_{IN}}{V_{PRI}} = 0.6\ A \tag{10}$$

where

- P_{IN} is the input power
- P_{OUT} is the output power
- η is the transformer efficiency
- V_{PRI} is the voltage across the primary winding

Use Equation 11 and Equation 12 to calculate the maximum ripple current at the primary side (ΔI_{RIPPLE}).

$$I_{PRI\_PEAK} = I_{PRI\_AVG} + \frac{1}{2} \times \Delta I_{RIPPLE} = 2.5\ A \tag{11}$$

$$\Delta I_{RIPPLE} = (2.5\ A - 0.6\ A) \times 2 = 3.8\ A \tag{12}$$

where

- I_{PRI_PEAK} is the peak current flowing through the primary winding

TI recommends choosing a 1.8-A ripple to keep the MOSFET within a safe region. Use Equation 13, Equation 14, and Equation 15 to calculate the inductance of the primary winding of the transformer (L_{PRI}).

$$V_{PRI} = L_{PRI} \times \frac{\Delta I_{RIPPLE}}{\Delta t} = L_{PRI} \times \frac{\Delta I_{RIPPLE}}{(1 - D) \times F_{SW}} \tag{13}$$

$$D = \frac{V_{OUT}}{V_{IN}} = \frac{15.3\ V}{12\ V + 15.3\ V} = 0.56 \tag{14}$$

$$L_{PRI} = \frac{V_{PRI}}{\Delta I_{RIPPLE}} \times \frac{1 - D}{F_{SW}} = \frac{20\ V}{1.8\ A} \times \frac{1 - 0.56}{210\ khz} = 23.2\ \mu H \tag{15}$$

where

- D is the switching duty cycle
- f_{SW} is the switching frequency of the converter
- V_{OUT} is the converter output voltage
- V_{IN} is the converter input voltage

TI recommends choosing the WÜRTH transformer (part number 750315445). The transformer is built with an EPC13 core through-hole package. The primary inductance of the transformer is 25 µH and has a turn ratio of N_{PS_POS} is 1 to 1, and N_{PS_NEG} is 1.67 to 1. The saturation current is 2.5 A. The DC resistances from three windings are 0.038 Ω, 0.092 Ω, and 0.063 Ω (see [5]).

1.5.2.3 Output Capacitor

The gate driver must deliver a peak current of 10-A source at turnon and 10-A sink at turnoff switching transients. The bias power supply must have sufficient output capacitance to minimize output ripple. This output capacitance requires the output capacitor to be sufficient enough to maintain the ripple below ±10%.

Use Equation 16 and Equation 17 to calculate the required capacitance (C_{OUT}) for a 15-V rail.

$$I_{PEAK} = C_{OUT} \times \frac{V_{DROP}}{T_{PD}} \tag{16}$$

$$V_{DROP} = 15\,V \times 10\% = 1.5\,V \tag{17}$$

where

- i_{PEAK} is the peak current that the gate driver requires
- V_{DROP} is the allowed voltage drop
- t_{PD} is the duration of the peak current

Use Equation 18 to calculate t_{PD}.

$$T_{PD} = \frac{Q_G}{I_{PEAK}} = \frac{3.3\,\mu C}{10\,A} = 0.33\,\mu s \tag{18}$$

where

- Q_G is the gate charge of the IGBT

Use Equation 19 to calculate C_{OUT}.

$$C_{OUT} = I_{PEAK} \times \frac{T_{PD}}{V_{DROP}} = 10\,A \times \frac{0.33\,\mu s}{1.5\,V} = 2.24\,\mu F \tag{19}$$

The capacitance for a –9-V rail can be calculated by using the same equations that were used for the 15-V rail. Positive and negative rails are implemented with 22-µF capacitors for sufficient energy and to overcome the DC-biasing effect.

1.5.3 12-V to 5-V Step-Down Converter

A +5-V rail is required for the auxiliary power supply. The +5-V rail power the SN6501-Q1 push-pull driver, the primary side of the ISO5852S gate driver, and the primary side of the ISO1541 I^2C isolator. The TPS57140-Q1 converts the +5 V from the +12-V input. TI recommends adding a CLC (4.7 µF, 1.5 µH, 4.7 µF) filter at the input to reduce the EMI noise generated from this power supply (see [3]). TI also recommends adding a RC snubber across the switching node to reduce the voltage spikes.

Table 3 provides the 12-V to 5-V step-down DC-DC converter specifications.

Table 3. 12-V to 5-V Step-Down Converter Specifications

PARAMETER	SPECIFICATION
V_{IN}	8 V to 18 V
V_{OUT}	+5 V
Output current ripple	±20%
I_{OUT}	1 A
Switching frequency	1 MHz
P_{OUT}	5 W

Figure 15 shows the schematic of the 12-V to 5-V step-down converter.

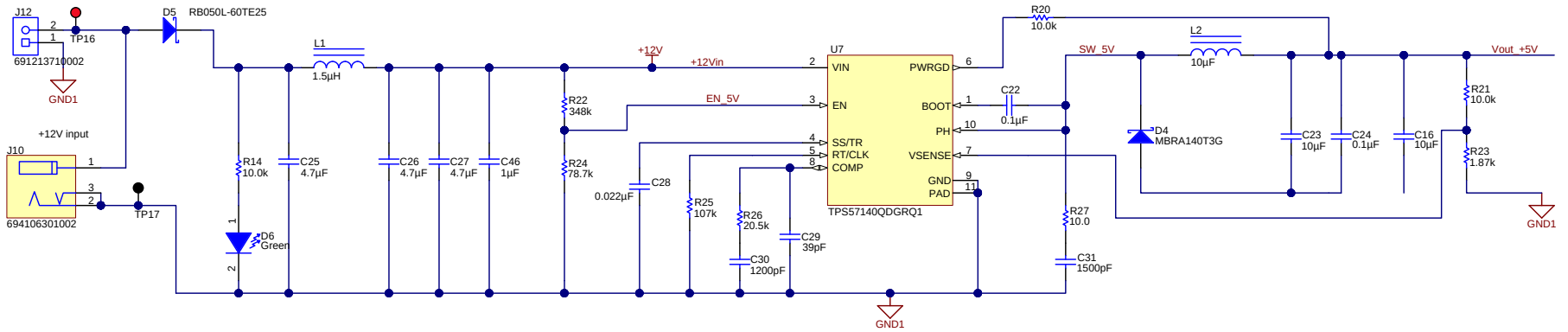


Figure 15. 12-V to 5-V Step-Down DC-DC Converter Schematic

1.5.3.1 Components Calculations

TI recommends choosing a switching frequency (f_{SW}) of approximately 1 MHz. The switching frequency is programmed by grounding the RT/CLK pin through a resistor (R_T). Use Equation 20 to calculate R_T.

$$R_T = \frac{206033}{F_{SW}(kHz)^{1.0888}} = \frac{206033}{1044^{1.0888}} = 107 k\Omega \tag{20}$$

Consider a 20% output-current ripple (I_{RIPPLE}) and use Equation 21 to calculate the minimum ouput conductance (L_{OUT_MIN}).

$$L_{OUT\_MIN} = \frac{V_{IN\_MAX} - V_{OUT}}{I_{RIPPLE}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times F_{SW}}$$

$$L_{OUT\_MIN} = \frac{13 - 5}{1\,A \times 40\%} \times \frac{5}{13 \times 1.044\,MHz}$$

$$L_{OUT\_MIN} = 7.3\ \mu H \tag{21}$$

where

- V_{IN_MAX} is the maximum input voltage
- V_{OUT} is the output voltage

TI recommends choosing an output inductance of 10 µH. Use Equation 22 to calculate the output peak current (I_{OUT_PEAK}).

$$I_{OUTPEAK} = I_{OUT} + I_{RIPPLE} = 1.05\ A \tag{22}$$

The output capacitance must sustain the voltage transient change during load dump. Consider a 4% variation of the output voltage and use Equation 23 to calculate the minimum output capacitance (C_{OUT_MIN}).

$$C_{OUT\_MIN} = \frac{2 \times \Delta I_{OUT}}{F_{SW} \times \Delta V_{OUT}} = \frac{2 \times 1\,A}{1.044\,MHz \times 5\,V \times 4\%} = 9.58\,\mu F \quad (23)$$

where

where

- ΔI_{OUT} is the change in the output current
- f_{SW} is the converter switching frequency
- ΔV_{OUT} is the allowable variation in the output voltage

TI recommends choosing a 20-µF output capacitance.

Choose V_{OUT} ripple as 1% and then use Equation 24 to calculate the maximum ESR of the output capacitor (C_{ESR}).

$$C_{ESR} = \frac{V_{OUT\_RIPPLE}}{I_{RIPPLE}} = \frac{5 \times 1\%}{0.4\,A} = 250\,m\Omega \quad (24)$$

1.5.3.2 Compensation

Use the TPS57xx0-Q1 calculation tool (see [4]) for calculating compensation network components. For most conditions, the regulator requires a phase margin between 60° and 90° at the crossover frequency. The TPS57140-Q1 uses type 2A compensation circuits where two capacitors and one resistor are required. Figure 16 shows different types of frequency compensation.

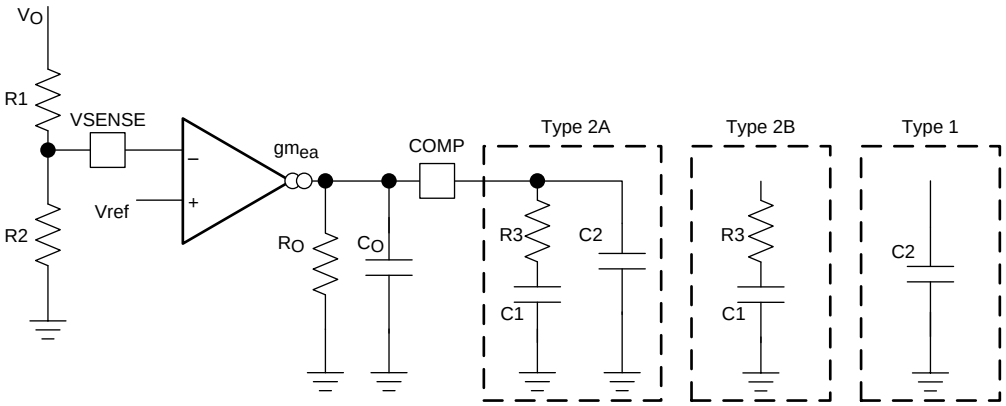


Figure 16. Different Types of Frequency Compensation

A phase margin of 77° is achieved by implementing compensation components. Figure 17 shows the calculated gain and phase margin plots.

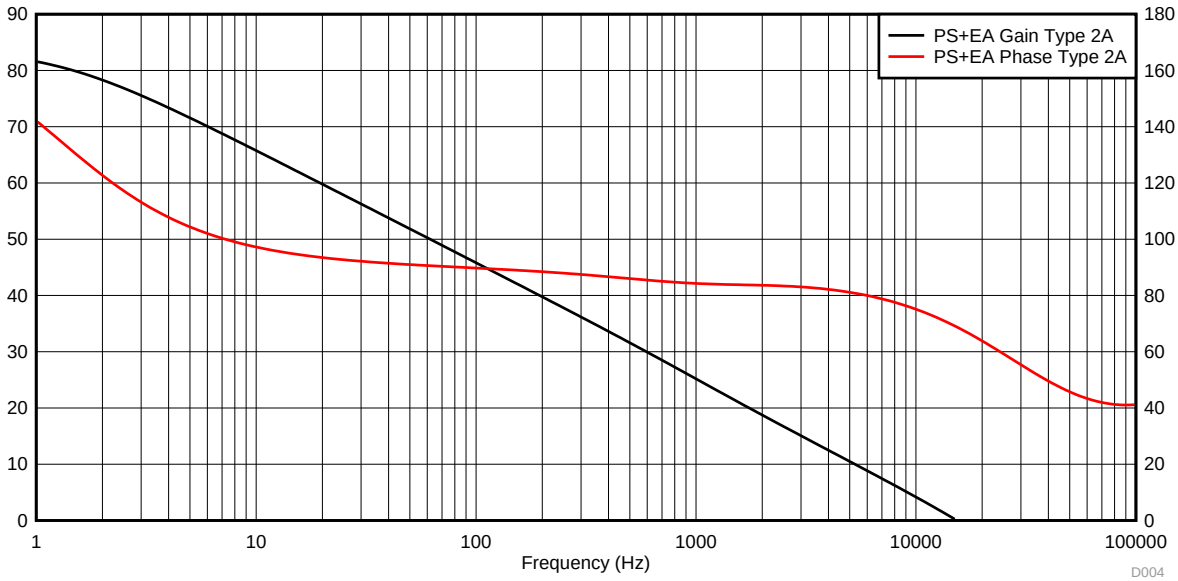


Figure 17. Achieved Gain and Phase Margin of 12-V to 5-V Step-Down DC-DC Converter

1.5.4 NTC Thermistor Signal Conditioning

The signal conditioning circuit processes the excited signal input from the NTC thermistor and sends it to the MCU. Signal excitation to the NTC thermistor is obtained from a resistive divider. Various differential voltages are generated with regards to the NTC resistance changes at different temperatures. Figure 18 shows the block diagram of the NTC signal-conditioning circuit.

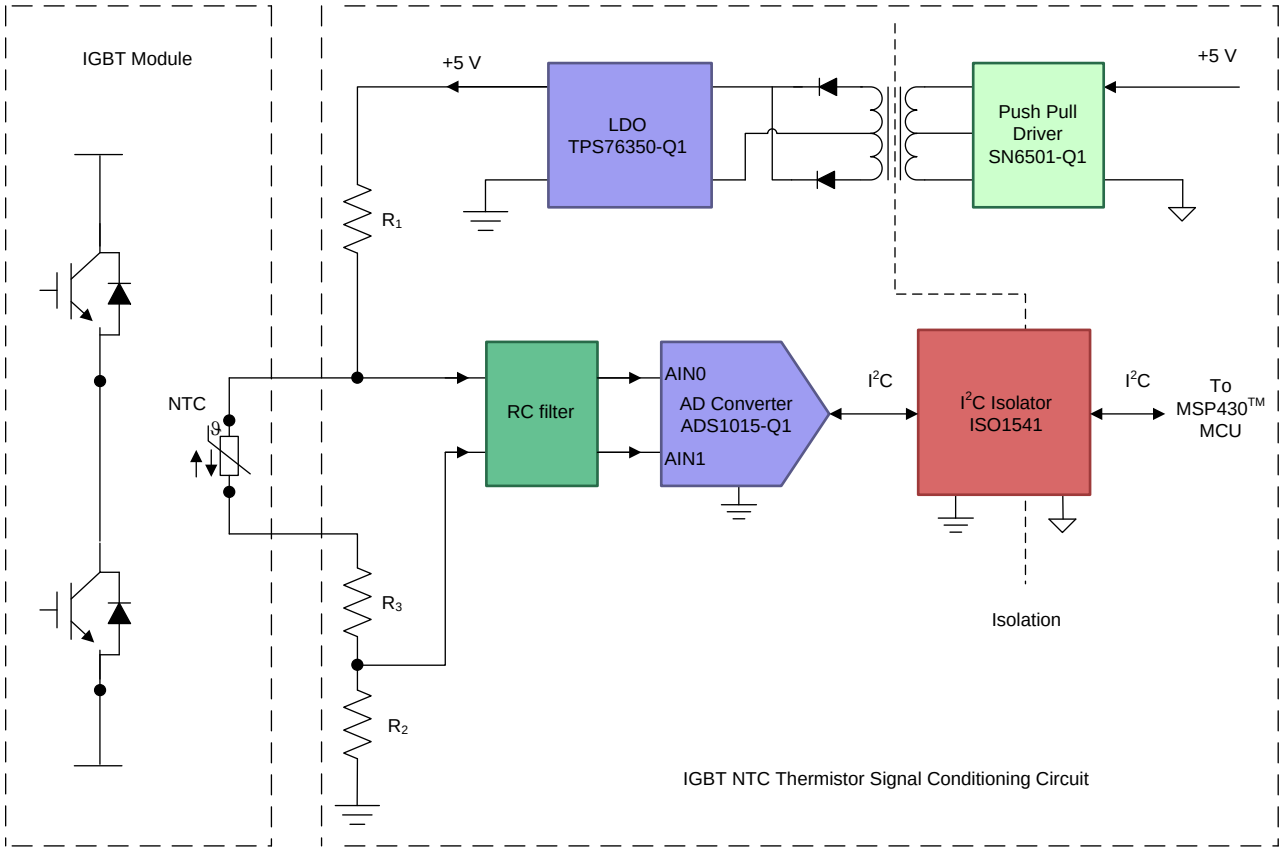


Figure 18. NTC Signal Conditioning Circuit Block Diagram

The SN6501-Q1 push-pull driver generates an isolated +5 V that supplies the divider, the ADS1015-Q1, and the primary side of the ISO1541 I^2C isolator. The multichannel ADC ADS1015-Q1 processes the multichannel signals from multiple NTCs from the three IGBT bridges in a complete inverter system. The ADS1015 features an input multiplexer that enables the I^2C communication through a single I^2C isolator. The ISO1541 isolates the MCU from the low-voltage side to the IGBT high-voltage side.

1.5.4.1 Push-Pull Isolated Power Supply

The total current consumption from the signal conditioning circuit consumes 50 mA from the isolated +5-V power rail. The push-pull isolated-converter output current is designed for 150 mA that is sufficient for three channels of NTC signal conditioning. The push-pull converter uses a center-tap configuration and provides isolated +5 V. The secondary transformer is designed to provide 6.25-V output, then a LDO is connected to regulate the +5-V output within ±2%. Table 4 provides the specifications of the converter.

Table 4. Push-Pull Isolated-Converter Specifications

PARAMETER	SPECIFICATION
V_{IN}	5 V, ±5%
V_{OUT}	+5 V
Output ripple	< 200 mV at full load
Full load	150 mA
Switching frequency	300 kHz to 620 kHz

Figure 19 shows the schematic of the push-pull isolated power supply. The schematic shows several external, discrete components: transformer T1, rectifier diodes D1 and D2, output capacitors C3, C12, C5, and C5.

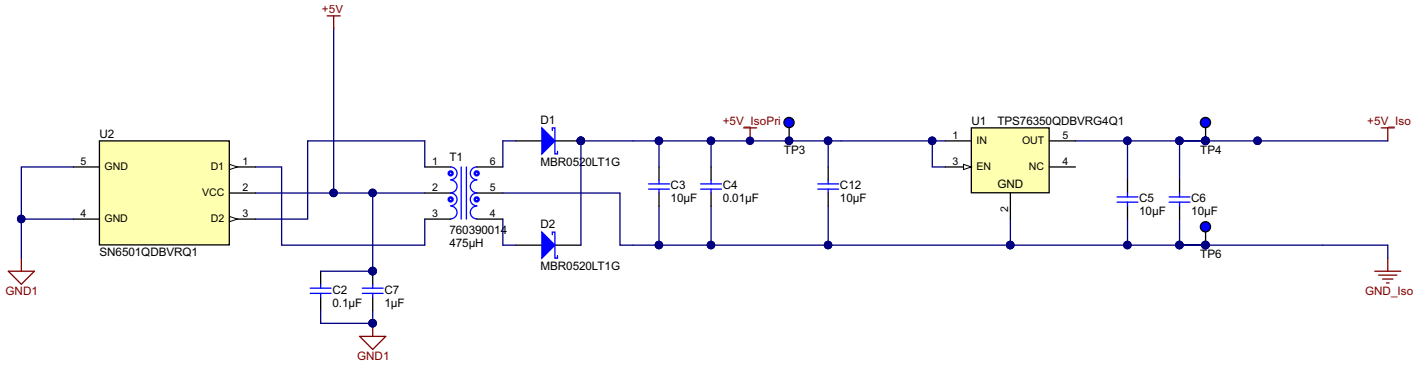


Figure 19. Push-Pull Isolated Power-Supply Schematic

Use Equation 25 to calculate the input peak current. Use η = 0.97 to account for transformer power-transfer efficiency.

$$I_{IN\_PEAK} = \frac{P_{OUT\_MAX} \div \eta}{V_{IN\_MIN}} = \frac{(5\ V \times 1.1 \times 0.3) \div 0.97}{4.75\ V} = 358\ mA \quad (25)$$

where

- P_{OUT_MAX} is the maximum output power

The SN6501-Q1 switches the internal dual MOSFETs with approximately 50% duty cycle each. Use Equation 26 to calculate the AC current that is flowing through the primary transformer (I_{PRI}).

$$I_{PRI} = \frac{I_{IN\_PEAK}}{2} = \frac{358\ mA}{2} = 179\ mA \quad (26)$$

Use Equation 27 to calculate the transformer turn ratio.

$$N_{PS} = \frac{V_{SEC} + V_F}{V_{PRI}} = \frac{6.25V + 0.35V}{5V} = 1.32:1 \quad (27)$$

where

- V_{SEC} is the voltage across the secondary winding
- V_F is the forward voltage of the diode
- V_{PRI} is the voltage across the primary winding

The Vt product of the transformer must be greater than Vt_{MIN}. Use Equation 28 to calculate Vt_{MIN}.

$$Vt_{MIN} = V_{IN\_MAX} \times \frac{T_{MAX}}{2} = \frac{V_{IN\_MAX}}{2 \times F_{MIN}} = \frac{5\ V \times 1.05}{2 \times 300\ kHz} = 8.75\ V\mu s \quad (28)$$

where

- F_{MIN} is the minimum switching frequency

TI recommends choosing the WÜRTH transformer number 760390014 [6] for this design.

1.5.4.2 ADC Front End

Figure 20 shows the ADC front end schematic. A resistive divider is used for signal excitation. Two 9.09-kΩ resistors are connected from +5 V to the NTC and from the NTC to ground. The ADS1015-Q1 is configured by the MSP430 through the I^2C communication during power up. Channels AIN0 and AIN1 have been selected and configured as differential inputs. Two TVS diodes SMAJ6.0A are added for high voltage-spike protection.

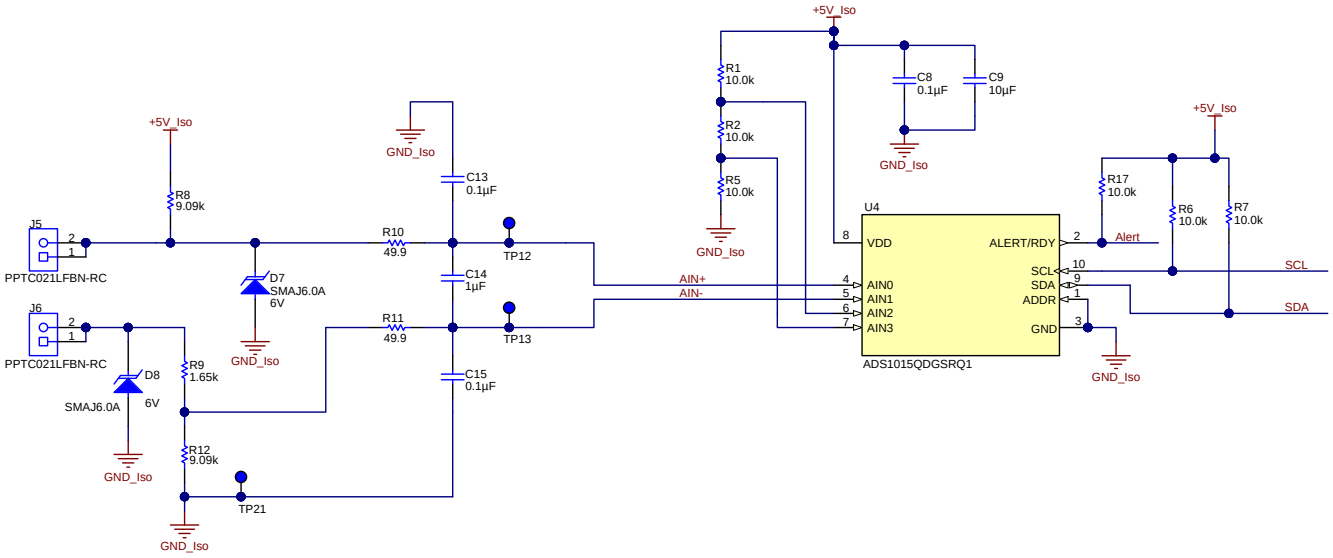


Figure 20. ADC Front-End Schematic

Four registers of the ADS1015-Q1 must be addressed.

- The conversion register contains the result of the last conversion in binary twos complement format.
- The configuration register sets the operating mode, input selection, data rate, programmable gain amplifier (PGA), and comparator modes. The PGA is set to two in this design to allow a full scale input of ±2.048 V. Window comparator is used, setting the ALERT-signal latches when the conversions are within the margin of the upper and lower threshold-temperature values. Set the comparator polarity as active low. Set the conversion rate to 3.3 ksps. Configure the I^2C clock frequency to be 400 kHz.
- The lo_thresh register sets the low threshold temperature value.
- The hi_thresh sets the high threshold temperature value.

1.5.4.3 Simulation

The circuit is implemented into the TINA-TI™ simulation software (see Figure 21). Add an RC filter at the input to reduce noise. Use Equation 29 to calculate and set the corner frequency (F_{CORNER}) of the RC filter to one-twentieth of the IGBT switching frequency.

$$F_{CORNER} = \frac{1}{2 \times \pi \times R \times C} = \frac{1}{2 \times \pi \times (49.9 + 49.9) \times 1\,\mu F} = 1.5\ kHz \tag{29}$$

An operation amplifier (OPA348) simulates the internal PGA of the ADS1015-Q1. The differential gain is set to two.

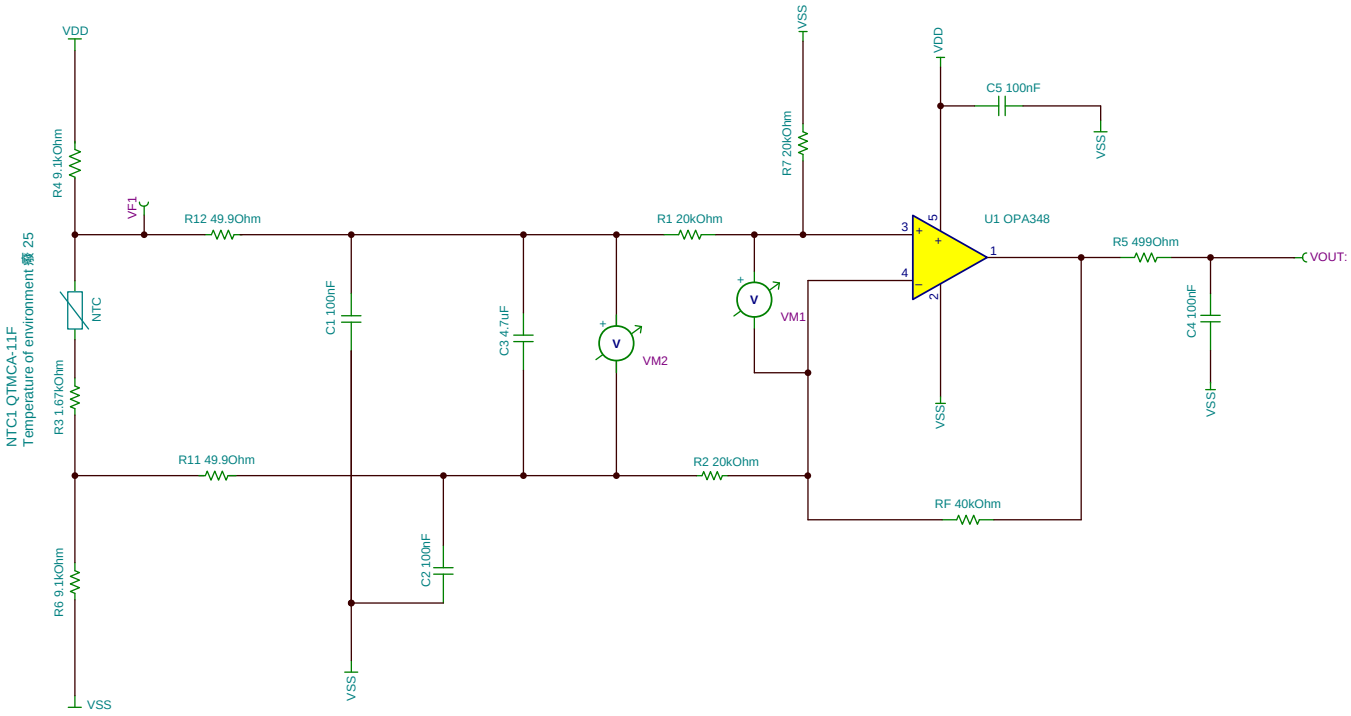


Figure 21. NTC Signal Conditioning AFE Simulation Circuit

Figure 22 shows the simulation results of the NTC AFE circuit. The output voltage from the AFE circuit (V_{OUT}) changes linearly with regards to the temperature change from 0°C to 150°C. The results show that this AFE circuit is suitable for this design. VF1 is the output of the signal excitation. VM2 is the generated differential voltage that is fed into the ADS1015-Q1 channels AN0 and AN1.

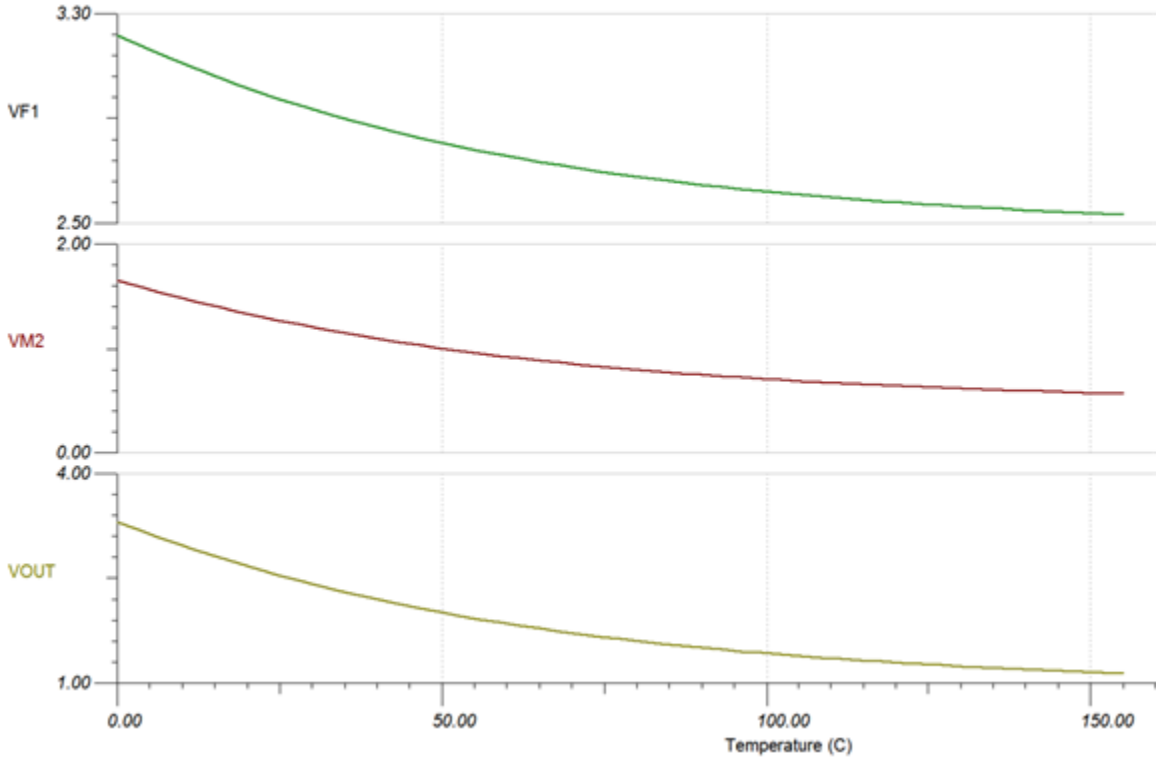


Figure 22. Simulated Results of NTC AFE Circuit

1.5.4.4 I²C Isolation

I²C isolation is implemented to ensure the central MCU safely communicates with the signal conditioning circuit. The ISO1541 bidirectional I²C isolator has been implemented. The isolator accepts the supply voltage from 3 V to 5.5 V at the primary and secondary sides. The ISO1541 provides 4.2-k peak isolation and supports up to a 1 MHz data transfer speed.

Figure 23 shows the I²C isolation. The +3.3-V rail and ground from the MSP430 LaunchPad is connected to the primary side. The +5 V and the isolated ground from the push-pull isolated power supply is connected to the secondary side.

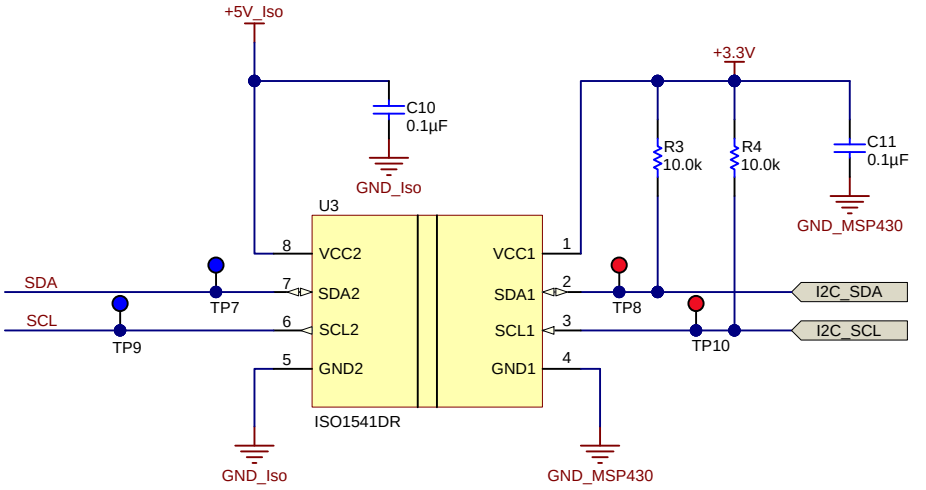


Figure 23. I²C Isolation Schematic

1.5.5 Isolated Gate Driver

Isolation to the high voltage is essential for the IGBT gate drivers. The ISO5852S has the built-in capacitive-isolation barrier with reinforced insulation in accordance with CSA61010-1-12 and IEC61010-1 standards.

One IS5852S drives one IGBT switch. Six devices are required to drive the six IGBTs in the inverter system. Figure 24 shows the gate driver schematic. Add two protection schemes (Schottky diodes D15 and D25 and Zener diodes D16 and D17) to prevent the IGBT gate from being damaged by potential voltage overshot. Use two shunts (J15 and J18) to enable and disable the bipolar junction transistor (BJT) current boost.

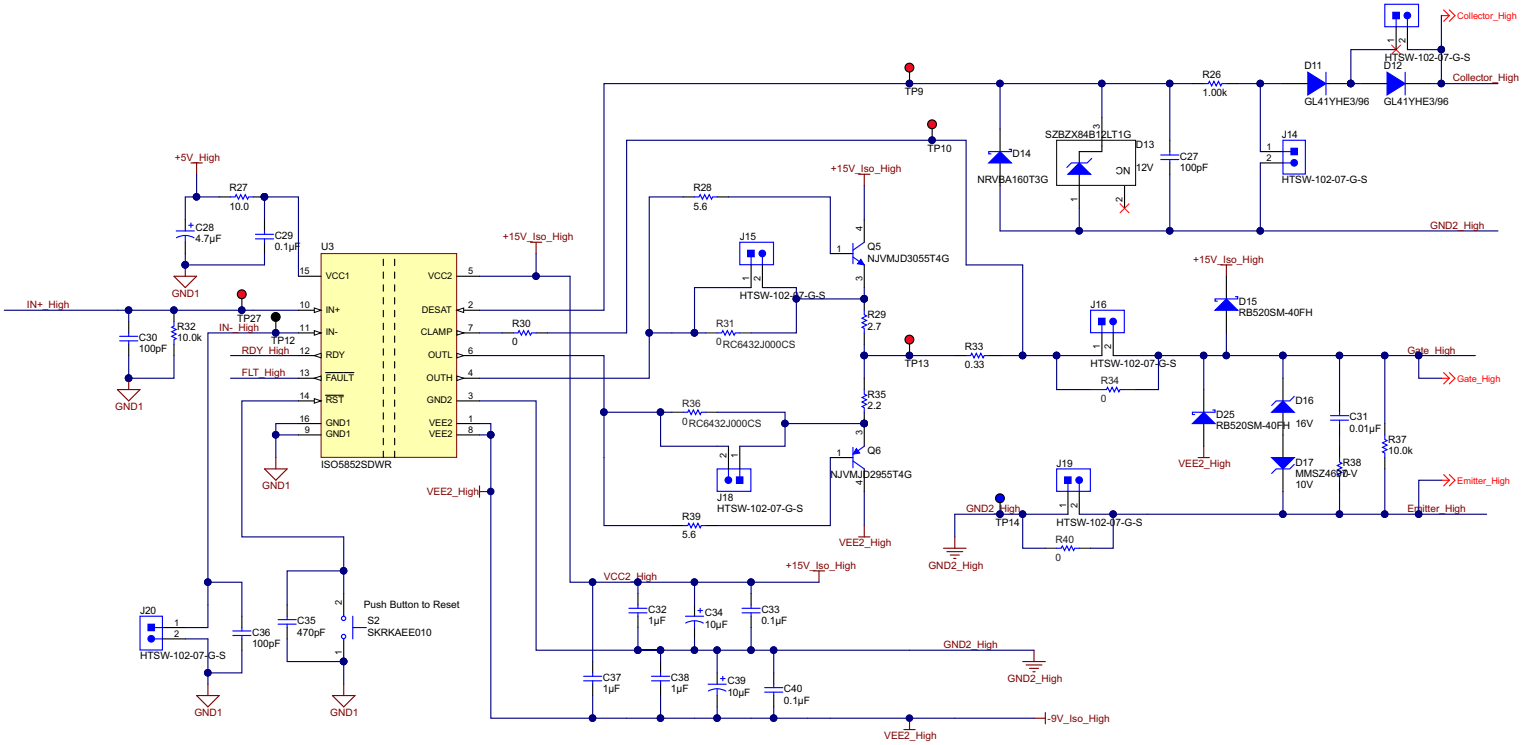


Figure 24. Isolated Gate Driver ISO5852S Schematic

1.5.5.1 Specifications and Features

Power dissipation within the gate driver IC must be controlled below the maximum ratings so the part is not damaged. Table 5 lists the specifications of a single ISO5852S. The maximum secondary side output power limits the maximum switching frequency that the gate driver can operate.

Table 5. ISO5852S Specifications

PARAMETER	SPECIFICATION
Primary side input voltage	5 V ± 5%
Secondary side input voltage	+15 V, –9 V
Gate drive maximum source current capacity I_{PEAK_ON}	2.5-A maximum
Gate drive maximum sink current capacity I_{PEAK_OFF}	5-A maximum
Maximum power dissipation	251 mW at 125°C
Maximum secondary side output power	1 W

The ISO5852S has the desaturation detection technique that is essential to detecting the short-circuit conditions in IGBT. This part of the circuit design is introduced in Section 1.5.5.5.

The ISO5852S contains undervoltage lockout circuitry to prevent insufficient gate drive to the external IGBT and an active-output pulldown feature that ensures the gate-driver output is held low if the output supply voltage is absent.

Because of the Miller effect, the ISO5852S also has an active Miller clamp that can prevent parasitic turnon of the IGBT for unipolar supply operation.

1.5.5.2 Gate Resistors Dimensioning

The ISO5852S delivers the output PWM through OUTH and OUTL separately, allowing independent control of the IGBT turnon and turnoff channels. Turnon and turnoff gate resistors can be added into each channel to adjust the switching speed.

Use Equation 30 and Equation 31 to calculate the minimum turnon and turnoff resistances (R_{GATE_ON} and R_{GATE_OFF}).

$$R_{GATE\_ON} = \frac{\Delta V}{I_{PEAK\_ON}} = \frac{24\ V}{2.5\ A} = 9.6\ \Omega \tag{30}$$

$$R_{GATE\_OFF} = \frac{\Delta V}{I_{PEAK\_OFF}} = \frac{24\ V}{5\ A} = 4.8\ \Omega \tag{31}$$

The ISO5852S has an internal resistance of 4 Ω in the on state and 2.5 Ω in the off state. The FF600R07ME4_B11 IGBT module has an internal resistance of 0.67 Ω. Select externally added R_{ON} = 5.1 Ω and R_{OFF} = 2.2 Ω.

1.5.5.3 Maximum Switching Frequency

The ISO5852S has a maximum allowed, total power dissipation of P_D = 251 mW that limits the maximum switching frequency that drives the IGBT. P_D consists of the total input power (P_{ID}), the total output power (P_{OD}), and the total output power under load (P_{OL}).

Use Equation 32 to calculate P_{ID}.

$$P_{ID} = V_{CC1} \times I_{Q\_PRI} = 5\,V \times 4.5\ mA = 22.5\ mW \tag{32}$$

where

- I_{Q_PRI} is the maximum input supply quiescent current at the ISO5852S primary side
- V_{CC1} is the input voltage at the primary side

Use Equation 33 to calculate P_{OD}.

$$P_{OD} = (V_{CC2} - V_{EE2}) \times I_{Q\_SEC} = (15\ V + 9\ V) \times 6\ mA = 144\ mW \quad (33)$$

where

- I_{Q_SEC} is the maximum input supply quiescent current on the ISO5852S secondary side
- V_{CC2} is the positive power rail applied to the ISO5852S secondary side
- V_{EE2} is the negative power rail applied to the ISO5852S secondary side

Use Equation 34 to calculate the maximum-output dynamic power.

$$P_{OL} = P_D - P_{ID} - P_{OD} = 251\,mW - 22.5\,mW - 144\,mW = 84.5\,mW \quad (34)$$

The maximum switching frequency can be derived from P_{OL}. Use Equation 35 to calculate the maximum switching frequency (F_{SW_MAX}).

$$P_{OL} = 0.5 \times F_{SW\_MAX} \times Q_G \times (V_{CC2} - V_{EE2}) \times \left(\frac{R_{ON\_MAX}}{R_{ON\_MAX} + R_{GATE\_ON}} + \frac{R_{OFF\_MAX}}{R_{OFF\_MAX} + R_{GATE\_OFF}} \right)$$

$$= 0.5 \times F_{SW\_MAX} \times 3.3\ \mu C \times (15\,V + 9\,V) \times \left(\frac{4\,\Omega}{4\,\Omega + 5.1\,\Omega} + \frac{2.5\,\Omega}{2.5\,\Omega + 2.2\,\Omega} \right)$$

$$F_{SW\_MAX} = \frac{84.5\ mW}{38.47 \times 10^{-6}} = 2.2\ kHz \quad (35)$$

where

- Q_G is the gate charge of the IGBT
- R_{ON_MAX} is the worst-case output resistance in the on state
- R_{OFF_MAX} is the worse-case output resistance in the off state
- R_{GATE_ON} is the gate resistance during turnon
- R_{GATE_OFF} is the gate resistance during turnoff

Only using the ISO5852S, the PWM output is limited to F_{SW} = 2.2 kHz. A push-pull current bosst stage that consists of two BJTs is necessary to increase the switching frequency, to decease the power consumption of the ISO5852S, and to boost the sink and source drive current.

1.5.5.4 Push-Pull Current Boost

Users can add two BJTs to increase the drive current. Figure 25 shows the push-pull current boost schematic.

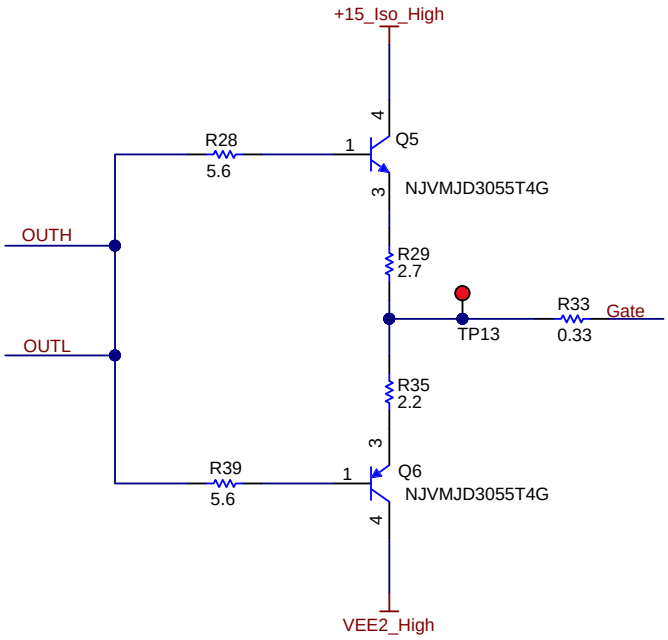


Figure 25. Gate Driver Push-Pull Current Boost Schematic

the push-pull boost enables up to a 10-A source and a 10-A sink peak drive current. The BJTs must withstand the 24-V voltage rating from the IGBT bias power supply. Select the complementary power transistor parts PNP NJVMJD3055T4G and NPN NJVMJD2955T4G (automotive grade) for this design.

Redimension the gate resistances that are in series with the two BJTs to be 2.7 Ω and 2.2 Ω for turnon and turnoff (see Equation 30 and Equation 31). The input capacitance of the IGBT is C_{IES} = 18.5 nF. Use Equation 36 and Equation 37 to calculate the duration of the peak pulse of the gate drive signal for turnon (τ_{ON}) and turnoff (τ_{OFF}).

$$\tau_{ON} = \frac{Q_G}{I_{ON\_PEAK}} = \frac{3.3\,\mu C}{7A} = 0.47\,\mu s \tag{36}$$

$$\tau_{OFF} = \frac{Q_G}{I_{OFF\_PEAK}} = \frac{3.3\,\mu C}{10A} = 0.33\,\mu s \tag{37}$$

where

- I_{ON_PEAK} is the peak current during turnon
- I_{OFF_PEAK} is the peak current during turnoff

Use Equation 38 through Equation 41 to calculate the power rating of the resistors. Consider a PMW drive signal of up to 30-kHz switching frequency. Use Equation 38 and Equation 39 to calculate the peak pulse power that is dissipated in the gate resistor at turnon (R_{ON_PEAK}) and turnoff (R_{OFF_PEAK}).

$$P_{ON\_PEAK} = I_{SOURCE}^2 \times R_{GATE\_ON} = 7^2 \times 2.7\ \Omega = 132.3\ W \tag{38}$$

$$P_{OFF\_PEAK} = I_{SIN\_K}^2 \times R_{GATE\_ON} = 10^2 \times 2.2\ \Omega = 220\ W \tag{39}$$

Use Equation 40 and Equation 41 to calculate the average power dissipations in the gate resistor for turnon (P_{ON_AVG}) and turnoff (P_{OFF_AVG}).

$$P_{ON\_AVG} = P_{ON\_PEAK} \times D_{DUTY\_CYCLE} = P_{ON\_PEAK} \times \frac{\tau_{ON}}{T}$$
$$= 132.3 \times 0.47\,\mu s \times 30\,kHz = 1.87\,W \quad (40)$$

$$P_{OFF\_AVG} = P_{OFF\_PEAK} \times D_{DUTY\_CYCLE} = P_{OFF\_PEAK} \times \frac{\tau_{OFF}}{T}$$
$$= 220 \times 0.33\,\mu s \times 30\,kHz = 2.18\,W \quad (41)$$

where

- D_{DUTY_CYCLE} is the PWM duty cycle
- T is the PWM switching period

Choose 3-W resistors with 1210 packages.

use Equation 42 and Equation 43 to calculate the minimum required resistance connected to the BJT base for turnon (R_{BASE_ON}) and turnoff (R_{BASE_OFF}).

$$R_{BASE\_ON} = \frac{V_{CC2} - V_{EE2} - V_{BE}}{I_{BASE\_ON}} - R_{GATE\_ON} - R_{ON\_MAX}$$
$$= \frac{15\,V + 9\,V - 0.7\,V}{2.5\,A} - 2.7\,\Omega - 4\,\Omega = 2.62\,\Omega \quad (42)$$

$$R_{BASE\_OFF} = \frac{V_{CC2} - V_{EE2} - V_{BE}}{I_{BASE\_OFF}} - R_{GATE\_OFF} - R_{OFF\_MAX}$$
$$= \frac{15\,V + 9\,V - 0.7\,V}{5\,A} - 2.2\,\Omega - 2.5\,\Omega = 0.04\,\Omega \quad (43)$$

where

- V_{BE} is the voltage drop across the base-to-emitter junction of the BJT
- I_{BASE_ON} is the maximum base current that can be applied to the BJT during turnon
- I_{BASE_OFF} is the maximum base current that can be applied to the BJT during turnoff

Equation 42 shows that the minimum base resistance of the high-side BJT is 2.62 Ω, and any resistance can be applied at the base of the low-side BJT. Two 5.6-Ω resistors (R28 and R36) are applied for both sides.

Use Equation 44 to calculate the average base current (I_{BASE}) to drive the BJTs.

$$I_{BASE} = \frac{I_C}{\beta} \quad (44)$$

where

- I_C is the collector current flowing through BJT while driving the IGBT
- β is the minimum DC current gain of the BJT

Use Equation 45 to reduce the dynamic output power fo the ISO5852S (P_{OL_REQ}).

$$P_{OL\_REQ} = \frac{1}{2} \times \frac{1}{\beta^2} \times (P_{ON\_AVG} + P_{OFF\_AVG}) = \frac{1}{2} \times \frac{1}{5^2} \times (1.87\,W + 2.18\,W) = 81\,mW \quad (45)$$

As the result, the required output power is reduced as the maximum of POL = 84.5mW, the 30 kHz switching frequency is suitable for this application.

1.5.5.5 Desaturation Detection Circuit

The DESAT fault protection prevents IGBT destruction that results from excessive currents during a short-circuit fault. When a short-circuit faults occurs the ISO5852S turns off the IGBT with a soft turnoff procedure that lasts 2 µs; this avoids the voltage overshoot between the IGBT collector and emitter. The PWM output slowly decreases and is clamped to the voltage of VEE2 when the voltage of the OUTL pin reaches 2 V with respect to VEE2. Section 3.5.6, Figure 90 shows the waveform of this feature.

Figure 26 shows the schematic of the desaturation detection circuit. DESAT diodes D11 and D12 conduct forward currents, allowing sensing of the saturated collector to emitter voltage of the IGBT when the IGBT is on. Diodes D11 and D12 block the high voltage when the IGBT is in the off state. Large forward voltage transients across the freewheeling diodes of the IGBTs can be generated while switching inductive loads. These large transients result in large negative voltage spikes on the DESAT pin, drawing substantial current out of the device. Resistor R26 limits the current flowing into the DESAT pin. A Schottky diode (D14) assures the DESAT pin input voltage to GND potential at low voltage levels.

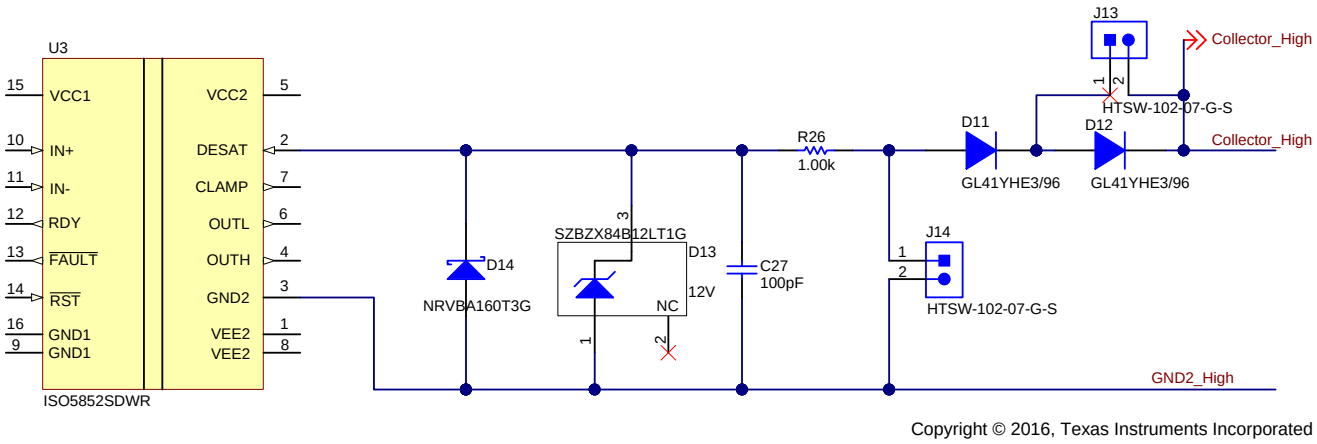


Figure 26. Desaturation Detection Current Schematic

The IGBT collector-to-emitter voltage that is fed into the DESAT pin is compared with the 9-V DESAT threshold internally. The sum of the forward voltage of the DESAT and the IGBT collector-emitter voltage compose the voltage at the DESAT pin. The IGBT collector-to-emitter voltage can be modified by adding multiple DESAT diodes in series when a fault condition (V_{CE_FAULT}) is triggered. Use Equation 46 to calculate the collector-to-emitter voltage modification.

$$V_{CE\_FAULT} = 9V - n \times V_F \tag{46}$$

where

- V_{CE_FAULT} is the voltage across the collector and emitter of the IGBT when the DESAT fault triggers
- n is the number of DESAT diodes in series
- V_F is the forward voltage across the DESAT diode

After the IGBT is turned on, the DESAT faults detection requires a blanking time to allow the IGBT collector-to-emitter voltage to drop below the 9-V threshold. The 500-µA internal-current source, 9-V DESAT voltage threshold, and the external blanking capacitor (C27 in Figure 26) control the DESAT blanking time (t_B). Use Equation 47 to calculate t_B.

$$t_B = \frac{V_{CE\_TH} \times C_{DESAT}}{500\,\mu A} = \frac{9V \times 100\,pF}{500\,\mu A} = 1.8\,\mu s \tag{47}$$

where

- V_{CE_TH} is the DESAT voltage threshold
- C_{DESAT} is the blanking capacitor

1.5.5.6 Active Miller Clamp

The collector current flows through the Miller capacitor and raises the gate voltage during the switching transient of the high-side IGBT; in this case, the low-side IGBT could faultily turn on. This risk increases when the ratio (reverse-transfer capacitance to input capacitance) increases.

The ISO5852S mitigates the chance of the low-side IGBT faultily turning on with the embedded active Miller-clamp feature. Connecting the IGBT gate to the CLAMP pin provides a low-impedance path to ground that prevents the IGBT from a fault turnon and suppresses the voltage spikes that get coupled into the IGBT gate.

The CLAMP transistor turns on when OUTL reaches 2 V with respect to VEE2 when the IGBT is turning off. The active Miller clamp is important for IGBTs that have a low reverse-transfer capacitance (C_{RES}) and do not require negative voltage to turn off. Section 3.5.5 shows experimental results of this feature.

1.5.6 Thermal Calculation in IGBT

Thermal management ensures the IGBT switching and dynamic performance and is essential to the IGBT system design because overheating occurs when excessive losses are generated in the IGBT.

It is essential to evaluate the switching behavior of the IGBT because the IGBT module data sheets characterize the switching behavior under specific conditions. Use data sheet parameters for estimation.

1.5.6.1 Losses in IGBT

IGBT and semiconductor power losses can be divided into the following three groups:

- Switching losses
- Condition losses
- Leakage losses when the IGBT is off (this amount is usually negligible)

The IGBTs operate under the following conditions:

- V_{CE} = 400 V
- I_{CE} = 20 A
- F_{SW} = 30-kHz maximum

The rise time (t_{ON}) is 1.22 µs and the fall time (t_{OFF}) is 1 µs. Use Equation 48 to calculate the losses of the IGBT.

$$P_{SW\_LOSS} = \frac{1}{2} \times V_{CE} \times I_{CE} \times (t_{ON} + t_{OFF}) \times F_{SW}$$
$$= \frac{1}{2} \times 400\,V \times 20\,A \times (1.22\,\mu s + 1\mu s) \times 30\,kHz = 266.4\,W \quad (48)$$

where

- V_{CE} is the collector-to-emitter voltage
- I_{CE} is the collector-to-emitter current
- t_{ON} is the rise time of the collector-to-emitter voltage
- t_{OFF} is the fall time of the collector-to-emitter voltage

Use Equation 49 to calculate the conduction losses of the IGBT (P_{CON_LOSS}).

$$P_{COND\_LOSS} = V_{SAT} \times I_{CE} \times R_{DS\_ON\_AVG}$$
$$= 1.75\,V \times 20\,A \times 0.1 = 3.5\,W \quad (49)$$

where

- V_{SAT} is the collect-emitter saturation voltage
- $R_{DS\_ON\_AVG}$ is the average channel resistance

The switching losses are dominant.

1.5.6.2 Power Dissipation in Load Resistor

Figure 27 shows how the load resistor is connected to the IGBT bridge. The IGBT at the high side is always clamped off and the IGBT at the low side switches on and off when the system is operating. The 400-V DC voltage is applied across the load resistor during the switching-on period of the low-side IGBT.

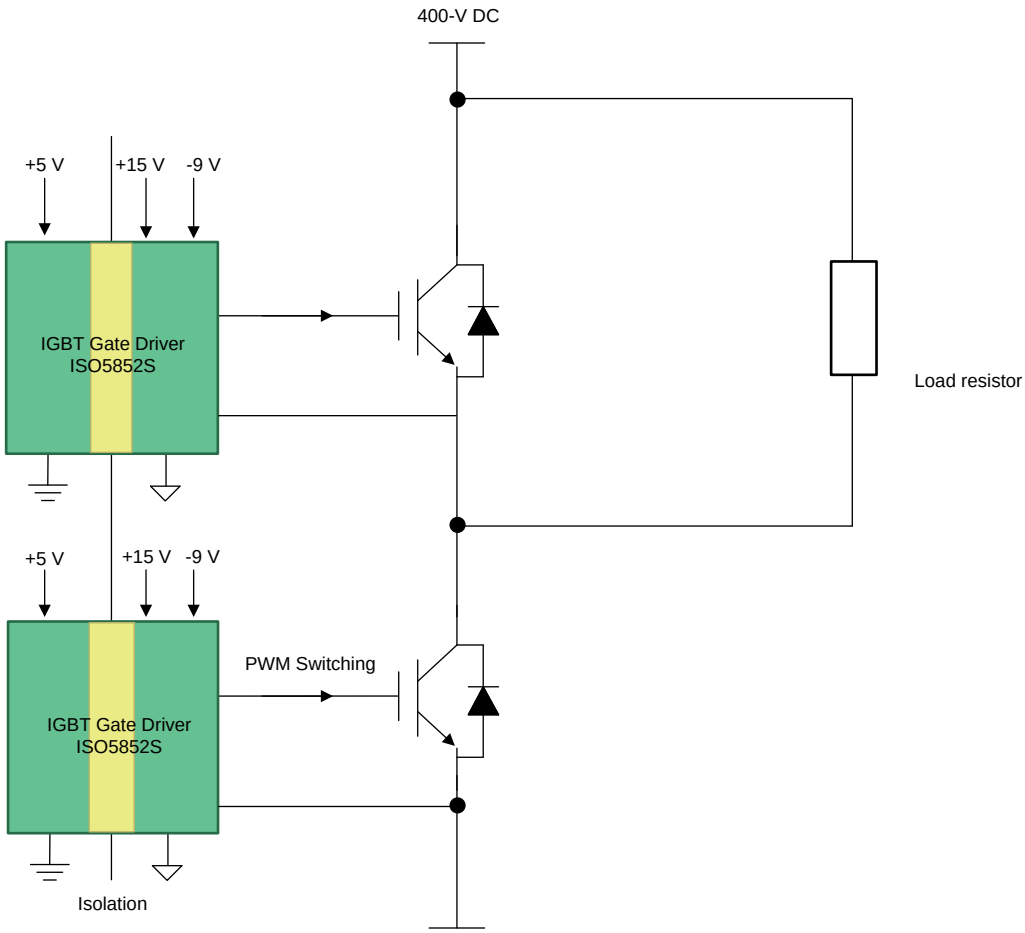


Figure 27. Load Resistor Connection

Use Equation 50 to calculate the peak current (I_{PEAK}) on the load.

$$I_{PEAK} = V_{DC} \div R_{LOAD} = 400\ V \div 22\ \Omega = 18.2\ A \quad (50)$$

Use Equation 51 to calculate the maximum power dissipation on the load resistor (P_{LOAD}).

$$P_{LOAD} = V_{DC} \times I_{CE} \times D_{DUTY\_CYCLE} = 300\,W \quad (51)$$

where

- V_{DC} is the voltage applied on the DC bus

P_{LOAD} limits the duty cycle. Consider an 8% duty cycle and use Equation 52 to calculate the average load current (I_{AVG}).

$$I_{AVG} = I_{PEAK} \times D_{DUTY\_CYCLE} = 18.2\,A \times 8\% = 1.456A \quad (52)$$

Use Equation 53 to calculate the RMS value of the load current.

$$I_{RMS} - I_{PEAK} \times \sqrt{D_{DUTY\_CYCLE}} = 18.2\,A \times \sqrt{8\%} = 5.14\,A \quad (53)$$

Use Equation 54 to calculate the power consumption that the load is operating under.

$$P_{HV} = I_{RMS}^{2} \times R_{LOAD} = 5.14A \times 5.14A \times 22\Omega = 581W \quad (54)$$

where

- R_{LOAD} is the load resistance

Use Equation 55 to calculate the losses in the reverse-polarity protection diode (D1 in Figure 13).

$$P_D = I_{RMS} \times V_F = 5.14\,A \times 1.65\,V = 8.5\,W \quad (55)$$

where

- V_F is the diode forward voltage onto the DC link

2 Getting Started Hardware

2.1 Hardware

Figure 28 shows the image of the IGBT gate driver board and the arrangement of the components. The IGBT gate driver and bias power-supply components are arranged for high-side and low-side symmetry. Keep isolations to the high voltages clean and free from any trace, pad, and via on the printed-circuit board (PCB).

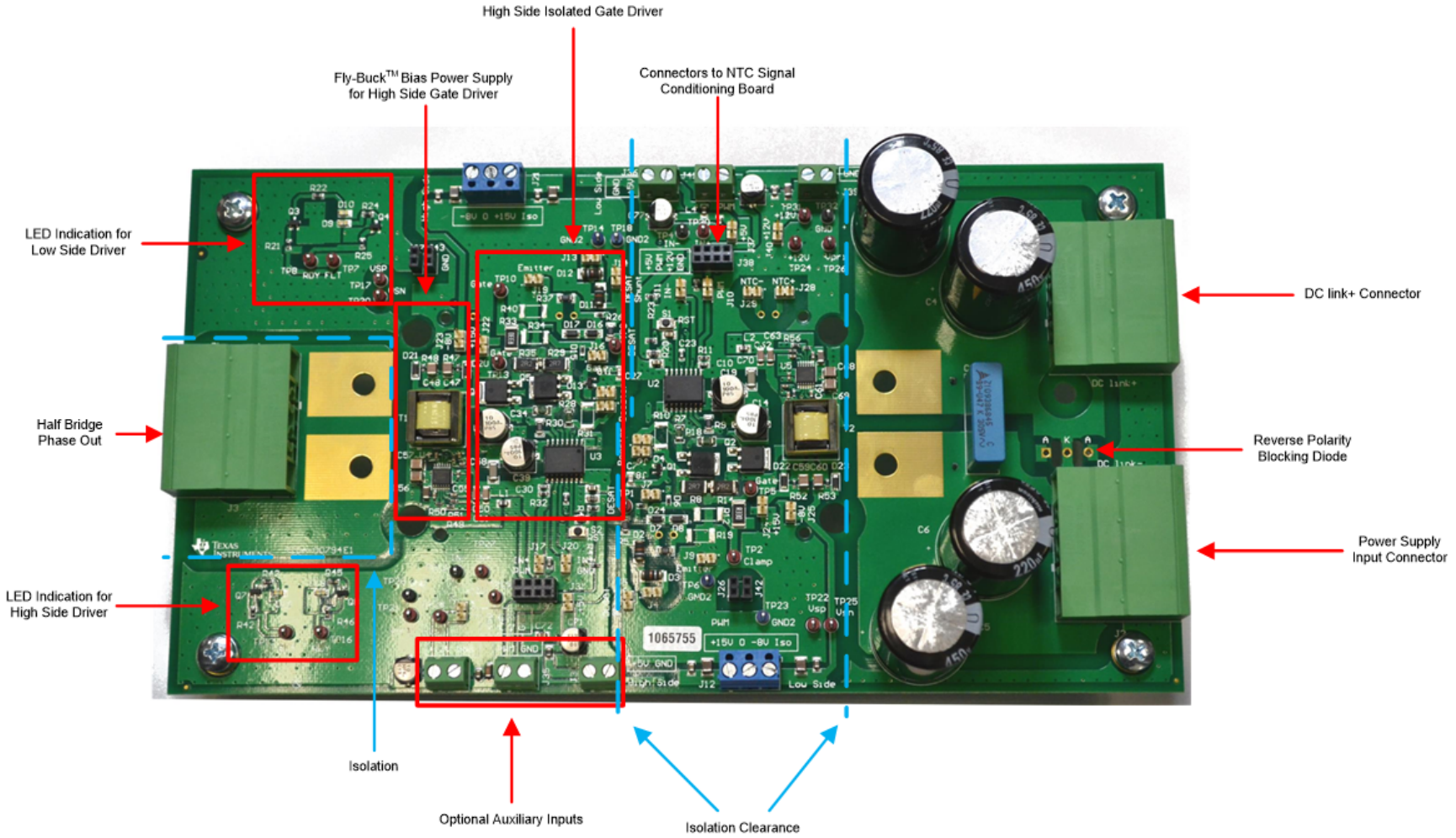


Figure 28. PCB of IGBT Gate Driver Board

Figure 29 shows the image of the NTC signal-conditioning board and the arrangement of the components. Optional input-terminal blocks for isolated and nonisolated +5-V power supplies are added in this design. Keep isolations to the high voltages clean and free from any trace, pad, and via on the PCB.

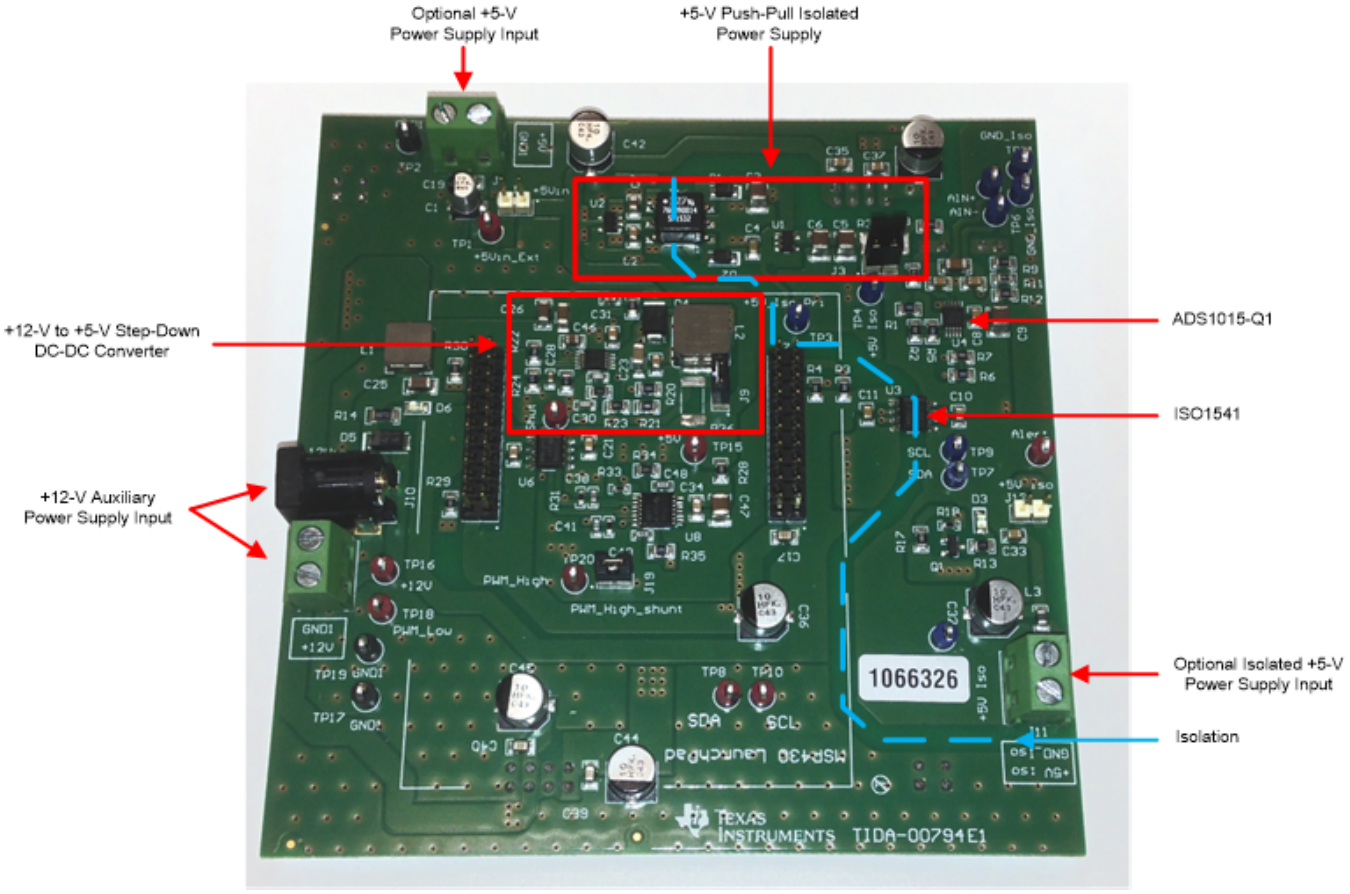


Figure 29. PCB of NTC Signal-Conditioning Board

Figure 30 shows the placement of the IGBT module (between the IGBT board and the heat sink).

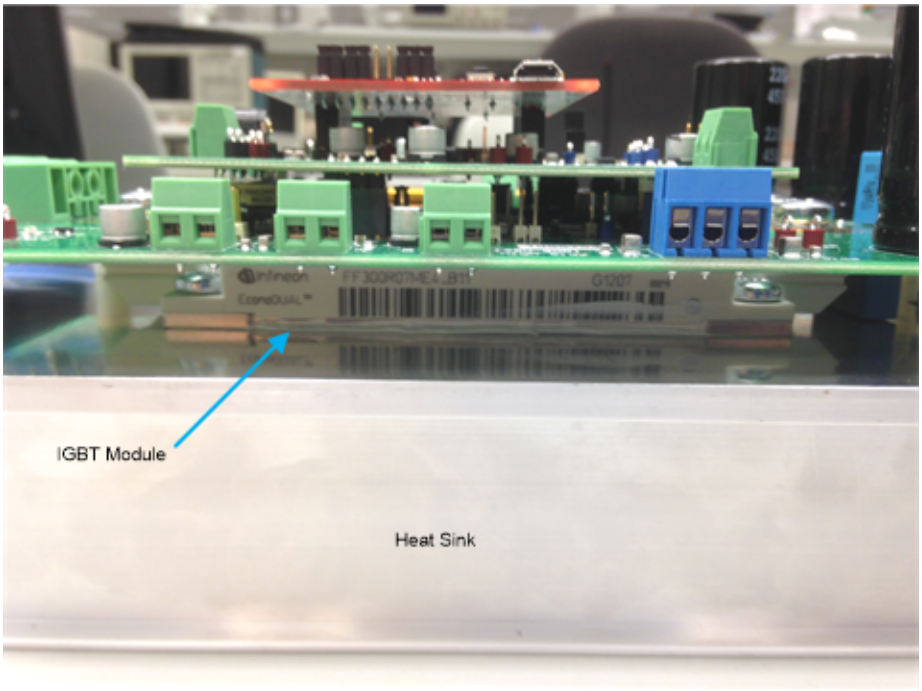


Figure 30. Placement of IGBT Module

Figure 31 shows the power connectors for the power-supply input and the phase output of the IGBT module. The primary power supply must be connected to DC link+ and DC link–.

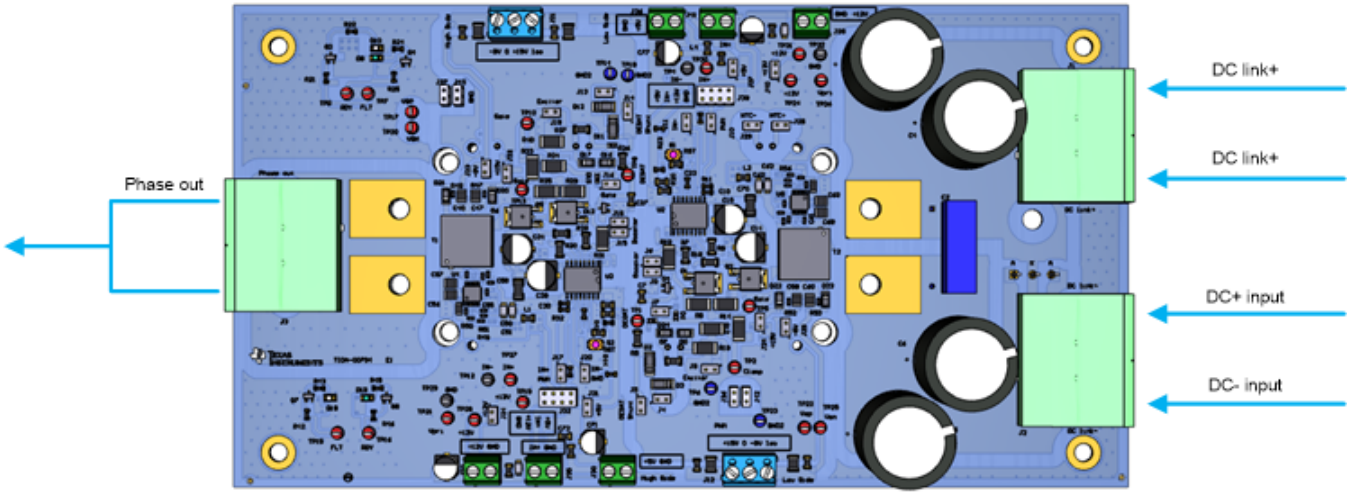


Figure 31. Power Connectors for DC Link

Figure 32 shows the assembled TIDA-00794 system. The following list shows the sequence of board placement from bottom to top.

1. Heat sink
2. IGBT module
3. IGBT gate driver board
4. NTC signal-conditioning board
5. MSP430 LaunchPad

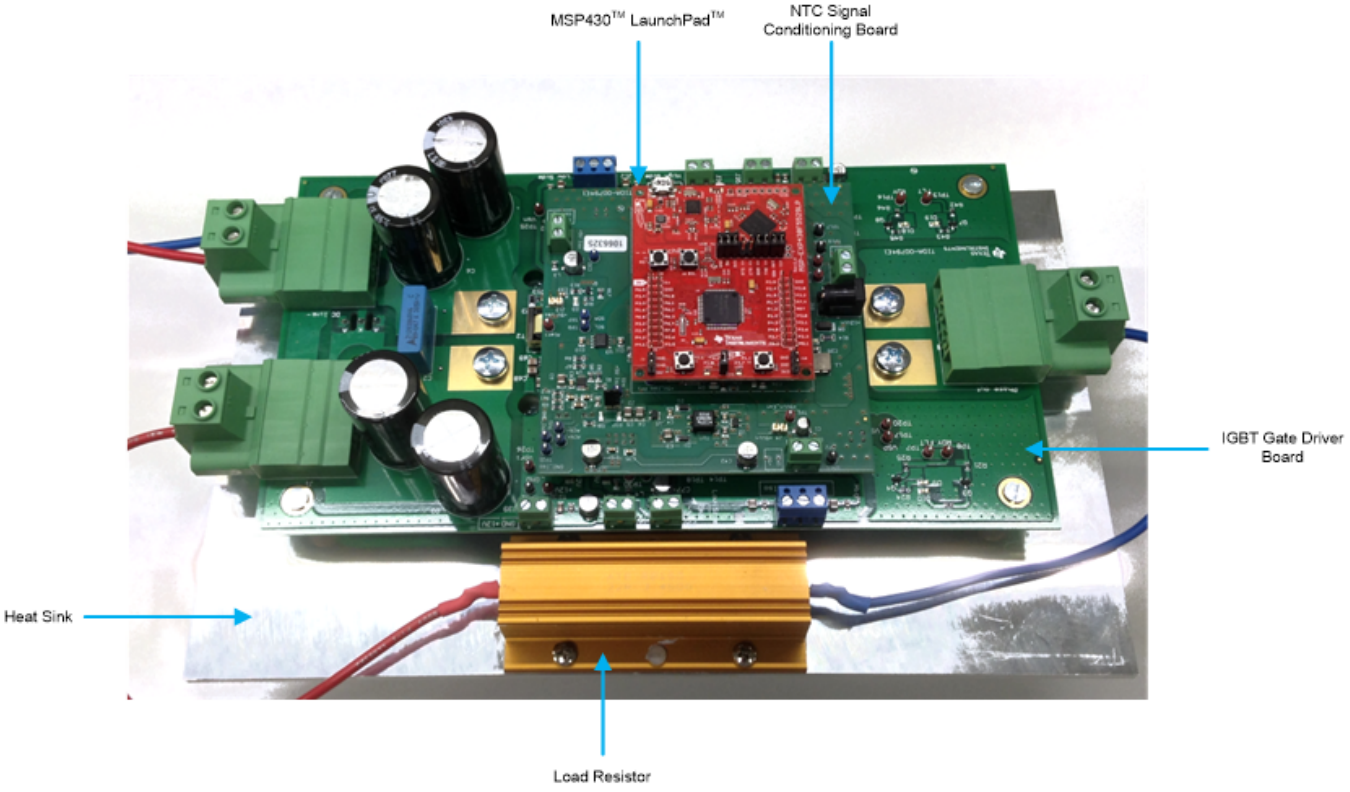


Figure 32. TIDA-00794 System

3 Testing and Results

3.1 System Test Setup

Figure 33 shows the system test setup. For this design, 400-V DC is applied across DC link+ and DC link–. The IGBT gate driver board generates the PWM signals that drive the IGBT module. The NTC signal-conditioning board processes the excited signal from the NTC thermistor.

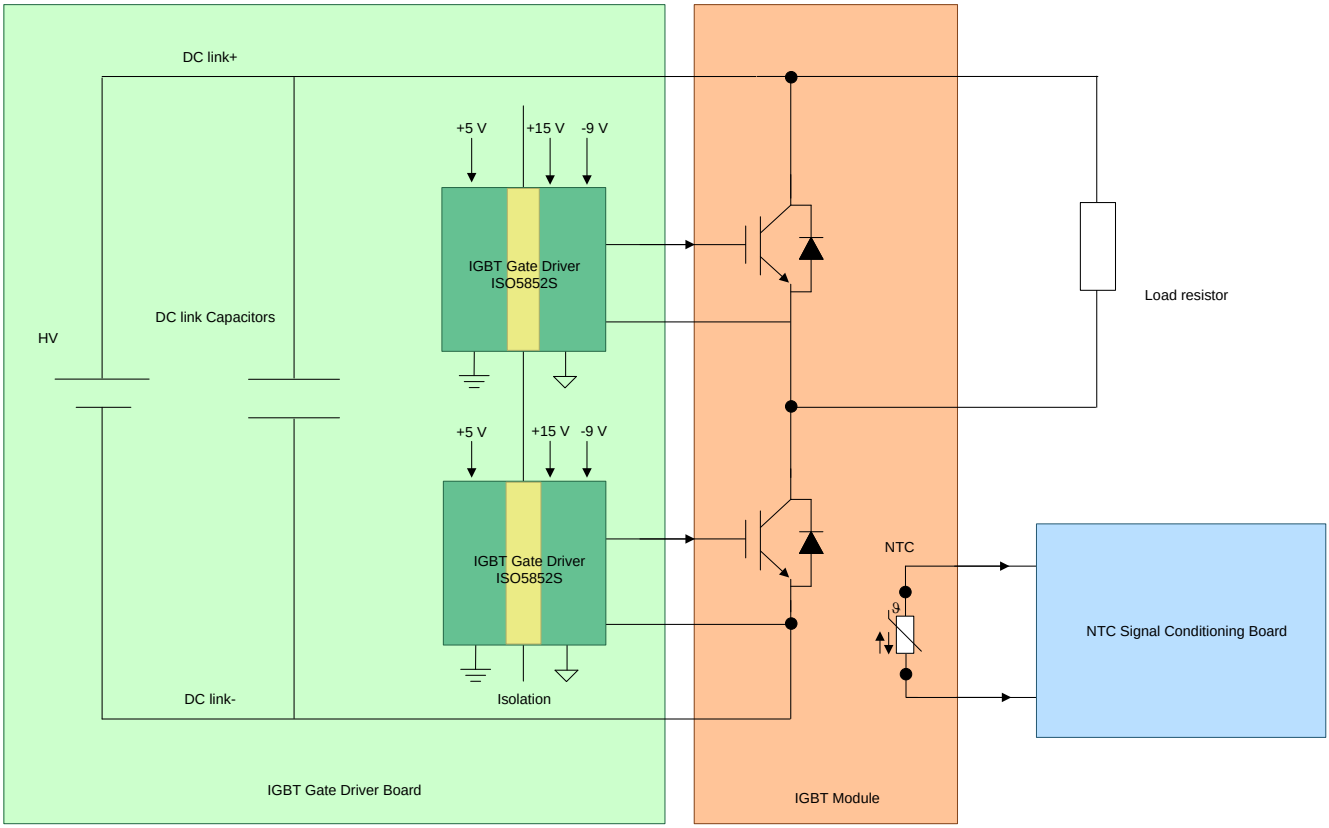


Figure 33. Block Diagram of System Test Setup

Figure 34 shows the wire diagram of the test setup. The MSP430 LaunchPad sends the PWM signal that controls the gate driver. Place gate drivers on top of the IGBT module. The IGBT module consists of two IGBTs in a half-bridge configuration. The auxiliary power supply provides +12 V to the power-management circuitry board.

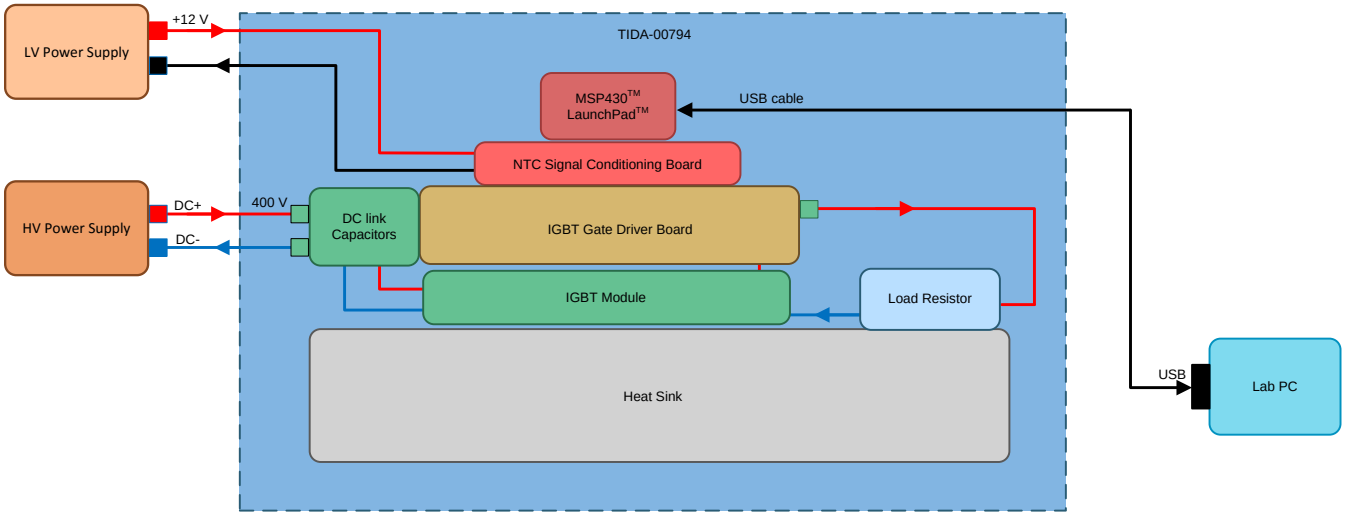


Figure 34. Wiring Diagram of Test Setup

Use twisted-cable pairs for all connections to reduce parasitic-inductive coupling. Place the entire system in into a safety box for protection.

3.2 Isolated Fly-Buck DC-DC Converter

This subsection shows the waveforms in the isolated Fly-Buck DC-DC converter that provide bias power to the secondary side of the IGBT gate driver. Figure 35 shows the test circuit of the LM5160-Q1 Fly-Buck converter.

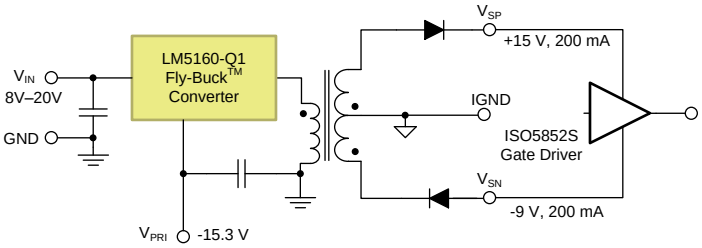


Figure 35. Test Circuit of LM5160-Q1 Fly-Buck™ Converter

3.2.1 Startup Waveforms

Figure 36 and Figure 37 show the startup waveforms of the +15-V rail and the –9-V rail.

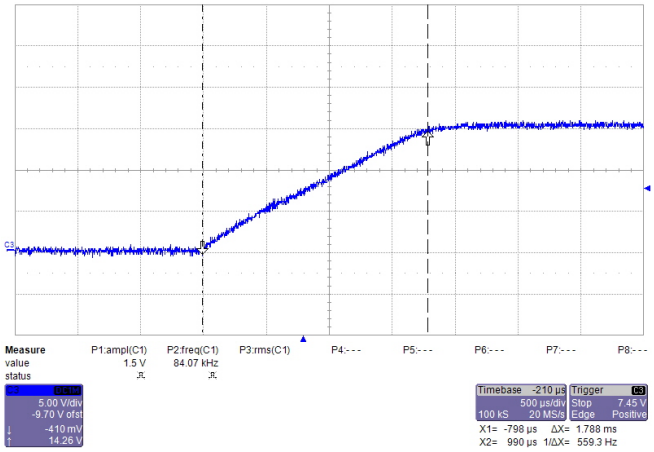


Figure 36. +15-V Rail During Startup

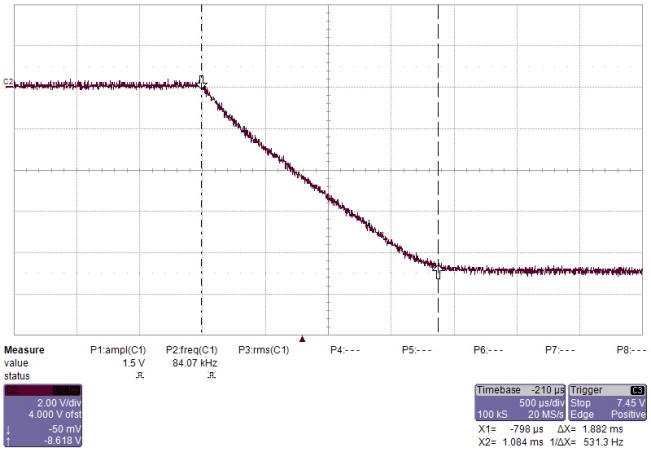


Figure 37. –9-V Rail During Startup

3.2.2 Switching-Node Waveforms

Figure 38 and Figure 39 show the voltage waveforms at the switching node of the LM5160-Q1 with no load and with full load (200 mA).

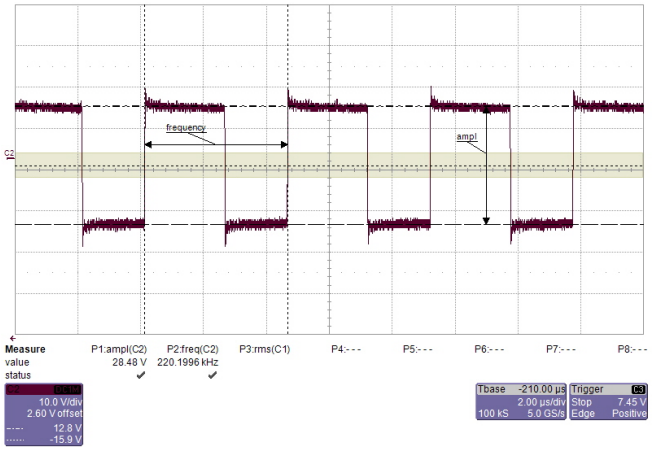


Figure 38. Voltage Waveforms at LM5160-Q1 Switch Node With No Load

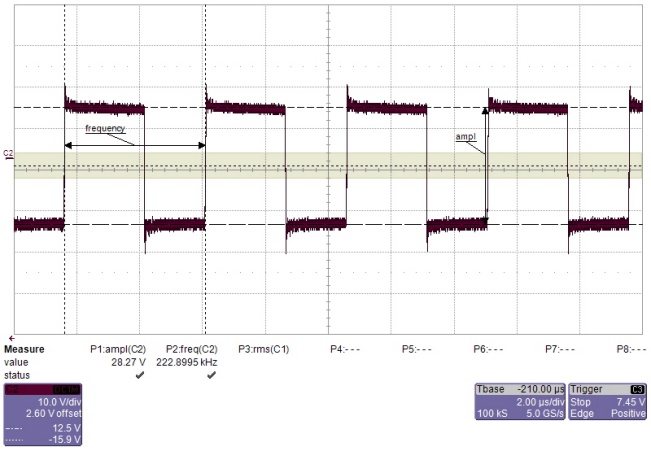


Figure 39. Voltage Waveforms at LM5160-Q1 Switch Node With Full Load

3.2.3 Output-Voltage Waveforms

Figure 40 and Figure 41 shows the output-voltage ripples of the +15-V rail with no load and with full load (200 mA). The peak ripple of the +15-V rail is 49.6 mV.

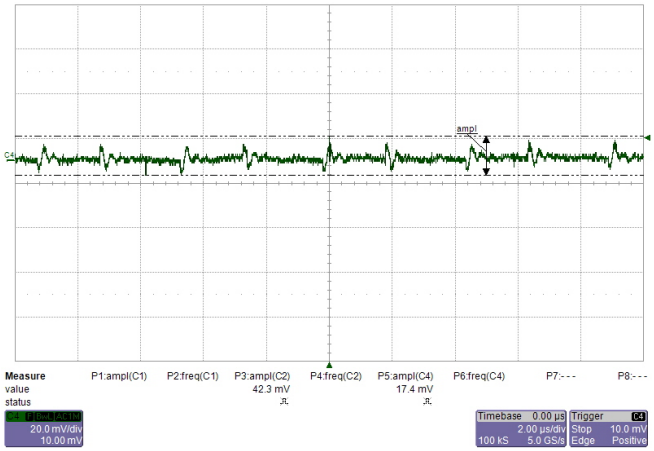


Figure 40. +15-V Rail Output Ripple With No Load

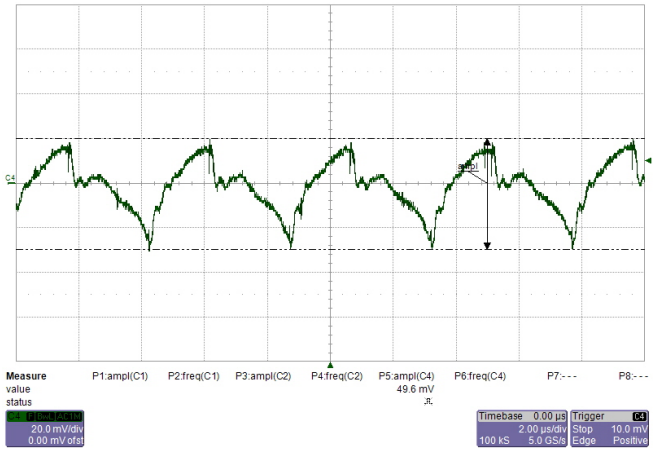


Figure 41. +15-V Rail Output Ripple With Full Load

Figure 42 and Figure 43 shows the output-voltage ripples of the –9-V rail with no load and with full load (200 mA). The peak ripple of the –9-V rail is 32.3 mV.

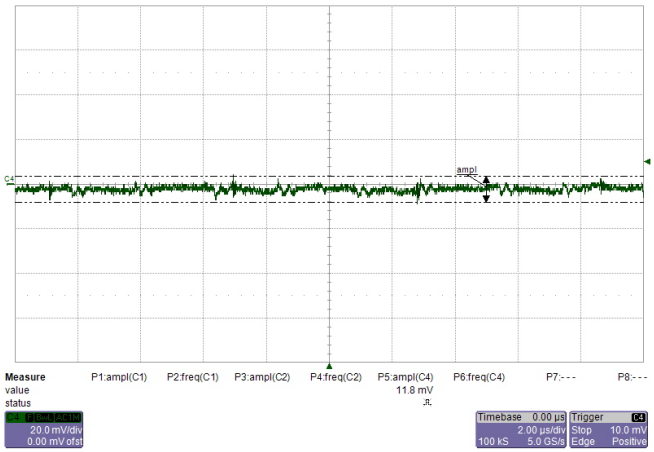


Figure 42. –9-V Rail Output Ripple With No Load

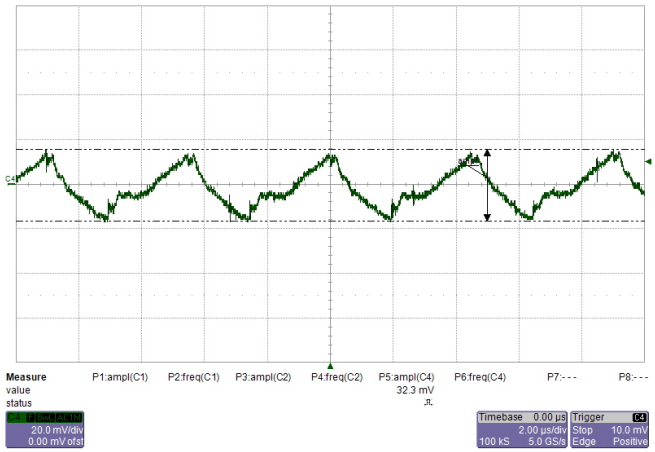


Figure 43. –9-V Rail Output Ripple With Full Load

3.2.4 Ripple at 2.5-A Source and 5-A Sink Current

Figure 44 shows the +15-V output ripples at the transition of delivering the 2.5-A source current.

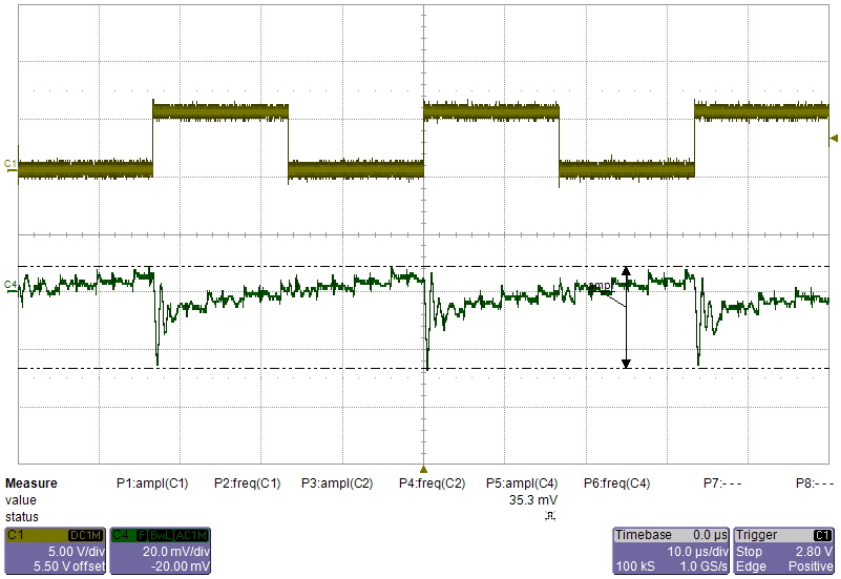


Figure 44. +15-V Output Ripple at Transition of 2.5-A Source Current

Figure 45 shows the –9-V output ripple at the transition of delivering the 2.5-A source current.

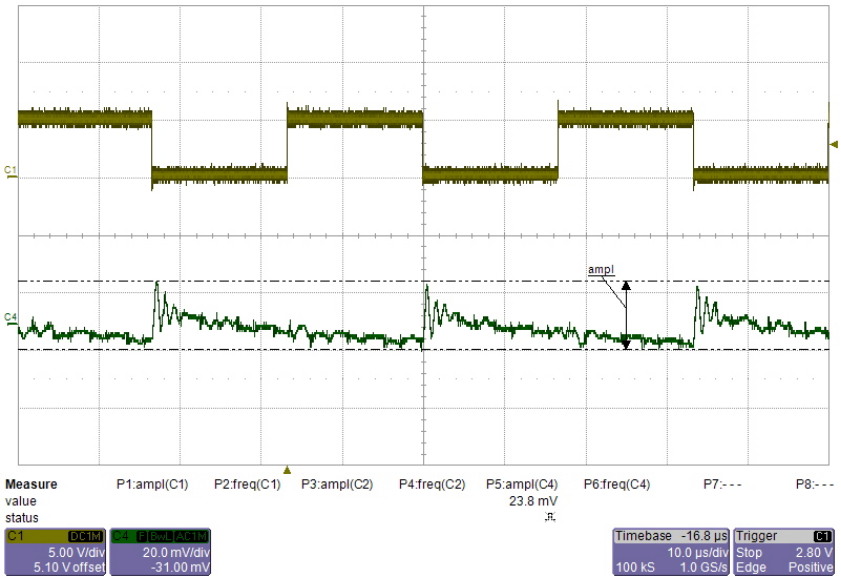


Figure 45. –9-V Output Ripple at Transition of 5-A Source Current

3.2.5 Ripple With BJT Current Boost

The Fly-Buck converter output ripples are measured after the push-pull current boost stage is added. The differential voltage across the 0.33-Ω sensing resistor is measured as a representation of the driving current. Place a 10-nF capacitor across the gate-emitter as the load. Figure 46 shows the measurement points from the schematic. Equation 56 shows what the 1V/div on the oscilloscope represents.

$$I_{GATE} = \frac{1V}{0.33\Omega} = 3A \tag{56}$$

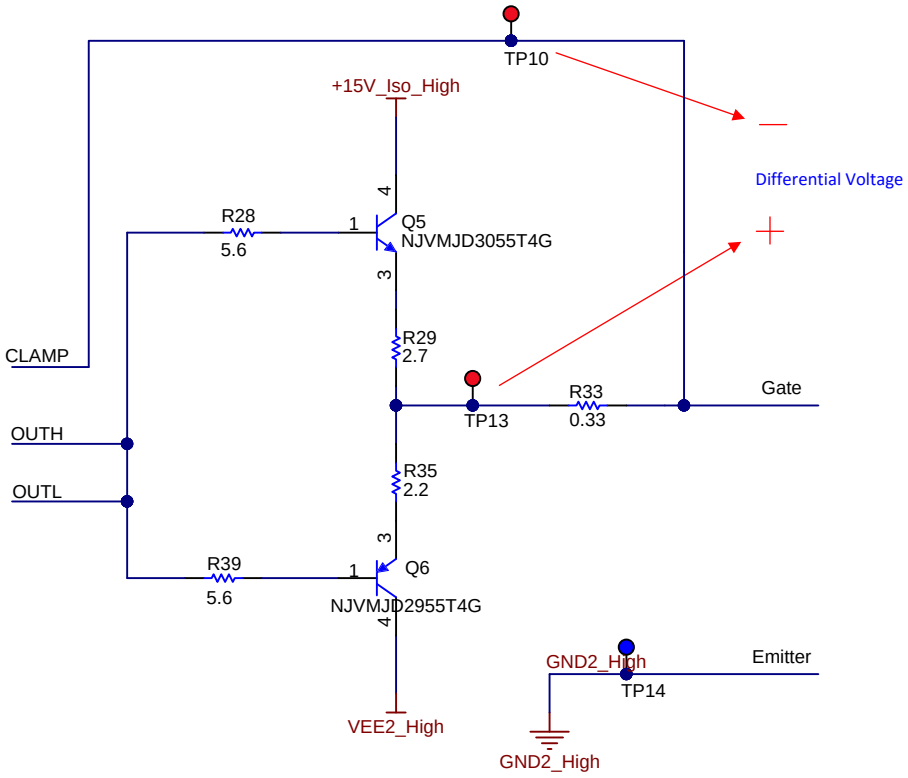


Figure 46. Measurement Points of Source and Sink Currents From Current Boost

Figure 47 shows the +15-V output ripple with the current-boost stage. The peak source current is 1.85 A.

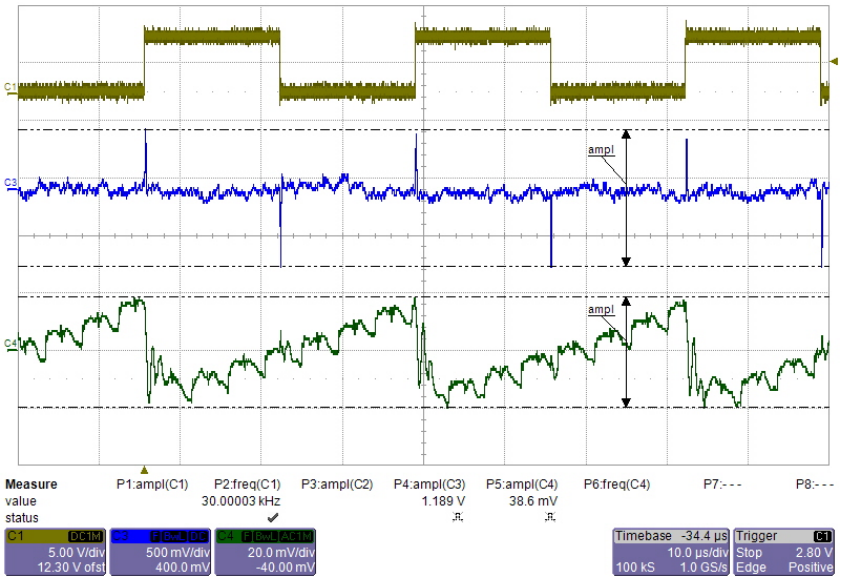


Figure 47. +15-V Output Ripple With BJT Current Boost

Figure 48 shows the –9-V output ripples with the current-boost stage. The sinking peak current is 2.34 A.

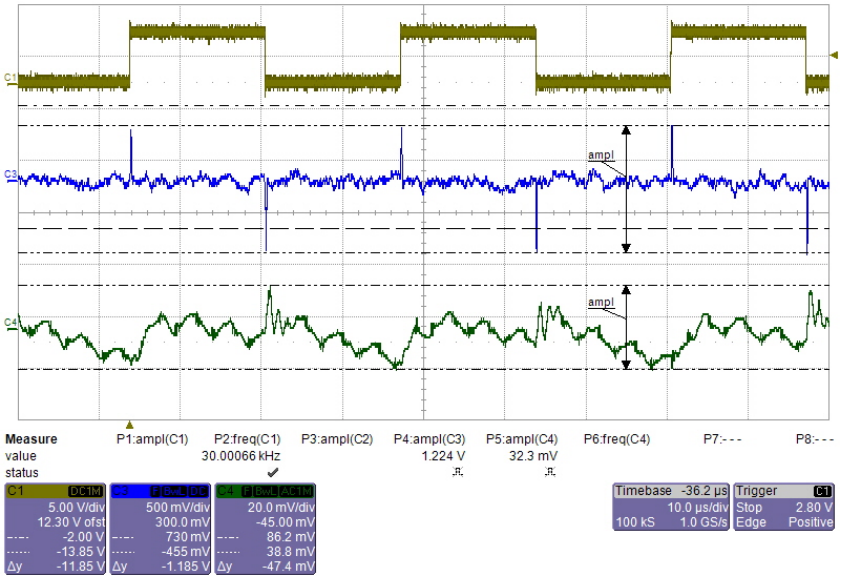


Figure 48. –9-V Output Ripple With BJT Current Boost

3.3 12-V to 5-V Step-Down DC-DC Converter

This section shows test results from the 12-V to 5-V buck converter based on the TPS57140-Q1. Figure 49 shows the diagram of the implemented step-down converter.

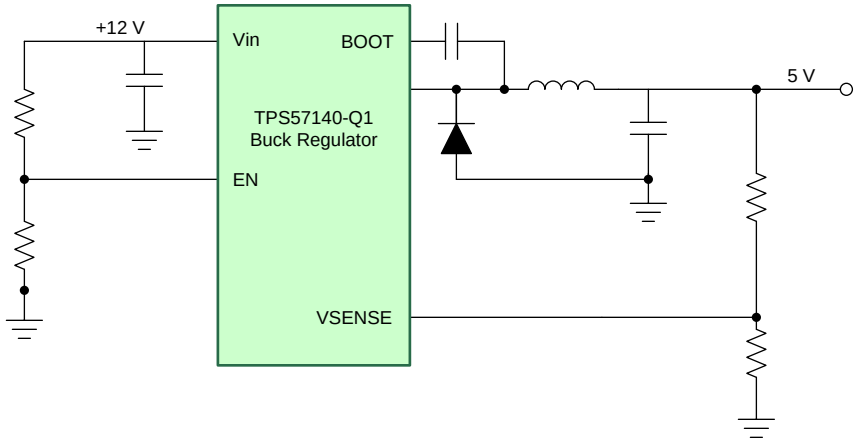


Figure 49. TPS57140-Q1 Step-Down Converter

3.3.1 Startup Waveform

Figure 50 shows the startup waveform of the +5-V rail. the soft start time is 9.3 ms.

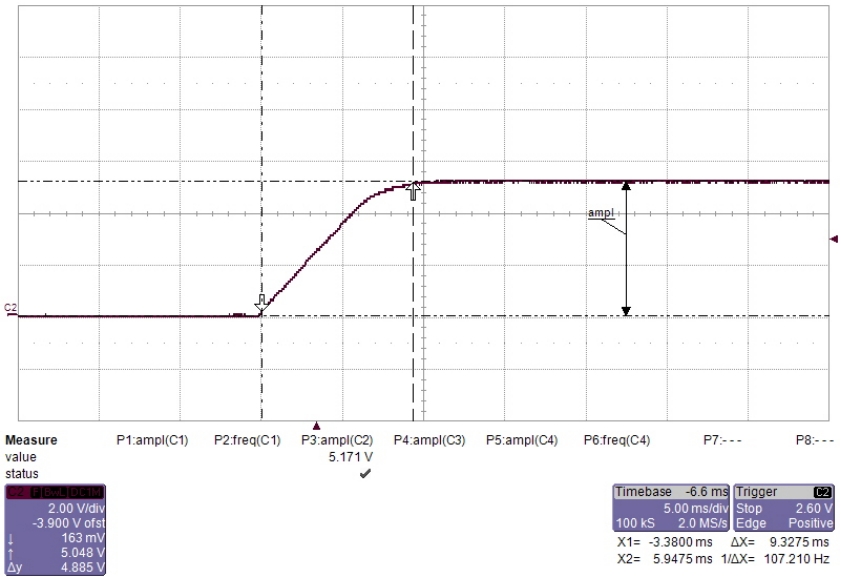


Figure 50. Startup Waveform of Step-Down Converter

3.3.2 Output-Voltage Waveform

Figure 51 and Figure 52 show the output ripple of the step-down DC-DC converter with no load and with full load. The ripple is 58.5 mV.

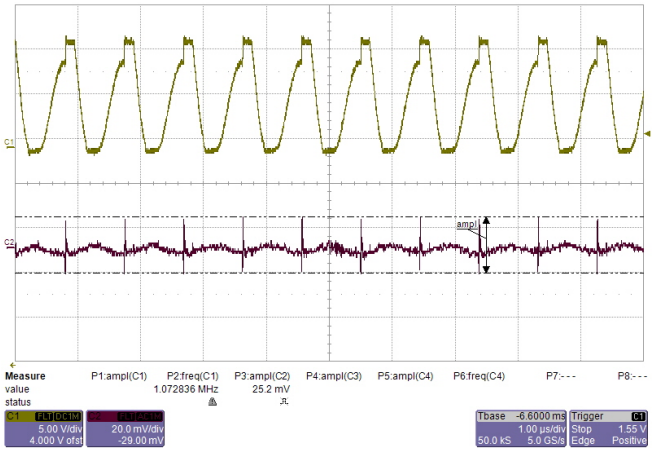


Figure 51. +5-V Output Ripple With No Load

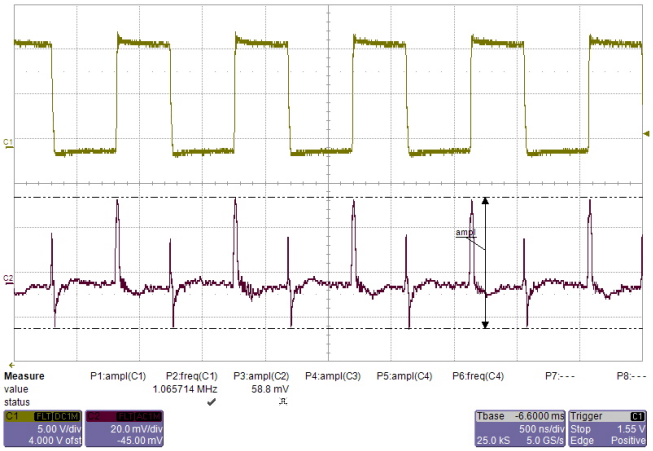


Figure 52. +5-V Output Ripple With Full Load (1 A)

3.3.3 Load Dump Test

Figure 53 and Figure 54 show the +5-V output waveforms during a 1-A step-up and step-down test. The undershot is 23.6 mV and the overshot is 51 mV.

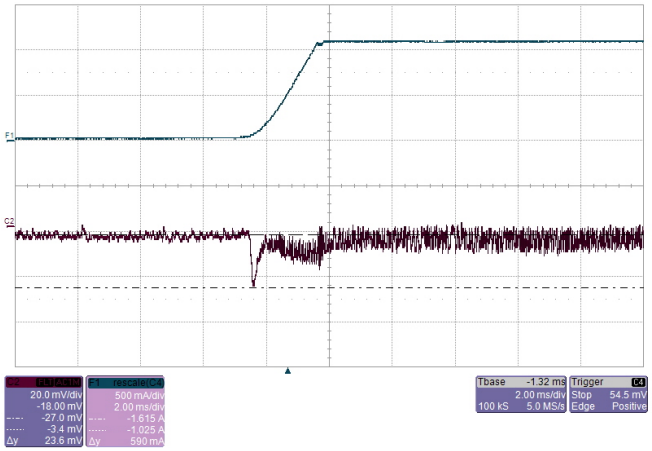


Figure 53. +5-V Load Dump During Load Step-Up

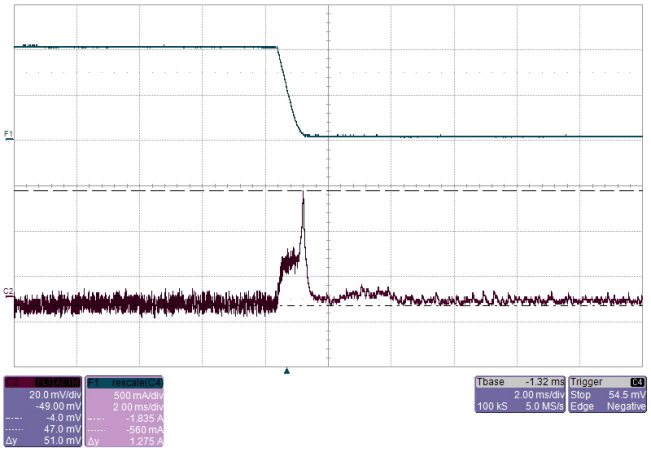


Figure 54. +5-V Load Dump During Load Step-Down

3.4 NTC Signal Conditioning

This section shows the measured waveforms in the signal conditioning circuit of the NTC thermistor.

3.4.1 Isolated Push-Pull Power Supply

Figure 55 shows a diagram of the +5-V isolated push-pull power supply.

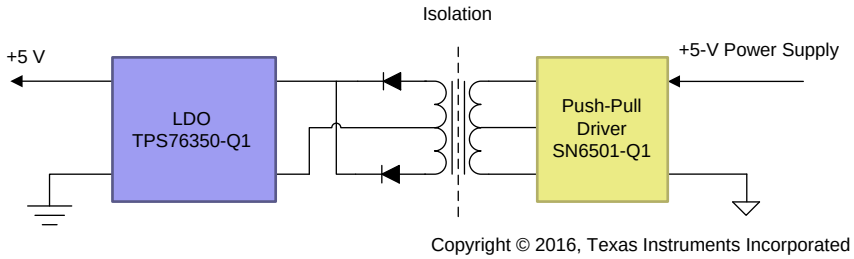


Figure 55. Diagram of Push-Pull Isolated Power Supply

Figure 56 and Figure 57 show the output voltage versus the ripples at the output of the secondary side of the transformer at no load and at full load (150 mA).

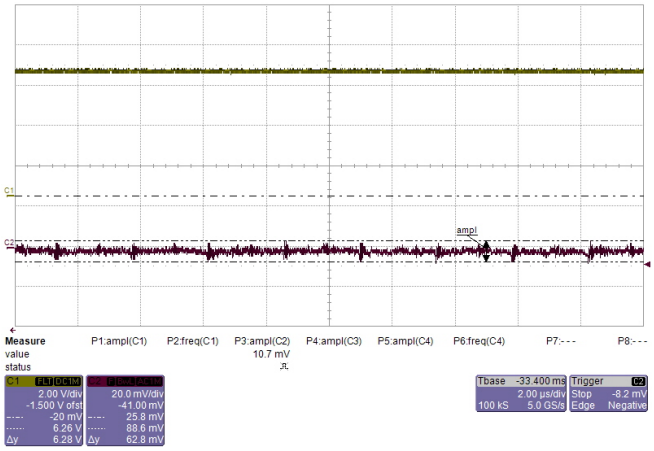


Figure 56. Output Ripple of Secondary Side of Transformer at No Load

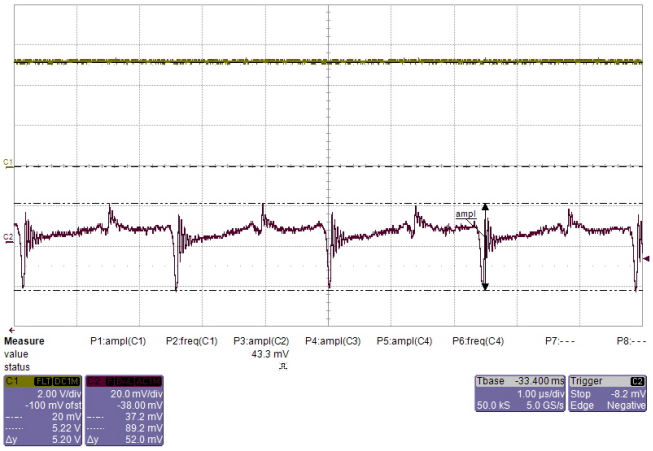


Figure 57. Output Ripple of Secondary Side of Transformer at Full Load

Figure 58 and Figure 59 show the output voltage versus the output ripples of the +5-V LDO output. The LDO reduces the noise generated by the transformer.

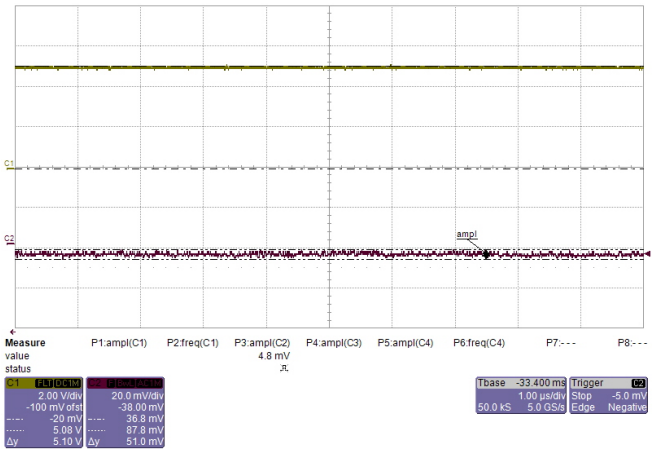


Figure 58. Output Ripple of LDO at No Load

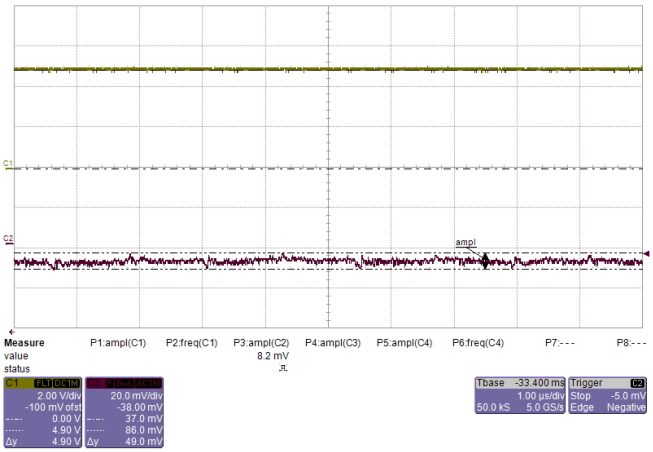


Figure 59. Output Ripple of LDO at Full Load

3.4.2 Signal Conditioning Circuit Characterization

The NTC signal conditioning circuit input is the differential voltage from the resistive divider. The measured data is transmitted from the ADS1015-Q1 to the MSP430 MCU through I^2C communication. The NTC resistance-to-temperature response data is obtained by curve fitting from the measured differential voltages. The IGBT module is placed into a temperature chamber for recording the NTC resistance change.

Figure 60 shows the test circuit with respect to the temperature response.

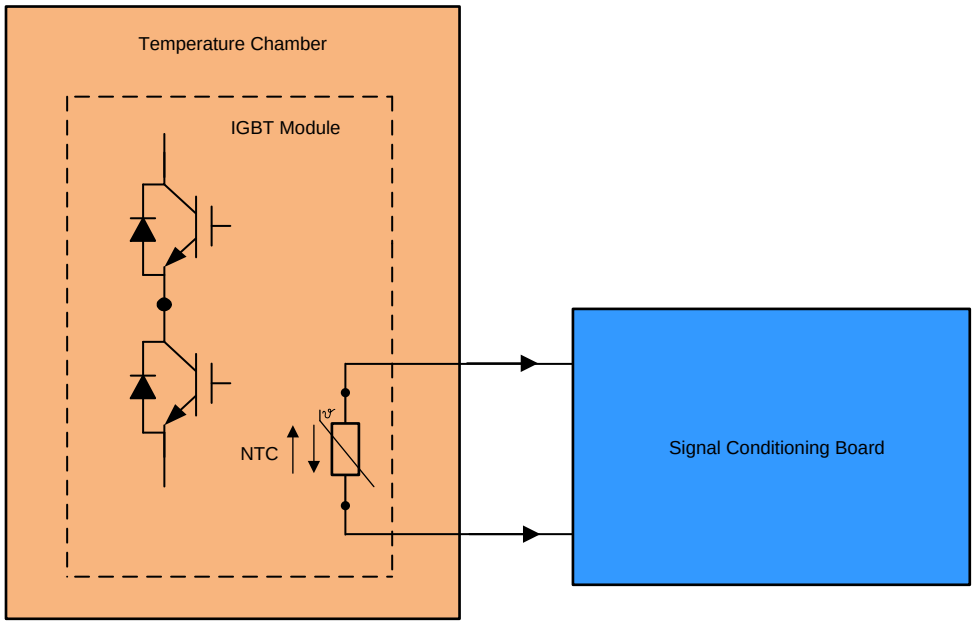


Figure 60. Test Circuit for NTC Signal Conditioning Board

Figure 61 shows the test setup.

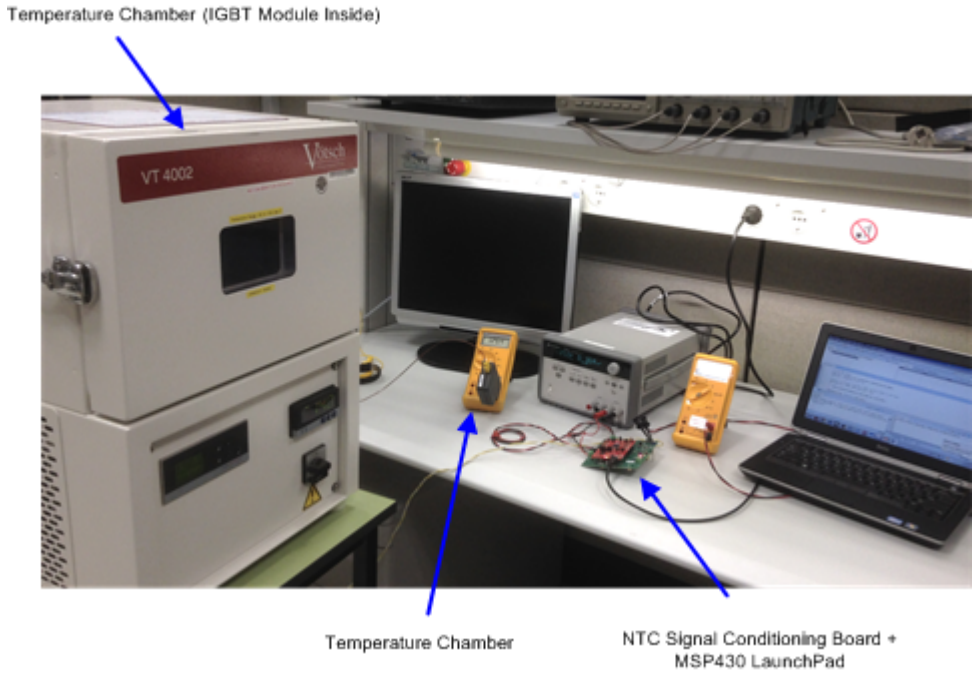


Figure 61. Test Setup for NTC Signal Conditioning Board

Extension of the differential voltages with regards to the entire temperature range (-40°C to +150°C) is done by curve fitting. Figure 62 shows the comparison of the curve-fitted results and the measurement from the ADC. The calculation matches closely to the measurement.

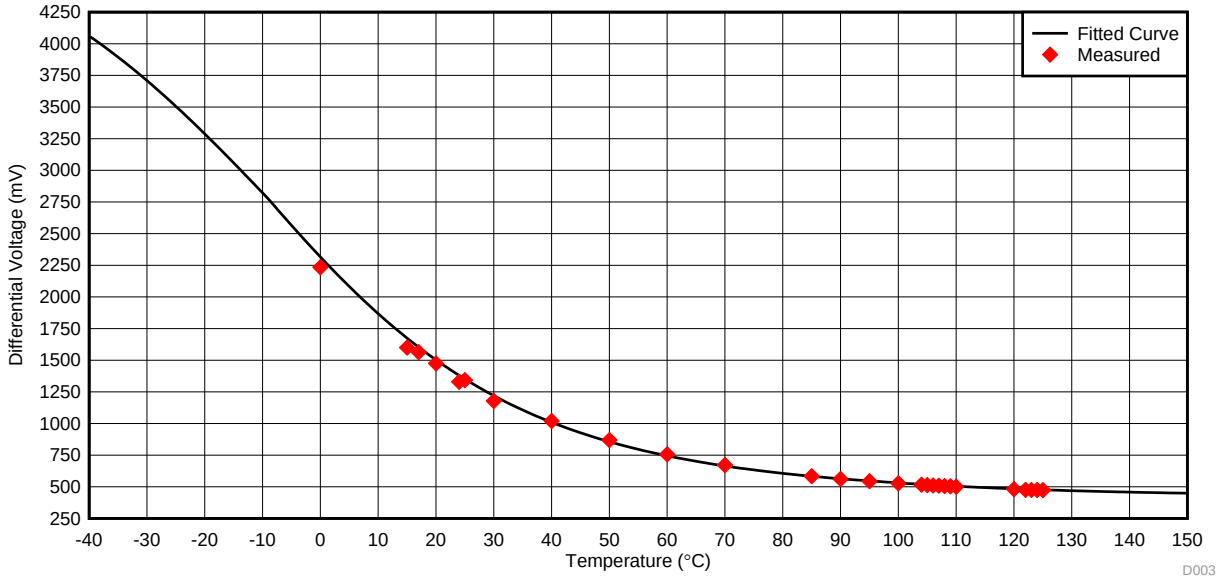


Figure 62. Comparison Between Measured and Calculated Differential Voltages at ADC Input

3.4.3 NTC Resistance-to-Temperature Characteristic

Use Equation 57 to calculate the NTC thermistor resistance-to-temperature characteristic.

$$R_{NTC} = R_{25} \times \left(e^{\beta\left(\frac{1}{T_2} - \frac{1}{T_1}\right)} \right) \tag{57}$$

where

- R_{25} = 5 kΩ is the NTC resistance at 25°C
- β is the beta value of the NTC
  - $\beta_{25/50}$ = 3407 k
  - $\beta_{25/80}$ = 3432 k
  - $\beta_{25/100}$ = 3453 k
- T_2 is the ambient temperature of the NTC in Kelvins
- T_1 = 298.15 k is the room temperature

Figure 63 shows the calculated curve of the temperature-resistance characteristic of the NTC thermistor.

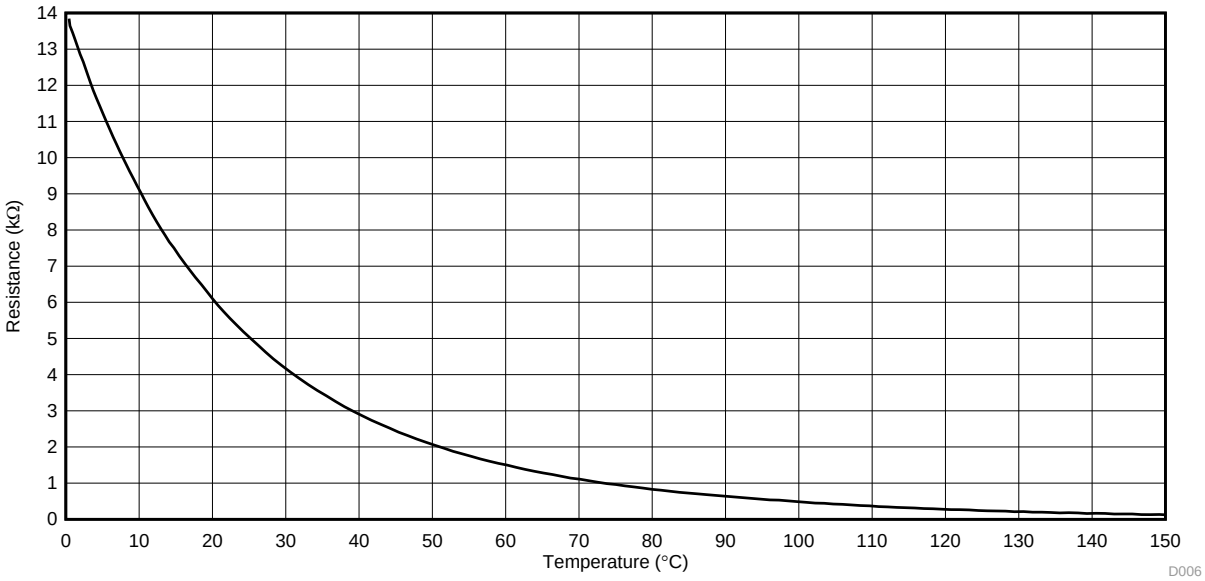


Figure 63. Calculated Temperature-Resistance Characteristic of NTC Thermistor

3.4.4 Overtemperature Shutdown-Signal Propagation Delay

This section shows the shutdown response of the whole system. The shutdown propagation delay begins when the MSP430 digital I/O shutdown signal is sent and ends when the IGBT gate start turns off. The high-temperature shutdown signal is triggered after the temperature of the NTC rises to the programmed upper threshold. Figure 64 shows the test circuit.

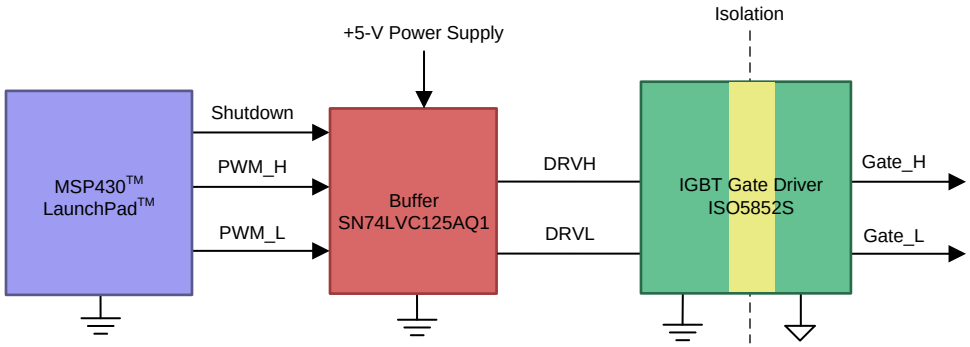


Figure 64. Test Circuit for Shutdown Digital-Control Signal Propagation Delay

Figure 65 shows the high temperature shutdown-response test of the whole system. The gate driver PWM output shuts down after the MSP430 digital output transitions from low to high.

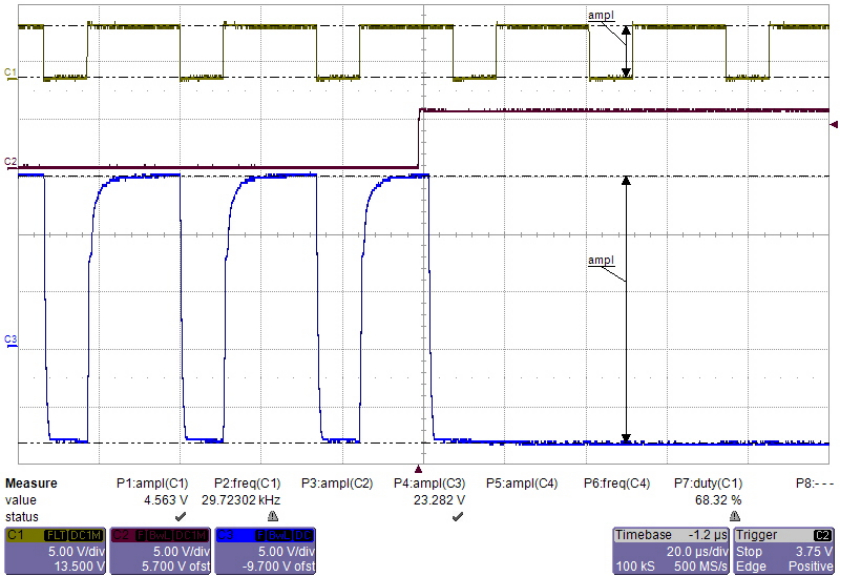


Figure 65. High Temperature Shutdown Response

Figure 66 shows the shutdown signal-propagation delay. The measurement begins when the MSP430 sends the shutdown signal (see Shutdown in Figure 64) and ends when the ISO5852S gate driver output turns off (see Gate_H and Gate_L in Figure 64). The total delay time is 2.539 µs.

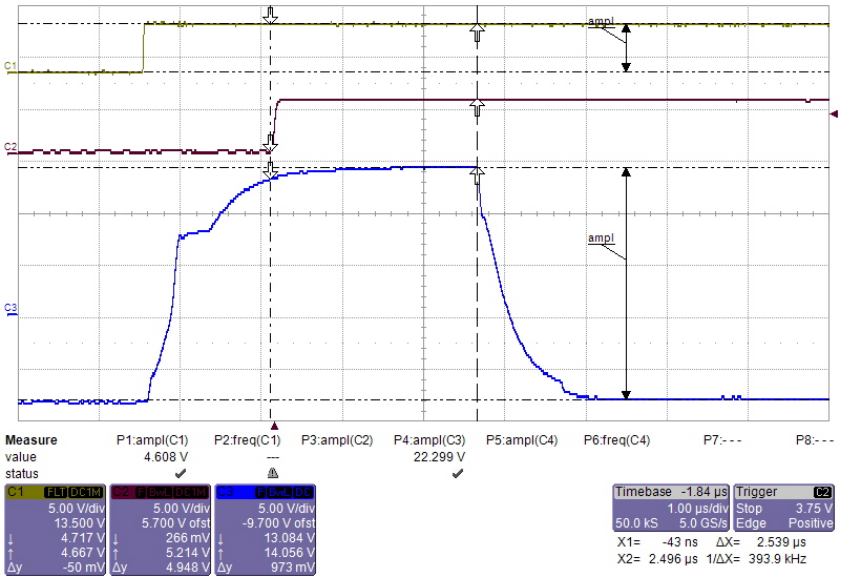


Figure 66. High Temperature Shutdown Propagation Delay

3.5 Gate Driver

3.5.1 PWM Switching

This section shows measurements of the gate driver. Figure 67 and Figure 68 show the PWM signals at the output of the ISO5852S and the push-pull current boost stage.

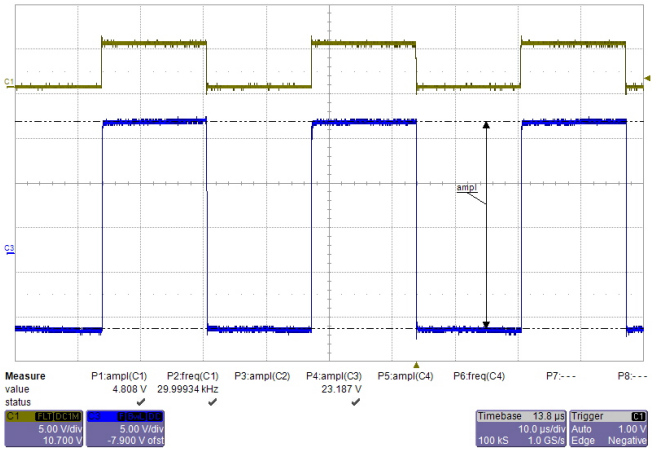


Figure 67. PWM Signals at Output of ISO5852S Gate Driver

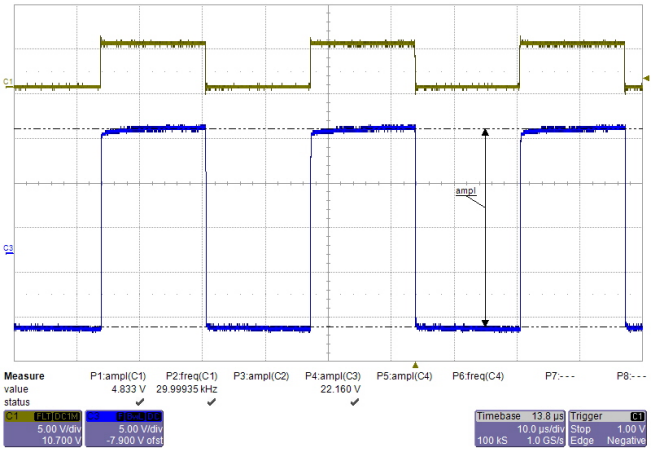


Figure 68. PWM Signals at Output of BJT Current Boost

3.5.2 PWM Propagation Delay

Figure 69 shows the PWM turnon delay between the primary side of the SN74LVC125A-Q1 and the output of the BJT current boost. **Figure 70** shows the PWM turnoff delay between the primary side of the SN74LVC125A-Q1 and the output of the BJT current boost. The turnon delay is 87.2 ns and the turnoff delay is 87.0 ns.

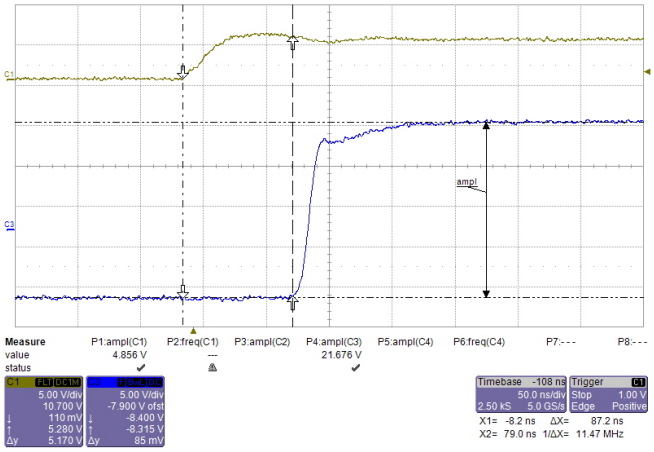


Figure 69. PWM Turnon Delay Between SN74LVC125A-Q1 and BJT

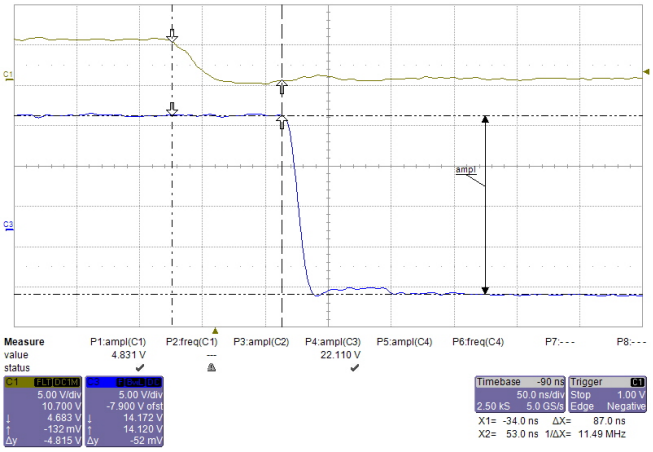


Figure 70. PWM Turnoff Delay Between SN74LVC125A-Q1 and BJT

3.5.3 Output of BJT Current Boost With Different Base Resistors

TI recommends adding resistors to the BJT base to limit the induced current. The value of the base resistors influences the switching speed of the BJTs. Higher resistance values slow down the speed and increase the losses. Two different resistor values are implemented and the BJT turnon and turnoff times are compared accordingly. See Equation 42 and Equation 43 for calculations.

Figure 71 and Figure 72 show the PWM rising speed of the BJT with 22-Ω and 3.3-Ω base resistors. A 10-nF capacitor was used between the gate and the emitter as the load in this test. The 3.3-Ω base resistance reduces the turnon time by 50 ns and reduces the turnoff time by 35 ns.

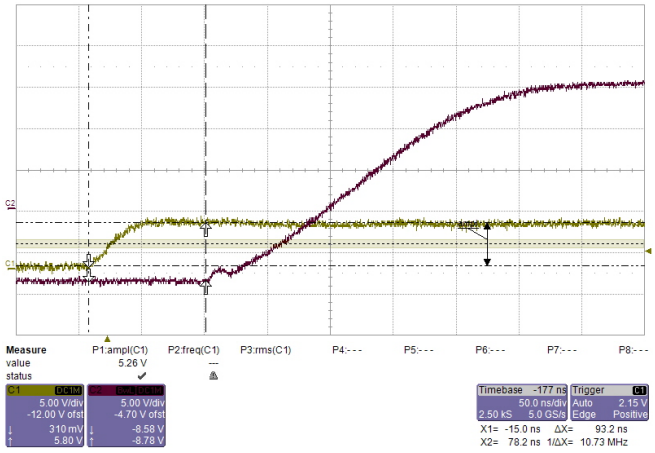


Figure 71. PWM Rise Slope With 22-Ω Base Resistor

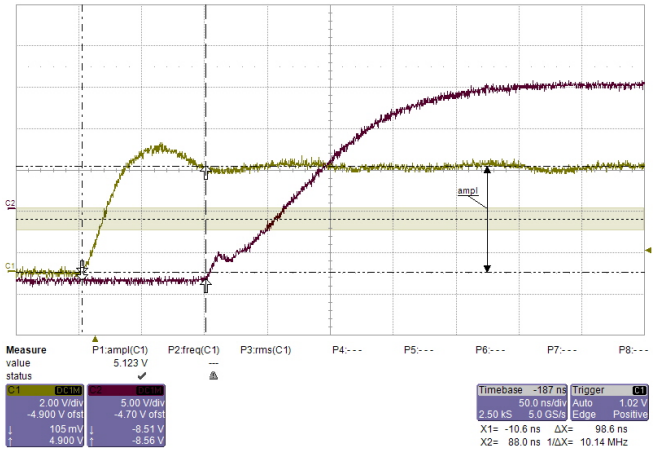


Figure 72. PWM Rise Slope With 3.3-Ω Base Resistor

Figure 73 and Figure 74 show the PWM falling speed of the BJT with a 22-Ω resistor and a 3.3-Ω resistor.

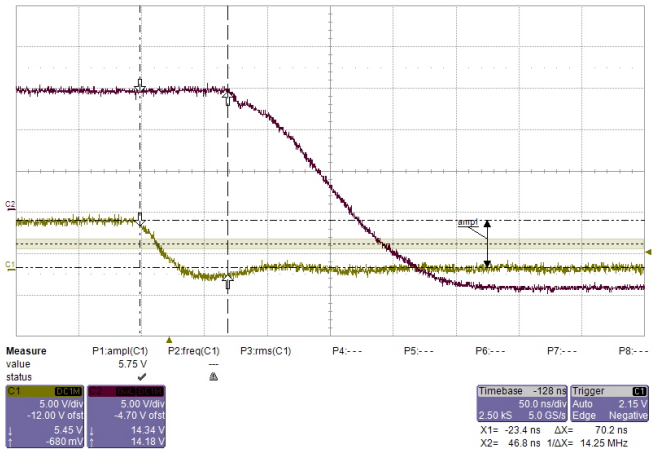


Figure 73. PWM Fall Slope With 22-Ω Base Resistor

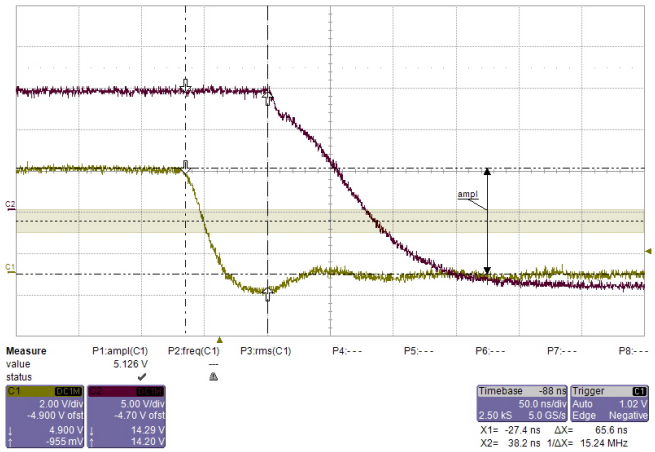


Figure 74. PWM Fall Slope With 3.3-Ω Base Resistor

3.5.4 Maximum Gate Sink and Source currents

The maximum source and sink currents from the gate driver during one PWM pulse were measured. A 100-nF capacitor was placed at the gate to emulate the IGBT gate capacitance. The total turnon gate resistance (R_{G_ON}) has been reduced to 2.37 Ω, and the total turnoff gate resistance (R_{G_OFF}) has been reduced to 2 Ω.

Figure 75 shows the test circuit of the maximum sink and source currents of the ISO5852S. Figure 76 shows the test circuit of the maximum sink and source currents of the BJT current boost. TI recommends applying 5.6-Ω resistors to the base of the BJT.

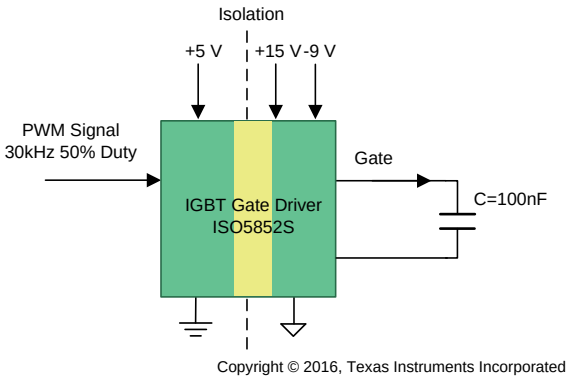


Figure 75. Test Circuit of ISO5852S

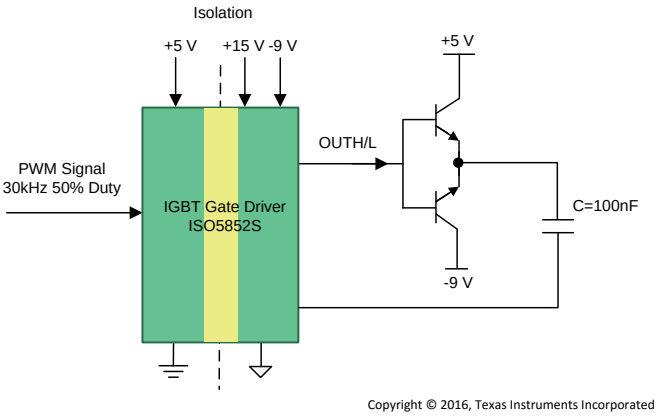


Figure 76. Test Circuit of BJT Current Boost

Figure 77 and Figure 78 show the PWM signals sent by the ISO5852S with and without the current boost. The rising slope is more steep with the current boost.

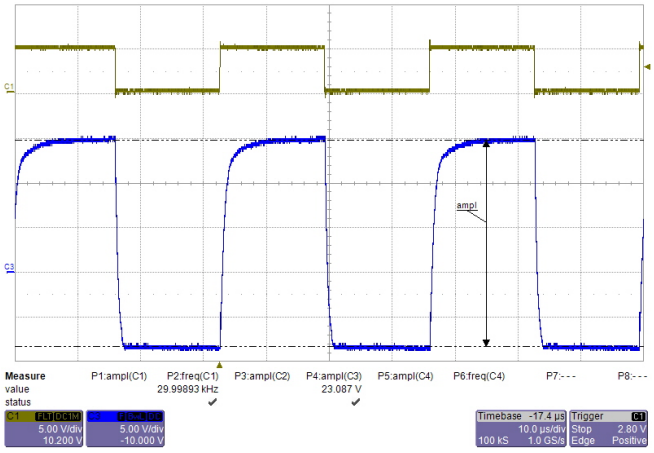


Figure 77. PWM Signal of Gate Driver Without BJT Current Boost

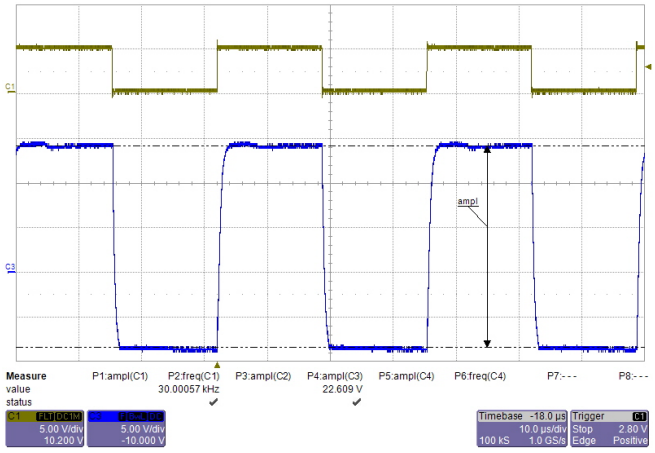


Figure 78. PWM Signal of Gate Driver With BJT Current Boost

Figure 79 through Figure 81 shows the sinking and sourcing drive current from the ISO5852S under a 100-nF load. A 2.79-A source current and a 4.59-A peak current were delivered in this test.

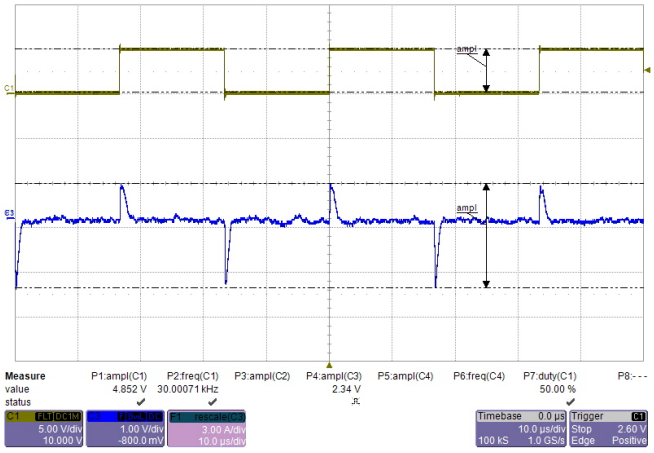


Figure 79. Sink and Source Currents of ISO5852S Under 100-nF Load

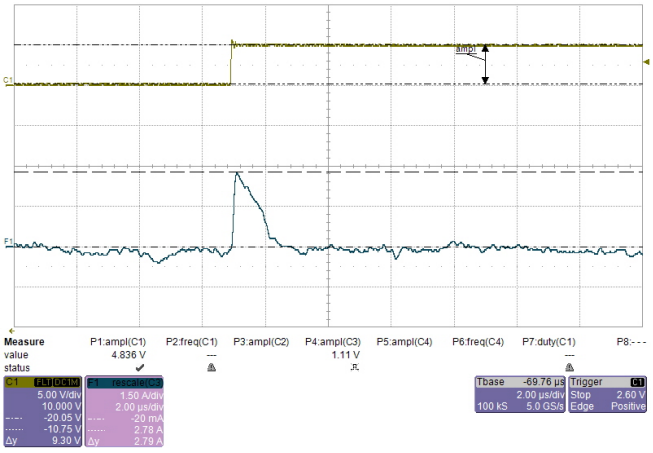


Figure 80. Source Current of ISO5852S Under 100-nF Load (2.79-A Peak)

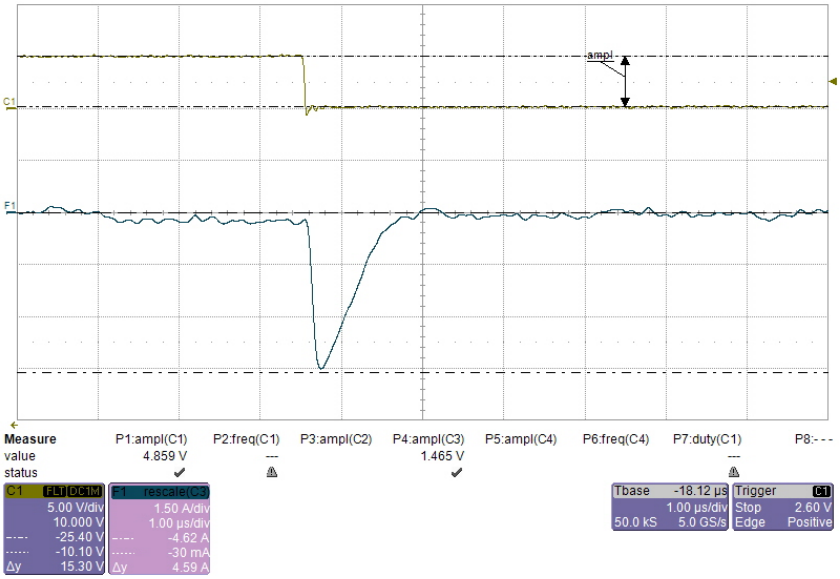


Figure 81. Sink Current of ISO5852S Under 100-nF Load (4.59-A Peak)

Figure 82 through Figure 84 shows the sink and source drive currents from the ISO5852S and the BJT current boost under a 100-nF load. A 6.69-A peak source current and a 7.20-A peak sink current were delivered in this test.

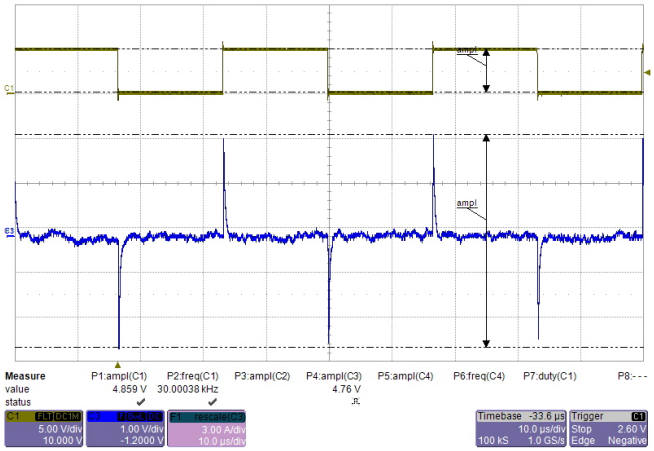


Figure 82. Sink and Source Current With BJT Current Boost Under 100-nF Load

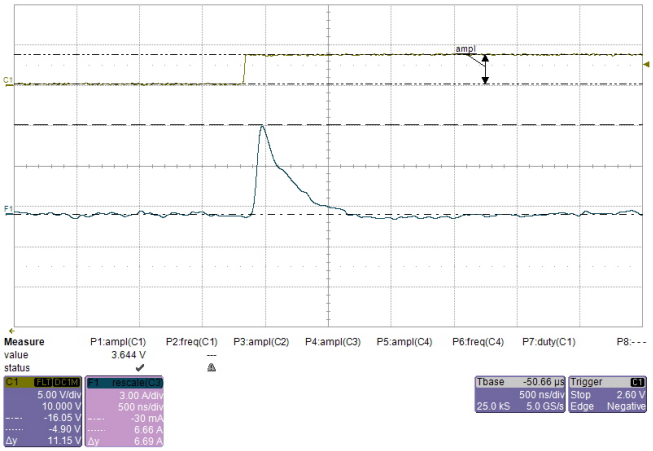


Figure 83. Source Current of BJT Current Boost Under 100-nF Load (6.69-A Peak)

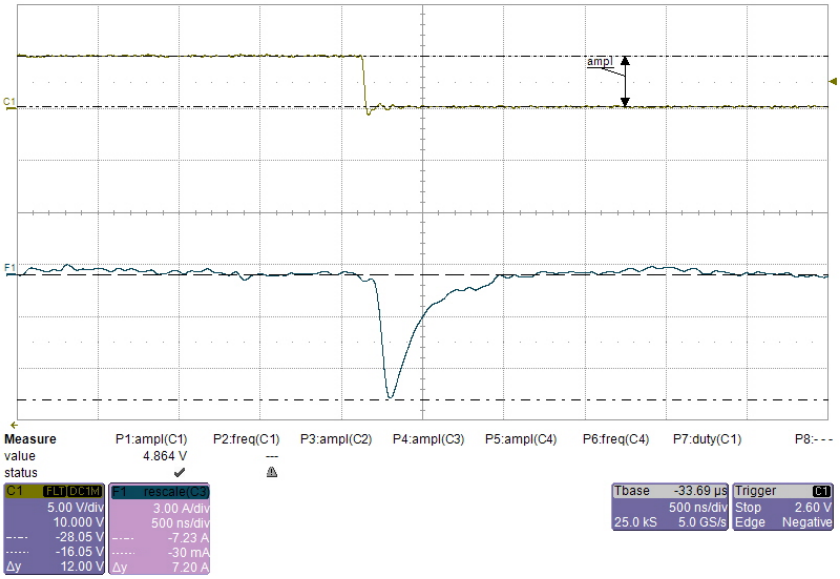


Figure 84. Sink Current of BJT Current Boost Under 100-nF Load (7.20-A Peak)

3.5.5 Active Miller Clamp

This section details the capability of the gate driver Miller clamp. A 400-V DC voltage was applied across DC link+ and DC link–. To capture the effect of the Miller clamp, the ISO5852S VEE2 pin was connected to the GND2 pin, the low-side IGBT is kept off, and the high-side is pulsed one time with a duration of 2 µs.

Figure 85 shows the test circuit.

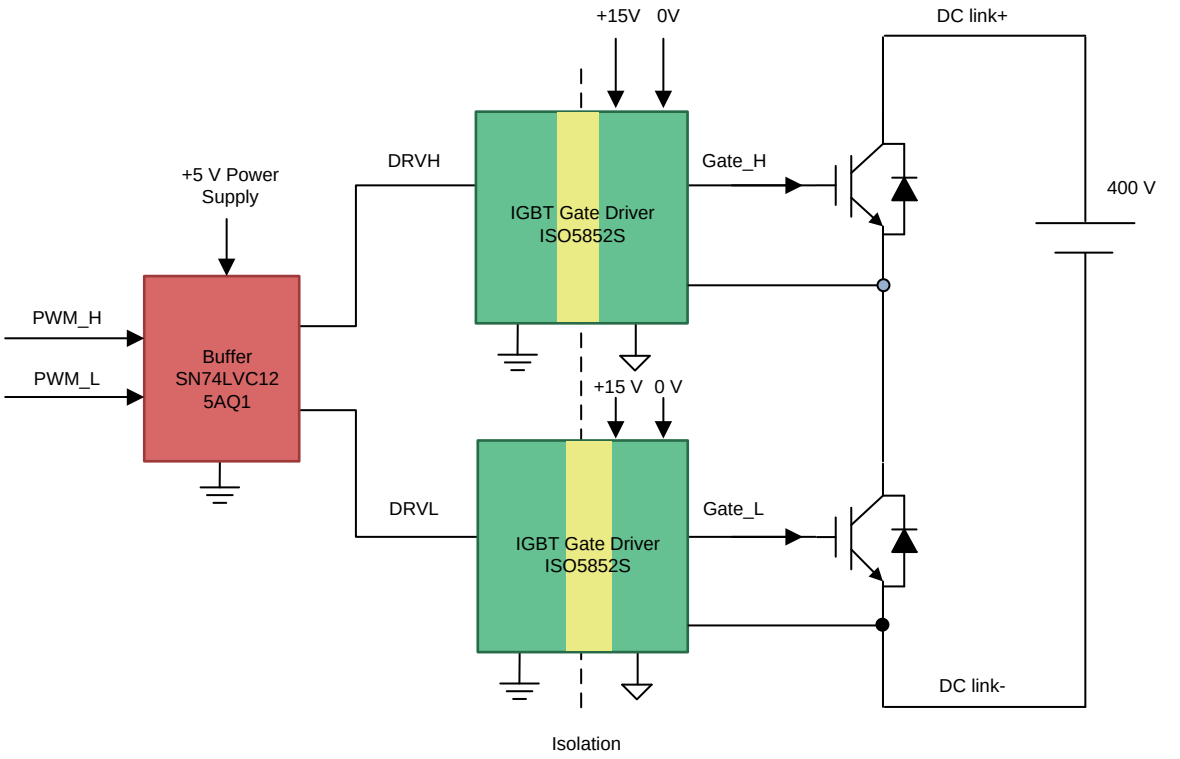


Figure 85. Test Circuit for Active Miller Clamp of Gate Driver

Figure 86 and Figure 87 show the measured waveforms. The Miller-induced voltage on the low-side IGBT is reduced to 1.5 V with the Miller clamp enabled. The switching dV/dt is: dV/dt = 400 V ÷ 140 ns = 2.86 kV/µs.

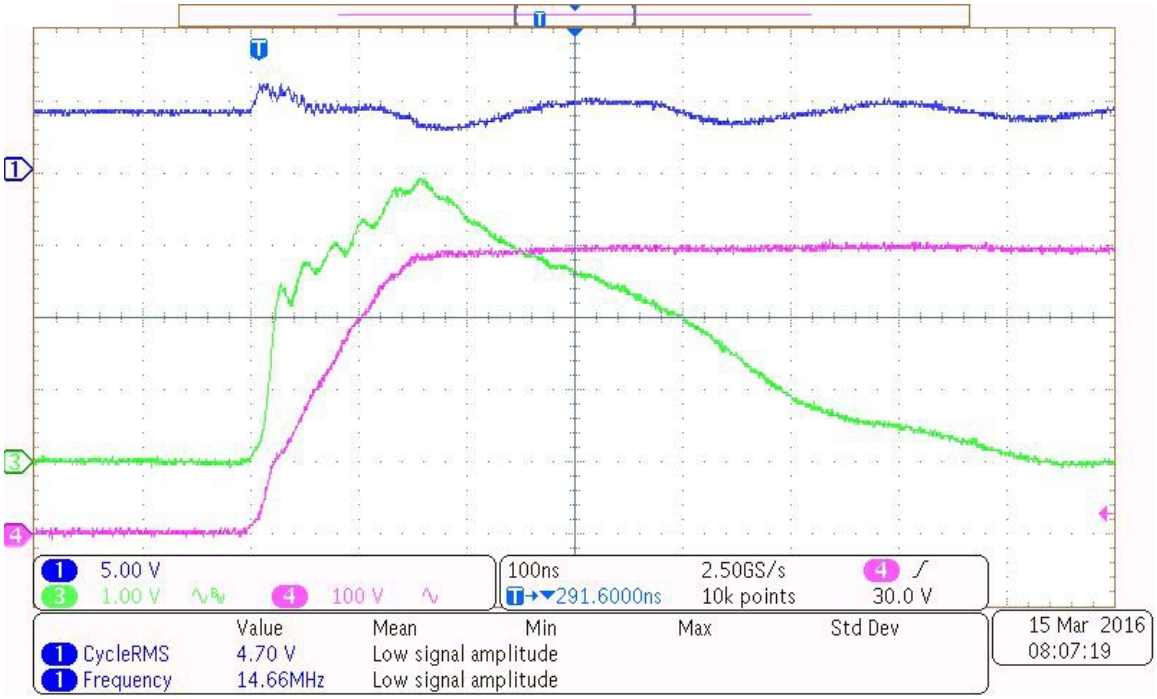


Figure 86. Active Miller Clamp Disabled

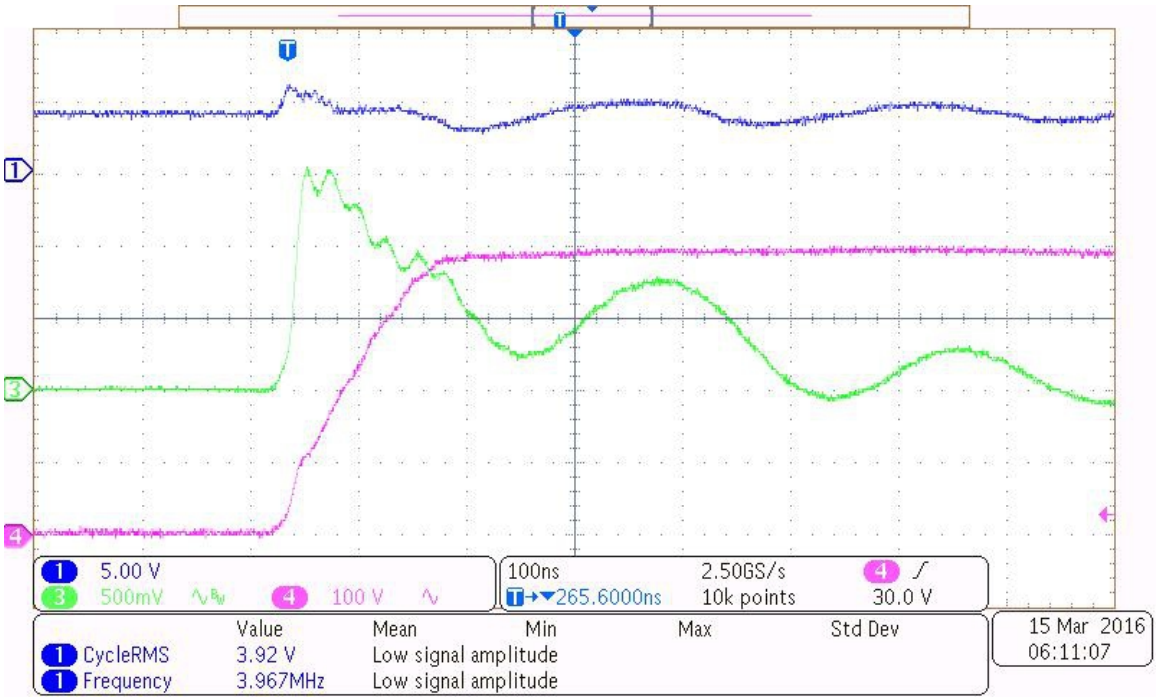


Figure 87. Active Miller Clamp Enabled

3.5.6 DESAT Protection Test

DESAT protection of the ISO5852S was tested under low-voltage and high-voltage conditions. Figure 88 shows the pin outs of the ISO5852S for measurements. Under a low-voltage condition:

- RST pin is set as the input and toggled with 50 kHz
- IN+ is tied together with IN– to ground

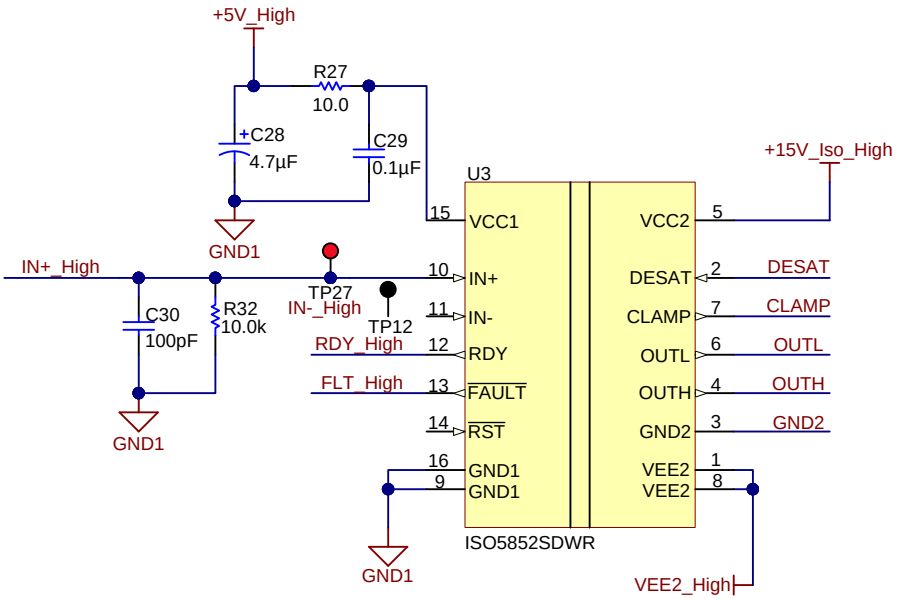


Figure 88. ISO5852S Pin Out

Figure 89 shows the measured waveforms. The $\overline{\text{FAULT}}$ pin goes low after DESAT reaches 9 V with a delay of 750 ns.

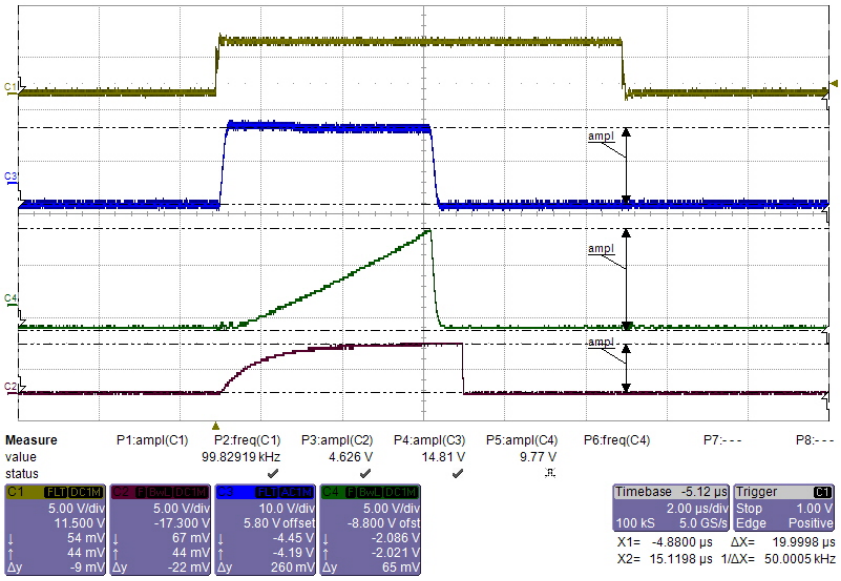


Figure 89. DESAT Protection — RST Pin Toggled With 50 kHz

After the digital-signal buffer of the SN74LVC125A-Q1 is disabled, the PWM input to the gate driver is put in a tri-state condition. This condition leaves the IGBT gate in a high impedance state. The ISO5852S has a soft-turnoff feature that discharges the gate capacitor and reduces the IGBT collector-emitter voltage overshot. The soft-turnoff period is 2 µs.

Figure 90 shows the ISO5852S output waveform when the soft turnoff is activated. The gate voltage gradually decreases from high potential until it reaches 2 V with regards to VEE2, then it is strongly clamped to the negative potential.

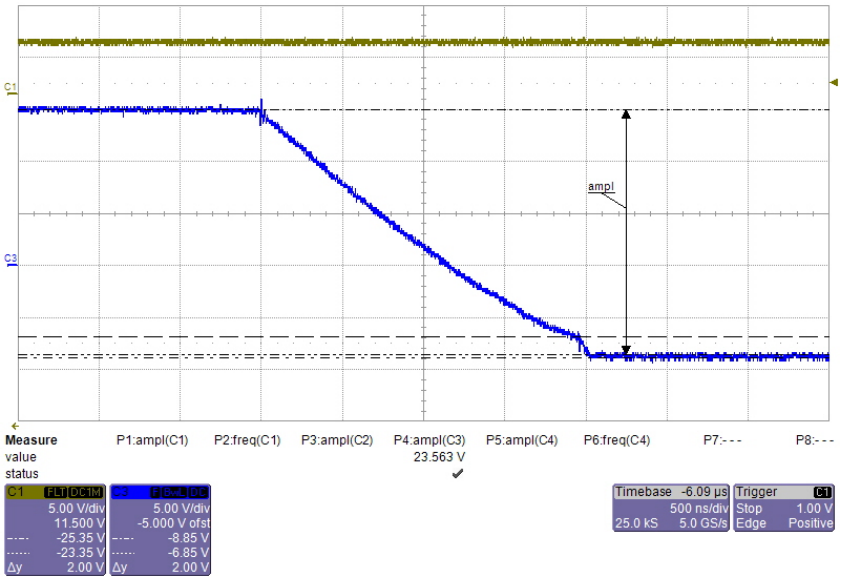


Figure 90. Soft Turnoff of ISO5852S

Figure 91 shows the PWM output after the BJT push-pull current boost is added. The soft turn off feature is lost. The gate voltage reduces within the same time period of the ISO5852S DESAT pin voltage.

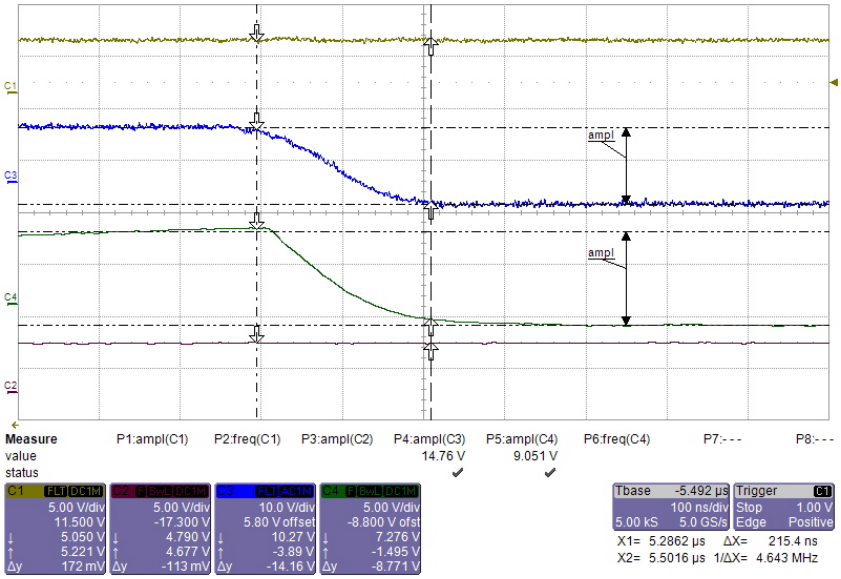


Figure 91. Turnoff With BJT current Boost

Figure 92 shows the propagation delay of the fault signal. The measurement begins when DESAT of the ISO5852S triggers and ends when the ISO5852S fault signal is sent.

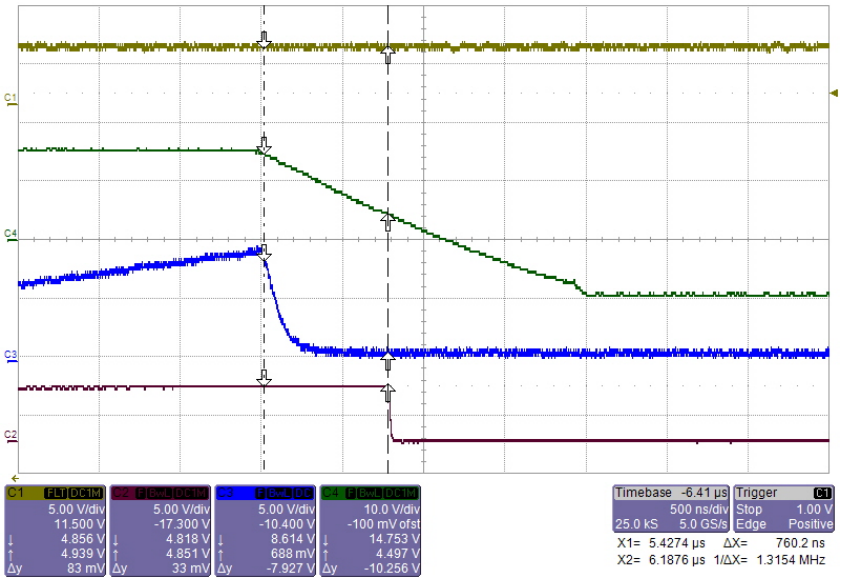


Figure 92. Delay of Fault Signal Out

Under a high voltage condition, DESAT protection is tested by applying a short circuit on the low-side IGBT. Up to 400-V of DC voltage is applied across the collector and source of the low-side IGBT. The high-side IGBT is kept off and the low side IGBT is driven by a single-shot pulse. A 0.2-Ω load resistor is added to limit the current. The pulse duration is limited to 6 µs for safe operation.

Figure 93 shows the test circuit for desaturation protection.

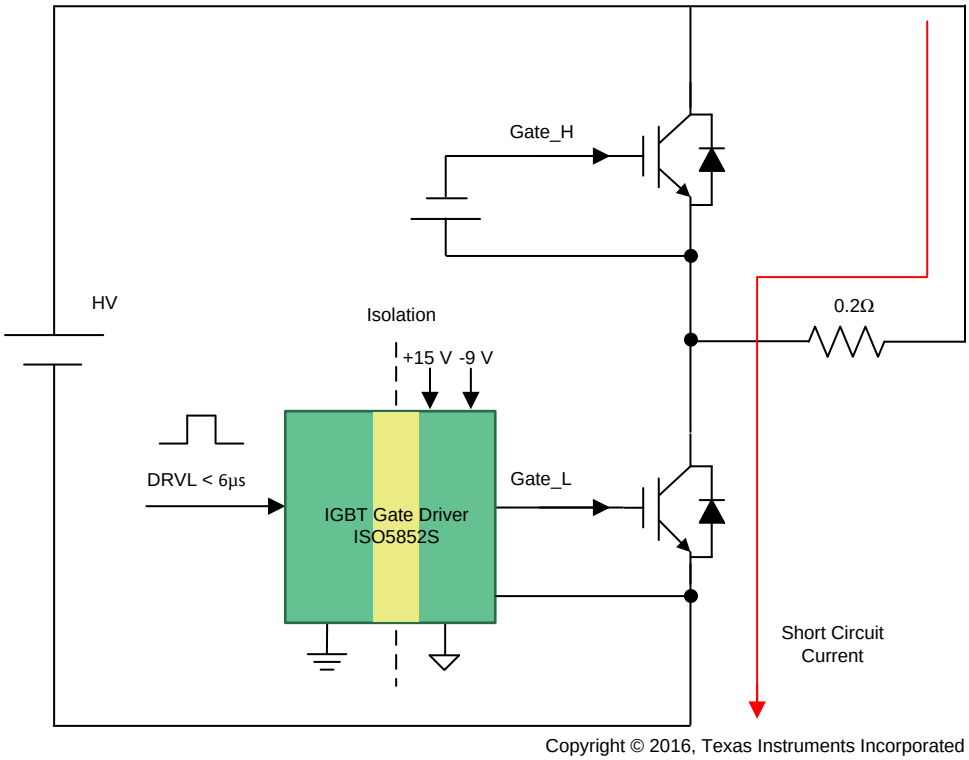


Figure 93. Test Circuit for Driver Desaturation Protection

Figure 94 through Figure 96 shows the DESAT detection of the driver with the BHT current boost. The DESAT response time is 396 ns.

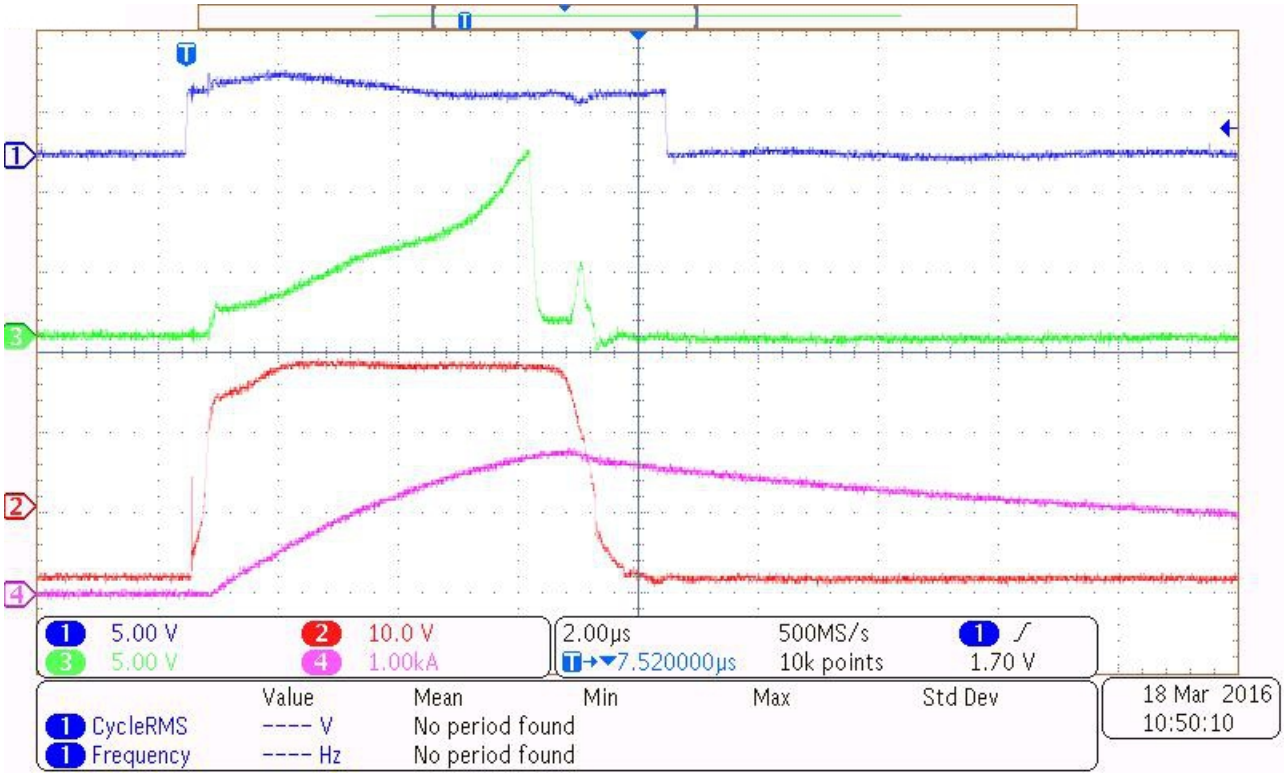


Figure 94. DESAT Protection Test With BJT Push-Pull Current Boost

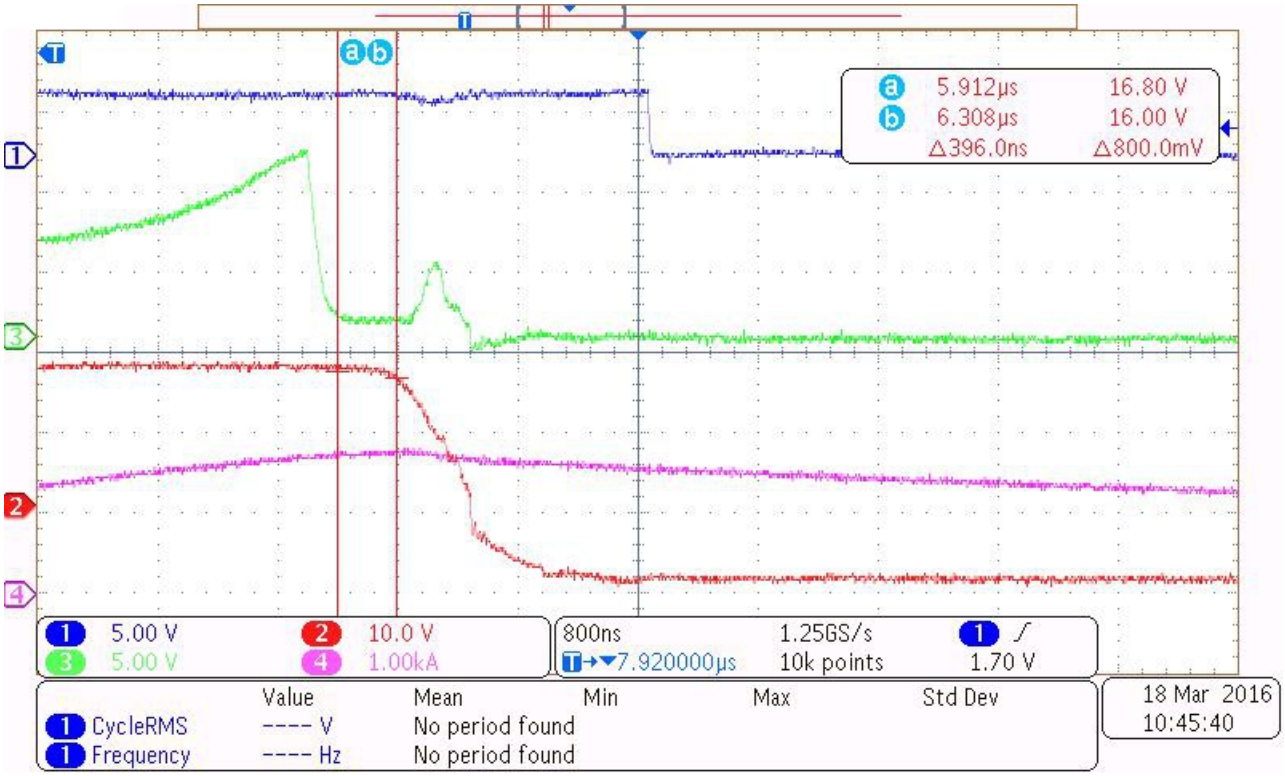


Figure 95. DESAT Protection Response Time

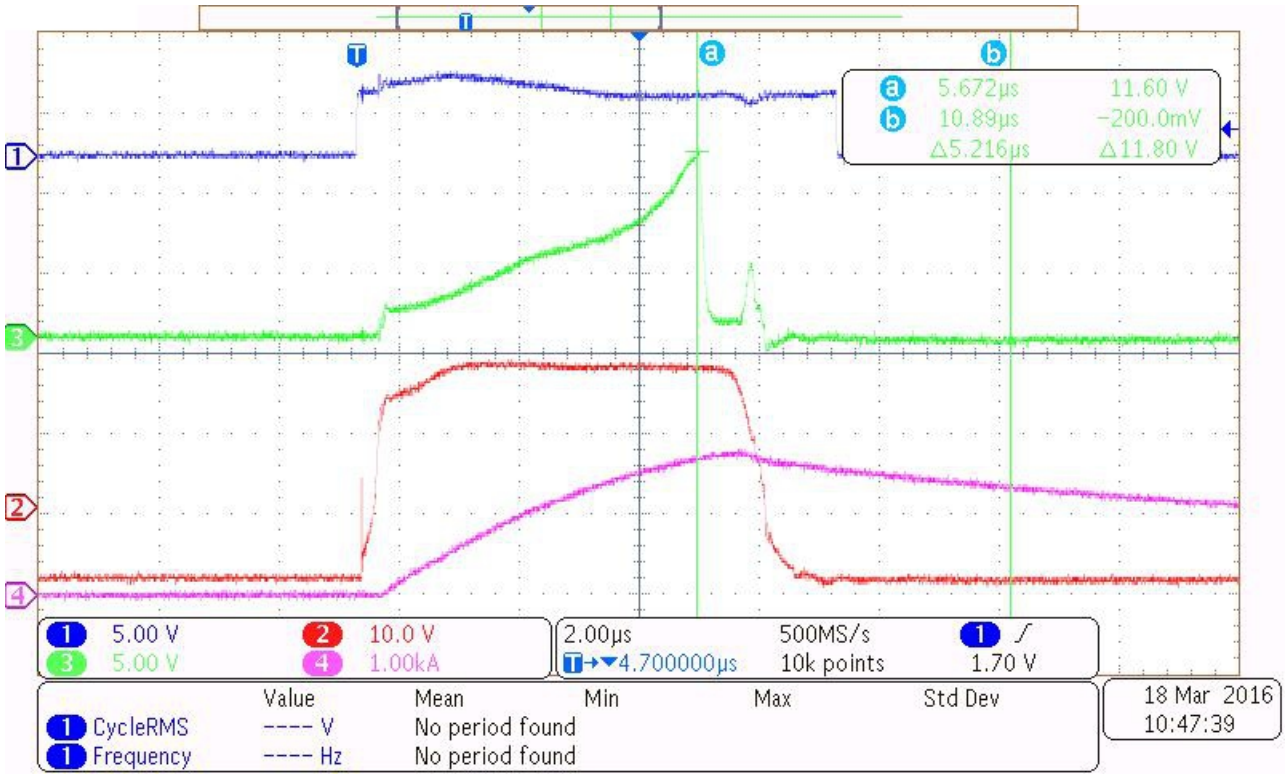


Figure 96. DESAT Detection Threshold

3.6 IGBT Switching Waveforms

This section shows the waveforms of IGBT drain-source current with respect to the drain-source voltage during switching transients. A 400-V DC voltage is applied on the DC bus. A 22-Ω load resistor is applied. The high-side IGBT is kept off and the low side IGBT is switched. Rise and fall periods are measured.

Figure 97 shows the test circuit with measurement points. The current flowing through the load resistor and the collector-to-emitter of the low side IGBT is measured.

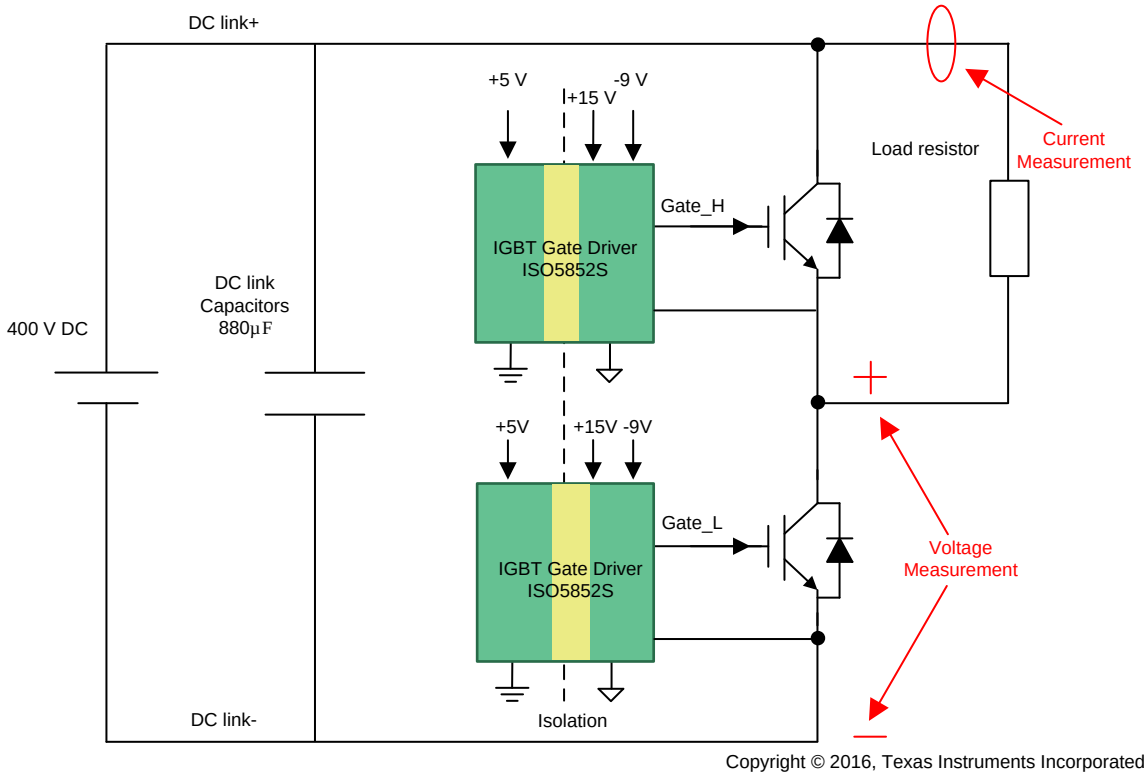


Figure 97. Test Points of IGBT Switching Waveforms

Figure 98 shows the switching waveforms of the IGBT.

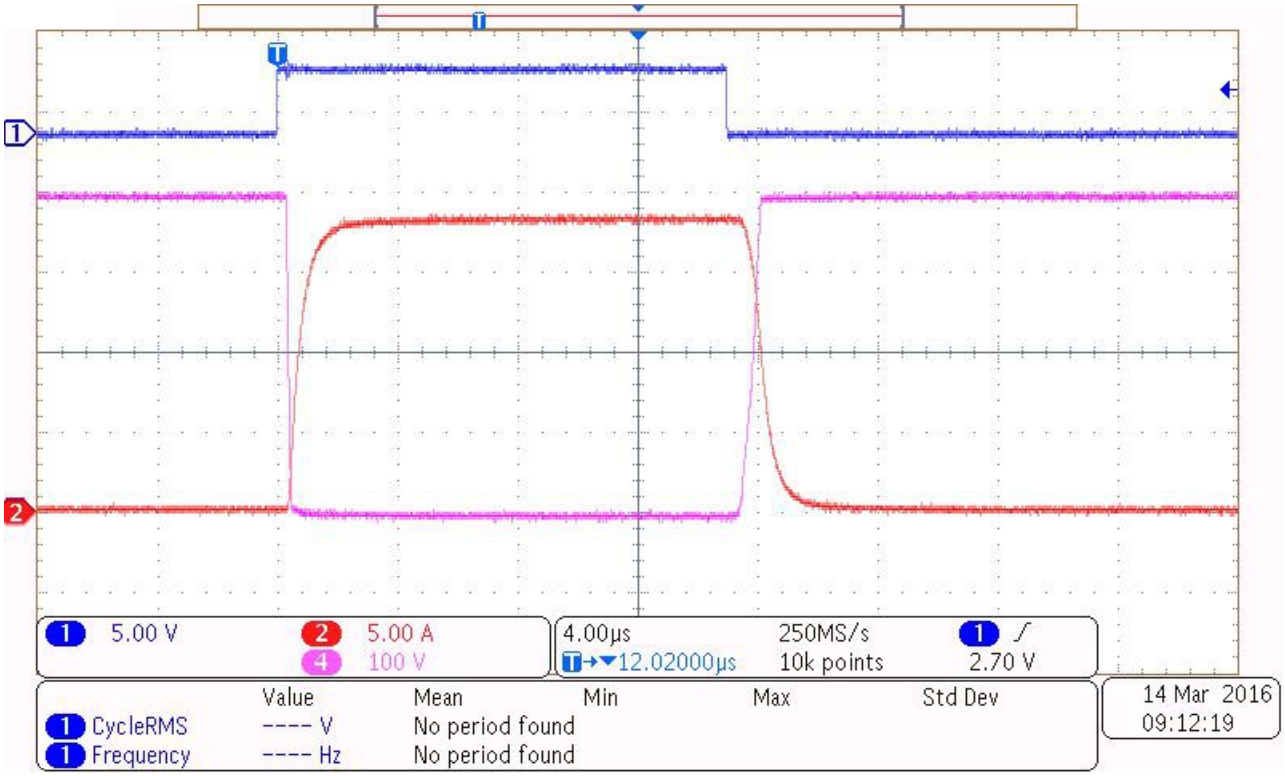


Figure 98. IGBT Switching Waveforms

Figure 99 and Figure 100 show the switching transient at turnon and turnoff.

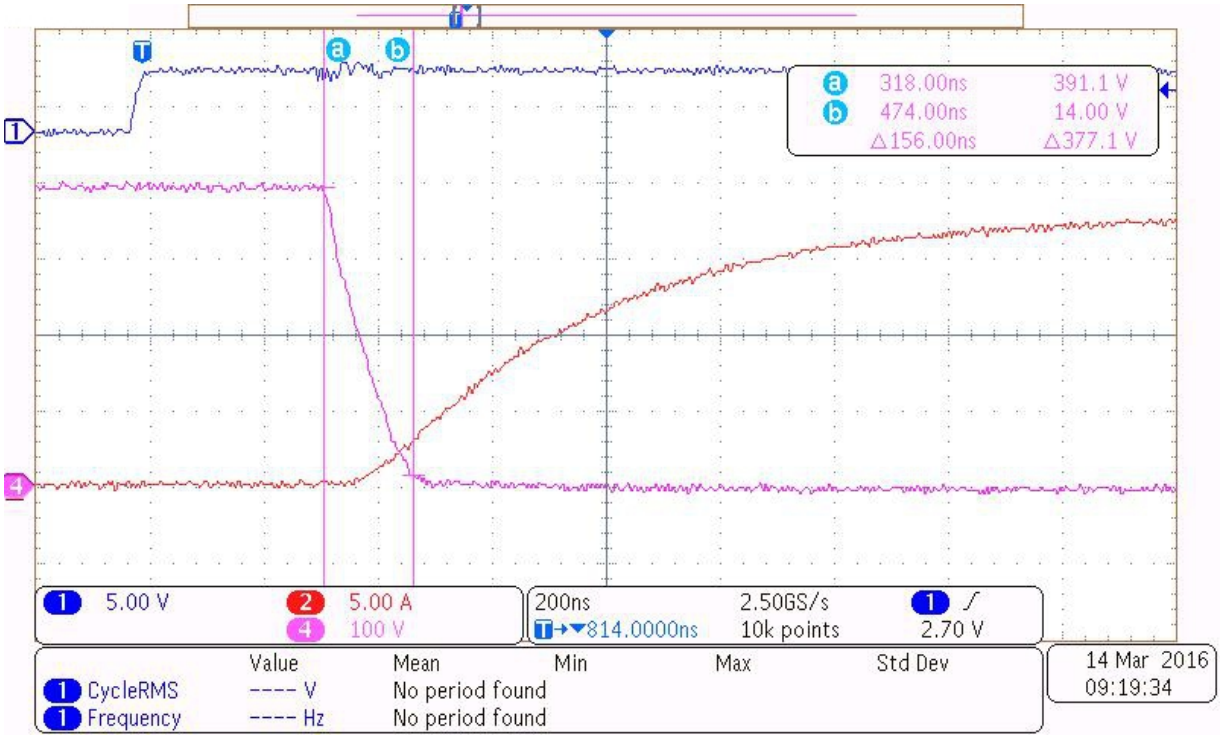


Figure 99. IGBT Turnon Transient

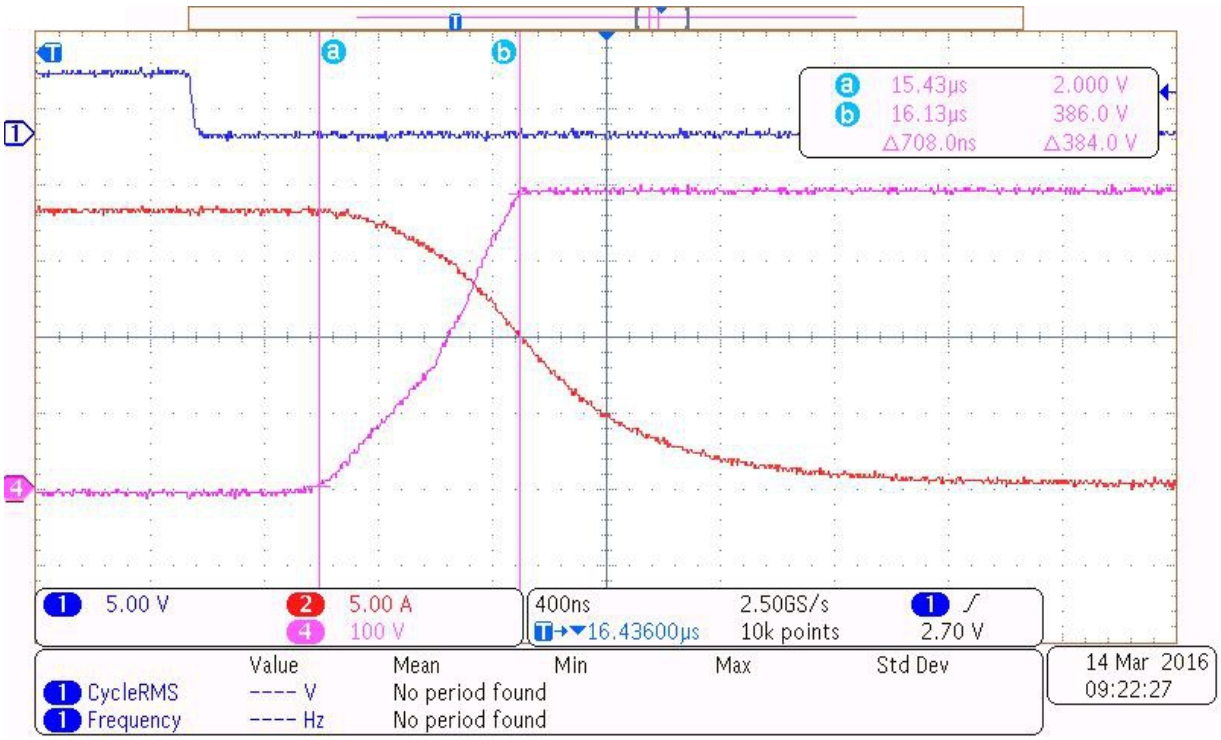


Figure 100. IGBT Turnoff Transient

3.7 Temperature Rise of Gate Driver Board

Figure 101 shows the thermal image of the low side gate driver channel after running at 100-nF gate-to-emitter capacitor load for 30 minutes at a room temperature of 25°C. The PWM into the gate driver is 30 kHz. The two gate resistors are the hottest spots in the circuit and the average temperature of the board is controlled below 55°C.

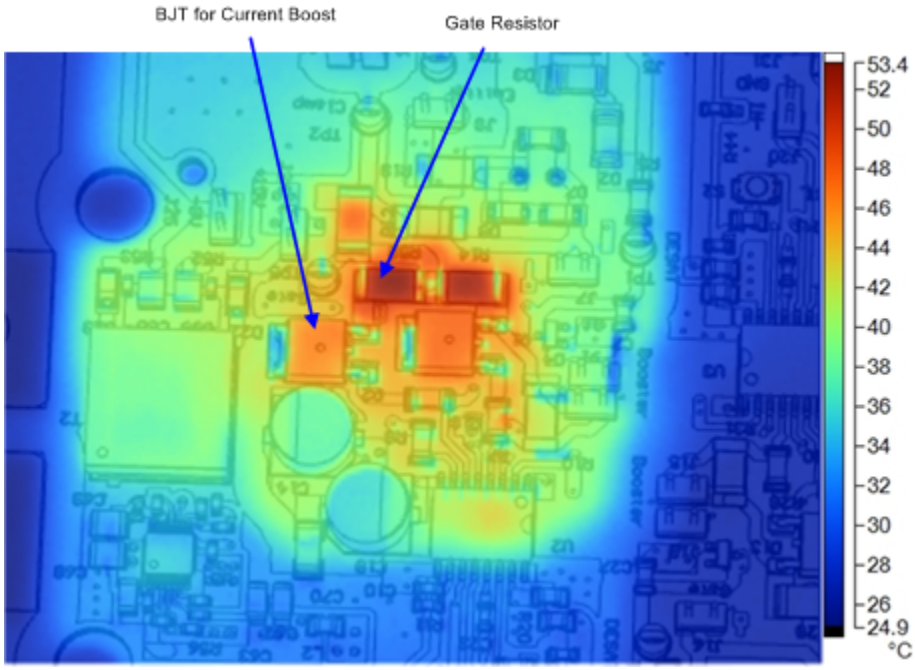


Figure 101. Thermal Image of Gate Driver Board at 100-nF Load for 30 Minutes

4 Design Files

4.1 Schematics

To download the schematics, see the design files at TIDA-00794.

4.2 Bill of Materials

To download the bill of materials (BOM) for each board, see the design files at TIDA-00794.

4.3 PCB Layout Recommendations

4.3.1 Layout Prints

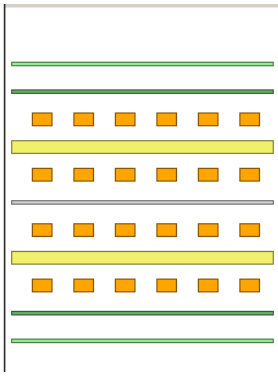
To download the layer plots, see the design files at TIDA-00794.

4.3.2 Layout Guidelines

Follow the layout guidelines in Section 4.3.2.1 and Section 4.3.2.2 to ensure the system functions.

4.3.2.1 Gate Driver Board

The gate driver board has a four-layer PCB. Figure 102 shows the board material, copper thickness, and the isolation space between different layers.



Layer Name	Type	Material	Thickness (mm)	Dielectric Material	Dielectric Constant	Pullback (mm)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask...	Surface Mat...	0.01016	Solder Resist	3.5			0
Top Layer	Signal	Copper	0.07				Top	
Dielectric1	Dielectric	Core	0.5	FR-4	4.2			
2nd Layer	Signal	Copper	0.07				Not Allowed	
Dielectric 2	Dielectric	Prepreg	1.016		4.8			
3rd Layer	Signal	Copper	0.07				Not Allowed	
Dielectric 3	Dielectric	Core	0.5		4.2			
Bottom Layer	Signal	Copper	0.07				Bottom	
Bottom Solder	Solder Mask...	Surface Mat...	0.01016	Solder Resist	3.5			0
Bottom Over...	Overlay							

Figure 102. Four-Layer Stack

Figure 103 shows the layout of the top layer where the high voltage area and the electrical clearance are indicated. A clearance of 160 mil is placed for practical purpose between different voltages of the primary side of the gate driver, secondary side of the gate driver, DC link+, DC link–, and phase out. The isolated gate driver (ISO5852S) and the isolated fly-buck transformer separate the high-voltage area to the low-voltage area. The remaining area is connected to the low-voltage ground.

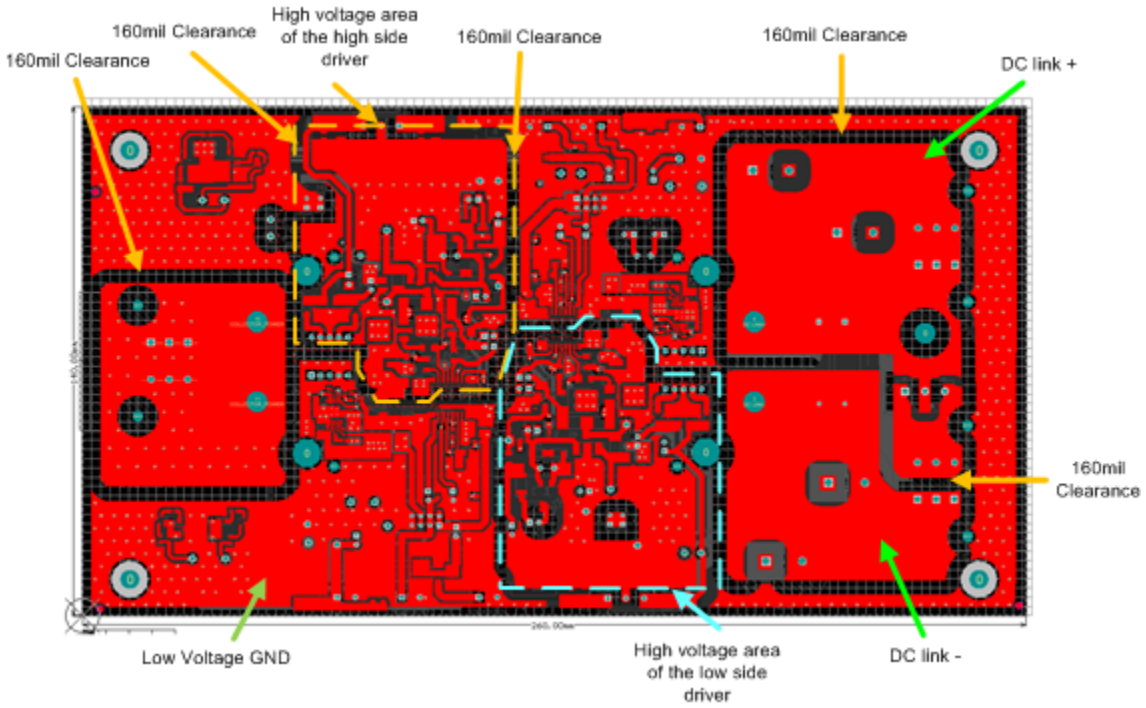


Figure 103. Top Layer of Gate Driver Board

Figure 104 shows the layout of the second layer. The figure shows the polygon pours that connect to GND2 of both gate drivers.

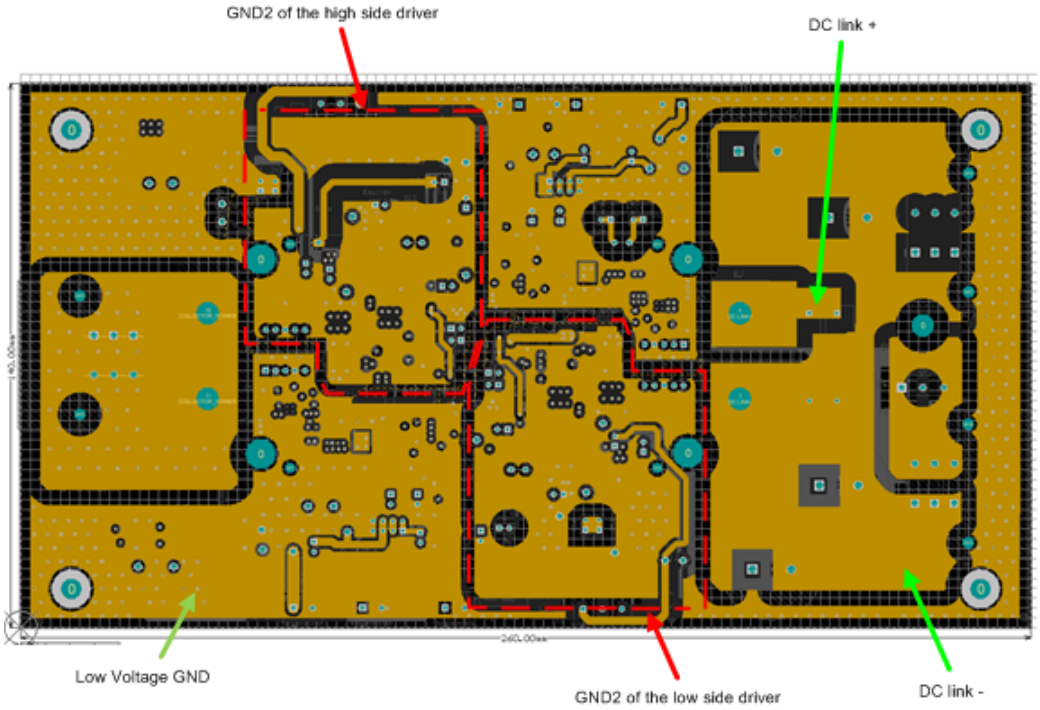


Figure 104. Second Layer of Gate Driver Board

Figure 105 shows the layout of the third layer. The figure shows the polygon pours that connect to VCC2 (+15 V) of both gate drivers.

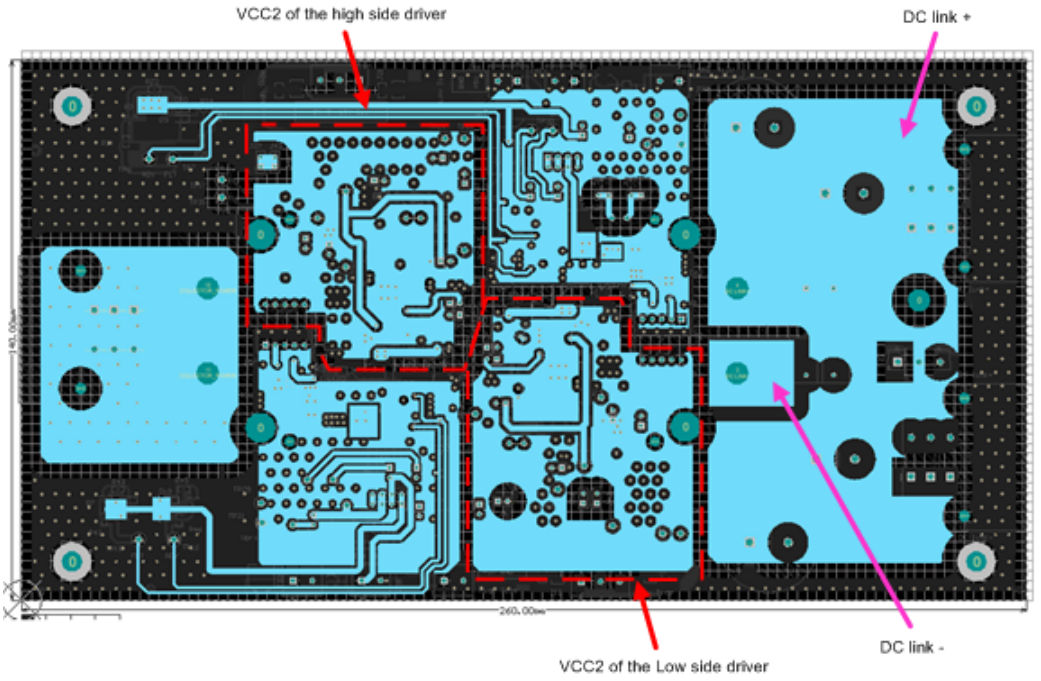


Figure 105. Third Layer of Gate Driver Board

Figure 106 shows the layout of the fourth layer. The figure shows the polygon pours that connect to VEE2 (–9 V) of both gate drivers.

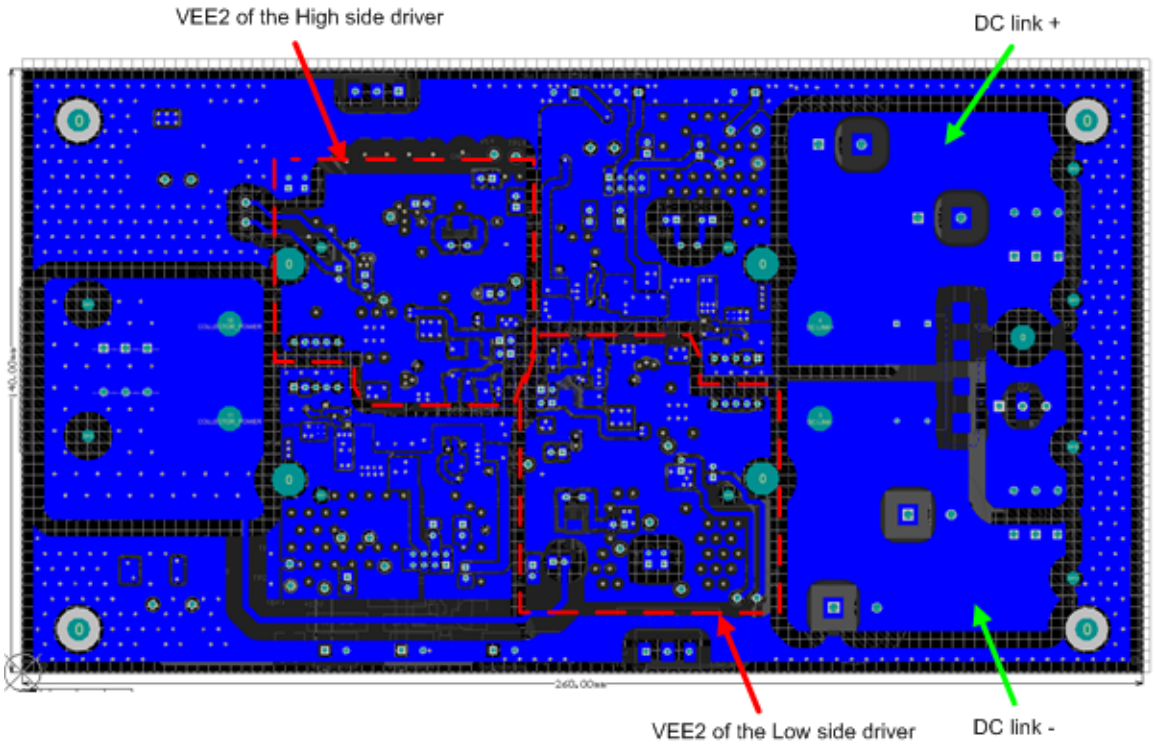


Figure 106. Fourth Layer of Gate Driver Board

Figure 107 and Figure 108 show the connection from the DESAT blocking diode to the collector of the high-side IGBT and the low-side IGBT.

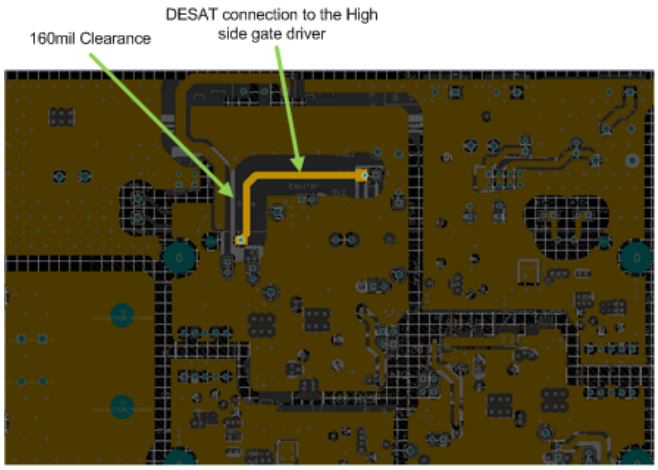


Figure 107. PCB Trade From DESAT to High-Side Driver

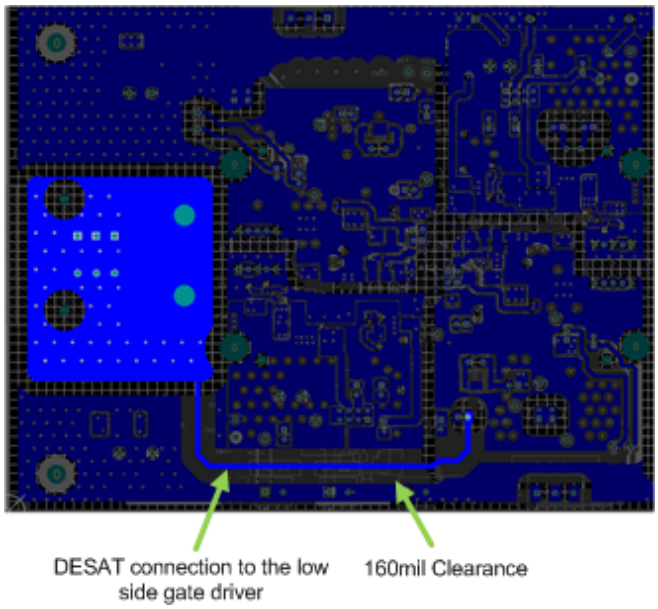


Figure 108. PCB Trace From DESAT to Low-Side Driver

Figure 109 shows the placement of the input and output capacitors for the isolated Fly-Buck converter.

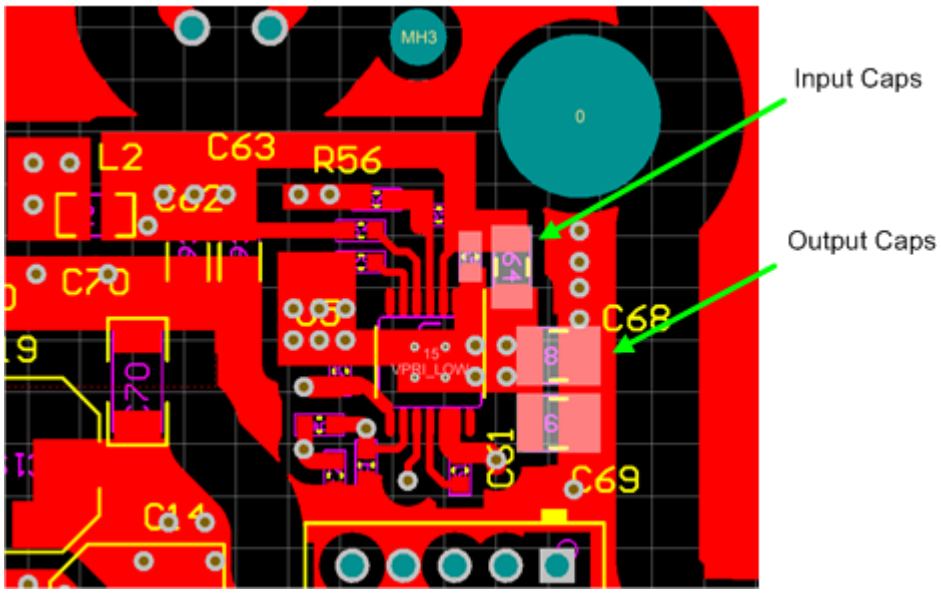


Figure 109. Placement of Input and Output Capacitors in Fly-Buck™ Converter

Figure 110 shows the placement of output capacitors and rectifying diodes at the secondary side of the transformer.

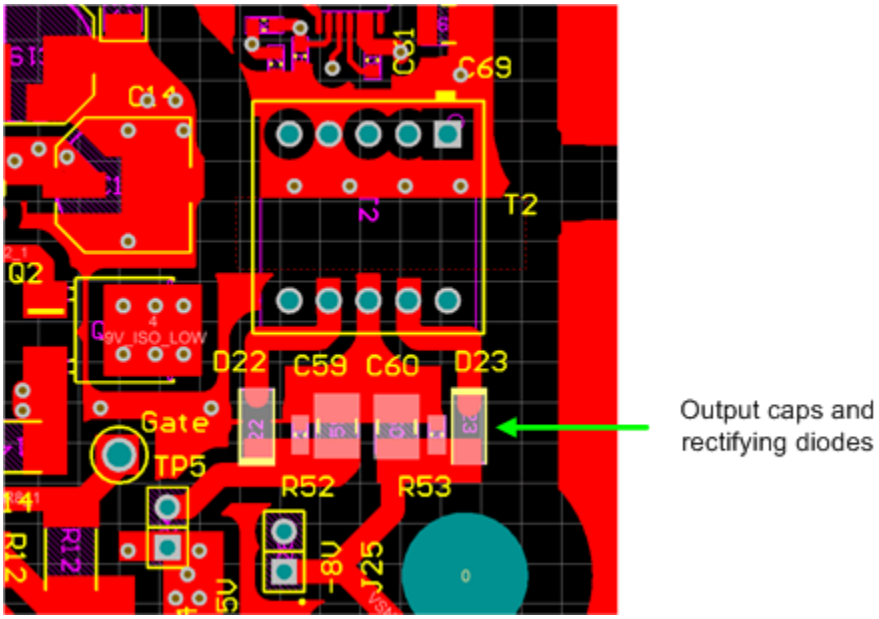
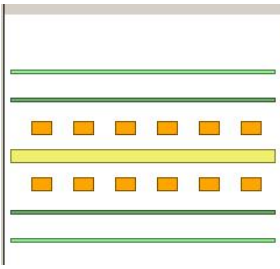


Figure 110. Placement of Transformer Secondary Components

4.3.2.2 NTC Signal Conditioning Board

The NTC signal conditioning board has a two-layer PCB. Figure 111 shows the board material, copper thickness, and the isolation space between different layers.



Layer Name	Type	Material	Thickness (mil)	Dielectric Material	Dielectric Constant	Pullback (mil)	Orientation	Coverlay Expansion
Top Overlay	Overlay							
Top Solder	Solder Mask...	Surface Mat...	0.4	Solder Resist	3.5			0
Top Layer	Signal	Copper	1.4				Top	
Dielectric1	Dielectric	Core	59.2	FR-4	4.8			
Bottom Layer	Signal	Copper	1.4				Bottom	
Bottom Solder	Solder Mask...	Surface Mat...	0.4	Solder Resist	3.5			0
Bottom Over...	Overlay							

Figure 111. Two-Layer Stack

Figure 112 and Figure 113 show the distance clearances between high-voltage and low-voltage circuits on the top and bottom layers on the NTC signal conditioning board.

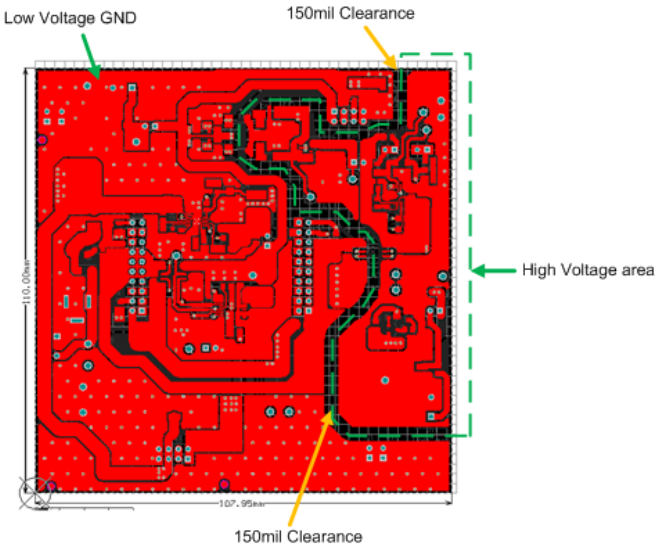


Figure 112. Top Layer

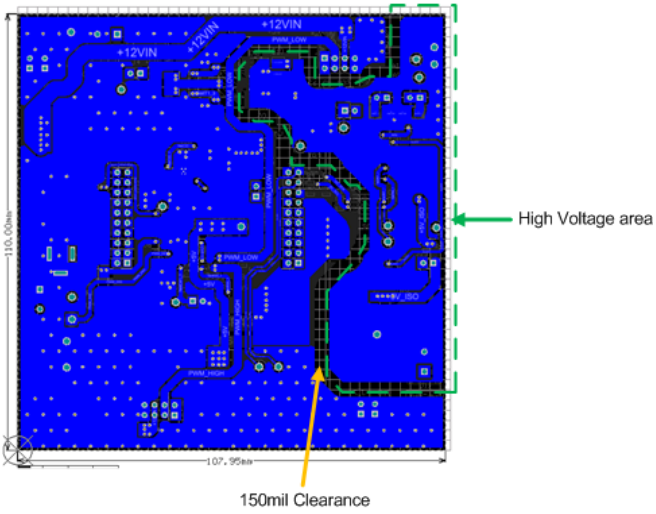


Figure 113. Bottom Layer

Figure 114 and Figure 115 show the route of the +12-V power rails on the top layer and the bottom layer. The rails are connected to the IGBT gate driver board through the connector.

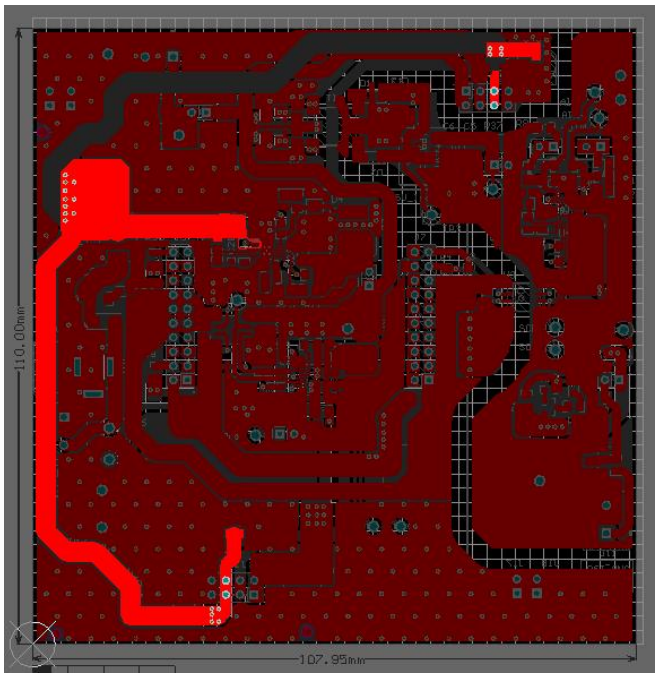


Figure 114. 12-V Power Rail on Top Layer

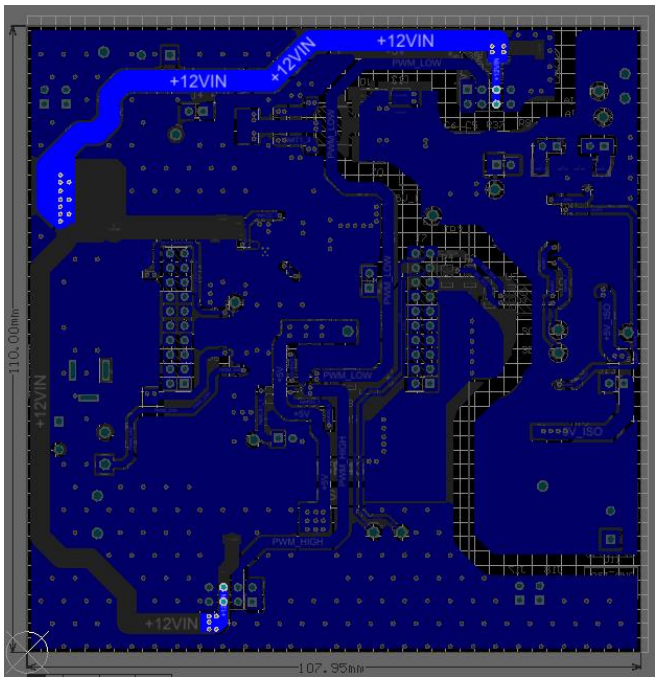


Figure 115. 12-V Power Rail on Bottom Layer

Figure 116 and Figure 117 show the route of the +5-V power rails on the top layer and the bottom layer. The rails are connected to the IGBT gate driver board through the connector.

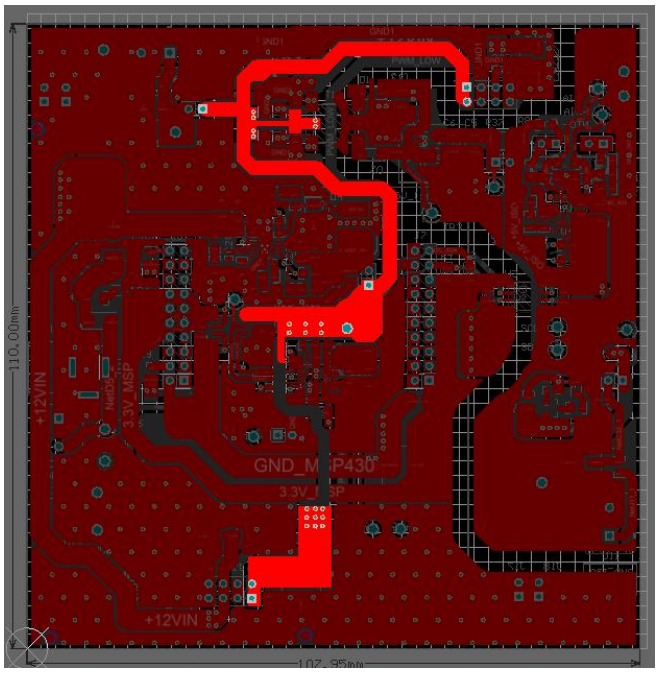


Figure 116. 5-V Power Rail on Top Layer

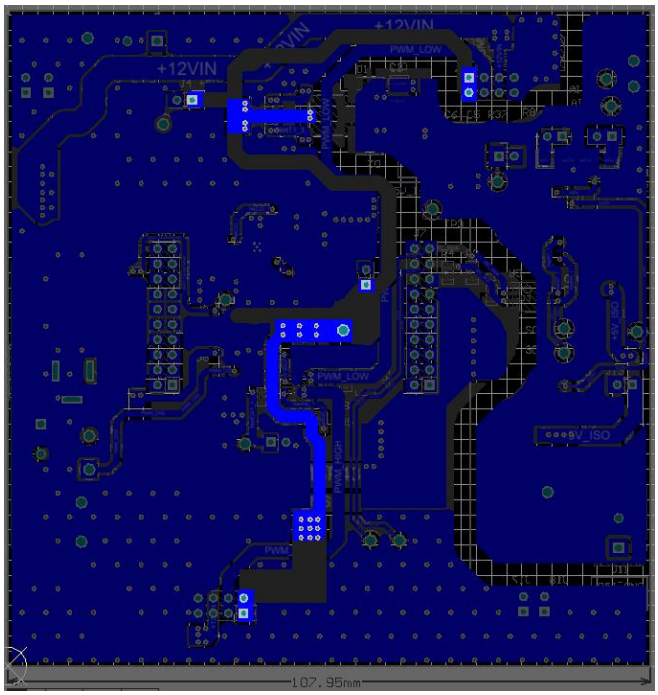


Figure 117. 5-V Power Rail on Bottom Layer

Figure 118 shows the PWM signal traces that are connected to the high-side and low-side gate drivers.

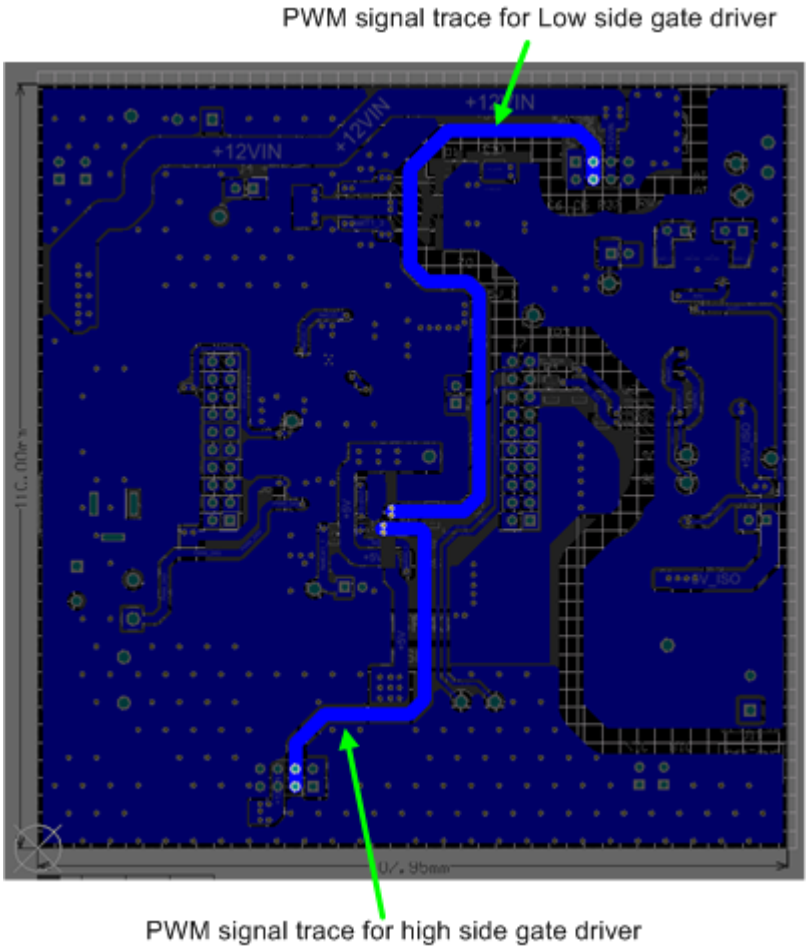


Figure 118. PCB Traces From PWM Signals to IGBT Gate Drivers

Figure 119 shows the placement of the input and output capacitors in the 12-V to 5-V step-down converter.

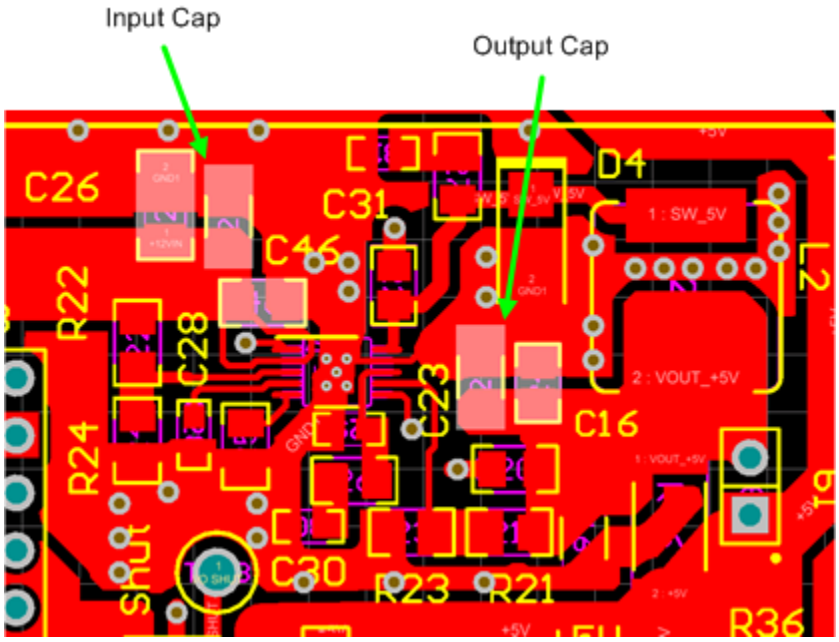


Figure 119. Placement of Input and Output Capacitors

Figure 120 shows the placement of the input capacitors and the output components in the 5-V, push-pull, isolated power supply.

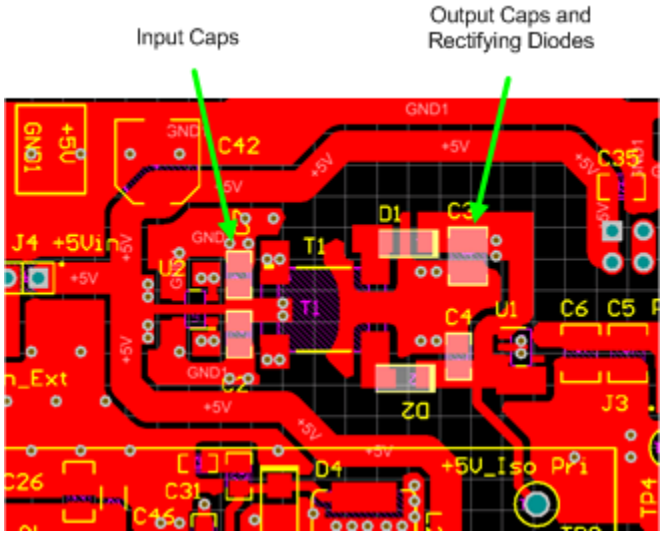


Figure 120. Placement of Input Capacitors and Output Components

Figure 121 shows the placement of the RC filter and the ADS1015-Q1.

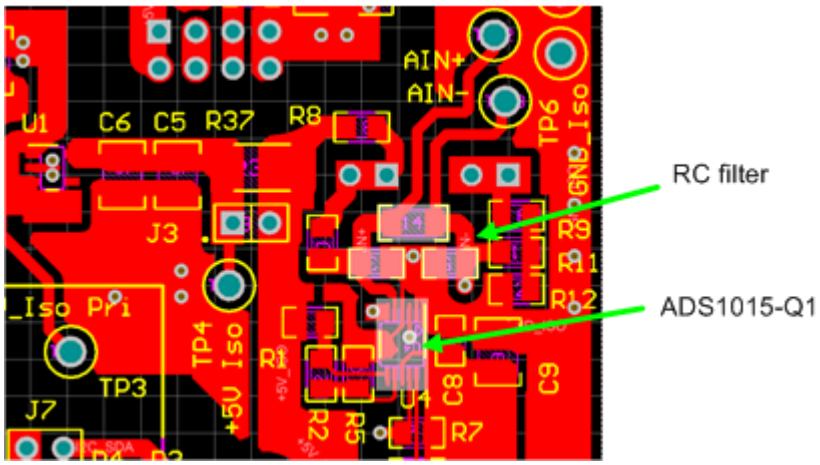


Figure 121. Placement of RC Filter and ADS1015-Q1

4.4 Altium Project

To download the Altium project files, see the design files at TIDA-00794.

4.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00794.

4.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00794.

5 Software Files

To download the software files, see the design files at TIDA-00794.

6 References

1. Infineon, *EasyPACK module with Trench/Fieldstop IGBT3 and Emitter Controlled 3 diode and PressFIT / NTC*, Data Sheet (B31A)
2. Texas Instruments, *Dual Isolated Outputs Fly-Buck Power Module Reference Design for Single IGBT Driver Bias*, Tools Folder (PMP10654)
3. Texas Instruments, *Passing CISPR25-Radiated Emissions Using TPS54160-Q1*, Application Report (SLVA629)
4. Texas Instruments, *TPS54xx0-Q1 and TPS57xx0-Q1 Design Calculation Tool*, Tools Folder (TPS54-57XX0-CALC)
5. WÜRTH, *TRANSFORMER*, Data Sheet (750315445)
6. WÜRTH, *TRANSFORMER*, Data Sheet (760390014)

7 Terminology

AFE— Analog front end

BJT— Bipolar junction transistor

CMTI— Common-mode transient immunity

DESAT— Desaturation

IGBT— Insulated gate bipolar transistor

LDO— Low-dropout regulator

MCU— Microcontroller unit

MOSFET— Metal-oxide-semiconductor field-effect transistor

NTC— Negative temperature coefficient thermistors

PCB— Printed Circuit Board

PWM— Pulse width modulation

TVS— Transient voltage suppression

UVLO— Undervoltage lockout

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9 About the Author

XUN GONG is an Automotive Systems Engineer at Texas Instruments where he is responsible for developing reference design solutions for the automotive segment in Power Train applications. Xun brings his extensive experience in IGBT gate drivers, SiC (Silicon Carbide) transistor gate drivers, IGBT temperature sensing, EMC in motor drive applications, and DC-DC converters to this role. Xun achieved his Ph.D. in Electrical Engineering from Delft University of Technology in Delft, Netherlands. Xun won the First Prize Paper Award of the IEEE Transactions on Power Electronics in 2014.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (March 2016) to A Revision	Page
• Changed from first page preview	2

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