TI Designs

Interface to a HIPERFACE Position Encoder

TI Designs

This design implements an EMC-compliant industrial hybrid analog and digital interface to a HIPERFACE position encoder. A 3.3-V supply RS-485 transceiver with IEC-ESD and IEC-EFT protection is used for the bidirectional parameter channel. For the analog sin/cos signal channel, two options are provided to offer flexibility for connection to processors with and without embedded ADC. The first option features a fully differential dual 12-bit ADC with SPI output, and the second option features a dual differential input with a single-ended analog output (0 to 3.3 V). The design features an industrial compliant 24-V input with a wide range from 16 to 36 V. The power supply for the encoder can be configured from 7 to 12 V (default 11 V) and offers short-circuit protection. A 3.3-V I/O connector with analog and logic signals provides an easy interface to a host processor with HIPERFACE master IP core. For quick evaluation, an example firmware is available for a C2000™ Piccolo™ MCU to calculate the absolute angle position and display it through virtual COM port.

Design Resources

TIDA-00202	Tool Folder Containing Design Files
SN65HVD72	Product Folder
ADS7254	Product Folder
THS4531A	Product Folder
OPA2365	Product Folder
TLV3202	Product Folder
TPS5401	Product Folder
C2000 Piccolo F28069M MCU LaunchPad	Tools Folder

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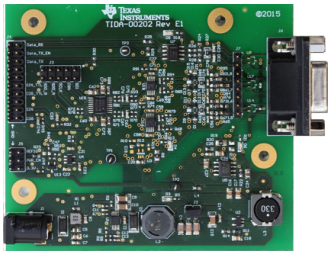
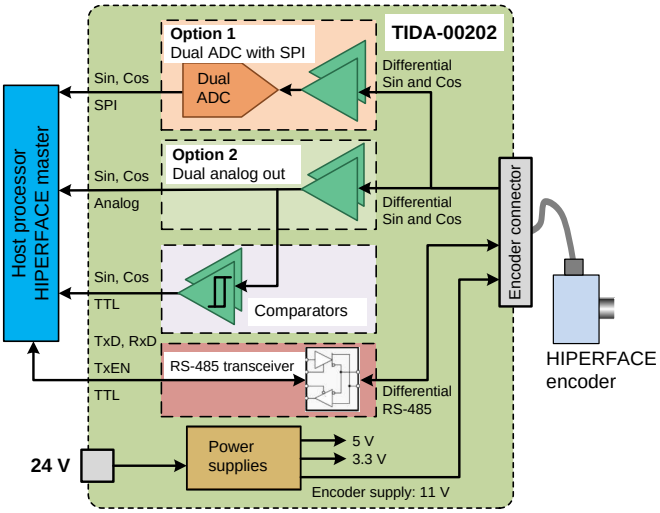


Design Features

- EMC-Compliant Interface to HIPERFACE Position Encoders With Digital Bidirectional Parameter Channel up to 38400 Baud and Analog Sin/Cos Channel With at Least 150-kHz Bandwidth
- 3.3-V Supply Half-Duplex RS-485 Transceiver With 12-kV IEC-ESD and 4-kV IEC-EFT
- Dual Signal Path Option for Sine and Cosine Signals With Wither Dual 12-bit ADC With SPI Output or Dual Analog Output (0 to 3.3 V) to Offer Flexibility for Connection to MCU With and Without Embedded ADC
- Host Processor Interface (3.3-V I/O) for Easy Connection to MCU Like C2000 for HIPERFACE Master
- Example Firmware on C2000 Piccolo MCU to Calculate and Display the Interpolated Absolute Angle From HIPERFACE Position Encoders
- Designed to Meet EMC Immunity for ESD, Fast Transient Burst, and Surge With Levels According to IEC61800-3

Featured Applications

- Servo Drives
- Industrial Drives
- Factory Automation and Control



1 System Description

This TI Design implements an industrial temperature and EMC-compliant interface to a HIPERFACE position encoder. The major building blocks of this TI Design are the hybrid interface for the bidirectional parameter channel, a dual-channel option for the analog sine and cosine process data signals, and the HIPERFACE-compliant encoder power supply with an enable signal through MCU.

A simplified system block diagram of a servo drive with a HIPERFACE master interface to a HIPERFACE encoder is shown in Figure 1 with the TI Design represented by the box in light green. To evaluate and test the TI Design TIDA-00202, a basic HIPERFACE master firmware was implemented on the C2000 Piccolo MCU This firmware is only showing basic HIPERFACE functionality for test purposes and provided in binary format.

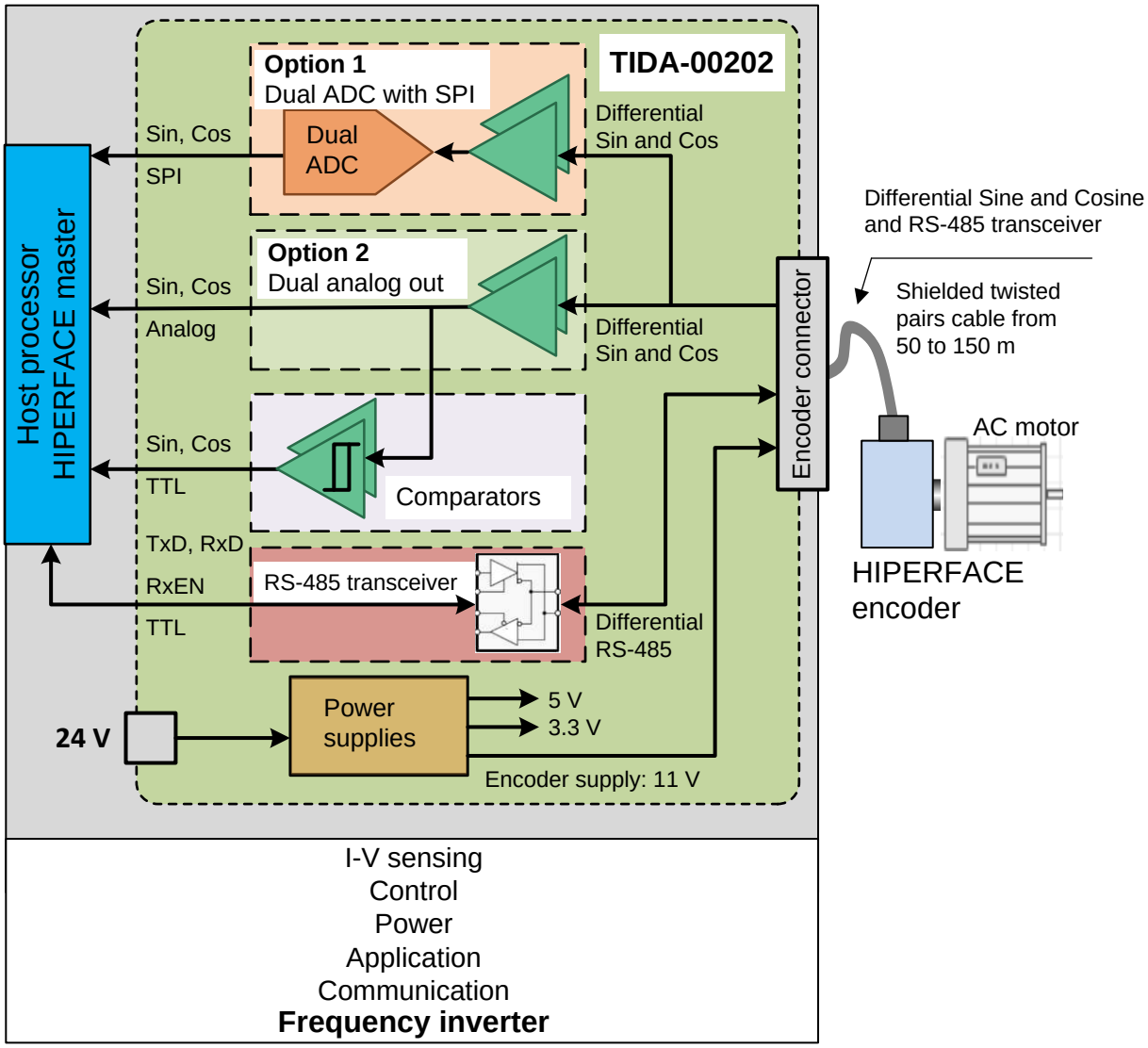


Figure 1. Simplified Block Diagram of TIDA-00202

The reference design connects to the HIPERFACE encoder through a Sub-D9 connector. The Sub-D9 connector has been tested to support cable lengths up to 100 m. For cable specifications, refer to the HIPERFACE standard.

The reference design is powered through a standard 24-V DC rail as typically used in drives. DC/DC buck converters generate two intermediate rails. These rails are used to generate the point of load 5-V and 3.3-V rails to supply the RS-485 transceiver and the analog signal chain, as well as the 11-V rail to supply the HIPERFACE encoder.

A dual option is provided for the analog process channel to provide flexibility select the processor to implement the HIPERFACE master. The first option offers an analog signal chain for processors with embedded dual ADC. The second option leverages a dual 12-bit ADC with SPI for processors without embedded dual ADC. Both channels can also be used in parallel to for additional redundancy or bandwidth optimization.

A 3.3-V compliant interface is provided to connect to a host processor to run the HIPERFACE master protocol as well as the signal processing for the sine and cosine signals.

The host processor interface provides the Data_IN, Data_OUT, and Data_EN signals for the digital parameter channel, an SPI with dual 12-bit data, and dual analog single-ended signals to support both processors with and without embedded ADCs as well as the quadrature encoded digital signals A and B for an incremental up-down counter.

1.1 Introduction to HIPERFACE

HIPERFACE is a digital protocol specified and owned by Sick. HIPERFACE is derived from **HI**gh **PER**formance Inter**FACE**. The key features of the HIPERFACE hybrid interface with reference to HIPERFACE specification from Sick are:

- Analog process data channel on which sine and cosine signals are transmitted differentially, with almost no delay
- Bidirectional parameter channel corresponding to the RS-485 specification for transmitting the absolute position information and various other parameters
- Only eight wires
- Cable length up to 100 m

1.1.1 HIPERFACE Physical Layer for the Digital Interface

The protocol is implemented with a standard UART interface, which can be found on the majority of the host processors.

As a physical layer, HIPERFACE uses a digital transfer in accordance with EIA-485 (RS-485). Valid RS-485 interface drivers must comply with the conditions in Table 1.

Table 1. HIPERFACE Transceiver Specifications

CHARACTERISTIC	VALUE
Transfer rate	0.6 to 38.4 kBaud (default 9.6 kBaud)
Permitted common-mode voltage	–7 to 12 V
Termination impedance	130-Ω termination with 1k resistor to GND

1.1.2 HIPERFACE Physical Layer for the Analog Sin/Cos Interface

Incremental rotary or linear position encoders are used in many applications to measure angular or linear position and speed. Depending on the application, encoders with TTL/HTL output signals or analog sinusoidal output signals are used. The latter is often referred to as sin/cos encoders. Analog sin/cos incremental encoders enable high-resolution position measurement. The high quality of the sinusoidal incremental signals permits high interpolation factors for digital speed control.

For more details on how to calculate the angle using the sin/cos and TTL signals, see the TIDA-00176 or TIDA-00178 reference design.

As a physical layer, HIPERFACE uses a differential analog sin/cos signal. A valid analog interface must comply with the conditions in Table 2.

Table 2. Analog HIPERFACE Signal Chain Specifications

CHARACTERISTIC	VALUE
Minimum ADC resolution	10 bit
ADC channel need	2 channels
Differential signal amplitude (peak-to-peak)	0.9 to 1.1 V_{PP}
Average signal voltage	2.0- to 3.0-V DC
Signal bandwidth (3-dB signal amplitude)	0 to 150 kHz
Output load capacity (current)	≥ ±7 mA

1.1.3 HIPERFACE Encoder Supply Voltage

Motor feedback systems with HIPERFACE have been developed to operate with a supply voltage of 7 to 12 V. The voltage supply is measured at the encoder plug connector. The specification for the HIPERFACE power supply is listed in Table 3.

Table 3. Power Supply Specification

PARAMETER	VALUE
Operating supply voltage	7 to 12 V
Operating current	≤ 250 mA

2 Key System Specifications

As outlined in Section 1, this TI Design realizes an industrial temperature range, EMC-compliant interface to HIPERFACE position encoders with differential analog output signals sin/cos, a digital RS-485 UART interface, and a 11-V supply voltage. The major building blocks of this TI Design are the dual path analog signal chain with the low propagation delay comparator block, the RS-485 interface, the power management block, the interfaces to the HIPERFACE encoder, and the interface to a host microcontroller for running the HIPERFACE master including digital signal processing and high-resolution position calculation.

To evaluate this TI Design with ease, an example firmware is provided for the TMS320F28069M InstaSPIN-MOTION™ LaunchPad™. The TMS320F28069M calculates the high-resolution angle position for both signal paths, using both options simultaneously, which are the dual 12-bit ADC through SPI and the analog output path to the TMS320F28069 internal dual S/H 12-bit ADC. The TMS320F28069M also implements a basic HIPERFACE master to request absolute angle position through the RS-485 interface. A menu is made available through a USB virtual COM port to display the high-resolution interpolated angle, the absolute angle through the digital parameter channel, and more.

TIDA-00202 features overview:

- EMC-compliant interface to HIPERFACE position encoders with digital bidirectional parameter channel up to 38400 baud and analog sin/cos channel with at least 150-kHz bandwidth
- Dual-signal path option for sine and cosine signals with onboard differential dual 12-bit simultaneous sampling ADC with SPI or dual analog output (0 to 3.3 V) to offer flexibility for connection to MCU with and without an embedded ADC
- Low propagation delay comparators with adjustable 160-mV hysteresis for better noise immunity to convert the analog signals sin and cos to 3.3-V TTL signals
- 3.3-V supply half-duplex RS-485 transceiver with 12-kV IEC-ESD and 4-kV IEC-EFT
- Host processor interface (3.3-V I/O) for easy connection to MCU like C2000 for the HIPERFACE master
- Example firmware on C2000 Piccolo MCU to calculate and display the interpolated absolute angle from HIPERFACE position encoders
- Designed to meet EMC immunity for ESD, fast transient burst, and surge with levels according to IEC61800-3

2.1 HIPERFACE Encoder Interface

The design offers either a shielded Sub-D9 female connector to connect to a HIPERFACE encoder or an 8-pin header connector to interface to the HIPERFACE encoders.

Table 4. HIPERFACE Encoder Interface

PARAMETER	TYPICAL VALUE	COMMENT
Encoder supply voltage	11 V (±5%), 250 mA	11 V was chosen for additional margin to compensate for voltage drop over longer cables w/ smaller gauge. Adjustable to, for example, 8 V through feedback resistor change
Analog input signals	SIN+, SIN–, COS+, COS–	130-Ω differential line termination with 1k PD resistor to GND and 1k PU to VCC
Input level and common mode voltage range for Sin+, Sin–, Cos+, Cos–	0.9- to 1.1 V_{PP} 2.0- to 3.0-V DC common mode	
Digital input signals	RS-485	130-Ω differential line termination with 1k resistor to GND and VCC (effective 121-Ω termination)

2.2 Analog Sin/Cos Signal Path

The analog process channel for the Sin/Cos signal offers two options: Option 1 features a 12-bit dual ADC with SPI output, and option 2 features dual single-ended analog output signals with 1.65-V DC offset.

Option 1 for signals SIN+, SIN– and COS+, COS– features a fully differential signal path with a dual 12-bit simultaneous sampling ADC with differential input and SPI output. The main features of this functional block are outlined in Table 5.

Table 5. 12-Bit Dual ADC With SPI Output

PARAMETER	TYPICAL VALUE	COMMENT
Gain (Sin, Cos)	5.0 (0.1%)	Adjustable, 0.1% resistors recommended. Assumes the input inductors L5-L8 (47 µH) are bypassed (0 Ω).
Offset (Sin, Cos)	< 1 mV	Un-calibrated
Offset Drift (Sin, Cos)	< 2 µV/°C	
Bandwidth (–3 dB)	≥ 150 kHz	
Quantization	12-bit	FSR = ±5 V (ADS7254) Drop-in compatible 14- or 16-bit versions available.
Sampling frequency	Up to 1 MSPS	
Data output format (Sin, Cos)	12-bit 2's complementary	
Serial interface (SPI slave)	3.3 V, up to 24-MHz SPI clock	Dual 16-bit data per SPI frame

Option 2 for the signals SIN+, SIN–, and COS+, COS– offers a single-ended analog output for sine and cosine with a 1.65-V bias voltage to interface to an embedded dual S/H ADC, which is for example integrated into microcontrollers like the C2000 Piccolo.

Table 6. Single-Ended Sin/Cos Analog Output

PARAMETER	TYPICAL VALUE	COMMENT
Single-ended analog output (Sin, Cos)	0 to 3.3 V, 1.65-V bias voltage	
Gain (Sin, Cos)	1.67 (0.1%)	Adjustable, 0.1% resistors recommended. Assumes the input inductors L5-L8 (47 µH) are bypassed (0 Ω).
Offset (Sin, Cos)	< 2.5 mV	Un-calibrated
Offset drift (Sin, Cos)	< 6 mV (within –40°C to 85°C)	Mainly determined by TLV431. For tighter spec, use, for example, REF2033
Bandwidth (–3d B)	~150 kHz	Adjustable LP filter for bandwidth adjustment. Assumes the input inductors L5-L8 (47 µH) are bypassed (0 Ω).

The comparator block features high-speed, low propagation delay comparators with adjustable ±80-mV hysteresis for better noise immunity and converts the analog signals sin and cos to 3.3-V TTL.

Table 7. Comparators

PARAMETER	TYPICAL VALUE	COMMENT
Digital output signals (Sin, Cos)	3.3-V TTL	
Hysteresis	~160 mV (±80 mV)	For increased noise immunity, adjustable through feedback resistor change
Propagation delay	~40 ns	Low propagation delay w/o hysteresis
Maximum phase delay (propagation delay and hysteresis)	< 30°	at 1 V_{PP}, 150-kHz input

2.3 Digital Parameter Channel

For the RS-485 transceiver to implement the digital parameter channel, the transceiver must meet at least the following specifications.

Table 8. RS-485 Transceiver Specification

PARAMETER	TYPICAL VALUE	COMMENT
Baud rate	600 Baud to 38.4 kBaud	UART interface
Digital I/O transmit (DATA_TX, DATA_TX_EN)	3.3-V TTL	With enable signal
Digital I/O receive (DATA_RX)	3.3-V TTL	Always enabled

2.4 Host Processor Interface

The host processor interface provides digital and analog signals at 3.3-V I/O. The digital interface signals specification is shown in Table 9:

Table 9. Digital Interface to Host Processor

PARAMETER	TYPICAL VALUE	COMMENT
SPI	3.3-V TTL	Up to 24-MHz SPI clock
eQEP signals	3.3-V TTL	No Index signal
RS485 signals	3.3-V TTL	TX, RX, and TX_EN

The analog signal specification is shown in Table 10:

Table 10. Analog Interface Signals to Host Processor

PARAMETER	TYPICAL VALUE	COMMENT
Analog single-ended	0 to 3.3 V, 1.65-V bias, gain =1.67	

2.5 Power Management

This TI Design features a 24-V DC input with a wide input voltage range from 17 to 36 V and reverse polarity protection. The onboard power management features a DC/DC buck, which generates an intermediate 12-V rail. An LDO is used to generate the 11-V encoder supply. A second DC/DC buck generates the 5-V rail. Another LDO then generates the 3.3-V rail.

The 11-V encoder supply features an LDO with thermal shutdown and an enable pin. Due to this, the HIPERFACE encoder supply voltage can be turned off through the host processor, if desired.

Table 11. Power Management

PARAMETER	VOLTAGE	CURRENT	COMMENT
Input voltage	24 V (17 to 36 V)	150 mA	Wide input voltage with reverse polarity protect
Intermediate rail	12 V (±5%)	500 mA	Intermediate rail. High-efficiency (> 80%) DC/DC buck power supply
Encoder supply	11 V (±5%)	250 mA	11 V was chosen for an additional margin to compensate for voltage drop over longer cables. Adjustable to, for example, 9 V through feedback resistor change
5-V supply	5 V (±5%)	400 mA	Analog signal chain supply (dual ADC, op amps)
3.3-V supply	3.3 V (±5%)	100 mA	Digital signal chain supply (RS-485, comparators)

2.6 Evaluation Firmware

To quickly evaluate the TIDA-00202 design, an example firmware for Piccolo F28069M MCU is provided, where the interpolated angle is calculated for both the 12-bit dual ADC ADS8354 and the F28069M MCU's embedded dual S/H 12-bit ADC. A user interface through USB virtual COM port at 115000 baud allows for easy performance evaluation.

The user interface through virtual COM port at 115000 baud supports the following features:

- Selection of HIPERFACE encoder line count: up to 32000
- Hardware and software synchronized sampling of the external dual sampling 12-bit ADC through SPI, the internal 12-bit dual S/H ADC, and the incremental counter
- High-resolution angle in 32-bit, fractional Q28 format. Angle scaled per unit from 0 to 0.9999999, up to 28-bit interpolated angle resolution
- Automatic absolute position initialization during initialization using the parameter channel of HIPERFACE
- Menu to support display mode or data dump mode at 10-Hz update rate for total interpolated angle, incremental angle, and phase with both, the 12-bit dual ADC (ADS7254) on the TIDA-00202 design, and the C2000 Piccolo MCU's on-chip 12-bit dual S/H ADC
- Diagnostic error message when encoder is not connected or when differential input voltage is below 0.3 V_{PP}

2.7 EMC Immunity

The TIDA-00202 is designed to meet ESD, EFT, and surge requirements per IEC61000-4-2, 4-4 and 4-5 with levels specified in the IEC 61800-3 standard "EMC immunity requirements for adjustable speed, electrical-power drive systems". It is assumed only the SubD-9 connector to the position encoder can be accessed, and shielded encoder cables are used to connect to the encoder. Because the encoder cable can exceed 30 m, ESD, EFT, and Surge apply per Table 12 for use in environment 2.

Table 12. EMC Immunity Requirements

PORT	PHENOMENON	BASIC STANDARD	LEVEL	PERFORMANCE (ACCEPTANCE) CRITERION
HIPERFACE encoder interface connecter	ESD	IEC61000-4-2	±4-kV CD or 8-kV AD, if CD not possible	B
	Fast transient burst (EFT)	IEC61000-4-4	±2 kV/5 kHz, capacitive clamp	B
	Surge 1.2/50 µs, 8/20 µs	IEC61000-4-5	±1 kV. Since shielded cable > 20 m, direct coupling to shield (2-Ω source impedance)	B

The performance (acceptance) criterion is defined as follows:

Table 13. Performance (Acceptance) Criterion

PERFORMANCE (ACCEPTANCE) CRITERION	DESCRIPTION
A	The module shall continue to operate as intended. No loss of function or performance even during the test
B	Temporary degradation of performance is accepted. After the test, the module shall continue to operate as intended without manual intervention.
C	During the test, loss of functions accepted, but no destruction of hardware or software. After the test, the module shall continue to operate as intended automatically, after manual restart, or power off, or power on.

3 Block Diagram

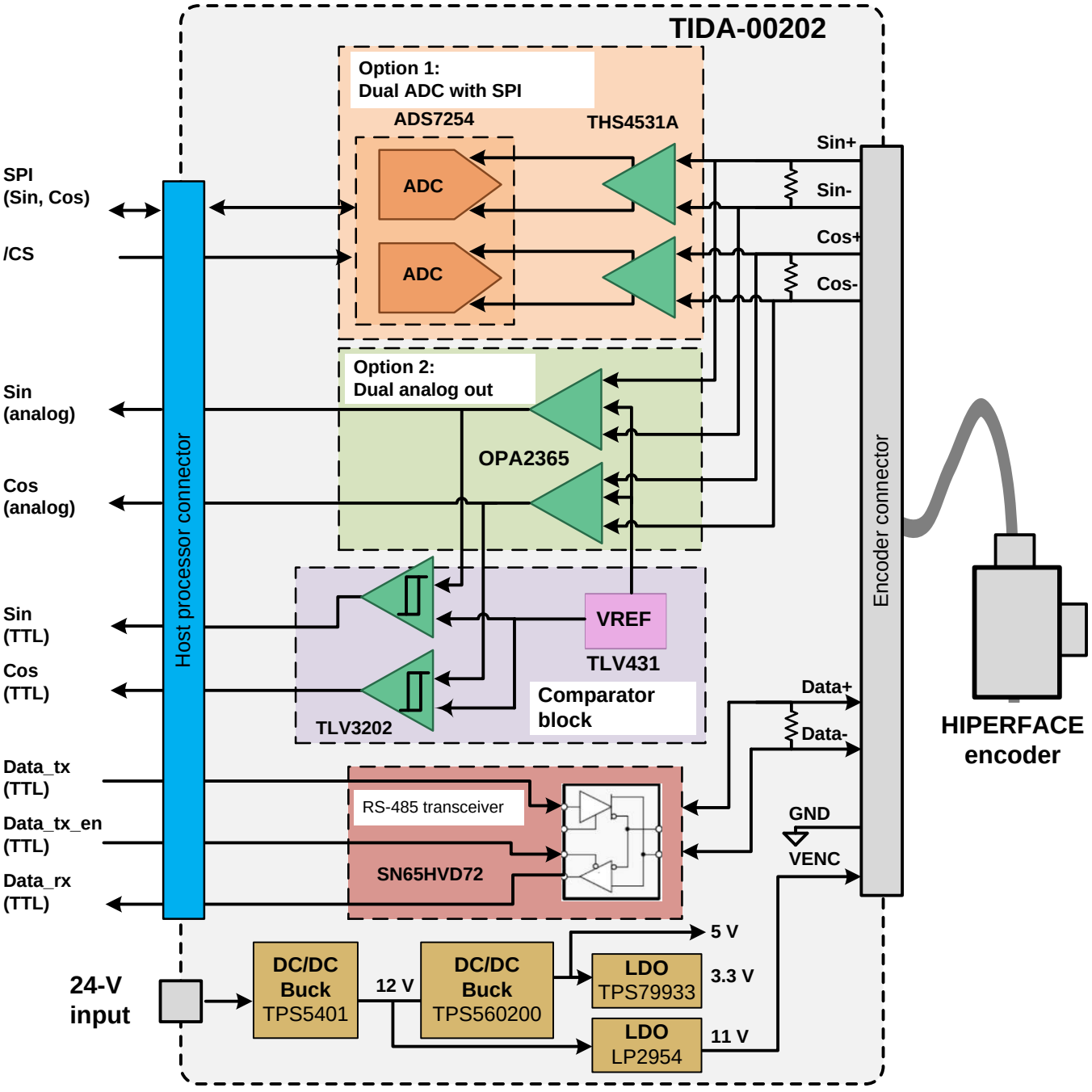


Figure 2. System Block Diagram of TIDA-00202

3.1 Highlighted Products

The following key products are used in this design with the key features highlighted.

3.1.1 ADS7254

The ADS7254 has been selected for the following reasons:

- Dual-channel, simultaneous sampling, with true differential inputs and dual or independent reference voltages to improve immunity against common mode noise
- High resolution (12-bit) with high precision (superb THD and SNR performance of –72-dB SNR, –90-dB THD)
- Drop-in pin-compatible 14-bit and 16-bit versions for flexibility pending required resolution versus cost optimization
- High speed (1 MSPS) and bandwidth to support at least 500-kHz analog input signals
- Sample point triggered by hardware (falling edge of /CS) allows host processor to precisely synchronize the sample point with the incremental counter latch.
- Dual, programmable, and buffered 2.5-V internal reference to provide common mode bias voltage to amplifier to almost cancel offset and offset drift-related errors
- Serial interface to host processor (dual data) with up to 24-MHz clock frequency to minimize latency
- Fully-specified over the extended industrial temperature range: –40°C to 125°C
- Small package

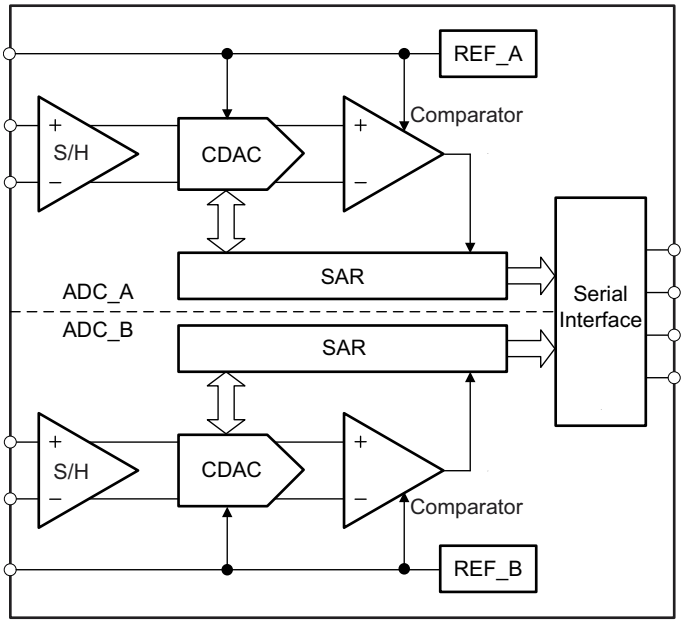


Figure 3. ADS7254 Block Diagram

3.1.2 THS4531A

To leverage the ADS7254 performance, the design requires a fully differential, high-speed amplifier with configurable output common mode voltage, like the THS45xx family.

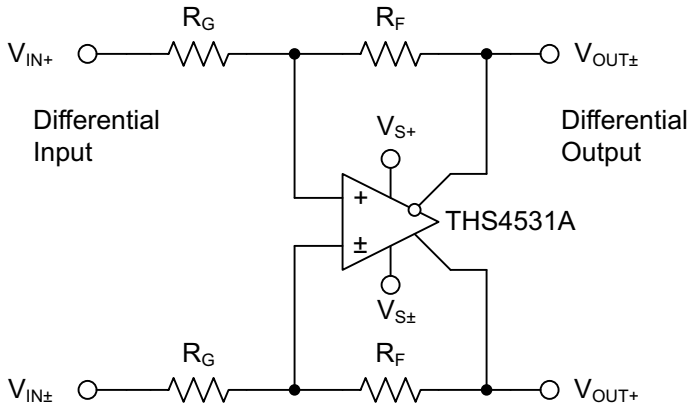


Figure 4. Differential Input to Differential Output Amplifier

The signal remains fully differential. The gain and optional filtering is defined by the input and feedback resistors and capacitors. The gain is set by the ration of R_F/R_G and the output common-mode voltage is set by the input signal V_{OCM}.

The THS4531A was chosen as it meets the topology and can drive the ADS7254. A single amplifier topology per package was used instead of the dual differential amplifier per package like the THS4532 for flexibility and easier PCB routing.

The key parameters of the THS4531A for use in this design are:

- Fully-differential architecture with adjustable output common-mode voltage
- High gain bandwidth: 27 MHz (6 MHz at G = 5)
- Low distortions, THD -120 dBc at 1 kHz (1 V_{RMS}, R_L = 2 kΩ)
- Low input voltage noise: 10 nV/√Hz (f = 1 kHz)
- Very low offset, V_{OS}: ±100 µV
- Very low offset drift, V_{OS} Drift: ±2 µV/˚C (industrial temperature range)
- Single 5-V supply to leverage same supply than ADS7254
- Rail-to-rail output (RRO) and negative rail input (NRI) to maximize input and output signal swing

3.1.3 OPA2365

For the input buffer and the differential to single-ended conversion, the OPA2365 has been selected due to:

- 2.2 to 5.5-V operation to leverage 5-V rail
- Rail-to-rail I/O
- Very low offset and offset drift: 200 µV (max) and 1 µV/K (typically)
- Low voltage and current noise: 4.5 nV/√(Hz) and 0.004 pA/√(Hz)
- Excellent THD+N: 0.0004%
- High common-mode rejection, CMRR: 100 dB (min)
- Slew rate: 25 V/µs
- Fast settling: 300 ns to 0.01% to drive external ADC

Other options include the OPA2322, which is a lower cost alternative, with 2-mV offset voltage and slightly reduced AC and DC performance.

3.1.4 TLV3202

The comparators selected are the TLV3202 (dual comparators), 40 ns, microPOWER, and push-pull output comparators with the following main characteristics:

- Low propagation delay of typical 40 ns
- Low input offset voltage of typical 1 mV to ensure minimum drift of switching threshold
- Push-pull outputs, to drive the input of a 3.3-V I/O host processor
- Industrial temperature range

3.1.5 SN65HVD72

The following parameters were considered regarding RS-485 transceivers:

- 3.3-V supply
- 3.3-V I/O with 5-V tolerant logic inputs
- Max 250 kBaud
- Large receiver hysteresis (80 mV) for improved noise rejection
- IEC61000-4-2 ESD (absolute maximum ratings): ±12 kV (contact discharge)
- IEC61000-4-4 EFT (absolute maximum ratings): ±4 kV

3.1.6 TLV431

The TLV431 is a low-voltage 3-terminal adjustable voltage reference with specified thermal stability over applicable industrial and commercial temperature ranges. Output voltage can be set to any value between V_{REF} (1.24 V) and 6 V with two external resistors. These devices operate from a lower voltage (1.24 V) than the widely used TL431 and TL1431 shunt-regulator references.

- Output voltage between 1.24 and 6 V using resistor divider
- Typical temperature drift 6 mV (–40°C to 85°C)
- Reference voltage tolerance 1.5%

The TLV431 is pin-to-pin compatible with the TLV431A, which has a better reference voltage tolerance and temperature drift between –40°C to 85°C.

3.1.7 TPS5401

The TPS5401 is a 42-V, 0.5-A, step-down regulator with an integrated high-side MOSFET. Current-mode control provides simple external compensation and flexible component selection. A low-ripple pulse-skip mode reduces the supply current to 116 µA when outputting regulated voltage with no load. Using the enable pin, the shutdown supply current is reduced to 1.3 µA when the enable pin is low.

- High efficiency at light loads with a pulse-skipping Eco-mode™ control scheme
- 3.5- to 42-V input voltage range
- 0.8-V ±3.5% internal voltage reference (device dependent)

The TPS5401 is pin-to-pin compatible with the following devices:

- TPS54040A with similar performance but more accurate output voltage and enable threshold
- TPS54140A, TPS54240, TPS54340, and TPS54540 with higher current options if more current are needed in different designs

4 Hardware Design

This section describes the different sub-modules of the complete design, explaining the choices made during the component and schematic process. The sub-modules explained are:

- Analog parameter channel signal chain
- Digital parameter channel signal chain
- Power supply
- Host processor interface

4.1 Analog Parameter Channel Signal Chain

For the analog signal chain, two optional paths are implemented:

- A fully differential signal path with digital SPI output, featuring fully differential amplifiers and fully differential dual 12-bit simultaneous sampling ADC with SPI output
- Dual analog differential input to single-ended analog dual outputs, to drive the comparator and connect to dual ADC for host processors with embedded ADCs

The dual analog path offers the option to either test the design with the onboard 12-bit dual path or use the analog differential to single-ended path with an MCU and embedded ADC. Additionally, since decoupled through a buffer from the high-resolution path, the analog path ensures ideal decoupling of the comparator path. This avoids crosstalk into the external analog path when switching output level during sine and cosine zero crossing.

Another use case would use both paths. One path for improved noise immunity with reduced bandwidth to filter out HF noise, while the other path would have offer standard bandwidth up to maximum speed. The lower bandwidth with improved noise immunity would be dedicated to the onboard 12-bit ADC, while the other path with standard bandwidth would be connected to the MCU with an embedded ADC.

The comparator subsystem will generate TTL level outputs for signals SIN and COS at a very low-propagation delay.

The following subsections explain each subsystem.

4.1.1 Option 1: Fully Differential Signal Path With Dual 12-Bit ADC With SPI

4.1.1.1 Input Signal Termination and Protection

Figure 5 shows the TIDA-00202 schematics of the input stage for the encoder's differential signals SIN and COS.

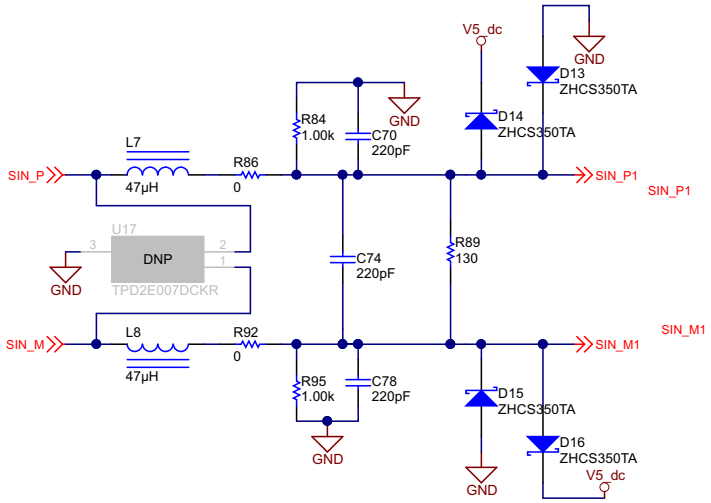


Figure 5. Termination for the Analog Inputs (SIN Input Shown)

The differential input signals are terminated with 130-Ω resistors each. Optional series 47-µH inductors are used for increased HF immunity along with around 120-kHz bandwidth.

Looking at the encoder signals SIN+/SIN– (named "SIN_P – SIN_M" in the schematic) signal conditioning block schematic from left to right, the following parts and functions can be distinguished:

- The series inductors L7 and L8 with 47 µH per HIPERFACE standard optional recommendation for high-frequency filtering. These are optional in this design and not recommended when accurate gain and minimum temperature related gain drift is mandatory.
- The HF noise suppression COG capacitors: C35, C38, and C41. For higher common-mode rejection, an additional 2-nF COG capacitor might be placed in parallel to the 220-pF capacitor from each differential input to GND.
- The impedance matching and termination resistor with parallel GND connection 130 Ω, 1k to GND: R89, R95, and R84
- Clamping diodes and op amp input protections (D13 to D16) to the 5-V rail and GND

4.1.1.2 Differential Amplifier THS4531A and 12-Bit ADC ADS7254

The two primary circuits, required to maximize the performance of a high-precision, successive approximation register (SAR) ADCs, are the input driver and the reference driver circuits. For details on selecting the amplifier, refer to Section 9.1 of the ADS7254 datasheet (SBAS556).

The THS4531A has been minded to work in combination with the ADS7254. The common-mode / DC-level of the input signal (2.5 V nominal) is provided to the THS4531A directly from the reference output of the ADS7254 itself to minimize potential offset and drift errors.

The differential input full-scale range (FSR) of the ADS7254 was configured to ±2 × V_{REF}. With the reference voltage of V_{REF} = 2.5 V, this yields a FSR of ±5 V. The maximum HIPERFACE encoder's differential input voltage is 1.1 V_{PP}. A voltage of higher than 1.35 V_{PP} should still be detected as a failure. A safety margin of 50% is added to the maximum peak-to-peak voltage, which is 1.8 V_{PP}. To match the ADC full-scale input range, the gain of the THS4531A should be 5.5. However, to remain in the linear output voltage range of the THS4531A at a 5-V supply, which is at least 0.25 to 4.8 V, the gain should be reduced by around 10%, hence the ideal differential amplifier gain would be 5.

To ensure a minimum gain error and especially drift between the channels, resistors with 0.1% accuracy and low temperature drift are needed. To minimize noise, the feedback resistors should be chosen in the lower kΩ range.

Due to the gain of 5, a typical 1-V_{PP} input signal leverages around 50% of the ADC FSR, which results in a loss of 1-bit of precision, hence yielding equivalent 11-bit resolution.

Figure 6 shows the schematics of the ADC with SPI signal path, the gain setting resistors are R66, R68, R79, R80, R83, R85, R94, and R96.

The parallel 220-pF feedback capacitors C57, C67, C68, and C79 were chosen for a 150-kHz (–3-dB) bandwidth.

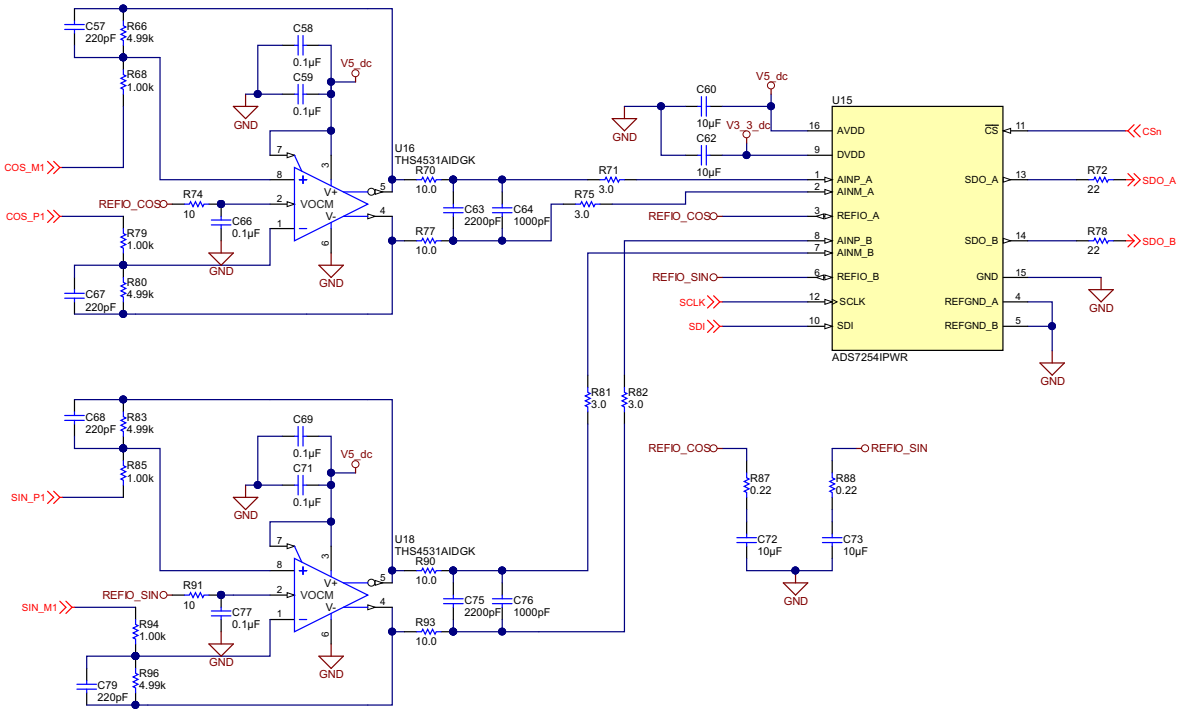


Figure 6. SIN and COS Signal Chain With Dual THS4531A and ADS7254

NOTE: The SIN input is connected to the ADS7254 channel B and the COS input to channel A for optimum performance layout and minimum numbers of vias.

The series 10-Ω resistors R70, R77 and the 2.2-nF and 1-nF capacitors C63, C64 (R90, R96, C75, and C76 for ADS7254 channel B) from the anti-aliasing filter. The filter capacitor C63 and C64 (C75 and C76), connected across the ADC inputs, filters the noise from the front-end drive circuitry, reduces the sampling charge injection and provides a charge bucket to quickly charge the internal sample-and-hold capacitors during the acquisition process. As a rule of thumb, the value of this capacitor should be at least 10 times the specified value of the ADC sampling capacitance. For these devices, the input sampling capacitance is equal to 40 pF. The capacitor should be a COG- or NPO-type because these capacitor types have a high-Q, low-temperature coefficient, and stable electrical characteristics under varying voltages, frequency, and time. To avoid amplifier stability issues, 10-Ω series isolation resistors R70, R77 (R90, R96) are used at the output of the amplifiers. For details, refer to the section 9.1 of the ADS7254 datasheet (SBAS556).

To minimize the impact of an offset drift of the ADC reference REFIO_SIN and REFIO_COS, the ADC references are used to bias the common-mode output voltage of the THS4531A. To buffer and decouple the VOCM signal at the THS4531A, small RC filters R74/C66 and R91/C77 R87, R88, C72, and C73 are added close to each pin.

The ADS7254 reference voltages REFIO_A and REFIO_B are decoupled with a 10-µF capacitor C72 and C73, respectively, and a 0.22-Ω resistor is added in series to avoid high-frequency oscillations.

To optimize the layout for cross-talk with minimum use of vias for the critical signals SIN+, SIN– and COS+, COS–, the following connections have been made:

1. The differential input signal SIN (SIN+, SIN–) has been inverted at the input of the THS4531A and again inverted by connecting to the ADS7254 input channel AINM_B and AINM_P.
2. The differential output signal of the THS4531A, COS+ and COS–, have been connected to the ADS7254 input pins AINP_A to COS– and AINM_A to COS+.

This results in the following hardware relationship. The ADS7254 channel B equals the HIPERFACE encoder signal SIN. The ADS7254 channel A equals the HIPERFACE encoder signal COS.

The configuration of the ADS7254 registers through serial interface is explained in Section 4.3.

4.1.2 Option 2: Analog Signal Path With Single-Ended Output for MCU With Embedded ADC

The parallel analog signal path should not impact the high-resolution path and especially the differential amplifier. Therefore, the differential signals SIN+,SIN– and COS+,COS– are tapped off after the input termination and protection and are buffered using unity gain amplifiers with very low offset and especially offset drift. The following amplifier should convert the differential signals into a single-ended signal. The minimum bandwidth should be least 150 kHz. The phase delay for the path to the comparator should be similar than the high-resolution path to ensure minimum phase lag.

The supply voltage should be a single supply of 5 V to support input common-mode voltages up to 3.5 V.

To match the high-resolution channel, the sum of the offset drift of both op amps should be at least 12-bit equivalent accuracy.

The analog output voltage should be scaled from 0 to 3.3 V with a 1.65-V common mode. Applying the same criteria in Section 4.1.1 with a maximum 1.1-V_{PP} input voltage and a 20% margin with regards to the 3.3-V FSR, the max gain yields 1.67.

Figure 7 shows the analog signal chain for channel SIN. The channel COS is identical.

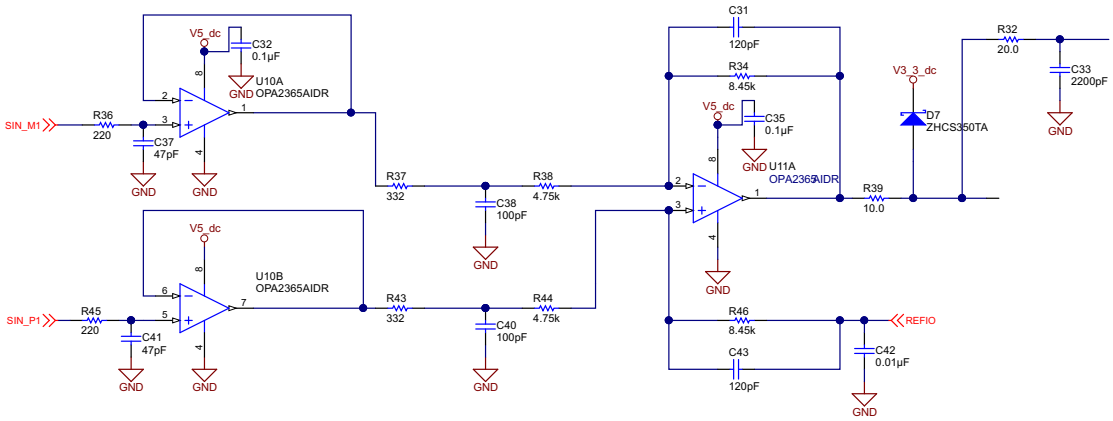


Figure 7. Analog Signal Path With Differential Input to Single-Ended Output for Signal SIN (Signal COS Not Shown)

The differential signals SIN_P and SIN_N are connected through a 220-Ω resistor to the non-inverting input of the OPA2365 (U10A and U10B). The OPA2365 (U10A and U10B) are configured as unity-gain buffer to avoid loading the source and introducing distortions. The 220-Ω series resistor limits the current into the non-inverting input of the OPA2365 in case of an over- or undervoltage event. The output of each buffer employs a small, adjustable RC-filter with, for example, R37 and C38 in Figure 7 with f_{-3dB} ~ 5 MHz for high-frequency noise reduction.

The following OPA2365 (U11A) is configured as differential to single-ended amplifier and level shifter. The gain is set to 1.67 and the output common-mode voltage to 1.65 V through a low-voltage adjustable precision shunt regulator TLV431. An adjustable 120-pF feedback capacitor is added in parallel to the 8450-Ω feedback resistor to low-pass filtering with a 150-kHz (–3-dB) bandwidth, ideally matched to the THS4531A bandwidth.

The 1.65-V bias voltage is decoupled with a 10-nF capacitor (C42) each.

Because the OPA2365 is supplied with 5 V, the output of the amplifier is clamped to 3.3 V (D7) with a series 10-Ω current limiting resistor (R39). This is to protect the following comparator (TLV3202) and an external ADC, which typically are 3.3-V FSR.

An anti-aliasing and decoupling RC network (R32/C33) is added to drive an external ADC. The filter was optimized for use with the embedded 12-bit dual S/H ADC in the C2000 Piccolo MCU family. For other ADCs, the filter has to be adjusted accordingly.

4.1.3 Comparator Subsystem for Digital Signals SIN and COS

The comparators are used to detect the zero-crossing of the analog signals SIN and COS and generate the corresponding digital 3.3-V TTL-compatible signals SIN_{TTL} and COS_{TTL}.

The TLC372 dual comparator with a 250-ns propagation delay is a lower cost option, depending overall system propagation delay and maximum frequency. It is normally sufficient for signals up to 150-kHz maximum frequency, as with the HIPERFACE encoder used in this design. However, the advantage of the TLV320x family is that it allows other components or the hysteresis to add more delay while still keeping the phase lag below 90 degrees (for example, 500 ns at a 500-kHz signal frequency). For example, a larger hysteresis would increase the propagation delay while improve immunity against noise.

4.1.3.1 Non-Inverting Comparator With Hysteresis Design

The input signals to all comparators are derived from the output of the single-ended to differential amplifier. The output signal is clamped to 3.3 V, as described in Section 4.1.2, and decoupled with an RC network (like R40 and C39 in Figure 8 for the SIN signal) to avoid crosstalk to the analog single-ended signals SIN and COS, respectively.

To match the phase between the high-resolution path and this path, the RC decoupling network at the input to the comparator matches the RC filter (2 × 10 Ω and 2.2 nF) at the THS4531A output.

The TLV3702 is configured as a non-inverting comparator to detect the zero-crossing of the analog sine and cosine signals, SIN and COS. Figure 8 shows the corresponding schematics for the signal SIN.

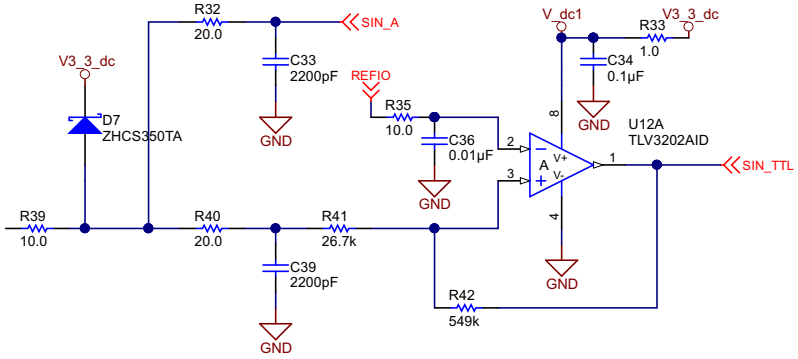


Figure 8. Comparator With Hysteresis for SIN Signal

The switching threshold is set by the reference voltage V_{REF} = 1.65 V (TLV431), which is also used to bias the single-ended analog signals for the differential to single-ended amplifiers. For each comparator, the reference input is taken from the TLV431and decoupled with a 10-Ω series resistor and a 10-nF capacitor.

A hysteresis is added for better noise immunity. The hysteresis ($V_{TH+} – V_{TH–}$) of a non-inverting comparator can be calculated per Equation 1:

$$V_{Hystereis} = \left(V_{Out\_High} - V_{Out\_Low}\right) \times \frac{R_G}{R_F} \quad (1)$$

with V_{Out_High} the high-level and V_{Out_Low} the low level comparator output voltage, R_F the feedback and R_G the input resistor into the non-inverting comparator input.

For the configuration of this design as outlined in Figure 8, the hysteresis has been set to around 160 mV per Equation 1. Since R39 and R40 are magnitudes lower than R41, they can be neglected.

$$V_{Hystereis} = 3.3\ V \times \frac{R41}{R42} \sim 160\ mV \quad (2)$$

The upper and lower switching thresholds V_{TH+} and V_{TH-} are defined per Equation 3 and Equation 4 with the reference voltage V_{REF} = 1.65 V.

$$V_{TH+} = 1.65\ V \times \left(1 + \frac{R41}{R42}\right) = 1.73\ V \quad (3)$$

$$V_{TH-} = (3.3\ V - 1.65\ V) \times \left(1 - \frac{R41}{R42}\right) = 1.57\ V \quad (4)$$

CAUTION

The lower threshold is a function of the supply voltage. However, the supply voltage tolerance of this design 5%, as typical with most designs. A ±5% tolerance with the 3.3-V supply voltage would affect the lower threshold by only by ±16 mV, resulting V_{TH-} range from approximately 1.56 to 1.59 V, hence still acceptable.

The 3.3-V supply of each comparator is decoupled with a 1-Ω series resistors and a 100-nF capacitor to minimize crosstalk through the 3.3-V rail to other comparators.

The hysteresis allows for a clean digital signal, meaning it avoids fast switching due to noise around the zero crossing point. The hysteresis, however, introduces an additional propagation delay, which depends on the analog signal amplitude $V_{IN\_PEAK-PEAK}$ at the comparator input.

$$\phi_{Hysteresis} \sim \sin^{-1}\left(\pm\frac{160\ mV}{V_{IN\_PEAK-PEAK}}\right) \quad (5)$$

Assuming a minimum input voltage of 0.9 V_{PP}, the output of the differential- to single-ended amplifier (gain = 1.67) will have an amplitude of 1.5 V_{PP} (0 to 10 kHz) and around 0.9 V_{PP} at 150 kHz due to low-pass filter attenuation. The hysteresis corresponding phase delay of the digital signals SIN and COS will be around 10 degrees for a 0.9-V_{PP} input at the comparator. At 150 kHz, this would translate into a total propagation delay of the comparator of around 190 ns + 40 ns =230 ns.

Due to the low propagation delay of the TLV3201 with only 40 ns, the overall delay of the comparator block remains well below 30 degrees up to 150 kHz and offers a sufficient margin for an additional phase lag due to tolerances and sample instant synchronization by the embedded processor.

The comparator for the COS signal has the same settings.

4.1.3.2 Comparator Subsystem Connected to THS4531A Output

For this design, the comparator subsystem was leveraging the differential-to-single-ended signal path for buffering and signal conditioning. For example, to connect the comparator subsystem to the differential signal path at the output of the THS4531A, refer to the TI Design TIDA-00178.

4.2 Digital Parameter Channel Signal Chain

When choosing the RS-485 for HIPERFACE, it is important to remember that the protocol is based on a UART protocol with a maximum baud rate of 38.4 kBaud and that HIPERFACE does not compensate for propagation delay. When HIPERFACE is implemented at maximum clock compared to cable length, the entire loop propagation delay (master and encoder) must not exceed 13 µs.

With this information, the SN65HVD72 was the chosen RS-485 device.

4.2.1 RS-485 Termination and Transient Protection

Figure 9 shows the RS-485 transceiver schematics for the digital parameter channel.

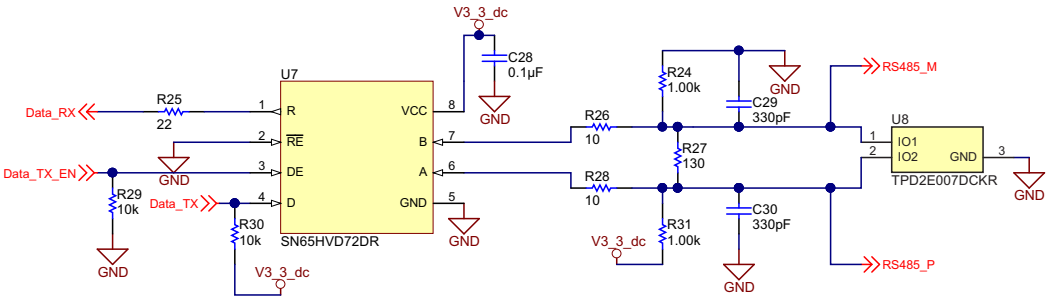


Figure 9. RS-485 Transceiver Configuration for HIPERFACE DATA+/DATA–

A single 130-Ω/0.4-W resistor was chosen as line termination resistor according to HIPERFACE specification.

A 10-Ω pulse-proof resistor is added into the SIN and COS bus lines if a transient voltage is higher than the specified maximum voltage of the transceiver bus terminals (see R26 and R28 in Figure 9). These resistors limit the residual clamping current into the transceiver and prevent it from latching up. In data receive mode, due to the low input current of the typical 240 µA, the voltage drop across the 10-Ω resistors is negligible. In data transmit mode, the voltage drop across both 10-Ω resistors is around 15%, which results in a slightly lower transmit differential voltage.

To further improve immunity against common-mode noise a 330-pF bypass capacitor is added from each differential RS-485 output DATA+ and DATA– to GND (see C29 and C30 in Figure 9).

The bus terminals of the SN65HVD7x transceiver family possess on-chip ESD protection against ±15-kV human body model (HBM) and ±12-kV IEC61000-4-2 contact discharge.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design. A complete list of layout guidelines can be found in the SN65HVD72 datasheet (SLLSE11). This design has especially implemented:

- V_{CC} and ground planes to provide low-inductance
- 100-nF bypass capacitors as close as possible to the V_{CC} pins of the transceivers and other digital logic
- At least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via inductance.

4.3 Power Management

Power management consists a DC/DC buck to generate a 12-V intermediate rail from the 24-V input voltage and a second DC/DC buck to generate the 5-V rail. The encoder supply voltage is derived from the intermediate 12-V rail. The 3.3-V rail is derived from the 5-V rail, as shown in Figure 10.

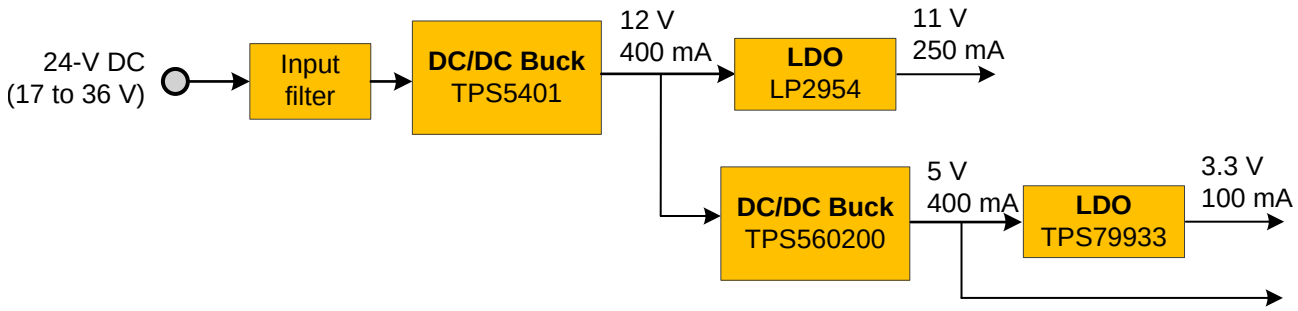


Figure 10. Power Management Subsystem

Because of the high performance required by the system and solution, most of the power rails are provided by low-noise LDOs. The drawback is the limited efficiency and low-output current capability. The maximum output current is limited by the thermal performance due to the high power losses.

A typical system would include the host processor for the HIPERFACE master (like a C2000 Piccolo MCU) on the same PCB. Therefore, the TIDA-00202 5-V intermediate rail was chosen to support at least 400 mA to provide sufficient current for the processor as well.

Minimize the noise introduced by both switcher solutions by proper layout and component selection.

4.3.1 24-V Input to 12-V Intermediate Rail

A switching DC-DC converter is provided to achieve the intermediate voltage rail of 12 V that supplies the encoder supply and the second buck converter. This is basically mandatory because the high V_{IN} / V_{OUT} ratio makes any LDO unsuitable for the power conversion.

The selected values for the input filter are shown in Figure 11. For more details about how to design an input EMI filter, see the application report *AN-2162 Simple Success With Conducted EMI From DC-DC Converters* (SNVA489).

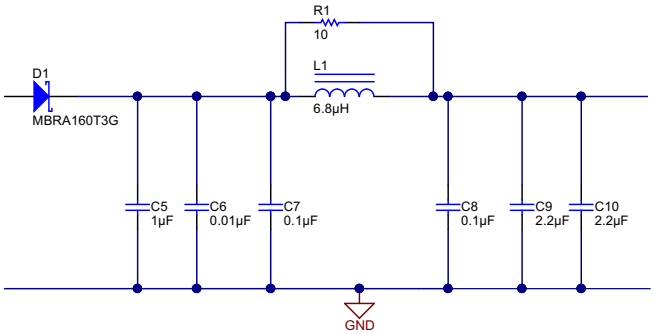


Figure 11. Input Filter Including Reverse Polarity Protection

The DC/DC buck converter has been designed to meet the following specifications:

- Input voltage: V_{IN} = 17 to 36 V, 24 V nominal
- Output voltage: 12 V at 500 mA
- Switching frequency: 500 kHz nominal
- Output voltage ripple: 25 mV_{PP} max
- Efficiency: > 80% at full load
- Non-isolated topology

The TPS5401 is selected because it is a buck converter with an integrated FET, a 3.5- to 42-V input voltage, and a 0.8- to 39-V output voltage at a 500-mA output current. Its frequency can be adjusted from 100 kHz to 2.5 MHz or can be synchronized with an external clock. It can also be enabled and disabled. The features of the TPS5401 fit these specifications well.

Note that the TPS5401 is pin-to-pin compatible with the TPS54040A, which is a higher cost version of the TPS54040A with similar performance but more accurate output voltage and enable threshold.

Also note that the TPS5401 is pin-to-pin compatible also with the TPS54140A, TPS54240, TPS54340, and TPS54540. This widens the part selection and offers flexibility to optimize the design with regards to power versus system cost.

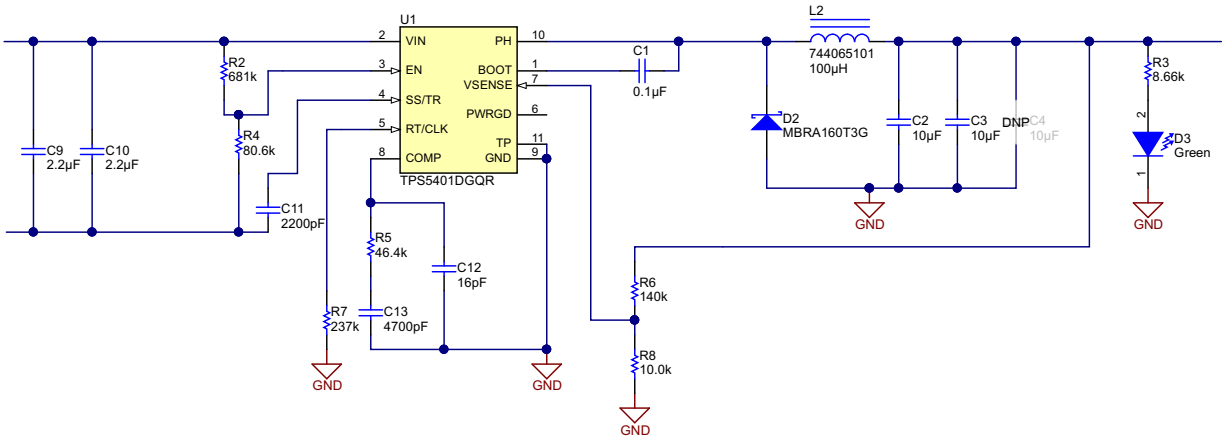


Figure 12. Schematic of 24-V to 12-V DC-DC Buck Converter With TPS5401

For a detailed explanation of the design process, see the TPS5401 datasheet (SLVSAB0) or the TIDA-00180 design guide (TIDU533), which shows the calculation for the TPS54040A.

The output voltage is set through R6 and R8 according to Equation 6:

$$R6 = 10\ k\Omega \times \left(\frac{12\ V - 0.8\ V}{0.8\ V} \right) = 140\ k\Omega \quad (6)$$

The tolerance of the output voltage is better than 5%. This assumes feedback resistors with a 1% tolerance and the internal bandgap tolerance from the TPS5401 of ±3.5%.

The switching frequency is set with R7 = 237 kΩ to 500 kHz.

4.3.2 11-V Encoder Supply

The design uses an LDO to achieve the 11-V encoder supply as the LDO has an enable pin to sequence with the 3.3-V rail of the digital power supply of the signal chain. This is done to ensure that the signal chain does not have signals on the pins from the encoder before the circuit is powered up.

The LDO LP2954 has the input and output voltage needed and can provide the wanted current. The A-version is not required due to the wide supply range of the HIPERFACE encoder.

The LP2954 has an enable pin and a thermal protection, which shuts down the LDO if a short on the power cables of the encoder happens. The LP2954 can also provide an error signal to alert an issue with the encoder.

The reference voltage of the LP2954 is 1.23 V; R22 is usually fixed to 100 kΩ. The output voltage is defined according to Equation 7.

$$R20 = R22 \times \left(\frac{11\,V - 1.23\,V}{1.23} \right) = 140\,k\Omega \tag{7}$$

With V_{OUT} = 11 V and R22 = 100 kΩ, R20 will be approximately 794 kΩ. 806 kΩ was chosen. This yields 11.14 V at the output.

The maximum power dissipation is 0.86 V × 250 mA = 215 mW with a junction-to-ambient thermal resistance is around 160°C/W. With 215 mW, the maximum junction temperature remains below 125°C at 85°C ambient.

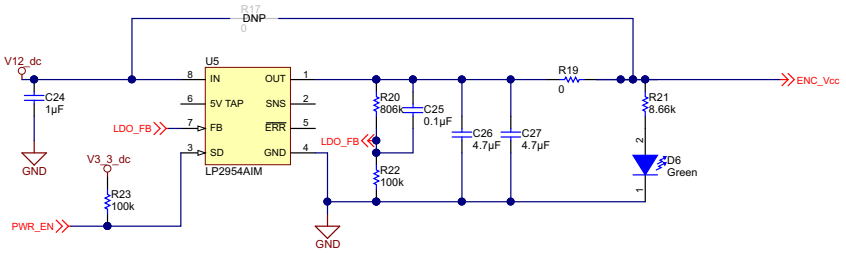


Figure 13. Schematic for 11-V Encoder Supply Rail

4.3.3 12-V Input to 5-V Intermediate Rail and Point-of-Load Supply

For the design, a 5-V and a 3.3-V rail is needed, as these rails supply a high-precision analog signal chain. A very low noise rail is needed. Here, an LDO would be ideal. Due to the same power considerations as the 11-V encoder supply, a 12-V to 5-V intermediate rail was done using the TPS560200.

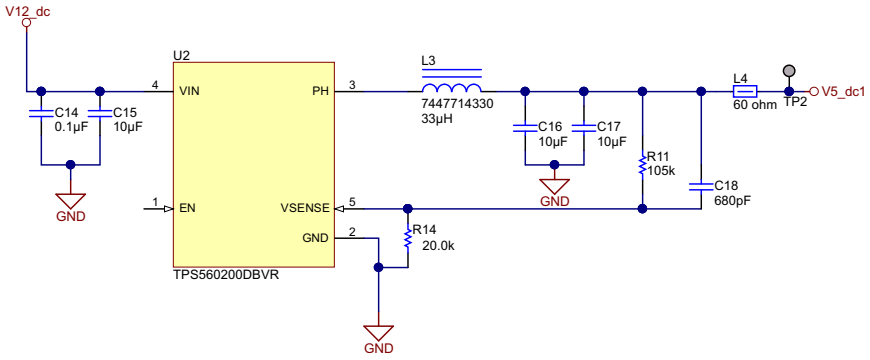


Figure 14. Schematic for 5-V Intermediate Rail

Calculate the output voltage with Equation 8.

The reference voltage of the TPS560200 is 0.8V, R14 is usually fixed to 20 kΩ.

$$R11 = R14 \times \frac{V_{OUT} - 0.8\ V}{0.8\ V} \tag{8}$$

With V_{OUT} = 6 V and R14 = 20 kΩ, R11 will be approximately 105 kΩ.

From the TPS560200 datasheet (SLVSC81), Equations 4 to 6 were used to calculate the peak and RMS current to decide which inductor and output capacitor to use.

Using these equations, a 33-µH inductor was chosen to ensure a low output voltage ripple. With the 33-µH inductor, the output capacitor was chosen to be around 6 µF to have the correct output filter for the TPS560200.

4.3.4 3.3-V and Optional 5-V Point-Of-Load Supply

Because of the relative low current (below 100 mA) demanded by the 3.3-V rail with the ultra-low power comparator TLV3202, the digital logic of the ADS7254, the SN65HVD72 RS-485 transceiver, and LDO was chosen for minimum BOM cost.

The 3.3-V rail is dedicated to the digital supply of the ADS7254 and the TLV3202 comparator to ensure a 3.3-V I/O interface to the host processor without the need for I/O level shifters. It is also dedicated to the RS-485 transceiver. Because of the low power consumption of the selected components, an LDO was selected for the 3.3-V and the 5V rail each with a nominal output current of 100 mA to minimize cost and BOM.

A fixed 3.3-V LDO TPS79933 was used for the 3.3-V rail.

The TPS71701 would have been fitted if a 14- or 16-bit ADC would have been used to ensure minimum noise on the 5-V supply rail. The 12-bit dual ADC ADS7254 an LDO was not required. The schematic is shown in Figure 15.

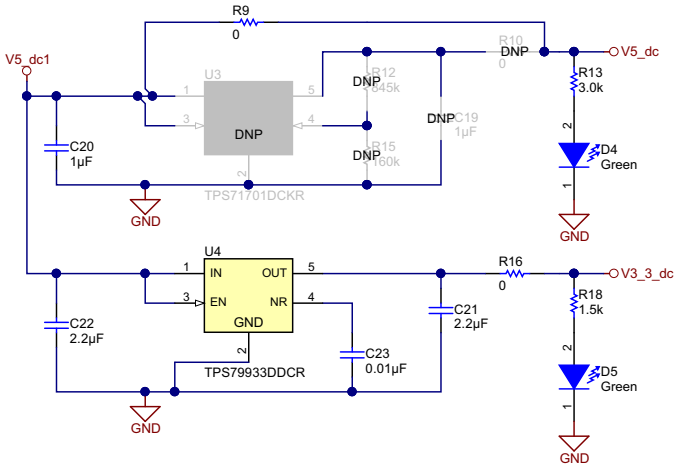


Figure 15. Schematic for 5-V and 3.3-V PoL for Signal Chain

4.4 Host Processor Interface

4.4.1 Signal Description

A 20-pin header and a 10-pin header interface are available to connect to a host processor. The headers provide the necessary signals to calculate the high-resolution interpolated angle for both signal paths, using the ADS7254 dual 12-bit ADC with SPI and an embedded dual S/H ADC on the host processor, if available.

The interface is compliant to 3.3-V I/O systems. To have a solid GND connection, all odd pins are assigned to GND. The signals on the even pins are listed in Table 14.

Table 14. TIDA-00202 Interface Connector to Host MCU

FUNCTION	SIGNALS	I/O (3.3 V)	COMMENT
12-bit high-resolution output channel for SIN, COS with ADS7254 and SPI (slave)	SDI (I)	Digital input	Data input for serial communication. Used for configuration of dual sampling mode
	/CS (I)	Digital input	Chip-select signal; active low. Falling edge of /CS latches the analog input (Hold) and initiates a new conversion. Use falling edge of /CS to latch QEP counter on host processor synchronously, like on Piccolo MCU
	SCLK (I)	Digital input, up to 24 MHz	Clock for serial communication
	SDO_A (O)	Digital output	Data output for serial communication, channel A and channel B. 16-bit 2's complementary data on each channel A and channel B. Input to output signal gain = 5.
	SDO_B (O)	Digital output	Data output for serial communication channel B
Digital quadrature encoded signals SIN and COS	SINTTL (O)	Digital output	160 mV (±80 mV) hysteresis for SIN and COS, configurable
	COSTTL (O)	Digital output	
Analog single-ended output channel for SIN and COS	SIN (O)	Analog output: 0 to 3.3 V, 1.65-V bias (single-ended)	Nominal output range: 0.82 to 2.48 V (1.65 ±0.83 V) for 1 V_{PP}, gain = 1.67, bias voltage = 1.65 V
	COS (O)	Analog output: 0 to 3.3 V, 1.65-V bias (single-ended)	Nominal output range: 0.82 to 2.48 V (1.65 ±0.83 V) for 1 V_{PP}, gain = 1.67, bias voltage = 1.65 V
Digital RS-485 signals	Data_RX (O)	Digital output	RS-485 data receive for the UART protocol
	Data_TX_EN (I)	Digital output	RS-485 data transmit enable for the UART protocol
	Data_TX (I)	Digital input	RS-485 data transmit for the UART protocol

For details on the connector pin assignment, see Section 6.

CAUTION

In order to synchronize the analog input sample of the ADS7254 12-bit dual sampling ADC with a QEP incremental counter module, use the /CS signal to the ADS7254 to latch the QEP counter too. For the MCU, like Piccolo, connect the /CS to the eQEP Strobe input pin EPEPxS, where x is the module number. The Piccolo eQEPx module can be configured to latch the QEP counter on a falling edge of the EQEPxS pin.

4.4.2 12-Bit Dual ADC ADS7254 With SPI Serial Output

This section outlines the configuration of the ADS7254 through the serial interface. This is split into programming the full-scale input voltage range with the internal ADS7254 reference and the serial data transfer.

4.4.2.1 ADS7254 Input Full Scale Range Output Data Format

In this design, the ADS7254 is intended to be configured for ±2 × V_{REF} input range. The internal reference voltage V_{REF} should be set to 2.5 V to yield a ±5-V FSR.

Table 15. ADS7254 Transfer Characteristics for TIDA-00202

INPUT VOLTAGE AINP_x - AINM_x	MODE	INPUT VOLTAGE	OUTPUT CODE (HEX)
< –5 V	±2 × V_{REF} RANGE	NFSC	800
–5 V + 1 LSB		FSR	801
–1 LSB		–1 LSB	FFF
0		0	0
5 V – 1 LSB		PFSR – 1 LSB	7FF

The output date format for each channel A and B is 16-bit signed integer output (2's complementary).

4.4.2.2 ADS7254 Serial Interface

The ADS7254 uses the serial clock (SCLK) for synchronizing data transfers in and out of the device. The CS signal defines one conversion and serial transfer frame. A frame starts with a CS falling edge and ends with a CS rising edge. Between the start and end of the frame, a minimum of N SCLK falling edges must be provided to validate the read or write operation. As shown in Table 16, N depends upon the interface mode used to read the conversion result. When N SCLK falling edges are provided, the write operation attempted in the frame is validated and the internal user-programmable registers are updated on the subsequent CS rising edge. This CS rising edge also ends the frame. If CS is brought high before providing N SCLK falling edges, the write operation attempted in the frame is not valid.

Table 16. ADS7254 SCLK Falling Edges for a Valid Write Operation

INTERFACE MODE	MINIMUM SCLK FALLING EDGES REQUIRED TO VALIDATE WRITE OPERATION N
32-CLK, dual-SDO mode (default)	32
32-CLK, single-SDO mode	48
16-CLK, dual-SDO mode	16
16-CLK, single SDO mode	32

The example firmware on the F28069M Piccolo MCU initializes the ADS7254 in the 32-CLK, single SDO mode.

For more details on the serial interface mode and read and write operations, refer to the AD7254 datasheet (SBAS556).

4.4.2.3 ADS7254 Conversion Data Read

As outlined in Table 16, the device provides four different interface modes to the user. These modes are able to read the conversion result as well. These modes offer flexible hardware connections and firmware programming. In the 32-CLK interface modes, the device uses an internal clock to convert the sampled analog signal. The conversion is completed during the first 16 periods of SCLK and the conversion result can be read on the subsequent SCLK falling edges. All devices in the family (that is, ADS8354, ADS7854, and ADS7254) support the 32-CLK interface modes. In addition to the 32-CLK interface modes, the ADS7854 and ADS8354 also support the 16-CLK interface modes. By using the 16-CLK interface modes, the same throughput can be achieved at much lower SCLK speeds.

The example firmware on the F28069M Piccolo MCU initializes the ADS7254 in the 32-CLK, single SDO mode.

The 32-CLK, single-SDO mode provides the option of using only one SDO pin (SDO_A) to read conversion results from both ADCs (ADC_A and ADC_B). SDO_B remains in 3-state and can be treated as a no connect (NC) pin. Figure 16 shows a detailed timing diagram for this mode.

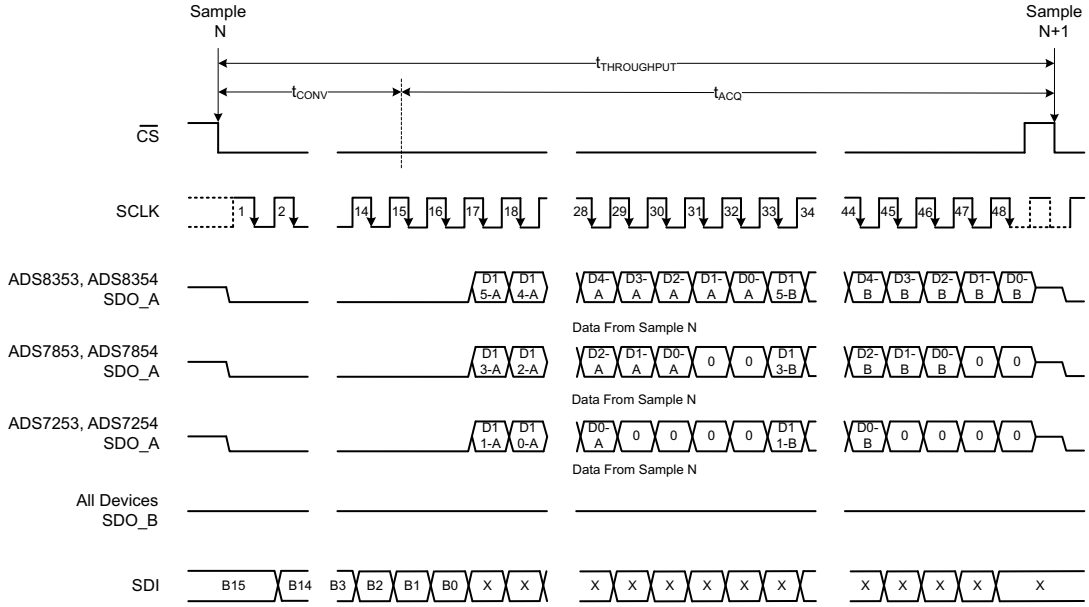


Figure 16. 32-CLK, Single-SDO Mode Timing Diagram

A CS falling edge brings the serial data bus out of 3-state and also outputs a 0 on the SDO_A pin. The device converts the sampled analog input during the conversion time (t_{CONV}). SDO_A reads 0 during this period. After completing the conversion process, the sample-and-hold circuit goes back into sample mode. The device outputs the MSB of ADC_A on the SDO_A pin on the 16th SCLK falling edge. The subsequent SCLK falling edges are used to shift out the conversion result of ADC_A followed by the conversion result of ADC_B on the SDO_A pin. In this mode, at least 48 SCLK falling edges must be given to validate the read or write frame. A CS rising edge ends the frame and puts the serial bus into 3-state.

Refer to the ADSxx54 data sheet for more details.

4.4.2.4 ADS7254 Register Configuration

To select the modes as outlined in the previous sections, the ADS7254 registers REFDAC_A, REFDAC_B, and CFR are programmed as follows.

REFDAC_X and CFR are 16-bit registers and are programmed as shown in Table 17, with the upper 4 bits selecting write/read mode and corresponding register.

Table 17. ADS7254 Register Configuration

REGISTER	DATA (HEX)	COMMENT
REFDAC_A	9FF8	Write mode to REFDAC_A, selects VREF_A = 2.5 V
REFDAC_B	AFF8	Write mode to REFDAC_B, selects VREF_B = 2.5 V
CFR	8640	Write mode to CFR, selects 32-CLK dual SDO mode with A and B on SDO_A, FSR = ±2 × V_{REF}, select internal V_{REF}

Refer to the ADSxx54 data sheet for more details.

4.5 Recommended Design Upgrades

A 10-Ω pulse-proof series resistor each should be placed between the 130-Ω termination resistor and the Schottky diode as indicated in Figure 17 for proper SIN and COS input termination. The fasted change is to move the 0-Ω resistor R86, R92 (on the SIN channel) to that node and replace the component with a 10-Ω plus prove resistor, for example CRCW060310R0JNEAHP for 0603 footprint.

This needs to be done for both SIN and COS signal path.

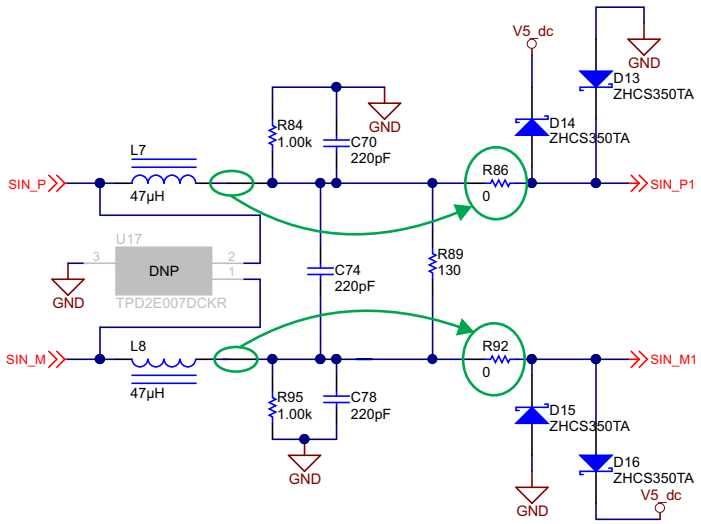


Figure 17. Upgrade to Input Termination and Protection Circuit

The selected 47-µH inductor has a significant 2.6- to 3.2-Ω resistance, which acts as a voltage divider with the termination resistors. For tight tolerance and minimum temperature drift, it should be replaced with a 0-Ω resistor or a common-mode choke with a much lower series resistance. Likely, the footprint would change in the latter case.

5 Software Design

To test and evaluate the design, the C2000 InstaSPIN LaunchPad LAUNCHXL-F28069M features the real-time C2000 Piccolo MCU TMS320F28069M.

5.1 Overview

Any embedded processor or microcontroller with embedded quadrature encoded pulse counter, a UART and SPI, and optionally a dual 12-bit ADC can be used in conjunction with the TIDA-00202 hardware design. The C2000 real-time control MCU family is an ideally suited processor for position feedback encoder applications especially as it can implement the entire motor control algorithm as well, which saves on system cost through integration (see the C2000 DesignDRIVE platform.

To easily evaluate the TIDA-00202 hardware reference design, an example firmware is provided for the C2000 F28069M Piccolo LaunchPad, which can evaluate the TIDA-00202 with HIPERFACE encoders. A user menu through a USB virtual COM port is provided to initialize the line count of selected HIPERFACE encoder and print the calculated high-resolution angle information along with other user-selectable data.

The main peripherals leveraged on the F28069M are the SPI-A peripheral to read the dual high-resolution 12-bit data signals $SIN_{external}$ and $COS_{external}$. The embedded dual S/H ADC is used to convert the single-ended analog signals $SIN_{internal}$ and $COS_{internal}$. The quadrature encoder pulse (eQEP2) module is used for directional up-down incremental count based on the signals SIN_{TTL} and COS_{TTL}. The SCI-B peripheral was used UART communication to get the absolute position initialization. The ePWM1 timer is used to generate periodic interrupts to trigger a new angle measurement. A 16-kHz period was chosen. The SCI-A peripheral was used to implement the UART based user interface at 115000 baud through virtual COM port.

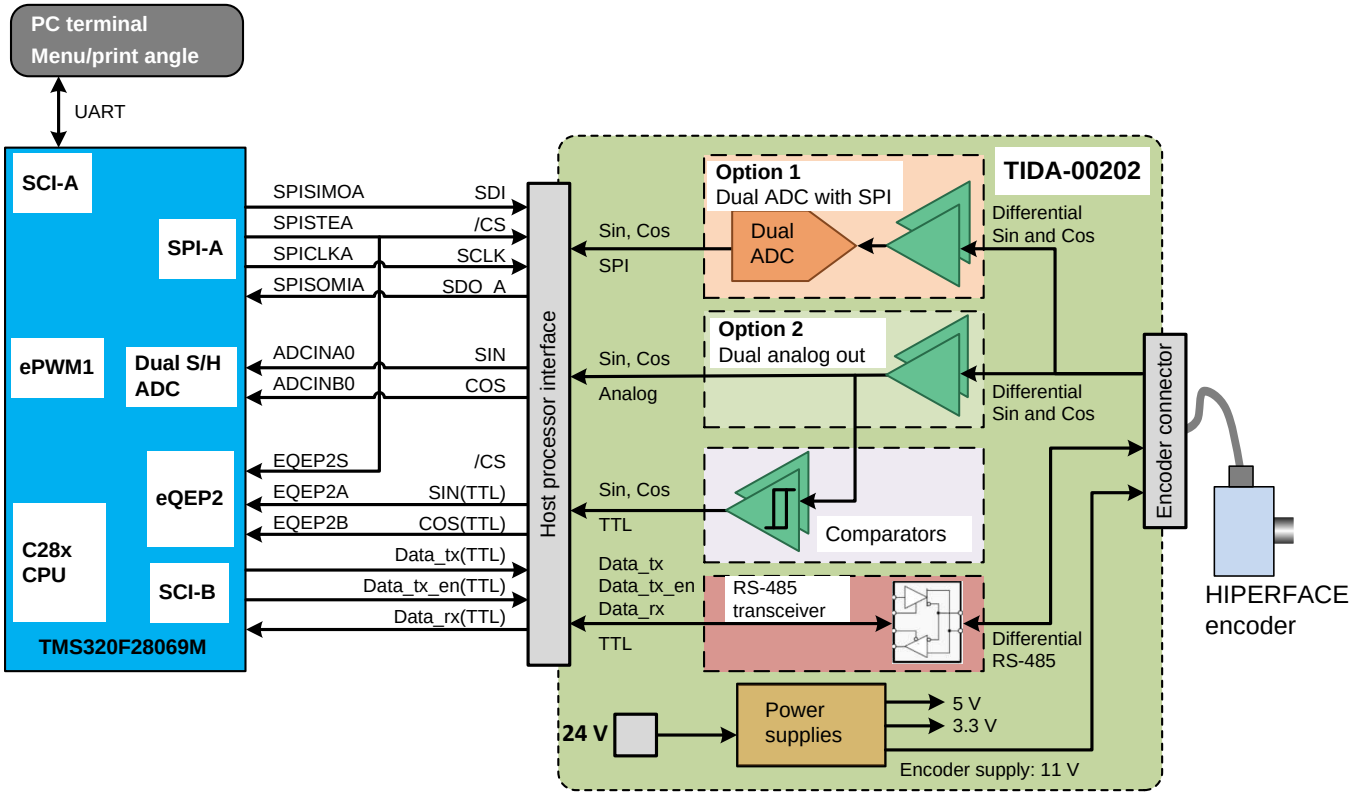


Figure 18. TMS320F28069M Peripheral Module and Pin Assignment to TIDA-00202 Host Processor Interface

5.2 C2000 Piccolo Firmware

The example firmware is developed and compiled for the Piccolo TMS320F28069M and leverages the peripheral modules outlined in Figure 18.

The firmware leverages C2000 controlSUITE™. The firmware basically consists of three functional blocks:

- The F28069M framework, as outlined in Figure 19
- The algorithm to synchronously sample the required data and calculate the interpolated angle
- The UART terminal-based user interface

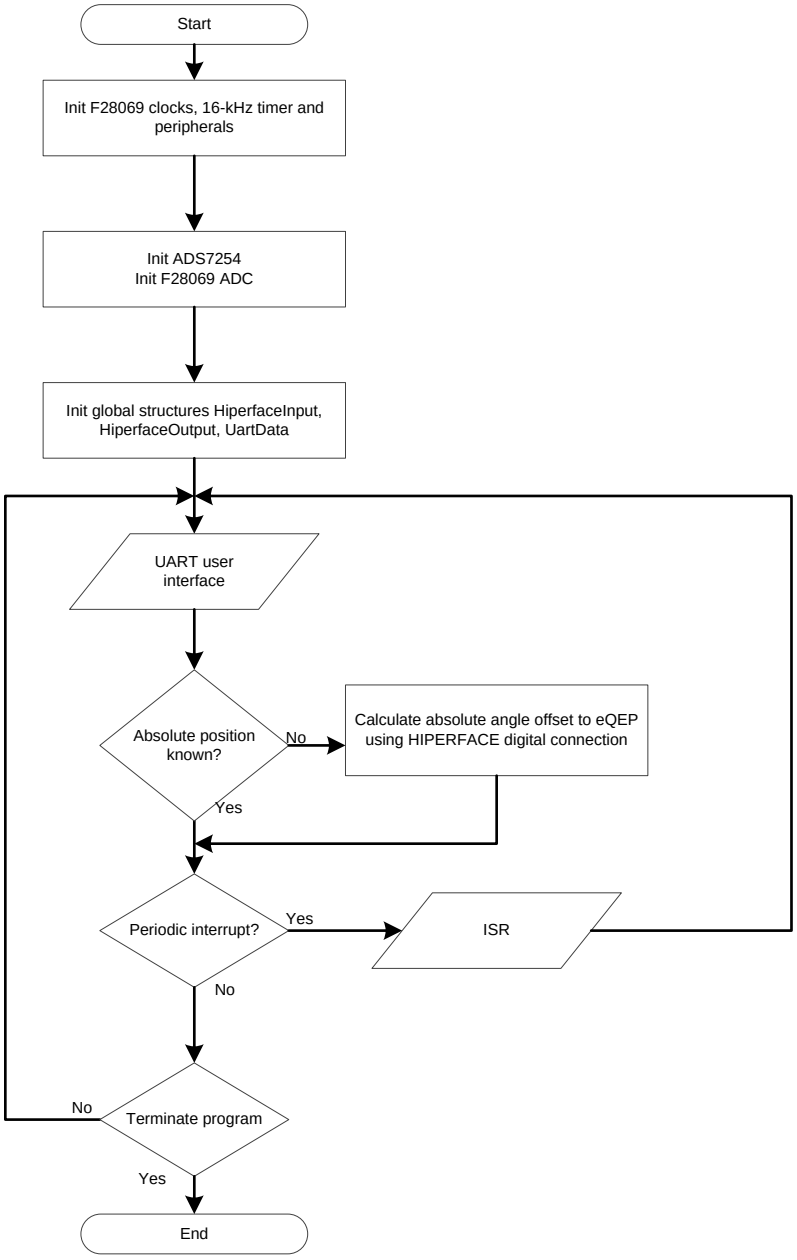


Figure 19. Flowchart of HIPERFACE Encoder F28069M Framework

The TMS320F28069M framework initializes the TMS320F26069M CPU clock to 80-MHz, the GPIO multiplexers, the peripherals like SPI-A, SCI-A (UART), SCI-B (UART), the ePWM1-based periodic timer and interrupt, and the embedded 12-bit dual S/H ADC. It also configures the external 12-bit dual ADC ADS7254 through SPI-A as outlined in Section 4.4.2.4. The SPI-A is configured as the SPI master with the serial clock of 10 MHz. This is the maximum SPI clock for the Piccolo F28069M. For other C2000 derivatives like the TMS320F2837xD/S Delfino the SPI clock can be up to the maximum 24 MHz of the ADS7254.

After initialization the program invokes the UART-based user interface and serves the period interrupt service routine (ISR). The period ISR implements the synchronized data capture, calculation of intermediate phase, and total interpolated angle based on both the external 12-bit ADC ADS7254 and the internal 12-bit ADC. It follows the algorithms outlined in Section 1. The code is written with 32-bit integer fractional Q28 numbers using TI's IQmath library. The advantage of 32-bit fractional numbers versus 32-bit IEEE floating point is that the resolution remains constant independent of the data range. Because the data range is limited from 0 to 1.0 for the angle (per unit) as well as for the ADC input data, which is scaled to maximum of ±5 V, Q28 numbers with an integer range ±8.0 provide enough headroom while accuracy remains constant for all data.

The flowchart of the ISR is shown in Figure 20.

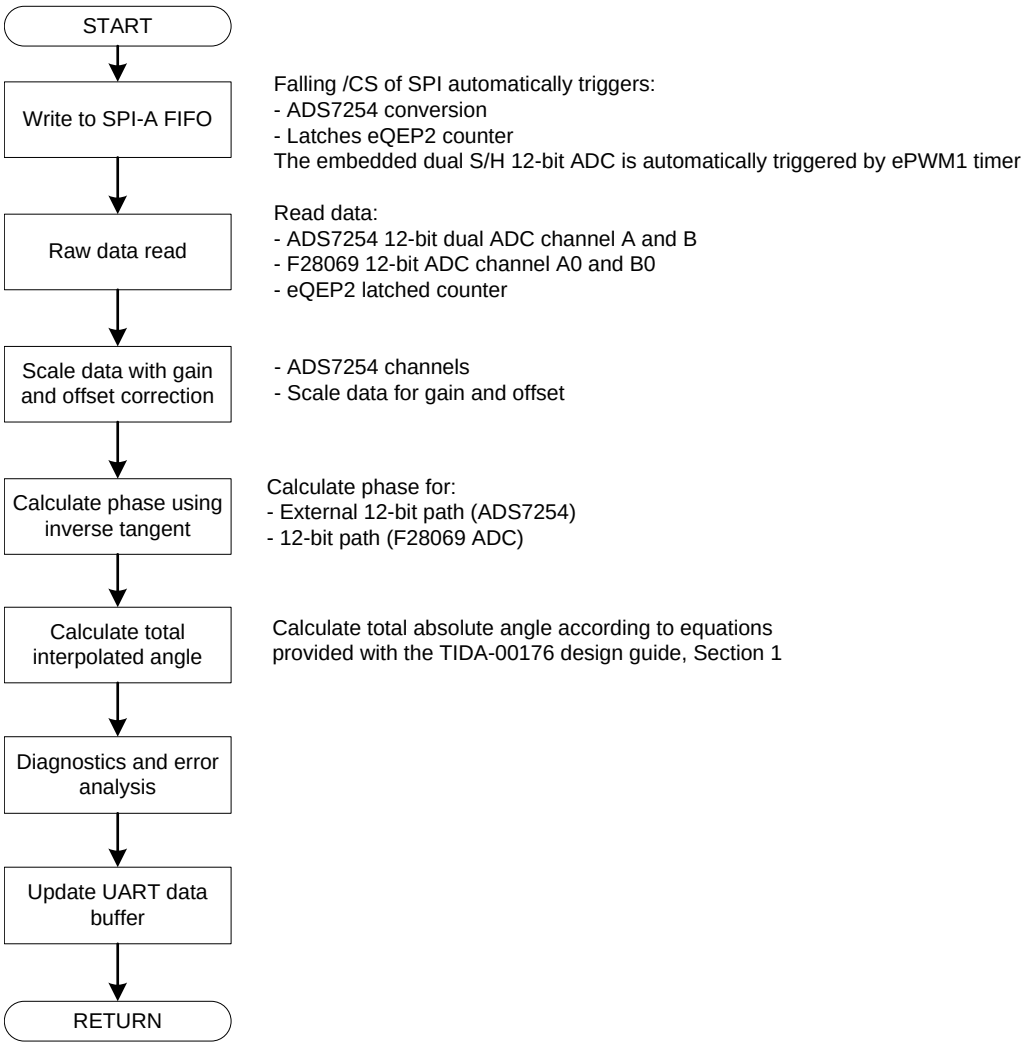


Figure 20. Flowchart of HIPERFACE Encoder Periodic ISR With Interpolated Angle Calculation

5.3 User Interface

For a quick evaluation, a virtual COM port-based user interface was implemented. Any terminal interface at 115000 baud like Tera Term can be used.

The user interface allows the user to enter the line count of the connected HIPERFACE encoder before the program reaches the main menu. The menu provides menu item options for the user to select either a basic display mode with just the high-resolution angle printed or an expert display mode, both with a 10-Hz update rate. Other menu items are data dump modes at 10-Hz update rates, intended write to a file for post analysis.

The flowchart of the user interface is shown in Figure 21.

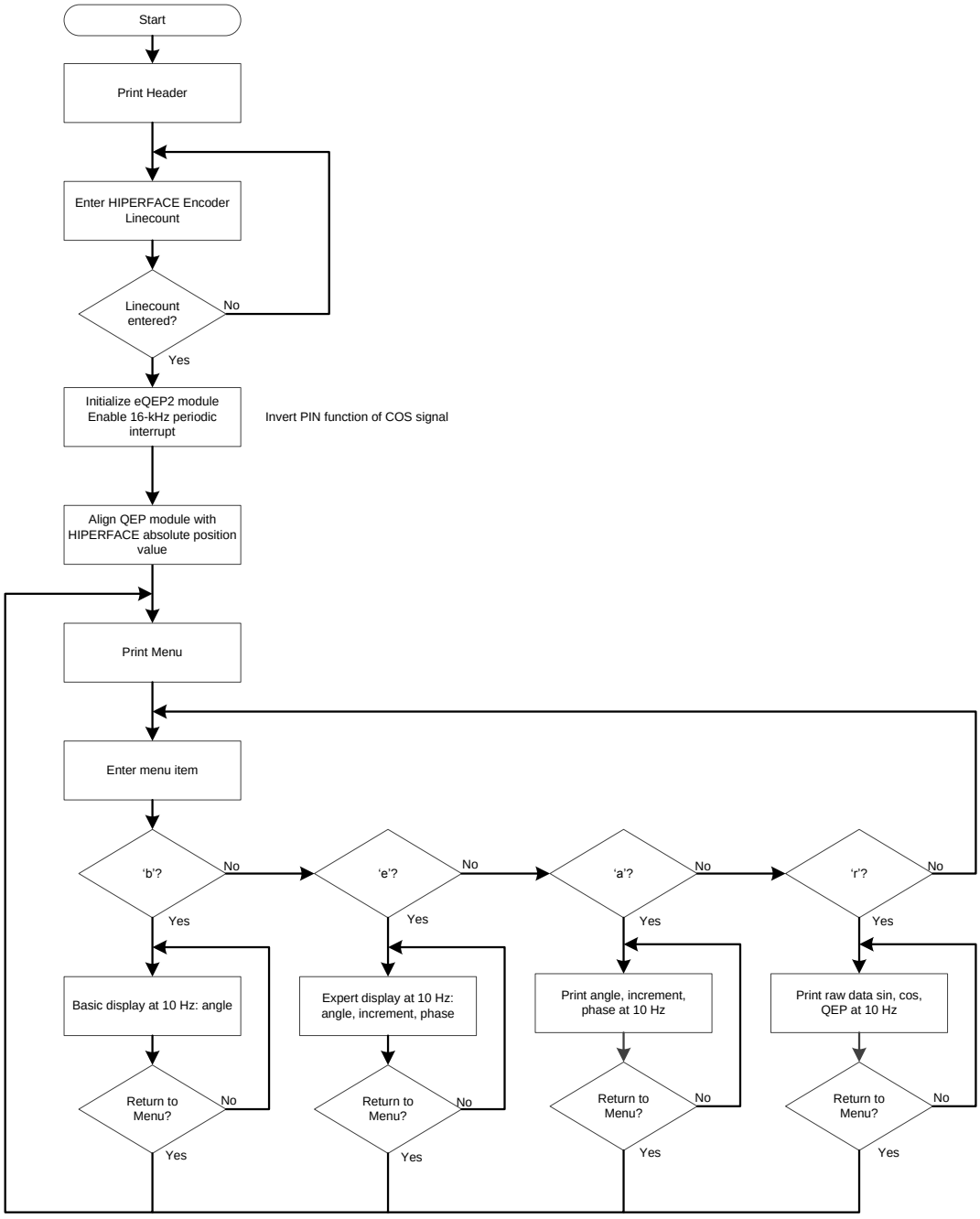


Figure 21. Flowchart of UART Terminal User Interface

Table 18 through Table 21 outline the data output format for each of the four menu items. In data dump mode, a 'tab' is included as a delimiter between the data in each row.

Table 18. Basic Display Mode Output Format and Data Scaling

MENU	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4	COLUMN 5
'b' basic display	Total angle with ADS7254 (scale)	—	—	—	—
Data format	Float (0 to 360 degrees)	—	—	—	—

Table 19. Expert Display Mode Output Format and Data Scaling

MENU	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4	COLUMN 5
'e' expert display	Total angle with ADS7254 (scale)	Absolute position from digital data	Incremental count	Phase ADS7254 (scale)	Phase F28069M ADC (scale)
Data format	Float (0 to 360 degrees)	Integer	Integer	Float (0 to 1.0)	Float (0 to 1.0)

Table 20. Angle Data Dump Menu Format and Scaling

MENU	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4	COLUMN 5	COLUMN 6
'd' angle dump	Total angle with ADS7254 (scale)	Total angle with F28069 ADC (scale)	Incremental count	Phase ADS7254 (scale)	Phase F28069M ADC (scale)	Periodic tick (scale)
Data format	Float (0 to 360 degrees)	Float (0 to 360 degrees)	Integer	Float (0 to 1.0)	Float (0 to 1.0)	Integer (66 µs)

Table 21. Raw Data Dump Menu Format and Scaling

MENU	COLUMN 1	COLUMN 2	COLUMN 3	COLUMN 4	COLUMN 5	COLUMN 6	COLUMN 7
'r' raw data	Incremental count (SW)	Incremental count (latch on /CS)	Input SIN+/SIN–, ADS7254 (scale)	Input COS+/COS–, ADS7254 (scale)	Input SIN+/SIN–, F28069 (scale)	Input COS+/COS–, F28069 (scale)	Periodic tick (scale)
	Integer	Integer	Float (V_{PP})	Float (V_{PP})	Float (V_{PP})	Float (V_{PP})	Integer (66 µs)

6 Getting Started

6.1 TIDA-00202 PCB Overview

Figure 22 and Figure 23 shows a photo of the top and bottom side of the TIDA-00202 PCB. The headers and default jumper settings are explained in Section 6.2.

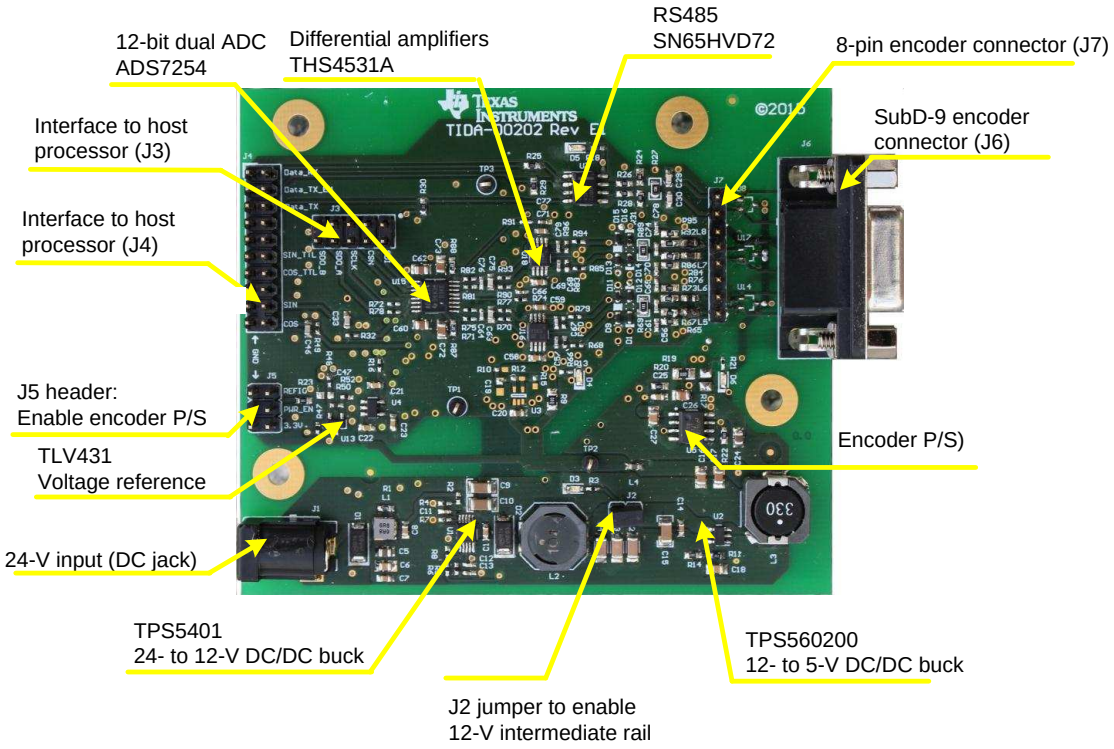


Figure 22. TIDA-00202 Board Picture (Top View)

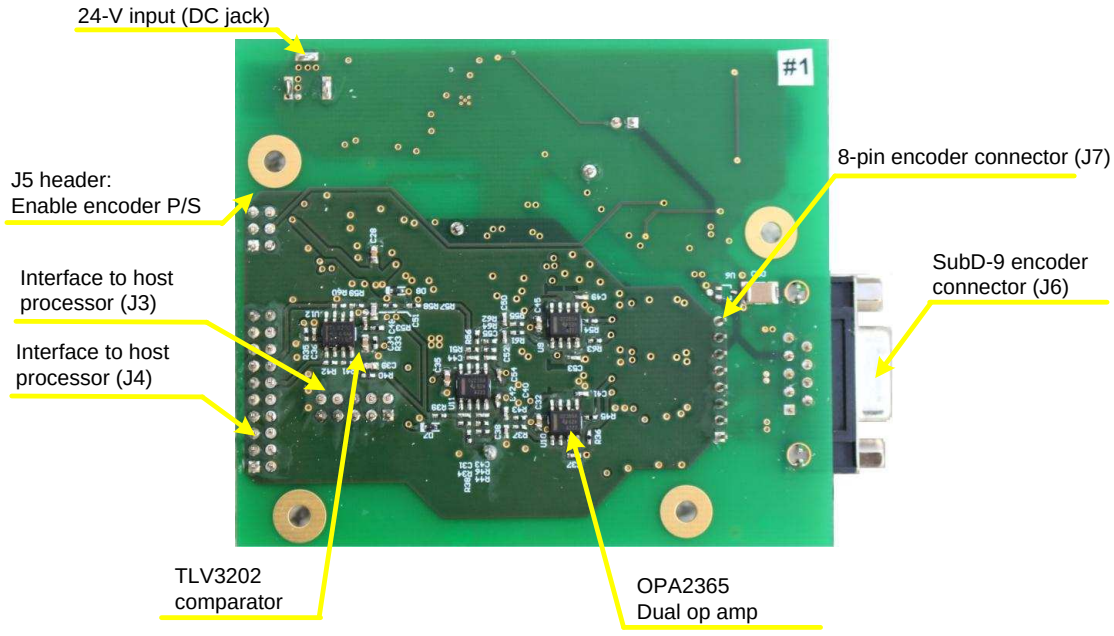


Figure 23. TIDA-00202 Board Picture (Bottom View)

6.2 Connector and Jumper Settings

6.2.1 Connectors

The connector assignment and jumper settings are outlined in Table 22 through Table 28.

The 24-V nominal input voltage can be supplied through either connector J1.

Table 22. 24-V Input (DC Jack J1)

PIN	DESCRIPTION
Internal	24-V input voltage (17 to 36 V)
External	GND

Table 23. Enable 12-V Intermediate Rail (J2)

PIN	DESCRIPTION
1	Output of TPS5401 (default 12 V)
2	12-V supply rail

Table 24. Host Processor Interface External ADC (J3)

PIN	DESCRIPTION	PIN	DESCRIPTION (3.3-V I/O)
1	GND	2	SDI (ADS7254)
3	GND	4	/CS (ADS7254)
5	GND	6	SCLK (ADS7254)
7	GND	8	SDO_A (ADS7254)
9	GND	10	SDO_B (ADS7254)

Table 25. Host Processor Interface Encoder (J4)

PIN	DESCRIPTION	PIN	DESCRIPTION (3.3-V I/O)
1	GND	2	Data_RX
3	GND	4	Data_TX_EN
5	GND	6	Data_TX
7	GND	8	
9	GND	10	
11	GND	12	SIN (TTL)
13	GND	14	COS (TTL)
15	GND	16	
17	GND	18	SIN (single-ended analog 0 to 3.3 V)
19	GND	20	COS (single-ended analog 0 to 3.3 V)

For detailed signal descriptions on the host processor interfaces, see Section 4.3.

Table 26. Header J7 With Encoder Supply Enable (J5)

PIN	DESCRIPTION	PIN	DESCRIPTION
1	GND	2	REFIO (1.65 V)
3	GND	4	ENABLE encoder supply voltage (11 V)
5	GND	6	3.3 V

Table 27. Encoder Sub-D9 Connector (J6)

PIN	DESCRIPTION	PIN	DESCRIPTION
1	RS485+	2	Encoder supply GND
3	SIN–	4	Encoder supply VCC (default 11 V)
5	COS+	6	RS485–
7	NC	8	SIN+
9	COS–		

Table 28. Encoder 8SIL100 Connector (J7)

PIN	DESCRIPTION	PIN	DESCRIPTION
1	RS485–	2	RS485+
3	Encoder supply GND	4	SIN–
5	SIN+	6	Encoder supply VCC (default 11 V)
7	COS–	8	COS+

6.2.2 Default Jumpers Configuration

Prior to working with the TIDA-00202 board, ensure the following default jumper settings are applied. Refer to the board picture in Figure 24.

Table 29. Default Jumpers Settings

HEADER	JUMPER SETTING
J2	Insert a jumper between J32 pins 1-2 to enable the 12-V intermediate rail connected to the POL.

6.3 Design Evaluation

6.3.1 Prerequisites

The following hardware equipment and software are required to evaluate the TIDA-00202 TI Design.

Table 30. Prerequisites

EQUIPMENT	COMMENT
24-V power supply	24-V output power brick with at least 250-mA output current Output connector 2.1-mm I.D. × 5.5-mm O.D. × 9.5-mm Female
TIDA-00202 hardware	For default jumper settings per Section 6.2.
1 jumper for board settings	2 pins, 100 mils
TIDA-00202 firmware	Download from TIDA-00202 design folder
InstaSPIN-MOTION F28069M Launchpad	Available through TI eStore
USB cable	Mini USB type A to USB type A cable
TIDA-00202 to LaunchPad adapter	Internal TI (optional)
Code Composer Studio™ 6 (CCS6)	Download from www.ti.com
PC terminal program	Any terminal program, like for example Tera Term
HIPERFACE Encoder	For example, SRS50-HWA0-K21

6.3.2 Hardware Setup

The following connections are required between the TIDA-00202 and the InstaSPIN-MOTION LaunchPad.

Table 31. TIDA-00202 Host Processor Interface (J4) to InstaSPIN LaunchPad

TIDA-00202 HOST PROCESSOR INTERFACE (J6)		CONNECT TO →	INSTASPIN-MOTION LAUNCHPAD	
J4 PIN	DESCRIPTION		HEADER PIN	DESCRIPTION (3.3-V I/O)
1	GND		J3-Pin 22	GND
19	GND		J2-Pin 20	GND
2	Data_RX		J2-Pin 18	GPIO44/SCIRXDB
4	Data_TX_EN		J1-Pin 9	GPIO33
6	Data_TX		J1-Pin 8	GPIO22/ SCITXDB
8		NC	NC	NC
10		NC	NC	NC
12	SIN (TTL)		J6-Pin 55	GPIO24/eQEP2A
14	COS (TTL)		J6-Pin 54	GPIO25/eQEP2B
16		NC	NC	NC
18	SIN (single-ended analog 0 to 3.3 V)		J3-Pin 27	ADCIN_A0
20	COS (single-ended analog 0 to 3.3 V)		J3-Pin 28	ADCIN_B0

Table 32. TIDA-00202 External ADC Interface (J3) to InstaSPIN LaunchPad

TIDA-00202 HOST PROCESSOR INTERFACE (J6)		CONNECT TO →	INSTASPIN-MOTION LAUNCHPAD	
J3 PIN	DESCRIPTION		HEADER PIN	DESCRIPTION (3.3-V I/O)
1	GND		J3-Pin 22	GND
3	GND		J2-Pin 20	GND
2	SDI (ADS7254)		J2-Pin 15	GPIO16/SPISIMOA
4	/CS (ADS7254)		J2-Pin 19 J6-Pin 59	GPIO27/eQEP2S GPIO19/SPISTEA
6	SCLK (ADS7254)		J1-Pin 7	GPIO18/SPICLKA
8	SDO_A (ADS7254)		J2-Pin 14	GPIO17/SPISOMIA
10	SDO_B (ADS7254)	NC	NC	NC

Follow these steps to setup the hardware:

1. Connect the TIDA-00202 board with the InstaSPIN-MOTION LaunchPad using the proper connections as shown above. Note: For the internal testing, an adapter board has been designed to interface between the TIDA-00202 and the InstaSPIN-MOTION LaunchPad, as shown in Figure 24.
2. Verify the TIDA-00202 is configured with the default jumper settings as per Section 6.2.2.
3. Connect the HIPERFACE encoder to the board by using either the SubD-9 connector (J6) or the SIL-8 connector (J7).
4. Insert the 24-V input from the power brick in the J1 connector.
5. Connect the USB mini cable from the InstaSPIN-MOTION LaunchPad to the PC.

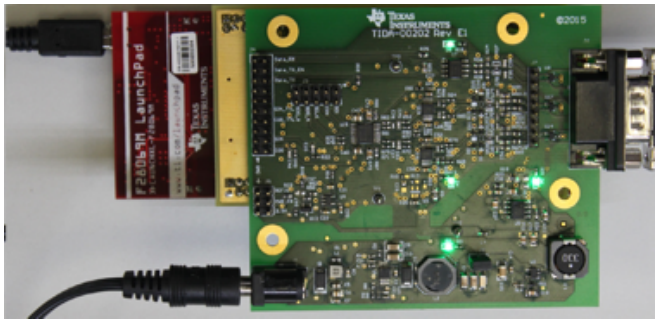


Figure 24. TIDA-00202 Board Mounted on the InstaSPIN-MOTION LaunchPad (Top View)

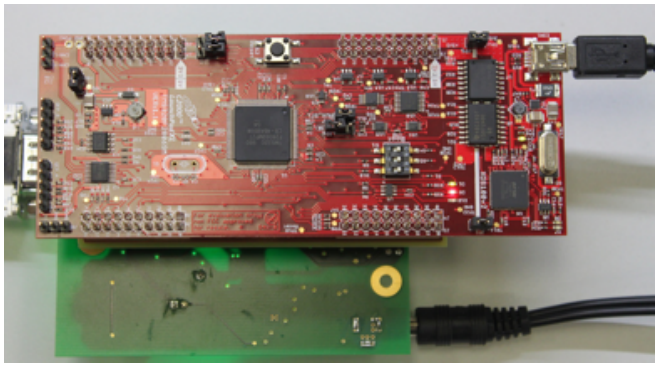


Figure 25. TIDA-00202 Board Mounted on the InstaSPIN-MOTION LaunchPad (Bottom View)

Please also refer to the InstaSPIN-MOTION LaunchPad prerequisites at http://www.ti.com/tool/launchxl-f28069m.

Ensure the following jumpers on the F28069 LaunchPad are set: JP1, JP2, JP3, and JP7. Do not set JP4, JP5, and JP6 as these must not be connected.

6.3.3 Software Setup

Follow these steps to setup the software:

1. If not done, download the TIDA-00202 HIPERFACE Encoder Firmware from the TIDA-00202 design folder and extract (for example, to folder c:\ti\tida-00202\bin).
2. Invoke a Terminal program like Tera Term that can connect to the corresponding virtual COM port of the InstaSPIN-MOTION F28069M LaunchPad.
3. Setup the Terminal program in Serial Console mode and set the parameters to:
   Baud Rate = 115200, Data = 8-bit, Parity = None, Stop = 1-bit, Flow Control = None
4. Launch CCS.
5. In CCS, setup the XDS100 JTAG target with the InstaSPIN-MOTION F28069M LaunchPad.
6. In CCS, connect to the TMS320F28069M and download TIDA-00202 binary output file:
   Run → Load Program → TIDA-00202_HIPERFACEEncoder_Example_Firmware_rev1_0.out
7. In CCS, run the target.

The terminal program should display the start screen of TIDA-00202 as shown in Figure 26.

NOTE: After the binary file has been loaded to the F28069M, Steps 4 through 7 are not required anymore. Simply reset the LaunchPad to restart the program. Ensure the F28069M is configured to boot from internal flash. Refer to the InstaSPIN-MOTION LaunchPad documentation.

To troubleshoot, if no connection is established, the VCP driver of the USB virtual Com port TI XDS100 Channel B needs to be enabled under Windows 7 Device Manager. For more details, refer to the InstaSPIN-MOTION LaunchPad documentation.

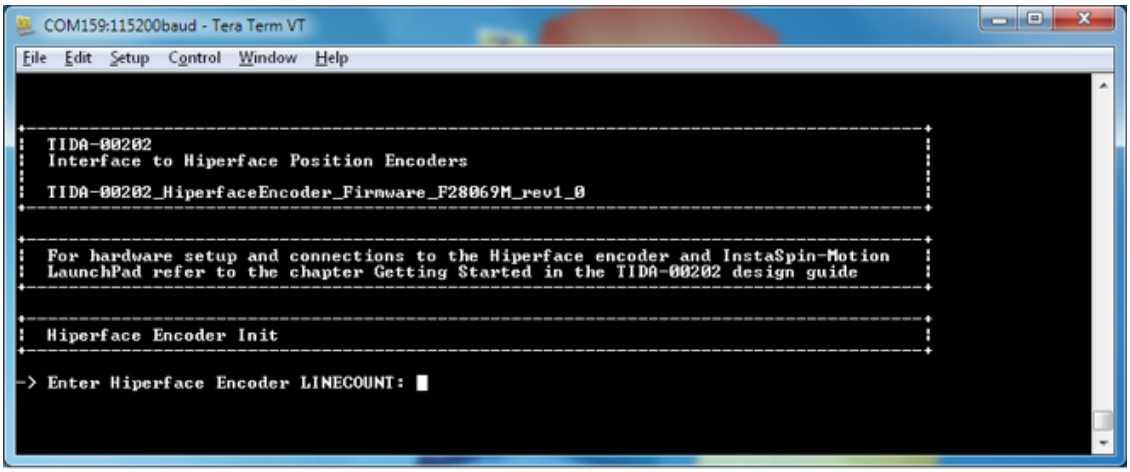


Figure 26. TIDA-00202 User Interface at Startup

6.3.4 User Interface

After startup, the user interface requires to enter the HIPERFACE encoder line count in decimal. After the line count is entered, the main menu is available, as shown in Figure 27.

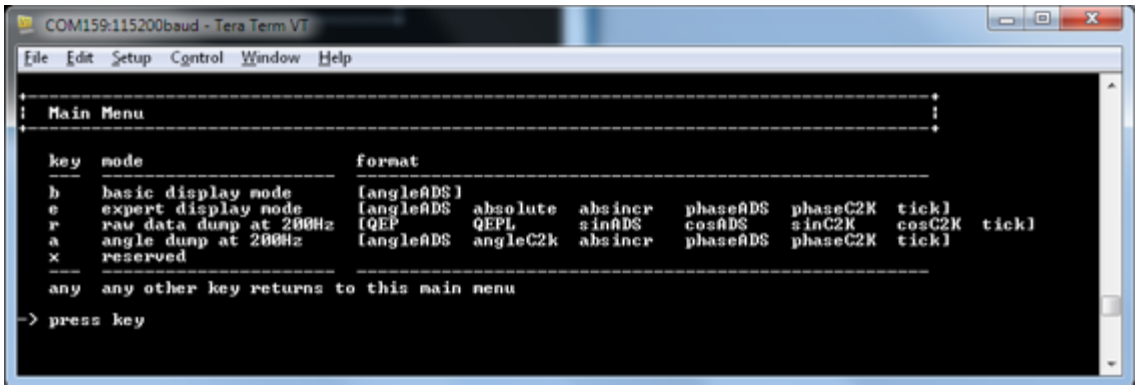


Figure 27. TIDA-00202 User Interface Main Menu

Four menus are available. Each can be selected by pressing the characters 'b', 'e', 'r', or 'a'. The menu item x is reserved for internal test modes during software development.

Press 'b' or 'e' to select the basic or expert display mode, which will print the interpolated angle in degrees or additional information. Note that the software is to test the board; sometimes the HIPERFACE digital data is not being transferred correctly, which can delay the absolute digital value. To return to the main menu, press any key.

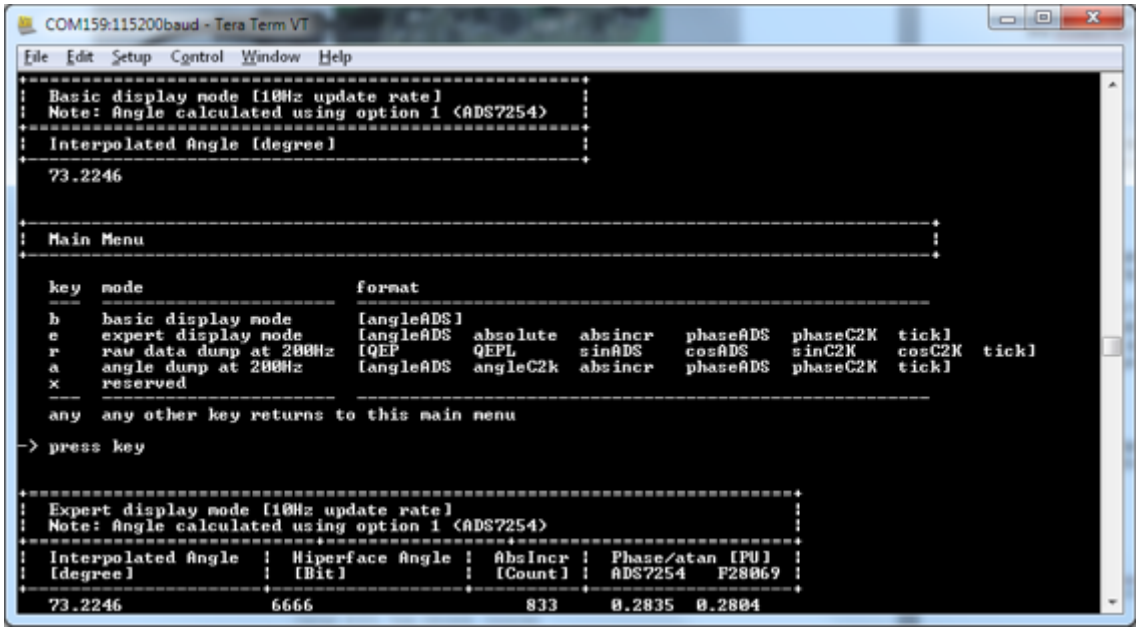


Figure 28. Basic Angle Display and Expert Display Mode

Press 'a' to start an angle data dump at a 10-Hz update rate. The data format is as outlined in Section 5. A screenshot is shown in Figure 29. Press any key to stop and return to the main menu.

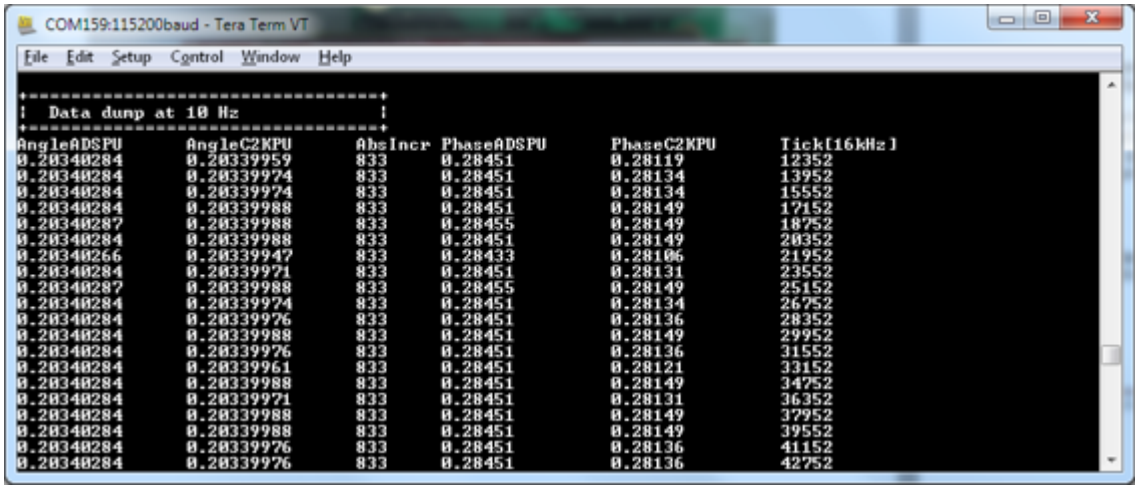


Figure 29. Angle Dump Mode at 10-Hz Update Rate

Press 'r' to start a raw data dump at a 10-Hz update rate. The data format is as outlined in Section 5. A screenshot is shown in Figure 30. Press any key to stop and return to the main menu.

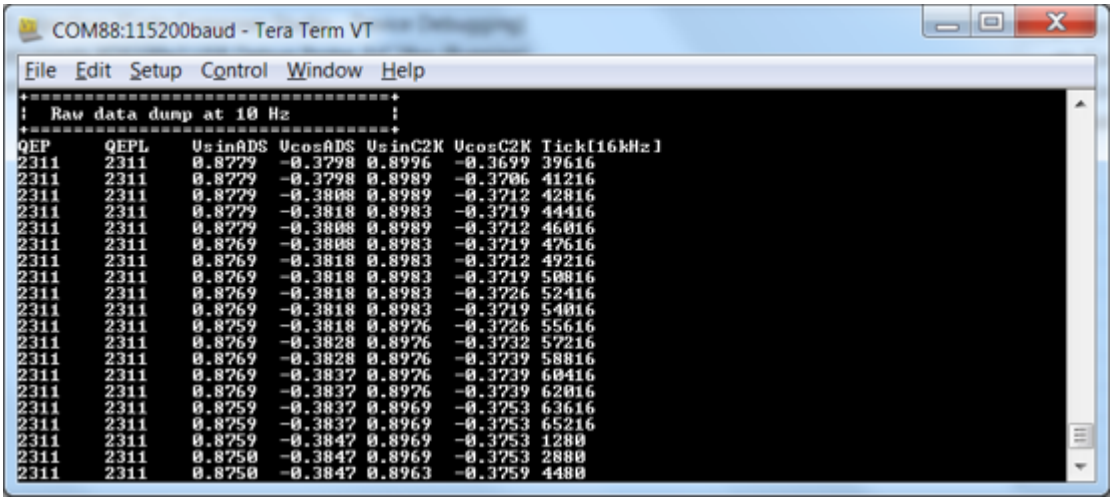


Figure 30. Raw Data Dump Mode at 10-Hz Update Rate

7 Test Results

Tests were done to characterize each individual functional block as well as the entire board. In particular, the following tests were conducted:

- Analog signal chain performance
- RS-485 based digital signal performance
- Power management
- System performance with HIPERFACE sin/cos emulation and HIPERFACE encoder

Tests were done at room temperature around 22°C to 23°C. The following equipment were used for the TIDA-00202 testing session:

Table 33. Test Equipment for TIDA-00202 Performance Tests

TEST EQUIPMENT	PART NUMBER
Programmable 16-bit waveform generator	Keysight (Agilent) 33600A
Low-speed oscilloscope (suitable for power supply tests)	Tektronix TDS2024B
High-speed oscilloscope (suitable for analog signal tests)	Tektronix TDS784C
Adjustable SMPS	Knuerr-Heinzinger Polaris 125-5
24 V at 2.5-A SMPS (power brick)	V-infinity 3A-621DN24
True RMS multimeter	Fluke 179
Differential probes	Tektronix P6630
Single ended probes	Tektronix P6139A
Programmable thermal chamber	Voetsch VT 4002
Programmable electronic load module	Chroma 63103
Control module for electronic load module	Chroma 6314
Sick shielded cable, M23, female/wires, 30 m	DOL-2308-G30MJB2
Sick shielded cable, M23, female/wires, 3 m	DOL-2308-G03MJB2
SICK HIPERFACE Encoders	SRS50-HWA0-K21

7.1 Analog Performance Tests

Figure 31 shows a picture of the TIDA-00202 analog signal chain tests.

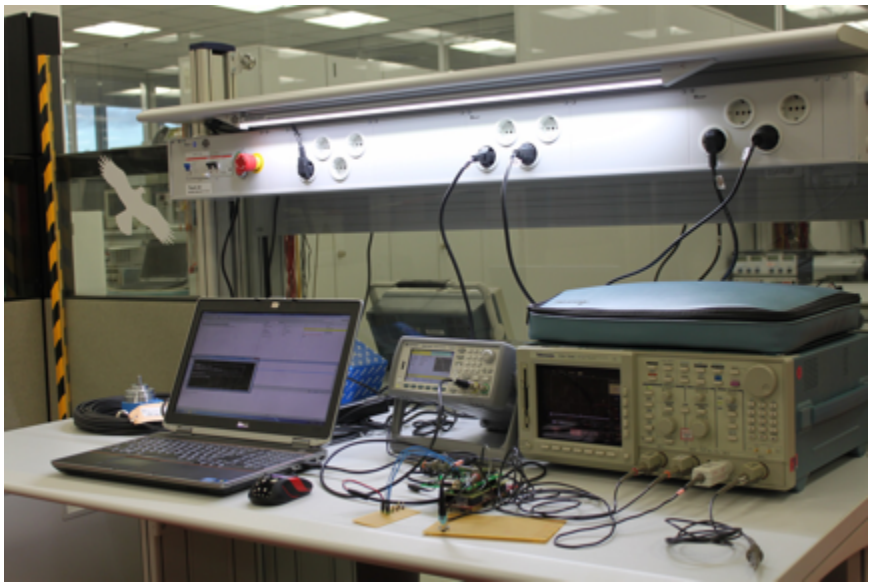


Figure 31. Test Setup for TIDA-00202 Analog Signal Chain Performance Tests

Both the 12-bit signal path featuring fully differential amplifiers THS4531A and the dual 12-bit ADC ADS7253 as well as the differential to single-ended analog signal path were tested. For this design's purpose, a dual output programmable function generator was used. The inputs signals are applied at connector J7 (differential inputs SIN and COS). The output waveforms have been collected at different probe points, depending on the signal path that was analyzed.

7.1.1 12-Bit Dual ADC Signal Path With SPI Output

The measurements have been taken on the high-precision, high-resolution signal path. A sinusoidal signal with 1 V_{PP} was injected at the encoder connector J7 inputs SIN+, SIN– and COS+, COS–, and the differential analog signals was measured at the ADS7254 differential inputs. Figure 32 outlines the input and output signals measured for the test.

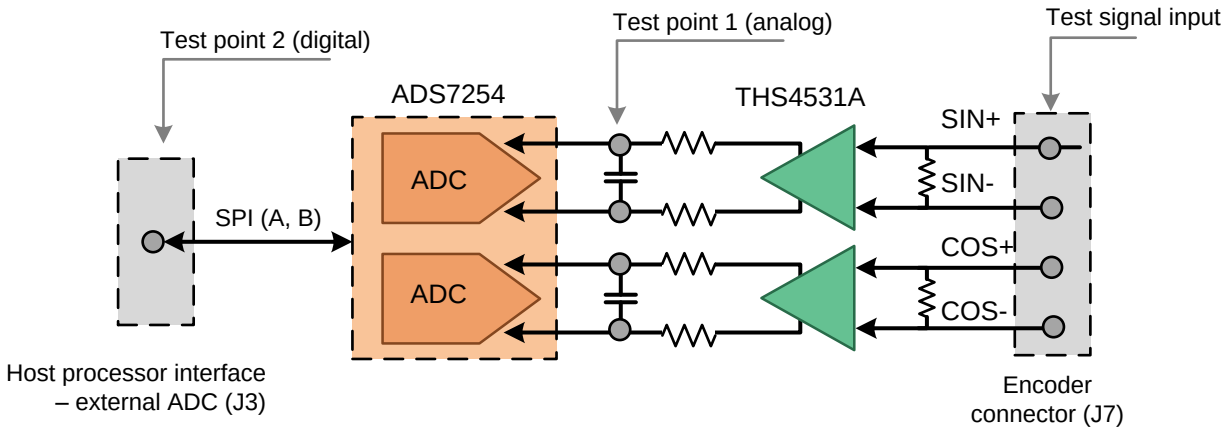


Figure 32. 12-Bit Dual ADC With SPI Signal Chain Measurement Points

Figure 33 shows the magnitude and phase response, which is mainly defined by the THS4531A gain setting of 2, the passive first order low-pass filter comprised of two 10-Ω series resistors, and the 2.2-nF parallel capacitor.

7.1.1.1 Bode Plot of Analog Path From Encoder Connector to ADS7254 Input

Figure 33 shows the bode plot for the option with the optional series 47-µH inductors and without. In the latter option, 0-Ω resistors were used instead of the 47-µH inductors.

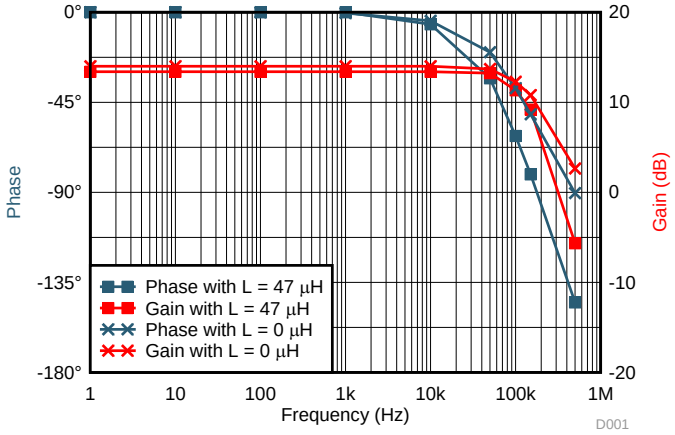


Figure 33. Bode Plot for the High-Resolution Analog from the Encoder Differential Input to the ADS7254 Differential Input (Channel SIN)

7.1.1.2 FFT Performance Plots for Entire 12-Bit Fully Differential Signal Path

For the following tests, the entire high-resolution signal chain, featuring the differential amplifier THS4531A connected through an RC filter to the dual 12-bit ADC ADS7254, has been tested. A sinusoidal test signal has been injected at the encoder differential input pins, and the 12-bit digital data has been analyzed.

The analysis has been done in the frequency domain to evaluate the performance on signal-to-noise ratio (SNR), total harmonic distortions (THD), signal-to-noise And distortion (SINAD), and effective number of bits (ENOB).

For the test a 1-kHz sine wave at an amplitude of 1 V_{PP} was used, which represents the typical sine and cosine differential output of the HIPERFACE encoders. This input signal is applied to one of the input channels, SIN+,SIN– or COS+,COS–, at a time, while the other channel was left unconnected. The purpose is to measure for crosstalk and zero-input noise level between the two channels SIN and COS.

Both channels SIN and COS were sampled at 16 kHz, and 8192 consecutive 12-bit samples were acquired for each channel. The DFT has been calculated for the collected data to measure the SNR and THD.

The Blackman-Harris windowing function was used to weigh the 8192 samples prior to the 8192 FFT.

The following figures show the DFT of the entire high-resolution channel with a sinusoidal input voltage of 1-V_{PP} amplitude and 1 kHz, which is half the full-scale input of 2 V_{PP}.

Note that due to the 8192 FFT, the signal power is spread over more than one frequency bin, hence the peak magnitude at the 1-kHz frequency bin is lower than the expected –9 dB (ideal case), see Figure 34.

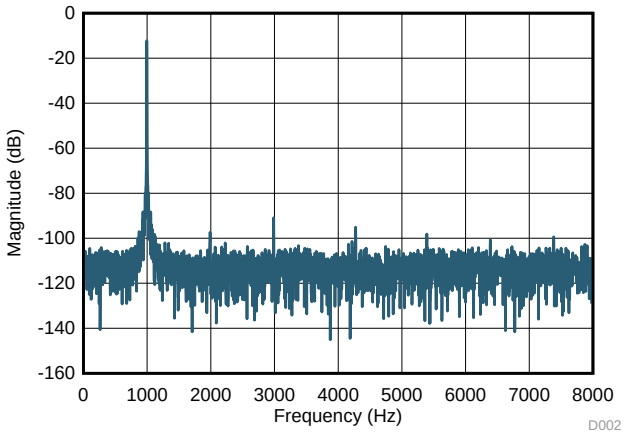


Figure 34. 8192-Point FFT of SIN Output (SPI) With 1-V_{PP}, 1-kHz Sine Wave Input Applied on Input SIN

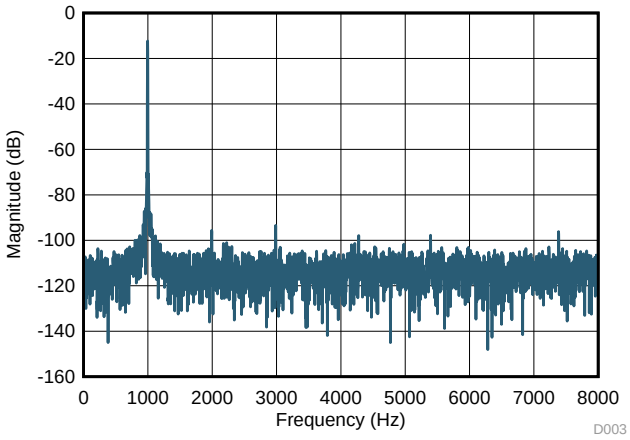


Figure 35. 8192-Point FFT of COS Output (SPI) With 1-V_{PP}, 1-kHz Sine Wave Input Applied on Input COS

Crosstalk analysis was also done for Figure 34 and Figure 35. This analysis is not shown as the input remains a constant zero DC value without an LSB change.

Figure 34 and Figure 35 refer to the theoretical full scale input range.

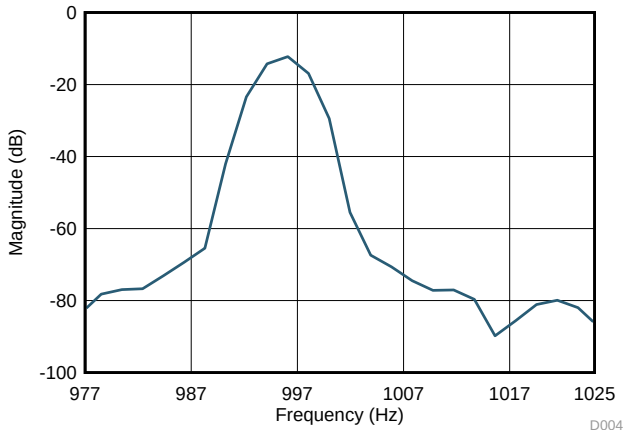


Figure 36. Zoom Around 1-kHz Signal Carrier From Figure 34

The 1-kHz signal has a slight spread in frequency. This is not due to the TIDA-00202 hardware but due to a sample aperture jitter with the F28069 software implementation, which triggered the SPI transfer to start the ADS7254 conversion (hold-mode) with a jitter of ±1 SPI CLOCK (10 MHz) equivalent to ±100 ns.

These figures also highlight that there is basically no crosstalk between the two differential analog channels SIN+, SIN– and COS+, COS–, and the idle (unconnected) channel noise floor is within 1 LSB.

SNR+THD versus the full-scale signal can then be calculated for this design and are listed in Table 34.

Table 34. ADS7254 Signal Path Typical Performance

PARAMETER	VALUE (MEASURED)
SNR+THD (FSR)	72.5 dB

7.1.2 Differential to Single-Ended Analog Signal Path

7.1.2.1 Bode Plot

The bode plot is shown for the option with the optional series 47-µH inductors and without. In the latter option, 0-Ω resistors were used instead of the 47-µH inductors.

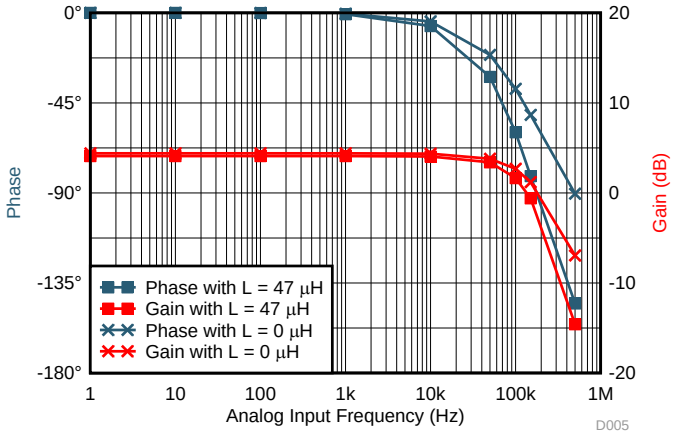


Figure 37. Bode Plot for Differential to Single-Ended Analog Signal Path (Channel SIN)

7.1.2.2 FFT Performance Plots for Single-Ended Analog Output Path

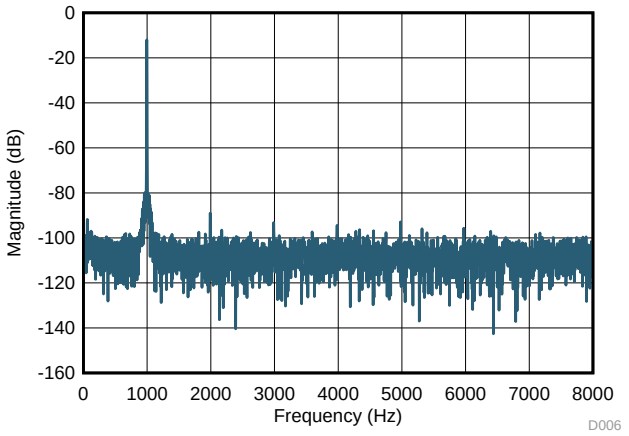


Figure 38. 8192-Point FFT of SIN Output (C2000 ADC) With 1-V_{PP}, 1-kHz Sine Wave Input Applied on Input SIN

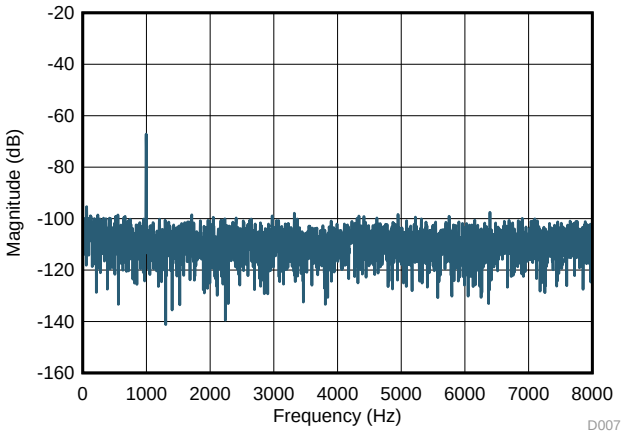


Figure 39. 8192-Point FFT of COS Output (C2000 ADC) With 1-V_{PP}, 1-kHz Sine Wave Input Applied on Input SIN

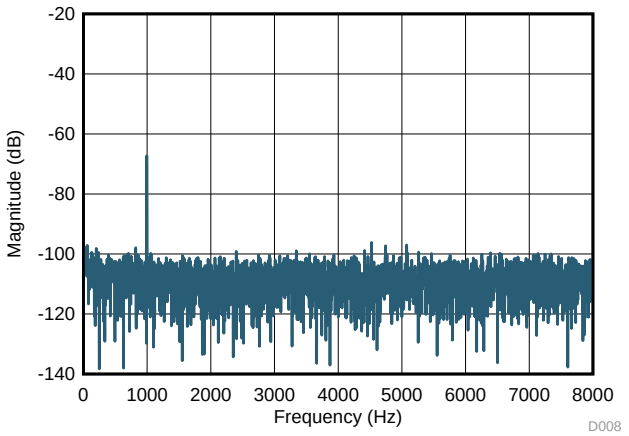


Figure 40. 8192-Point FFT of SIN Output (C2000 ADC) With 1-V_{PP}, 1-kHz Sine Wave Input Applied on Input COS

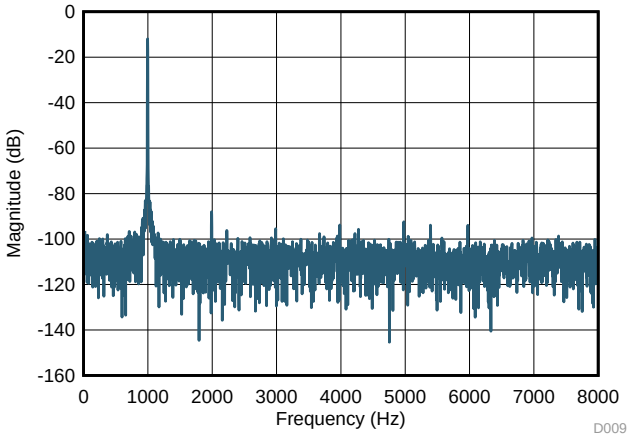


Figure 41. 8192-Point FFT of COS Output (C2000 ADC) With 1-V_{PP}, 1-kHz Sine Wave Input Applied on Input COS

SNR+THD versus the full-scale signal can then be calculated for this design and are listed in Table 35.

Table 35. TMS320F28069 Signal Path Typical Performance

PARAMETER	VALUE (MEASURED)
SNR + THD (FSR)	69 dB

7.1.3 Comparator Subsystem With Digital Output Signals SIN_{TTL} and COS_{TTL}

In this section, the performance of the comparator with hysteresis that converts the single-ended analog signals SIN and COS into digital signals was tested.

The focus was on the propagation delay of the comparator output signals SIN_{TTL} and COS_{TTL} at the host connector J4 versus the analog input at the ADS7254 for the high-resolution path as well as the single-ended analog signals for the analog path.

The aim of the test was to measure the overall signal delay of the comparator path versus the analog path, considering the delays introduced by hysteresis, phase shift due to low-pass filtering, and the propagation delay of the comparator itself.

Since both channels SIN and COS were done absolutely symmetrical with regards to the comparator output, measurements have only been conducted with the SIN channel.

The analog signals were both measured with a single-ended probe, hence on the differential input of the ADS7254 only the positive differential signal was measured versus GND.

For the test, sinusoidal input signals were injected at the encoder connector J7, SIN_P, SIN_M and COS_P, COS_M.

For the signal path, the amplitude of the input signal was set to 1.0 V_{PP} with a frequency of 100 Hz and 150 kHz (maximum) to test the worst case scenario for the propagation delay.

Test results are shown in the following figures. Note that both the high-resolution path (at the differential input of the ADS7254) and the single-ended analog path (at connector J4 Pin 12) are compared to the comparator output (at connector J4 Pin 18).

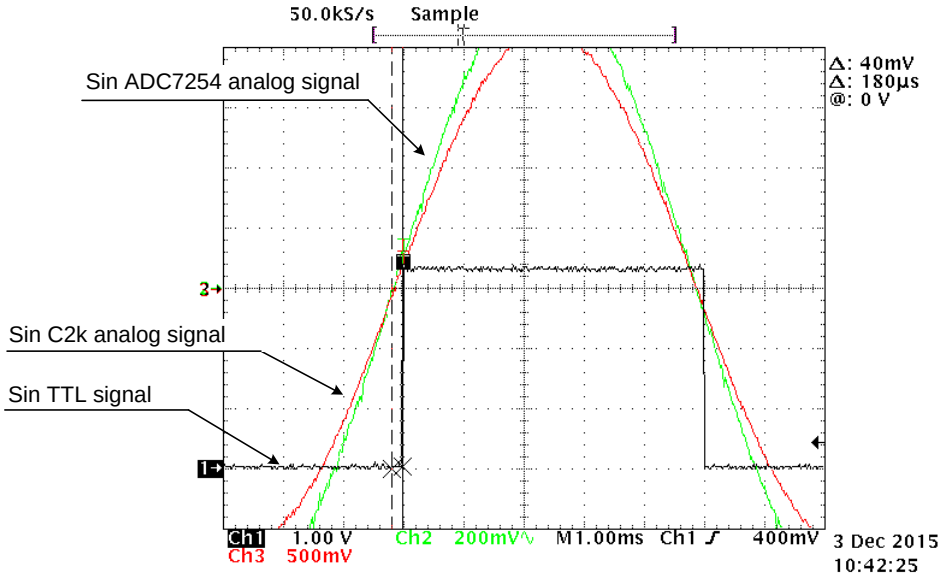


Figure 42. Comparator Output SIN_{TTL} versus Differential Input to ADS7254 and Analog Output SIN (J4-12) With Input 1.0 V_{PP}, 100 Hz at Encoder Connector J7-4, J7-5

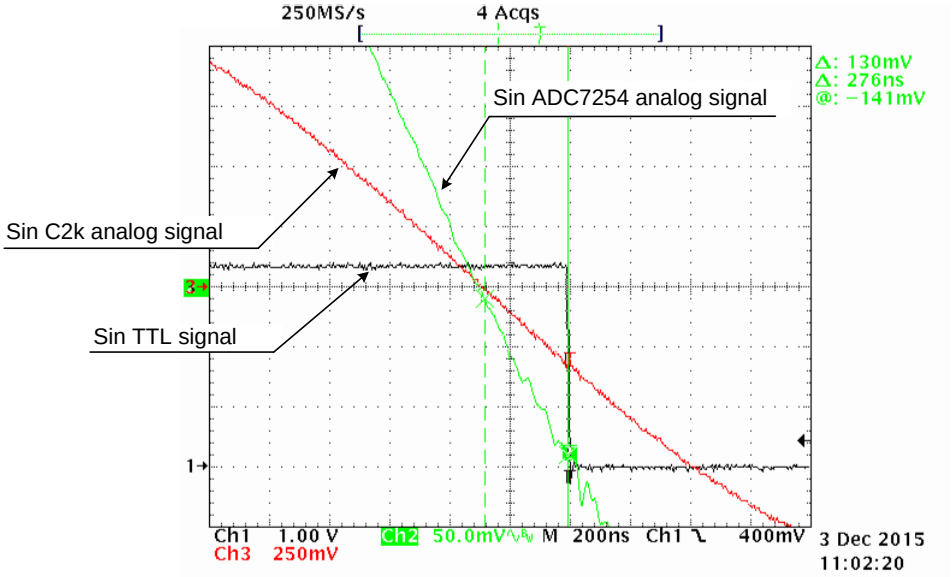


Figure 43. Comparator Output SIN_{TTL} versus Differential Input to ADS7254 and Analog Output SIN (J4-12) With Input 1.0 V_{PP}, 150 kHz at Encoder Connector J7-4, J7-5

As expected, the maximum overall phase shift including RC filter decoupling networks occurs at 150 kHz is total around 276 ns, equal to 15 degrees, hence well below the 30 degrees per specification in Section 2. The very low propagation delay of the TLV3202 with typically 40 ns has a major impact on this low number. This also gives a major margin to compensate all the possible spreads in the parameters influencing the amount of phase delay due to low-pass filters, and especially a larger margin on the host MCU with regards to synchronized sampling of the analog signals versus the incremental counter.

The propagation delay at 100 Hz is almost the same than for the high-resolution channel because the delay at lower frequencies is dominated by the amplitude-dependent hysteresis.

In a second step, only the delay related to the comparator with hysteresis was measured. The delay was specified as the input to the comparator (analog signal at R41) and the output of the comparator.

The delay introduced by the comparator block only (hysteresis and comparator propagation delay) has been measured and is listed in Table 36.

Table 36. Hysteresis Comparator Subsystem Delay

INPUT AT ENCODER CONNECTOR	VOLTAGE AT COMPARATOR INPUT (SUCH AS R41)	PROPAGATION DELAY	PHASE DELAY
1.0 V_{PP}, 100Hz	1.67 V	180 µs	6.5 degrees
1.0 V_{PP}, 150 kHz	0.9 V	276 ns	14.9 degrees

7.2 Digital Parameter Channel Performance Tests

7.2.1 RS-485 Eye Diagrams versus Cable Length

The following figures show the eye diagrams using random NRZ data measured differentially with 130-Ω termination at the cable end (slave receive side) with a differential Tektronix probe. The master transmitter clock rate was connected to channel 1 of the scope to trigger sampling of the differential data at the far cable end. The master clock was measured single ended at the input of the master RS-485 clock transmitter and is shown as reference (Ch1, 5 V/div, 25 ns) on the scope plots as well.

Measurements were conducted at cable lengths of 33 m and 3 m with maximum data rates as well as with the maximum rate specified per HIPERFACE for the HVD72.

Measurements at 33-m Cable Length

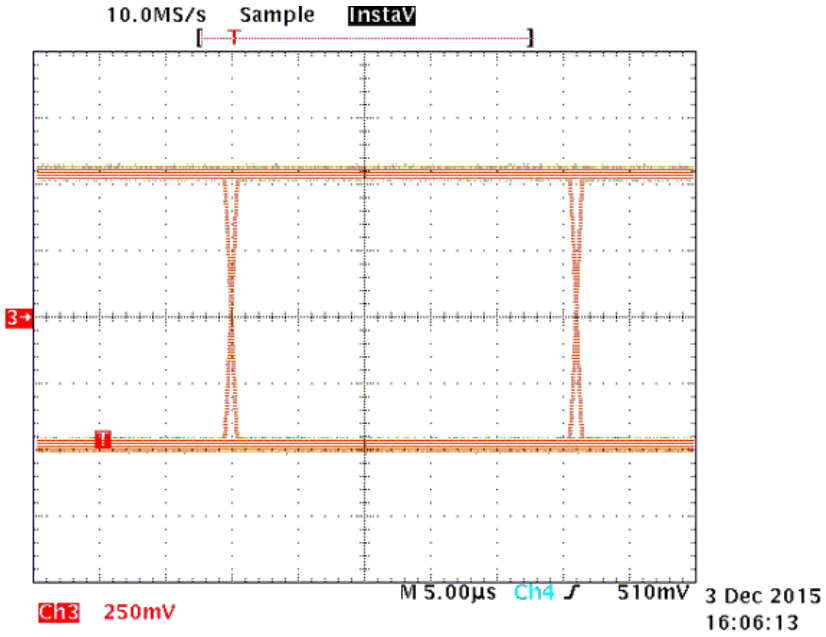


Figure 44. Eye Diagram HVD72, 33-m Cable Data Rate 38.4 kbaud

Measurements at 3-m Cable Length

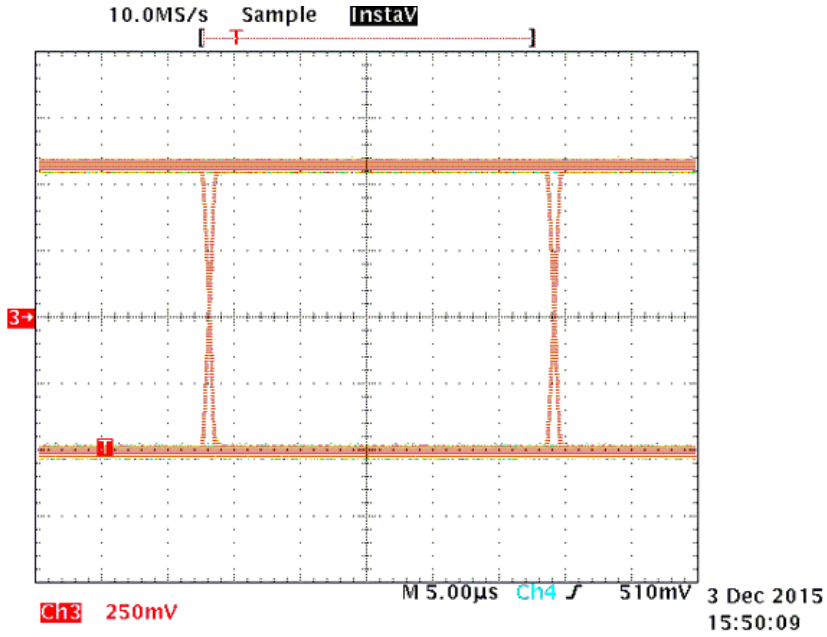


Figure 45. Eye Diagram HVD72, 3-m Cable Data Rate 38.4 kbaud

7.2.2 RS-485 Transceiver Propagation Delay and Differential Output Levels

Figure 46 shows the transmit data levels measured single-ended versus GND at the HIPERFACE SubD-9 connector pins Data+ and Data– with a 3-m cable and 1230-Ω parallel termination at the far end. The high level is around 2.8 V and the low level around 0.8 V. When comparing with the datasheet, this is around 15% lower. The reason is that in transmit direction the 10-Ω pulse proof resistors between the output terminals COS and SIN parallel termination impedance form a voltage divider with a factor of 122 Ω/142 Ω, which is approximately 0.86.

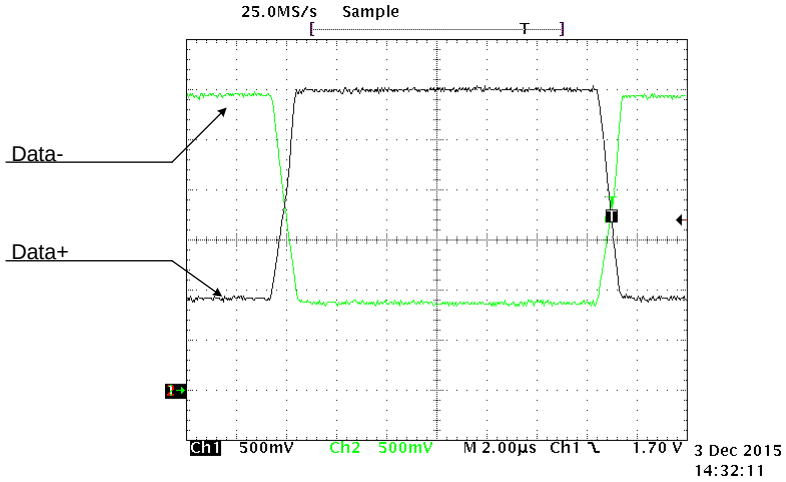


Figure 46. Voltage versus GND Connector J7 Terminals DATA+ and DATA– in Data Transmit Mode

Figure 47 and Figure 48 show the rise and fall time propagation delay of the SN65HVD72 RS-485 transceiver driver and receiver with 122-Ω parallel termination. Note the different time scale for driver and receiver measurement. The driver propagation delay measured is around 0.7 µs, the receiver propagation delay is around 75 ns.

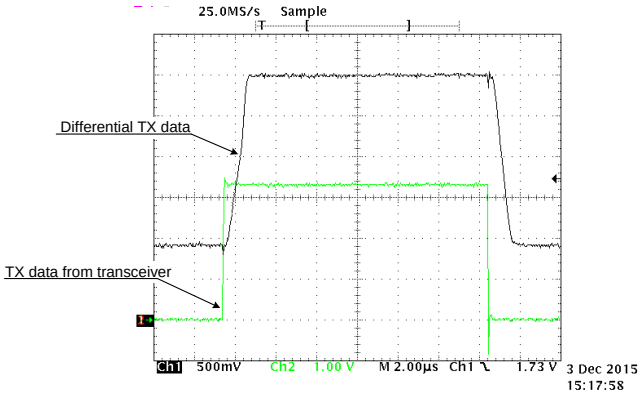


Figure 47. SN65HVD72 Propagation Delay for the Driver

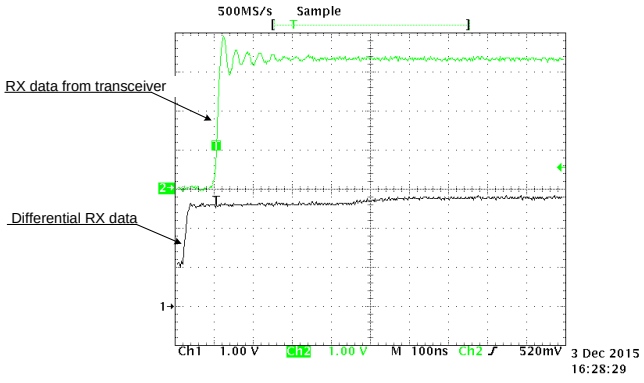


Figure 48. SN65HVD72 Propagation Delay for the Receiver

7.3 Power Supply Tests

7.3.1 24-V DC/DC Input Supply

The following tests were performed to characterize the DC/DC buck converter, which converts the 24-V to a 12-V intermediate rail.

7.3.1.1 Load-Line Regulation

The line-load regulation is within the ±10-mV range over the full working conditions. V_{OUT} is the expected 12 V ±2% (regulator's accuracy) plus the accuracy of the resistor divider R7/R10.

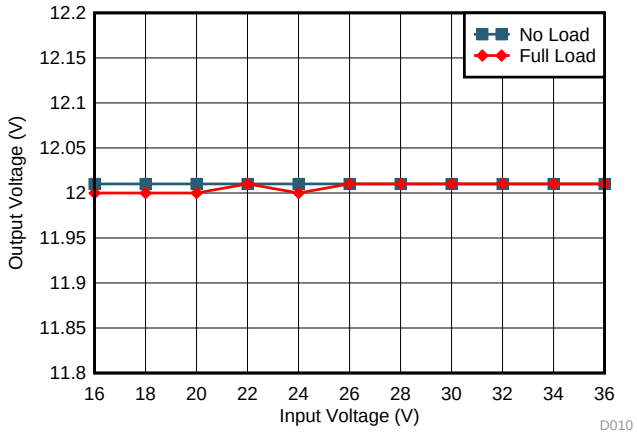


Figure 49. Load-Line Regulation 24-V to 12-V Rail

7.3.1.2 12-V Output Voltage Ripple

The V_{OUT} ripple at 12 V is below 15 mV_{PP}.

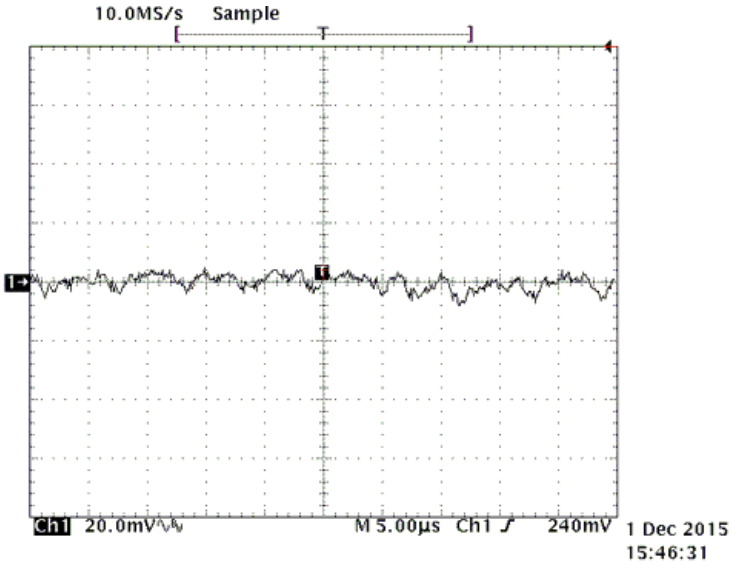


Figure 50. Output Voltage Ripple at 24-V Input, Nominal Load at 22°C Ambient Temperature

7.3.2 Encoder Power Supply Output Voltage

The output voltage of the LDO providing the supply for the encoder is well regulated and meets the spec requirements, as for the measurements in Figure 51.

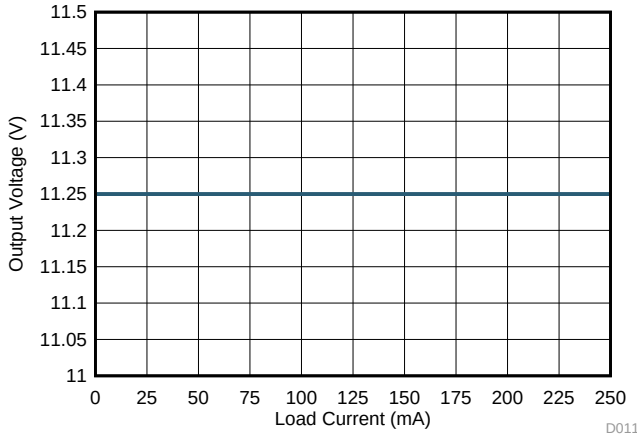


Figure 51. Encoder Power Supply Output Voltage versus Load Current (0 to 250 mA)

The LDO has a shutdown mode when excess current is drawn from the device. Figure 52 shows the shutdown when a short circuit is done on the output.

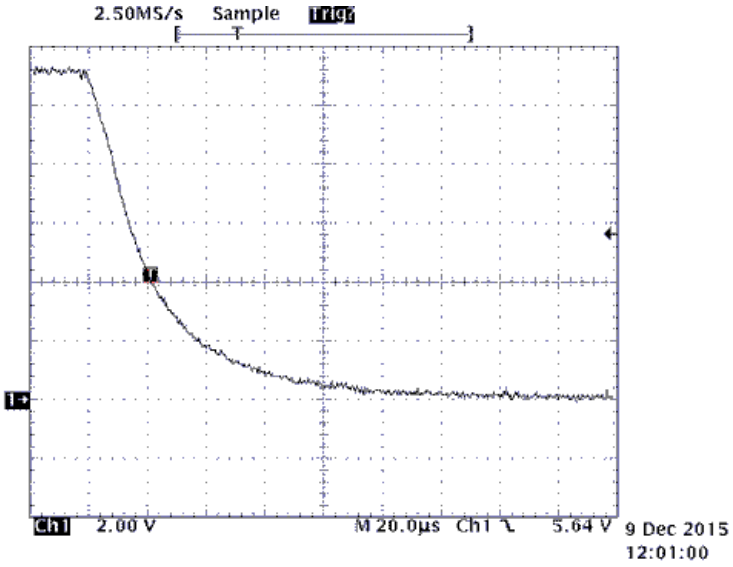


Figure 52. Shutdown of the Encoder Power Supply During a Short Circuit

This feature can be used with the error pin to detect a short circuit and turn off the encoder power supply from the processor. For more details on this option, see the LP2954 datasheet (SNVS096).

7.3.3 5-V and 3.3-V Point-of-Load

The following tests were performed to characterize the DC/DC buck converter, which converts the 12-V to a 5-V rail directly.

7.3.3.1 Output Voltage Regulation

Table 37. Measured Output Voltage

SPECIFIED OUTPUT VOLTAGE	MEASURED VOLTAGE	CURRENT
5 V	5.02 V	0 mA
5 V	5.00 V	400 mA

7.3.3.2 5-V Output Voltage Ripple

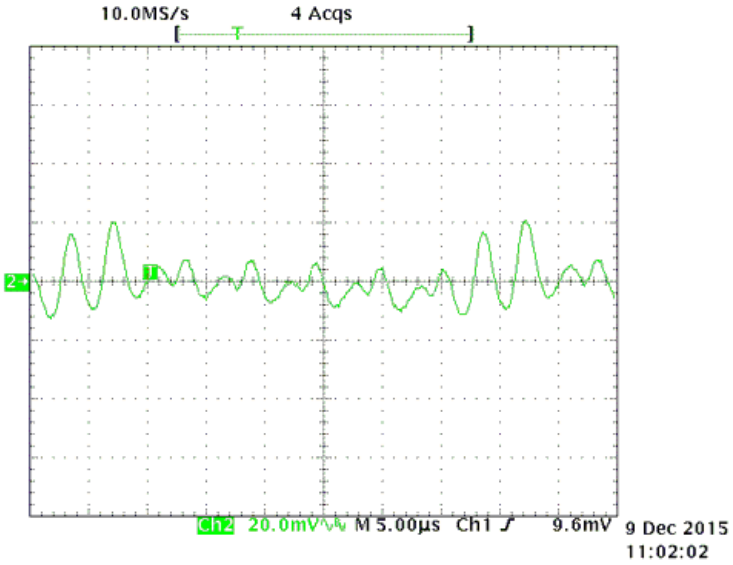


Figure 53. Output Voltage Ripple at 5-V Input at Light Load 25 mA at 22°C Ambient Temperature

The ripple is due to the low power consumption of the design. Due to this, the TPS is in an eco-mode, which gives the ripple as seen in Figure 53. If the 5-V rail was used for several other components, drawing more current, this ripple will be smaller.

7.3.3.3 Typical Current Consumption at 3.3 V and 5 V

The nominal current consumption on the 3.3-V and 5-V rails was measured with a HIPERFACE encoder connected and the F28069M LaunchPad triggering a new measurement at 16 kHz.

Table 38. Measured Output Voltage

SPECIFIED OUTPUT VOLTAGE	MEASURED VOLTAGE AT NOMINAL LOAD	NOMINAL CURRENT
5 V	5.02 V	25.5 mA
3.3 V	3.34 V	2.9 mA

The average load current at 3.3 V is expected low due to low power ADS7254, the TLV3202 as well as SN65HVD72 low quiescent current. The HIPERFACE digital data transmission occurs at 10 Hz, hence the average time of the transceiver active is below 5%.

7.4 System Performance

7.4.1 HIPERFACE Encoder Sin/Cos Output Signal Emulation

For this purpose, the encoder output signals have been emulated. Sinusoidal test signals from DC up to 150 kHz were injected into the differential inputs SIN+,SIN– and COS+,COS–. The same signal was injected into both channels. The data was captured at a 16-kHz sample rate.

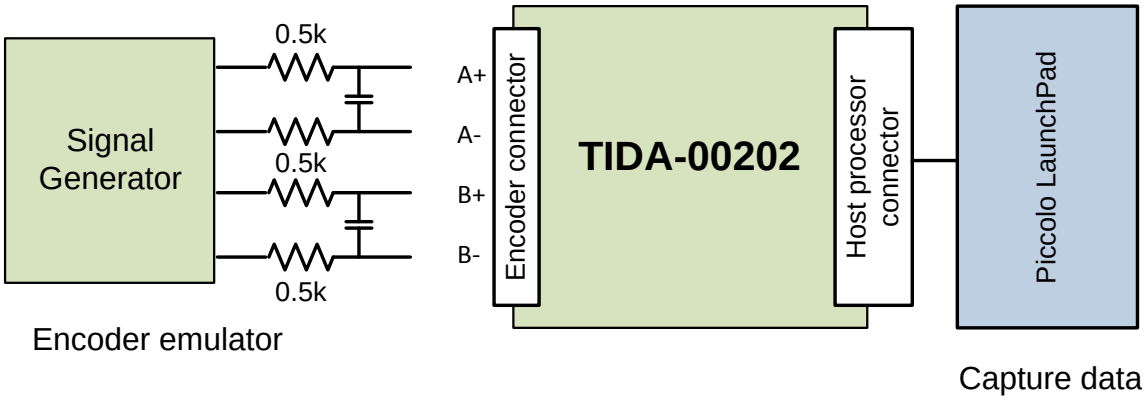


Figure 54. Test Setup for Encoder Signal Emulation

7.4.1.1 One Period (Incremental Phase) Test

To eliminate a gain, offset, and phase shift with a dual signal generator, the following setup was applied: Only one output signal of a sine generator was low-pass filtered as shown in Figure 54 and injected to both inputs SIN and COS at the encoder connector J7 of the TIDA-00202, hence feeding with the same signal. This will eliminate the limitation of the function generator. Furthermore, any mismatch amongst the two channels of the ADS7254 (and their respective signal conditioning paths) as well as the analog single-ended output with the dual ADC from the C2000 Piccolo MCU can be better evaluated.

The data has been acquired at a 16-kHz sample rate using the F28069M LaunchPad connected to the TIDA-00202, as outlined in Section 6.

After the ADS7254 channel SIN and COS data had been acquired by the F28069M, the 12-bit raw data was dumped into an Excel file. Then the raw data for channel COS has been exactly phase shifted by 90 degrees. After that, the phase was calculated using the inverse tangent of the raw data SIN and 90-degree phase shifted raw data COS.

This test has been done for a 1.0-V_{PP} amplitude and a frequency of 10 Hz and 1 kHz. The result is shown in the following figures.

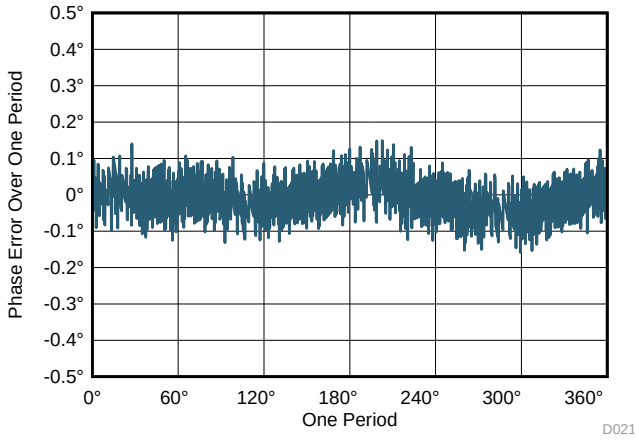


Figure 55. Phase Error Over One Signal Period When 1.0-V_{PP}, 10-Hz Input is Applied on ADS7254 Signal Chain

Within one incremental line (one signal period = 360 degrees), the phase error remains well within ±0.15 degrees. This corresponds to an error of ±0.15/360 = 0.0417%. With respect to a 12-bit resolution, this equals to around ±2 LSB only.

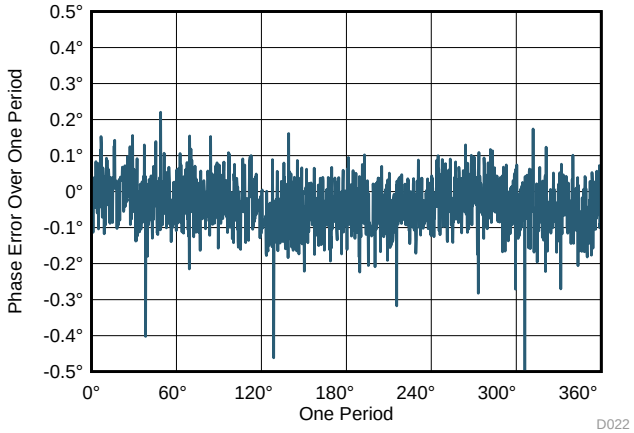


Figure 56. Phase Error Over One Signal Period When 1.0-V_{PP}, 10-Hz Input is Applied on F28069 Signal Chain

Within one incremental line (one signal period = 360 degrees), the phase error remains well within ±0.5 degrees. This corresponds to an error of ±0.3/360 = 0.0833%. With respect to a 12-bit resolution, this equals to around ±4 LSB only.

The noise distribution is even within ±0.1 (±1 LSB).

Note that an error of ±0.15 degrees over one signal period will correspond to a total error of ±110 micro-degrees (0.3969 arc seconds) for an encoder with 1024 line counts.

7.4.1.2 One Mechanical Revolution Test at Maximum Speed (150 kHz)

For this test, the high-resolution interpolated angle over one mechanical revolution was calculated within the TIDA-00202 connected to the Piccolo F28069M LaunchPad. The sample rate was set to 16-kHz at 80-MHz CPU clock.

The aim of the test was to verify the interpolation algorithm works at maximum input signal frequency of 150 kHz without missing any incremental count or mismatching the interpolated phase (arc tangent) and the corresponding line count (QEP), for example due to mismatch of latching the analog samples and the QEP counter.

For that purpose, a 360-degree spin of the encoder has been emulated using the dual signal generator. The test was performed with the dual output signal generator in the following way: The two output signals are coupled in amplitude and frequency with a 90-degree phase shift. The two signals are then applied as input at the TIDA-00202 encoder connector J9 SIN+,SIN– and COS+,COS– pins.

The total interpolated angle was stored in the F28069M RAM and read through CCS memory dump.

The calculated high-resolution angle is compared with an ideal phase assuming an encoder with 1024 line counts. Therefore, 1024 signal periods at 150 kHz equal one emulated revolution. The total angular phase ramps at a rate of 360 degrees × (150 kHz / 1024) = 52,734 degrees/second. Table 39 provides the timings for 1 µs and 100 ns, which equals one F28069M CPU clock at 80 MHz.

Table 39. Angular Speed for HIPERFACE Encoder With Line Count 1024 Running at Approximately 8800 rpm

IDEAL ANGULAR SPEED	ANGLE CHANGE IN 1 µs	ANGLE CHANGE IN 100 ns (SPI CLOCK)
52.734 degrees/second	0.052734 degrees	0.005 degrees

Figure 57 shows the interpolated angle error assuming an ideal ramp (150 kHz, 1024 signal periods per revolution) measured at 16 kHz, which yields 109 consecutive samples per revolution.

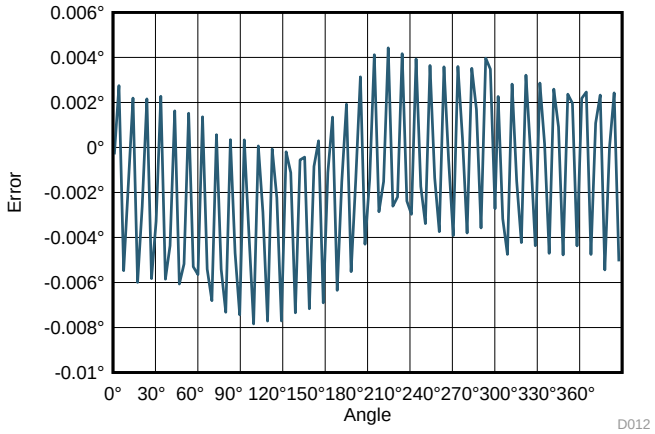


Figure 57. Error of the Interpolated Angle Over One Revolution With Encoder Emulation (1-V_{PP}, 150-kHz Input at 16-kHz Sampling)

The aim was not to test for accuracy, but to verify that no increment was lost. With a 1024 line count emulation, one incremental line count would correspond 360/1024 = 0.35 degrees. The angle error (difference) to ideal straight line remains within around ±0.06 degrees.

Therefore, the high-resolution angle interpolation algorithms work well at up to 150 kHz and no incremental count is lost.

The reason for the systematic angle error over one revolution is due to jitter with the F28069 software to trigger the SPI transfer /CS of ±1 SPI clock cycle (100 ns). The falling edge of /CS latches the analog input. Just a lead or lag due to a jitter of 100 ns translates into a phase difference of around 100 ns × 150 kHz × 360/1024 degrees ~ 0.005 degrees. This exact systematic angle error can be seen in Figure 57. This can be fixed in the software by synchronizing the peripherals in the hardware.

7.4.2 HIPERFACE Encoder System Tests

Systems tests have been done for both analog signal channel options 1 and 2 with HIPERFACE encoders SRS50-HWA0-K21 with a cable length of 3 and 33 m.

The following static angle tests have been done with a SRS50-HWA0-K21 HIPERFACE Encoder at 3- and 33-m cable length. A picture of the test setup is shown in Figure 58.

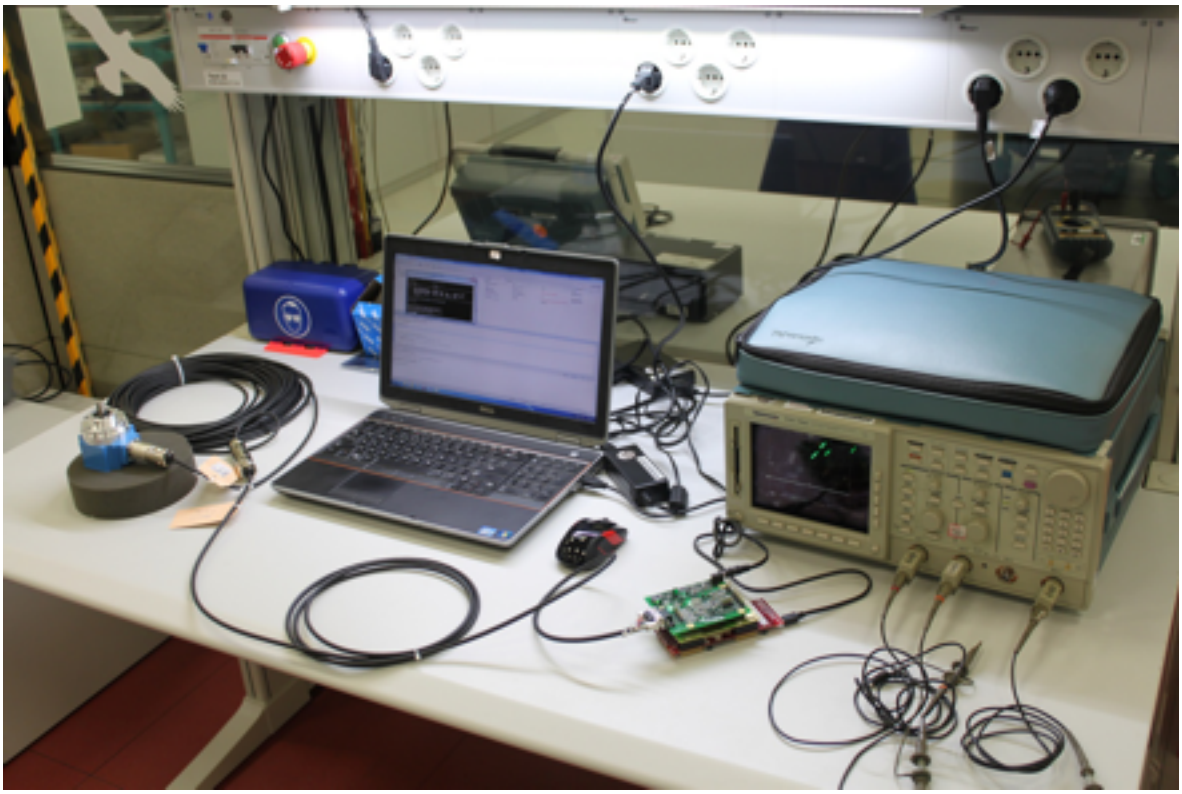


Figure 58. TIDA-00202 Test Setup With 3-m Cable (Other Option is 33 m) and SRS50-HWA0-K21 HIPERFACE Encoder

The following figures show the measured angle and angle distribution with the SRS50-HWA0-K21 over time for a static angle at 3- and 33-m cable length accordingly. The shaft was not fixed.

7.4.2.1 Functional System Tests With ADS7254 Dual ADC Channel

Note that the absolute angle for the 3- and 33-m measurements slightly changed due to mechanical vibrations when unscrewing the 3-m cable from the encoder and mounting the 33-m cable instead.

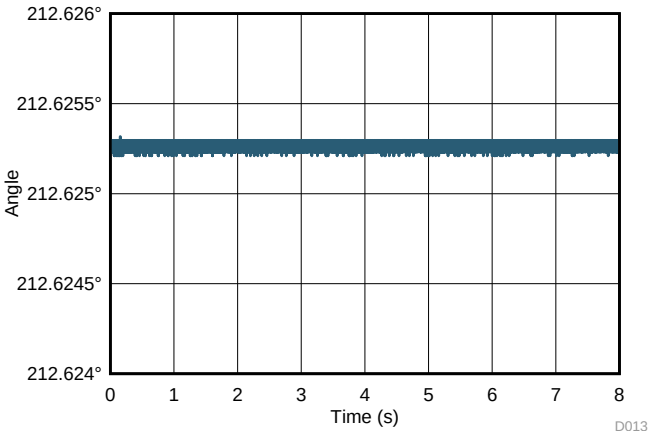


Figure 59. System Test, Measured Angle Distribution With SRS50-HWA0-K21 at 3-m Cable Length With ADS7254 Signal Path

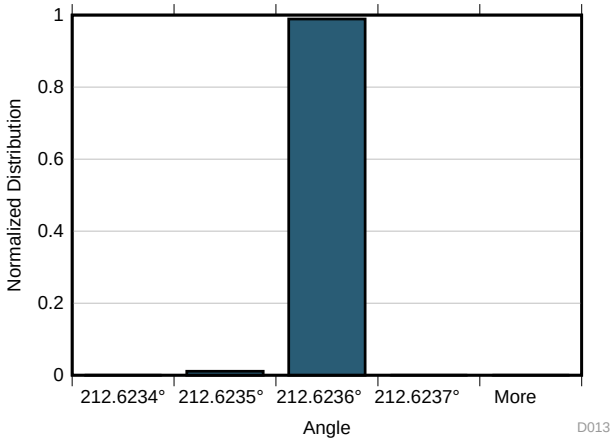


Figure 60. Angle Distribution (Histogram) 3-m Cable With ADS7254 Signal Path (8192 Samples Total)

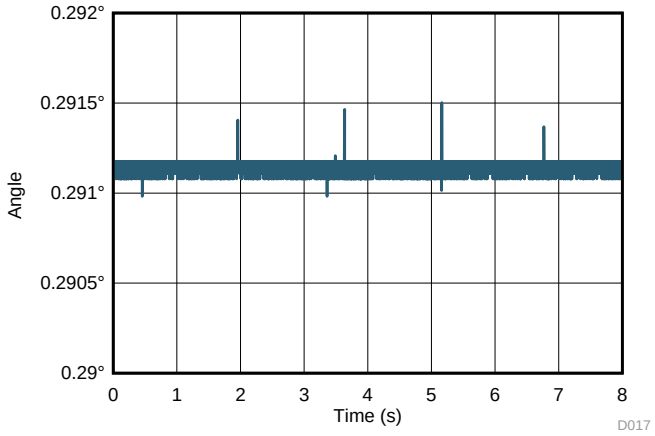


Figure 61. System Test, Measured Angle Distribution With SRS50-HWA0-K21 at 33-m Cable Length With ADS7254 Signal Path

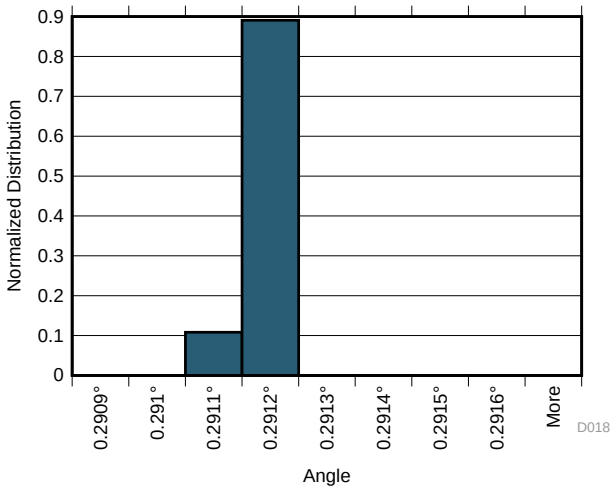


Figure 62. Angle Distribution (Histogram) 3-m Cable With ADS7254 Signal Path (8192 Samples)

7.4.2.2 Functional System Tests With Single-Ended Analog Channel and F28069M Dual ADC

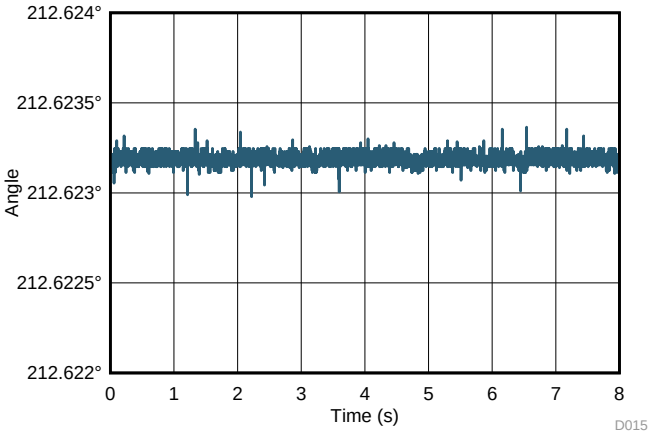


Figure 63. System Test, Measured Angle Distribution With SRS50-HWA0-K21 at 3-m Cable Length With Analog Single-Ended Path and Dual ADC With F28069M

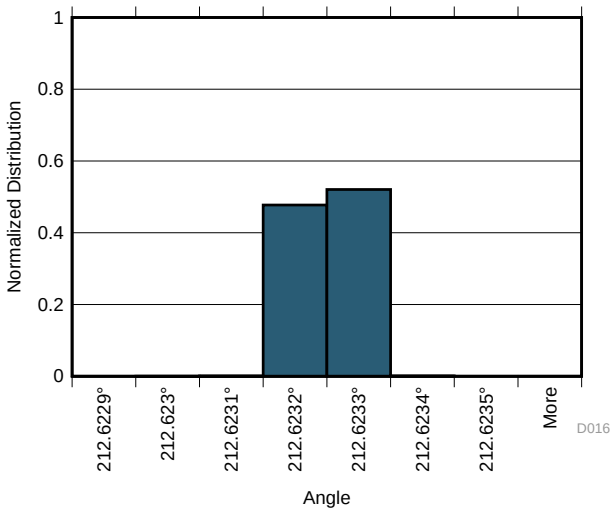


Figure 64. Angle Distribution (Histogram) With 3-m Cable for Analog Single-Ended Path and Dual ADC With F28069M (8192 Samples Total)

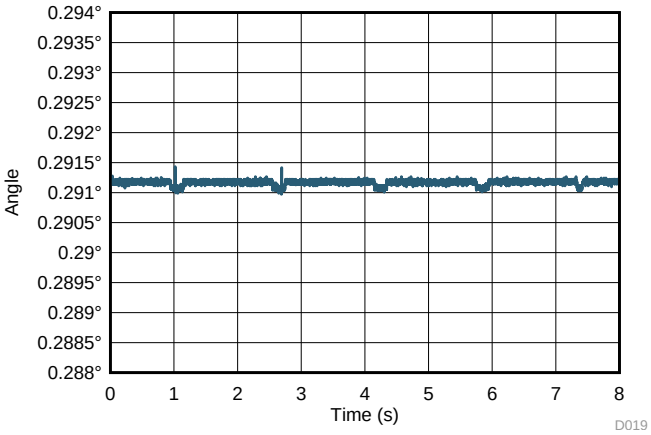


Figure 65. System Test, Measured Angle Distribution With SRS50-HWA0-K21 at 33-m Cable Length With Analog Single-Ended Path and Dual ADC With F28069M

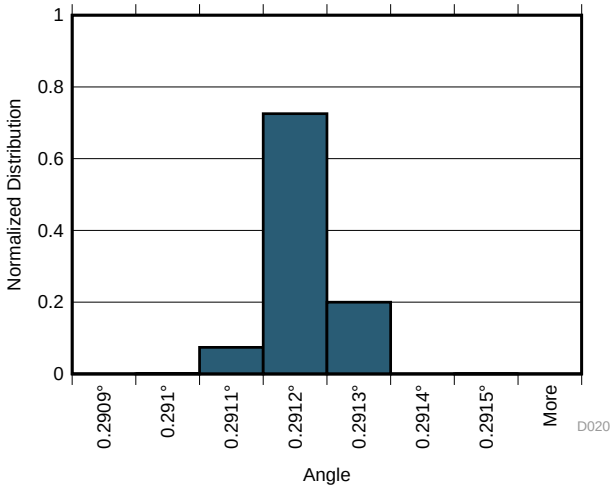


Figure 66. Angle Distribution (Histogram) With 33-m Cable for Analog Single-Ended Path and Dual ADC With F28069 (8192 Samples Total)

The measured angle with the SRS50-HWA0-K21 has a noise distribution of ±0.0003 degrees (1.08 arc seconds). There is no significant difference between the 3- and 33-m measurement because the attenuation of the cable was around –1.5 dB at 0 Hz.

7.4.2.3 Host Processor Interface Analog Single-Ended Signals and Digital Parameter Channel Signals at 9600 Baud

Figure 67 shows the analog and digital signals generated from the HIPERFACE encoder. The signals are measured on the host processor connector J4.

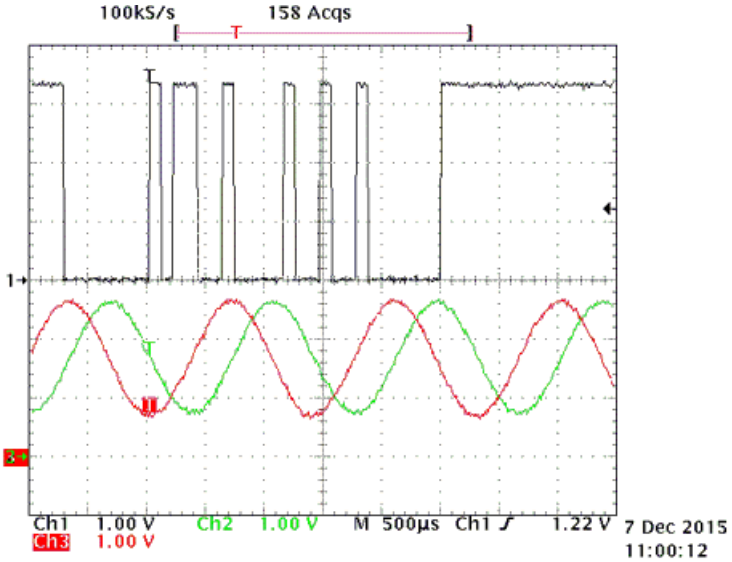


Figure 67. System Test, Digital and Analog Signals of the HIPERFACE Position Encoder Measured at J4

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00202.

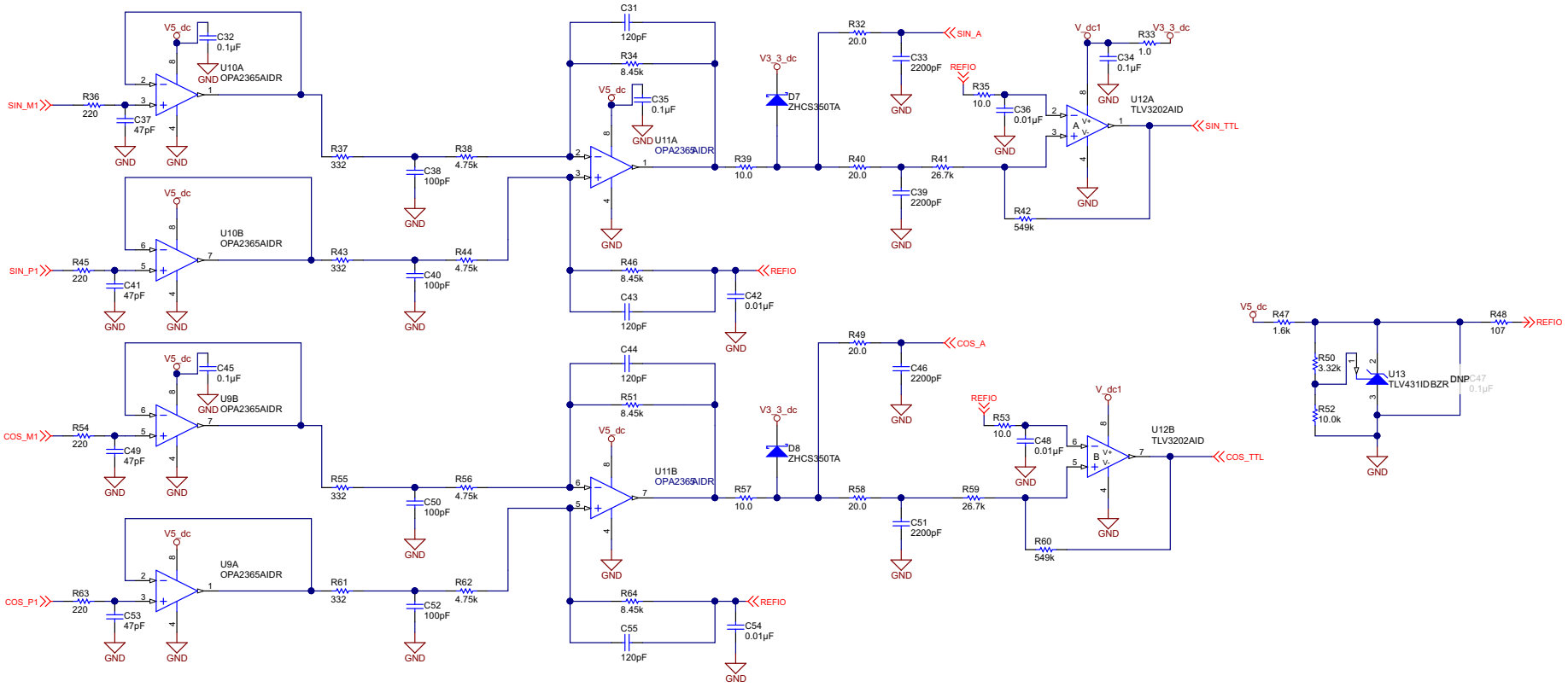


Figure 68. HIPERFACE SIN/COS Signal Path Option 1 Dual ADC With SPI Output Schematic

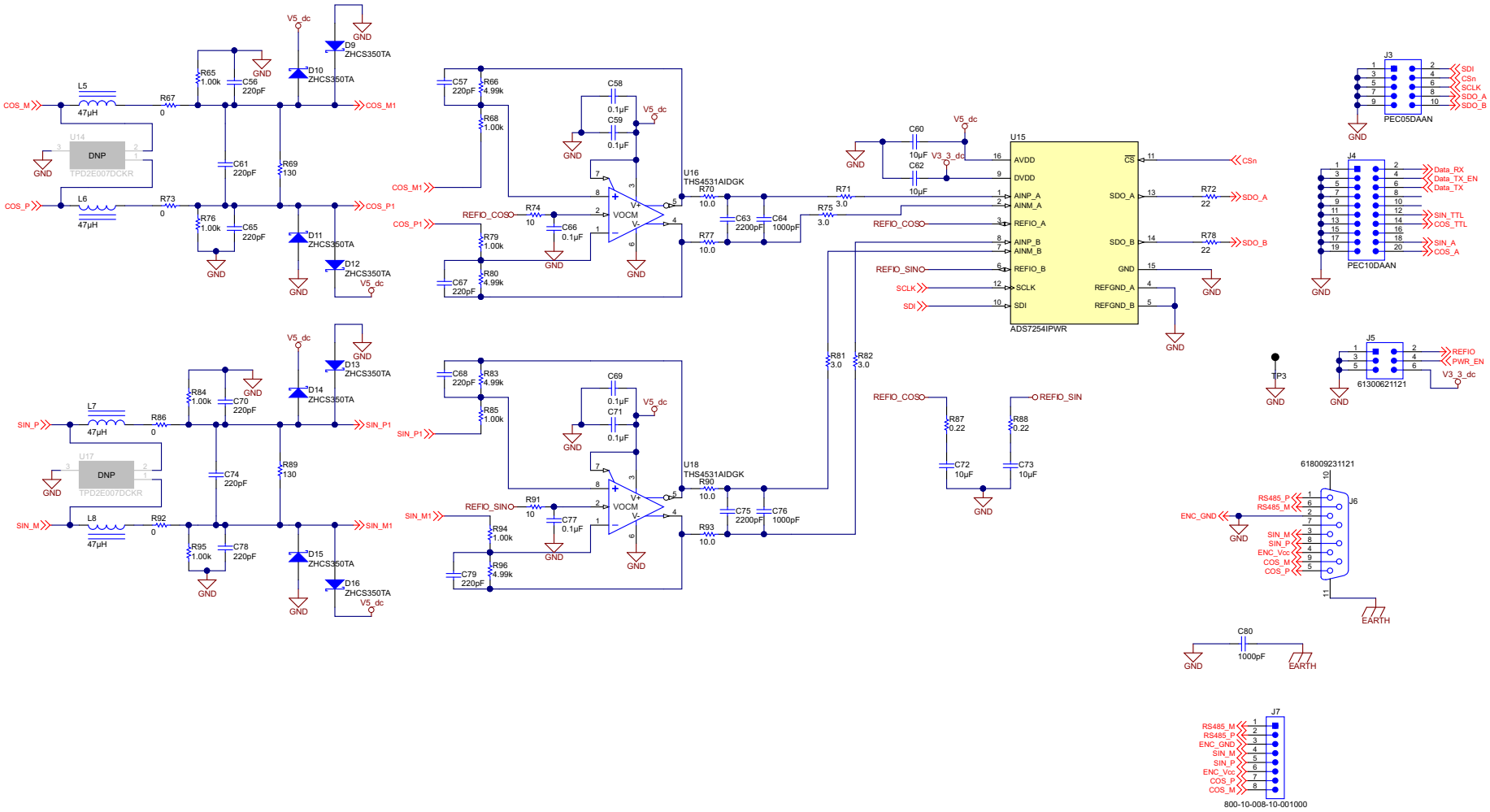


Figure 69. HIPERFACE SIN/COS Signal Path Option 2 Dual Analog Output Schematic

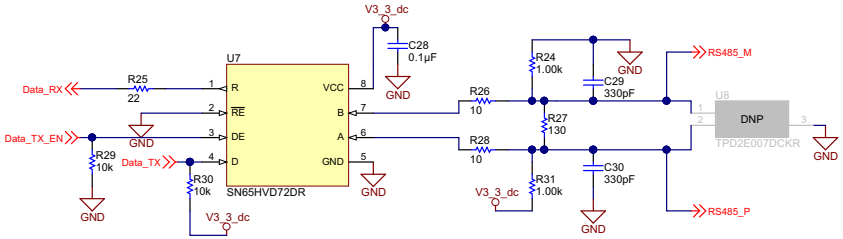


Figure 70. RS-485 Schematic

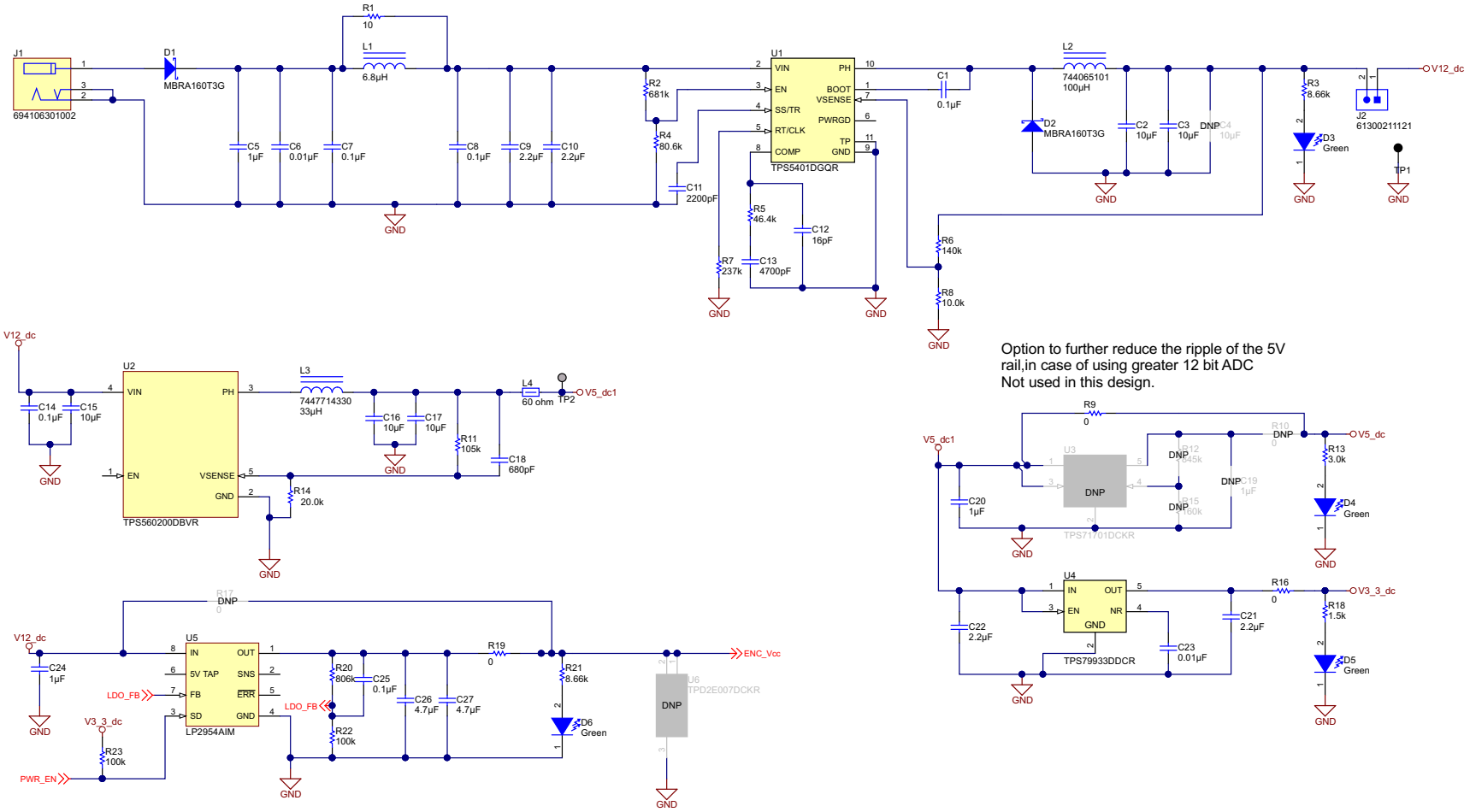


Figure 71. Power Management Schematic

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00202.

Table 40. BOM

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE	FITTED
1	!PCB1	Printed Circuit Board	Any	TIDA-00202		Fitted
4	C1, C7, C8, C25	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206095	0603	Fitted
2	C2, C3	CAP, CERM, 10 µF, 50 V, +/- 10%, X5R, 1206_190	TDK	CGA5L3X5R1H106K160AB	1206_190	Fitted
2	C5, C24	CAP, CERM, 1 µF, 50 V, +/- 10%, X7R, 0805_140	Wurth Elektronik	885012207103	0805_140	Fitted
1	C6	CAP, CERM, 0.01 µF, 50 V, +/- 10%, X7R, 0805	Wurth Elektronik	885012207092	0805	Fitted
2	C9, C10	CAP, CERM, 2.2uF, 50V, +/-10%, X5R, 1206	MuRata	GRM31CR61H225KA88L	1206	Fitted
1	C11	CAP, CERM, 2200 pF, 16 V, +/- 10%, X7R, 0402	Wurth Elektronik	885012205027	0402	Fitted
1	C12	CAP, CERM, 16 pF, 50 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1H160JA01D	0402	Fitted
1	C13	CAP, CERM, 4700 pF, 16 V, +/- 10%, X7R, 0402	Wurth Elektronik	885012205029	0402	Fitted
1	C14	CAP, CERM, 0.1 µF, 25 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206071	0603	Fitted
1	C15	CAP, CERM, 10 µF, 25 V, +/- 10%, X7R, 1206	Wurth Elektronik	885012208069	1206	Fitted
2	C16, C17	CAP, CERM, 10 µF, 25 V, +/- 10%, X5R, 0805	MuRata	GRM219R61E106KA12	0805	Fitted
1	C18	CAP, CERM, 680 pF, 25 V, +/- 10%, X7R, 0805	Wurth Elektronik	885012207059	0805	Fitted
1	C20	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206052	0603	Fitted
2	C21, C22	CAP, CERM, 2.2 µF, 16 V, +/- 20%, X5R, 0603	Wurth Elektronik	885012106018	0603	Fitted
1	C23	CAP, CERM, 0.01 µF, 16 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206040	0603	Fitted
2	C26, C27	CAP, CERM, 4.7 µF, 25 V, +/- 10%, X7R, 0805_140	MuRata	GRM21BR71E475KA73L	0805_140	Fitted
7	C28, C32, C34, C35, C45, C58, C69	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206046	0603	Fitted

Table 40. BOM (continued)

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE	FITTED
2	C29, C30	CAP, CERM, 330 pF, 50 V, +/- 5%, C0G/NP0, 0603	Wurth Elektronik	885012006060	0603	Fitted
4	C31, C43, C44, C55	CAP, CERM, 120 pF, 50 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1H121JA01D	0402	Fitted
6	C33, C39, C46, C51, C63, C75	CAP, CERM, 2200 pF, 50 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H222JA01D	0603	Fitted
4	C36, C42, C48, C54	CAP, CERM, 0.01 µF, 50 V, +/- 10%, C0G/NP0, 0402	MuRata	GCM155R71H103KA55D	0402	Fitted
4	C37, C41, C49, C53	CAP, CERM, 47 pF, 50 V, +/- 5%, C0G/NP0, 0402	Wurth Elektronik	885012005044	0402	Fitted
4	C38, C40, C50, C52	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0402	Wurth Elektronik	885012005061	0402	Fitted
10	C56, C57, C61, C65, C67, C68, C70, C74, C78, C79	CAP, CERM, 220 pF, 50 V, +/- 5%, C0G/NP0, 0402	Wurth Elektronik	885012005063	0402	Fitted
2	C59, C71	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206046	0603	Fitted
2	C60, C62	CAP, CERM, 10 µF, 16 V, +/- 10%, X7R, 0805_140	Samsung	CL21B106KOQNNNE	0805_140	Fitted
2	C64, C76	CAP, CERM, 1000 pF, 50 V, +/- 5%, C0G/NP0, 0402	MuRata	GRM1555C1H102JA01D	0402	Fitted
2	C66, C77	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, 0402	Wurth Elektronik	885012205037	0402	Fitted
2	C72, C73	CAP, CERM, 10 µF, 10 V, +/- 10%, X7R, 0805	Wurth Elektronik	885012207026	0805	Fitted
1	C80	CAP, CERM, 1000 pF, 2000 V, +/- 10%, X7R, 1812	AVX	1812GC102KA1	1812	Fitted
2	D1, D2	Diode, Schottky, 60V, 1A, SMA	ON Semiconductor	MBRA160T3G	SMA	Fitted
4	D3, D4, D5, D6	LED, Green, SMD	Wurth Elektronik	150060GS75000	LED_0603	Fitted
10	D7, D8, D9, D10, D11, D12, D13, D14, D15, D16	Diode, Schottky, 40 V, 0.35 A, SOD-523	Diodes Inc.	ZHCS350TA	SOD-523	Fitted
4	H1, H2, H3, H4	Machine Screw, Round, #4-40 x 1/4, Nylon, Philips panhead	B&F Fastener Supply	NY PMS 440 0025 PH	Screw	Fitted
4	H5, H6, H7, H8	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone	1902C	Standoff	Fitted
1	J1	WR-DC DC Power Jack, R/A, TH	Wurth Elektronik	694106301002	WR-DC DC Power Jack, R/A, TH	Fitted
1	J2	Header, 2.54 mm, 2x1, Gold, TH	Wurth Elektronik	61300211121	Header, 2.54mm, 2x1, TH	Fitted
1	J3	Header, 100mil, 5x2, Tin, TH	Sullins Connector Solutions	PEC05DAAN	Header, 5x2, 100mil, Tin	Fitted

Table 40. BOM (continued)

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE	FITTED
1	J4	Header, 100mil, 10x2, TH	Sullins Connector Solutions	PEC10DAAN	Header, 10x2, 2.54mm, TH	Fitted
1	J5	Header, 2.54mm, 3x2, Gold, TH	Wurth Elektronik	61300621121	Header, 2.54mm, 3x2, TH	Fitted
1	J6	Receptacle, D-Sub, 9 Position, R/A, TH	Wurth Elektronik	618009231121	Receptacle, D-Sub, 9 Position, R/A, TH	Fitted
1	J7	Header, 100mil, 8x1, TH	Mill-Max	800-10-008-10-001000	Header, 8x1, 100mil, TH	Fitted
1	L1	Inductor, Shielded, 6.8 µH, 0.88 A, 0.3682 ohm, SMD	Wurth Elektronik	74438334068	SMD, 2-Leads, Body 3.2x3.2mm	Fitted
1	L2	Inductor, Shielded Drum Core, Ferrite, 100 µH, 0.9 A, 0.33 ohm, SMD	Wurth Elektronik eiSos	744065101	WE-TPC-XLH2	Fitted
1	L3	Inductor, Shielded Drum Core, Ferrite, 33 µH, 2.5 A, 0.066 ohm, SMD	Wurth Elektronik	7447714330	10x5x10mm	Fitted
1	L4	Ferrite Bead, 60 ohm @ 100 MHz, 5.1 A, 1.6x0.8mm	Wurth Elektronik	74279228600	1.6x0.8mm	Fitted
4	L5, L6, L7, L8	Inductor, Wirewound, Ferrite, 47 µH, 0.035 A, 2.5 ohm, SMD	Taiyo Yuden	LBMF1608T470K	0603	Fitted
3	R1, R26, R28	RES, 10 ohm, 5%, 0.25W, 0603	Vishay-Dale	CRCW060310R0JNEAHP	0603	Fitted
1	R2	RES, 681 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402681KFKED	0402	Fitted
2	R3, R21	RES, 8.66 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW04028K66FKED	0402	Fitted
1	R4	RES, 80.6 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040280K6FKED	0402	Fitted
1	R5	RES, 46.4 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040246K4FKED	0402	Fitted
1	R6	RES, 140 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402140KFKED	0402	Fitted
1	R7	RES, 237 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402237KFKED	0402	Fitted
2	R8, R52	RES, 10.0 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040210K0FKED	0402	Fitted
2	R9, R19	RES, 0, 5%, 0.125 W, 0805	Vishay-Dale	CRCW08050000Z0EA	0805	Fitted
1	R11	RES, 105 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603105KFKEA	0603	Fitted
1	R13	RES, 3.0 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04023K00JNED	0402	Fitted
1	R14	RES, 20.0 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060320K0FKEA	0603	Fitted
1	R16	RES, 0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	0402	Fitted
1	R18	RES, 1.5 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K50JNED	0402	Fitted
1	R20	RES, 806 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603806KFKEA	0603	Fitted
2	R22, R23	RES, 100 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW0603100KFKEA	0603	Fitted
6	R24, R31, R65, R76, R84, R95	RES, 1.00 k, 1%, 0.1 W, 0603	Vishay-Dale	CRCW06031K00FKEA	0603	Fitted
1	R25	RES, 22, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060322R0JNEA	0603	Fitted

Table 40. BOM (continued)

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE	FITTED
3	R27, R69, R89	RES, 130, 1%, 0.4 W, AEC-Q200 Grade 0, 0805	Rohm	ESR10EZPF1300	0805	Fitted
2	R29, R30	RES, 10 k, 5%, 0.1 W, 0603	Vishay-Dale	CRCW060310K0JNEA	0603	Fitted
4	R32, R40, R49, R58	RES, 20.0, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040220R0FKED	0402	Fitted
1	R33	RES, 1.0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021R00JNED	0402	Fitted
4	R34, R46, R51, R64	RES, 8.45 k, 0.1%, 0.063 W, 0402	Panasonic	ERA-2AEB8451X	0402	Fitted
8	R35, R39, R53, R57, R70, R77, R90, R93	RES, 10.0, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040210R0FKED	0402	Fitted
4	R36, R45, R54, R63	RES, 220, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402220RJNED	0402	Fitted
4	R37, R43, R55, R61	RES, 332, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402332RFKED	0402	Fitted
4	R38, R44, R56, R62	RES, 4.75 k, 0.1%, 0.063 W, 0402	Panasonic	ERA-2AEB4751X	0402	Fitted
2	R41, R59	RES, 26.7 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW040226K7FKED	0402	Fitted
2	R42, R60	RES, 549 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402549KFKED	0402	Fitted
1	R47	RES, 1.6 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04021K60JNED	0402	Fitted
1	R48	RES, 107, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402107RFKED	0402	Fitted
1	R50	RES, 3.32 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW04023K32FKED	0402	Fitted
4	R66, R80, R83, R96	RES, 4.99 k, 0.1%, 0.063 W, 0402	Panasonic	ERA-2AEB4991X	0402	Fitted
4	R67, R73, R86, R92	RES, 0, 5%, 0.1 W, 0603	Vishay-Dale	CRCW06030000Z0EA	0603	Fitted
4	R68, R79, R85, R94	RES, 1.00 k, 0.1%, 0.063 W, 0402	Panasonic	ERA-2AEB102X	0402	Fitted
4	R71, R75, R81, R82	RES, 3.0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04023R00JNED	0402	Fitted
2	R72, R78	RES, 22, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040222R0JNED	0402	Fitted
2	R74, R91	RES, 10, 5%, 0.063 W, 0402	Vishay-Dale	CRCW040210R0JNED	0402	Fitted
2	R87, R88	RES, 0.22, 1%, 0.1 W, 0603	Panasonic	ERJ-3RQFR22V	0603	Fitted
2	TP1, TP3	Test Point, Miniature, Black, TH	Keystone	5001	Black Miniature Testpoint	Fitted
1	U1	Buck Step Down Regulator with 3.5 to 42 V Input and 0.8 to 39 V Output, -40 to 150 degC, 10-Pin MSOP-PowerPAD (DGQ), Green (RoHS & no Sb/Br)	Texas Instruments	TPS5401DGQR	DGQ0010D	Fitted
1	U2	4.5V to 18V Input, 500mA Synchronous Step Down SWIFT Converter with Advanced Eco-mode, DBV0005A	Texas Instruments	TPS560200DBVR	DBV0005A	Fitted
1	U4	Single Output High PSRR LDO, 200 mA, Fixed 3.3 V Output, 2.7 to 6.5 V Input, with Low IQ, 5-pin SOT (DDC), -40 to 85 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TPS79933DDCR	DDC0005A	Fitted

Table 40. BOM (continued)

QTY	DESIGNATOR	DESCRIPTION	MANUFACTURER	PARTNUMBER	PACKAGE REFERENCE	FITTED
1	U5	5V Micropower Low-Dropout Voltage Regulator, 8-pin Narrow SOIC	Texas Instruments	LP2954AIM	M08A	Fitted
1	U7	3.3V-Supply RS-485 with IEC ESD Protection, D0008A	Texas Instruments	SN65HVD72DR	D0008A	Fitted
3	U9, U10, U11	50 MHz, Low-Noise Single-Supply Rail-to-Rail Operational Amplifier, 2.2 to 5.5 V, -40 to 125 degC, 8-pin SOIC (D0008A), Green (RoHS & no Sb/Br)	Texas Instruments	OPA2365AIDR	D0008A	Fitted
1	U12	40-ns, microPOWER, Push-Pull Output Comparators, D0008A	Texas Instruments	TLV3202AID	D0008A	Fitted
1	U13	Low Voltage Adjustable Precision Shunt Regulator, 39 ppm / degC, 15 mA, -40 to 85 degC, 3-pin SOT-23 (DBZ), Green (RoHS & no Sb/Br)	Texas Instruments	TLV431IDBZR	DBZ0003A	Fitted
1	U15	Dual, High-Speed,12-Bit, Simultaneous-Sampling, Analog-to-Digital Converter, PW0016A	Texas Instruments	ADS7254IPWR	PW0016A	Fitted
2	U16, U18	Ultra Low Power, Rail-to-Rail Output, Fully-Differential Amplifier, DGK0008A	Texas Instruments	THS4531AIDGK	DGK0008A	Fitted
0	C4	CAP, CERM, 10 µF, 50 V, +/- 10%, X5R, 1206_190	TDK	CGA5L3X5R1H106K160AB	1206_190	Not Fitted
0	C19	CAP, CERM, 1 µF, 16 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206052	0603	Not Fitted
0	C47	CAP, CERM, 0.1 µF, 50 V, +/- 10%, X7R, 0603	Wurth Elektronik	885012206095	0603	Not Fitted
0	FID1, FID2, FID3	Fiducial mark. There is nothing to buy or mount.	N/A	N/A	Fiducial	Not Fitted
0	R10	RES, 0, 5%, 0.063 W, 0402	Vishay-Dale	CRCW04020000Z0ED	0402	Not Fitted
0	R12	RES, 845 k, 1%, 0.063 W, 0402	Vishay-Dale	CRCW0402845KFKED	0402	Not Fitted
0	R15	RES, 160 k, 5%, 0.063 W, 0402	Vishay-Dale	CRCW0402160KJNED	0402	Not Fitted
0	R17	RES, 0, 5%, 0.125 W, 0805	Vishay-Dale	CRCW08050000Z0EA	0805	Not Fitted
0	U3	Single Output LDO, 150 mA, Adjustable 0.9 to 6.2 V Output, 2.5 to 6.5 V Input, with High-Bandwidth PSRR, 5-pin SC70 (DCK), -40 to 125 degC, Green (RoHS & no Sb/Br)	Texas Instruments	TPS71701DCKR	DCK0005A	Not Fitted
0	U6, U8, U14, U17	ESD Protection Array for AC Signal Data Interface, 2 Channels, -40 to +85 degC, 3-pin SC70 (DCK), Green (RoHS & no Sb/Br)	Texas Instruments	TPD2E007DCKR	DCK0003A	Not Fitted

8.3 PCB Layout

The design is done using a four-layers PCB. One of these layers is used for one complete ground plane and another as a power plane.

Layout guidelines can be also found in the datasheets of the TI parts used in the TIDA-00202.

8.3.1 Layout Prints

To download the layout prints, see the design files at TIDA-00202.

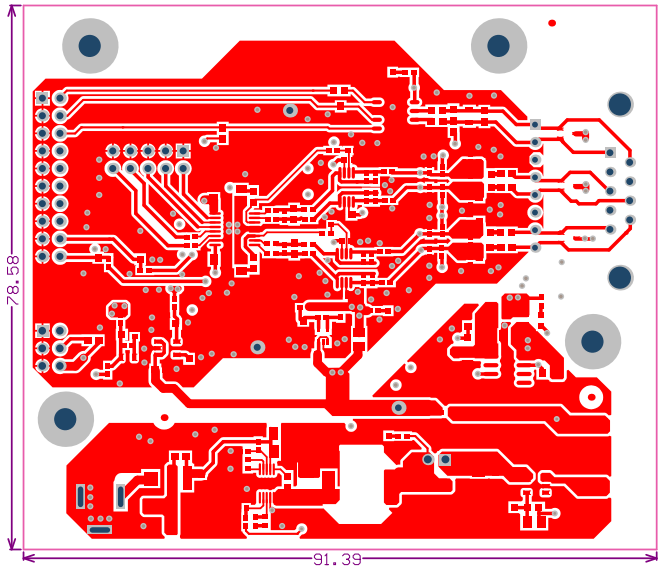


Figure 72. Top Layer

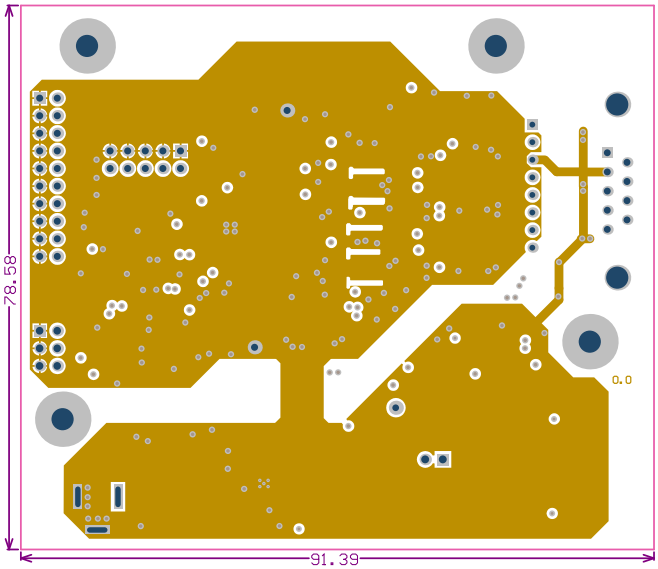


Figure 73. Mid-Layer 1 — GND Plane

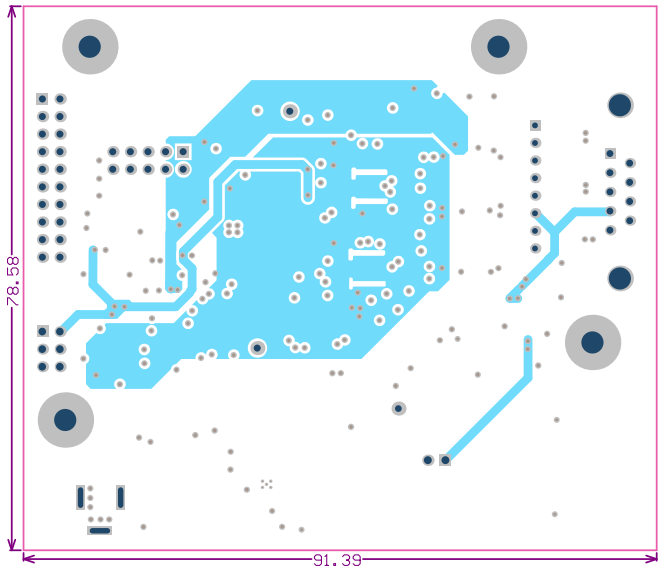


Figure 74. Mid-Layer 2 — Power Plane

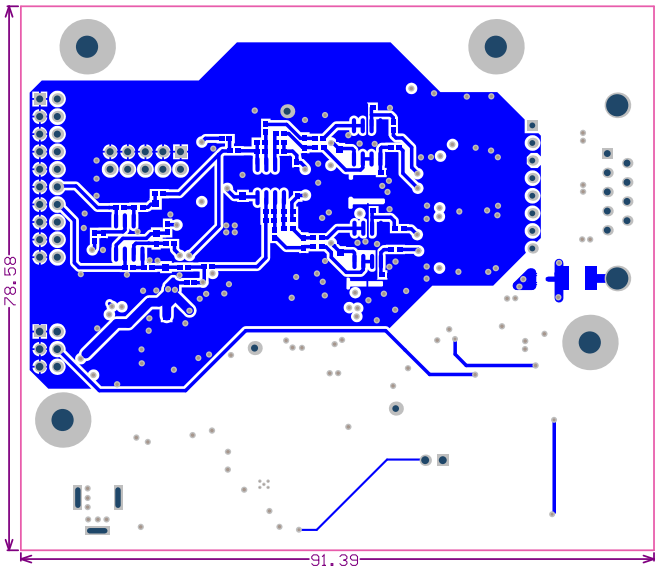


Figure 75. Bottom Layer

8.3.2 Layout Guidelines

The design follows the guidelines from the TIDA-00176, TIDA-00178, and TIDA-00179 TI Designs. For details, see the layout guidelines in their respective design guides.

8.4 Altium Project Files

To download the Altium project files, see the design files at TIDA-00202.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00202.

8.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00202.

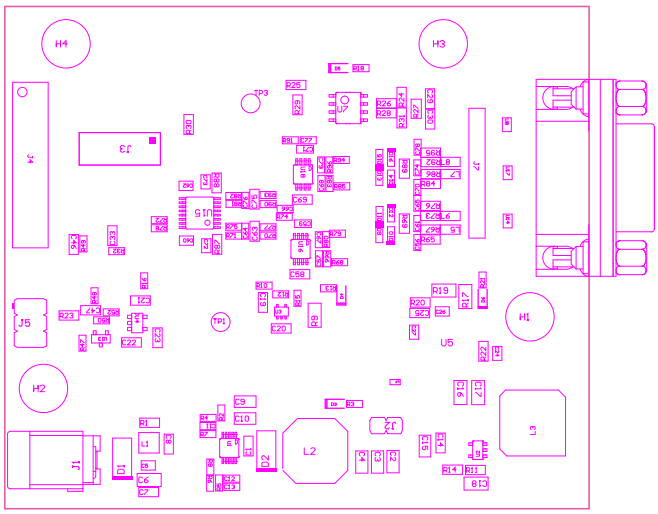


Figure 76. Top Layer

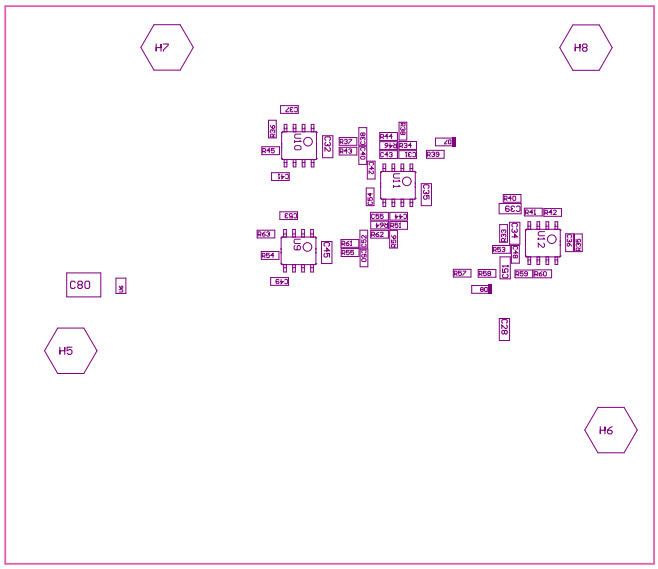


Figure 77. Bottom Layer

9 Software Files

To download the software files, see the design files at TIDA-00202.

10 References

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12. Texas Instruments, *40-ns, microPOWER, Push-Pull Output Comparators*, TLV3201 Datasheet (SBOS561)
13. Texas Instruments, *SN65HVD7x 3.3-V Supply RS-485 With IEC ESD Protection*, SN65HVD72 Datasheet (SLLSE11)
14. Texas Instruments, *TPS5401 0.5-A, 42-V Input, Step-Down SWIFT™ Converter*, TPS5401 Datasheet (SLVSAB0)
15. Texas Instruments, *TPS560200 4.5-V to 17-V Input, 500-mA Synchronous Step-Down SWIFT™ Converter With Advanced Eco-Mode™*, TPS560200 Datasheet (SLVSC81)
16. Texas Instruments, *LP2954/LP2954A 5V and Adjustable Micropower Low-Dropout Voltage Regulators*, LP2954 Datasheet (SNVS096)
17. Texas Instruments, *TPS799 200-mA, Low-Quiescent Current, Ultralow Noise, High-PSRR Low-Dropout Linear Regulator*, TPS799 Datasheet (SBVS056)
18. Texas Instruments, *TPS717 Low-Noise, High-Bandwidth PSRR, Low-Dropout, 150-mA Linear Regulator*, TPS717 Datasheet (SBVS068)

11 About the Authors

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2015) to A Revision	Page
• Changed from preview page	1

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