TI Designs – TIDA-00699

Automotive Wide Vin power frontend with cold crank operation, transient protection, and EMI filter

Design Overview

This solution was designed to be a broadly applicable automotive off-battery front end power supply for 10-15W systems. There is a focus on EMI/EMC testing and compliance as well to help designers satisfy the regulatory requirements associated with producing an automotive electronic subsystem.

Design Resources

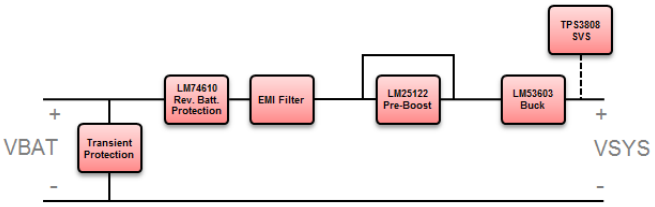
TIDA-00699	Design Folder
LM53603-Q1	Product Folder
LM25122-Q1	Product Folder
LM74610-Q1	Product Folder
TPS3808G01-Q1	Product Folder

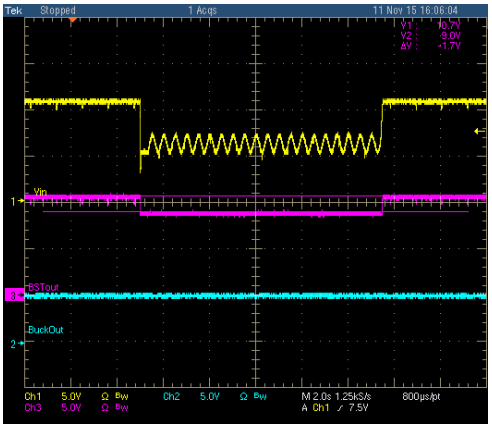
Design Features

- Wide-Vin front end power supply for 10-15W systems
- Off-Battery operation with reverse battery protection
- Designed and tested for severe cold-crank operation
- Designed and tested to ISO 7637-2:2004 Pulse 1, 2a, 3a/b and 5b (clamped load dump)
- Tested for CISPR25 Conducted and Radiated Emissions

Featured Applications

- ADAS Vision Systems
- Automotive Radar





Contents

1 Key System Specifications

PARAMETER		COMMENTS	MIN	TYP	MAX	UNIT
System Input						
V_{IN}	Input Voltage	Battery voltage range (DC)	3.1	13	36	V
$V_{CLAMP}+$	Positive Clamping Voltage	Positive input protection TVS clamping range	28.9		42.1	V
$V_{CLAMP}-$	Negative Clamping Voltage	Negative input protection TVS clamping range	15.6		25.8	V
P_{PK}	Peak Pulse Power Dissipation	Maximum TVS power dissipation		600		W
Output Voltage						
V_{OUT}	VSYS	System output voltage, across load	4.97	5	5.03	V
Output Current(s)						
I_{OUT}	VSYS	Max output current. Drawing more than 2.5A is not recommended for thermal reasons. See the Thermal Images testing to see the temperature rise at different load levels		2.5	3	A

Figure 1: System Specifications

2 System Description

This system was designed to be a generic front-end power supply for always-on systems in the car that must operate through all battery conditions. The design was done with the following points in mind:

- The system must maintain a constant output voltage over the full DC range of battery conditions specified in OEM standards or ISO 16750-2:
  - V_{IN}(min) down to 3.2V simulating a severe cold cranking condition
  - V_{IN}(max) up to 18V simulating the upper range of normal battery operation
- The system must clamp/filter high-voltage electrical fast transients and maintain operation through them:
  - These pulses include clamped Load Dump (up to 38V) and other transients outlined in ISO 7637-2:2004
- The system must properly respond to a reverse battery polarity event and shut down appropriately
- The design should be compliant with the CISPR 25 automotive EMI standard, both radiated and conducted emissions
- The layout of the board should be done in such a way to minimize the footprint of the solution while maintaining high performance

As stated above, this solution is generic to many 10-15W applications in many subsystems in the vehicle which maintain always-on operation. Below is an example of a Mono Front Camera system:

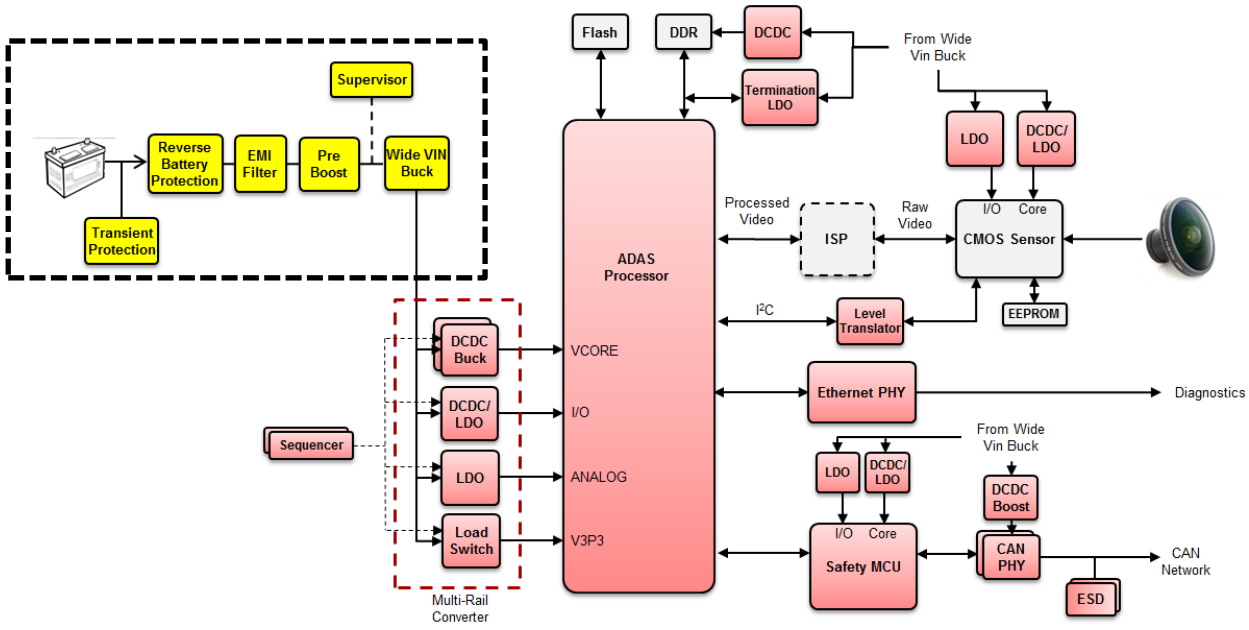


Figure 2: Example TDA3x-based Mono Front Camera Block Diagram

The yellow blocks are all components found on the TIDA-00699 board. The front end supply does everything necessary to supply a clean, regulated, protected supply to the rest of the system, while also preventing noise and transients generated in the system from coupling back into the rest of the system. It essentially separates the system from the very dynamic (and sometimes dangerous) voltage levels coming from the battery supply lines in the vehicle.

3 Block Diagram

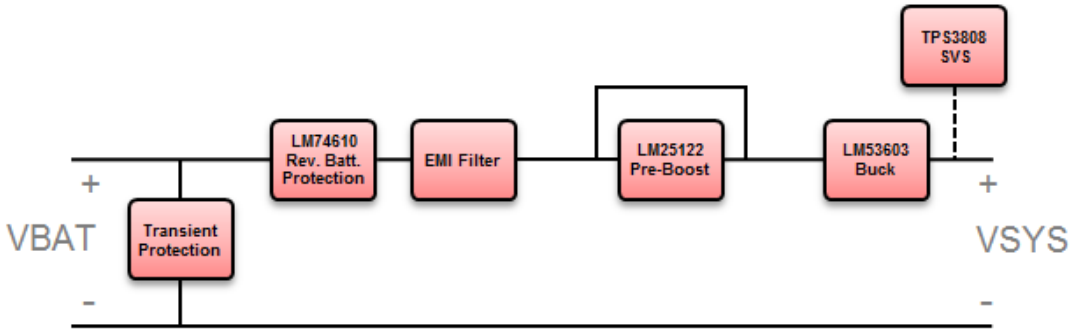


Figure 3: Off-battery front end

3.1 Highlighted Products

This design utilizes the following TI products:

- **LM53603-Q1** is a 2.1MHz synchronous buck converter with a wide input voltage range from 3.5V to 36V (42V transients) enabling it to work directly from an automotive battery.
- **LM25122-Q1** is a synchronous boost converter with a wide input voltage range (40V max, and Vin extending down to <3.0V in our topology)
- **LM74610-Q1** "Smart Diode" is a high-side NFET controller intended for reverse-battery protection.
- **TPS3808G01-Q1** is an adjustable voltage supervisory circuit which detects undervoltage conditions and reports it out on an open-drain RESET pin

More information on each device and why they were chosen for this application follow in the next sections.

3.1.1 LM53603-Q1

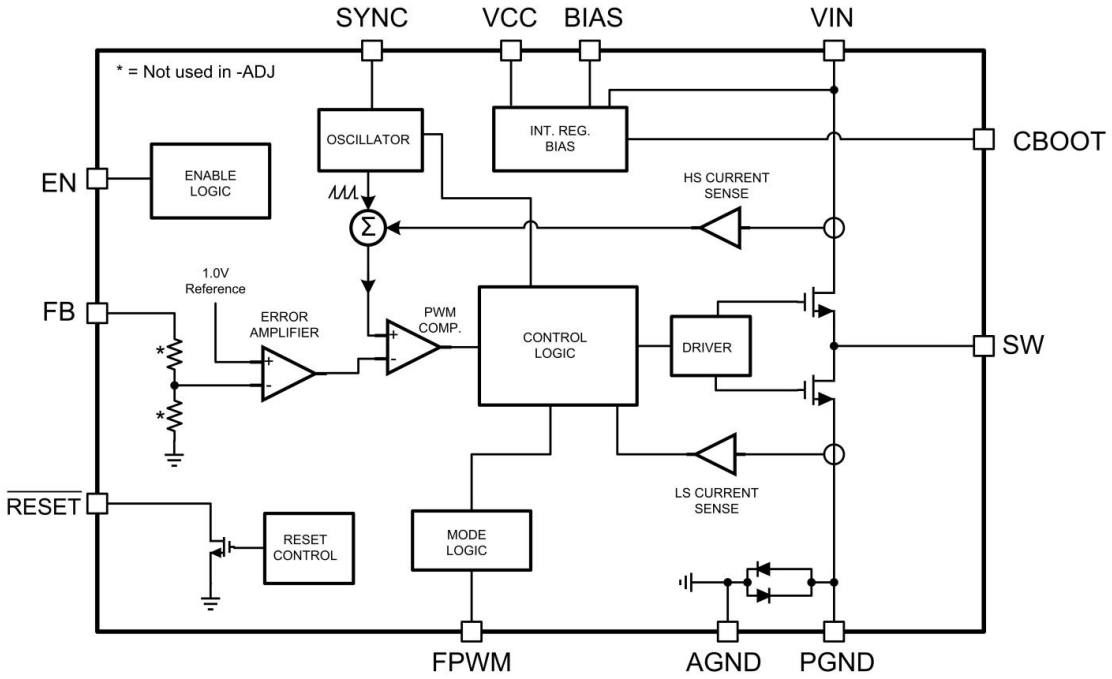


Figure 4: LM53603-Q1 3A Wide-Vin Synchronous Buck Converter

- The device has a 3A maximum output current. Our design operates at 5V which means we are capable of a maximum 15W output. With thermal de-rating in mind, between 10-15W is realistically achievable with this device.
- The device switches nominally at 2.1MHz during PWM mode. Automotive designs typically require DCDCs to switch outside of the AM radio band, and switching above it (rather than below) allows us to reduce the size of the external components.
- Forced PWM mode via an external pin is required to maintain our switching frequency through all load conditions. Devices without this feature will fall into discontinuous conduction or PFM mode at low load conditions, and the switching frequency will fall into the AM band. Though this sacrifices some efficiency, it helps with EMI compliance
- Integrated FETs with synchronous rectifier provides for a more efficient approach than asynchronous devices, and makes forced PWM mode possible
- External clock synchronization, though not used in this design, can be used to avoid beat frequencies between multiple converters, or to allow a master dither the clock signal. It can be an important feature for systems attempting to optimize EMI performance. On our design this is pinned out to an external header for evaluation of this feature
- The EN signal can be used to put the device into a shutdown mode by an external signal, essentially turning the system off and reducing power consumption to very low levels. On this design this is pinned out to an external header for evaluation of this feature
- Wide input voltage range (3.5-36V, 42V transients) is required to operate straight off of the battery

3.1.2 LM25122-Q1

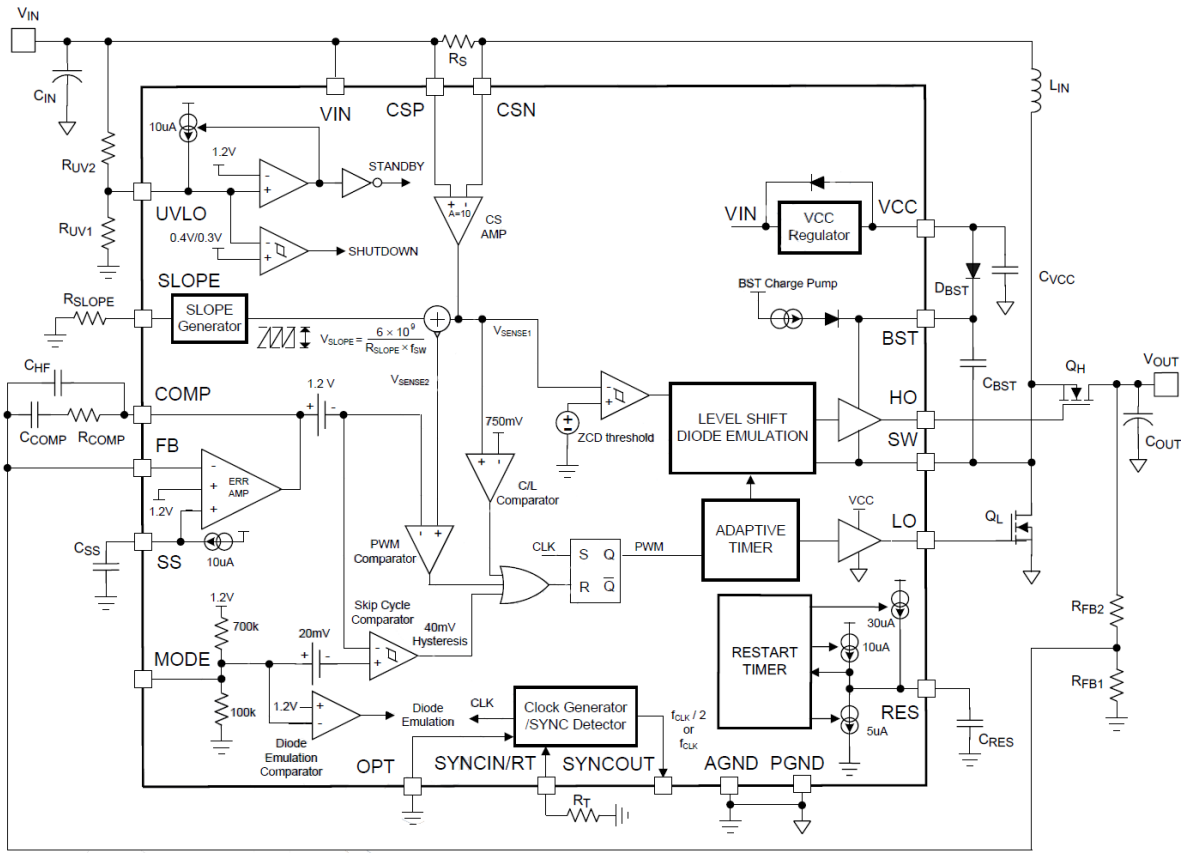


Figure 5: LM25122 Synchronous Boost Controller

- Synchronous solution allows for higher efficiency during boost operation. More importantly, during normal operation (Boost not switching), the high side FET is used as a bypass device (rather than a diode), significantly reducing power dissipation
- Wide input voltage range allows for use directly off of battery
- UVLO pin can be used as a shutdown when pulled low, putting the system into a low power consumption state. This feature is pinned out on a header on this design
- Using split-rail approach extends the input voltage range down to very low voltages (<3V possible). More on this topology later in this document.

3.1.3 LM74610-Q1

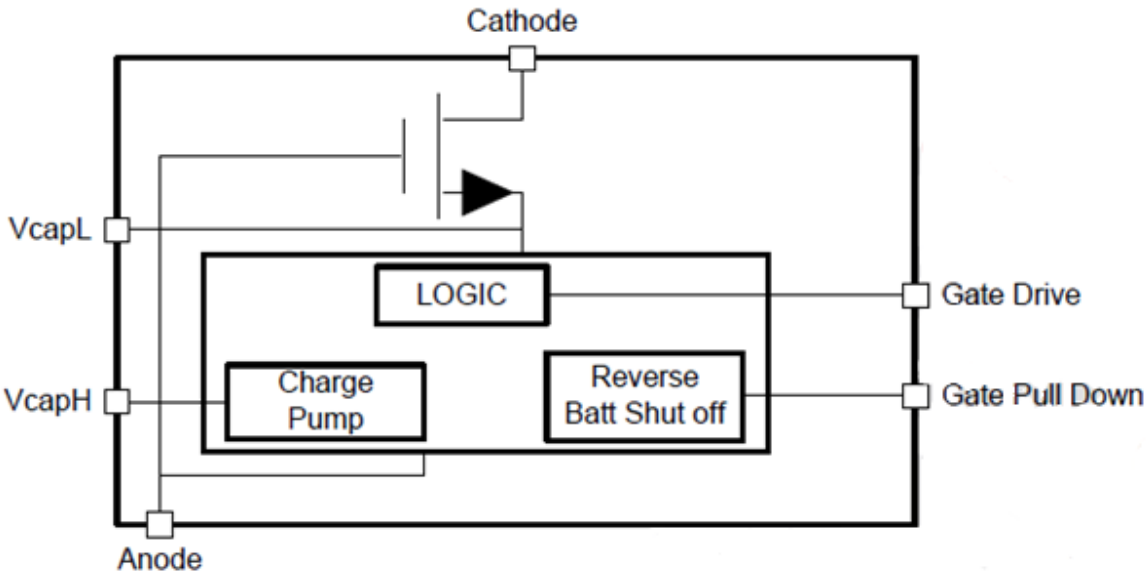


Figure 6: LM74610 Smart Diode for reverse battery protection

- Satisfies the requirement for reverse-battery protection on all electrical subsystems
- Controls an external NFET in series with the battery supply input to act as an ideal diode, reducing voltage drop and power loss as opposed to a discrete diode solution
- Quickly turns off FET when a reverse-battery condition is detected, isolating and protecting downstream circuitry
- Has no ground reference, leading to virtually zero I_Q operation. This helps the subsystem draw less standby current from the battery. Many OEMs have very small I_Q budgets.
- Because the voltage drop across the FET is negligibly small, this provides more input voltage headroom for the Wide Vin buck converter, allowing it to operate at even lower battery input voltages. For example, a cold-crank scenario could see the battery voltage temporarily drop to as low as 3.5V at the input of our system… with a diode solution, the buck converter would see 3.5V – 0.7V(typ) = 2.8V and would not be able to maintain the 3.3V system voltage. With the smart diode solution, the buck will still see close to 3.5V during this condition and can continue to operate.

3.1.4 TPS3808G01-Q1

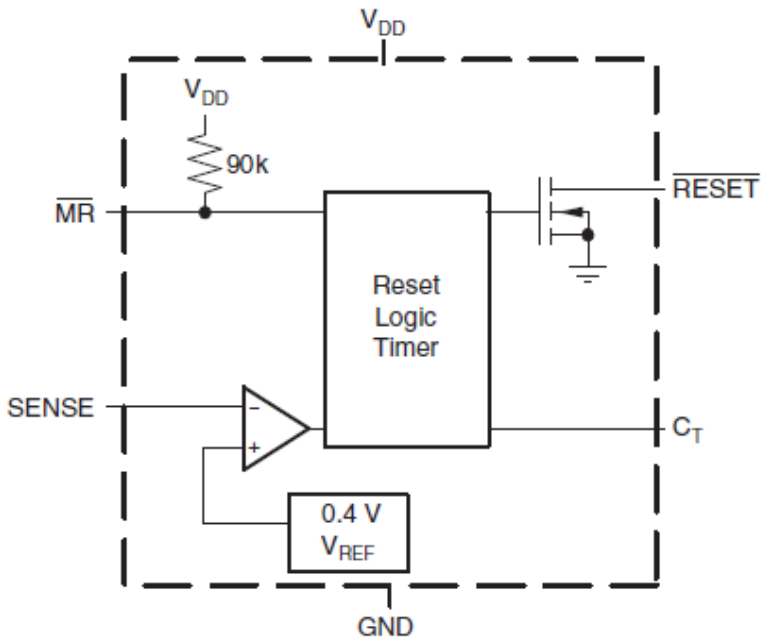


Figure 7: TPS3808G01-Q1 Supply Voltage Supervisor

- Adjustable voltage limit, with hysteresis, to define an under-voltage limit for any supply
- Used on our board for system output voltage (5V); VDD can be powered from this rail, but VDD has an operating range down to 1.8V so it will continue operation even if the system voltage starts to fall and lose regulation
- Open-drain /RESET output can signal a host controller or ECU of an out-of-regulation system voltage. On this design this is pinned out to a header for use by the designer

4 Automotive EMC/EMI Standards

One of the focuses of this design is on designing and testing for compliance with EMC/EMI standards that are important to automotive customers. There are many important standards/tests, but we've chosen to focus on the ones most applicable to front-end (off-battery) power supplies: ISO7637-2, ISO16750-2, and CISPR25.

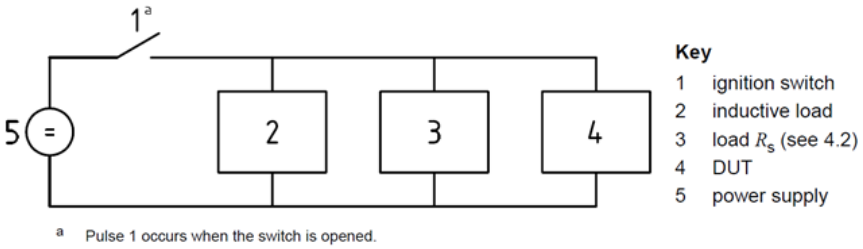
Any Tier 1 or OEM designer, however, will probably only be familiar with the version of these standards produced by OEMs themselves. Auto manufacturers have their own internal standards for EMC, but an important thing to note is that these are often based on the international ISO/IEC standards; changes are typically only in a few parameters of different tests or limits, but the essence of the requirements are the same.

4.1 ISO 7637-2

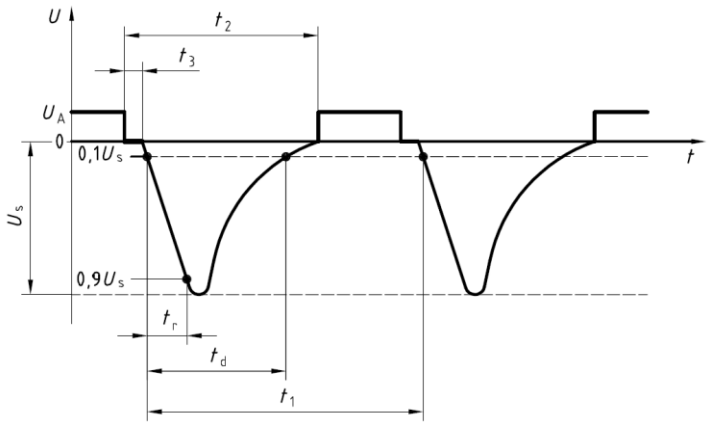
ISO 7637 is titled "Road vehicles – Electrical disturbances from conduction and coupling", and part 2 is specifically "Electrical transient conduction along supply lines only." As we are designing the portion of the power supply of a subsystem that directly comes from supply lines, this is very relevant. The standard defines a test procedure, including the description of test pulses, to test the susceptibility of an electrical subsystem to transients which could potentially be harmful to its operation. Each pulse is modeled to simulate a transient that could be created by a real event in the car. The following subsections go into the pulses that we test for in this design.

4.1.1 ISO 7637-2 Pulse 1

From the standard: "*This test is a simulation of transients due to supply disconnection from inductive loads. It is applicable to DUTs which, as used in the vehicle, remain connected directly in parallel with an inductive load.*" Here is a diagram of what such an applicable system would look like:



The pulse itself, simulating an inductive kick in a parallel system, is a high voltage, negative-going transient. The waveform and its parameters (12V system is applicable for us) are given below:



Parameter	12 V system	24 V system
U_s	–75 V to – 100 V	– 450 V to – 600 V
R_i	10 Ω	50 Ω
t_d	2 ms	1 ms
t_r	$\left(1^{\ 0}_{-0,5}\right)$ µs	$\left(3^{\ 0}_{-1,5}\right)$ µs
t_1 [a]	0,5 s to 5 s	
t_2	200 ms	
t_3 [b]	< 100 µs	

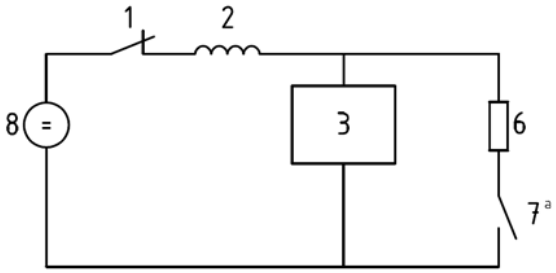
[a] t_1 shall be chosen such that the DUT is correctly initialized before the application of the next pulse.

[b] t_3 is the smallest possible time necessary between the disconnection of the supply source and the application of the pulse.

The specific parameters vary from standard to standard.

4.1.2 ISO 7636-2 Pulse 2a

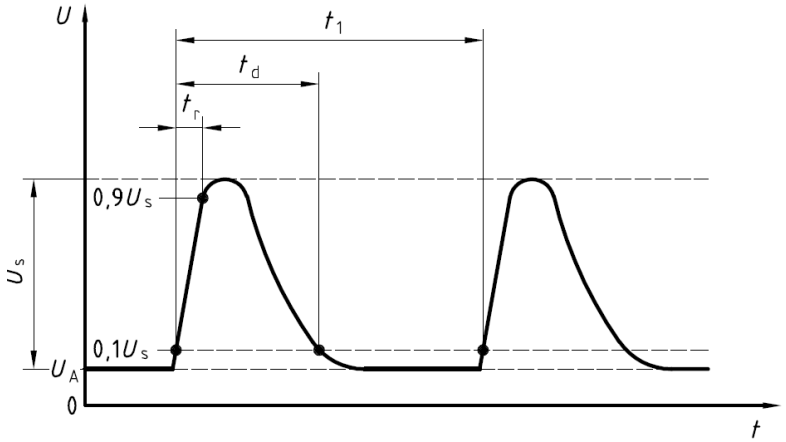
From the standard: "*Pulse 2a simulates transients due to sudden interruption of currents in a device connected in parallel with DUT due to inductance of the wiring harness.*" Here is a diagram of what such an applicable system would look like:



Key
1 ignition switch
2 wiring harness (inductive)
3 DUT
4 d.c. motor with internal inductance
5 motor switch
6 load
7 load switch
8 power supply

[a] Pulse 2a occurs when the load switch (7) is opened while the ignition switch (1) is closed.

The pulse itself, simulating an inductive kick from the wiring harness, is a high voltage, positive-going transient. The waveform and its parameters (12V system is applicable for us) are given below:



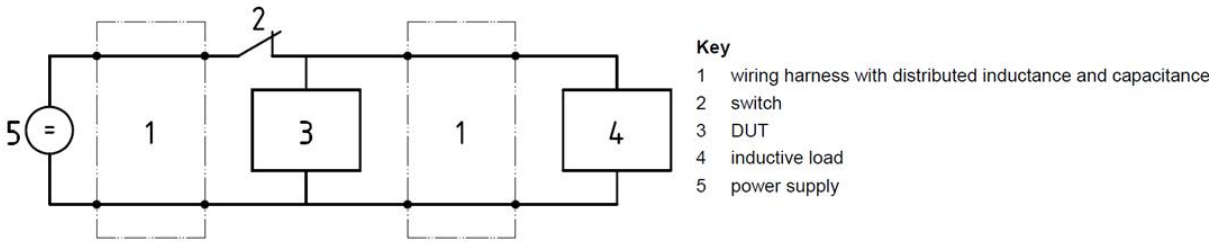
Parameter	12 V system	24 V system
U_s	+ 37 V to + 50 V	
R_i	2 Ω	
t_d	0,05 ms	
t_r	$\left(1^{\ 0}_{-0,5}\right)$ µs	
t_1 [a]	0,2 s to 5 s	

[a] The repetition time t_1 can be short, depending on the switching. The use of a short repetition time reduces the test time.

The specific parameters vary from standard to standard.

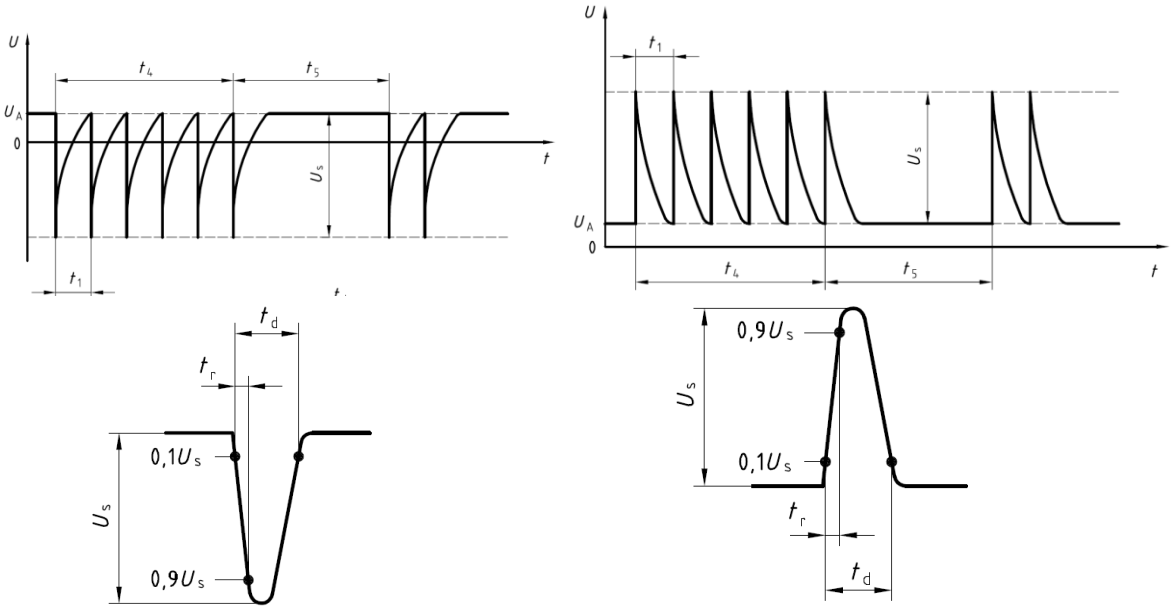
4.1.3 ISO 7637-2 Pulses 3a & 3b

From the standard: "*These test pulses are a simulation of transients which occur as a result of the switching processes. The characteristics of these transients are influenced by distributed capacitance and inductance of the wiring harness.*" Here is a diagram of what such an applicable system would look like:



Key
1 wiring harness with distributed inductance and capacitance
2 switch
3 DUT
4 inductive load
5 power supply

The description is a little vague (i.e. "as a result of the switching processes"), but it is essentially transients caused by the making and breaking of contact of a mechanical switch. The waveforms and their parameters (12V system is applicable for us) are given below:



Parameter	12 V system	24 V system
U_s	– 112 V to – 150 V	– 150 V to – 200 V
R_i	50 Ω	
t_d	$\left(0,1^{+0,1}_{0}\right)$ µs	
t_r	5 ns ± 1,5 ns	
t_1	100 µs	
t_4	10 ms	
t_5	90 ms	

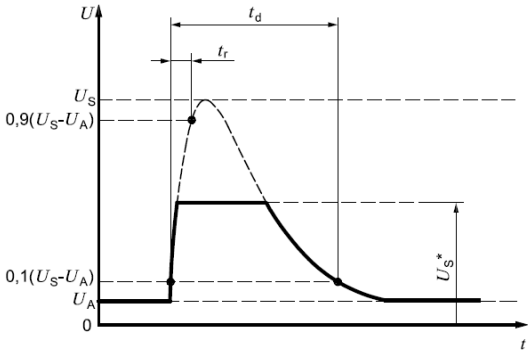
Parameter	12 V system	24 V system
U_s	+ 75 V to + 100 V	+ 150 V to + 200 V
R_i	50 Ω	
t_d	$\left(0,1^{+0,1}_{0}\right)$ µs	
t_r	5 ns ± 1,5 ns	
t_1	100 µs	
t_4	10 ms	
t_5	90 ms	

The specific parameters vary from standard to standard.

4.1.4 ISO 7637-2 Pulse 5b (Clamped Load Dump)

From the standard: "*This test is a simulation of load dump transient, occurring in the event of a discharged battery being disconnected while the alternator is generating charging current and with other loads remaining on the alternator circuit at this moment. […] Load dump may occur on account of a battery being disconnected as a result of cable corrosion, poor connection or of intentional disconnection with the engine running.*" It is worth noting here that this pulse was actually moved from ISO 7637 to ISO 16750 (covered in the next section), but for historical reasons it is still often grouped with the ISO 7637-2 pulses, so we discuss it here.

The actual load dump event is extremely high energy and high voltage, which would be very difficult (and expensive) to protect against on every subsystem in the vehicle. Instead, every OEM installs a clamping circuit to the alternator, which limits the voltage to a more manageable level for the subsystem. This clamped voltage varies from OEM to OEM but is typically in the range of 30-38V.



Parameter	Type
	U_N = 12 V
U_S [a] V	$79 \leqslant U_S \leqslant 101$
U_S^* V	35
R_i [a] Ω	$0,5 \leqslant R_i \leqslant 4$
t_d ms	$40 \leqslant t_d \leqslant 400$
t_r ms	$10\left(^{0}_{-5}\right)$

Key

t	time
U	test voltage
t_d	duration of pulse
t_r	rising slope
U_A	supply voltage for generator in operation (see ISO 16750-1)
U_S	supply voltage
U_S^*	supply voltage with load dump surpression

4.1.5 Related Standards

As stated previously, OEMs (and other standards organizations) maintain their own versions of these pulses in their own standards; typically the pulses simply have slightly different parameters depending on the OEM, but often they are exactly the same. Below is an example comparison of the ISO 7637-2 defined pulses with various OEM's definitions:

	Vmax (V)	Rsource (Ω)	Tr	Tduration
ISO 7637-2: Pulse 1	-100	10	1us	2ms
OEM#1	-100	10	1us	2ms
OEM#2	-100	10	1us	2ms
OEM#3	-100	10	1us	2ms
OEM#4	-100	4	1us	2ms
ISO 7637-2: Pulse 2a	50	2	1us	50us
OEM#1	75	4	1us	50us
OEM#2	100	10	1us	50us
OEM#3	50	2	1us	50us
OEM#4	75	4	1us	50us
ISO 7637-2: Pulse 3a	-150	50	5ns	0.1us
OEM#1	-150	50	5ns	0.1us
OEM#2	-150	50	5ns	0.1-0.2us
OEM#3	-150	50	5ns	0.1us
OEM#4	-150	50	5ns	0.1us
ISO 7637-2: Pulse 3b	100	50	5ns	0.1us
OEM#1	100	50	5ns	0.1us
OEM#2	100	50	5ns	0.1-0.2us
OEM#3	100	50	5ns	0.1us
OEM#4	100	50	5ns	0.1us

As you can see, there are only small variations in most pulses. Pulse 2a has some significant differences but overall energy content of the pulses is actually very similar. For our testing, we actually used OEM#4's parameters, as they represent the worst case on most pulses.

4.2 ISO 16750-2

ISO 16750 is titled "Road vehicles – Environmental conditions and testing for electrical and electronic equipment", and part 2 is specifically "Electrical loads." An easy way to think of this standard is that it essentially defines a series of "supply voltage quality" events – variations of the battery supply voltage under various conditions. These conditions, for the most part, are not harmful to the electrical subsystem, but can affect its state of operation. The tests in this standard are designed to see how the subsystem behaves before, during, and after these events. The required behavior can be classified into multiple "Functional Classes":

- **Functional Class A**

  All functions of the device/system perform as designed during and after the test

- **Functional Class B**

  All functions of the device/system perform as designed during the test. However, one or more may go beyond the specified tolerance. All functions return automatically to within normal limits after the test. Memory functions shall remain Class A.

- **Functional Class C**

One or more functions of a device/system do not perform as designed during the test but return automatically to normal operation after the test.

- **Functional Class D**

One or more functions of a device/system do not perform as designed during the test and do not return to normal operation after the test until the device/system is reset by simple "operator/use" action.

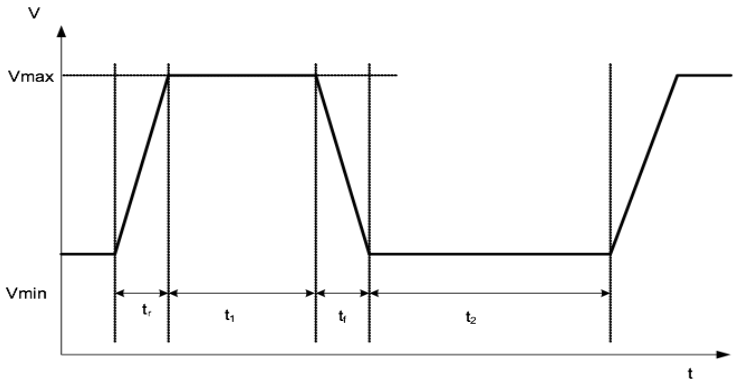
- **Functional Class E**

One or more functions of a device/system do not perform as designed during and after the test and cannot be returned to proper operation without repairing or replacing the device/system.

The standard actually defines *many* different tests, but only a small subset of them is really applicable to this design. I describe several below, though only the Cold Crank test results are given later in this document.

4.2.1 ISO 16750-2: 4.3.1.2 Jump Start

This test simulates the supply seen by the subsystem during the so-called "jump start" where two 12V batteries are connected to the supply lines in series. This is an overvoltage condition which is sustained for a period of time:



t_r < 10ms

t_f < 10ms

t_1 = 60 seconds

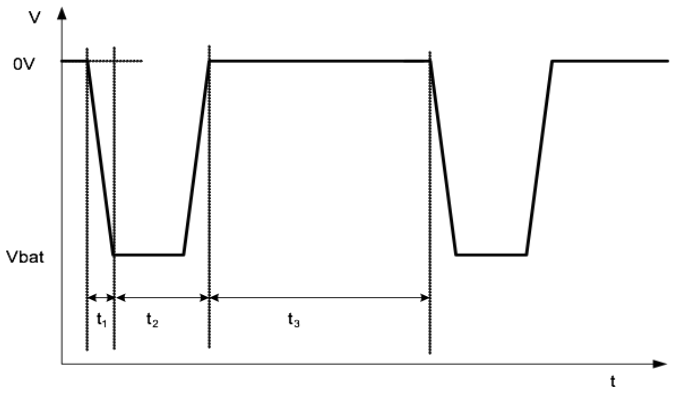
V_{max} = 26 V

V_{min} = 10.8 V

Functional class C is the requirement for this test.

4.2.2 ISO 16750-2: 4.7 Reversed Voltage

From the standard: "*This test checks the ability of a DUT to withstand against the connection of a reversed battery in case of using an auxiliary starting device.*"



$t_1 \leq 10ms$ (rise and fall times)

$t_2 = 60$ seconds

$V_{bat} = -14$ V

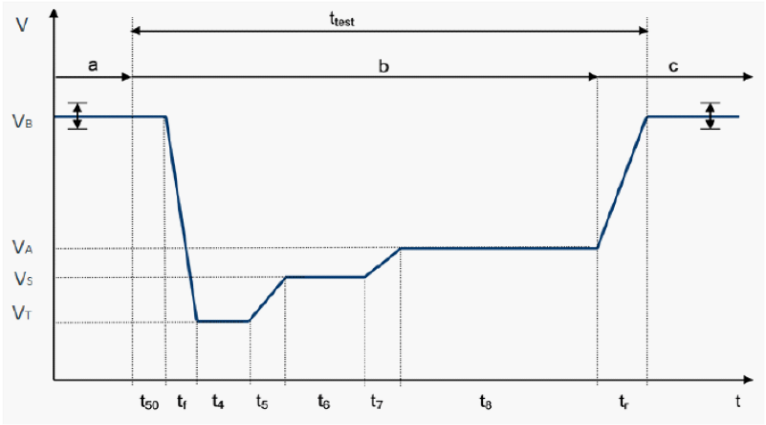
The subsystem does not need to operate during this event, but upon removing the reverse-polarity and re-establishing the normal supply voltage (12V), the subsystem to satisfy Functional Class A.

4.2.3 Cranking profiles

Cranking tests simulate the droop in supply voltage when the engine is started due to the large current draw of the starter motor. The voltage levels are very dependent on the temperature of the car during start-up, with severe cold leading to the largest drop in voltage ("Cold Crank").

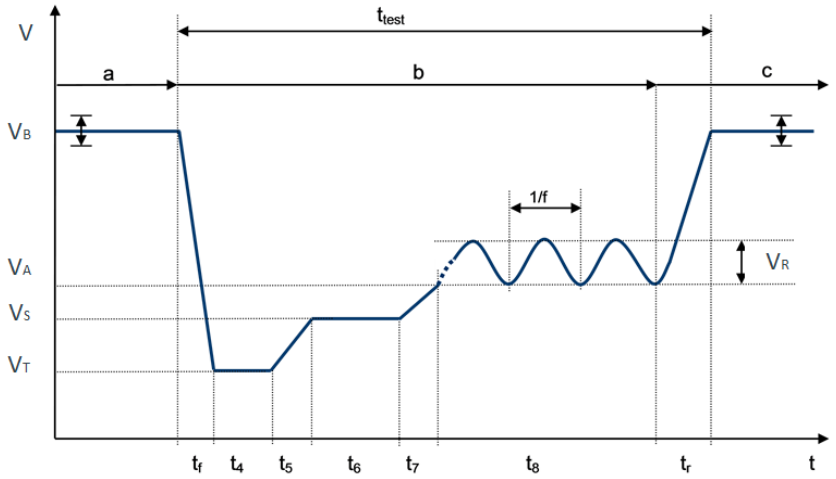
Though the profile itself looks similar for all OEMs, the voltage levels can vary from standard to standard. For this reason, we choose to use the conditions defined by one OEM who has the most severe requirements. We will test both the "Hot Start" (least severe) condition and "Cold Start" (most severe condition.

Warm Start



Parameters	"Short" test sequence	"Long" test sequence
V_B	11,0 V	
V_T	7,0 V (0%, -4%)	
V_S	8,0 V (0%, -4%)	
V_A	9,0 V (0%, -4%)	
t_{50}	≥10 ms	
t_f	≤1 ms	
t_4	15 ms	
t_5	70 ms	
t_6	240 ms	
t_7	70 ms	
t_8	600 ms	
t_r	≤1 ms	
Break between two cycles	5 s	20 s

Cold Start



Parameter	"Normal" test pulse	"Severe" test pulse
V_B	11,0 V	11,0 V
V_T	4,5 V (0%, -4%)	3,2 V $^{+0,2\,V}$
V_S	4,5 V (0%, -4%)	5,0 V (0%, -4%)
V_A	6,5 V (0%, -4%)	6,0 V (0%, -4%)
V_R	2 V	2 V
t_f	≤1 ms	≤1 ms
t_4	0 ms	19 ms
t_5	0 ms	≤1 ms
t_6	19 ms	329 ms
t_7	50 ms	50 ms
t_8	10 s	10 s
t_r	100 ms	100 ms
f	2 Hz	2 Hz

4.3 CISPR 25

CISPR 25 is the automotive EMI standard that most OEMs base their own requirements on. The title is: "*Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers*." Basically, the purpose of the standard is to limit the amount of emissions from a subsystem in a few important frequency bands, to ensure it doesn't interfere with other systems that **intentionally** operate (i.e. receive) in those bands.

For example, an AM radio receiver is "listening" (tuned) to a specific frequency (say 710 kHz), picking up a radio station's signal put out on that frequency. It only wants to receive and amplify the signals intended for AM Radio broadcast on that frequency. However, if another system on the car is unintentionally emitting a lot of energy (noise) at that frequency, it impedes the radios ability to resolve the radio station's signal cleanly, and the user may hear a lot of noise in the signal, or obscure the intentional signal altogether. Standards like CISPR25 are specifically designed to avoid this by setting acceptable limits on these systems. OEMs will define their own limits but CISPR25 provides examples.

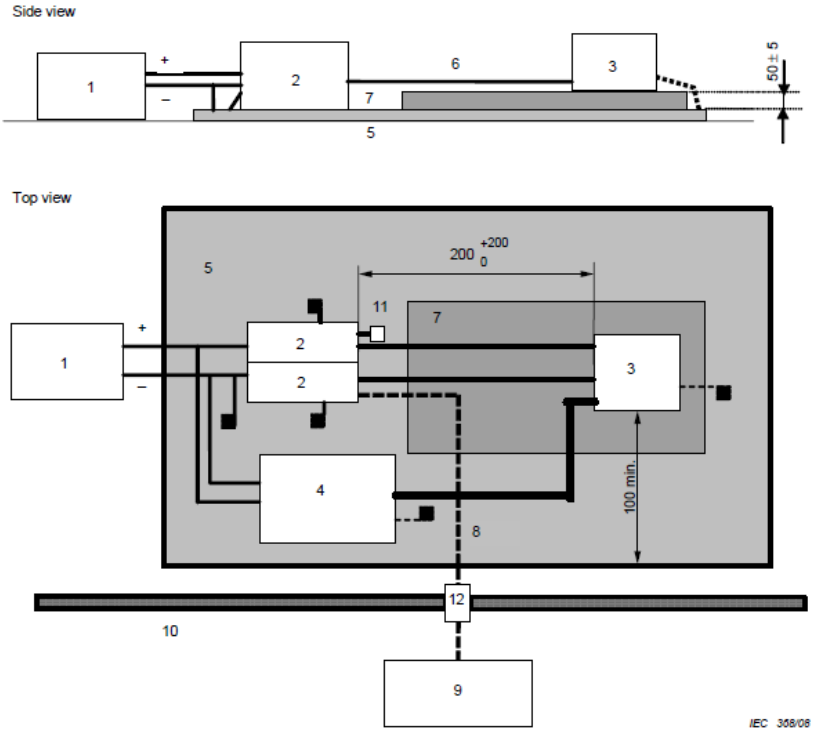
The testing and limits are split into two separate types of emissions: Conducted and Radiated. Conducted emissions are coupled onto supply lines directly through conductors (traces, wires, etc.), and radiated emissions are emitted as EM waves and can be picked up by intentional/unintentional antennas on other systems.

The test procedures, relevant frequency bands, and limits are different for both, but the basics are similar: the subsystem (or 'DUT') is placed in an isolated room/chamber, and setup in a well-defined, reproducible electrical setup. All other possible emitters are removed from the chamber, and the DUT is turned on and allowed to operate normally. The DUT is powered through an Artificial Network (or LISN) and loaded per its normal operation. A spectrum analyzer is then used to measure its emissions across different frequencies (either through the LISN or from an Antenna) and compared against the CISPR 25 limits. Both the peak and average values of the emissions are measured, and both must pass.

Finally, the level of "passing" falls into several categories, or "classes", which have different limits. OEMs define which class a specific subsystem must satisfy.

4.3.1 Conducted Emissions

The test setup is outlined in the official CISPR 25 documentation:



1 Power supply (may be placed on the ground plane)
2 Artificial network
3 EUT (housing grounded if required in test plan)
4 Load simulator (metallic casing grounded if required in test plan)
5 Ground plane
6 Power supply lines
7 Low relative permittivity support ($\varepsilon_r \leq 1{,}4$)
8 High-quality coaxial cable e.g. double-shielded (50 Ω)
9 Measuring instrument
10 Shielded enclosure
11 50 Ω load
12 Bulkhead connector

There are actually variations on this setup depending on the subsystem being tested, but for our testing purposes, we will use the above setup. Please see the official documentation for further information about the test setup.

Conducted emissions testing is only done in the lower frequency bands for the standard. The limits are defined in the CISPR 25 documentation:

Peak Limits

Service / Band	Frequency MHz	Levels in dB(µV)									
		Class 1		Class 2		Class 3		Class 4		Class 5	
		Peak	Quasi-peak	Peak	Quasi-peak	Peak	Quasi-peak	Peak	Quasi-peak	Peak	Quasi-peak
BROADCAST											
LW	0,15 - 0,30	110	97	100	87	90	77	80	67	70	57
MW	0,53 - 1,8	86	73	78	65	70	57	62	49	54	41
SW	5,9 - 6,2	77	64	71	58	65	52	59	46	53	40
FM	76 - 108	62	49	56	43	50	37	44	31	38	25
TV Band I	41 - 88	58	-	52	-	46	-	40	-	34	-
TV Band III	174 - 230	Conducted emission – Voltage method Not applicable									
DAB III	171 - 245										
TV Band IV/V	468 - 944										
DTTV	470 - 770										
DAB L band	1447 - 1494										
SDARS	2320 - 2345										
MOBILE SERVICES											
CB	26 - 28	68	55	62	49	56	43	50	37	44	31
VHF	30 - 54	68	55	62	49	56	43	50	37	44	31
VHF	68 - 87	62	49	56	43	50	37	44	31	38	25

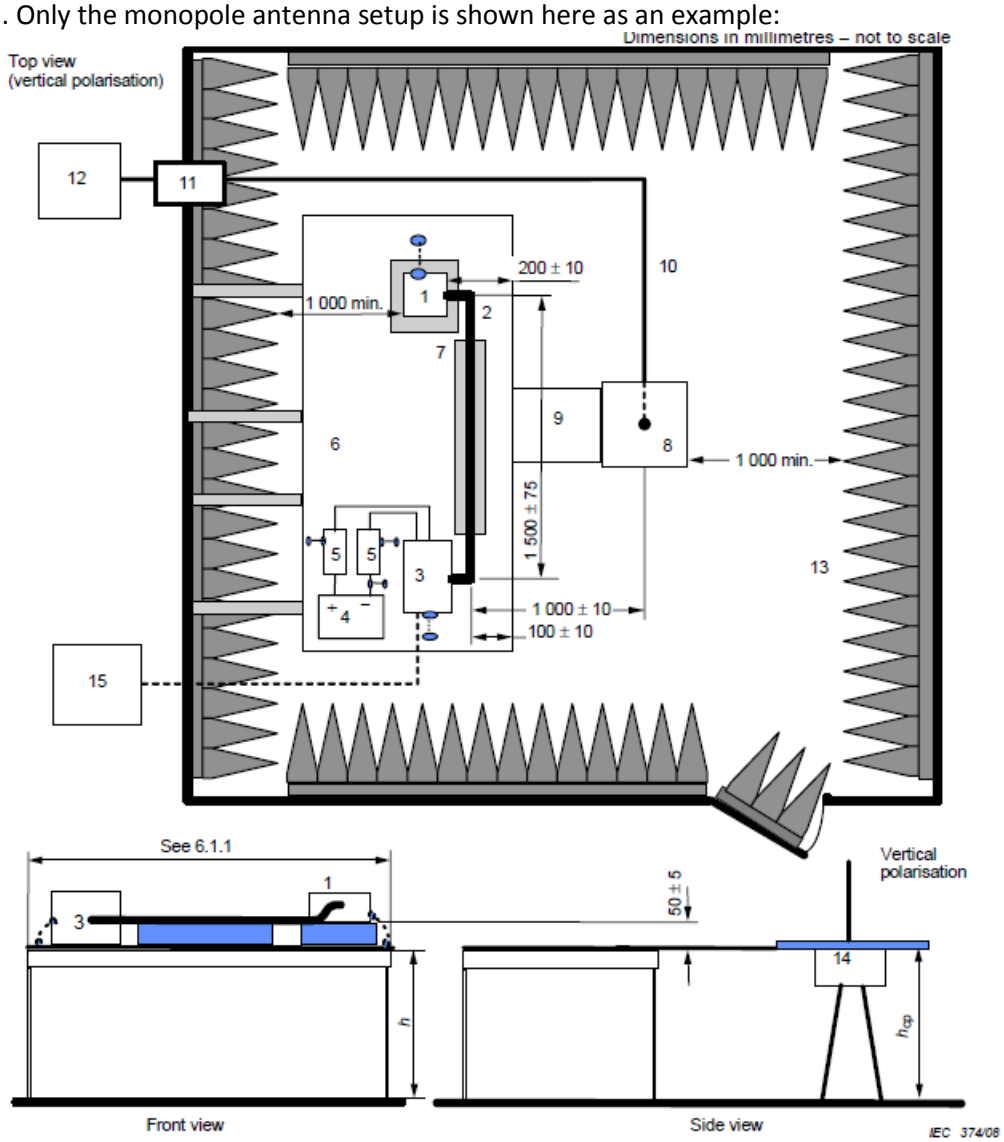
Average Limits

Service / Band	Frequency MHz	Levels in dB(µV)				
		Class 1	Class 2	Class 3	Class 4	Class 5
		AVG	AVG	AVG	AVG	AVG
BROADCAST						
LW	0,15 - 0,30	90	80	70	60	50
MW	0,53 - 1,8	66	58	50	42	34
SW	5,9 - 6,2	57	51	45	39	33
FM	76 - 108	42	36	30	24	18
TV Band I	41 - 88	48	42	36	30	24
TV Band III	174 - 230	Conducted emission – Voltage method Not applicable				
DAB III	171 - 245					
TV Band IV/V	468 - 944					
DTTV	470 - 770					
DAB L band	1447 - 1494					
SDARS	2320 - 2345					
MOBILE SERVICES						
CB	26 - 28	48	42	36	30	24
VHF	30 - 54	48	42	36	30	24
VHF	68 - 87	42	36	30	24	18

In our case, the DCDC regulators in the system will be the main sources of conducted emissions. The switching action of the input current waveforms will emit energy back onto the supply lines, and this must be filtered. They will emit at their fundamental switching frequency and harmonics.

4.3.2 Radiated Emissions

The test setup is outlined in the official CISPR 25 documentation. Three different antennas are used to measure over the full frequency range of the testing, and three slightly different test setups are required. Only the monopole antenna setup is shown here as an example:



1 EUT (grounded locally if required in test plan)
2 Test harness
3 Load simulator (placement and ground connection according to 6.4.2.5)
4 Power supply (location optional)
5 Artificial network (AN)
6 Ground plane (bonded to shielded enclosure)
7 Low relative permittivity support ($\varepsilon_r \leq 1,4$)
8 Rod antenna with counterpoise (dimensions: 600 mm by 600 mm typical)
h = (900 ± 100) mm
$h_{cp} = h + (+10 / -20)$ mm
9 Grounding connection (full width bond between counterpoise and ground plane)
10 High-quality coaxial cable e.g. double-shielded (50 Ω)
11 Bulkhead connector
12 Measuring instrument
13 RF absorber material
14 Antenna matching unit (the preferred location is below the counterpoise; if above the counterpoise then the base of the antenna rod shall be at the height of the ground plane)
15 Stimulation and monitoring system

Please see the official documentation for further information about the other test setups.

The limits are defined in the CISPR 25 documentation, and cover a much wider band than the conducted emissions test:

Peak Limits

Service / Band	Frequency MHz	Levels in dB(µV/m)									
		Class 1		Class 2		Class 3		Class 4		Class 5	
		Peak	Quasi-peak	Peak	Quasi-peak	Peak	Quasi-peak	Peak	Quasi-peak	Peak	Quasi-peak
BROADCAST											
LW	0,15 - 0,30	86	73	76	63	66	53	56	43	46	33
MW	0,53 - 1,8	72	59	64	51	56	43	48	35	40	27
SW	5,9 - 6,2	64	51	58	45	52	39	46	33	40	27
FM	76 - 108	62	49	56	43	50	37	44	31	38	25
TV Band I	41 - 88	52	-	46	-	40	-	34	-	28	-
TV Band III	174 - 230	56	-	50	-	44	-	38	-	32	-
DAB III	171 - 245	50	-	44	-	38	-	32	-	26	-
TV Band IV/	468 - 944	65	-	59	-	53	-	47	-	41	-
DTTV	470 - 770	69	-	63	-	57	-	51	-	45	-
DAB L band	1447 - 1494	52	-	46	-	40	-	34	-	28	-
SDARS	2320 - 2345	58	-	52	-	46	-	40	-	34	-
MOBILE SERVICES											
CB	26 - 28	64	51	58	45	52	39	46	33	40	27
VHF	30 - 54	64	51	58	45	52	39	46	33	40	27
VHF	68 - 87	59	46	53	40	47	34	41	28	35	22
VHF	142 -175	59	46	53	40	47	34	41	28	35	22
Analogue UHF	380 - 512	62	49	56	43	50	37	44	31	38	25
RKE	300 - 330	56	-	50	-	44	-	38	-	32	-
RKE	420 - 450	56	-	50	-	44	-	38	-	32	-
Analogue UHF	820 - 960	68	55	62	49	56	43	50	37	44	31
GSM 800	860 - 895	68	-	62	-	56	-	50	-	44	-
EGSM/GSM 900	925 - 960	68	-	62	-	56	-	50	-	44	-
GPS L1 civil	1567 - 1583	-	-	-	-	-	-	-	-	-	-
GSM 1800 (PCN)	1803 - 1882	68	-	62	-	56	-	50	-	44	-
GSM 1900	1850 - 1990	68	-	62	-	56	-	50	-	44	-
3G / IMT 2000	1900 - 1992	68	-	62	-	56	-	50	-	44	-
3G / IMT 2000	2010 - 2025	68	-	62	-	56	-	50	-	44	-
3G / IMT 2000	2108 - 2172	68	-	62	-	56	-	50	-	44	-
Bluetooth/802.11	2400 - 2500	68	-	62	-	56	-	50	-	44	-

Average Limits

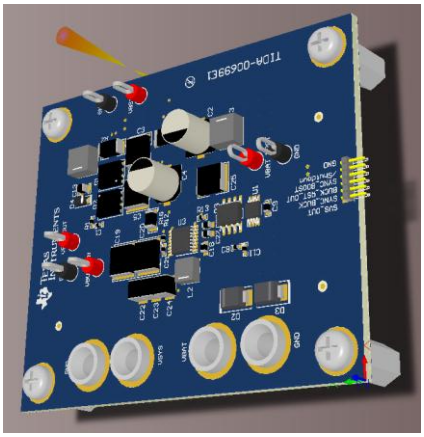
Service / Band	Frequency MHz	Levels in dB(µV/m)				
		Class 1	Class 2	Class 3	Class 4	Class 5
		AVG	AVG	AVG	AVG	AVG
BROADCAST						
LW	0,15 - 0,30	66	56	46	36	26
MW	0,53 - 1,8	52	44	36	28	20
SW	5,9 - 6,2	44	38	32	26	20
FM	76 - 108	42	36	30	24	18
TV Band I	41 - 88	42	36	30	24	18
TV Band III	174 - 230	46	40	34	28	22
DAB III	171 - 245	40	34	28	22	16
TV Band IV/V	468 - 944	55	49	43	37	31
DTTV	470 - 770	59	53	47	41	35
DAB L band	1447 - 1494	42	36	30	24	18
SDARS	2320 - 2345	48	42	36	30	24
MOBILE SERVICES						
CB	26 - 28	44	38	32	26	20
VHF	30 - 54	44	38	32	26	20
VHF	68 - 87	39	33	27	21	15
VHF	142 -175	39	33	27	21	15
Analogue UHF	380 - 512	42	36	30	24	18
RKE	300 - 330	42	36	30	24	18
RKE	420 - 450	42	36	30	24	18
Analogue UHF	820 - 960	48	42	36	30	24
GSM 800	860 - 895	48	42	36	30	24
EGSM/GSM 900	925 - 960	48	42	36	30	24
GPS L1 civil	1567 - 1583	34	28	22	16	10
GSM 1800 (PCN)	1803 - 1882	48	42	36	30	24
GSM 1900	1850 - 1990	48	42	36	30	24
3G / IMT 2000	1900 - 1992	48	42	36	30	24
3G / IMT 2000	2010 - 2025	48	42	36	30	24
3G / IMT 2000	2108 - 2172	48	42	36	30	24
Bluetooth/802.11	2400 - 2500	48	42	36	30	24

5 System Design and Component Selection

Below we will discuss the considerations behind the design of each subsection of the system.

5.1 PCB / Form Factor

This design was not intended to fit any particular form-factor. The only goal of the design with regards to the PCB was to make as compact a solution as possible while still providing a reasonable way to test the performance of the board. Below is a 3D render of the board showing the dimensions:



In a final, production quality version of this design, there are several techniques that could be used to reduce the size of the solution:

- Test points, headers, standoffs, and banana plugs can be removed in final version
- Zero ohm resistors are currently used to isolate each supply for testing of each individual block. These can be removed as they service no direct function for the board
- Optimization can be done with regards to the number, size, and value of capacitors in the system

5.2 Input Protection

5.2.1 Reverse Battery Protection

Reverse Battery protection is required in every electronic subsystem of a vehicle, both by OEM standards, as well as ISO 16750-2, an international standard pertaining to supply quality. The goal is to provide a way to prevent reverse-biasing components which are sensitive to polarity, like polarized capacitors and most integrated circuits.

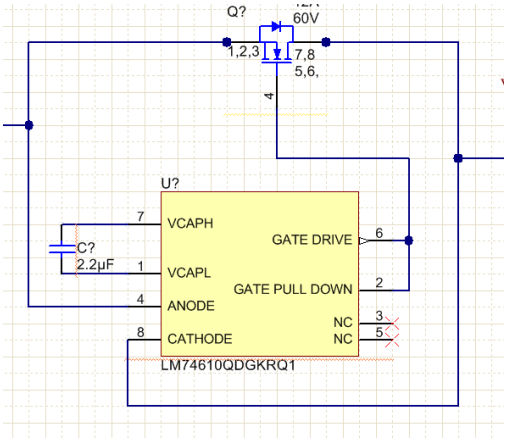


Figure 8: Reverse battery input protection

Rather than use the traditional diode rectifier solution for reverse battery protection, our implementation uses an N-channel MOSFET driven by the LM74610-Q1 Smart Diode Controller. The diode solution's power dissipation can be significant due to the typically 600-700mV forward drop (P = I*V), whereas using our solution only results in the loss due to the $R_{DS(ON)}$ of the FET, which can be significantly lower, resulting in greater efficiency and less thermal dissipation required.

The LM74610 team provides recommendations, as well as a tool, which can be used to help select a FET for your application. Here are the important considerations:

- Ensure that the continuous current rating is sufficient for your application
- The V_{GS} threshold should be 2.5V maximum
- V_{SD} should be at least 0.48V @ 2A and 125°C

For this design, the FET needs to be rated at least as high as our clamped input voltage; a 40V FET would be acceptable, but we chose to use a 60V for additional headroom.

5.2.2 TVS Diodes

TVS diodes are required on the supply input of the system to protection against both positive and negative going transients. The transients we are concerned with are detailed in ISO 7637-2:2004, pulses 1 and 2a. Pulses 3a/b are also important and are filtered both by the TVS diodes, as well as the LC pi filter downstream. Many systems in a car can simply shut down during these transients until the condition passes, but many applications are required to continue operation through them. OEM specifications will define a "class of operation" for each test which defines the required operational status during/after the event; in this design we aim for the highest class of operation, which means maintaining the same level of operation during each event as if it weren't present. For this reason, we must shunt the transients instead of using an over-voltage shutdown scheme.

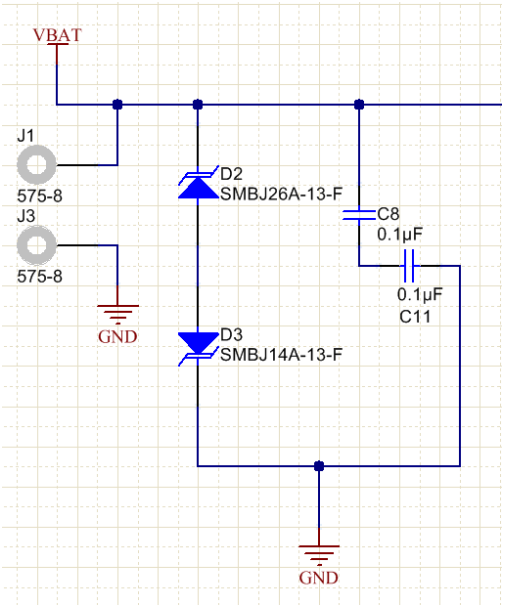


Figure 9: Input transient protection

The diode breakdown voltages should be chosen such that transients are clamped at voltages which will protect the MOSFET/rest of the system. The positive clamping device should clamp above double-battery (jump-start) and clamped Load Dump voltages, but lower than the maximum operating voltage of the downstream devices. In our case this means starting to clamp around 28V but having a maximum clamping voltage below 40V. Ideally, somewhere around 36V (maximum clamping voltage) would be the best choice.

The reverse clamping device should clamp all negative voltages greater than the battery voltage so that it does not short out during a reverse-battery condition.

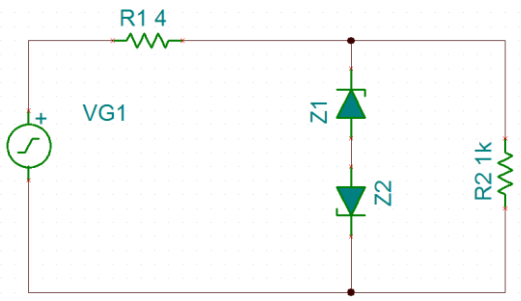
The other parameter to choose for the TVS diodes is the Peak Power rating. This is important to us because it is proportional to the package size of the diodes. We need to measure the amount of peak power that the diode could see to size it properly. The important features are its clamping voltage, the voltage of the pulse it is clamping, and the source impedance of the pulse. The rise time and duration of the pulse also play a role, but we will ignore that for now. Below we give the example of calculating it for Pulse 2a from OEM#4 in the chart given earlier in this document, which ends up being the worst case:

$-V_{Pulse} = 75V$

$-R_{Source} = 4\Omega$

$-V_{Clamp} = 33V$ (this was found empirically for this pulse, as TVS diodes do not clamp precisely)

A simple model of the circuit is seen below. The worst case assumption is that the load (R2 in this case) is drawing very little current, so the majority will go through the TVS diodes. We will also ignore the drop across the second TVS diode for simplicity.



If V_{Zener} = 33V, and VG1 (pulse generator) generates a 75V pulse, this implies that there is a 42V drop across R1 (the source impedance of the pulse as defined in the OEM spec). 42V / 4Ω = 13A coming out of the pulse generator. We assume that most of this passes through the Zener diode, and so we can estimate the peak power seen by the device as P = I*V = 33V * 13A = 429W. Providing plenty of margin, the next highest rated TVS diodes are SMB sized, 600W peak power rated diodes. These were chosen for this design and have been verified on the bench on previous designs.

5.2.3 Input Capacitors exposed to battery inputs

A final consideration for the front-end protection is the input capacitor. Due to flexion of the PCB or other means, it is possible for a ceramic capacitor to mechanically fail short; if this happens to an input capacitor connected directly to the battery, this could cause a hard short at the battery terminals.

To avoid this, typically two ceramic capacitors are used in series – if one fails, there is still another to avoid a short. The capacitors should also be aligned at 90° with respect to each other on the layout – this gives a good chance that a flexion in one direction may only affect the capacitor aligned in that direction, but not the one in the other. Recently, component manufacturers have designed capacitors specifically for this application which affectively includes the two caps described above into a single SMD package.

5.3 Voltage Supervision

- Connect VDD to VSYS – the part can be supplied down to 1.7V, so even in the event of an under-voltage condition, the supervisor will remain operational after the supply has lost regulation.
  - .1uF decoupling cap connected to filter any transients from resetting the supervisor
- Connect 0.1uF cap to CT, the delay capacitor, but DNP it
  - A constant current source charges this cap to act as a timer for the programmable delay. After an under-voltage condition is detected, the RST out will be pulled low by the device. It will remain low until after the supply has recovered. After recovery, it will wait a length of time equal to this programmable delay before de-asserting the RST out pin.
  - We don't have a spec we need to meet for this, so 0.1uF was chosen just to leave a pad in case one is desired. We will DNP (do not populate) this part so the CT pin will remain floating. This will give a 20ms delay time by default.
- MR manual reset out is a no-connect, we have no use for it here

- RST out is the UV error flag to the outside system. A pullup is required to an appropriate supply voltage as this pin is an open-drain output

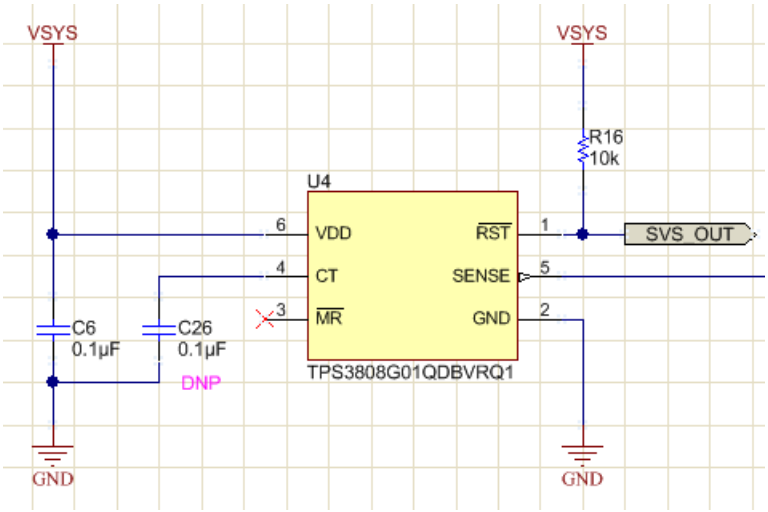


Figure 10: Supervisor circuit

- Setting the trip point
  - Threshold voltage reference on SENSE pin is 0.405V, so we use a resistor divider to detect an adjustable UV threshold
  - Choose 4.5V as our threshold
  - Choose R_{Bottom} = 10k, calculate R_{Top} → 101.1k, use closest standard value → 102k
  - Use 1% resistors if a precise threshold is required

5.4 Boost Converter

A boost converter (or "pre-boost") is sometimes included in an off-battery power supply to extend the operating range of the subsystem down to low values (down to 3V in some cases). This allows the subsystem to continue operation through such conditions as cold crank.

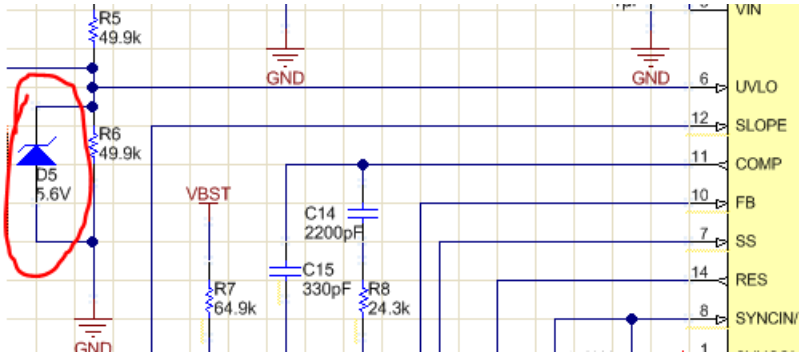
The boost will only operate when the input voltage drops below a pre-determined level, and helps sustain a high input voltage for the buck converter to maintain regulation of the system voltage. When the system voltage is adequately high (for us, >9V), the boost simply acts in "bypass mode", allowing the input voltage to the system to pass directly through to the buck.

A big consideration when choosing a boost converter is whether to choose a synchronous or asynchronous architecture. A synchronous solution is more efficient, especially during normal operation when the boost is in bypass mode. During bypass mode, the boost is essentially doing nothing, but the high side rectifier is still in the main conduction path. A diode rectifier drops 0.5-0.7V, leading to significant power loss (and voltage headroom loss), whereas a FET only has a loss proportional to its R_{DS}(on), which is comparatively smaller. Conversely, an asynchronous boost has simpler control circuitry, and is typically significantly cheaper to design.

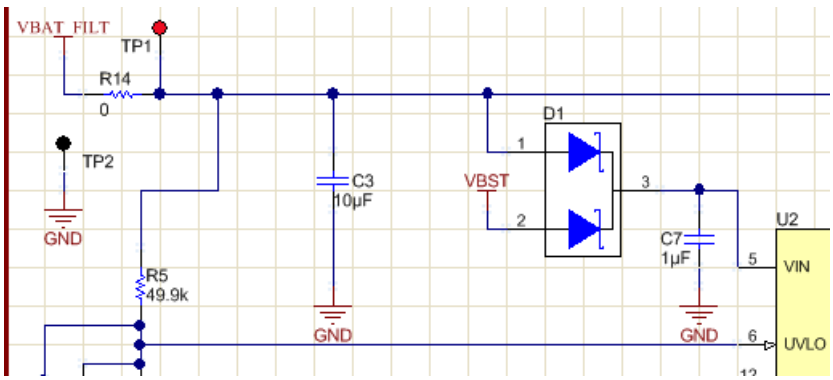
We ended up choosing a synchronous solution to enhance efficiency during bypass mode.

Below is the step by step design procedure for designing in the LM25122 into this application:

- Set Switching Frequency with resistor from SYNCIN/R_T pin to ground
  - We want 470kHz to place fundamental below AM band
  - $R_T = 9x10^9 / F_{SW} = 19.15k$. A standard value of 19.1k is the closest match
- Pull MODE pin high to set the device into Forced PWM mode, ensuring constant switching frequency across load conditions, and making it easier to design EMI filters around it
  - The ABS MAX of this pin is 15V, so we cannot tie to VIN. Therefore pulling it up to VCC (regulated 7.6V output) is the correct way of doing this if no other low-voltage rail is available on the board
- UVLO Resistors
  - The UVLO pin has an ABS MAX rating of 15V. A Zener diode is placed in parallel with the bottom resistor to clamp during overvoltage transients and not damage the pin. 49.9k chosen at random for the divider since we are not using this functionality and simply want the UVLO voltage to always be >1.2V (which is it's trip point for entering low power mode).



- Set the OPT pin
  - Used to set SYNC functionality. Tied to ground is most basic setting, clock is free running and set by R_T resistor
- Vin pins
  - Using a diode ORing technique, the booster output can be used directly to bias internal circuitry when Vin drops low, extending the V_{IN} range very low. This is technique is called "split rail" and is outlined in Reference 10 at the end of this document
  - The ORing diodes must have a reverse voltage rating of at least 40V



- Select FB resistor values (V_{OUT} = 9V, V_{REF} = 1.2V)
    - Choose R_{BOTTOM} = 10k
    - ((V_{OUT}/V_{REF})-1) * R_B = R_{TOP} = 65k (64.9k is closest standard value)
- Choosing FETs
    - V_{DS}(max) should be greater than the maximum V_{OUT}, which for us is the max Vin of the system (during bypass mode)
        - Need V_{DS}(max) >= 40V
    - Needs to be able to be driven by the part's gate drive
        - If V_{IN} > 6V, V_{DRIVE} = 6V
        - If V_{IN} < 6V, V_{DRIVE} = Vin
    - Needs to be able to handle the maximum SWITCH current (not load)
        - To be safe and reduce temperature rise, the FET should be chosen such that there is a large margin between the maximum switch current and its maximum drain current rating
    - Optimize for $R_{DS(ON)}$ – current rating & package (silicon) size are inversely proportional to $R_{DS(ON)}$, which effects efficiency
- Choosing an inductor
    - Assume worst case for V_{IN} and calculate duty cycle (Vout = 9V, Vin = 3.1V) -> ~0.655
    - Assume worst case output current of 2.2A
    - Inductor current is given by Equation 25 in the LM25122 datasheet:
        - I_L = I_{OUT}/1-D = 2.2/(1-.655) = 6.38A
    - Ripple current chosen to be 30% of I_L, which is ~1.9A. Therefore, our peak inductor current is:
        - I_L(peak) = (I_{RIPPLE}/2) + 6.38 = ~7.34A
    - By choosing a ripple current, we can now calculate the required inductance value:
        - I_{RIPPLE} = (V_{IN} / L) * (D * (1/F_{SW})) --> 1.9A = (3.1V / L) * (.655 * (1 / 470000Hz))
            - Solving for L we get a value of 2.27uH
    - Given 20% headroom on I_{L_Peak} -> 7.34 * 1.2 = 8.8A
    - We must choose an inductor with I_{SAT} > 8.8A, L = ~2.2uH, and optimize for small size and low ESR.
- Output Capacitors
    - This is dominated by the ESR of the output caps, in relation to the amount of ripple current flowing through them
    - We want to define a maximum ripple voltage on the output
        - Choose 3% of VOUT, so 0.03 * 9V = 270mV pk-pk ripple
    - We have already chosen a ripple current level when selecting our inductor: 1.9A
    - Equation for output voltage ripple:
        - V_{RIPPLE} = I_{RIPPLE} * (R_{ESR} + (1/(4* C_{OUT} *F_{SW})))
        - 0.27 = 1.9 * (.02 + (1/(4* C_{OUT} *470000)))
        - C_{OUT}(min)= 4.3uF
            - Doesn't take a lot to achieve this, but we also need to take into account our transient response characteristics

- Need significantly more capacitance to handle load-transients. In pre-boost this is very important since the device will usually turn on into a full load
- Choose 4x10uF, plus the two on the input of the LM53603

- Input capacitors
  - Needs to be sufficient to handle RMS current, so usually requires multiple parallel capacitors. Ceramic capacitors can handle significant ripple current without self-heating due to their low ESR. However, a bulk capacitor with high ESR is still necessary to raise the input impedance of the converter and avoid oscillations with the EMI filter

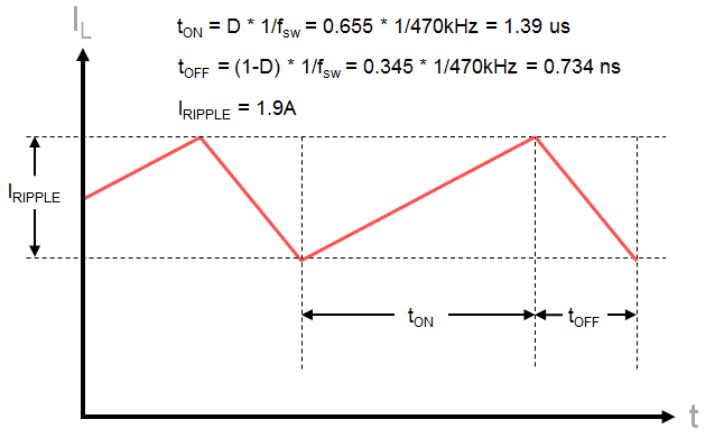
5.5 EMI Filter

As discussed in a previous section on Conducted Emissions testing, DCDC converters can couple a lot of energy (especially at its fundamental switching frequency) back through the battery inputs and into the rest of the vehicle. This energy is mostly produced because of the switching action of the input current waveform, which is translated into voltage noise by the ESR of the input capacitors which carry most of this current. A low-pass filter, placed between the input of the module and the DCDC converters, can attenuate this noise. It also filters incoming noise from entering our system, which is an added benefit.

There are two ways to design this filter: empirically, and theoretically (by calculation and simulation).

The empirical approach is to design your system **without** the EMI filter, measure the conducted emissions with a spectrum analyzer, and compare it to the standard you are trying to pass (for us, CISPR25). Then calculate the attenuation you would need to pass at certain frequencies, and simply place the corner frequency of your filter low enough to achieve that attenuation. The downside of this is that you have to wait on hardware to begin the design, gain access to a testing lab to get initial results, and then modify the hardware and re-test later. This isn't a bad method, but we didn't have any initial hardware to test with, and most designers won't have ready access to a testing chamber, and want to be able to pass on their first try, or with some minor adjustments in the chamber.
The theoretical approach is a little more complicated but still very intuitive:

- We fist make the assumption that the boost converter is our main culprit, and that noise generated by the downstream buck will be filtered by the boost inductor/caps
- The main sources of noise will be the at the switching frequency of the boost (470kHz), and it's harmonics. If we can estimate the amplitude of the noise at that frequency and attenuate it appropriately, the harmonics will be attenuated as well.
- First, let's look at the input current waveform of the boost, which is an asymmetric triangular wave:

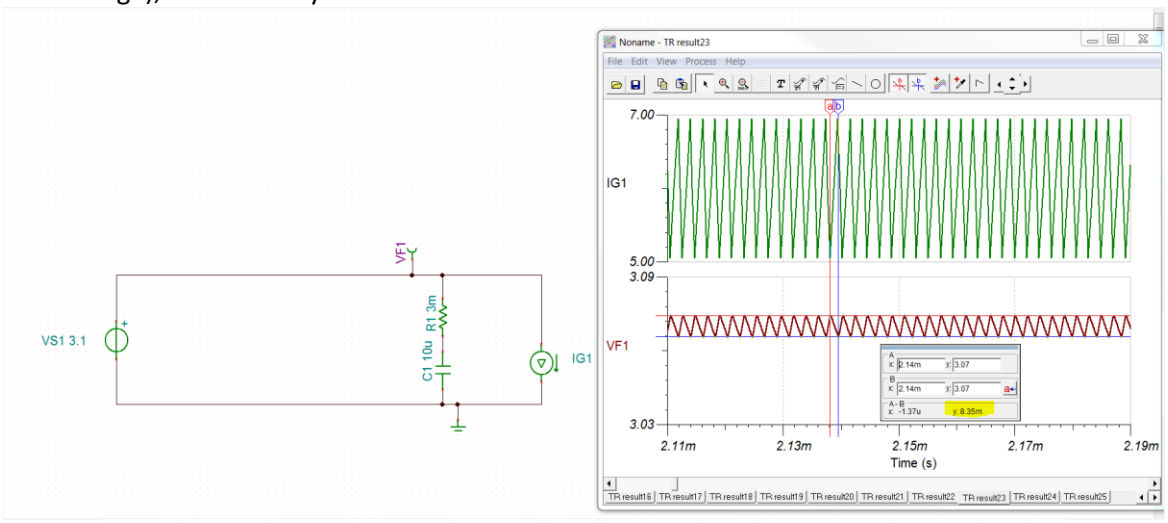


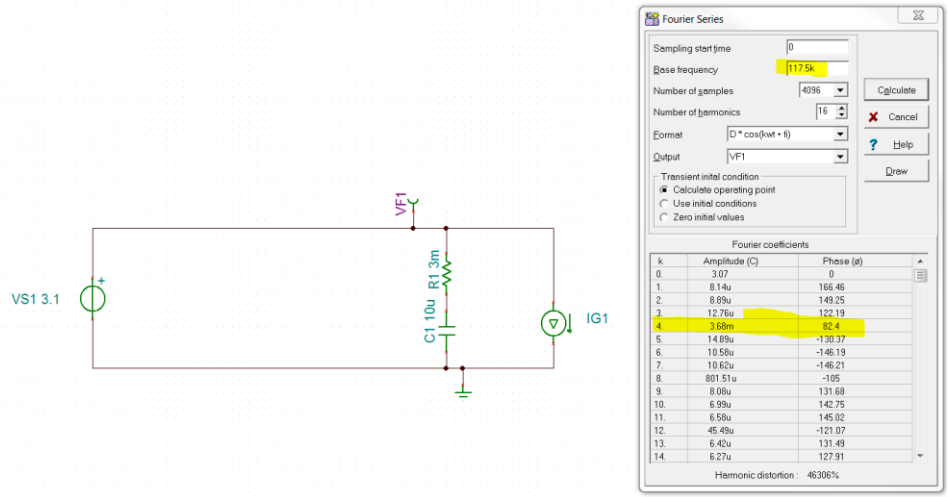
- The input voltage is basically the voltage generated by the ripple current through the ESR of the input capacitors. Since we are using ceramic capacitors, this ESR is very low, around 3mΩ. Therefore the peak amplitude of the input voltage ripple is around 3mΩ * 1.9A = 5.7mV
- However, we are concerned with the frequency content at 470kHz, and not the time domain.
    - By taking the Fourier transform of this asymmetric triangle waveform, we can find the coefficients/amplitudes of each of the component frequencies. The math for this is left out, but you can find instructions for this easily.
    - The coefficient of the fundamental for this type of waveform is found to be 0.8, so we can multiple that times our time domain amplitude to find the energy at 470kHz
        - 0.8 * 5.7mV = **4.56mV**
    - We convert this to dBuV to make analyzing it with respect to the CISPR 25 standards easier: 20 * log(4.56mV / 1uV) = ~**73dBuV**
- Now that we know what the energy content is at 470kHz, we can compare this to the CISPR25 spec and calculate how much to attenuate
    - The CISPR25 spec does not define a limit at 470kHz (we did this on purpose), but the limit at 530kHz for Class 5 conducted emissions is 54dBuV (peak), which means we need an attenuation of at least **19dB**
    - In order to provide more margin, we will shoot for 40dB attenuation at the switching frequency
- Now that we know how much attenuation we need at 470kHz, we can calculate where to place the corner frequency of the filter. Since we are using a 2nd order low pass filter (LC Pi filter), it will have a roll-off of -40dB/decade. Therefore, to get 40dB of attenuation at 470kHz, we need to **place our corner frequency (f_c) at 47kHz**
    - The corner frequency is related to the values of the filter inductor and capacitor by the following formula: $2\pi * f_c = \frac{1}{\sqrt{L*C}}$
    - We have two degrees of freedom here, so we just choose a convenient L of 2.2uH. We already have an appropriately sized 2.2uH inductor on the board, so this helps consolidate BOM items
    - Calculating out for C, we get ~5.2uF. This is not a standard value, so we will choose a larger value instead, 10uF. Choosing a larger value will only lower the corner frequency of our filter, providing more attenuation at 470kHz. In addition, ceramic capacitors suffer from DC bias effects and usually truly operate at less capacitance than they are rated
- Our filter is now designed! The last step is to add a damping capacitor C_D with a high ESR on the output of the filter. The purpose of this is to raise the input impedance of the boost converter, which helps avoid oscillations between the filter and boost tanks. Please see

reference [9] for a further discussion of this. The two guidelines for choosing the capacitor are:

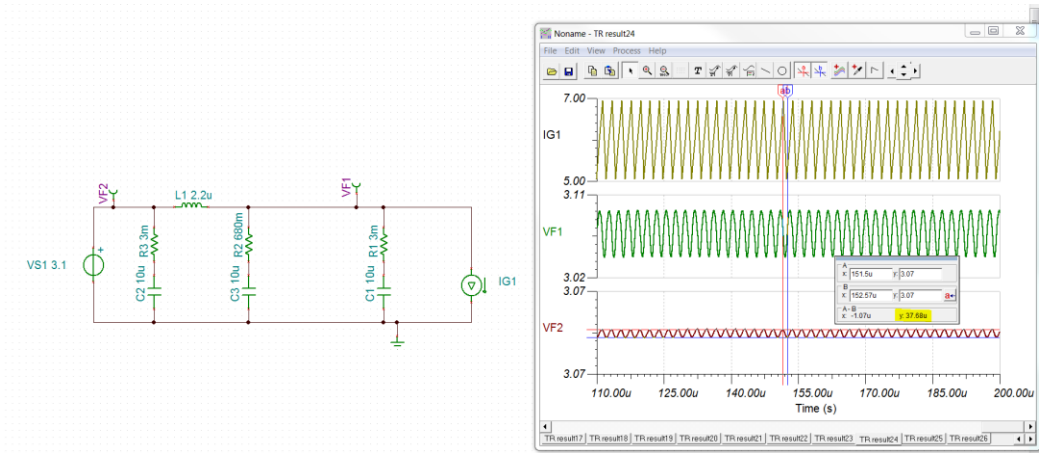
- $C_D > 4*C_{IN(boost)} \rightarrow C_D > 4 * 10uF$
- $ESR_{Cd} > \sqrt{\frac{L_f}{C_f}} \rightarrow ESR > \sim 0.469\Omega$
- We choose a polarized capacitor with values C = 47uF and ESR = 600mΩ, which satisfies our requirements

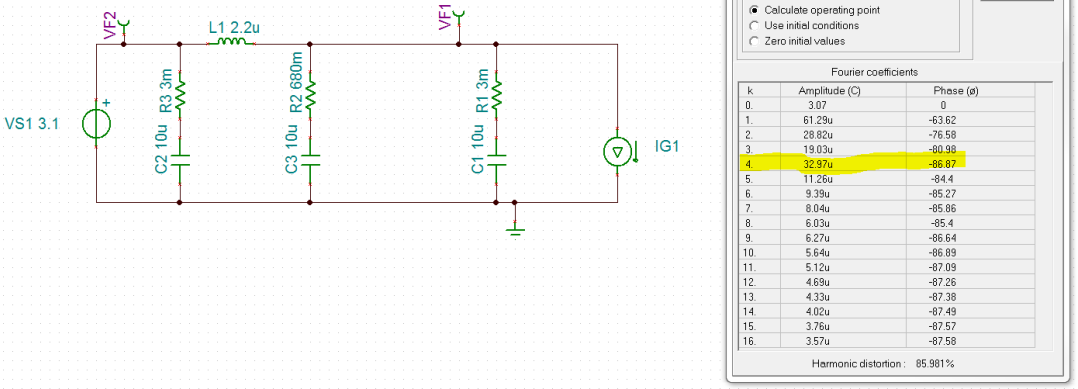
- Finally, we can verify the filter performance with simulations using TINA (TI SPICE simulator). Here is the circuit without filter. IG1 models the boost converter as a variable constant current source. C1 is the input capacitor (with ESR) of our converter. The results show an 8.35mV ripple voltage (1st image), and 3.68mV/71dBuV at the switching frequency (2nd image), which is very close to our calculation earlier earlier:





- With the addition of the filter, the amplitudes are reduced to values expected from our calculations:





- Converting the bottom result, we get 30.36 dBuV, which is almost exactly 40dB of attenuation, as we calculated.

5.6 Buck Converter

The buck converter is the main component of this design. Several factors go into choosing a good buck converter for off-battery operation:

- Most importantly, the input voltage range should be higher (with margin) than the highest possible input voltage it could see. For us this is a combination of the maximum Load Dump voltage, as well as the maximum clamping voltage of our protection circuitry, in the 30-38V range. The LM53603 has a maximum DC range up to 36V, transients up to 42V, which is appropriate
- The switching frequency should be above or below the AM band (~530 – 1800kHz) to avoid placing the fundamental in that protected band, which would make it very hard to pass EMI. Placing it above the band has the added benefit of shrinking external components. The LM53603 has a 2.1MHz nominal switching frequency, which is perfect.
    - The switching frequency should also maintain its nominal value over V_{IN} range
- The buck should have good dropout performance. In 3.3V systems without pre-boost, this is even more important, allowing the V_{IN} of the system to fall very low without losing regulation.

- Integrated FETs and compensation greatly reduce design complexity and size of solution

Here is a step by step procedure for most of the design of the circuit:

- A 0.1uF capacitor needs to be placed on the BIAS pin to decouple the input to the internally generated voltage regulator
- Connect FPWM pin to VCC, **NOT** to V_{IN}
  - This sets the part in forced PWM to maintain switching frequency at light loads
  - ABS MAX of this pin is not high enough to connect to V_{IN}

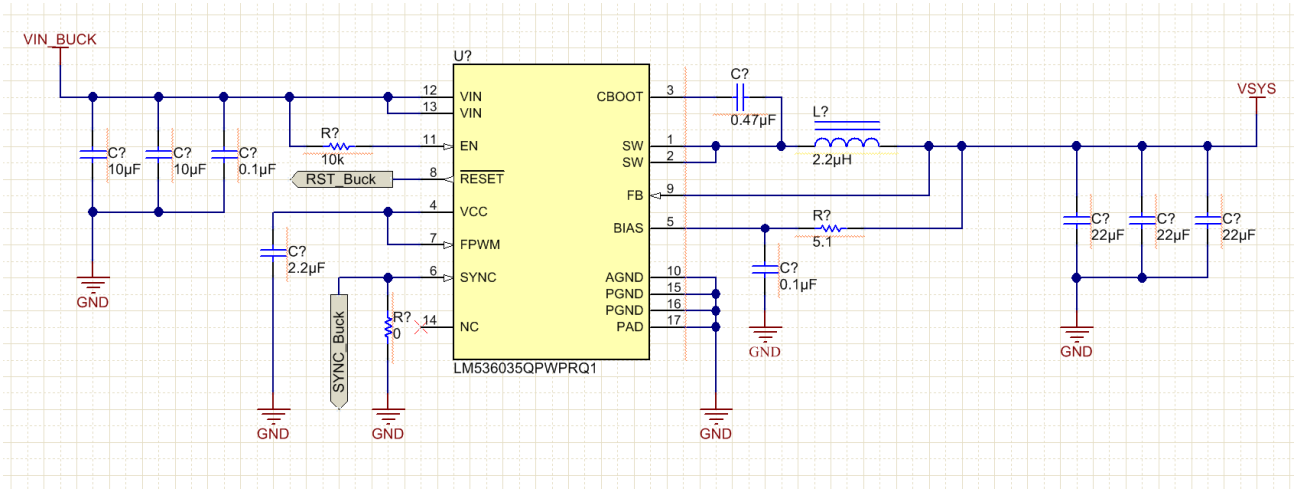


Figure 11: Completed LM53603 Schematic

- Choosing an inductor
  - The calculation can be done similarly to that of the boost to get the desired ripple current. The datasheet actually recommends a 2.2uH inductor which ends up being a good choice for this current level and input/output ratio. In addition, by following the datasheet, we can feel comfortable that our output filter will work with the internal compensation network.
- Add output capacitors
  - Since the compensation network is internal to the device and cannot be tuned, the designer must place the LC output pole in a given range to ensure stability. The datasheet provides recommendations the values of L and C_{OUT} which should be followed.
  - Keep in mind the voltage rating of ceramic output capacitors. Ceramic capacitors lose some capacitance due to DC biasing, which scales as a function of the percentage of the total voltage rating. Make sure your ceramic caps maintain enough effective capacitance at your operating point and de-rate accordingly.
- Add input capacitors
  - Values are chose such that they can handle the RMS ripple current. Ceramic capacitors are capable of handling a lot of RMS current due to their low ESR
  - These need to be 50V due to being exposed directly to battery voltage
  - These are sort of “shared” with the boost’s output capacitors which also help to handle the ripple current

5.7 General Power Supply Design Considerations

Choose inductors for DC-DC converters such that:

- The ripple current is between 20-40% of the load current I_{LOAD} (with the given F_{SW}, V_{IN}, and V_{OUT}). For this design, 40% was used.
- The temperature ratings are appropriate for an automotive application, typically -40°C to 125°C for ADAS applications.
- Saturation current is chosen per the following equation for peak current, plus additional margin:

$$I_{SAT} \geq (I_{LOAD} + \frac{1}{2} I_{RIPPLE}) * 1.2$$

For ADAS applications, it is recommended that all ceramic capacitors use X7R dielectric material, which ensures minimum capacitance variation over the full temperature range. The voltage rating of the capacitors should be greater than the maximum voltage they could see, and 2x the typical voltage they see to avoid DC bias effects. The amount of output capacitance used depends on output ripple and transient response requirements, and there are many equations and tools available online to help estimate these. Supplies in this solution were designed for a +/-2.5% (5%) total transient response. Low-ESR ceramic capacitors were used exclusively to reduce ripple. For internally-compensated supplies, please see device-specific datasheets, as they may have limitations on acceptable LC output filter values.

IC's should always be qualified per AECQ100. TI parts which are qualified will typically end their part numbers with "Q1".

For improved accuracy, all FB resistor dividers should use components with 1% or better tolerance.

0Ω resistors are used at the input and output of all of the supplies for testing purposes only, and could be removed if needed in a production board.

6 Getting Started Hardware

The TIDA-00699 is quite easy to get set up with. Please refer to the below diagram:

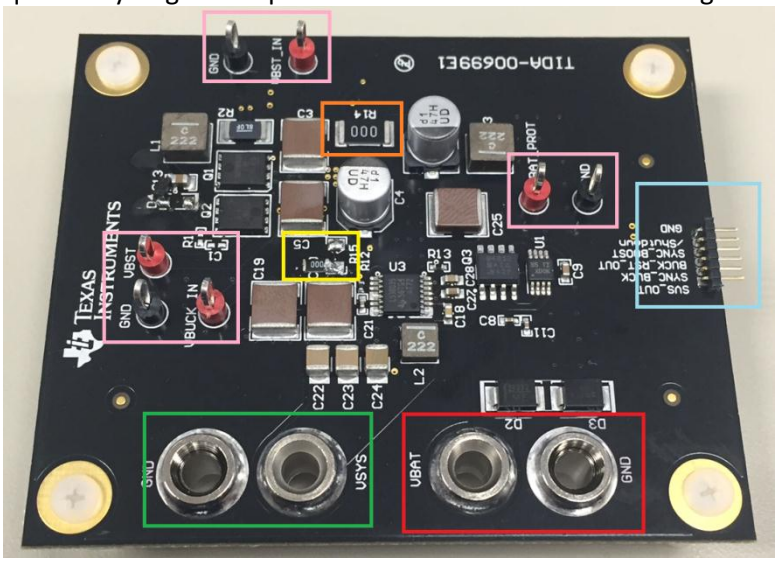


Figure 12: Getting started with the board

- The connectors **boxed in red** are for the input voltage to the system. These are female receptacles for standard banana plugs. Acceptable limits for input voltage are 3.2-36V, and a 10A limit should be set on the power supply if possible
- The connectors **boxed in green** are for the system output. They are also receptacles for banana plugs. They can be connected to an external load.
- The resistor **boxed in yellow** is a 0 ohm which can be used to disconnect the output of the boost converter from the input of the buck converter. The resistor **boxed in orange** is also a 0 ohm which can disconnect the boost converter from the input filter/protection circuitry. These make it possible to test each device on its own.
- The header **boxed in blue** has some signals to shut down the devices, sync them to external clocks, or to monitor the system output voltage via the Supply Voltage Supervisor output.
- The test points **boxed in pink** can be used to hook test probes onto

7 Test Setup

The following diagrams show how to set up for various tests

7.1 Ripple and Thermal Image Setup

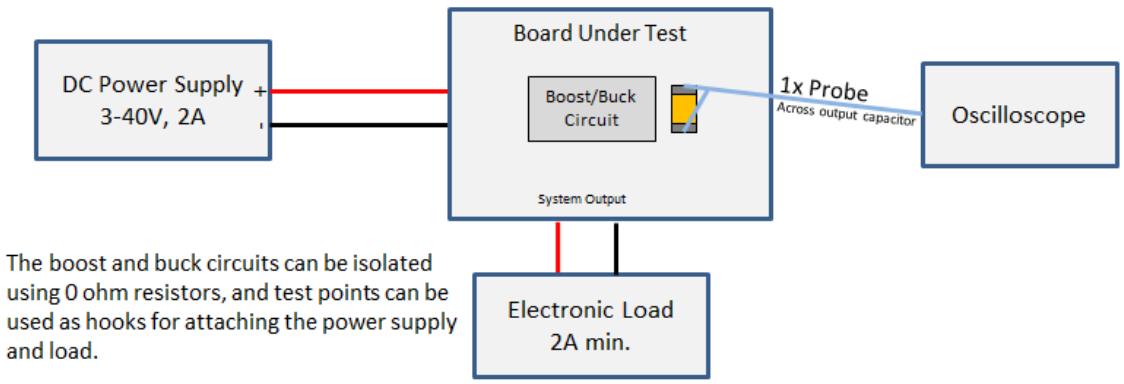


Figure 13: Setup for measuring output voltage ripple of DCDC converters

7.2 Efficiency Setup

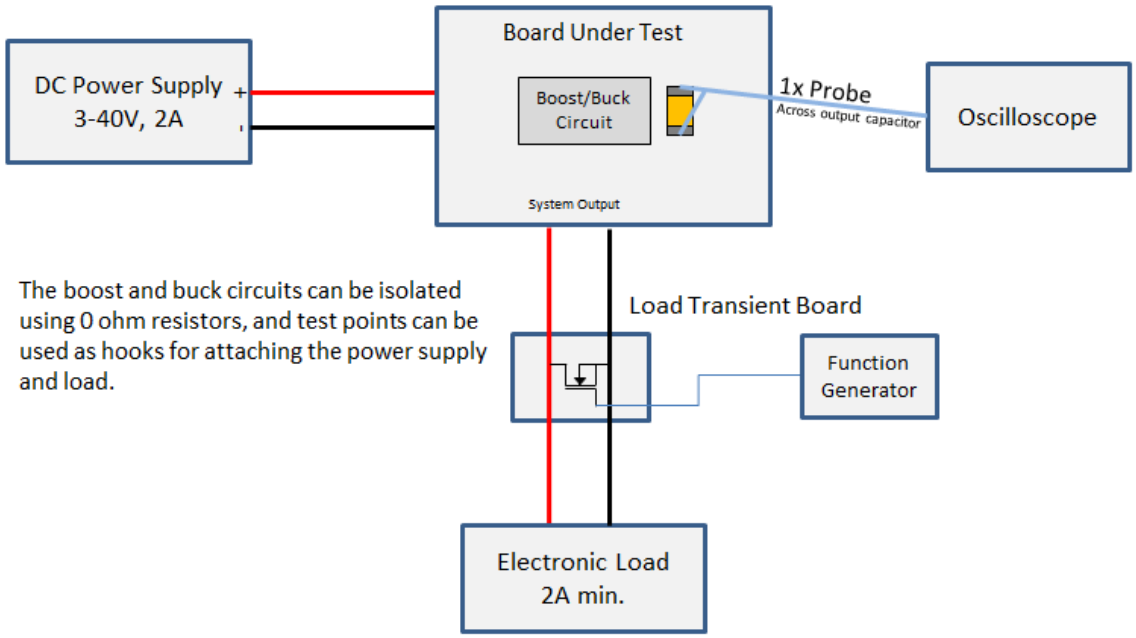


Figure 14: Setup for measuring DCDC efficiency

7.3 Load Regulation Setup

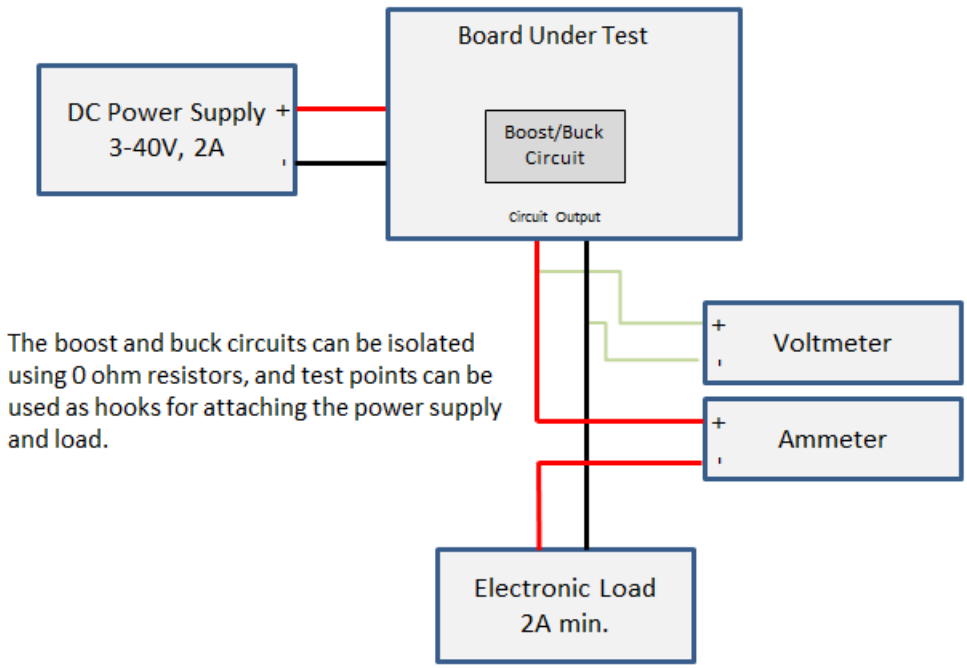


Figure 15: Setup for measuring Load Regulation

7.4 Electrical Transient Setup

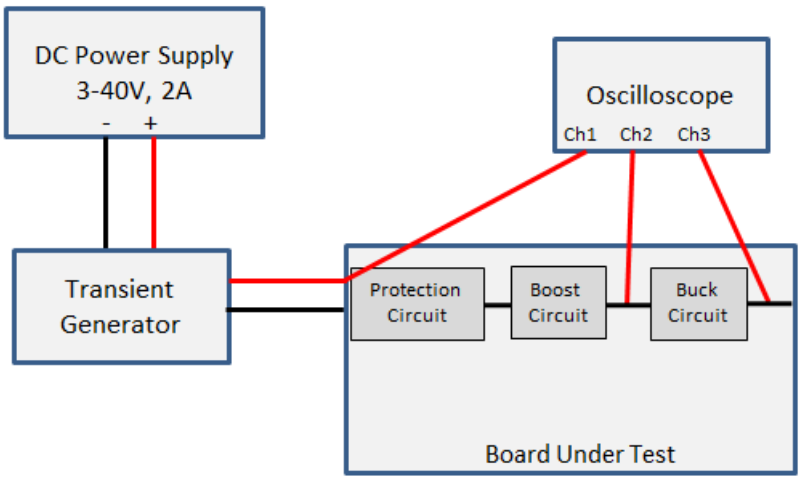


Figure 16: Electrical Transient Setup (NSG 5500 used for Transient Generator)

To work with the NSG 5500 you will also need the Teseq AutoStar software, which has pre-defined pulses which the user can tweak to meet specific requirements. Below is an example:

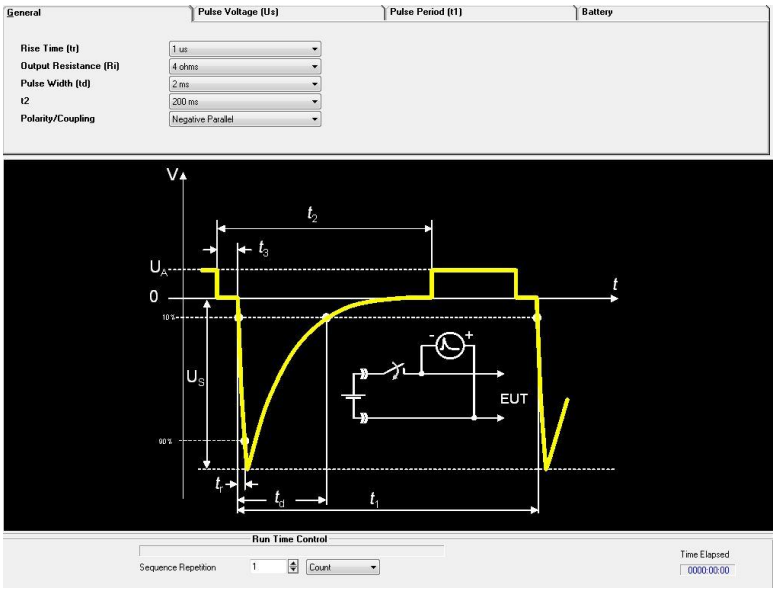


Figure 17: AutoStar setup for Pulse 1

8 Test Data

The following sections show the test data from characterizing the switching power supplies in the system.

8.1 Efficiency

Below are the results of the efficiency test on the system. The VIN that is given is what is applied to the board inputs, not the voltage at the input of the boost converter power stage. This implies that this is a measure of the **total system efficiency** taking all losses into account, and not simply that of the boost+buck combination.

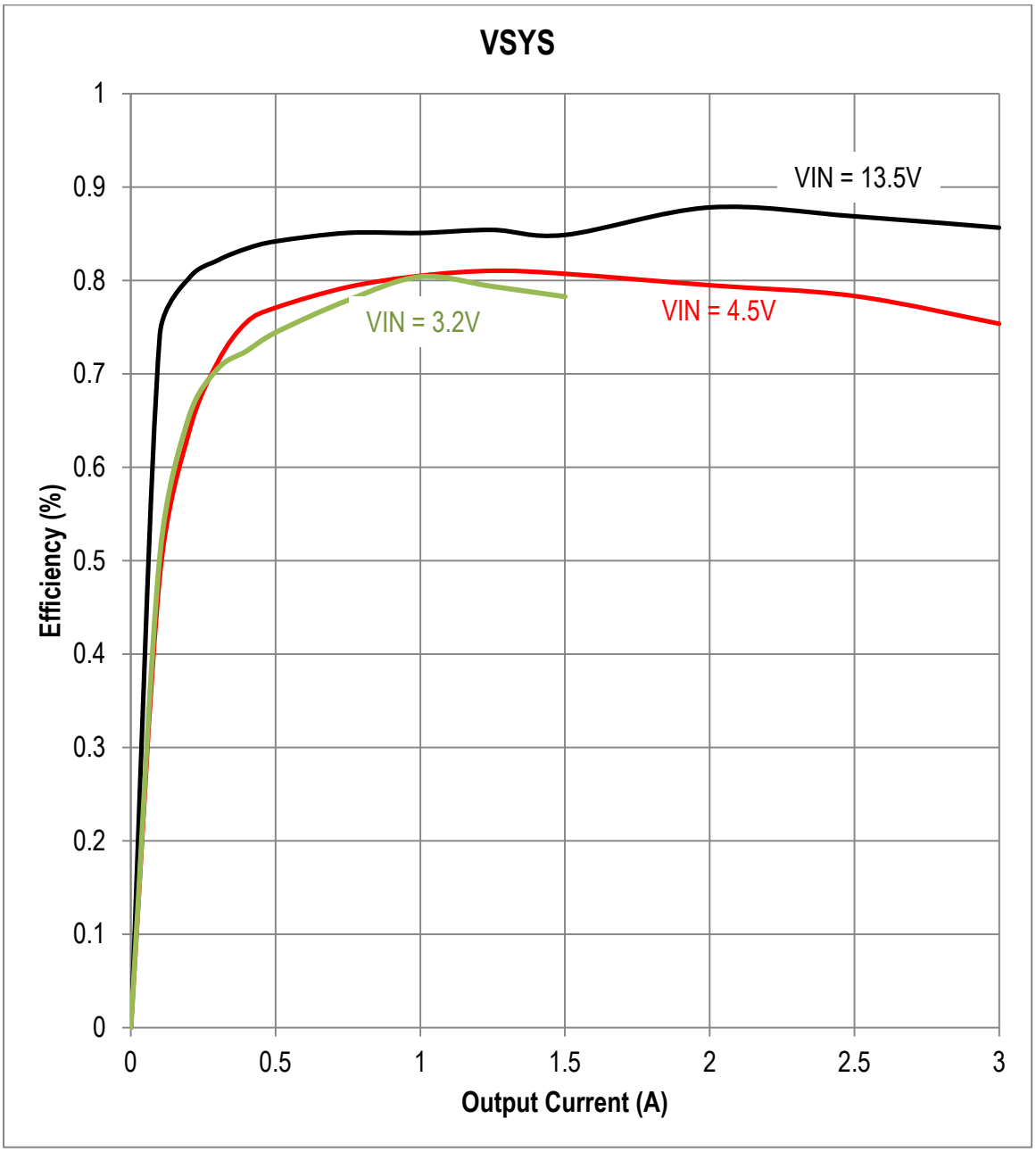


Figure 18: System efficiency

8.2 Load Regulation

The results below show the % deviation from nominal output voltage as a function of output current and input voltage. Due to losses between the system input and the boost converter, full load cannot be achieved at 3.2V because the affective input voltage to the power stage is too low. The voltage at the system input needs to be ≥3.8V in order to drawn more than 1.75A.

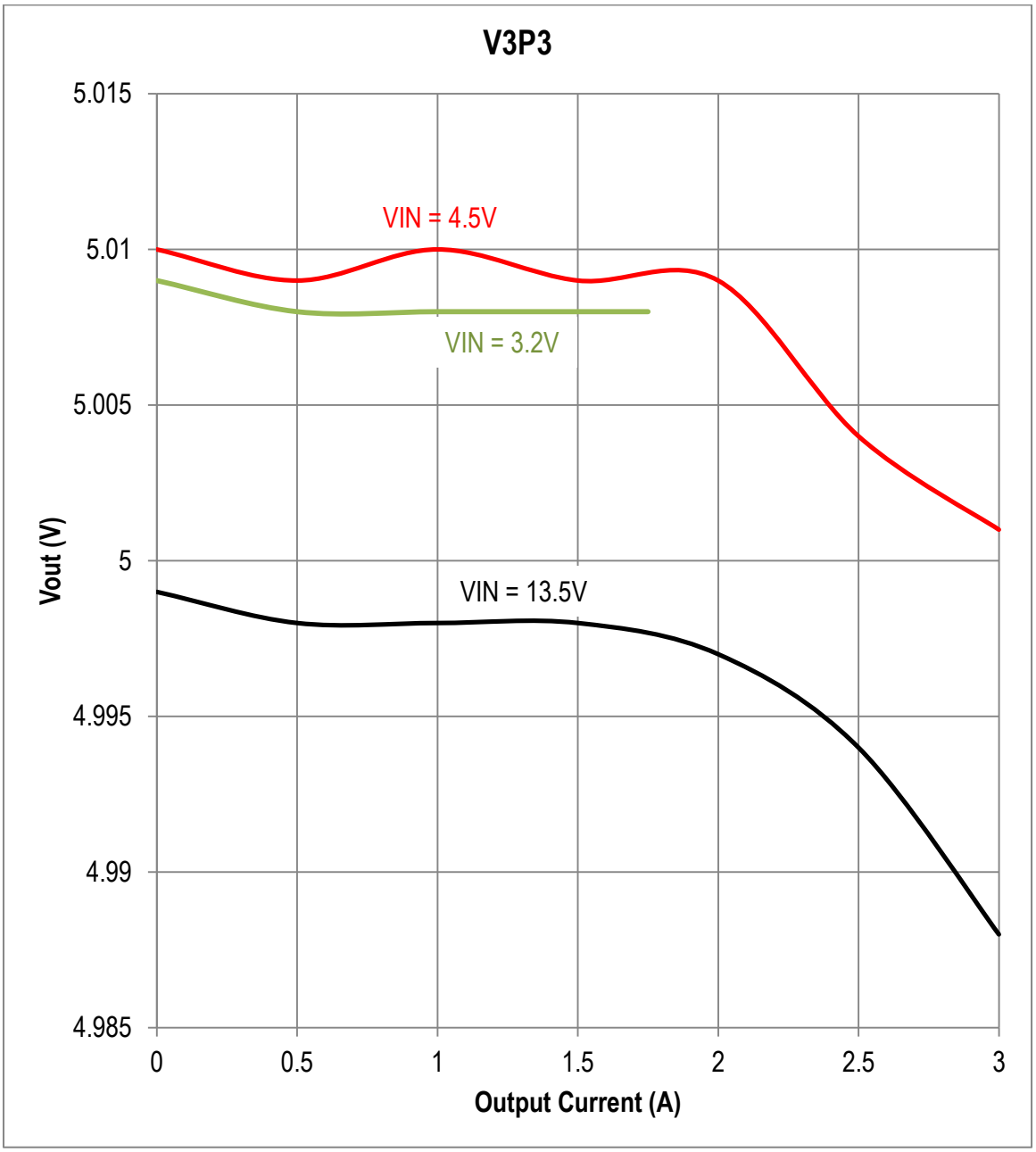


Figure 19: VSYS Load Regulation

8.3 Output voltage ripple

The images below show the output voltage ripple of the system output voltage at different Vin and Iout levels.

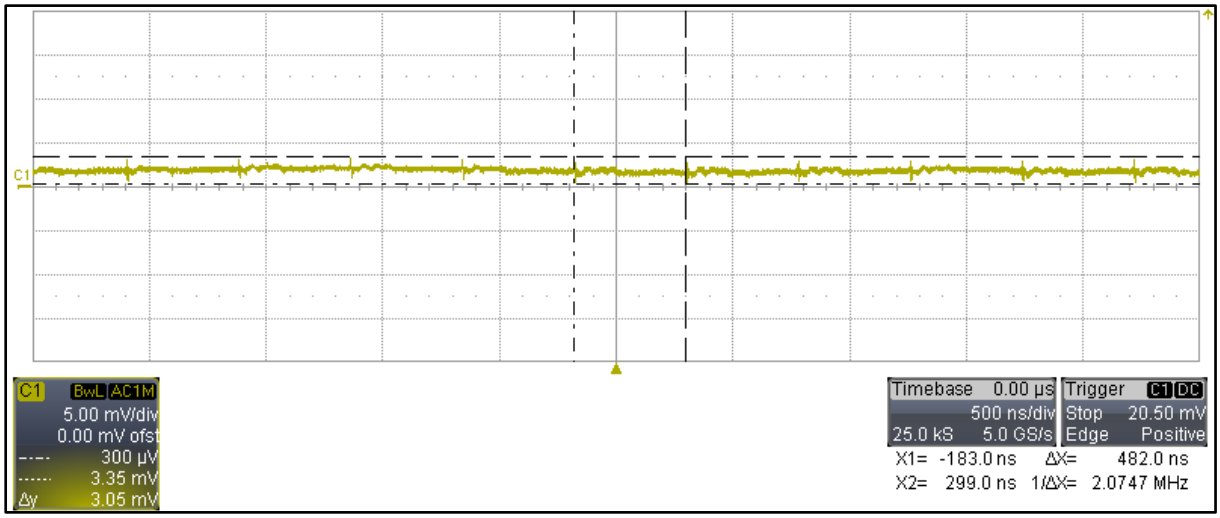


Figure 20: Vin = 13.5V, Iout = 0A

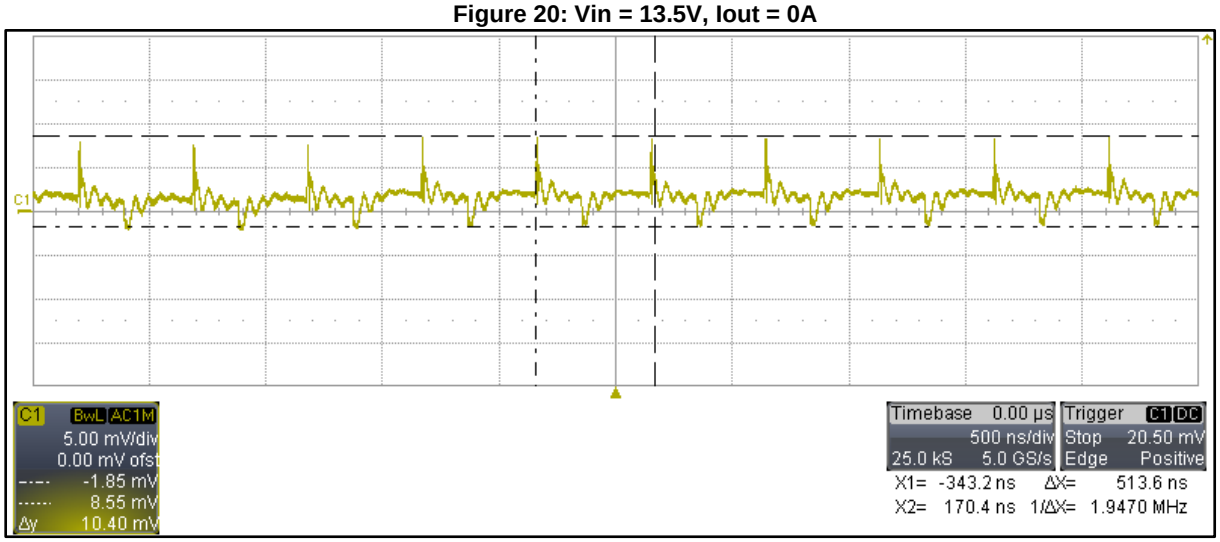


Figure 21: Vin = 13.5V, Iout = 2.5A

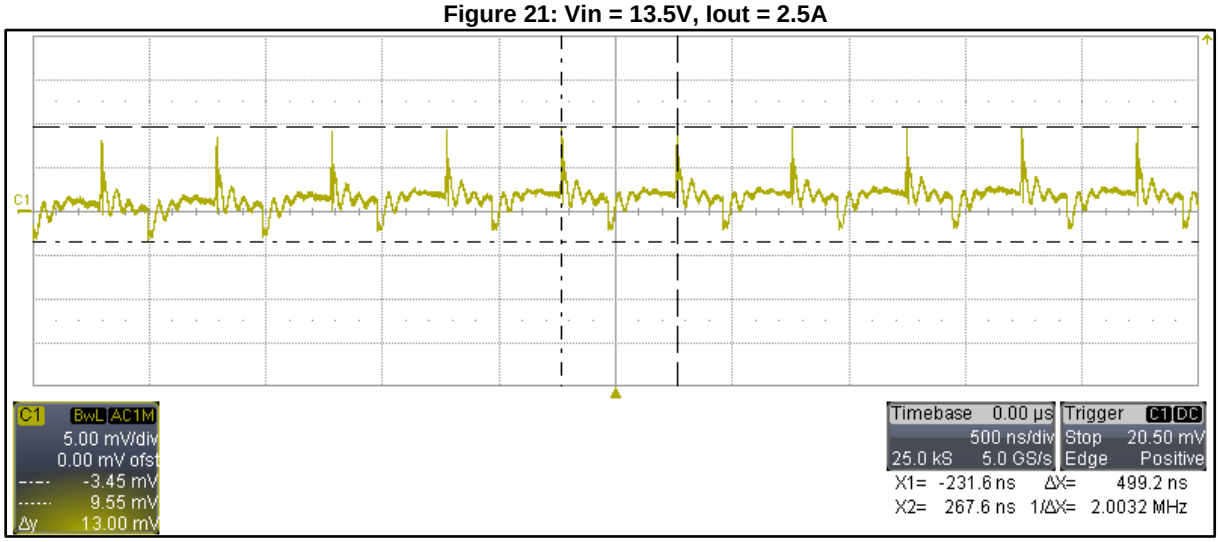


Figure 22: Vin = 13.5V, Iout = 3A

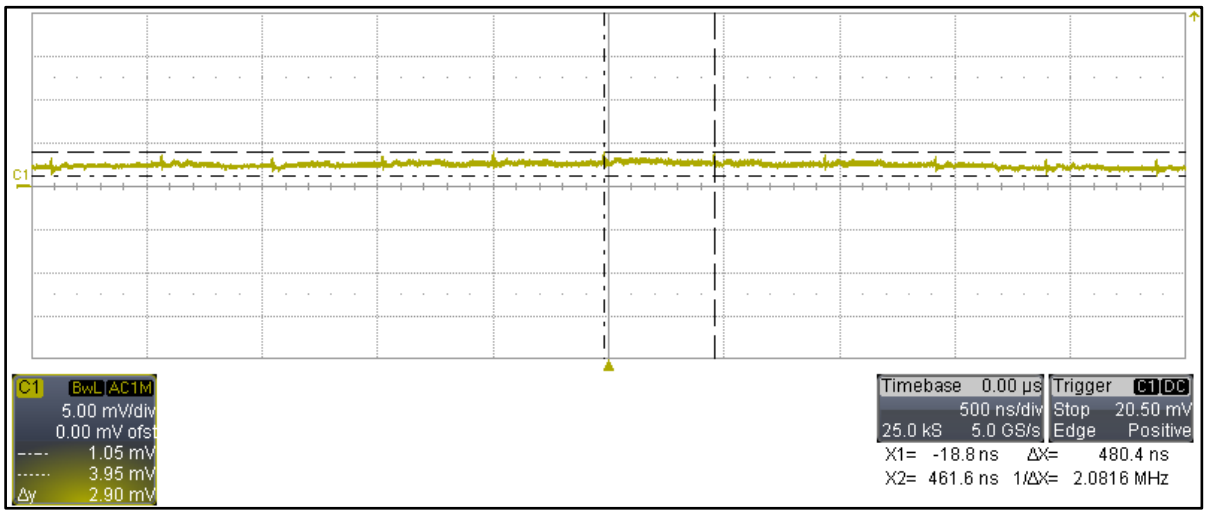


Figure 23: Vin = 3.2V, Iout = 0A

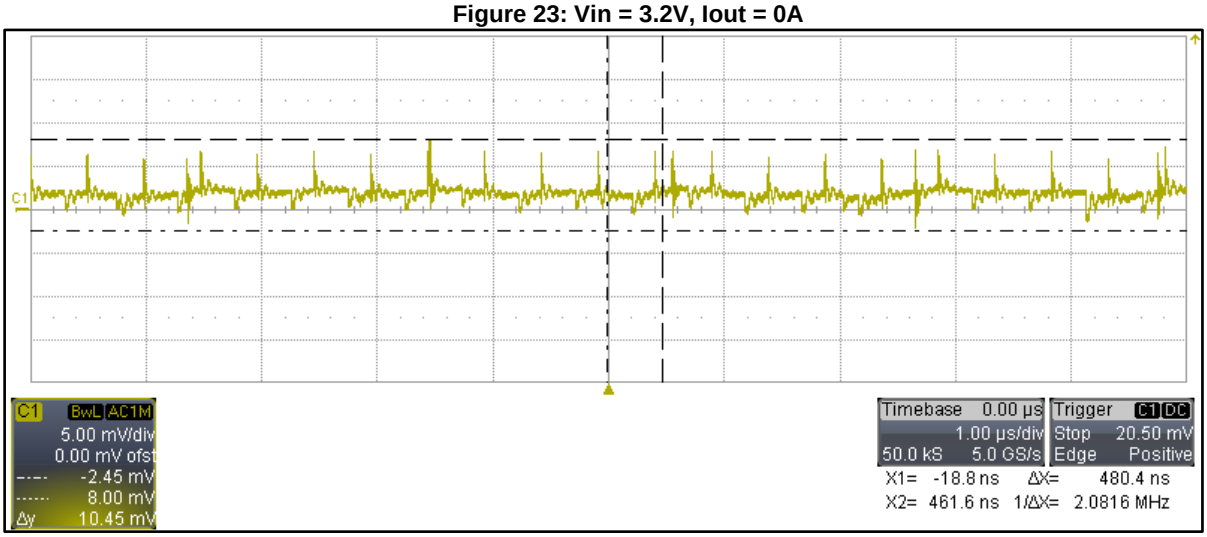


Figure 24: Vin = 3.2V, Iout = 2.5A

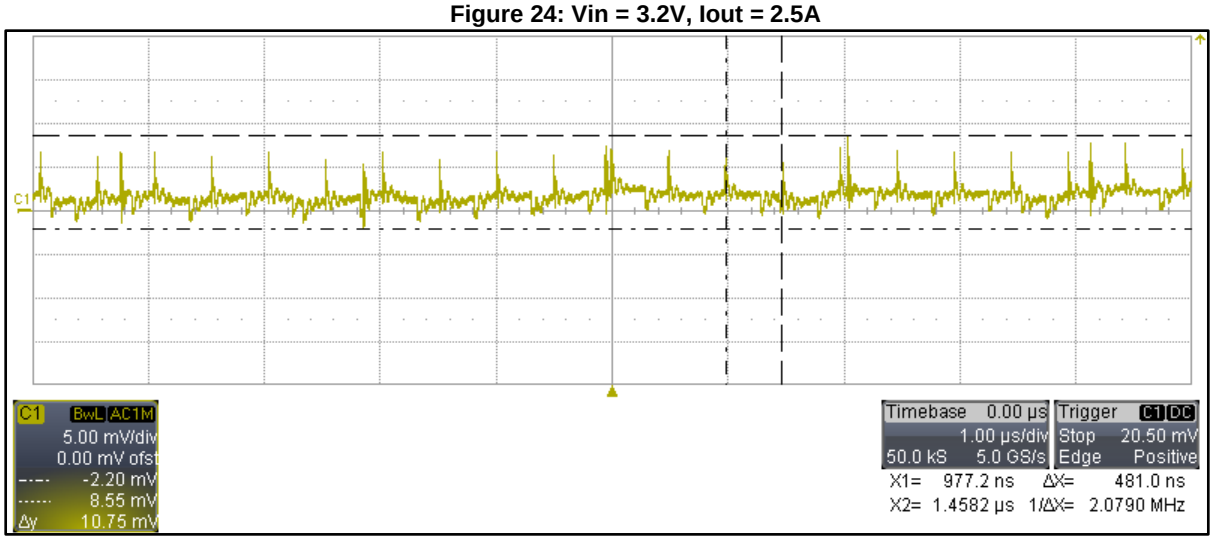


Figure 25: Vin = 3.2V, Iout = 3A

8.4 Thermal images

All of the thermal images were taken after the temperature had settled for at least 1 minute. We tested at normal operating voltage (13.5V) as well as the lowest input voltage (3.2V). These are the voltages **at the board input** and don't take into account losses between there and the power stage. The full load range could not be tested at 3.2V due to reasons outlined in other sections.

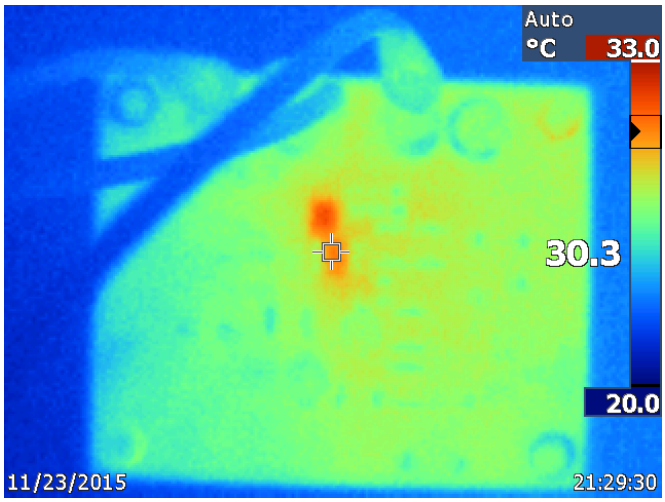


Figure 26: Vin = 13.5V, Iout = 0A

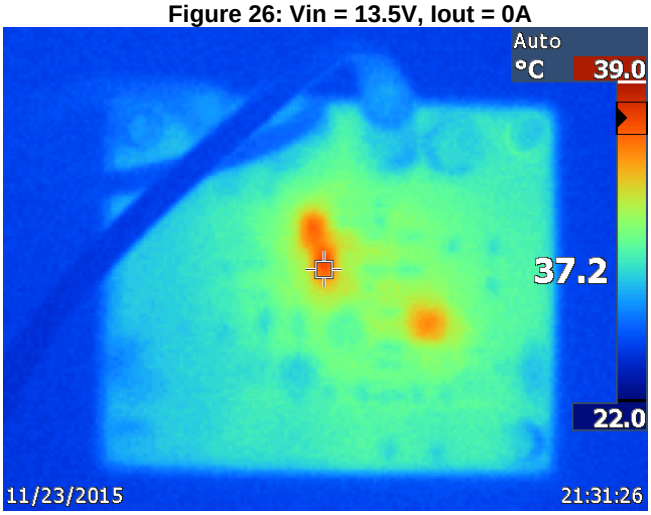


Figure 27: Vin = 13.5V, Iout = 1A

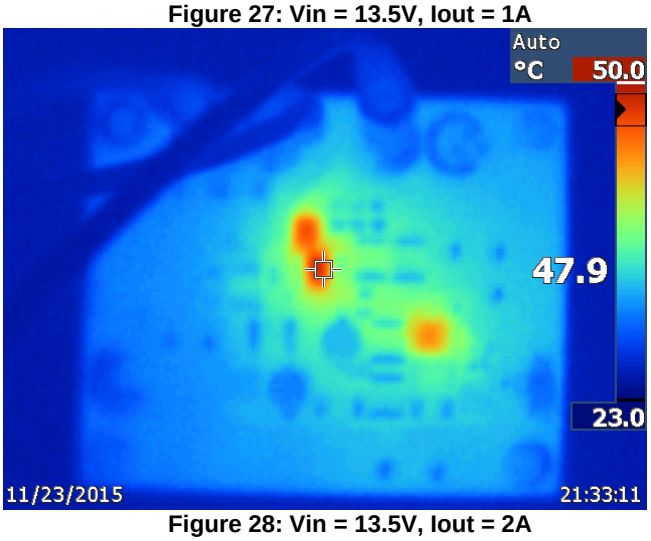


Figure 28: Vin = 13.5V, Iout = 2A

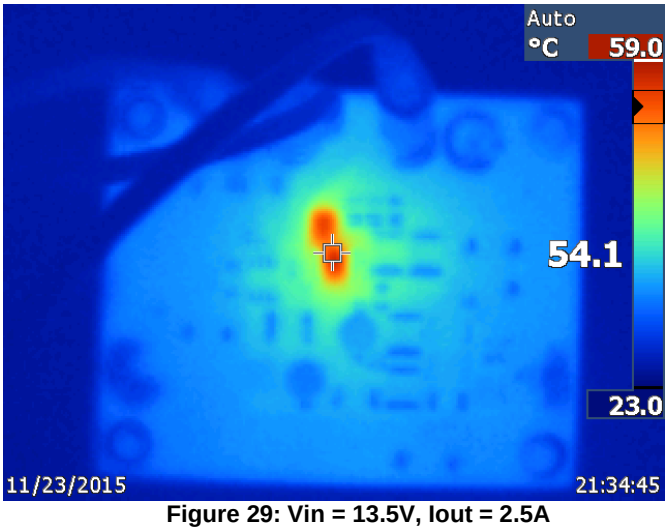


Figure 29: Vin = 13.5V, Iout = 2.5A

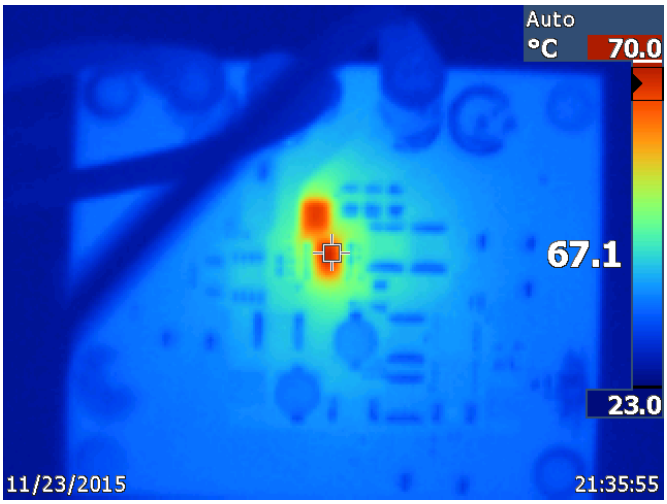


Figure 30: Vin = 13.5V, Iout = 3A

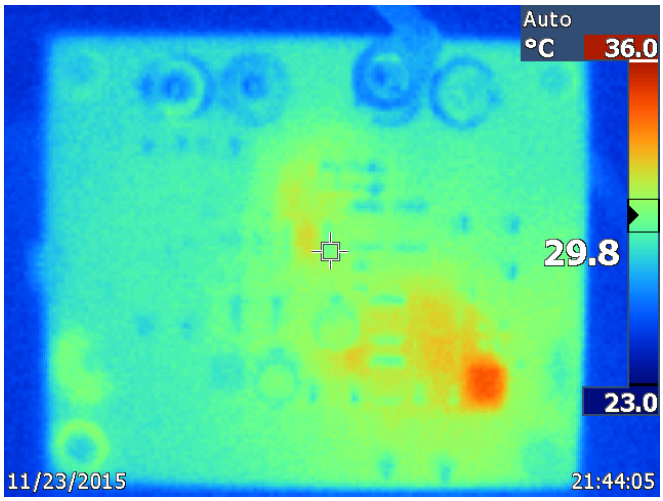


Figure 31: Vin = 3.2V, Iout = 0A

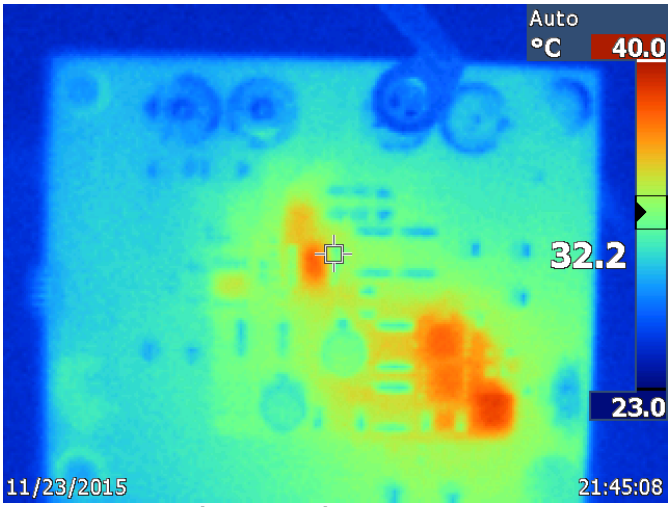


Figure 32: Vin = 3.2V, Iout = 1A

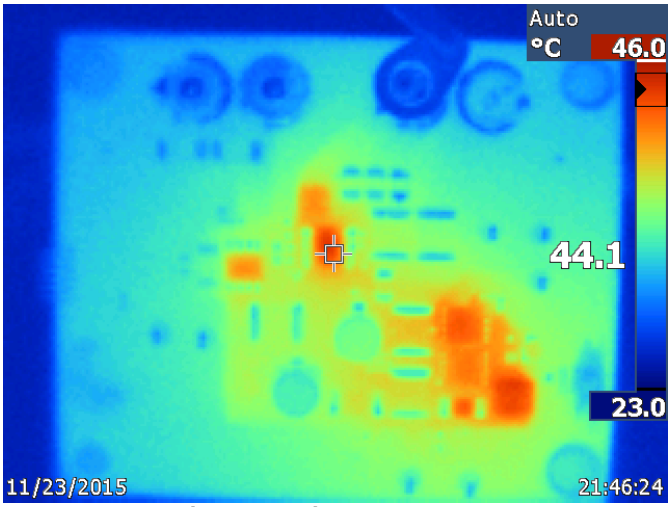


Figure 33: Vin = 3.2V, Iout = 1.5A

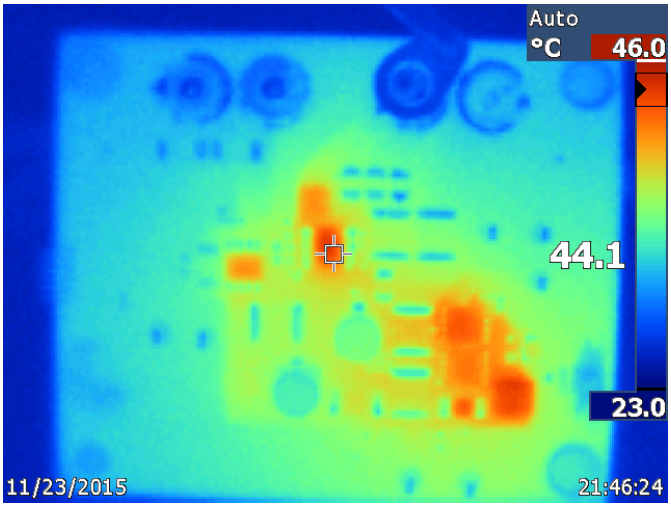


Figure 34: Vin = 3.2V, Iout = 1.75A

8.5 Electrical Transient Testing

We performed three electrical transient test pulses to verify our transient suppression scheme: ISO 7637-2:2004 Pulse 1, 2a, 3a, 3b, and 5b (Clamped/Suppressed Load Dump). A battery DC voltage of 13.5V is used for all tests.

8.5.1 ISO Pulse 1

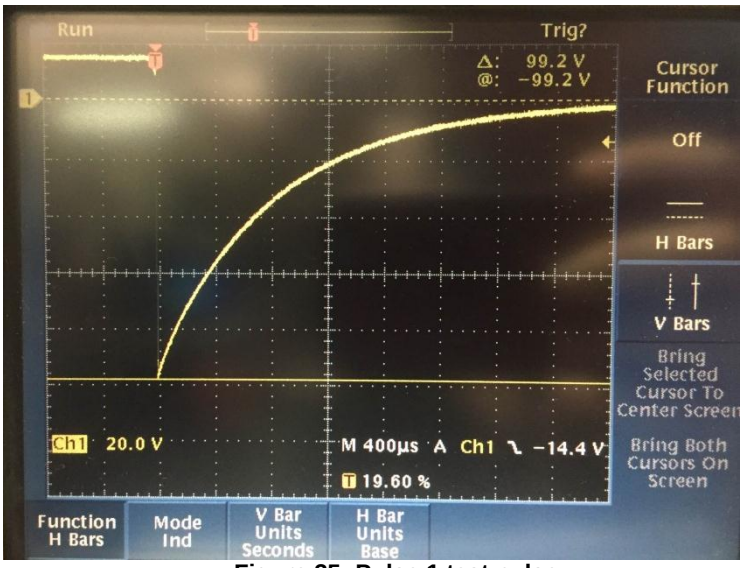


Figure 35: Pulse 1 test pulse

The pulse was first verified open-circuit. The following parameters were used:

- V_{min} = -100V (-99.2 achieved)
- R_{source} = 4Ω
- T_{rise} = 1µs
- $T_{duration}$ = 2ms

We then subjected our circuit to the pulse (blue trace) and measured the disturbance to the input of the power stage (yellow trace) as well as the system output (purple trace):

Figure 36: TVS circuit clamps the negative voltage to -21V

Though it is not shown here, the LM74610 disconnects the circuit from the input within a few µs of the pulse, and the output is sustained by the residual charge on the input capacitors until the supply voltage recovers.

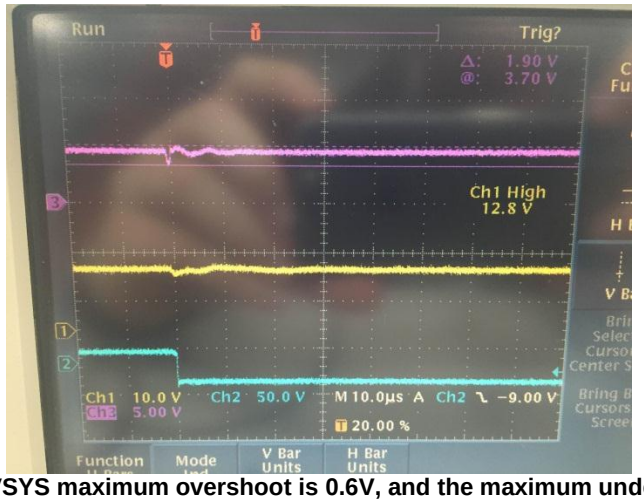


Figure 37: VSYS maximum overshoot is 0.6V, and the maximum undershoot is -1.3V

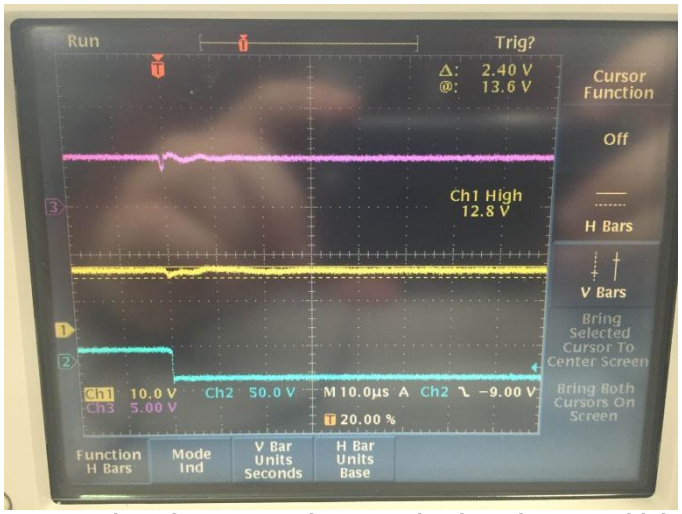


Figure 38: Maximum overshoot is 0.1V, maximum undershoot is 2.3V, which is still well within the normal operation conditions of the battery voltage

8.5.2 ISO Pulse 2a

Figure 39: Pulse 2a test pulse

The pulse was first verified open-circuit. The following parameters were used:

- V_{pulse} = 75V (77.2V achieved), superimposed on 13.5V DC (so ~90.7V max)
- R_{source} = 4Ω
- T_{rise} = 1µs
- $T_{duration}$ = 50µs

We then subjected our circuit to the pulse and tried to measure the disturbance to the system output. However, due to the TVS clamping and the damping done by the input filter, the pulse is not even visible at the inputs of the board, so it wouldn't be descriptive to show an image of it. This is good though – a combination of the TVS and LC filter successfully attenuate this pulse to negligible levels before it even reaches the input of the power stage.

However, to showcase the effect of the clamping circuit alone, we modified the board to isolate everything except for the diodes by lifting the reverse battery protection FET:

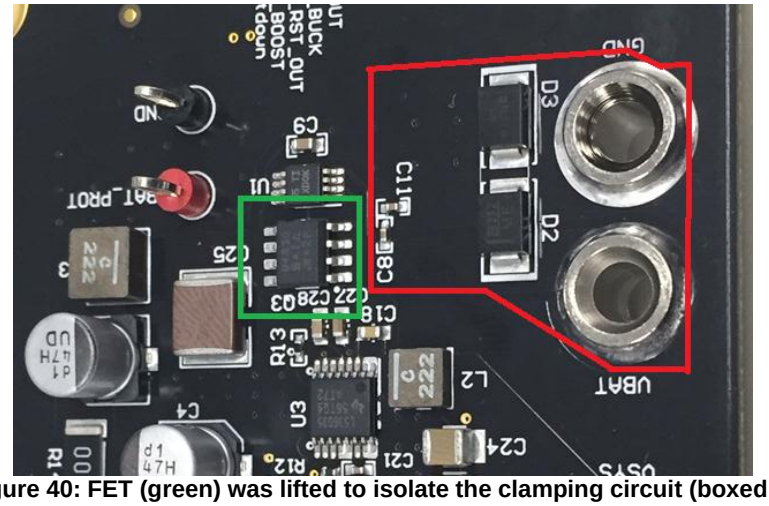


Figure 40: FET (green) was lifted to isolate the clamping circuit (boxed in red)

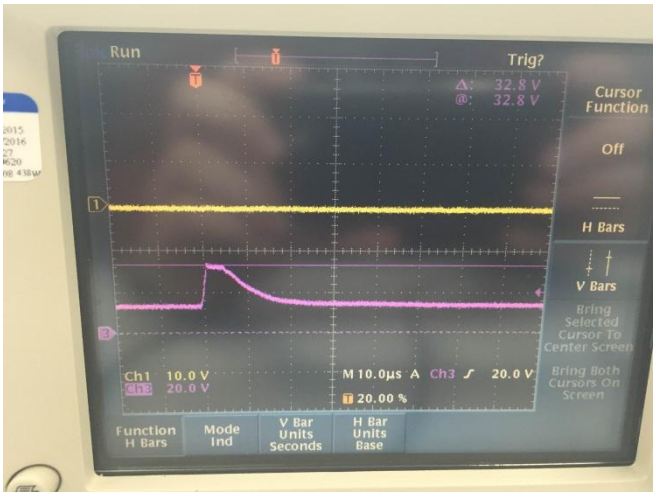
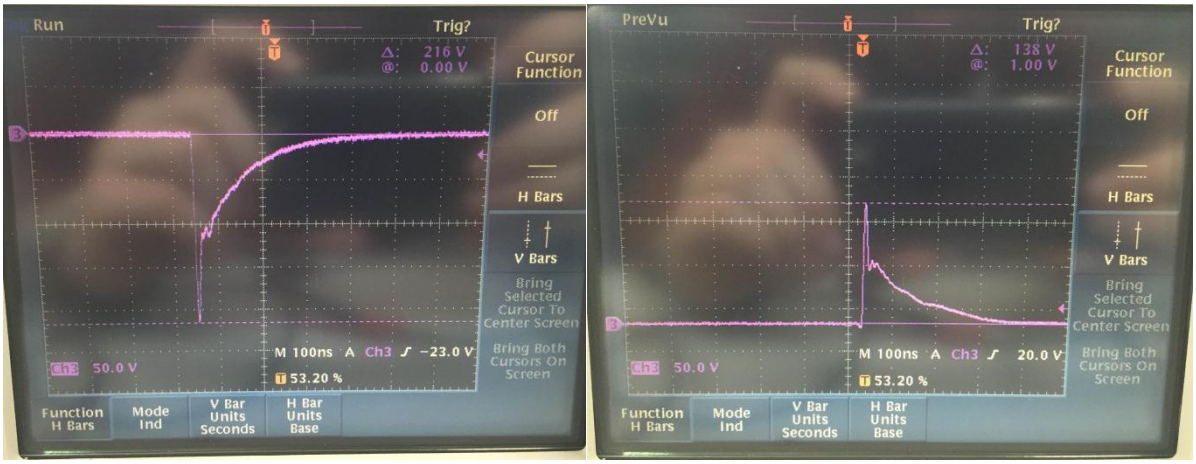


Figure 41: Input pulse is clamped to 32.8V by TVS diodes

In this configuration you can see that the clamping circuit is working correctly by limiting the pulse to 32.8V, below the maximum input voltage of the downstream devices.

8.5.3 ISO Pulse 3a/b



The pulse was first verified open-circuit. The following parameters were used for Pulse 3a:

- V_{pulse} = -150V
- R_{source} = 50Ω
- T_{rise} = 5ns
- $T_{duration}$ = 0.1µs

And for Pulse 3b:

- V_{pulse} = 100V
- R_{source} = 50Ω
- T_{rise} = 5ns
- $T_{duration}$ = 0.1µs

Pulse 3a and Pulse 3b are very fast, high voltage transients. However, they are so low-energy (high source impedance, short duration) that once connected to the input of my circuit, they are completely dampened by the input filter. Their disturbance is not even visible at the input of the boost converter stage, so no screenshots were taken as they would show nothing of value.

8.5.4 ISO Pulse 5b (clamped load dump)

Figure 42: Pulse 5b (clamped load dump) test pulse

The pulse was first verified open-circuit. The following parameters were used:

- V_{pulse} = 36V (22.5V superimposed on 13.5V DC voltage)

- R_{source} = 0.5Ω
- T_{rise} = 10ms
- $T_{duration}$ = 400ms

We then subjected our circuit to the pulse (yellow trace) and measured the disturbance to the input of the power stage (blue trace) as well as the system output (purple trace):

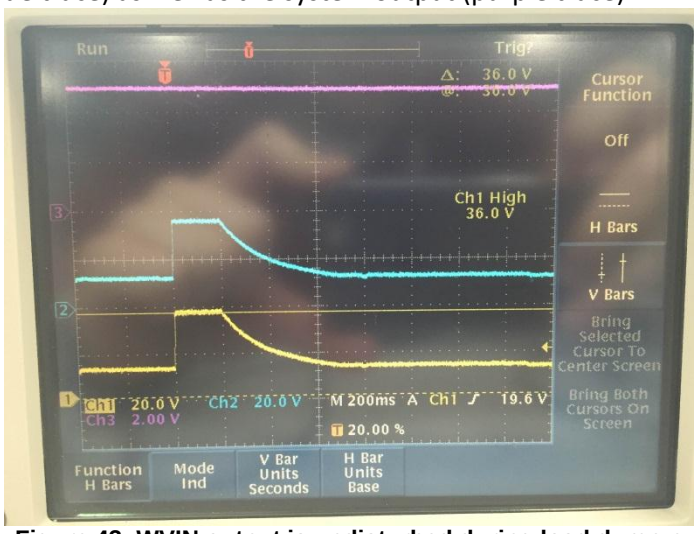


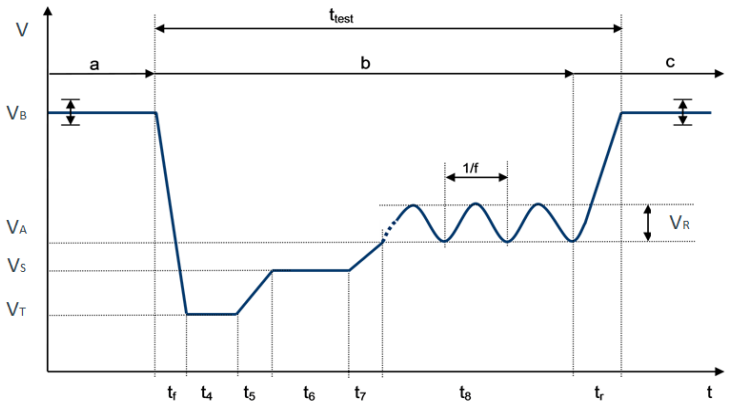
Figure 43: WVIN output is undisturbed during load dump pulse

Though the load dump pulse is quite energetic, it is slow enough that it doesn't cause any significant line transient effects on the output of the LM53603, as the control loop is quick enough to respond to the rising input voltage. The TVS protection circuit also does not need to clamp this pulse as it is low enough in magnitude not to damage downstream devices.

8.6 Cold Crank test

Testing our design for operation during a severe cold crank pulse was a large objective of this design. In fact, it is the leading reason for including a pre-boost converter in this system. In order to be effective, the pre-boost must turn on quickly as the battery voltage falls, and sustain its output at very low input voltages. It must also do this without significant under/overvoltage excursions in order to maintain a clean input for the buck converter.

Here are the parameters we used for this test (we tested only the "Severe" pulse):



Parameter	"Normal" test pulse	"Severe" test pulse
V_B	11,0 V	11,0 V
V_T	4,5 V (0%, -4%)	3,2 V $^{+0,2\,V}$
V_S	4,5 V (0%, -4%)	5,0 V (0%, -4%)
V_A	6,5 V (0%, -4%)	6,0 V (0%, -4%)
V_R	2 V	2 V
t_f	≤1 ms	≤1 ms
t_4	0 ms	19 ms
t_5	0 ms	≤1 ms
t_6	19 ms	329 ms
t_7	50 ms	50 ms
t_8	10 s	10 s
t_r	100 ms	100 ms
f	2 Hz	2 Hz

Figure 44: Test pulse parameters

After testing the waveform open-loop, we subjected our board to the test pulse (yellow) and measured the boost output/buck input (purple) as well as the system output (blue):

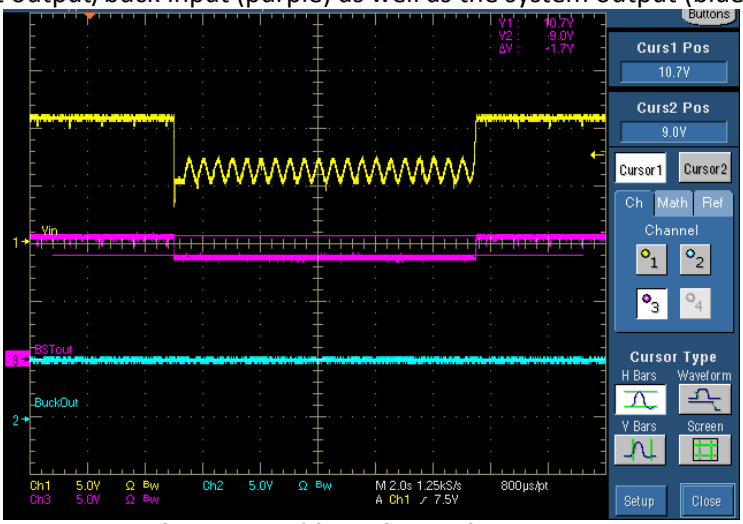


Figure 45: Cold Crank tested on our system

The boost responded quickly once its input dropped below the OV threshold and turned on to sustain a 9V output, allowing the buck converter to operate seamlessly without any disturbance to the output. Once the battery voltage recovered, the boost turns off and normal operation continues.

Below we can see a zoomed in version of the beginning of the waveform:

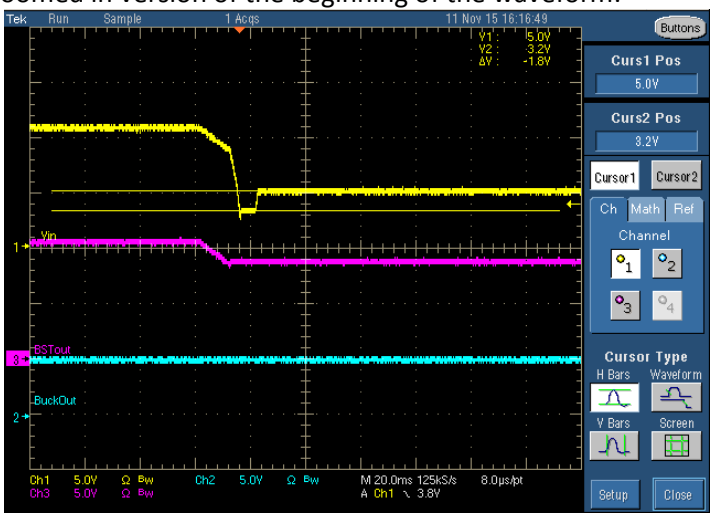


Figure 46: Cold Crank - lowest voltage dip

The lowest voltage the boost sees is 3.2V at the battery input. As this is our lowest specified input for the system, it is good to see that the boost is able to maintain 9V out through this low dip. It is also important that the boost turns on very quickly as the input voltage falls:

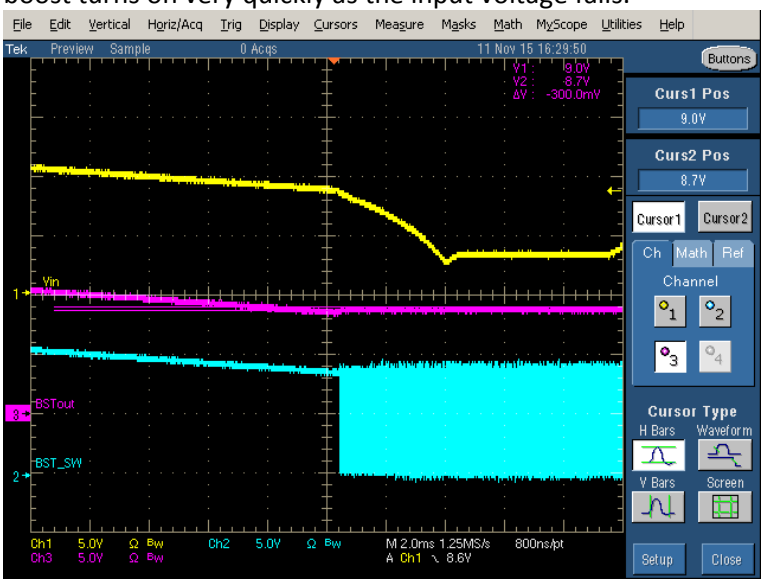


Figure 47: Cold Crank - boost turn-on (switch node in blue)

The figure above shows the device starts switching (blue) when the input (yellow) falls just below 9V. The boost output falls only 300mV below its target output voltage before recovering.

8.7 CISPR25 Emissions Testing

CISPR25 EMI testing was done at a 3rd party facility with compliant ALSE chambers used for emissions testing. Both Conducted and Radiated emissions tests were done. Background on the standard and the test setup are given earlier in this document. When looking at the results, the blue lines are Class 5 limits for Average emissions, and the red lines are the Peak emission limits. A table of measurements is available upon request, but this report only shows the graphs.

8.7.1 Conducted Emissions

The conducted emissions setup is shown below (power cable not attached). The LISNs are the gray boxes on the left side, the car battery is behind them, and the DUT is sitting on the insulating material on the right. To test at 4.5V, a variable voltage supply was fed in through the bulkhead from outside of the chamber.

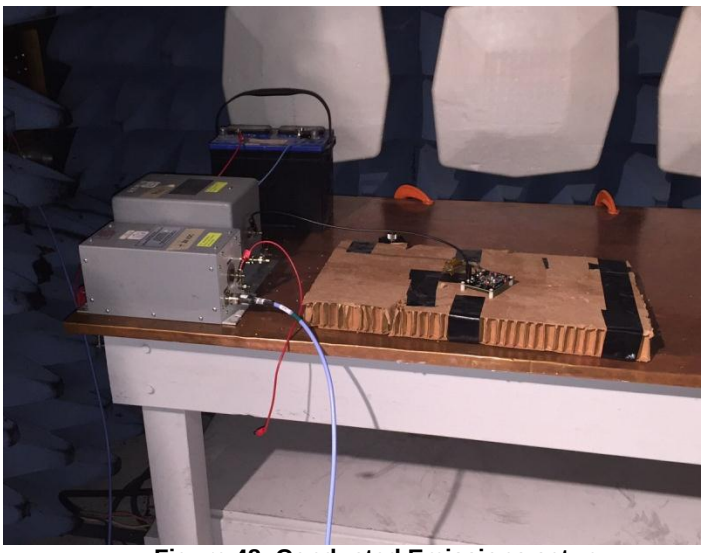


Figure 48: Conducted Emissions setup

The results are taken on both the Return (ground) and Line (hot) side through their respective LISN. We tested at 12V (with the actual car battery) as well as 4.5V (so that the pre-boost is actually turned on). A 1A load was connected during operation. Before testing we measured the noise floor by doing an ambient measurement with the DUT disconnected. The measurement technique changes above 30MHz, hence the raise in the noise floor:

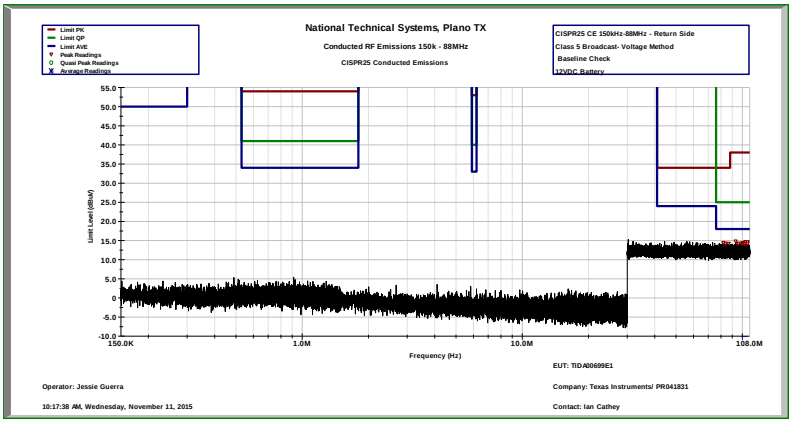


Figure 49: Ambient noise level - Return Side

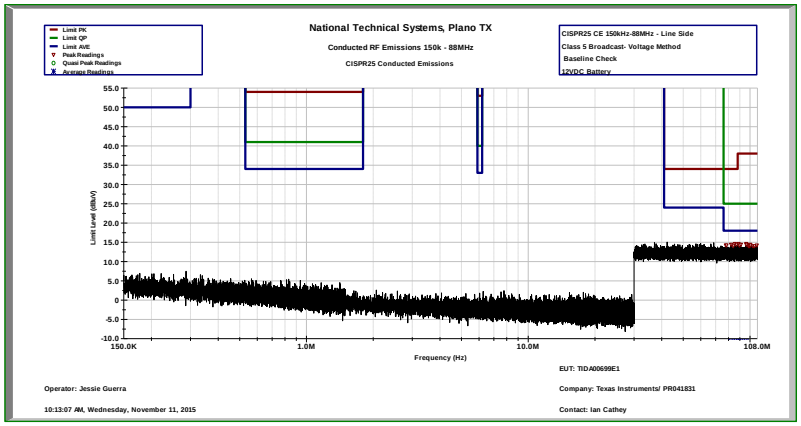


Figure 50: Ambient noise level - Line side

The rest of the results are given below at each VIN from both the line and return side:

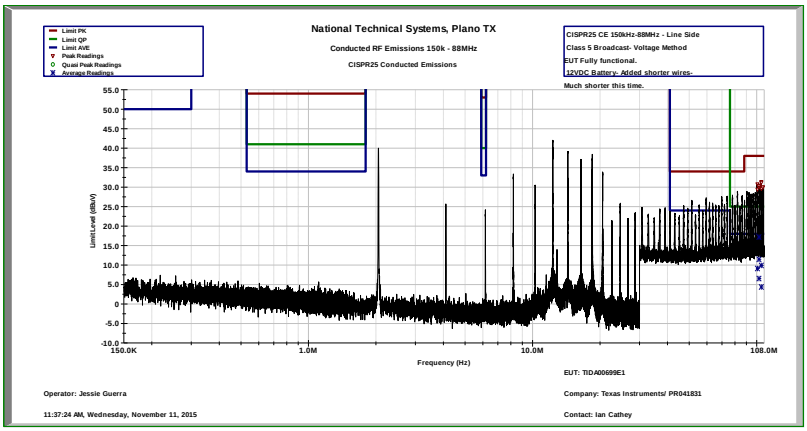


Figure 51: VIN = 12V, Line Side

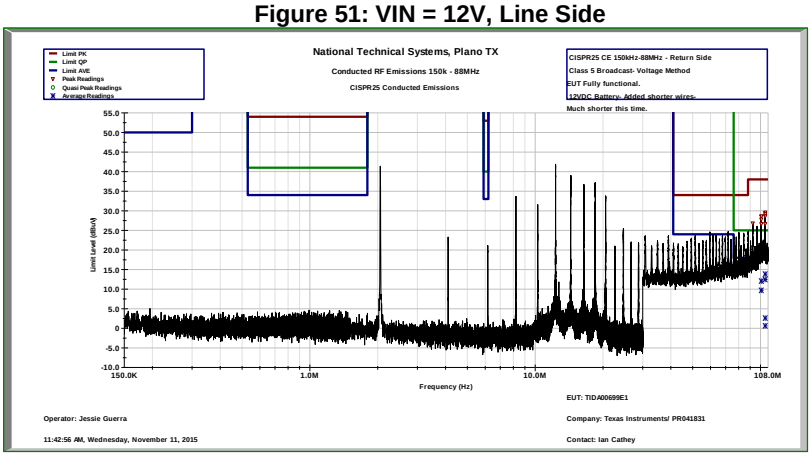


Figure 52: VIN = 12V, Return side

At 12V, both the line and return side results Peak and Average results are below the Class 5 limits for CISPR25 Conducted Emissions. You can clearly see a large peak at the nominal switching frequency of the buck converter (2.1MHz) and smaller peaks at its 3rd and 5th harmonics.

We need to lower the operating voltage to 4.5V in order to let the boost activate so we can see its effects on the spectrum:

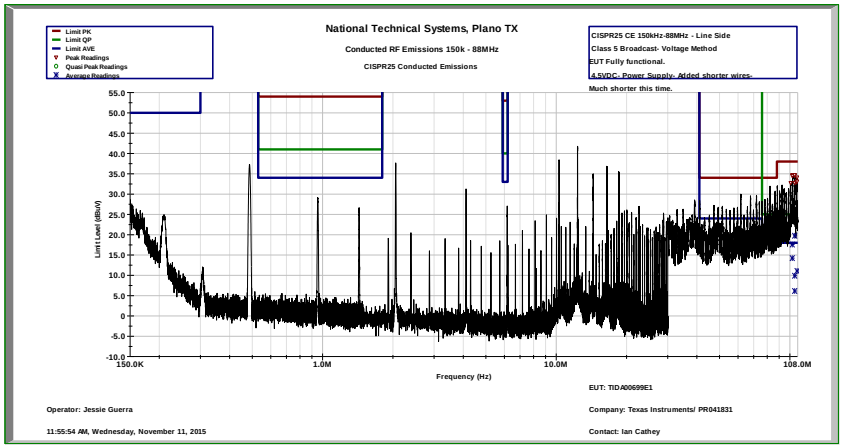


Figure 53: VIN = 4.5V, Line Side

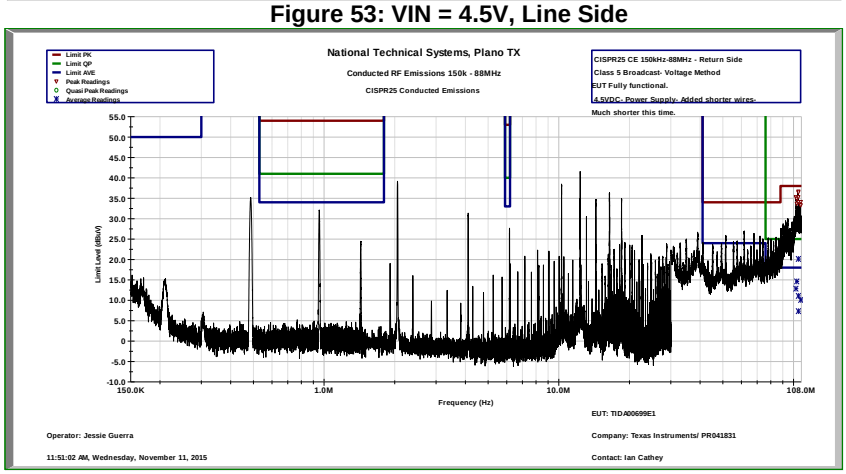


Figure 54: VIN = 4.5V, Return Side

At this voltage level, the switching frequency of the boost and its harmonics can be seen. However, for some reason there was also an increase in the spectrum around the top end of the measurement. This seems to be caused by variations in the test setup. Nonetheless, there is a single frequency (104.89MHz) where the average result is slightly above the Class 5 limits, and therefore **both the line and return sides only satisfy CISPR25 Class 4 operation** (limits not shown on graph).

That is a bit disappointing, but with some work on cleaning up the test setup, it would probably be possible to eliminate that peak, as there are no switching frequencies generated on our board even close to that level. It was shown during testing that the orientation of the board and the power cable lengths (within the tolerance of the specification) was a major contributor to these peaks. Using proper shielded or twisted pair cables could be sufficient to avoid these peaks.

8.7.2 Radiated Emissions

The conducted emissions setup is shown below. The LISNs are the gray boxes on the left side, the car battery is behind them, and the DUT is sitting on the insulating material on the right. To test at 4.5V, a variable voltage supply was fed in through the bulkhead from outside of the chamber. Unlike conducted emissions, the measurements must be broken down into different sections, each being tested with a different type of antenna appropriate for that band. Due to the limitations of the testing facility, we were only able to test up to 1GHz (could not achieve low enough noise floor above this).

There is some ambiguity in the CISPR25 spec as to whether the DUT should be grounded to the test ground plane. It should only be connected if it would be so in the car. Since our design is not a complete “module”, and it somewhat generic, we have the option to do this. Often this will improve results by several dBuV.

Here is an image of the test setup for Radiated Emissions, in this example with a monopole antenna used to test the lower frequencies:

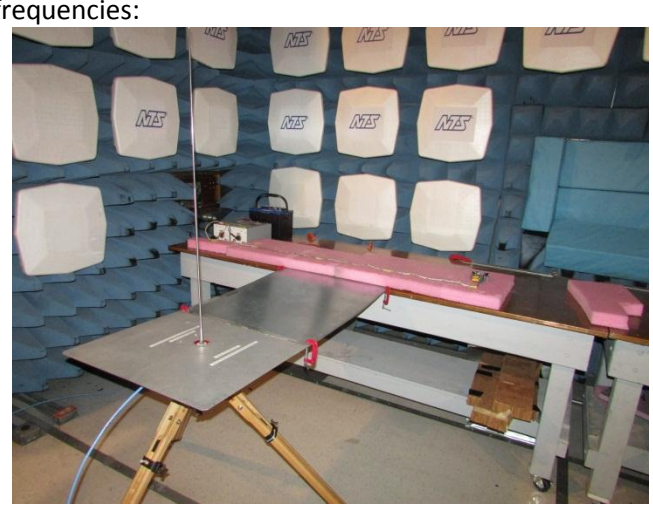


Figure 55: Radiated emissions setup with monopole antenna

Below are the results when testing at 12V (pre-boost converter not active):

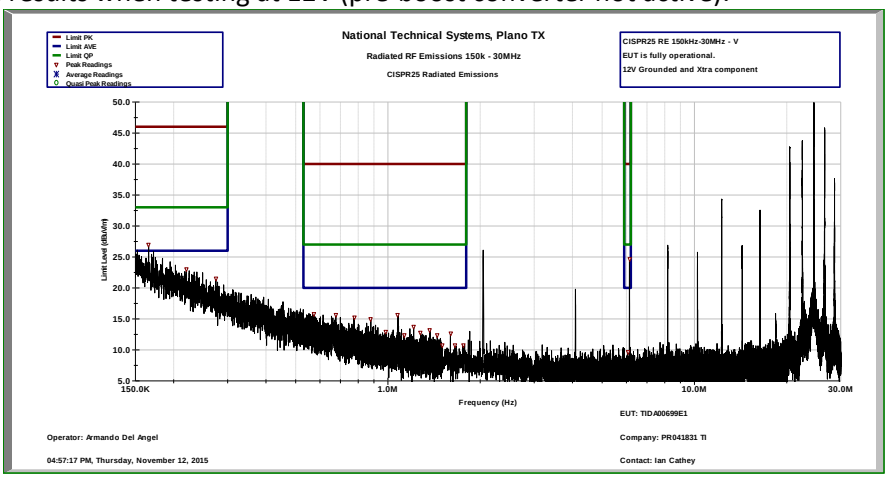


Figure 56: VIN = 12V, testing 150kHz - 30MHz

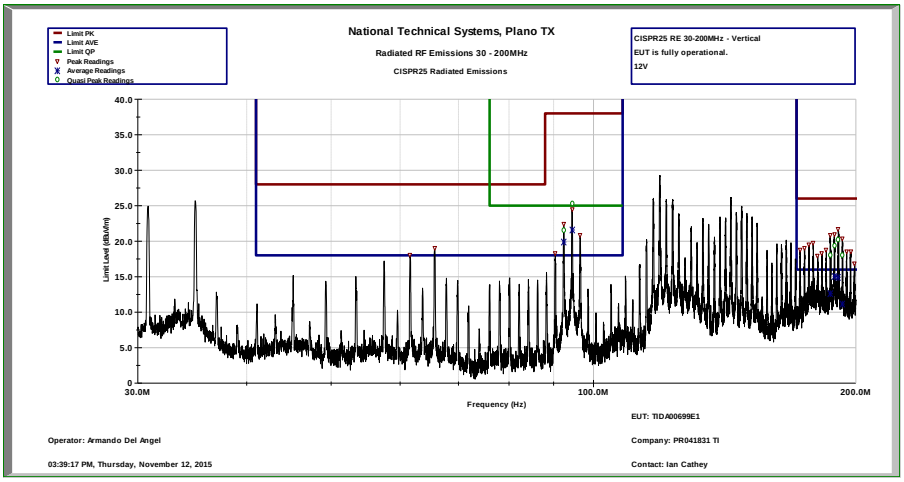


Figure 57: VIN = 12V, testing 30 – 200MHz, Antenna Vertically Oriented

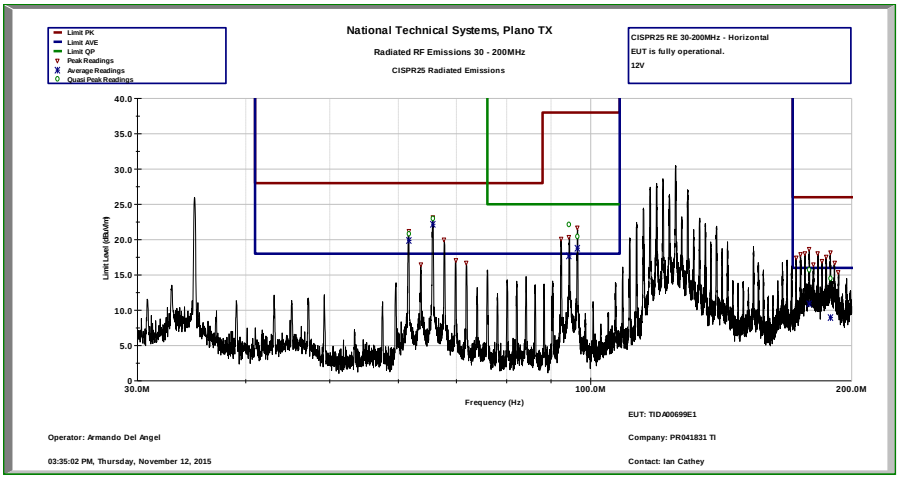


Figure 58: VIN = 12V, testing 30 – 200MHz, Antenna Horizontally Oriented

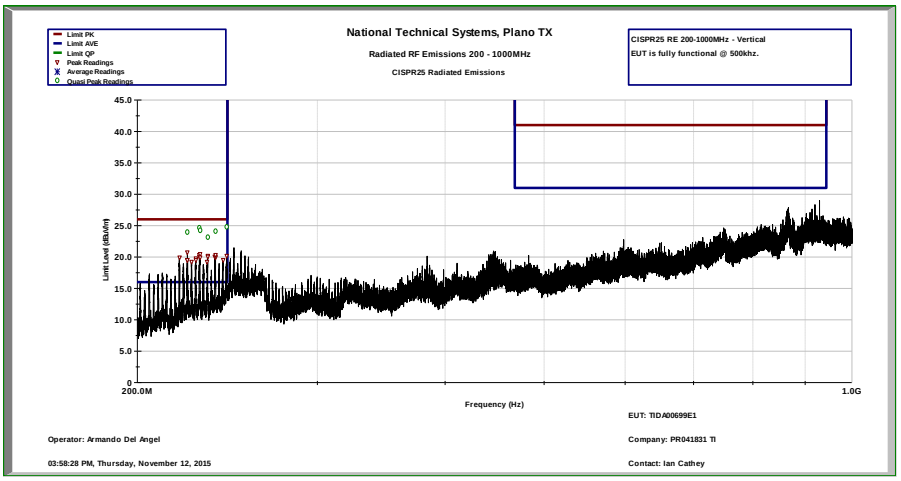


Figure 59: VIN = 12V, testing 200MHz - 1GHz, Antenna Vertically Oriented

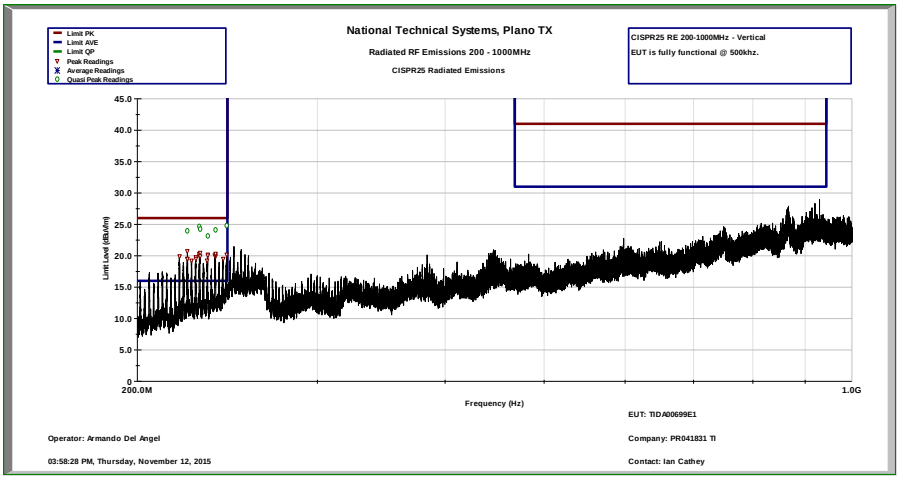


Figure 60: VIN = 12V, testing 200MHz - 1GHz, Antenna Horizontally Oriented

Based on the above results, **for 12V operation the peak and average results are CISPR25 Class 4 compliant**. There are only a few average peaks in the 30-200MHz band that are not below the Class 5 limits. With an enclosure/shielding, this could possibly be brought down into compliance.

Below are the results when testing at 4.5V (pre-boost active):

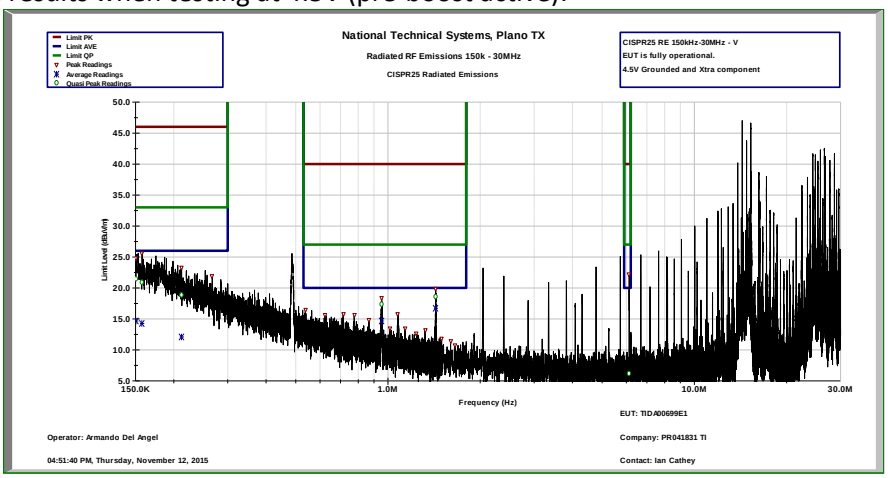


Figure 61: VIN = 4.5V, testing 150kHz - 30MHz

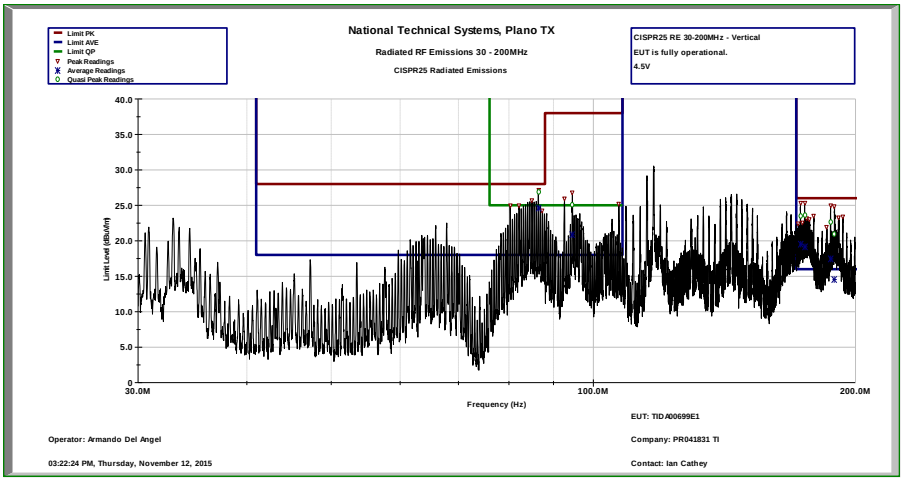


Figure 62: VIN = 4.5V, testing 30 – 200MHz, Antenna Vertically Oriented

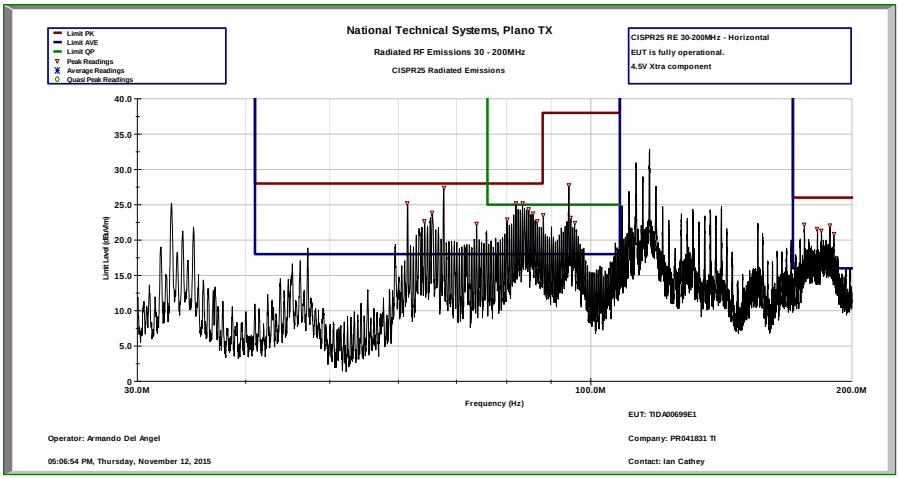


Figure 63: VIN = 4.5V, testing 30 – 200MHz, Antenna Horizontally Oriented

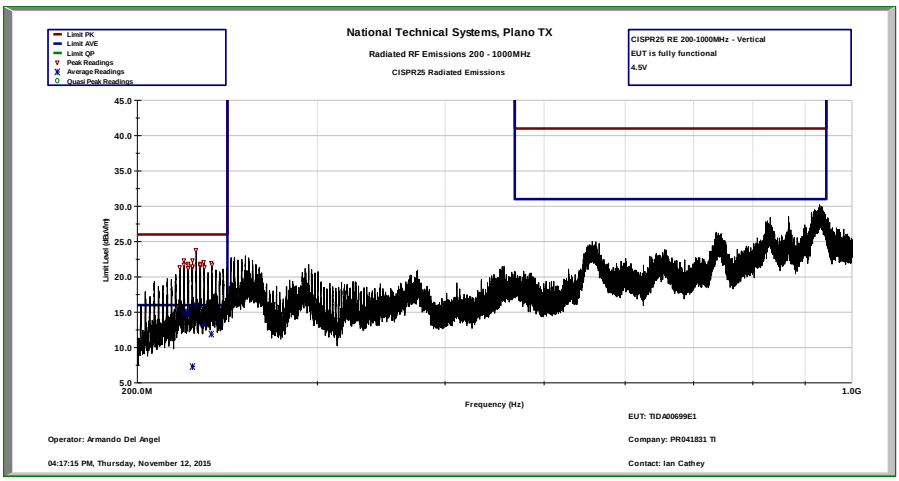


Figure 64: VIN = 4.5V, testing 200MHz - 1GHz, Antenna Vertically Oriented

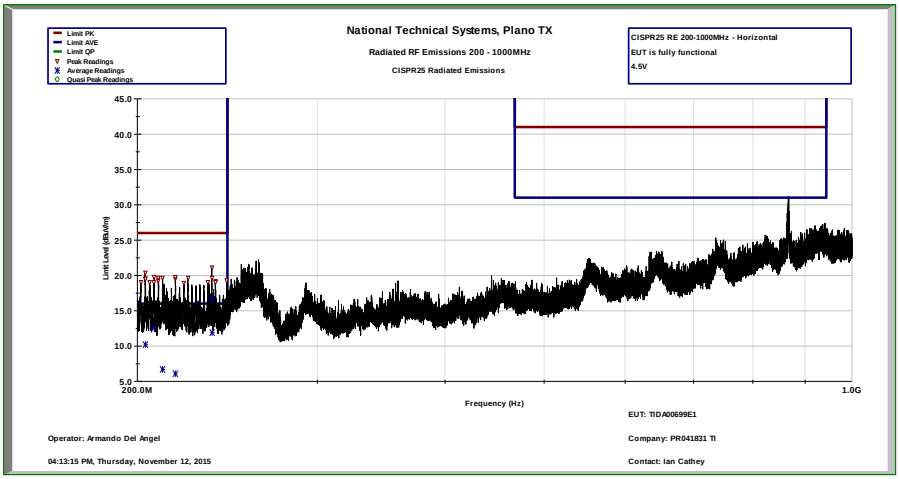


Figure 65: VIN = 4.5V, testing 200MHz - 1GHz, Antenna Horizontally Oriented

Based on the above results, **for 4.5V operation the peak and average results are CISPR25 Class 3 compliant**. There are only a few average peaks in the 30-200MHz band that are not below the Class 4 limits. With an enclosure/shielding, this could possibly be brought down into compliance. Testing with

the board grounded to the test ground plane (which would be within the spec) would also likely improve results across all frequency ranges.

8.7.3 Summary of Results

Below is a table summarizing the results of both the Conducted and Radiated portions of the test across different operating points and test conditions:

		12V	4.5V
Conducted Emissions			
150kHz - 108MHz	Peak	Class 5	Class 5
	Average	Class 5	Class 4
Radiated Emissions			
150kHz - 30MHz	Peak	Class 5	Class 5
	Average	Class 5	Class 5
30MHz - 200MHz Horiz.	Peak	Class 5	Class 5
	Average	Class 4	Class 3
30MHz - 200MHz Vert.	Peak	Class 5	Class 5
	Average	Class 4	Class 3
200MHz - 1GHz Horiz.	Peak	Class 5	Class 5
	Average	Class 5	Class 4
200MHz - 1GHz Vert.	Peak	Class 5	Class 5
	Average	Class 5	Class 4

9 Design Files

9.1 Schematics

To download the Schematics for each board, see the design files at http://www.ti.com/tool/tida-00699

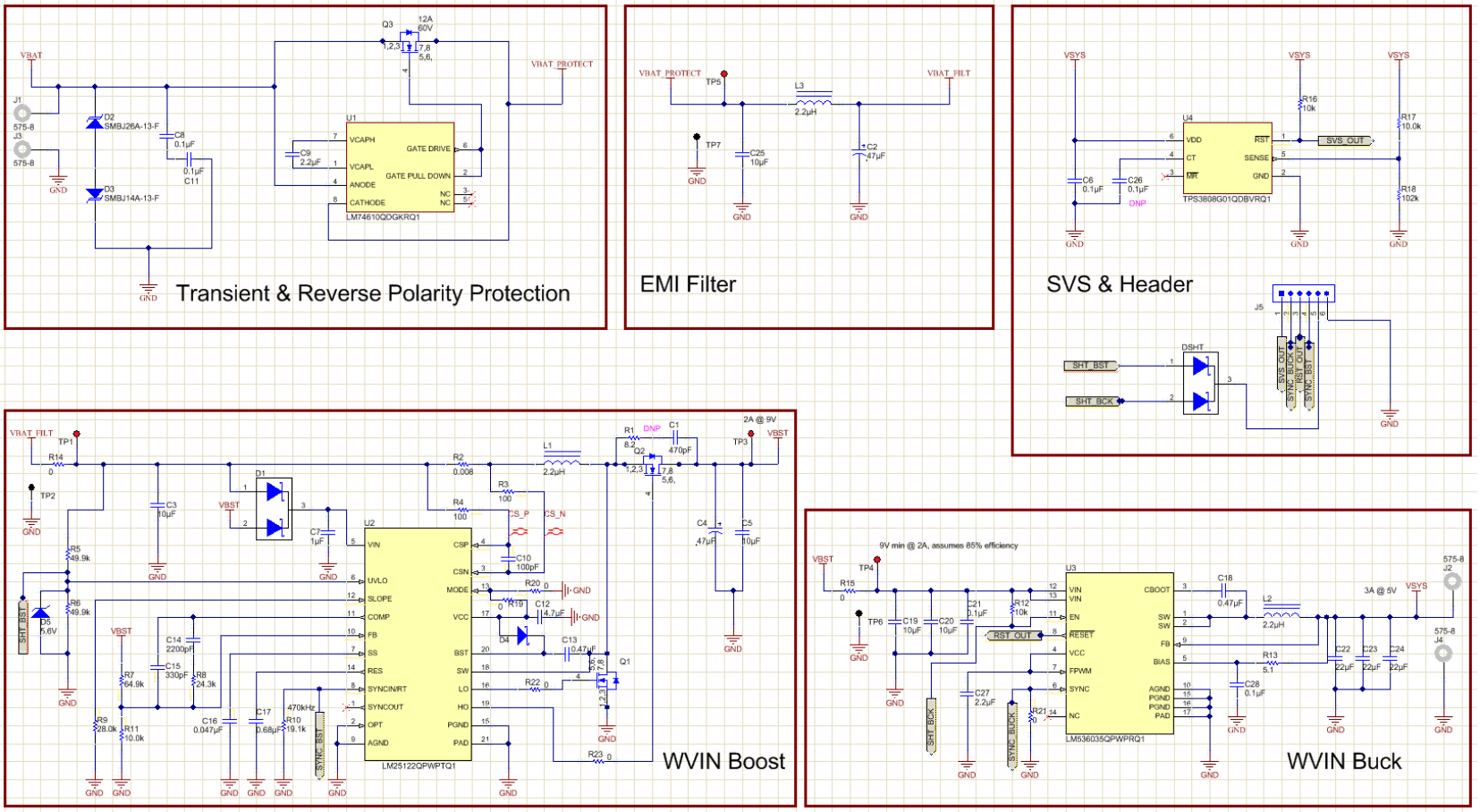


Figure 66: Battery Front End and Sequencing/Supervision Schematics

9.2 Bill of Materials

To download the Bill of Materials for each board, see the design files at http://www.ti.com/tool/tida-00699

Table 1: TIDA-00699 BOM

Designator	Value	PartNumber	Description	Footprint	Quantity
C1	470pF	C1005X7R1H471K	CAP, CERM, 470 pF, 50 V, +/- 10%, X7R, 0402	0402	1
C2, C4	47uF	EEE-FK1H470XP	CAP, AL, 47uF, 50V, +/-20%, 0.68 ohm, SMD	SM_RADIAL_D8	2
C3, C5, C19, C20, C25	10uF	CGA9N3X7R1H106K230KB	CAP, CERM, 10 µF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 2220	2220	5
C6, C26, C28	0.1uF	GCM188R71C104KA37J	CAP, CERM, 0.1 µF, 16 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603_095	3
C7	1uF	GCM31CR72A105KA03	CAP, CERM, 1 µF, 100 V, +/- 10%, X7R, AEC-Q200 Grade 1, 1206_190	1206_190	1
C8, C11, C21	0.1uF	CGA2B3X7R1H104M050BB	CAP, CERM, 0.1 µF, 50 V, +/- 20%, X7R, AEC-Q200 Grade 1, 0402	0402	3
C9	2.2uF	GRM188R71A225KE15D	CAP, CERM, 2.2 µF, 10 V, +/- 10%, X7R, 0603	0603	1
C10	100pF	C0402C101J3GACTU	CAP, CERM, 100 pF, 25 V, +/- 5%, C0G/NP0, 0402	0402	1
C12	4.7uF	GRM21BR71A475KA73L	CAP, CERM, 4.7 µF, 10 V, +/- 10%, X7R, 0805	0805_HV	1
C13	0.47uF	UMK212B7474KG-T	CAP, CERM, 0.47 µF, 50 V, +/- 10%, X7R, 0805	0805_HV	1
C14	2200pF	885012205027	CAP, CERM, 2200 pF, 16 V, +/- 10%, X7R, 0402	0402	1
C15	330pF	C1005C0G1H331J	CAP, CERM, 330 pF, 50 V, +/- 5%, C0G/NP0, 0402	0402	1
C16	0.047uF	06033C473JAT2A	CAP, CERM, 0.047 µF, 25 V, +/- 5%, X7R, 0603	0603	1
C17	0.68uF	0805ZC684KAT2A	CAP, CERM, 0.68 µF, 10 V, +/- 10%, X7R, 0805	0805_HV	1
C18	0.47uF	CGA3E3X7R1E474K080AB	CAP, CERM, 0.47 µF, 25 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603_095	1
C22, C23, C24	22uF	CGA6P1X7R1C226M250AC	CAP, CERM, 22 µF, 16 V, +/- 20%, X7R, AEC-Q200 Grade 1, 1210	1210_280	3
C27	2.2uF	GCM188R70J225KE22D	CAP, CERM, 2.2 µF, 6.3 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0603	0603_095	1
D1, DSHT	40V	BAS40-05-7-F	Diode, Schottky, 40 V, 0.2 A, SOT-23	SOT-23	2
D2	26V	SMBJ26A-13-F	Diode, TVS, Uni, 26 V, 600 W, SMB	SMB	1
D3	14V	SMBJ14A-13-F	Diode, TVS, Uni, 14 V, 600 W, SMB	SMB	1
D4	60V	PMEG6010CEH,115	Diode, Schottky, 60 V, 1 A, SOD-123F	SOD-123F	1
D5	5.6V	MMSZ5232B-7-F	Diode, Zener, 5.6 V, 500 mW, SOD-123	SOD-123	1

H5, H6, H7, H8		1902C	Standoff, Hex, 0.5"L #4-40 Nylon	Keystone_1902C	4
J1, J2, J3, J4		575-8	Standard Banana Jack, Uninsulated, 8.9mm	Keystone575-8	4
J5		GRPB061VWCN-RC	Header, 50mil, 6x1, Gold, R/A, TH	Sullins_GRPB061VWCN	1
L1, L3	2.2uH	XAL5030-222MEB	Inductor, Shielded, Composite, 2.2 µH, 9.2 A, 0.01 ohm, SMD	XAL5030	2
L2	2.2uH	XAL4020-222MEB	Inductor, Shielded, Composite, 2.2 µH, 5.5 A, 0.04 ohm, SMD	XAL4020	1
Q1, Q2	60V	CSD18531Q5A	MOSFET, N-CH, 60V, 19A, SON 5x6mm	TRANS_NexFET_Q5A	2
Q3	60V	SQ4850EY	MOSFET, N-CH, 60 V, 12 A, SO-8	SO-8	1
R1	8.2	CRCW04028R20JNED	RES, 8.2, 5%, 0.063 W, 0402	0402	1
R2	0.008	WSL20108L000FEA18	RES, 0.008, 1%, 1 W, 2010	2010	1
R3, R4	100	CRCW0402100RJNED	RES, 100, 5%, 0.063 W, 0402	0402	2
R5, R6	49.9k	CRCW040249K9FKED	RES, 49.9 k, 1%, 0.063 W, 0402	0402	2
R7	64.9k	CRCW040264K9FKED	RES, 64.9 k, 1%, 0.063 W, 0402	0402	1
R8	24.3k	CRCW040224K3FKED	RES, 24.3 k, 1%, 0.063 W, 0402	0402	1
R9	28.0k	CRCW040228K0FKED	RES, 28.0 k, 1%, 0.063 W, 0402	0402	1
R10	19.1k	CRCW040219K1FKED	RES, 19.1 k, 1%, 0.063 W, 0402	0402	1
R11, R17	10.0k	CRCW040210K0FKED	RES, 10.0 k, 1%, 0.063 W, 0402	0402	2
R12, R16	10k	CRCW040210K0JNED	RES, 10 k, 5%, 0.063 W, 0402	0402S	2
R13	5.1	CRCW04025R10JNED	RES, 5.1, 5%, 0.063 W, 0402	0402	1
R14	0	CRCW25120000Z0EG	RES, 0, 5%, 1 W, 2512	2512	1
R15	0	CRCW12060000Z0EA	RES, 0, 5%, 0.25 W, 1206	1206	1
R18	102k	CRCW0402102KFKED	RES, 102 k, 1%, 0.063 W, 0402	0402	1
R19, R20, R21	0	CRCW04020000Z0ED	RES, 0, 5%, 0.063 W, 0402	0402L	3
TP1, TP3, TP4, TP5	Red	5010	Test Point, Multipurpose, Red, TH	Keystone5010	4
TP2, TP6, TP7	Black	5011	Test Point, Multipurpose, Black, TH	Keystone5011	3
U1		LM74610QDGKRQ1	Smart Diode Controller, DGK0008A	DGK0008A_N	1
U2		LM25122QPWPTQ1	Wide-Input Synchronous Boost Controller With Multiple Phase Capability, PWP0020A	PWP0020A_N	1
U3		LM536035QPWPRQ1	5V, 3A, Buck Regulator For Automotive Applications, PWP0016H	PWP0016H_N	1
U4		TPS3808G01QDBVRQ1	LOW-QUIESCENT-CURRENT PROGRAMMABLE-DELAY SUPERVISORY CIRCUIT, DBV0006A	DBV0006A_N	1

9.3 PCB Layout Recommendations

9.3.1 Noise Sensitive Traces and Components

- Route voltage feedback (FB) traces away from other noisy traces or components, like I2C clock lines. Avoid routing things under the switch node of a power inductor altogether if possible:

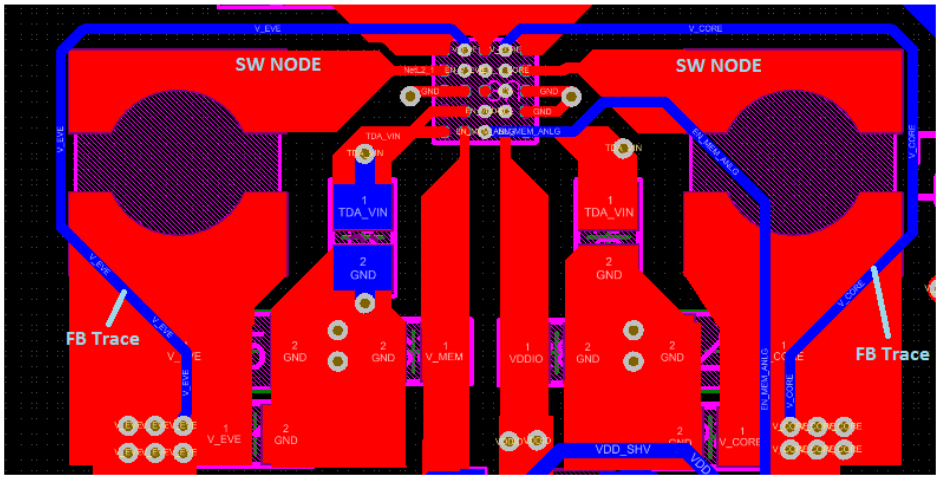


Figure 67: Routing FB traces around SW nodes

FB nodes are high impedance lines which are quite sensitive to disturbances. The switch node can radiate a significant amount of energy and could couple noise into FB traces or other sensitive lines. Placing these traces on the other side of the board (with ground planes between them) helps mitigate ill effects as well.

- It is critical that analog/control loop components be placed such that their trace lengths back to the IC are minimized. Below is an example of the Feedback and Compensation components for the boost converter:

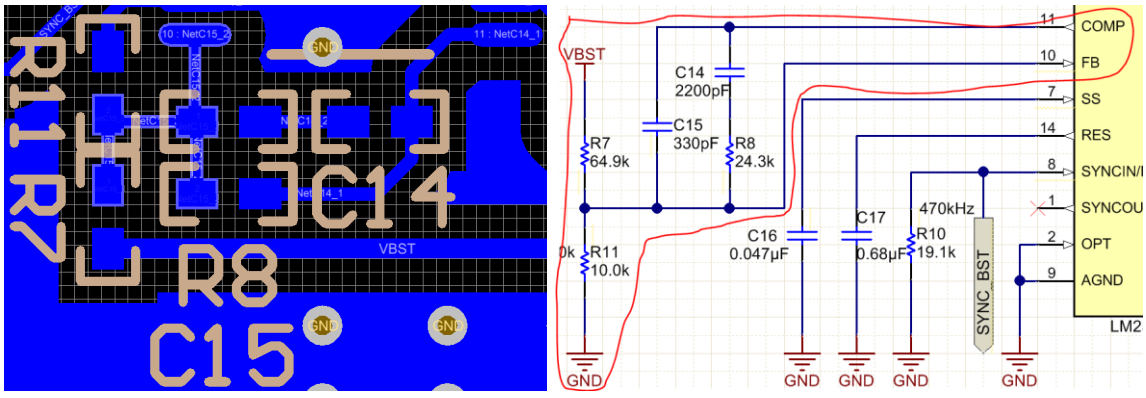


Figure 68: Compensation/Feedback components placed close to IC

The FB and COMP nodes are especially high impedance and thus susceptible to picking up noise. As these are critical in the operation of the devices control loop, poor placement and routing of these components/traces can affect the performance of the device by introducing unwanted parasitic inductances and capacitances.

- The boost converter is a controller (external FET) and therefore gate drive signals must be routed between the IC and the FETs. These nodes switch very quickly and therefore the distance (and therefore inductance) they travel should be minimized. An important part of this is to use the minimum amount of vias as possible. In our case, since the controller is on the bottom layer, one via is required:

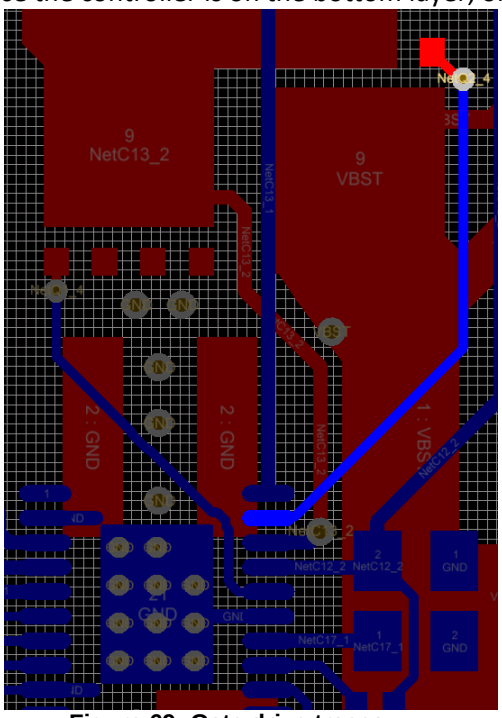
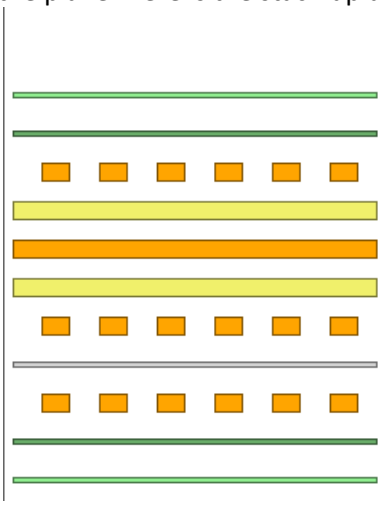


Figure 69: Gate drive traces

9.3.2 PCB Layering recommendations

- If using a 4 layer board, layer 2 should be a ground plane. Since most of the components/switching currents are on the top layer, this reduces the inductive effect of the vias when currents are returned through the plane. Here is the stack-up used in this board:



Layer Name	Type	Material	Thickness (mil)
Top Overlay	Overlay		
Top Solder	Solder Mask/...	Surface Mat...	0.4
Top Layer	Signal	Copper	1.4
Dielectric1	Dielectric	Core	59.2
Internal Plan...	Internal Plane	Copper	1.417
Dielectric 2	Dielectric	Core	10
Signal Layer 1	Signal	Copper	1.417
Dielectric 3	Dielectric	Prepreg	5
Bottom Layer	Signal	Copper	1.4
Bottom Solder	Solder Mask/...	Surface Mat...	0.4
Bottom Over...	Overlay		

Figure 70: Layer stack up

9.3.3 General Power Supply Considerations

- Input capacitors should be placed as close to the IC as possible to reduce the parasitic series inductance from the capacitor to the device it is supplying. This is especially important for DCDC converters as the inductance from the capacitor to the high-side switching FET can cause high voltage spikes and ringing on the switch node, which can be damaging to components and cause problems for EMI.
- Place the **input** capacitors in order of descending size/value, with the smallest being closest to the device input pin. Contrastingly, place the **output** capacitors in order of descending size/value, with the largest being closest to the device's output pins/power inductor.

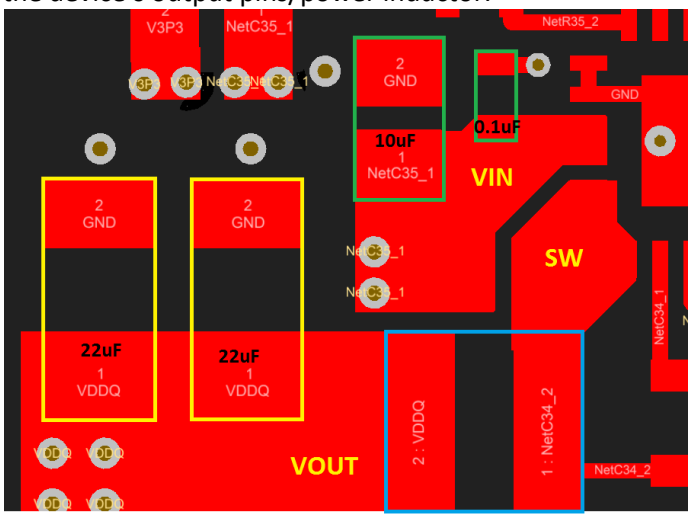


Figure 71: Input/output Capacitor placement in DCDC Converter (Green = C_{IN}, Blue = L, Yellow = C_{OUT})

- Use wide copper areas/traces for routing outputs of the converters to the connectors or loads. This reduces the I*R drop along the power path and thus improves load regulation:

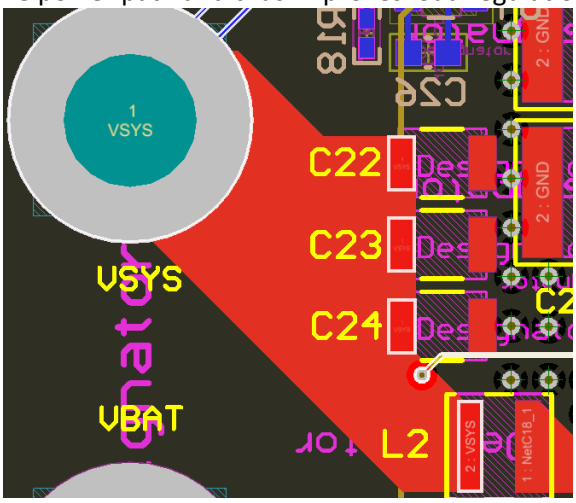


Figure 72: Wide traces for power path

The resistivity of a trace drops as the width of the trace increases$\left(R \propto \frac{1}{W}\right)$. If not using DCDC/linear converters capable of differential remote sensing, care must be taken that the voltage drop from the location of regulation (close to the converter) to the load is not significant. While there isn't really a maximum limit on this, there is a minimum. PCB traces, like wires, are rated for current ranges based on

their cross-sectional area. This depends not only on the width but also on the thickness/height of the trace. Calculators are available online for calculating minimum trace width.

- Minimize the loop area and series path inductance of the switching return current in a DCDC converter. It is preferable that this be on the same layer and can be achieved by careful placement of the components, as can be seen below with the grounds of the input and output capacitors very close to each other:

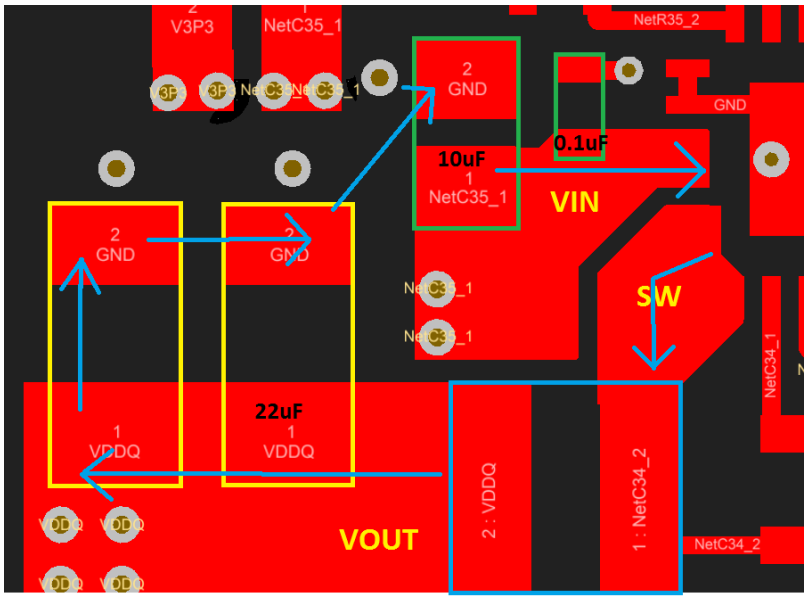


Figure 73: Current loop shown in light blue.

- The power inductors should be close to the switch node pins of the ICs, minimizing the distance from the pin to the inductor, but maintaining large area as much as possible. The goal is to minimize both the parasitic inductance, as well as reduce the radiated emissions from the node:

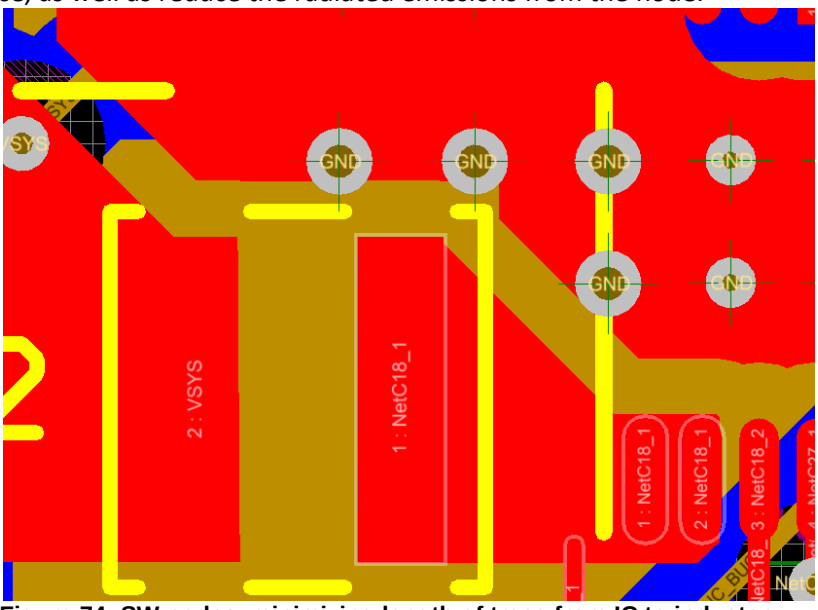


Figure 74: SW nodes, minimizing length of trace from IC to inductor

- If a bootstrap capacitor is used, place this close to the power inductor

9.3.4 Protection Circuitry

- Place TVS diodes (D2 & D3) as close to the battery terminal inputs as possible, rather than close to the downstream circuit it is protecting, to reduce the inductance of the path and allow it to react to a transient quickly.
- Place the reverse polarity protection close to the downstream circuitry. In the event that the protection FET (Q3) shuts off quickly, the inductance of the traces between the FET and the downstream circuitry could cause a large voltage transient due to the sudden interruption of current flow. Reducing the path/loop area of this section of the circuit will mitigate this as much as possible.
- Capacitor C9 should be placed as close as possible to the LM74610
- The LM74610 gate charge/discharge trace to the FET should be as short as possible
- Capacitors C8 & C11 should be placed at a right angle to each other

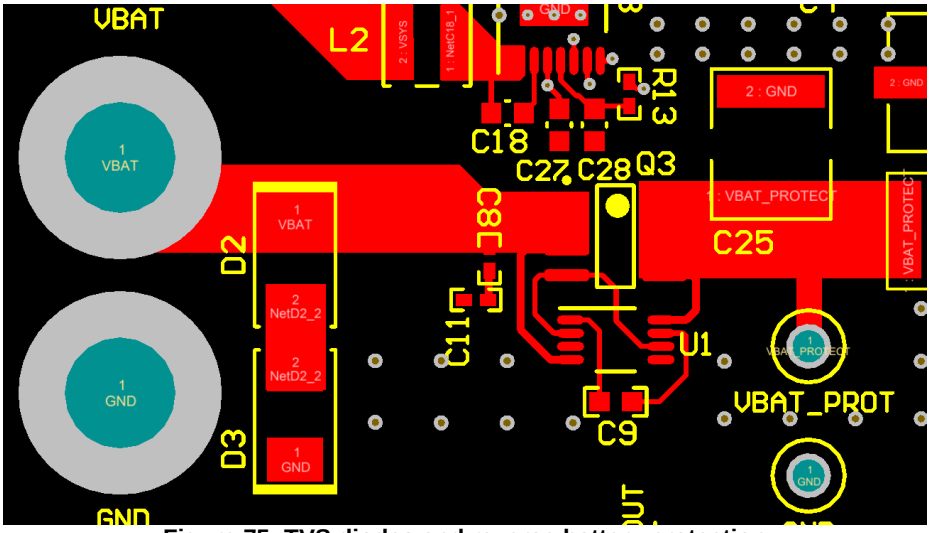


Figure 75: TVS diodes and reverse battery protection

9.3.5 Layout Prints

To download the Layout Prints for each board, see the design files at http://www.ti.com/tool/tida-00699

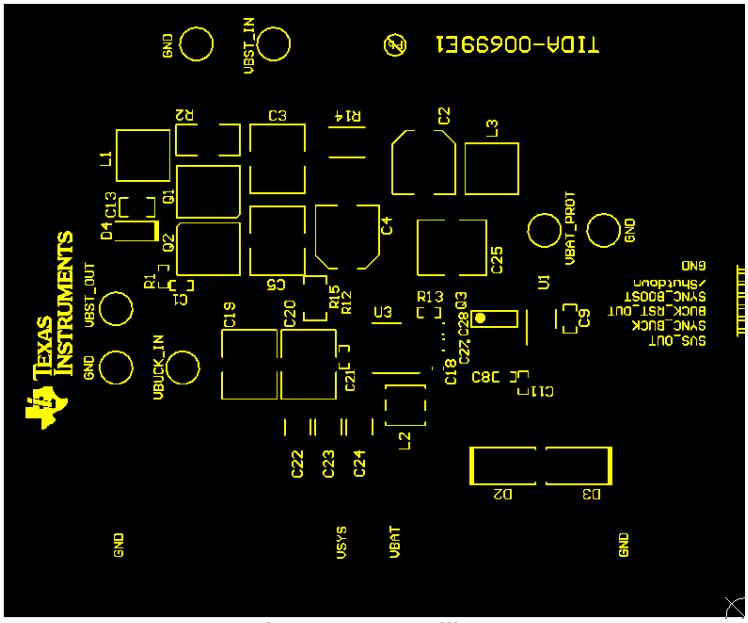


Figure 76: Top Silkscreen

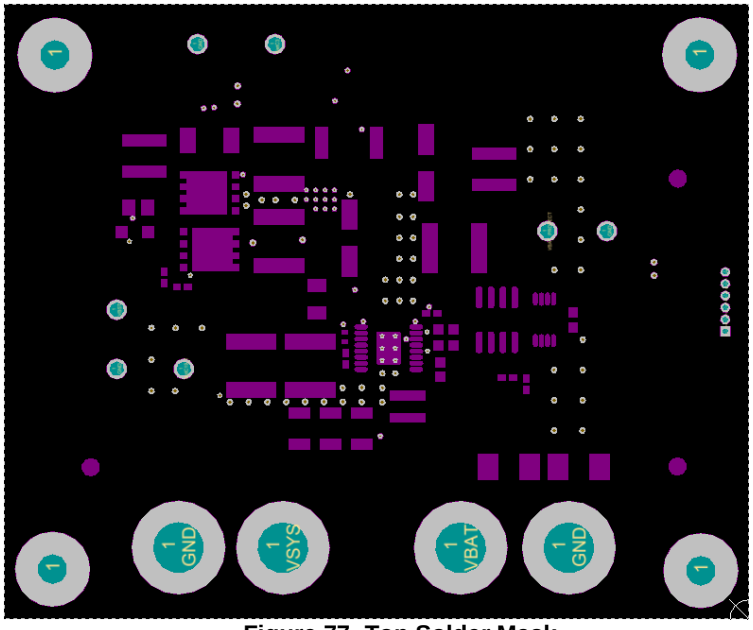


Figure 77: Top Solder Mask

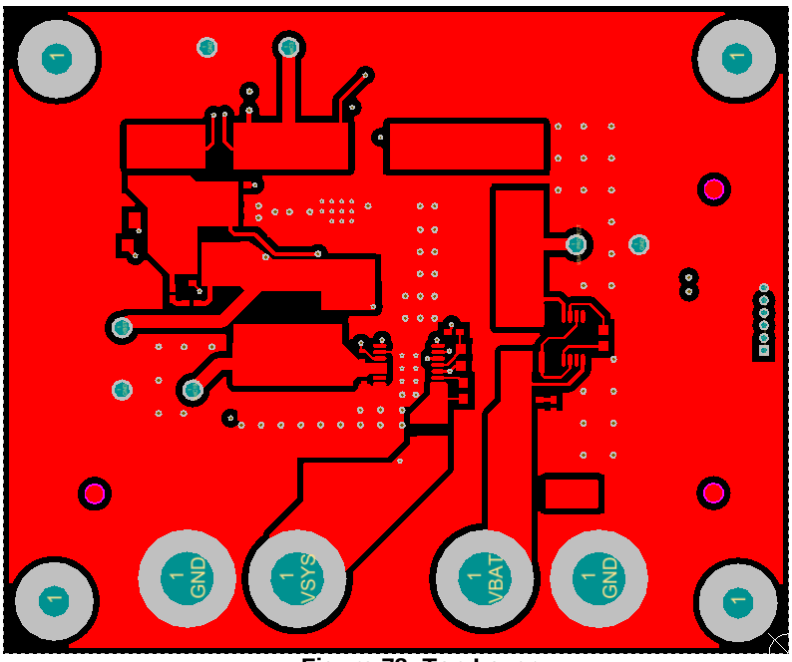


Figure 78: Top Layer

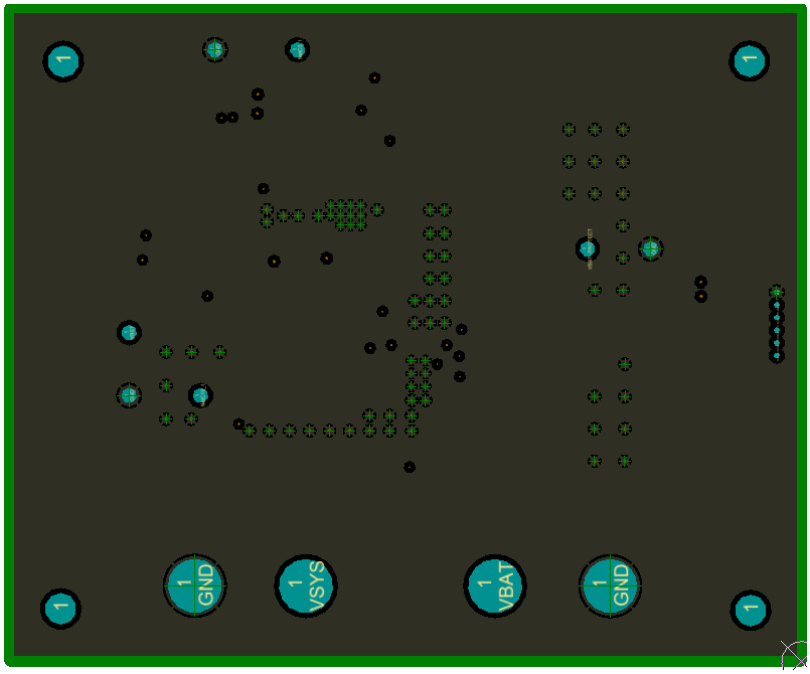


Figure 79: Layer 2 - Ground

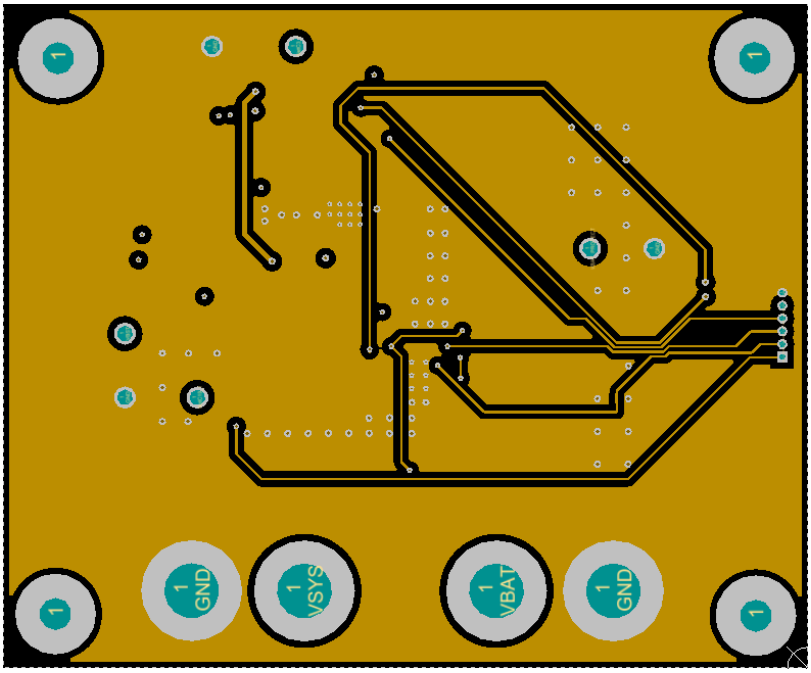


Figure 80: Layer 3 – Signal

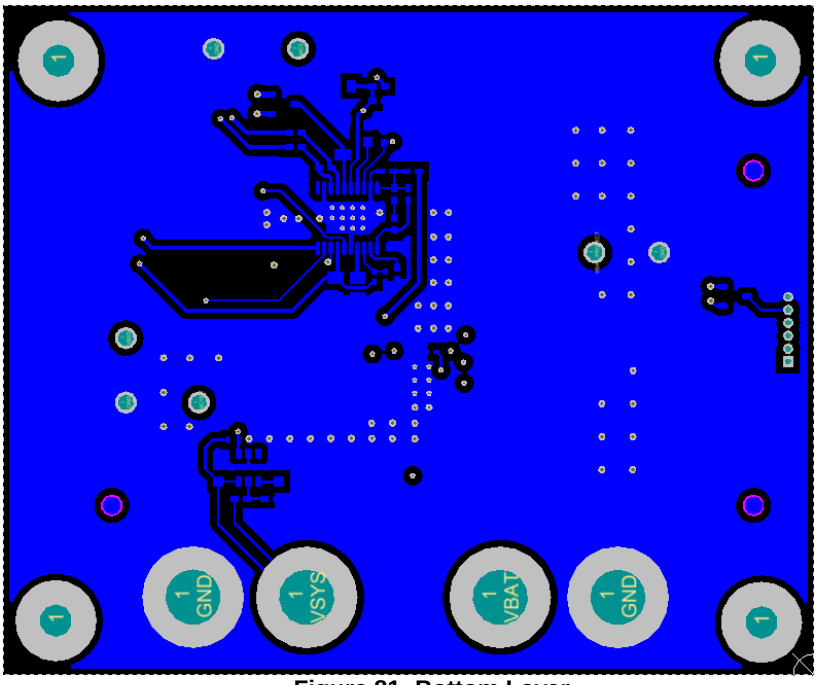


Figure 81: Bottom Layer

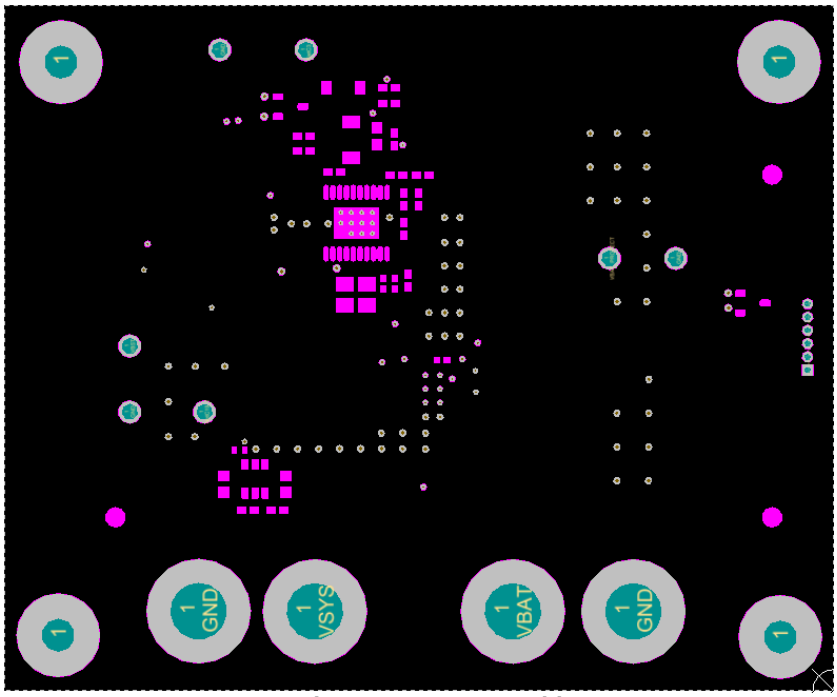


Figure 82: Bottom Solder

Figure 83: Bottom silkscreen

9.4 Altium Project & Gerber files

To download the Altium project & Gerber files for each board, see the design files at http://www.ti.com/tool/tida-00699

10 Software Files

TINA - SPICE simulation program

11 References

1. LM53603-Q1 datasheet (http://www.ti.com/product/lm53603)
2. LM25122-Q1 datasheet (http://www.ti.com/product/lm25122-q1)
3. LM74610-Q1 datasheet (http://www.ti.com/product/lm74610-q1)
4. LM3880-Q1 datasheet (http://www.ti.com/product/lm3880-q1)
5. ISO 7637-2:2004 *Road vehicles – Electrical disturbances from conduction and coupling – Part 2: Electrical transient conduction along supply lines only*, section 5.6
6. ISO 16750-2:2010 *Road vehicles – Environmental conditions and testing for electrical and electronic equipment – Part 2: Electrical loads*, section 4.6
7. CISPR 25, Edition 3.0 2008-03, *Vehicles, boats and internal combustion engines – Radio disturbance characteristics – Limits and methods of measurement for the protection of on-board receivers*
8. "AN-2155 Layout Tips for EMI Reduction in DC / DC Converters", Texas Instruments Application Note, literature number snva638a. (http://www.ti.com/lit/an/snva638a/snva638a.pdf)
9. "AN2162 Simple Success with Conducted EMI from DC-DC Converters", Alan Martin, Texas Instruments Application Note, literature number snva489c. (http://www.ti.com/lit/an/snva489c/snva489c.pdf)
10. "Split-rail approaches extend boost-converter input-voltage ranges", Haifeng Fan, Texas Instruments Analog Applications Journal. (http://www.ti.com/lit/an/slyt556/slyt556.pdf)

12 Terminology

13 About the Author

IAN CATHEY is a Systems Engineer at Texas Instruments. As a member of the Automotive Systems Engineering team, Ian focuses on ADAS (Advanced Driver Assistance Systems) end-equipments, creating reference designs for top automotive OEM and Tier 1 manufacturers. He brings to this role experience in power electronics and embedded systems design. Ian earned his Bachelor of Science in Electrical Engineering from the University of Cincinnati in Cincinnati, OH.

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