TI Designs

Power Reduction Using Dynamic Switching

Design Overview

Dynamically switching a load is a useful technique used to minimize power consumption in a system. Some loads may only require a certain time period of activity. For example, a sensor or RF antenna only requires enabling to sample data, but can remain inactive while this data is being processed. The designer can accomplish significant power savings by periodically switching a load on and off.

Design Features

- Decreased System Power Consumption
- Improved System Thermal Performance

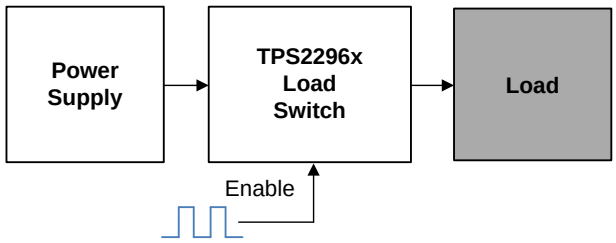
Featured Applications

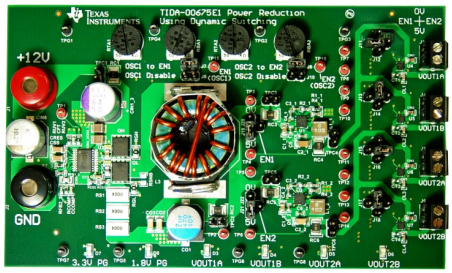
- Automotive
- Industrial Systems
- High Current Loads

Design Resources

TIDA-00675	Tool Folder Containing Design Files
TPS22965-Q1	Product Folder
TPS62090-Q1	Product Folder
LM25117-Q1	Product Folder

TI E2E™ Community — ASK Our E2E Experts





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1 Key System Specifications

Table 1. Key System Specifications

PARAMETER	SPECIFICATION	DETAILS
Operating voltage	1.8 V and 3.3 V	Typical power rails
Enable and disable frequency	10 Hz to 500 Hz	On and off switching frequency for the load
Load enable duty cycle	50%, 80%	Duty cycle during the enable period
Maximum current	0.5, 1.5, and 3.0 A	Resistive loads are used to produce this DC current
Load capacitance	10 µF	Sample load
C_T	0 pF	A value of C_T = 0 pF is used to increase switching frequency

2 System Description

Users can utilize dynamic switching as a technique to lower the average system power consumption and improve the overall system thermal performance. Load switches can be used to periodically enable and disable a load that is inactive during certain periods of time. As follows, the load only remains powered up during the time that it requires to perform a task, and is disabled otherwise. This user's guide provides examples of switching frequency across different loads and duty cycles. Power consumption comparisons are presented to show the advantage of using this technique.

2.1 TPS22965-Q1 and TPS22965N-Q1

The TPS22965-Q1 and TPS22965N-Q1 devices are single channel, 4-A load switches in an eight-pin SON package (see Figure 1). To reduce the voltage drop in high current rails, the devices implement a low resistance N-channel MOSFET. The device has a programmable slew rate for applications that require a specific rise time.

The device has very low leakage current during the off state. This low leakage current prevents downstream circuits from pulling high standby current from the supply. An integrated control logic, driver, power supply, and output discharge FET (on TPS22965-Q1 only) eliminate the requirement for any external components, which reduces the solution size and BOM.

The TPS22965N-Q1 device does not feature an output discharge field-effect transistor (FET). Excluding this feature enables the device to keep the load from discharging completely between power cycles.

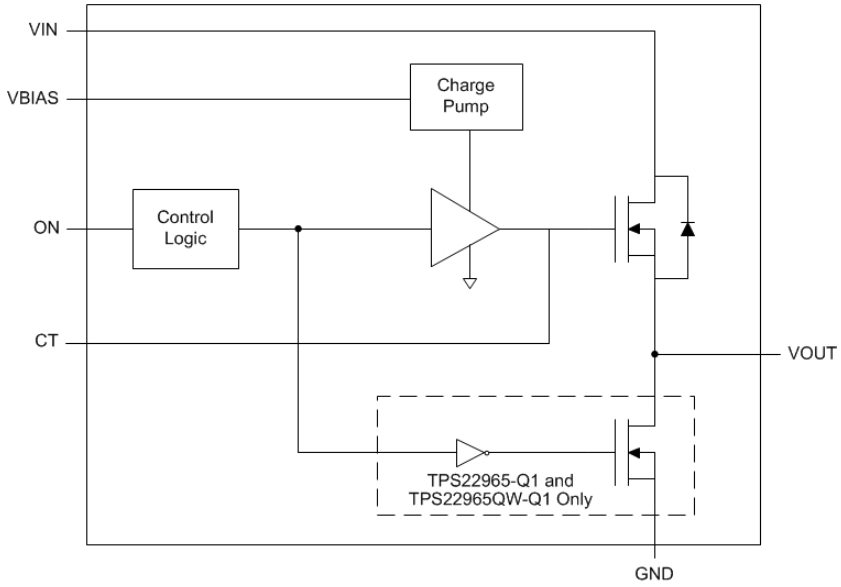

Figure 1. TPS22965-Q1 and TPS22965N-Q1 Functional Block Diagram

3 Block Diagram

The main system power is a 12-V source. The LM25117-Q1 DC-DC converter allows direct connection to a car battery. The power is stepped down to 5 V and powers the second stage. During this second stage, the 1.8 V and 3.3 V are generated and branched to the load switches.

Each rail (3.3 V and 1.8 V) is branched to two load switches: one with quick output discharge (QOD) and one without QOD. The enable signal of each of the switches in the system has the following configuration options:

- ON – Load switch is always enabled
- OFF – Load switch is always disabled (load is not powered)
- PWM – Load switch enable pin is connected to an oscillator with programmable frequency and duty cycle

The system features multiple probe points to measure current consumption at different portions of the power tree. These multiple probe points allow for individual branch probing and the evaluation of power supply efficiency (see Figure 2).

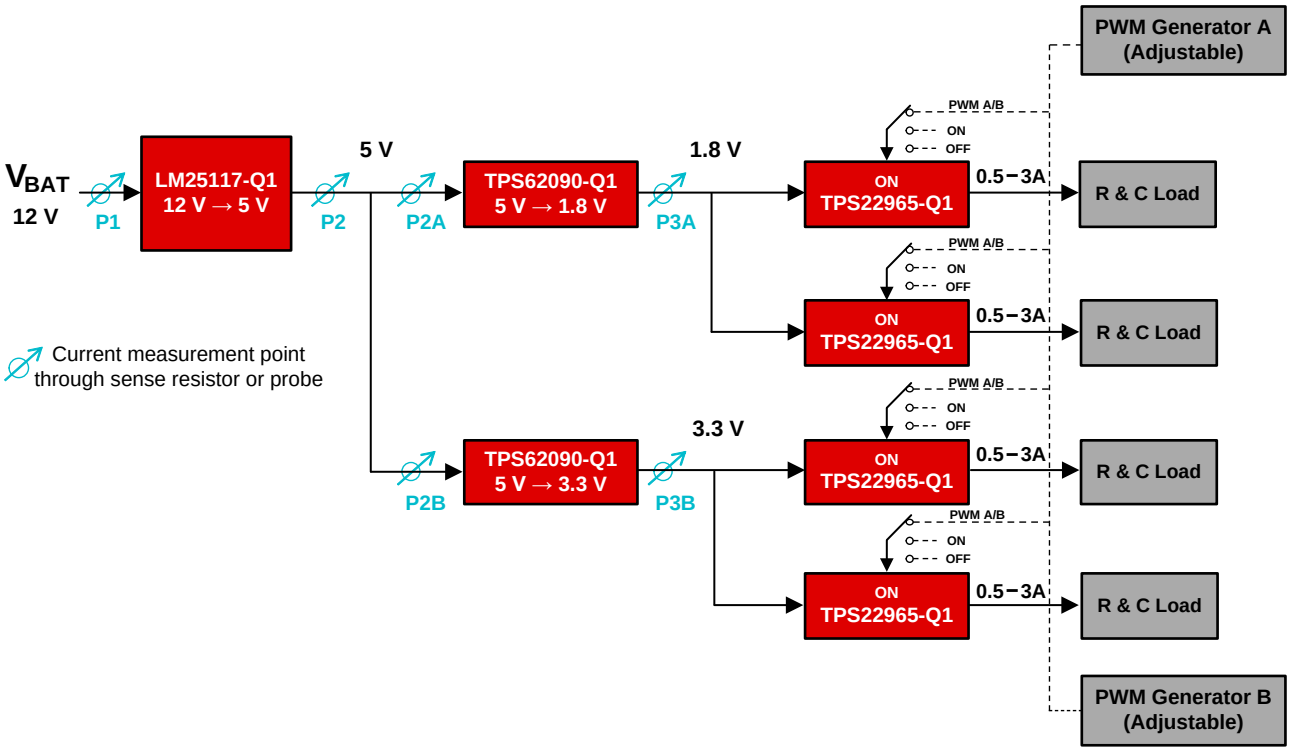

Figure 2. Dynamic Load Switching Using Typical Power Tree

3.1 Highlighted Products

3.1.1 TPS22965-Q1 and TPS22965N-Q1

- Integrated single-channel load switch
- Qualified for both commercial and automotive applications
- Device temperature range: –40˚C to 105˚C
- Input voltage range: 0.8 V to 5.5 V
- Low on resistance ®$_{ON}$)
  - R_{ON} = 16 mΩ at 3.6 V (V_{BIAS} = 5 V)
- 4-A maximum continuous switch current
- Configurable rise time
- Quick output discharge (QOD) to discharge the load after the switch has been disabled (TPS22965-Q1 only)

3.1.2 LM25117-Q1

- Synchronous buck controller intended for step-down regulation applications from a high voltage or widely varying input supply
- Both commercial and automotive qualified applications
- AEC-Q100 qualified device temperature grade 1: –40˚C to 125˚C
- Wide operating range from 4.5 V to 42 V
- Robust 3.3-A peak gate drivers
- Free-run or synchronizable clock up to 750 kHz
- Programmable output from 0.8 V
- Precision 1.5% voltage reference

3.1.3 TPS62090-Q1

- High-frequency synchronous step-down converter optimized for small solution size, high efficiency, and suitable for battery powered applications
- Qualified for automotive applications
- AEC-Q100 qualified device temperature grade 1: –40°C to 125°C
- 2.5- to 5-V input voltage range
- 95% converter efficiency
- 100% duty cycle for lowest dropout
- 2.8- and 1.4-MHz typical switching frequency
- 0.8-V to V_{IN} adjustable output voltage

4 System Design Theory

This section discusses the theory and expectations regarding power consumption reduction as a result of power-on and power-off switching of a load, as well as the switching frequency and duty cycle restrictions on the TPS22965/N-Q1 load switch.

4.1 Average Power Consumption

Power consumption can be defined in multiple ways. Two important parameters that a designer must consider when designing a power supply for a load are the average power consumption and the peak power. This reference design focuses on the average power consumption of the system.

The following Figure 3 shows an example system that is continuously enabled and remains running at an input voltage of 3.3 V. The current waveform shows that the average current consumption is approximately 1.5 A. Equation 1 shows the average power consumption for this type of system, which can be calculated as follows:

$$P(t) = V(t) \times I(t) \quad (1)$$

For this particular example, the average power consumption is 4.95 W.

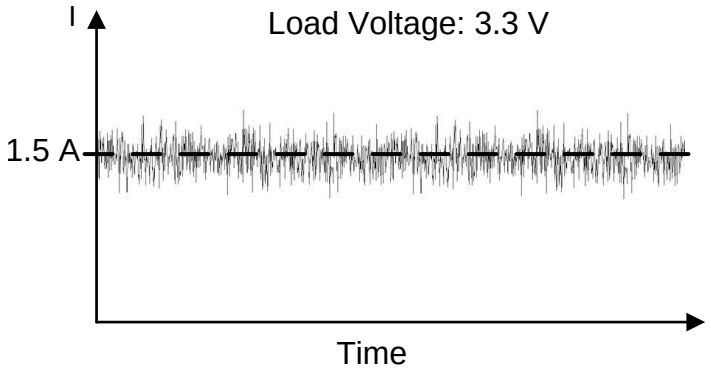

Figure 3. Average Power Consumption Example: Always Enabled

The following Figure 4 shows an example system that dynamically switches the load on and off. The assumption during the disabled period is that the load does not have any required tasks to perform. During the enabled period, the load consumes an average of 1.5 A. During the disabled period, the load voltage is zero. Furthermore, the load is enabled for 50% of the time.

For low enough switching frequencies, the switching losses may be ignored in the calculation of the average power consumption. The systems considered in this analysis are to be in the range of 10 Hz to 500 Hz.

The following Section 4.2 discusses the rate at which the current rises to the nominal active value, or drops to zero.

The following Equation 2 shows the power consumption approximation:

$$P(t) = V(t) \times I(t) \times \text{Duty Cycle} \quad (2)$$

The estimated average power consumption for this system is approximately 2.48 W. Note that the peak power consumption still remains at 4.95 W during the enabled period.

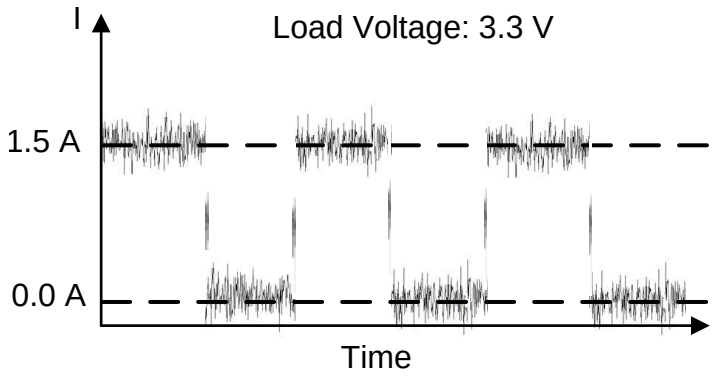

Figure 4. Average Power Consumption Example: 50% Duty Cycle Dynamic Switching

4.2 Switching Frequency and Duty Cycle

The switching frequency and duty cycle of the system is limited by the AC timing characteristics of the load switch.

Figure 5 shows the main TPS22965/N-Q1 timing parameters that affect how fast the load switch can enable and disable a load. The value of these timing parameters primarily depends on the following variables:

- V_{IN}
- V_{BIAS}
- C_L
- Temperature
- Process variation

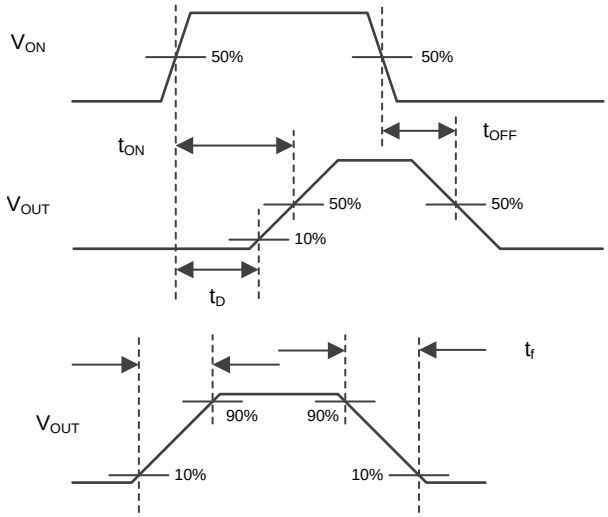

Figure 5. TPS22965/N-Q1 AC Timing Parameter Definitions

Table 2 shows a sample set of timing parameters for the TPS22965-Q1 load switch. Refer to the device data sheet (SLVSCI3) for the actual timing parameters.

Table 2. Load Switch Timing Parameters

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = V_{ON} = V_{BIAS} = 5 V, T_A = 25ºC					
t_{ON} Turnon time	RL = 10 Ω, CL = 0.1 µF, CT = 1000 pF, CIN = 1 µF		1600		µs
t_{OFF} Turnoff time			9		
t_R V_{OUT} rise time			1985		
t_F V_{OUT} fall time			3		
t_D ON delay time			660		

The typical switching characteristics allow the device to operate at 500 Hz.

4.2.1 Quick Output Discharge (QOD)

The difference between the TPS22965-Q1 and TPS22965N-Q1 devices is the quick output discharge (QOD) feature. The TPS22965-Q1 includes a QOD feature. When the switch has been disabled, an internal discharge resistor connects between VOUT and GND. This resistor has a typical value of 225 Ω and prevents the output from floating while the switch is disabled.

This feature can be a useful tool when performing dynamic switching. The TPS22965-Q1, which features QOD, can help to quickly discharge the load during the disabled state if no residue energy is desired in the system. Alternatively, the TPS22965N-Q1 device, which does not feature QOD, can allow the capacitive load to retain energy and allow further power savings. Note that some loads may require a full discharge between power cycles.

5 Getting Started Hardware

5.1 PCB Connections and Test Points

Table 3. PCB Connections and Test Points

CONNECTION	NAME	DESCRIPTION
TPC1	P1	12-V sense
TPC2	P2	5-V sense – main
TPC3	P2B	5V sense, 3.3-V regulator
TPC4	P3B	3.3-V sense
TPC5	P2A	5V- sense, 1.8-V regulator
TPC6	P3A	1.8-V sense
J1	12-V VBATT	12-V power input
J2	GND	12-V power ground
J3	R & C Load 3	3.3-V TPS22965 load
J4	R & C Load 4	3.3-V TPS22965N load
J5	R & C Load 1	1.8-V TPS22965 load
J6	R & C Load 2	1.8-V TPS22965N load
J7	Osc to EN1	Oscillator 1 disconnect
J8	Disable Timer	Timer1 disable
J9	Osc to EN2	Oscillator 2 disconnect
J10	Disable Timer	Timer2 disable
J11	J11	3.3-V TPS22965 VIN option
J12	J12	3.3-V TPS22965 ON option
J13	J13	3.3-V TPS22965N VIN option
J14	J14	3.3-V TPS22965N ON option
J15	J15	1.8-V TPS22965 VIN option
J16	J16	1.8-V TPS22965 ON option
J17	J17	1.8-V TPS22965N VIN option
J18	J18	1.8-V TPS22965N ON option
J19	J19	3.3-V TPS62090 EN option
J20	J20	3.3-V TPS62090 EN option
J21	J21	1.8-V TPS62090 EN option
J22	J22	1.8-V TPS62090 EN option

5.2 Printed Circuit Board (PCB) Features

The PCB features a wide range of flexibility for usage. The PCB features an option to use onboard (with duty-cycle and frequency control) or off-board oscillators, onboard or off-board loads, and current probe or sense points. Figure 6, Figure 7, and Figure 8 highlight the key components on the top side of the board. Figure 9 highlights the key components on the bottom side of the board.

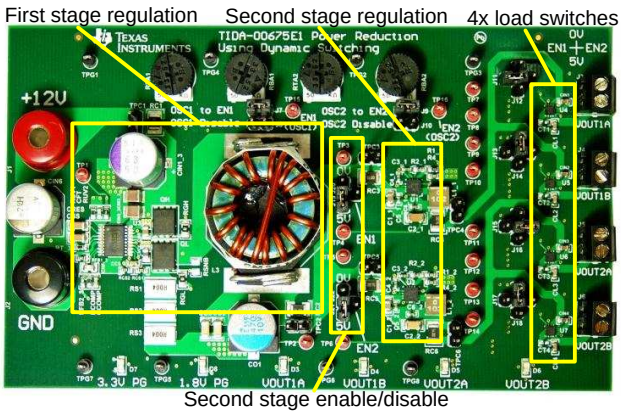

Figure 6. Board Top View—Regulation Stages and Load Switch Locations

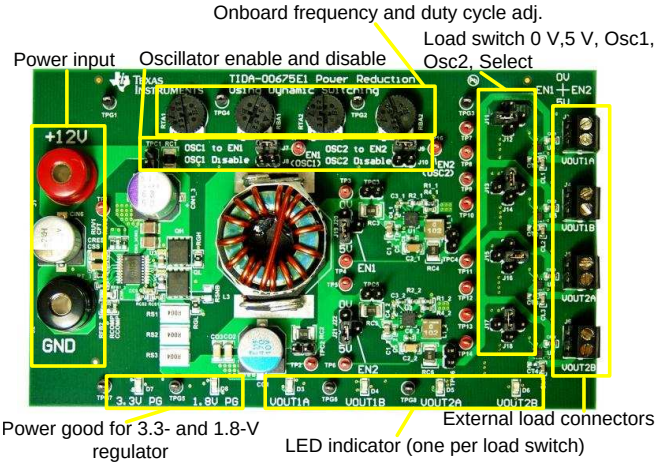

Figure 7. Board Top View—Input, Output, Oscillator Control, Load Switch Options, and LEDs

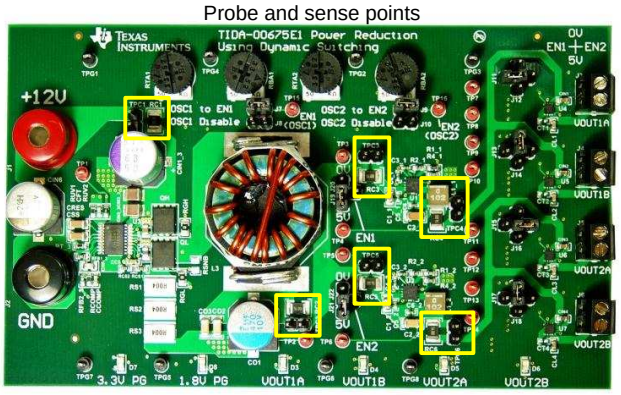

Figure 8. Board Top View—Current Sense and Probe Locations

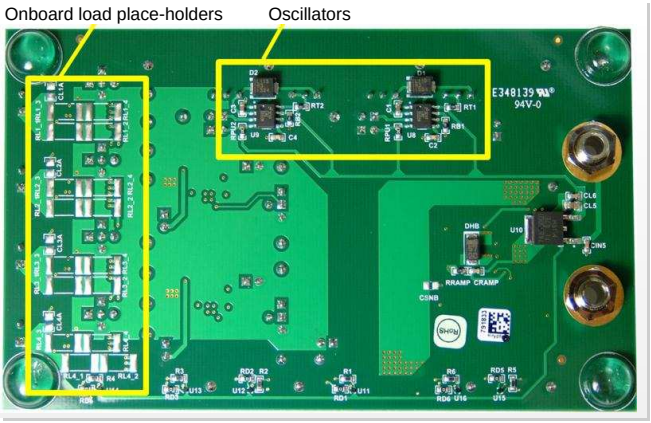

Figure 9. Board Bottom View—Oscillators, Onboard Load Option

6 Test Setup

The following Figure 10 and Figure 11 show how to connect the input voltage and the location of the external loads. The voltage source is a standard 12-V DC external power supply. The PCB features banana jack inputs for easy connection.

Figure 10. Test Setup, No Power

Figure 11 shows the board connected to the power supply. Note that the power good (PG) light-emitting diodes (LEDs) are fully illuminated. The VOUT2A LED is fully lit, showing a large duty cycle of operation on those particular loads. In contrast, VOUT2A, VOUT1A, and VOUT1B show a dimmed LED because of the low duty cycle used in this example.

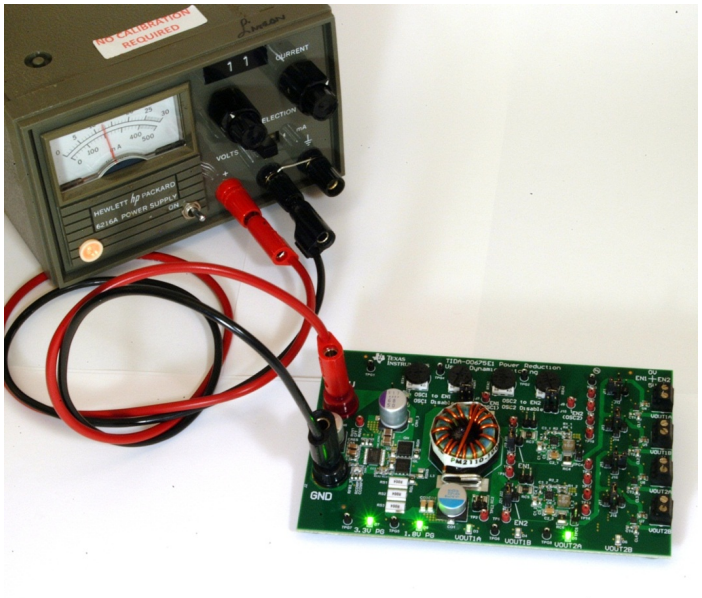

Figure 11. Test Setup, Board Powered-Up

In the following Figure 12, the values of C_L and R_L have been selected and externally connected to the connectors at VOUT1A, VOUT1B, VOUT2A, and VOUT2B.

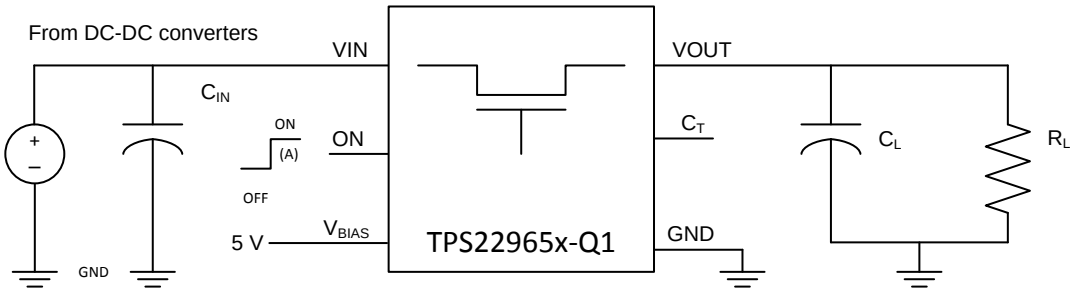

Figure 12. Load Diagram

The following experiments use the following setup, unless otherwise specified:

- C_T pin feature is unused
- C_L is fixed at 10 µF
- R_L is set to generate the desired load current at the output

The loads are externally connected to connectors J3 through J6.

7 Test Data

Several use case scenarios have been tested to observe the difference in power consumption. The following subsections show the relative power consumption differences between different combinations of switching frequency, duty cycle, and loads.

7.1 Effects of Dynamically Switching Load on Power Consumption

Certain loads in a system may be switched off during their inactive period in a periodic fashion. The following set of results show the difference in power consumption between keeping a load enabled 100% of the time and switching it on and off. This section uses the TPS22965 load switch, which features an internal discharge pulldown resistor when the switch has been disabled.

Table 4 shows the benefit of switching the load ON rather than keeping the load enabled. When switching the load ON and OFF at both 10 Hz and 500 Hz an approximate 50% reduction occurs. During the 500-Hz case, the load is fully powered for a shorter time period because a larger percentage of time has been spent ramping up and ramping down the resistive load.

Table 4. TPS22965 Switching Frequency Test Data at 3.3 V

VOLTAGE (V)	LOAD CURRENT (A)	SWITCHING FREQUENCY POWER (P3B)			DUTY CYCLE	C_L	CT	QOD
		ALWAYS ON (W)	10 Hz (W)	500 Hz (W)				
3.3	0.5	1.71	0.87	0.80	50%	10 µF	None	Yes
3.3	1.5	5.05	2.70	2.26	50%	10 µF	None	Yes
3.3	3	9.65	5.49	4.20	50%	10 µF	None	Yes

Table 5 shows similar test results at 1.8 V. This data also shows the effect in power consumption reduction in a system with more than one level of regulation. The effects of the power consumption savings have been multiplied by the efficiency of each regulation stage. Figure 2 shows the location of test points P2A and P3A.

Table 5. TPS22965 Switching Frequency Test Data at 1.8 V

VOLTAGE (V)	LOAD CURRENT (A)	SWITCHING FREQUENCY POWER (P2A)			SWITCHING FREQUENCY POWER (P3A)			DUTY CYCLE	C_L	CT	QOD
		ALWAYS ON (W)	10 Hz (W)	500 Hz (W)	ALWAYS ON (W)	10 Hz (W)	500 Hz (W)				
3.3	0.5	0.90	0.52	0.48	0.83	0.45	0.42	50%	10 µF	None	Yes
3.3	1.5	3.54	1.82	1.61	3.04	1.40	1.47	50%	10 µF	None	Yes
3.3	3	7.02	3.53	3.13	5.74	3.10	2.91	50%	10 µF	None	Yes

7.2 Effects of Duty Cycle on Power Consumption

The previous Section 7.1 describes the effects of switching the load ON and OFF with a 50% duty cycle; however, some loads may allow the use of a different duty cycle. The following test data shows the effect of changing the duty cycle.

The data in Table 6 suggests that, if possible, reducing the duty cycle of the load is beneficial by lowering power consumption; however, some loads may have restrictions on the amount of time they require to be ON to ensure they have been properly initialized.

Table 6. Effects of Duty Cycle on Power Consumption

VOLTAGE (V)	LOAD CURRENT (A)	SWITCHING FREQUENCY POWER (P3B)			C_L	CT	QOD
		10 Hz AT 80% DUTY CYCLE (W)	10 Hz AT 50% DUTY CYCLE (W)	10 Hz AT 20% DUTY CYCLE (W)			
3.3	0.5	1.43	0.87	0.37	10 µF	None	Yes
3.3	1.5	4.07	2.70	1.14	10 µF	None	Yes
3.3	3	6.87	5.49	2.27	10 µF	None	Yes

7.3 Effects of QOD on Power Consumption

The preceding power consumption data in Section 7.2 describes the power consumption when using a load switch with a QOD resistor. This section shows the effect of not having a discharge resistor when the load switch has been disabled. Some loads may tolerate not being fully discharged between power cycles, in which case, it may be beneficial to the system to retain as much of the charge stored and not dissipate it through the QOD resistor. The TPS22965N device allows a load to maintain the charge between power cycles as this device does not feature an internal QOD resistor.

The load in this example has been reduced to simulate a load with low resistance but high capacitance during the inactive cycle.

In this particular case, the objective is to maintain the energy in the system and not discharge it through the internal QOD resistor. The data in Table 7 clearly shows a significant difference in power consumption when there is no QOD present in the load switch. Figure 13 shows the voltage output of the switching waveform. Note that the output never reaches the 0-V level between power cycles.

Table 7. Effects of QOD on Power Consumption

VOLTAGE (V)	LOAD CURRENT (µA)	SWITCHING FREQUENCY POWER (P1)		C_L	CT	QOD
		ALWAYS ON (mW)	500 Hz AT 50% DUTY CYCLE (mW)			
3.3	33	0.29	24.8	10 µF	None	Yes
3.3	33	0.29	0.290	10 µF	None	No

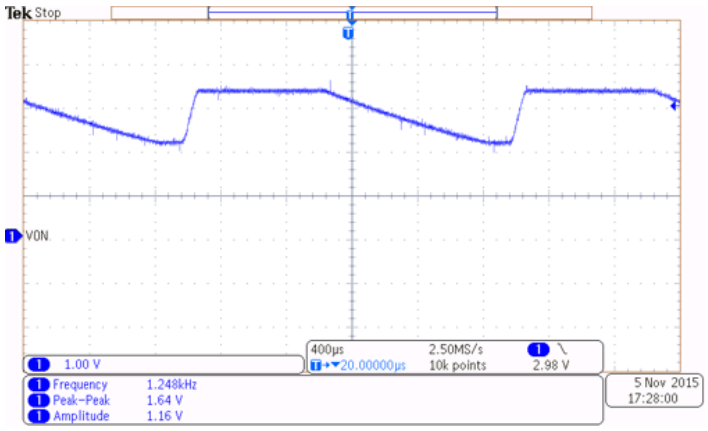

Figure 13. Output Voltage With No QOD

7.4 Comparison of Full System Power Consumption

The following data in Table 8 shows a comparison of the entire system running. All four switches are enabled and the power is measured at the 12-V input. The results include power supply efficiencies for both stages.

Table 8. Comparison of Full System Power Consumption

VOLTAGE (V)	LOAD CURRENT (A)	SWITCHING FREQUENCY POWER (P1)		C_L	CT	QOD
		ALWAYS ON (W)	10 Hz AT 50% DUTY CYCLE (W)			
3.3 V and 1.8 V	0.5	6.4	3.6	10 µF	None	Both
3.3 V and 1.8 V	1.5	19.7	11.2	10 µF	None	Both

8 Design Files

8.1 Schematics

To download the schematics, see the design files at TIDA-00675.

8.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00675.

8.3 PCB Layout Recommendations

For the TPS22965-Q1 and TPS22965N-Q1 devices, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace should be as short as possible to avoid parasitic capacitance.

For additional information on PCB layout recommendations on TPS22965-Q1, TPS22965N-Q1, LM25117-Q1, and TPS62090-Q1, refer to the device specific data sheets.

8.3.1 Layout Prints

To download the layout prints, see the design files at TIDA-00675.

8.4 Altium Project

To download the Altium project files, see the design files at TIDA-00675.

8.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00675.

8.6 Assembly Drawings

To download the assembly files, see the design files at TIDA-00675.

9 References

1. Texas Instruments, *Load Switches: What Are They, Why Do You Need Them And How Do You Choose The Right One?*, Application Report (SLVA652)
2. Texas Instruments, *LM25117/Q1 Wide Input Range Synchronous Buck Controller With Analog Current Monitor*, LM25117 and LM25117-Q1 Datasheet (SNVS714)
3. Texas Instruments, *3-A High-Efficiency Synchronous Step-Down Converter with DCS-Control™*, TPS62090-Q1 Datasheet (SLVSC55A)

10 About the Author

IVÁN GARCIA is a Systems Engineer at Texas Instruments, where he is responsible for developing load switch and eFuse solutions. Iván earned his Bachelors of Science and Masters in Science in Electrical Engineering from The University of Texas at El Paso.

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