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TI Designs – Precision: CerTIfied Design

2-wire 4-20mA Transmitter, EMC/EMI Tested Reference Design

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Design Resources

TIPD190	All Design files
TINA-TI™	SPICE Simulator
DAC8551	Product Folder
XTR116	Product Folder

Circuit Description

This 2-wire, or loop-powered, analog output can accurately control the loop current from 4 mA to 20 mA. The design also includes an output protection circuit for IEC61000-4 immunity and a bridge rectifier to enable functionality regardless of the polarity of loop supply connections.

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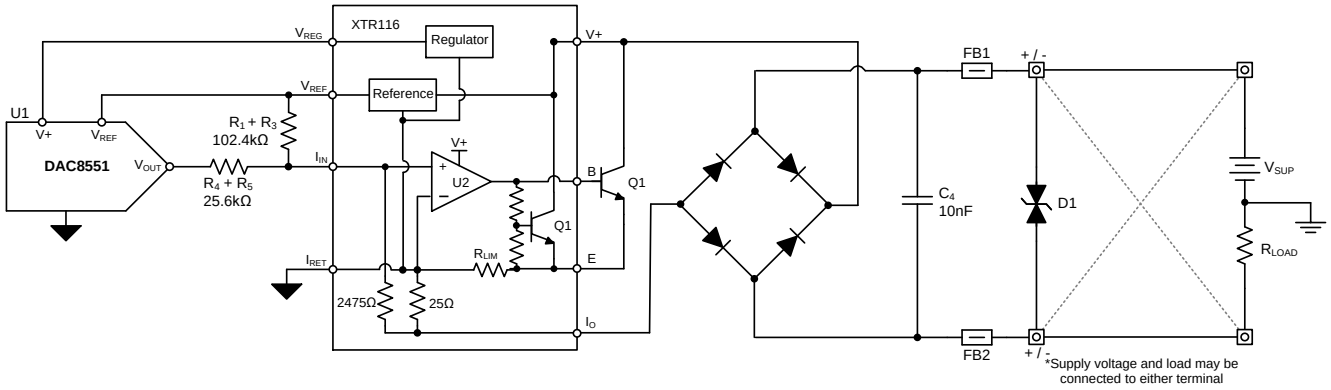

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1 Design Summary

The design requirements are as follows:

- Supply Voltage: ≤36 V
- Input: 3-Wire SPI
- Output: 4-20 mA, 0.5% FSR Total Unadjusted Error (TUE)
- Loop Compliance Voltage: V_S – 12 V

In addition to the parametric goals above, the design is expected to deliver immunity to the IEC61000-4 suite of tests with minimum impact on the accuracy of the system. The design goals, simulated results, and measured performance are summarized in Table 1. Figure 1 depicts the measured transfer function and accuracy of the design, illustrating results collected from 6 boards.

Table 1. Comparison of Design Goals, Calculated, and Measured Performance

	Goal	Calculated	Measured
Output TUE	0.5% FSR	0.495% FSR	0.142% FSR
Loop Compliance Voltage	12 V	n/a	7.5 V
IEC61000-4 Immunity	Pass	n/a	Pass

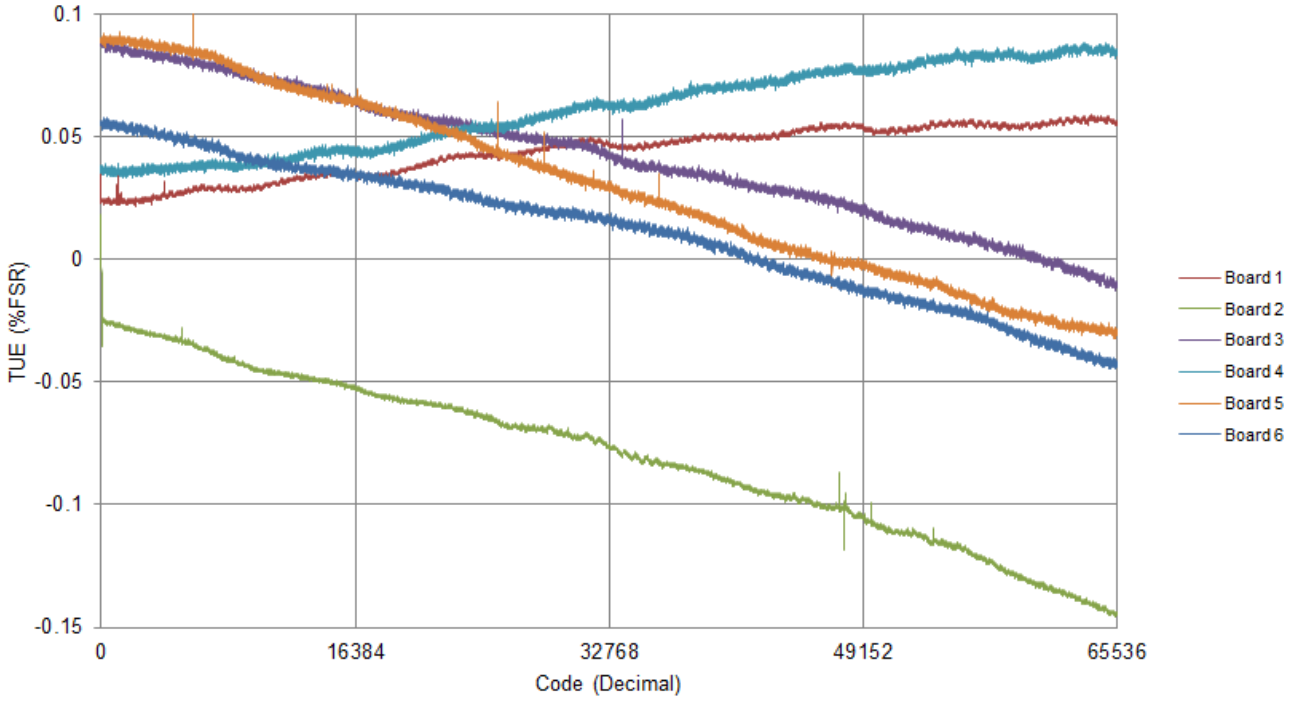

Figure 1: Measured TUE vs. Input Code

2 Theory of Operation

2.1 Voltage to Current Converter

A simplified form of the voltage to current converter is shown in Figure 2. This design is commonly referred to as a loop-powered, or 2-wire, 4-20 mA transmitter. The transmitter has only two external input terminals: a supply connection and an output, or return, connection. The transmitter communicates back to its host, typically a PLC analog input module, by precisely controlling the magnitude of its return current. In order to conform to the 4-20 mA communication standard, the complete transmitter must consume less than 4 mA of current.

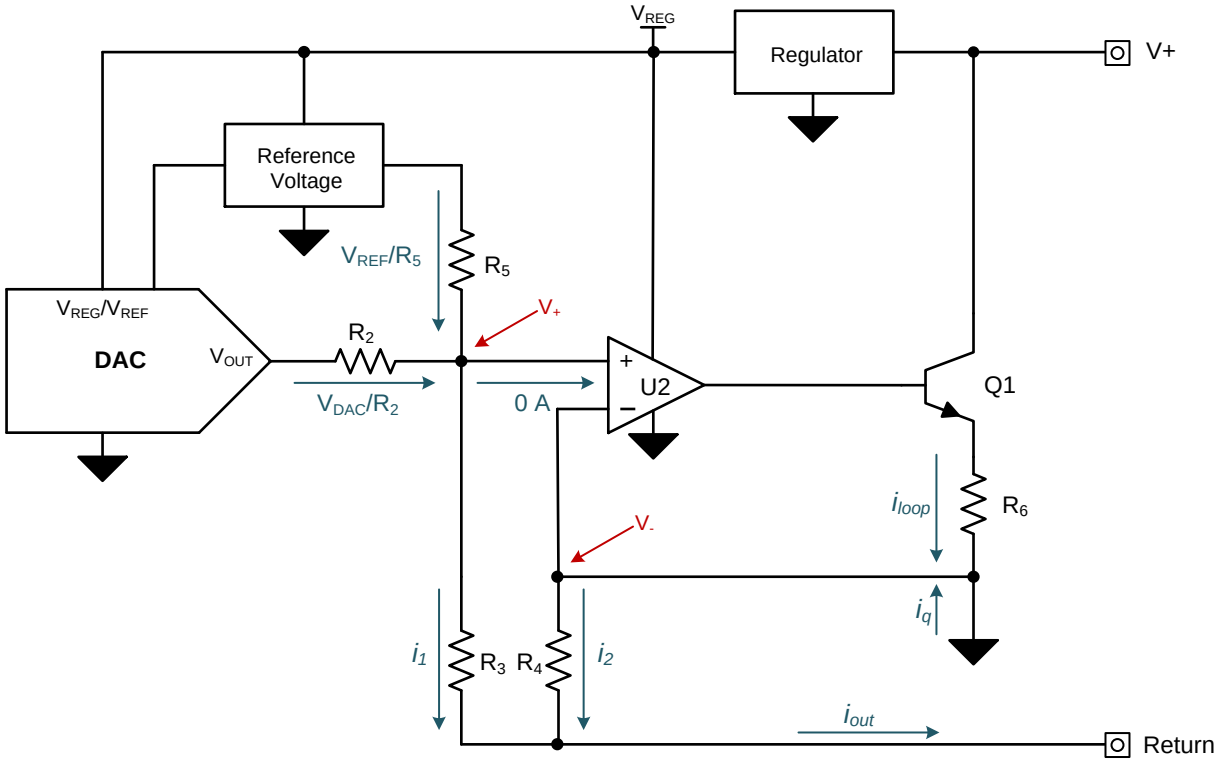

Figure 2: Simplified Voltage to Current Converter Circuit

Negative feedback of the U2 op amp will force the inverting (V_-) and non-inverting (V_+) input terminals to the same voltage. In this circuit V_- is directly tied to the local ground. Therefore the potential at the non-inverting input terminal will be driven to the local ground. This means that the voltage difference across R_2 is equal to DAC output voltage, V_{OUT}, and the voltage difference across R_5 is equal to reference voltage V_{REF}. These voltage differences cause current to flow through R_2 and R_5, as illustrated in Figure 2. The current through these components sum into the current flowing through R_3, i_1, as defined in Equation (1).

$$i_1 = \frac{V_{DAC}}{R_2} + \frac{V_{REF}}{R_5} \quad (1)$$

For the inputs of the op amp to be equal to each other, the current flowing through R4, i_2, must create a voltage drop across R4 that is equal to the voltage drop across R3. The quiescent current of the components (regulator, amplifier, DAC, etc.) used in the transmitter design, i_Q, creates a small part of the i_2 current. The op amp then drives the base of the Q1 NPN BJT to create the remainder of the current, i_{LOOP}, such that the voltage drops across R3 and R4 are equal.

Since the voltage drops across R_3 and R_4 are equal, different sized resistors will cause different currents flow through each resistor. This can be used to apply gain to the current flow through R_4 by controlling the ratio of resistor R_3 to R_4, as shown in Equation (2).

$$\begin{aligned} V_+ &= i_1 \cdot R_3 \\ V_- &= i_2 \cdot R_4 \\ V_+ &= V_- \\ \Rightarrow i_2 &= \frac{i_1 \cdot R_3}{R_4} \end{aligned} \quad (2)$$

The current gain is helpful to allow a majority of the output current to come directly from the loop through Q1 instead of from the input stage of circuit. This, in addition to low-power components, keeps the current consumption of the voltage to current converter low. The currents i_1 and i_2 sum to form the output current, i_{OUT}, as shown in Equation (3).

$$\begin{aligned} i_{out} &= i_1 + i_2 = \frac{V_{DAC}}{R_2} + \frac{V_{REF}}{R_5} + \frac{R_3}{R_4} \cdot \left(\frac{V_{DAC}}{R_2} + \frac{V_{REF}}{R_5} \right) \\ i_{out} &= \left(\frac{V_{DAC}}{R_2} + \frac{V_{REF}}{R_5} \right) \cdot \left(1 + \frac{R_3}{R_4} \right) \end{aligned} \quad (3)$$

The complete transfer function, arranged as a function of input code, is shown in Equation (4) below.

$$i_{out}(Code) = \left(\frac{V_{REF} \cdot Code}{2^N \cdot R_2} + \frac{V_{REG}}{R_5} \right) \cdot \left(1 + \frac{R_3}{R_4} \right) \quad (4)$$

where : N is the number of bits of DAC resolution

R_6 is included to reduce the gain of transistor Q1 and therefore reduce the closed loop gain of the voltage to current converter to achieve a stable design. Resistors R_2, R_3, R_4, and R_5 should be sized based on the full-scale range of the DAC, regulator voltage, and the desired current output range of the design.

2.2 Loop Voltage Regulator

A loop voltage regulator is required in this design to step down the loop supply voltage, nominally 24 V, to a low-voltage commonly used by precision analog components. LDOs, DC/DC converters, and shunt regulators are all acceptable solutions.

2.3 Diode Bridge & Protection Circuit

The industrial environment can be very dangerous for sensitive electronic components. Systems are therefore designed to be very robust and include protection against incorrect wiring and to provide immunity to environmental hazards that may lead to electrical overstress or undesired performance. Figure 3 shows the circuit used to protect this design from these events.

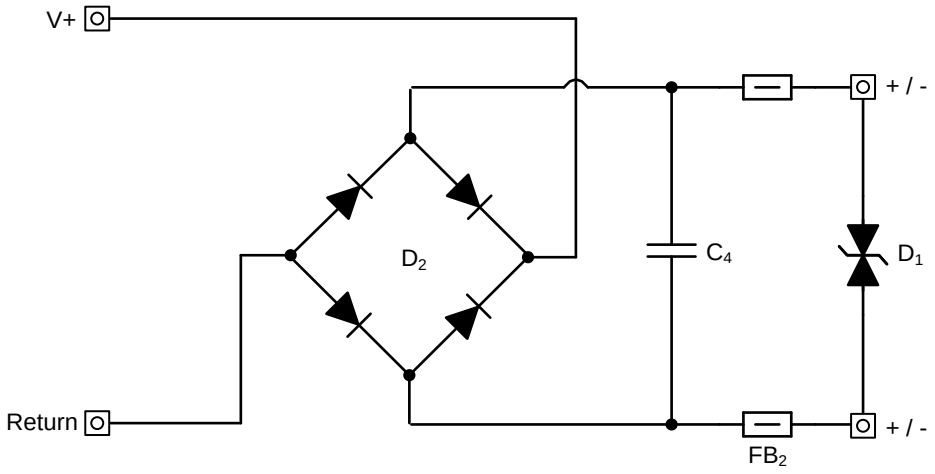

Figure 3: Diode Bridge & Protection Circuit

To protect against incorrect terminal connections a diode bridge is implemented. Two diodes are placed with their cathodes connected to the positive node of the loop transmitter and anodes connected to each of the terminal blocks. Similarly, two diodes are placed with anodes connected to the return node of the loop transmitter and cathodes connected to each of the terminal blocks. This arrangement allows the circuit to function regardless of which terminal is connected to the supply and which is connected to the return, protecting against incorrect wiring faults.

2.3.1 IEC61000-4 Test Standard

Many transient signals or radiated emissions common in industrial applications can cause electrical over-stress (EOS) damage or other disruptions to unprotected systems. IEC61000-4 is a test suite that simulates these transient and emission signals and awards a certification to systems that prove to be immune. During each of the IEC61000-4 tests, the output of the equipment under test (EUT) is monitored for deviations or total failure. Results are assigned one of four class ratings for each test. The classes are listed and described in Table 2.

Table 2. IEC61000-4 Result Classes

Grade	Description
Class A	Normal performance within an error band specified by the manufacturer.
Class B	Temporary loss of function or degradation of performance which ceases after the disturbance is removed. The equipment under test recovers its normal performance without operator interference.
Class C	Temporary loss of function or degradation of performance, correction of performance requires operator intervention.
Class D	Loss of function or degradation of performance which is not recoverable, permanent damage to hardware or software, or loss of data.

See Appendix B for photos of conventional test setups for each of the tests mentioned in this section. Full details of each of the IEC61000-4 tests are licensed by the IEC and must be purchased.

2.3.1.1 IEC61000-4-2: Electrostatic Discharge

The electrostatic discharge (ESD) immunity test emulates the electrostatic discharge of an operator directly onto an electrical component. To simulate this event, an ESD generator applies ESD pulses to the EUT either through air discharge or through vertical and horizontal coupling planes. Air discharge tests are conducted near any exposed I/O terminal.

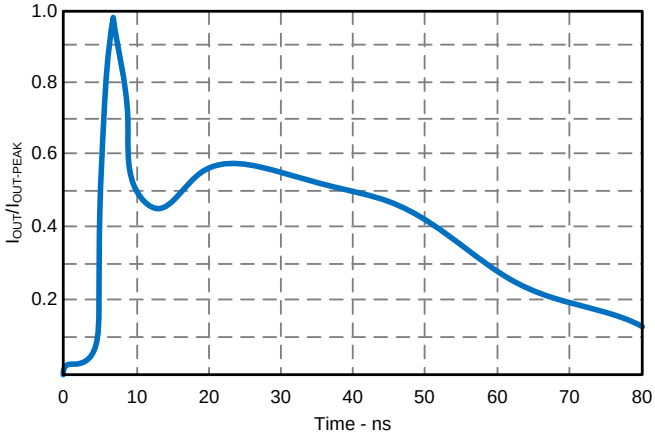

Figure 4: IEC61000-4 ESD Test Pulse

The ESD test pulse is pictured in Figure 4. The ESD test pulse is a high frequency transient with a pulse period of less than 100ns. The pulse is a high-voltage signal, ranging from 4 kV to 15 kV depending on the threat level appropriate for the EUT. The complete ESD test requires 10 sequential discharges of each positive and negative polarity for each test configuration.

2.3.1.2 IEC61000-4-3: Radiated Immunity

The radiated immunity (RI) test emulates exposure to high frequency radiated emissions, such as radio devices or other emissions common in industrial processes. The frequency range and field strength of the radiated signals vary in this test based on the type of EUT. For this design the tested frequency range was 80 MHz – 1 GHz and the field strength was 20 V/m.

2.3.1.3 IEC61000-4-4: Electrically Fast Transient

The burst immunity, or electrically fast transient (EFT) emulates day to day switching transients from various sources in a typical industrial application space. The test is performed on power, signal, and earth wires – or a subset depending on what is appropriate for the EUT.

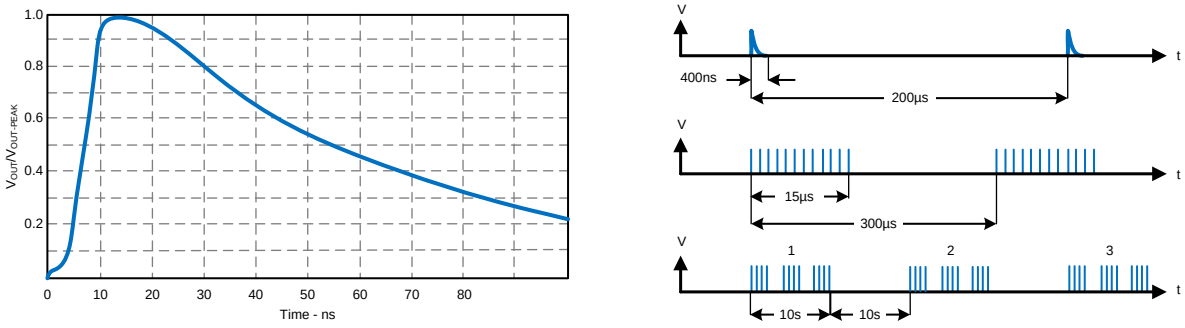

Figure 5: IEC61000-4 EFT Test Pulses

In this test a burst generator produces a series of EFT bursts, each lasting 15ms with 300ms in between bursts. The pulse rate of each burst is approximately 5 kHz. A typical test will expose the EUT to 1 – 3 minutes of EFT bursts. Similar to the ESD test pulse, the EFT pulses are a high frequency signal but the magnitude of the EFT test pulse only ranges from 0.25 kV to 4 kV. Bursts of both positive and negative polarity are applied.

2.3.1.4 IEC61000-4-6: Conducted Immunity

The conducted immunity (CI) test simulates exposure to radio frequency transmitters in the range of 150 kHz to 80 MHz. Like the RI test, the field strength of the CI transmitter can vary, ranging from 3 V/m to 10 V/m.

2.3.2 Protection Circuitry

The IEC61000-4 transients have two main components: a high frequency component and a high energy component. These two properties can be leveraged with a strategy of attenuation and diversion by the protection circuitry to deliver robust immunity.

Attenuation uses passive components, primarily resistors and capacitors, to attenuate high-frequency transients and to limit series current. Ferrite beads are commonly used with voltage outputs to maintain dc accuracy while still limiting series current, but they can also be useful for current outputs since they do not add any additional compliance voltage headroom at dc. A ferrite is included in series between each of the terminal blocks and the diode bridge along with a parallel capacitor to attenuate the high-frequency transients and limit current flow during exposure to transients.

Diversion capitalizes on the high voltage properties of the transient signals by using diodes to clamp the transient within supply voltages or to divert the energy to ground or the return path. Transient voltage suppressor (TVS) diodes are helpful to protect against the IEC transients because they break down very quickly and often feature high power ratings which are critical to survive multiple transient strikes. A TVS diode is included in between the two terminal block connections, positioned close to the terminal blocks in the PCB layout.

2.4 Loop Compliance Voltage

Loop compliance voltage defines the maximum voltage that may be present at the point of load of the current output for the loop transmitter to remain in the linear region of operation. Equation (5) can be used to express the maximum load that the loop transmitter can drive or the minimum supply voltage that the transmitter needs to drive a given load.

$$Compliance Voltage \leq V_{SUP} - I_{OUT} R_{LOAD} \quad (5)$$

Compliance voltage can be influenced by two components of the transmitter design – the operating region of the loop pass transistor, Q1, and the supply requirements for the loop regulator.

In normal operation Q1 is in the forward-active region, but it is possible to enter other operating regions. The reverse-active region is not possible in this circuit due to the diode bridge rectifier included in the protection circuitry. It is possible for Q1 to approach the cut-off region because current flowing through Q1 into R_6 creates a voltage drop that effectively raises the emitter voltage. In order to maintain V_{BE} the A1 output voltage must increase proportionally to the emitter voltage, but A1 will eventually encounter output swing to rail limitations causing Q1 to enter cut-off. In most designs this is not a concern because circuit stability can be realized with a small R_6 resistor.

It is possible for Q1 to enter saturation, but in most cases V_{CE} is smaller than the required supply voltage for the loop regulator. Therefore, compliance voltage in most designs is defined by the required input supply voltage for the loop regulator, which is impacted directly by the size of R_4, R_{LOAD}, and any cabling impedance that reduces the supply voltage seen by the regulator.

3 Component Selection

Component selection for all devices used in this design is limited to low power devices in order to comply with the 4-20 mA standard. Figure 6 shows a detailed diagram of the complete design including final values for discrete components and the specific integrated circuits used.

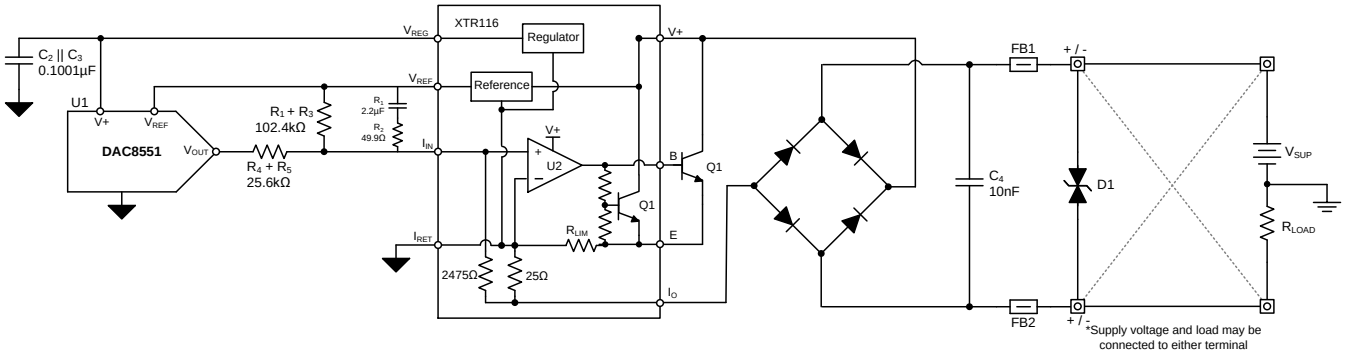

Figure 6: Detailed Design Diagram

3.1 Voltage-to-Current Converter & Regulator

The XTR116 is a complete front-end for loop-powered transmitters used in industrial automation and process control applications. It includes a 5V loop regulator, 4.096V reference, and voltage to current converter circuitry. The regulator and reference voltages can be used to provide the power and reference voltages to a conventional low-voltage precision DAC and other sensor conditioning circuitry used to control the input to the XTR116.

The TUE of the XTR116 is 0.25% FSR referred to its input voltage. Additional errors will be contributed to the design due to the errors associated with the reference voltage of the XTR116.

3.2 DAC

Accuracy errors associated with the DAC will propagate through the rest of the signal chain and potentially decrease the accuracy of the overall solution. Therefore, the DAC dc error sources should be less than or comparable to those of the XTR116 in order to minimize the impact the DAC has on the design. A DAC with minimal offset error, gain error, and linearity errors (INL and DNL) of similar to the maximum 0.25% FSR TUE of the XTR116 should be chosen. In order to pair well with the XTR116, the device should be capable of functioning with the 5V supply regulator and 4.096V reference outputs of the XTR116.

DAC8551 was chosen for this design because it delivers good dc performance, at 0.33% FSR maximum, while consuming a maximum of 250 µA under nominal operating conditions. The DAC8551 works well with the 5 V supply and 4.096 V reference from the XTR116.

3.3 Diodes

3.3.1 TVS Diode

A bidirectional TVS diode is used to divert high voltage transients to ground. Selection of this diode should be based on working voltage, breakdown voltage, leakage current and power rating. The working voltage specification defines the largest reverse voltage that the diode is meant to be operated at continuously without it conducting. This is the voltage at the “knee” of the reverse breakdown curve where the diode begins to break down and exhibits some small leakage current. As the voltage increases above the working voltage, more current will begin to flow through the diode. The breakdown voltage defines the reverse voltage at which the diode is fully allowing current to flow. It is important to keep in mind that if excessive current flows through a diode, the breakdown voltage will rise.

The diode breakdown voltage should be low enough to protect all components connected to the output terminals and to provide headroom to continue providing this protection as the breakdown voltage rises with large currents. In this design the working voltage of the TVS diode should be at or above the upper limit of the allowed supply voltages since any higher voltage would cause leakage through the diode. In this case a diode with working voltage of 36V, breakdown voltage of 40 V, and power rating of 400 W was chosen.

An additional parameter to consider for TVS diode selection is leakage current. At the working voltage, when the diode is not operating in its breakdown region, some current will flow through the diode and can affect system accuracy. The diode selected for this design features 1 µA maximum leakage current at the working voltage.

3.3.2 Diode Bridge

A diode bridge, or bridge rectifier, is used in this design to keep the design functioning as intended regardless of the arrangement of terminal block connections. Selection of this diode should be based on low reverse leakage current and low forward voltage. Low reverse leakage current should also be considered because two diodes in the bridge configuration will always be reverse biased and allowing some leakage current and will directly impact accuracy. Low forward voltage is helpful because this allows for the design to achieve lower compliance voltage.

The DSRHD10 was chosen for this design because it offers 4 diodes in the desired arrangement in a single package. This device features 0.1 µA reverse leakage current at peak reverse bias of 1000V and 1.15 V forward voltage at peak forward current of 1 A. Reverse leakage current improves to less than 0.01 µA under the operating conditions defined by this design. Similarly forward voltage improves to ~0.6 V.

3.4 Passives

Series ferrites and a parallel capacitor are used to attenuate transient signals that may remain after passing the TVS diode. The ferrites are chosen based on their current rating, impedance at dc, and impedance at high frequency. In this design the chosen ferrites feature 42 mΩ max impedance at dc, 600 Ω impedance at 100MHz, and 3 A current rating. The capacitor chosen has a voltage rating of 100V.

Several of the resistors used in this design must have tight tolerances in order to achieve high accuracy. This includes the gain setting resistors R_4 and R_5 and the offset setting resistors R_1 and R_3. Resistor R_2 and capacitor C_1 are included for stability of the XTR116 reference output, and their tolerance is not critical.

4 Calculation

At this time of this document, complete SPICE models are not available for each of the devices used in this design. Therefore, hand calculations based on the errors described in each product datasheet were performed to estimate the DC accuracy of this design at room temperature.

4.1 DAC Calculations

The DAC contributes three primary error sources to the system: offset error, gain error, and integral non-linearity error (INL), which are specified in the product datasheet. Each of these errors are derived from uncorrelated sources, allowing a root-sum-squared (RSS) technique to be applied to sum the error sources. The equation used to sum these error sources is shown in Equation (6). Typical and maximum calculation results are shown in Table 3.

$$TUE_{DAC} = \sqrt{OffsetError_{DAC}^{2} + GainError_{DAC}^{2} + LinearityError_{DAC}^{2}} \quad (6)$$

Table 3. DAC Calculation Results

Parameter	Calculated Typical	Calculated Maximum
INL Error (%FSR)	0.0046	0.0122
Offset Error (%FSR)	0.0488	0.2930
Gain Error (%FSR)	0.0200	0.1500
TUE (%FSR)	0.0529	0.3294

4.2 XTR Calculations

Similar to the DAC, the XTR116 contributes offset, gain, and linearity errors which are described in the product datasheet. Each of these errors are derived from uncorrelated sources, again allowing a RSS technique to be applied to sum the error sources. The equation used to sum these error sources is shown in Equation (7). Typical and maximum calculation results are shown in Table 4.

$$TUE_{XTR} = \sqrt{OffsetError_{XTR}^{2} + GainError_{XTR}^{2} + LinearityError_{XTR}^{2}} \quad (7)$$

Table 4. DAC Calculation Results

Parameter	Calculated Typical	Calculated Maximum
Linearity Error (%FSR)	0.0010	0.0100
Offset Error (%FSR)	0.0024	0.0122
Gain Error (%FSR)	0.0500	0.2000
TUE (%FSR)	0.0532	0.2505

The XTR116 also includes an internal reference which will contribute additional dc errors. The reference voltage input for the DAC8551 is the reference voltage from the XTR116, therefore the initial accuracy of the XTR116 reference voltage contributes a gain error to the DAC performance. Since the LSB size of the DAC8551 is also modified by reference tolerance, the linearity of the DAC8551 is also slightly impacted by reference accuracy. The XTR116 reference voltage is also used by R_1 and R_3 to create the zero-scale current for the system, so the initial accuracy of the reference also contributes a gain error. In this case the offset, gain, and linearity errors contributed by the reference initial accuracy are directly correlated, so the TUE calculation is simply a summation of these error terms. Table 5 summarizes the errors contributed by the XTR116 reference voltage.

Table 5. DAC Calculation Results

Parameter	Calculated Typical	Calculated Maximum
Linearity Error (%FSR)	0.000002	0.00003
Offset Error (%FSR)	0.0125	0.0625
Gain Error (%FSR)	0.0510	0.2875
TUE (%FSR)	0.063502	0.35003

4.3 Resistor Calculations

Resistors R_1 and R_3 are used along with the XTR116 reference voltage to create an offset current used to set the zero-scale output of the system. The tolerance of these resistors will contribute an offset error to the design. R_4 and R_5 are used with the DAC8551 output voltage to set the span of the system output, and therefore their tolerance will contribute a gain error to the design. Typical and maximum error contributions are calculated assuming a Gaussian distribution of resistor values with 0.1% maximum tolerance.

$$TUE_{Resistors} = \sqrt{OffsetError_{Resistors}^{2} + GainError_{Resistors}^{2}} \quad (8)$$

Table 6. Resistor Calculation Results

Parameter	Calculated Typical	Calculated Maximum
Offset Error (%FSR)	0.0083	0.0250
Gain Error (%FSR)	0.0333	0.1001
TUE (%FSR)	0.0343	0.1031

4.4 System Calculations

Aggregate system performance can be calculated by the RSS of each of the uncorrelated error sources discussed in sections 4.1, 4.2, and 4.3. Table 7 summarizes the calculated performance of this system and includes the design goals stated at the beginning of this document.

Table 7. DAC Calculation Results

Parameter	Calculated Typical	Calculated Maximum	Goal
Linearity Error (%FSR)	0.0047	0.0158	n/a
Offset Error (%FSR)	0.0511	0.3009	n/a
Gain Error (%FSR)	0.0813	0.3939	n/a
TUE (%FSR)	0.0962	0.4959	0.5000

5 PCB Design

The PCB schematic and bill of materials can be found in the Appendix.

5.1 PCB Layout

For optimal performance of this design follow standard PCB layout guidelines, including proper decoupling close to all integrated circuits and adequate power and ground connections will large copper pours.

Additional considerations must be made for providing robust EMC/EMI immunity. All protection elements should be placed as close to the output connectors as possible to provide a controlled return path for transient currents that does not cross sensitive components. To allow optimum current flow wide, low-impedance, low-inductance traces should be used along the output signal path and protection elements. When possible copper pours are used in place of traces. Stitching the pours provides an effective ground return path around the PCB and helps reduce the impact of radiated emissions.

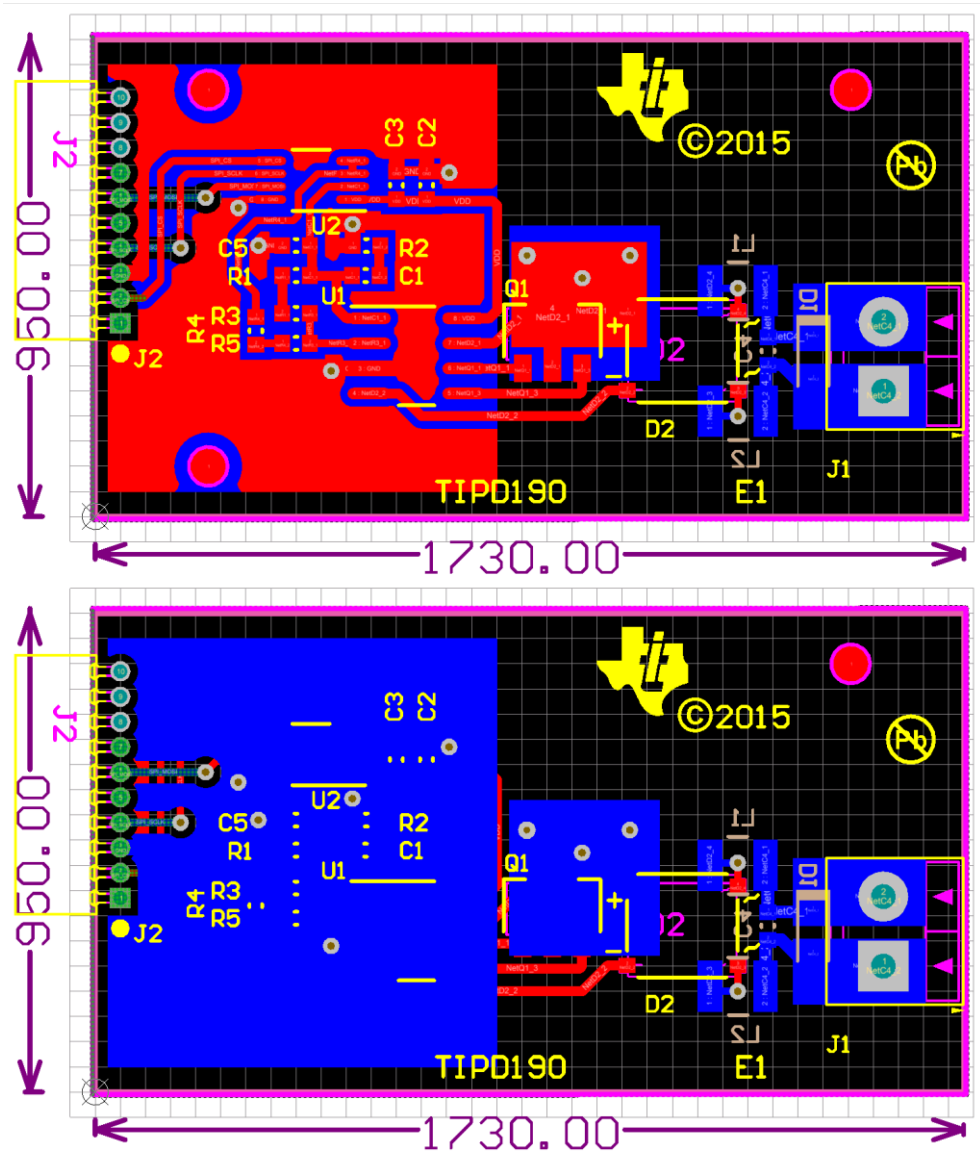

Figure 7: PCB Layout

6 Verification & Measured Performance

DC transfer function data for the system current output was collected using an 8 ½ digit digital multi-meter while driving a 250 Ω load with 24 V loop supply voltage. The measured results, including end-point performance, are shown in Figure 8.

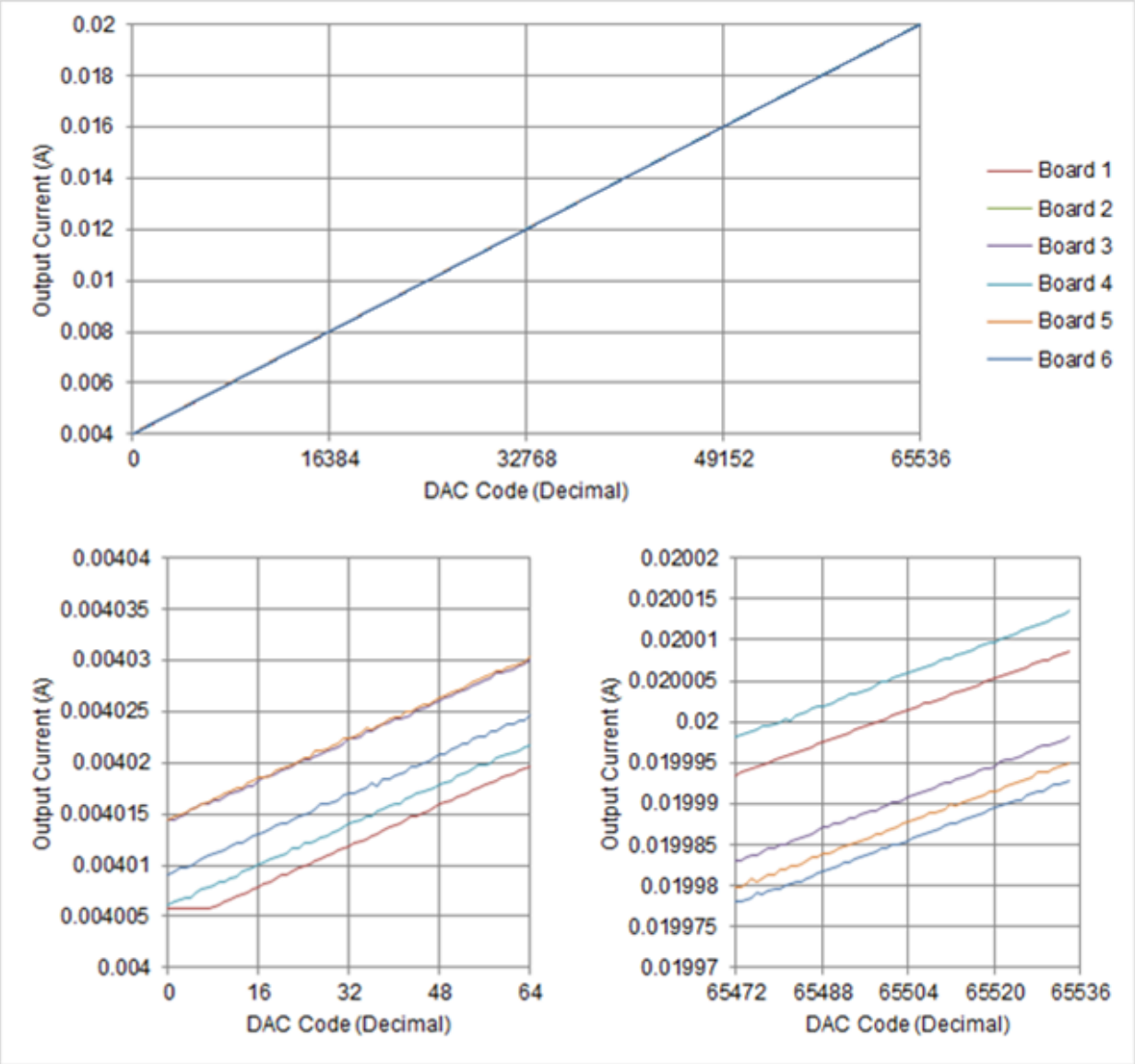

Figure 8: Output Current vs. Input Code

In order to better understand system performance, the calculated total unadjusted output current error in % FSR is shown in Figure 9. Additionally, the measured INL is shown in Figure 10.

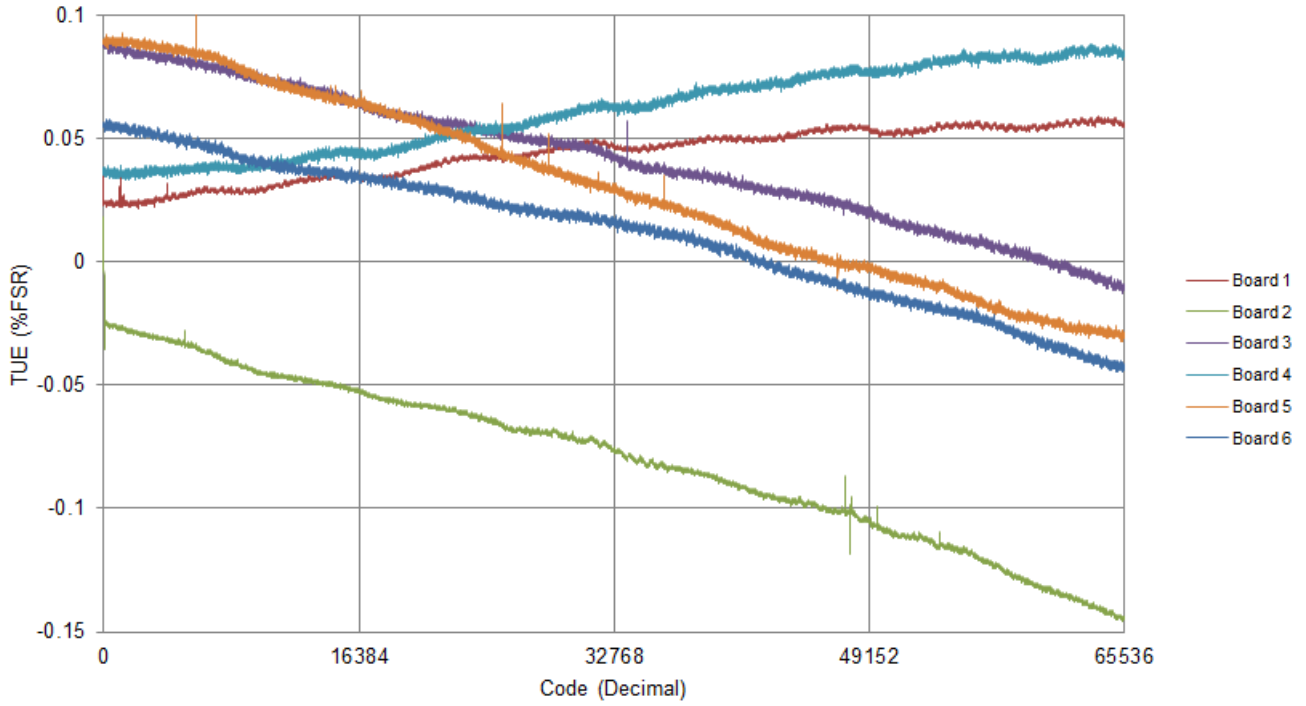

Figure 9: Output Current TUE vs. Input Code

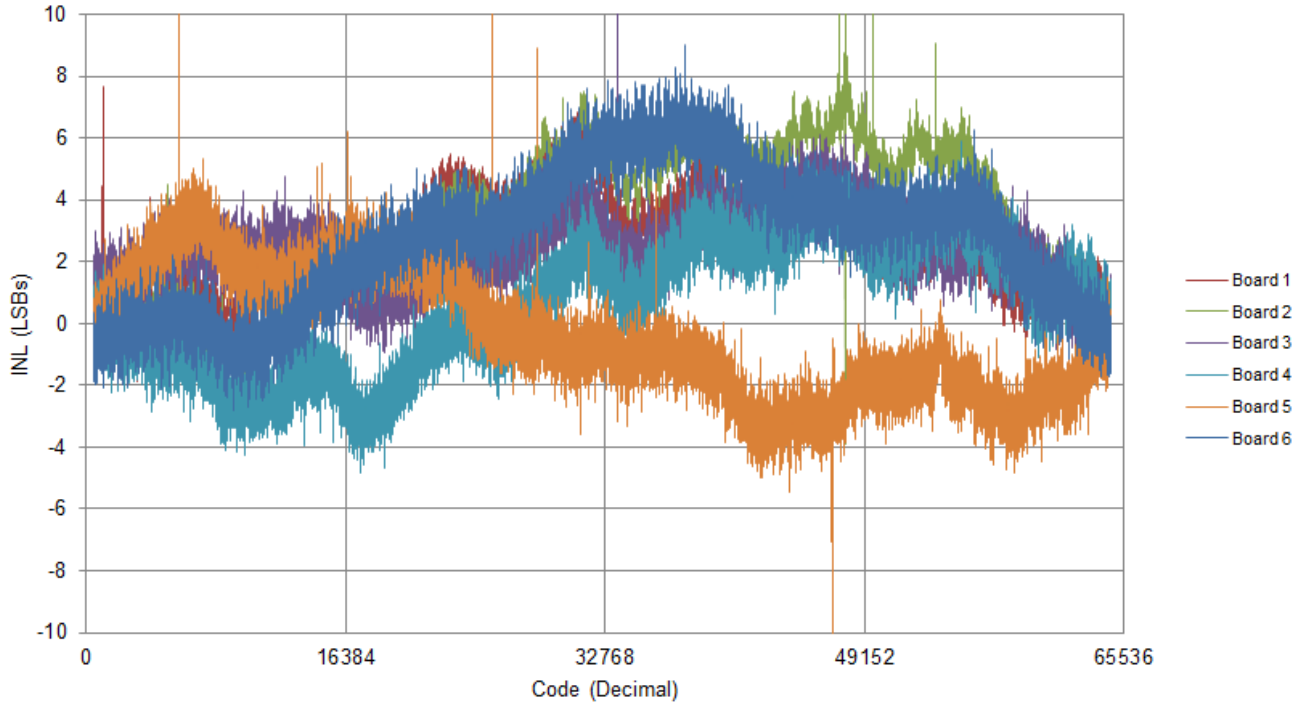

Figure 10: Output Current INL vs. Input Code

6.1 Measured Results Summary

The accuracy goals, simulated results, and measured performance for output current TUE are summarized in Table 8. Measured results are well aligned with the calculated typical and calculated maximum values.

Table 8. Measured Results

Parameter	Measured Results	Calculated Typical	Calculated Maximum	Goal
Linearity Error (%FSR)	0.0122	0.0047	0.0158	n/a
Offset Error (%FSR)	0.0885	0.0511	0.3009	n/a
Gain Error (%FSR)	0.1192	0.0813	0.3939	n/a
TUE (%FSR)	0.1420	0.0962	0.4959	0.5000

7 Certification Testing Results

Class A performance for this EUT will be assigned for outputs that stay within 0.5% FSR of their intended value, during exposure to each IEC61000-4 disturbance. The output was configured to a 12mA static dc level before the tests and the input was not changed while the tests were active. The IEC61000-4 certifications do not specify what supporting equipment is used to monitor the output of the EUT. For this design, an Agilent 34401A 6.5 digit digital multi-meter with resolution set to fast 5.5 digit mode was selected to monitor the output current.

7.1 IEC61000-4-2: ESD (Electrostatic Discharge)

ESD tests were conducted at ±8 kV for the contact and vertical and horizontal coupling planes. The threat level was set to ±15 kV for air discharge. ESD had minimal effect on the output current. During and after the tests the output stayed within 0.5% FSR of the output value. Table 9 summarizes the results of the ESD tests. Figure 11 through Figure 13 show the output during each test.

Table 9. IEC61000-4-2 Results

Test	Level	Result	Class
Horizontal Coupling Plane	8kV	Pass	A
Vertical Coupling Plane	8 kV	Pass	A
Contact	8 kV	Pass	A
Air Discharge	15 kV	Pass	A

7.1.1 I_{OUT} ESD Results

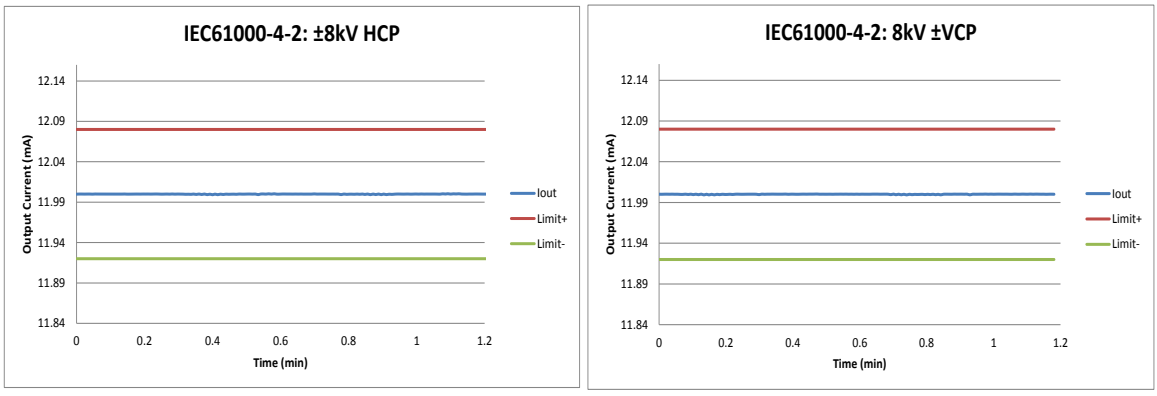

Figure 11: ±8 - kV ESD Horizontal (left) and Vertical (right) Coupling Planes (HCP and VCP)

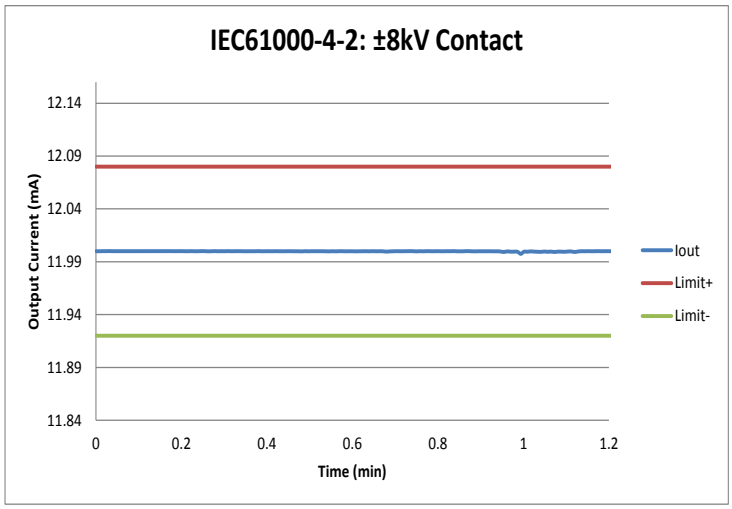

Figure 12: ±8kV Contact Discharge

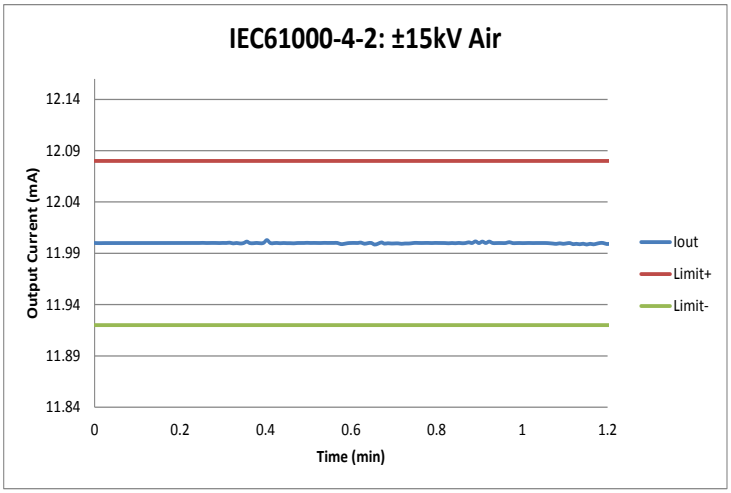

Figure 13: ±15 kV ESD Air Discharge

7.2 IEC61000-4-3: RI (Radiated Immunity)

Exposure to radiated emissions with field strengths up to 20V/m had minimal impact on the output resulting in a class A rating for these tests. Table 10 summarizes the results of each test and Figure 14 shows the output during each test.

Table 10. IEC61000-4-3 Results

Antennae Orientation	Level	Result	Class
Horizontal and Vertical	20 V/m	Pass	A

7.2.1 I_{OUT} RI Results

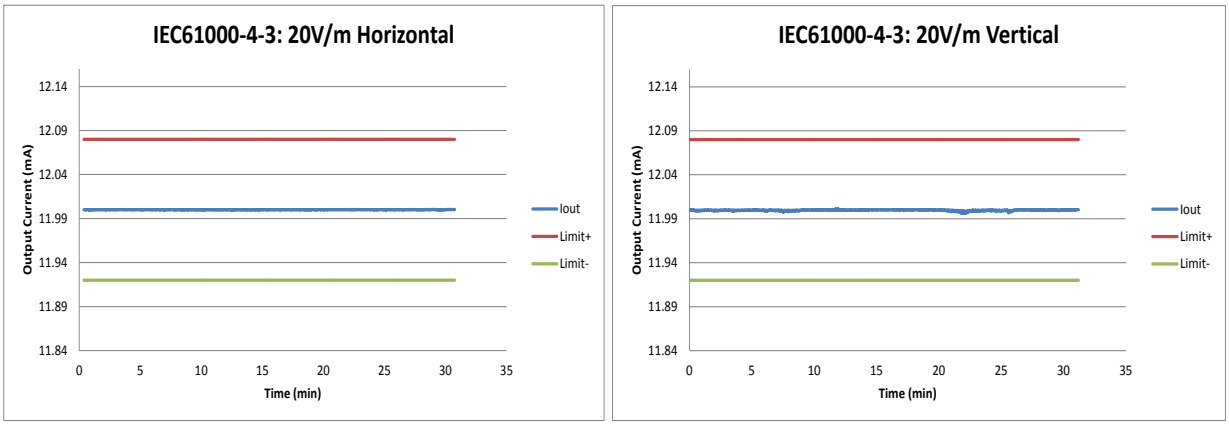

Figure 14: Horizontal (left) and Vertical (right) Polarity at 20V/m

7.3 IEC61000-4-4: EFT (Electrically Fast Transient)

The electrical fast transient bursts had a measurable effect on the output current at ±4kV, but almost no effect at ±2kV. Neither threat level resulted in deviations outside of the 0.5% limit resulting in a Class A rating. After testing was complete normal functionality was restored. Table 11 summarizes the results of each test. Figure 15 and Figure 16 show the output during each test.

Table 11. IEC61000-4-4 Results

Level	Result	Class
± 2 kV	Pass	A
± 4 kV	Pass	A

7.3.1 I_{OUT} EFT Results

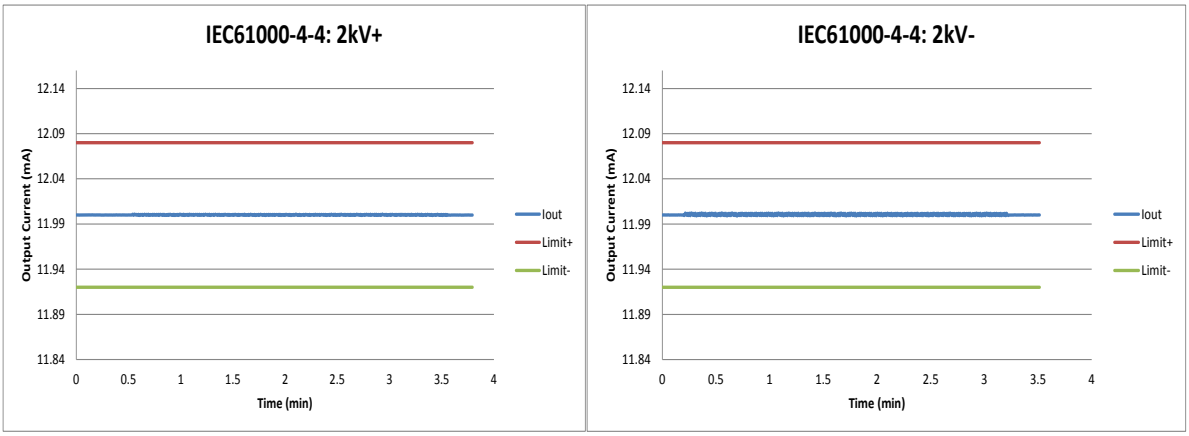

Figure 15: 2kV EFT Positive (left) and Negative (right)

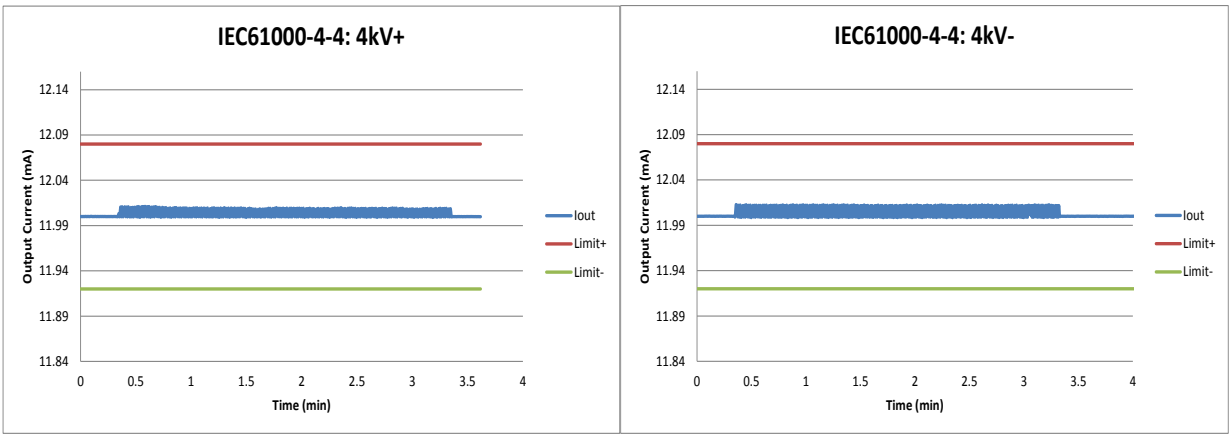

Figure 16: 4kV EFT Positive (left) and Negative (right)

7.4 IEC61000-4-6: CI (Conducted Immunity)

The conducted immunity tests resulted in minimal deviations in the output current resulting in a Class A rating for these tests. The results are summarized in Table 12. Figure 17 shows the behavior of the output during exposure to the CI test.

Table 12. IEC61000-4-6 Results

Result	Class
Pass	A

7.4.1 I_{OUT} CI Results

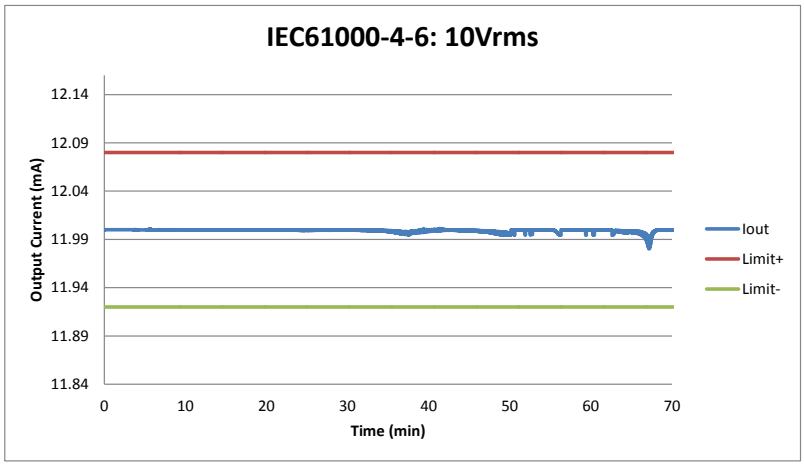

Figure 17: 10 Vrms Conducted Immunity Results

8 Modifications

2-wire sensor transmitters are often designed with 16-bits or 12-bits of resolution with varying accuracy. There are several alternative DACs that would fit well in a 2-wire loop powered transmitter from Texas Instruments, some of these devices are listed in Table 13.

Table 13. Alternate DACs

Device	Resolution	Offset Error (Typ)	Gain Error (Typ)	DNL Error (Typ)	INL Error (Typ)
DAC7311	12-bits	0.05 mV	0.05% FSR	0.2 LSBs	0.3 LSBs
DAC7551	12-bits	12 mV	0.15% FSR	0.08 LSBs	0.35 LSBs
DAC8411	16-bits	0.05 mV	0.05% FSR	0.5 LSBs	4 LSBs
DAC8551	16-bits	2 mV	0.02% FSR	0.25 LSBs	3 LSBs
DAC8830	16-bits	n/a*	0.0015% FSR	0.5 LSBs	0.5 LSBs

*DAC8830 is an unbuffered R-2R DAC, with no output amplifier there is no offset error specification

Similarly there are a few other 2-wire transmitter integrated circuits similar to the XTR116 that would fit well into this design. They are listed in Table 14.

Table 14. Alternate XTRs

Device	Regulator Voltage	Reference Voltage	Offset Error (Typ)	Gain Error (Typ)	Linearity Errors (Typ)
XTR116	5 V	4.096 V	0.1 mV	0.05% FSR	0.003% FSR
XTR115	5 V	2.5 V	0.1 mV	0.05% FSR	0.003% FSR
XTR117	5 V	N/A	0.1 mV	0.05% FSR	0.003% FSR

9 About the Authors

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Masaharu Takahashi is a Field Applications Engineer in Nagoya, Japan supporting industrial and other high performance analog customers. He completed work on this system during a 6-month rotation working with the Precision Digital to Analog Converters team in Dallas, Texas.

10 Acknowledgements & References (if applicable)

The author wishes to acknowledge NTS (National Technical Systems) in Plano, TX for their assistance performing the electromagnetic compatibility tests.

1. *IEC Publication 61000-4-2 "Electromagnetic Compatibility (EMC) – Part 4-2: Testing and Measurement Techniques – Electrostatic Discharge Immunity Test," International Electrotechnical Commission, 2008.*

2. *IEC Publication 61000-4-3 "Electromagnetic Compatibility (EMC) – Part 4-3: Testing and Measurement Techniques – Radiated, Radio-Frequency, Electromagnetic Field Immunity Test," International Electrotechnical Commission, 2006.*

3. *IEC Publication 61000-4-4 "Electromagnetic Compatibility (EMC) – Part 4-4: Testing and Measurement Techniques – Electrical Fast Transient/Burst Immunity Test," International Electrotechnical Commission, 2012.*

4. *IEC Publication 61000-4-6 "Electromagnetic Compatibility (EMC) – Part 4-6: Testing and Measurement Techniques – Immunity to Conducted Disturbances, Induced by Radio-Frequency Fields," International Electrotechnical Commission, 2008.*

5. *IEC Publication 61000-4-5 "Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test," International Electrotechnical Commission, 2012.*

6. *H. Ott, Electromagnetic Compatibility. John Wiley & Sons Inc., 2009.*

7. *Electromagnetic Compatibility. John Wiley & Sons Inc., 2009.*

A.1 Electrical Schematic

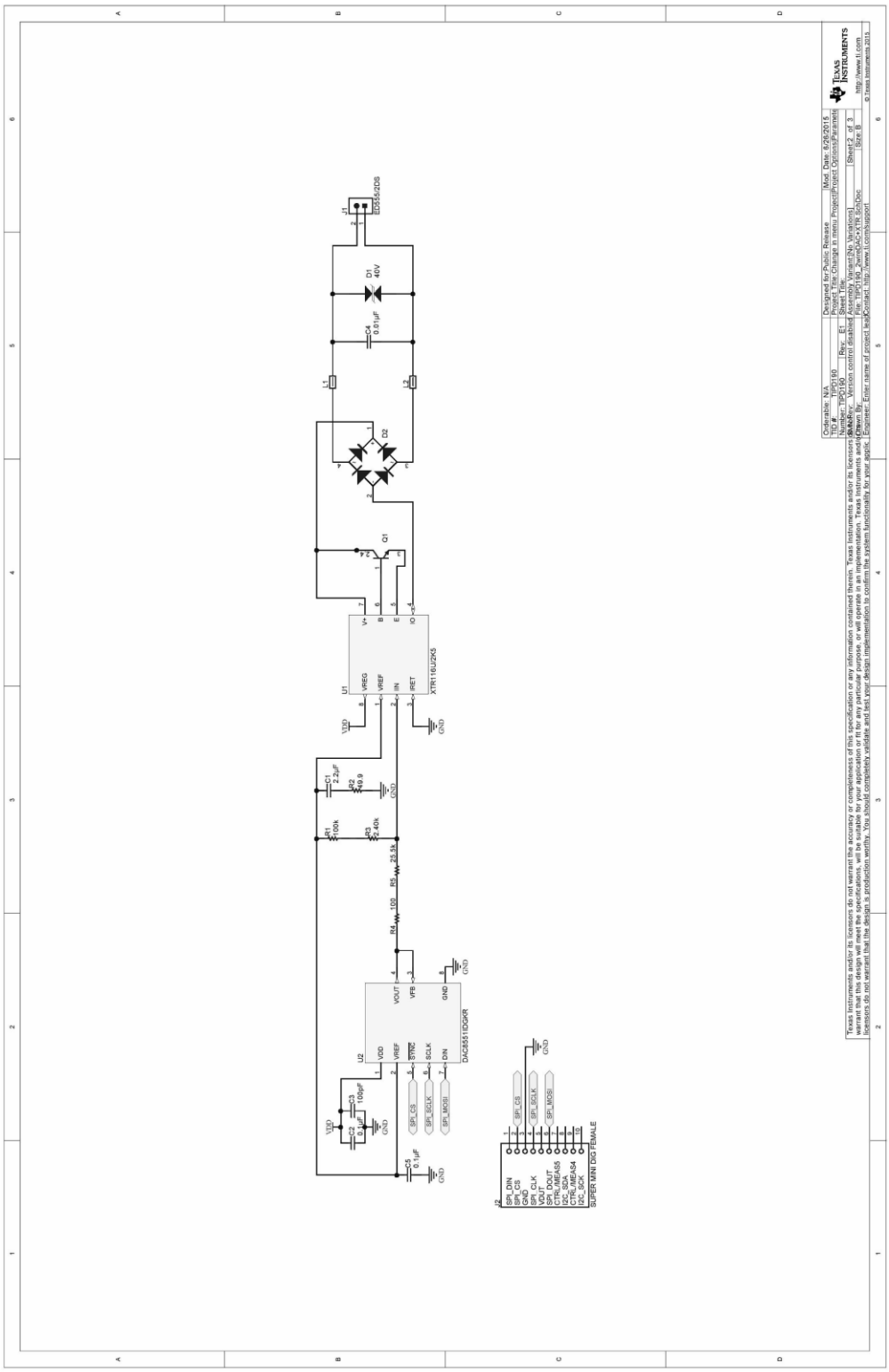

Figure A-1: Electrical Schematic

A.2 Bill of Materials

TEXAS INSTRUMENTS

Bill of Materials

TI DESIGNS
TIPD190: 2-wire 4-20mA Transmitter, EMC/EMI Tested

Item	Designator	Quantity	Value	Description	Manufacturer	Part Number
1	C1	1	2.2uF	CAP, CERM, 2.2 µF, 10 V, +/- 10%, X7R, 0603	MuRata	GRM188R71A225KE15D
2	C2, C5	2	0.1uF	CAP, CERM, 0.1 µF, 100 V, +/- 10%, X7R, 0603	MuRata	GRM188R72A104KA35D
3	C3	1	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	MuRata	GRM1885C1H101JA01D
4	C4	1	0.01uF	CAP, CERM, 0.01 µF, 100 V, +/- 10%, X7R, 0603	MuRata	GRM188R72A103KA01D
5	D1	1	40V	TVS DIODE 36VWM 60VC SOD323	Bourns Inc	CDSOD323-T36SC
6	D2	1	1000V	Diode, Switching-Bridge, 1000V, 1A, 5.0x1.21x6.2mm	Diodes Inc.	DSRHD10-13
7	J1	1		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS
8	J2	1		Receptacle, 50mil 10x1, R/A, TH	Mill-Max	851-43-010-20-001000
9	L1, L2	2	2000 ohm	Ferrite Bead, 2000 ohm @ 100 MHz, 1.2 A, 1210 (H=2.5mm)	Taiyo Yuden	FBMH3225HM202NT
10	Q1	1	0.08V	Transistor, NPN, 45V, 1A, SOT-89	Diodes Inc.	FCX690BTA
11	R1	1	100k	RES, 100 k, 0.1%, 0.1 W, 0603	Panasonic	ERA-3AEB104V
12	R2	1	49.9	RES, 49.9, 1%, 0.1 W, 0603	Vishay-Dale	CRCW060349R9FKEA
13	R3	1	2.40k	RES, 2.40 k, 0.1%, 0.1 W, 0603	Panasonic	ERA-3AEB242V
14	R4	1	100	RES, 100, 0.1%, 0.1 W, 0603	Panasonic	ERA-3AEB101V
15	R5	1	25.5k	RES, 25.5 k, 0.1%, 0.1 W, 0603	Panasonic	ERA-3AEB2552V
16	U1	1		4-20mA CURRENT LOOP TRANSMITTERS, D0008A	Texas Instruments	XTR116U/2K5
17	U2	1		16-BIT, ULTRA-LOW GLITCH, VOLTAGE OUTPUT DIGITAL-TO-ANALOG CONVERTER, DGK0008A	Texas Instruments	DAC8551IDGKR

Figure A-2: Bill of Materials

Appendix B.

B.1 IEC61000-4 Photos

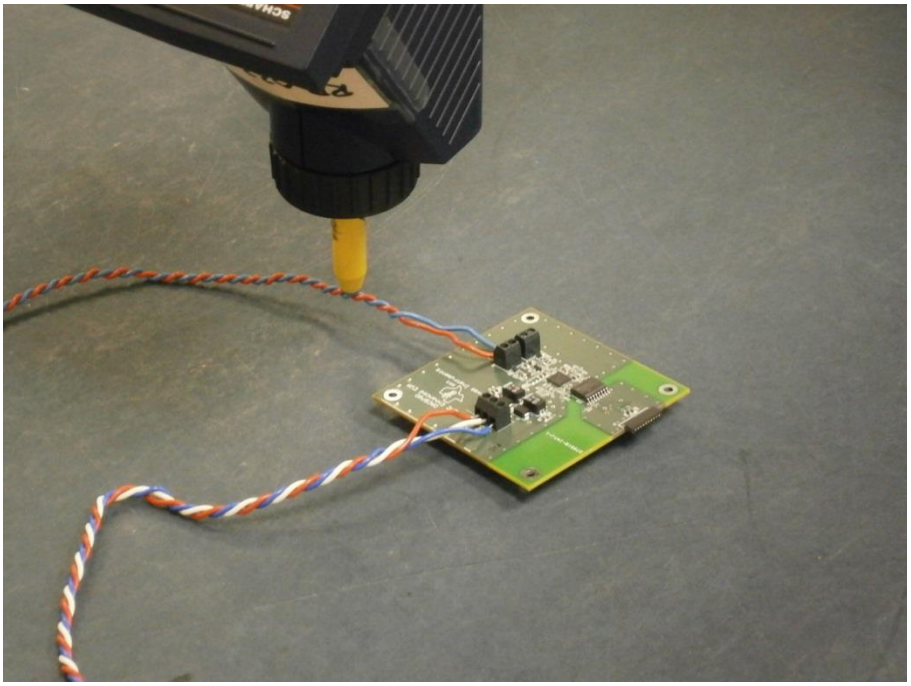

Figure B-1: 15kV ESD Air Discharge

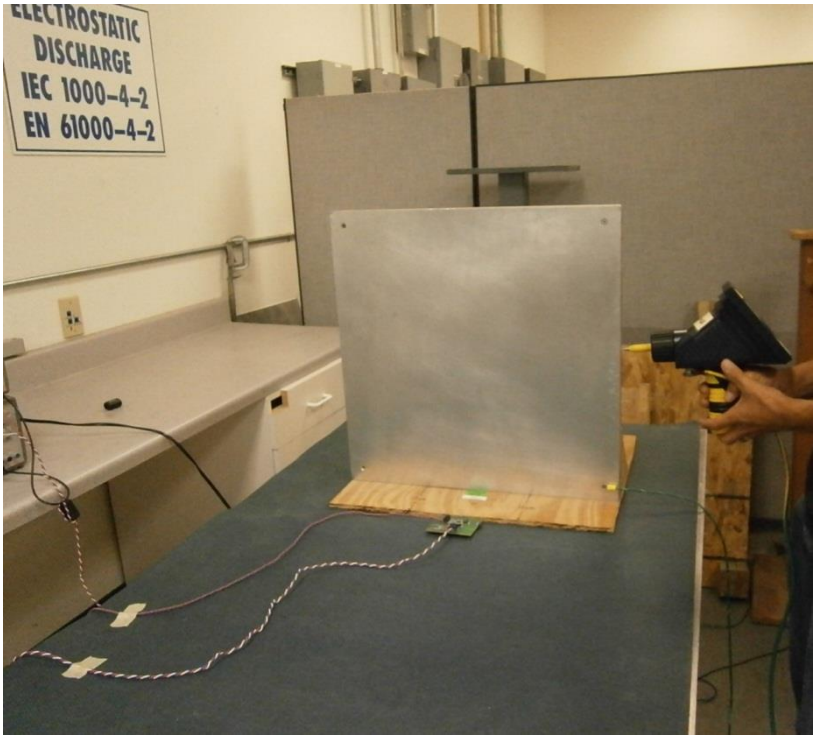

Figure B-2: 8kV ESD Vertical Contact Discharge

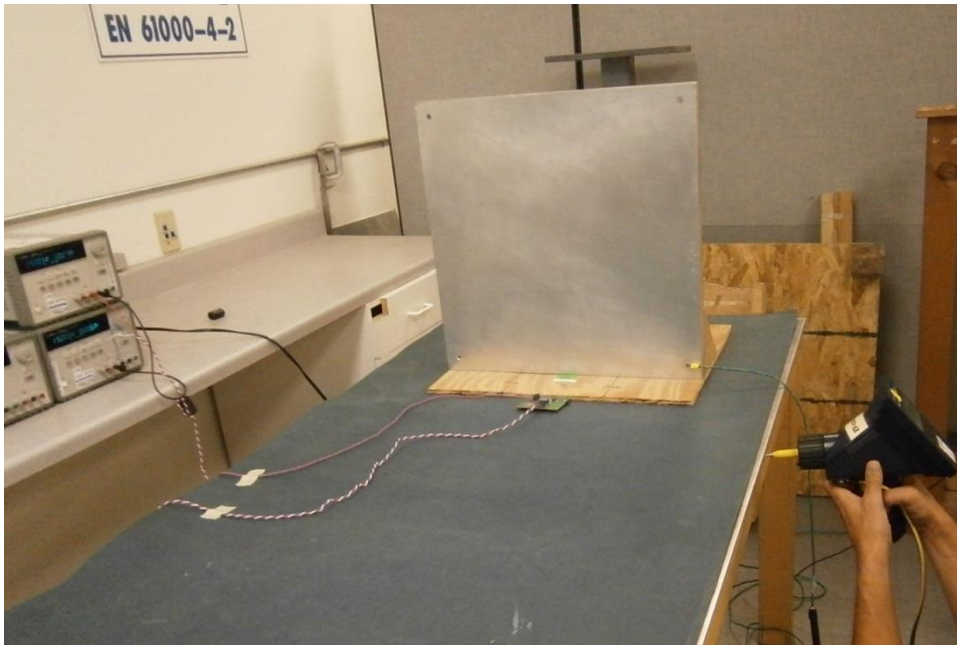

Figure B-3: 8kV ESD Horizontal Contact Discharge

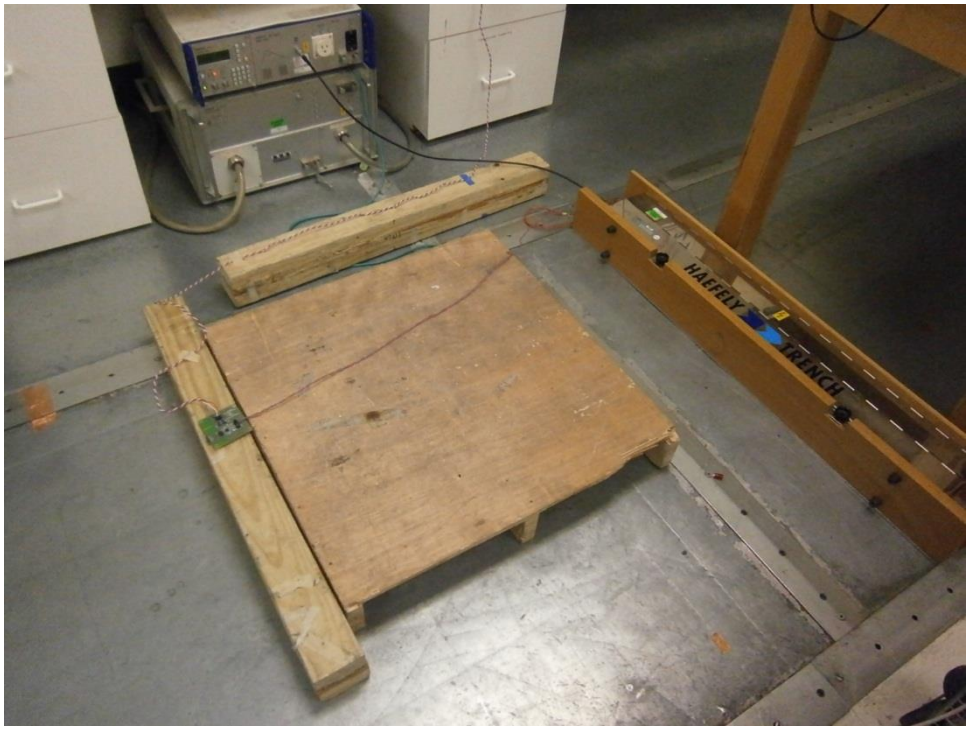

Figure B-4: EFT Test Setup

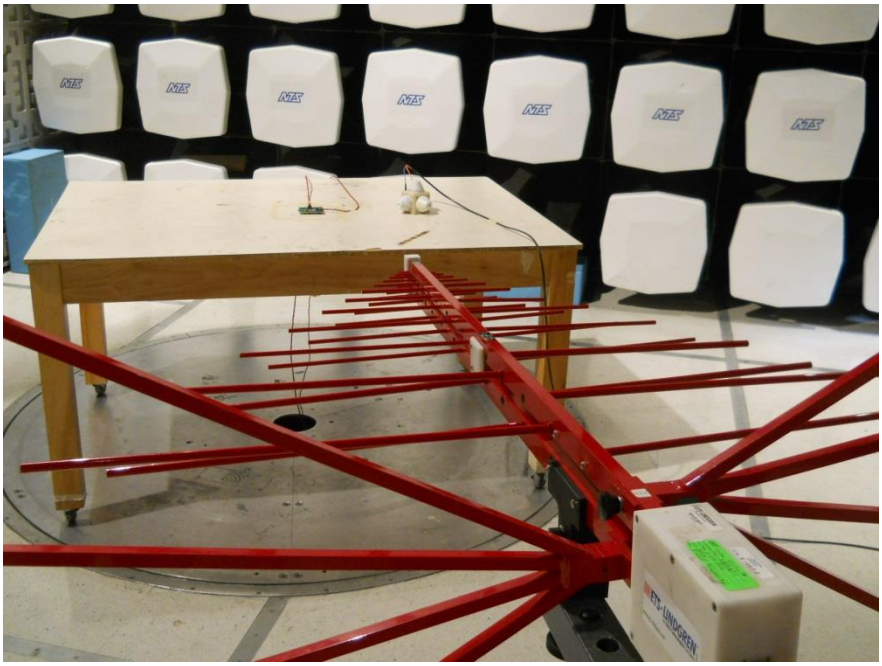

Figure B-5: Horizontal Radiated Immunity

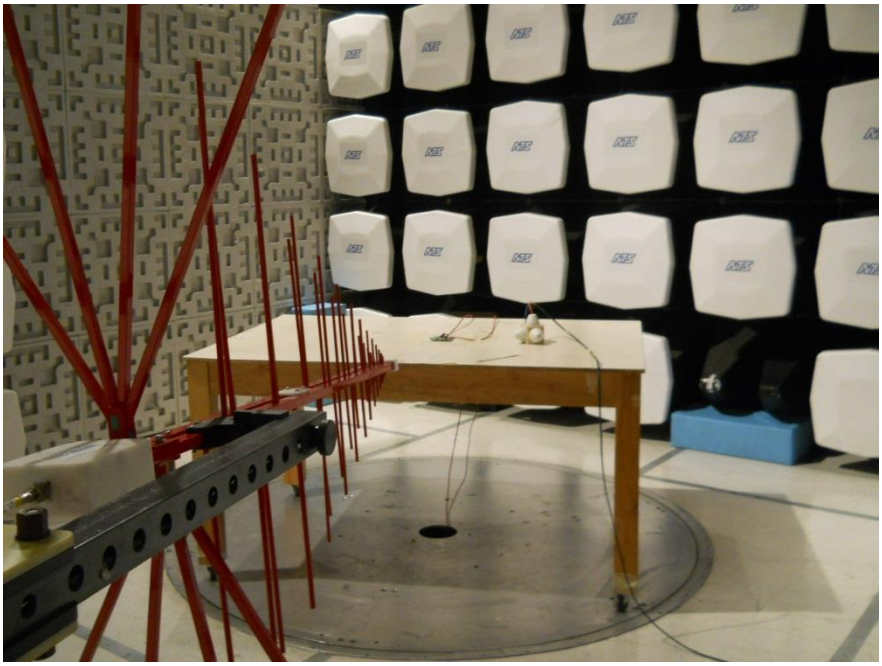

Figure B-6: Vertical Radiated Immunity

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