TIDA-00716 Test Report
Xilinx® Spartan® 6 Power Reference Design with TPS650250 Power Management IC

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TPS650250EVM-447	Tools Folder

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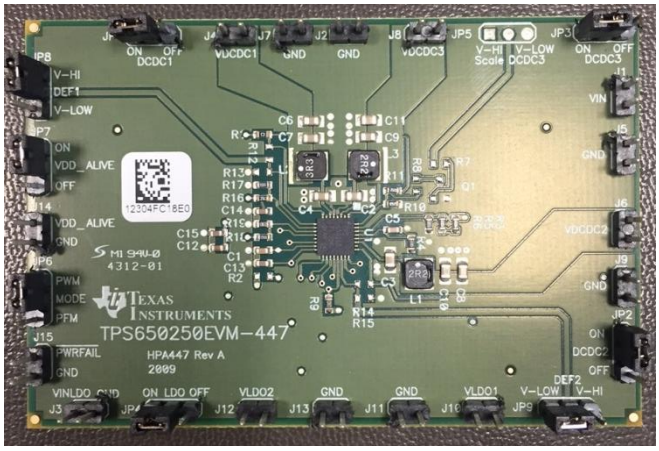

Figure 1 - Top Side

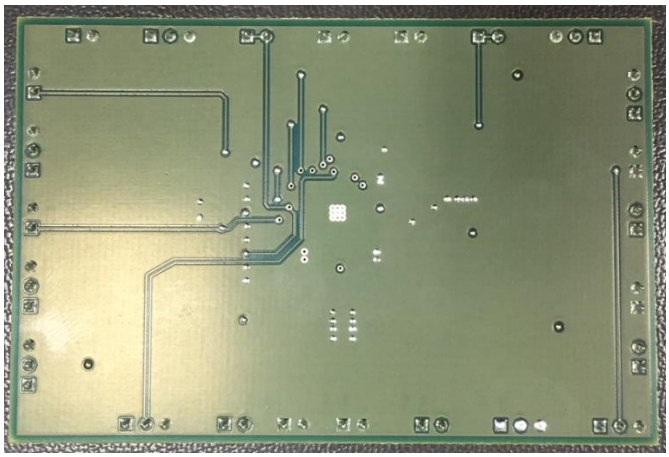

Figure 2 - Bottom Side

Report Contents

Feature Applications

- Video Surveillance
- Flat-Panel Displays
- Audio
- Medical Devices

Description

The TIDA-00716 design is a compact, integrated solution for the Xilinx Spartan 6 FPGA. This design showcases the TPS650250 as an all-in-one IC used to supply the rails needed for powering the Spartan 6. This design is based on the Spartan 6 LXT family, but can be repurposed to power the Spartan 6 LX family. With user controlled external sequencing, separate enables and external resistor dividers, the TPS650250 offers a simple and flexible solution that can be leveraged across multiple designs across the Spartan 6 family. This power management IC has an input voltage range between

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3.5 and 5.5V and can be run from a 5V supply or a single cell Li-Ion battery. This design has been tested and verified for industrial applications (-40°C to 85°C).

TPS650250/Spartan 6 Block Diagram (Return to Top)

Power Supply Block Diagram

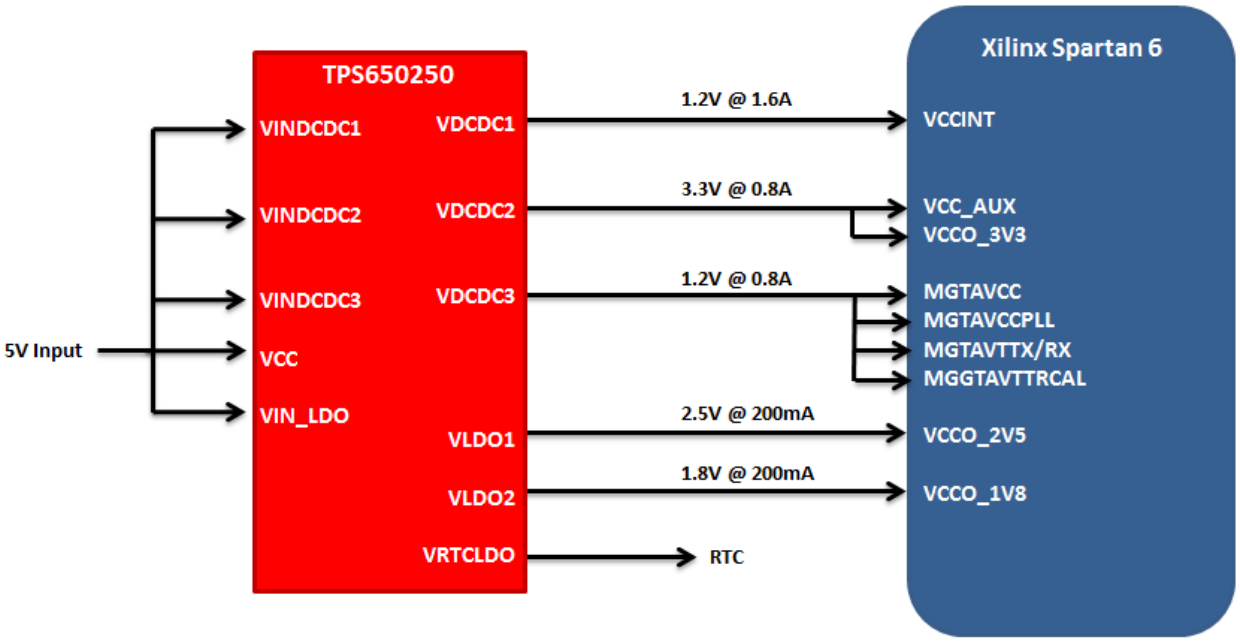

Figure 3 – Spartan 6 Block Diagram

Typical Voltage and Current Requirements in End Applications

Depending on application and design on FPGA, current consumption can vary. The table below highlights the typical max currents each power output of the TPS650250 converters to the rails of the Spartan 6 LXT. The rails in **BOLD** are specific to the Spartan 6 LXT family. VCCO can bet set to 1.2, 1.5, 2.5, 2.8 or 3.3V depending on application. These voltages can be set via an external resistor divider.

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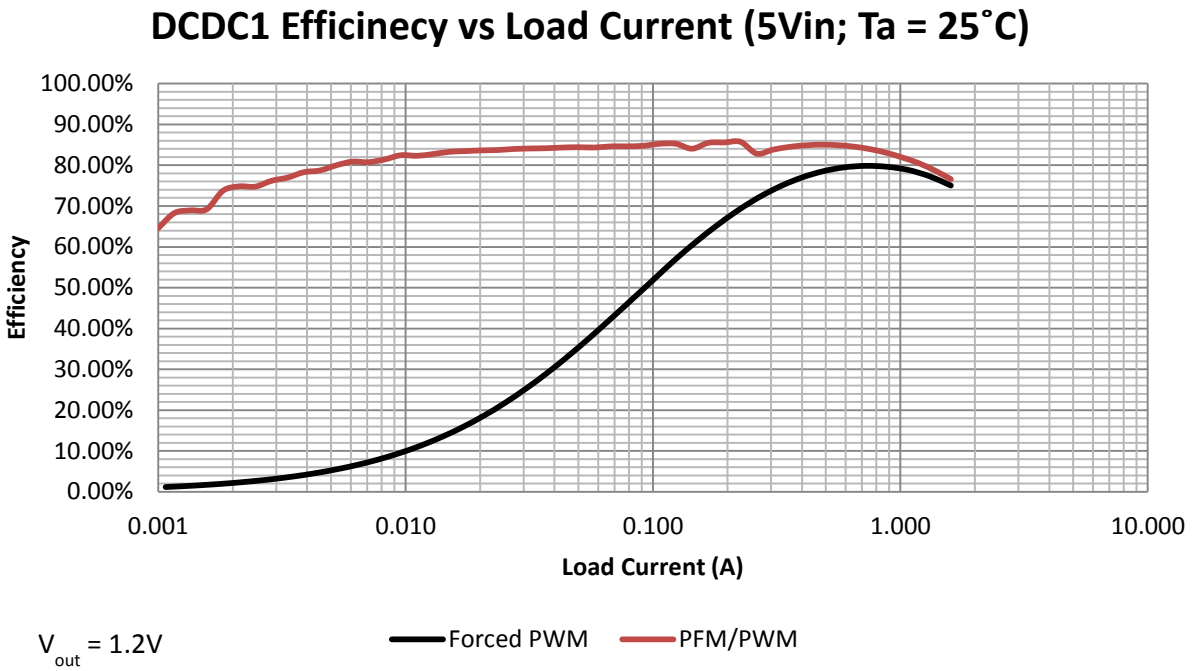
Spartan 6 Supply Rails	Voltage	Current Consumption (A)
VCC_INT	1.2V	1.6
VCC_AUX	3.3V	0.8
VCCO_2		
MGTAVCC	**1.2V**	**0.8**
MGTAVCCPLL		
MGTAVTTX/RX		
MGGTAVTTRCAL		
VCCO_1	1.2-3.3V	0.200
VCCO_3	1.2-3.3V	0.200

Note: *The current consumption numbers above are only estimates and the actual current consumption may vary depending on the application.*

Efficiency Curves (Return to Top)

DCDC1 (Vout=1.2V) – *VCC_INT*



V_{out} = 1.2V

Figure 4 - DCDC1 Efficiency @ 25C

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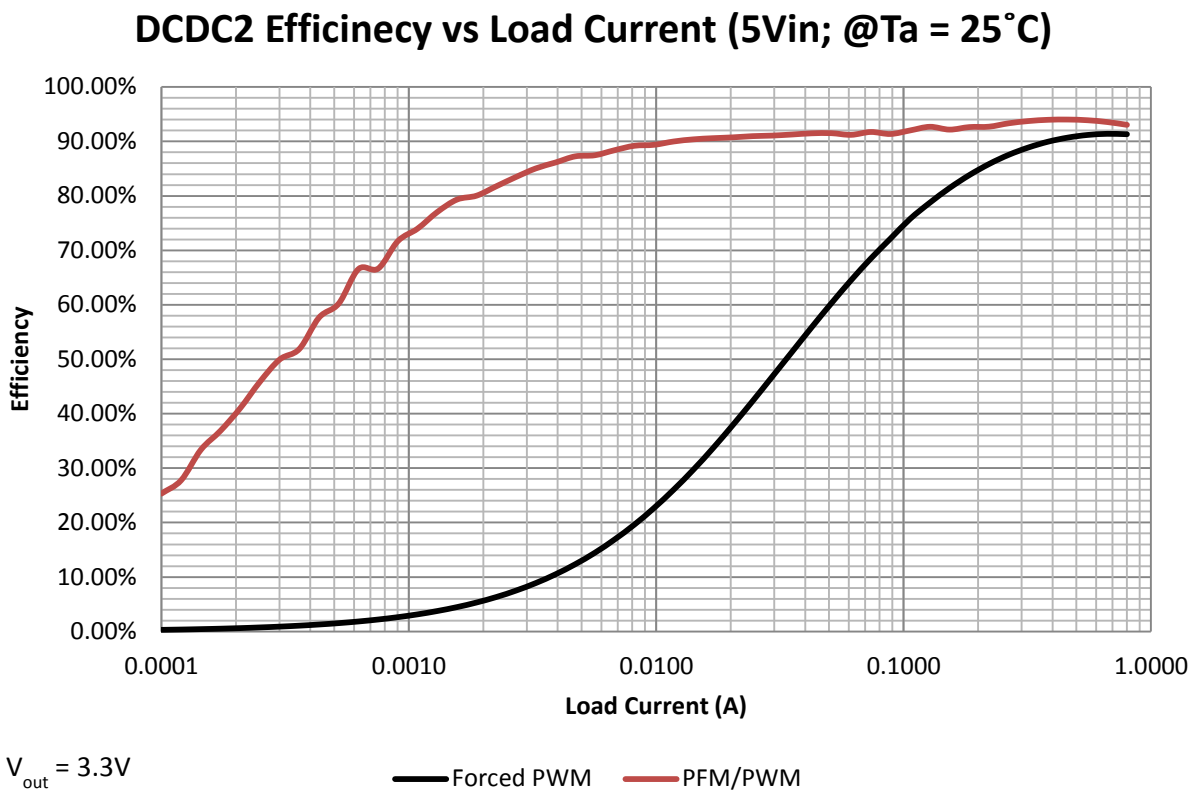
DCDC2 (Vout=3.3V) – VCC_AUX, VCCO_3V3



V_{out} = 3.3V

Figure 5 - DCDC2 Efficiency @ 25C

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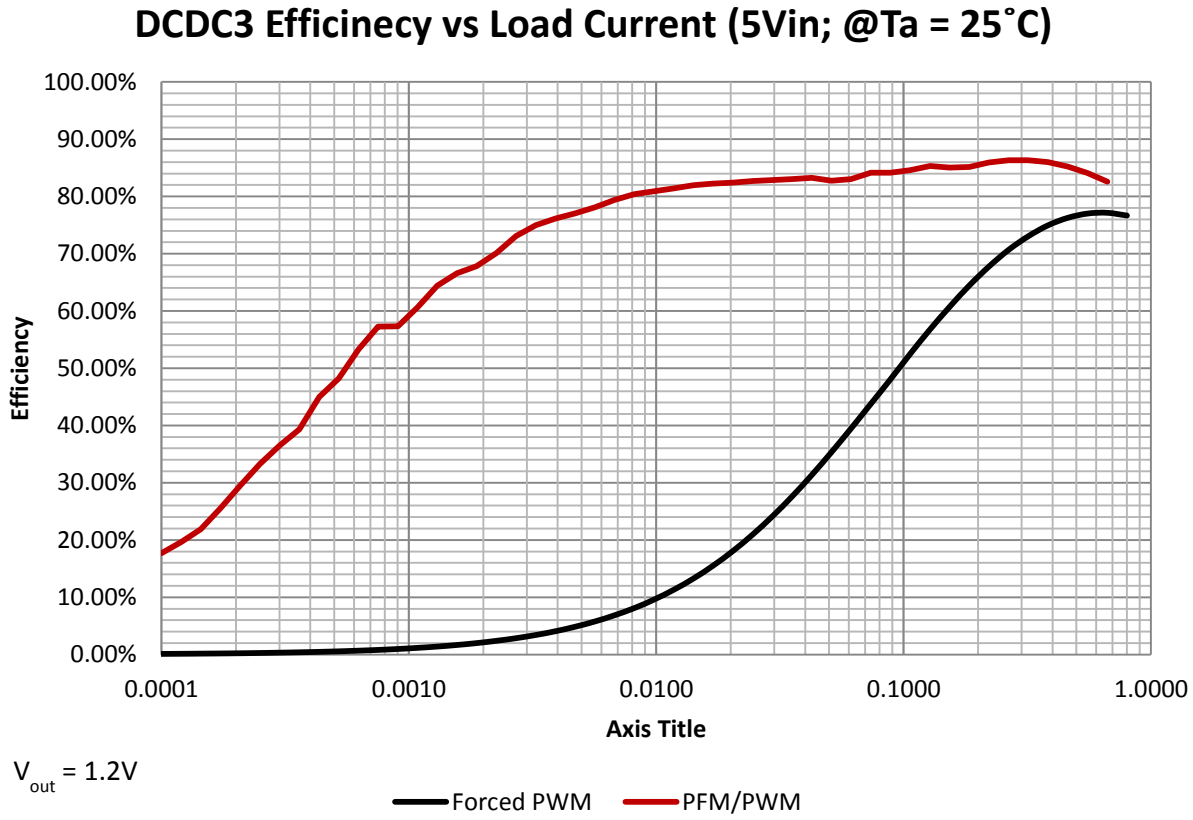
***DCDC3 (Vout=1.2V)* – MGTAVCC, MGTAVCCPLL, MGTAVTTX/RX, MGGTATTRCAL**



V_{out} = 1.2V

Figure 6 - DCDC3 Efficiency @ 25C

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Load Regulation (Return to Top)

DCDC1 (Vout=1.2V) – *VCC_INT*

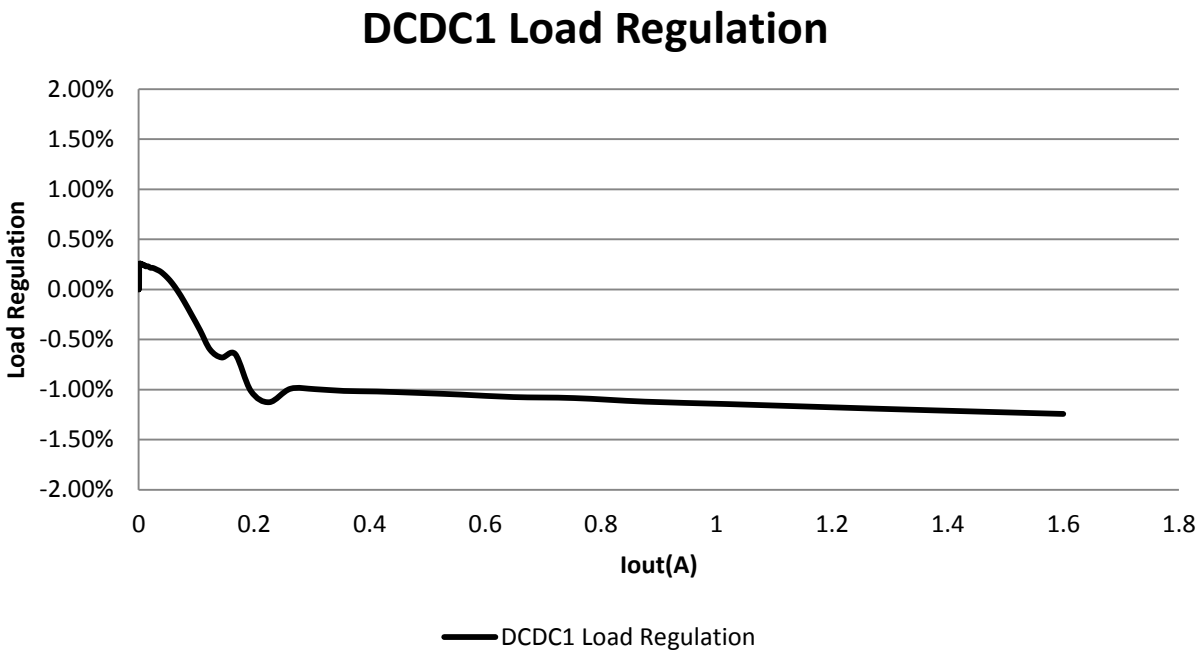

Figure 7 – DCDC1 Load Regulation @ 25C

DCDC2 (Vout=3.3V) – *VCC_AUX, VCCO_3V3*

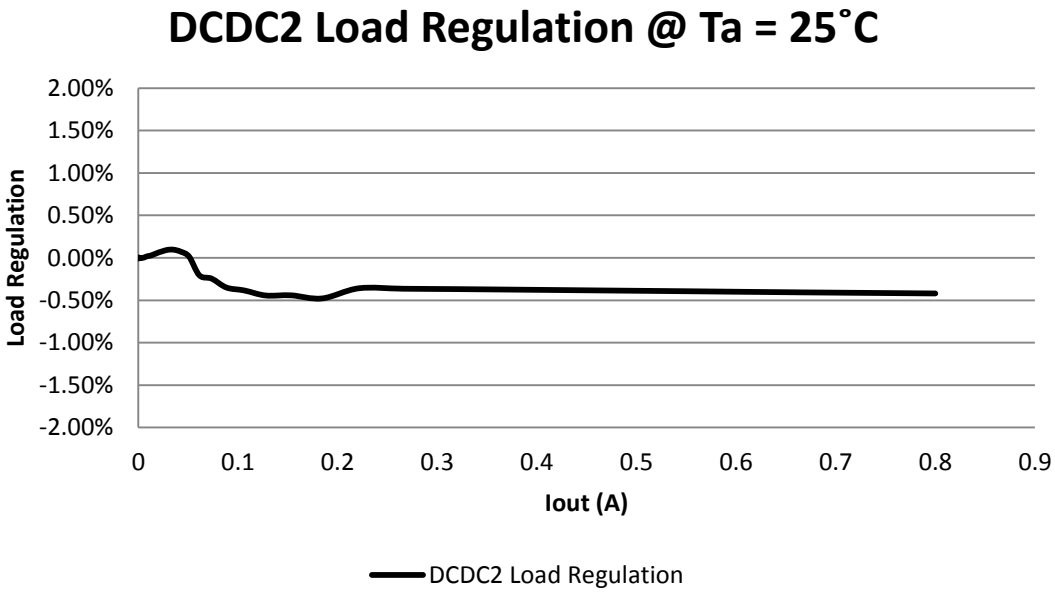

Figure 8 – DCDC2 Load Regulation @ 25C

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DCDC3 (Vout=1.2V) – *MGTAVCC, MGTAVCCPLL, MGTAVTTX/RX, MGGTATTRCAL*

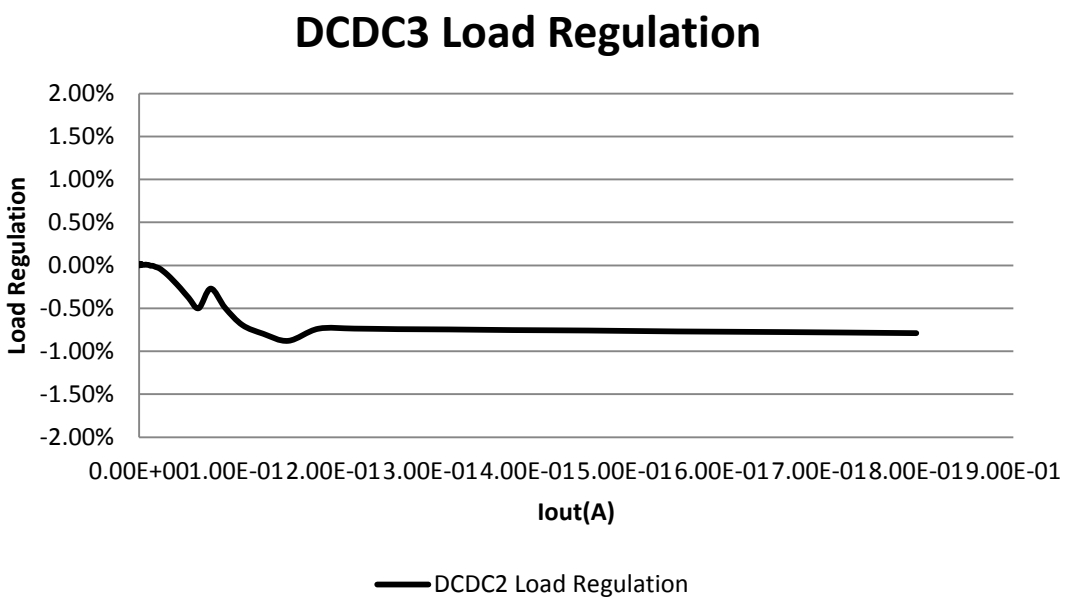

Figure 9 – DCDC3 Load Regulation @ 25C

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Output Ripple Voltage (Return to Top)

DCDC1 (Vout = 1.2V) – VCC_INT (Light Load, PFM Mode)

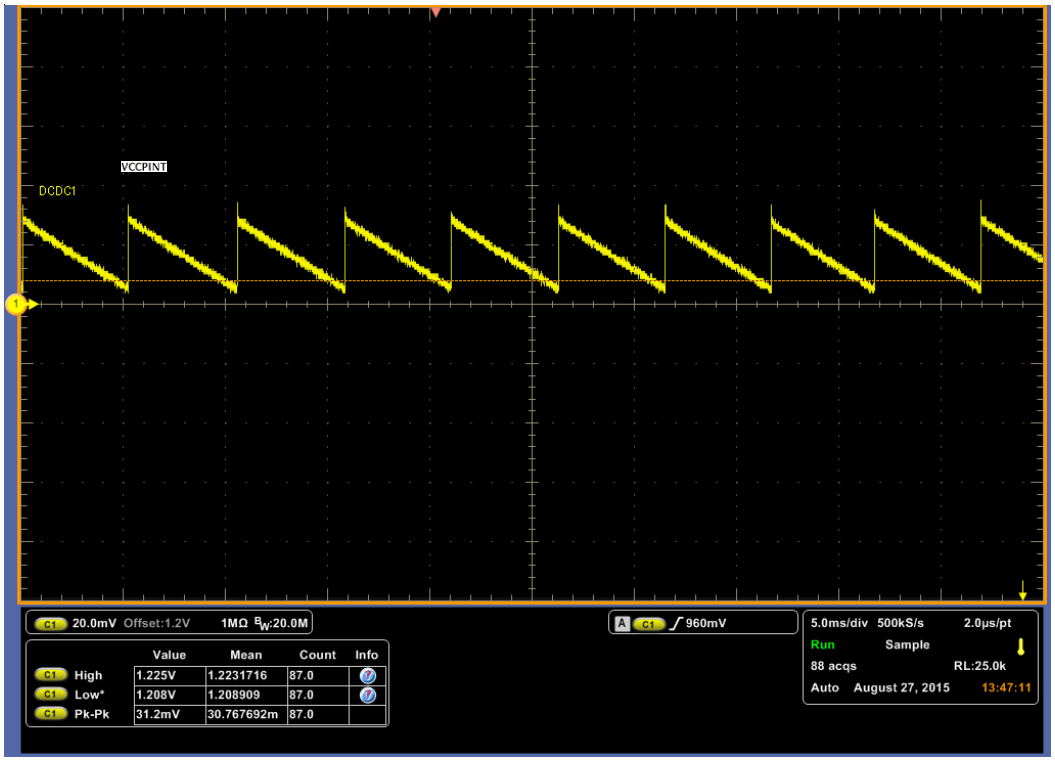

Figure 10 – DCDC1 Voltage Ripple, Light Load @ 25C

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DCDC1 (Vout = 1.2V) – VCC_INT (Max Typical Load)

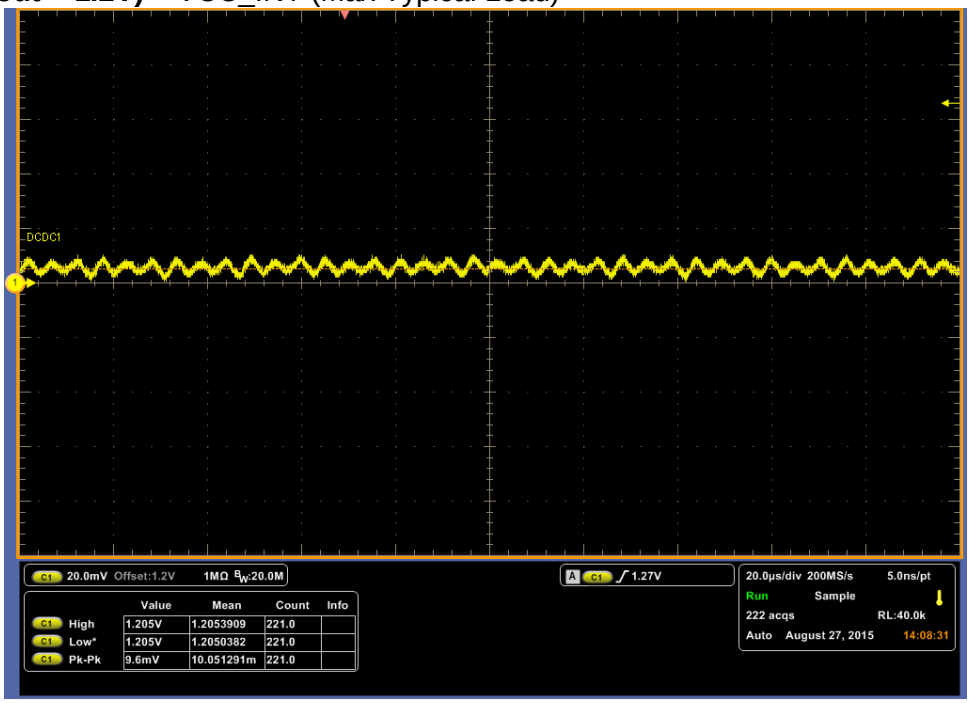

Figure 11 – DCDC1 Voltage Ripple, Max Load @ 25C

DCDC2 (Vout = 3.3V) – VCC_AUX, VCCO_3V3 (Light Load, PFM Mode)

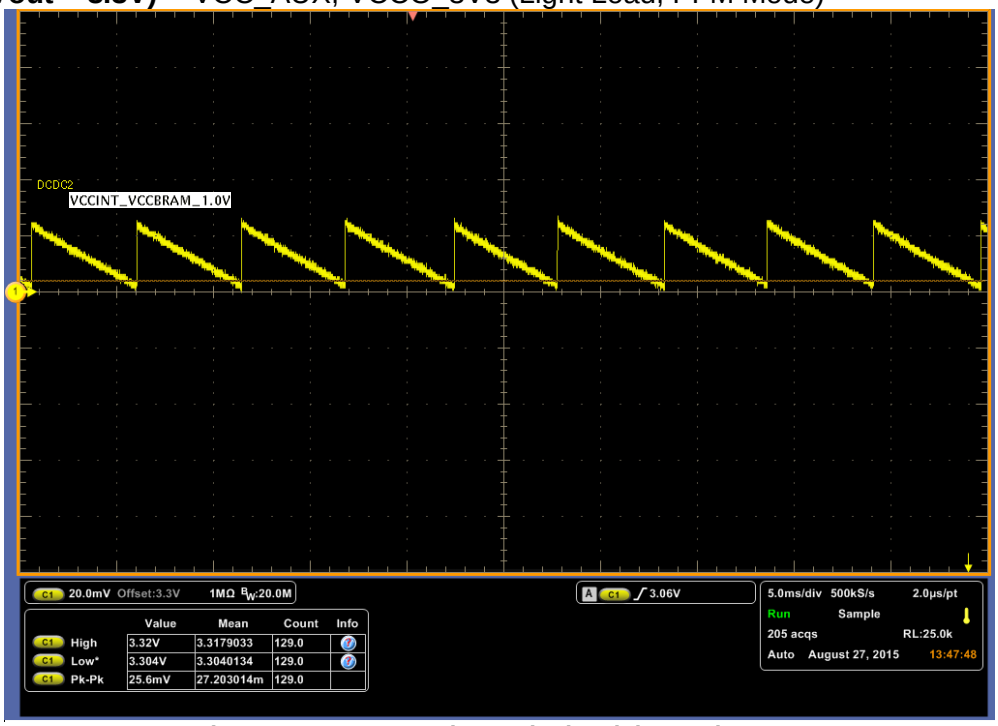

Figure 12 – DCDC2 Voltage Ripple, Light Load @ 25C

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DCDC2 (Vout = 3.3V) – VCC_AUX, VCCO_3V3 (Max Typical Load)

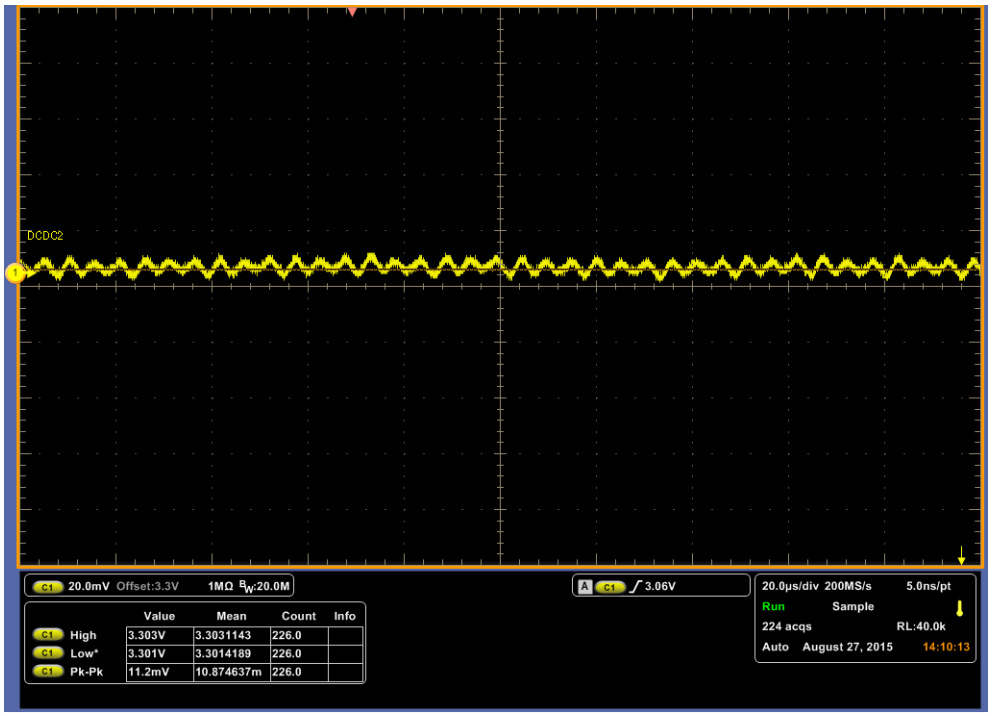

Figure 13 – DCDC2 Voltage Ripple, Max Load @ 25C

DCDC3 (Vout = 1.2V) – MGTAVCC, MGTAVCCPLL, MGTAVTTX/RX, MGGTATTRCAL (Light Load, PFM Mode)

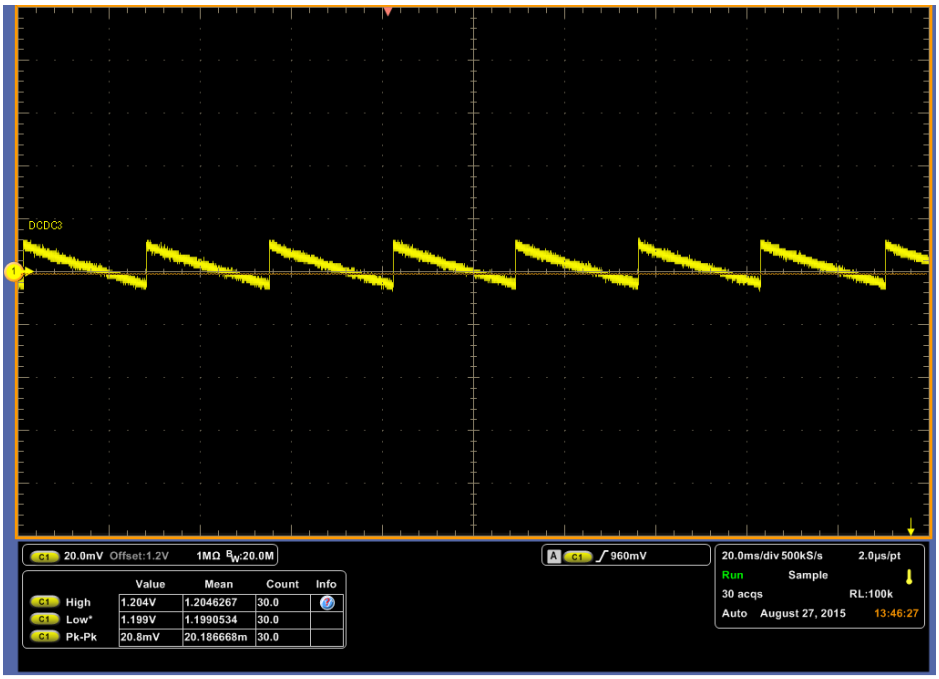

Figure 14 – DCDC3 Voltage Ripple, Light Load @ 25C

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DCDC3 (Vout = 1.2V) – MGTAVCC, MGTAVCCPLL, MGTAVTTX/RX, MGGTATTRCAL (Max Typical Load)

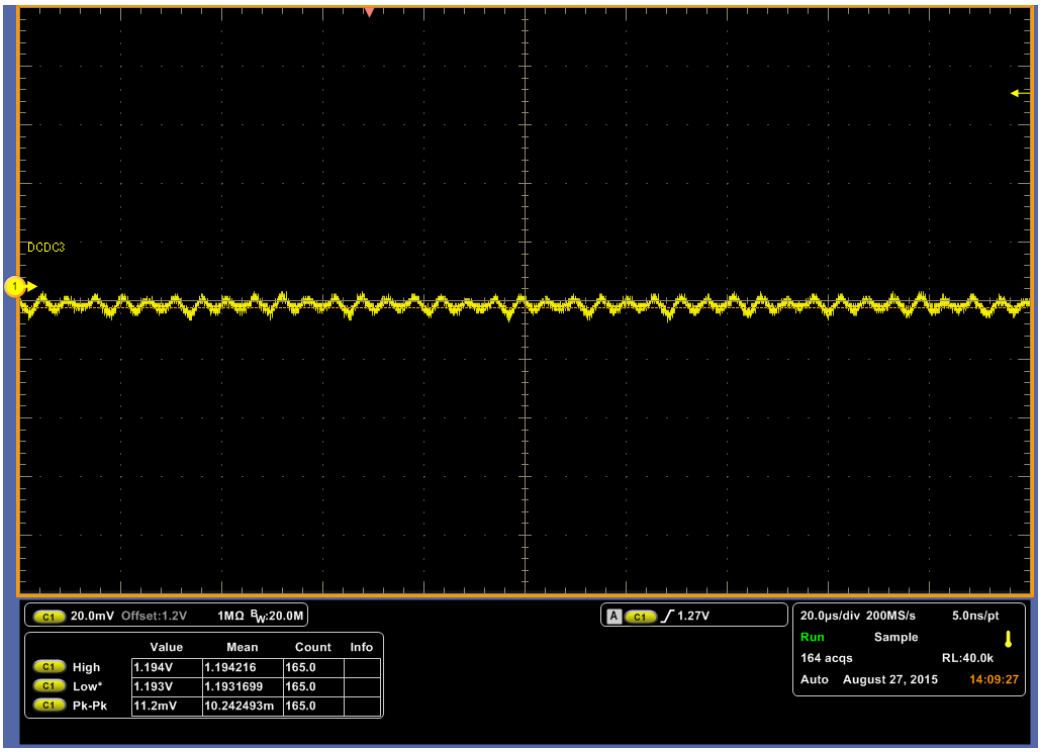

Figure 15 – DCDC3 Voltage Ripple, Max Load @ 25C

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Load Transients (Return to Top)

Load transients for each of the DC-DC converters were completed by applying a load step of 0mA to around 50% of the max load for the converter under test. The regulators surpass specifications set for the Xilinx Spartan Family.

DCDC1 (Vout = 1.2V) – VCC_INT Load Step (0mA to 850mA, Rise Time: 9µS; Fall Time:9µS)

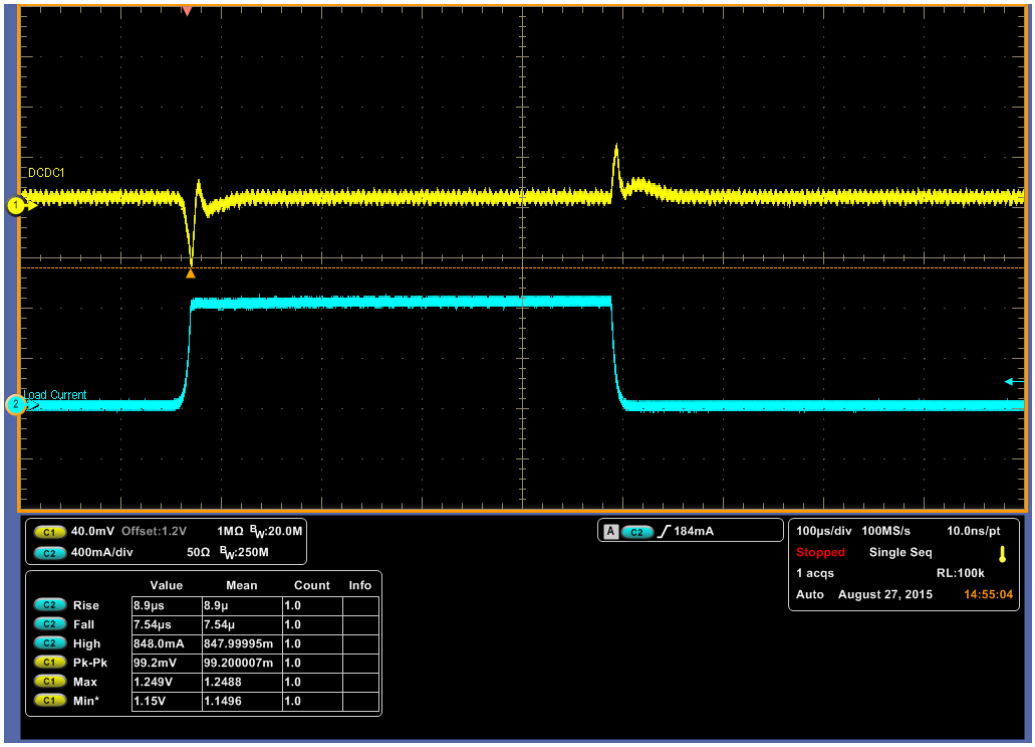

Figure 16 – DCDC1 Load Transient Response @ 25C

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DCDC2 (Vout = 3.3V) – VCC_AUX, VCCO_3V3 Load Step (0mA to 545mA, Rise Time: 7µS; Fall Time:7µS)

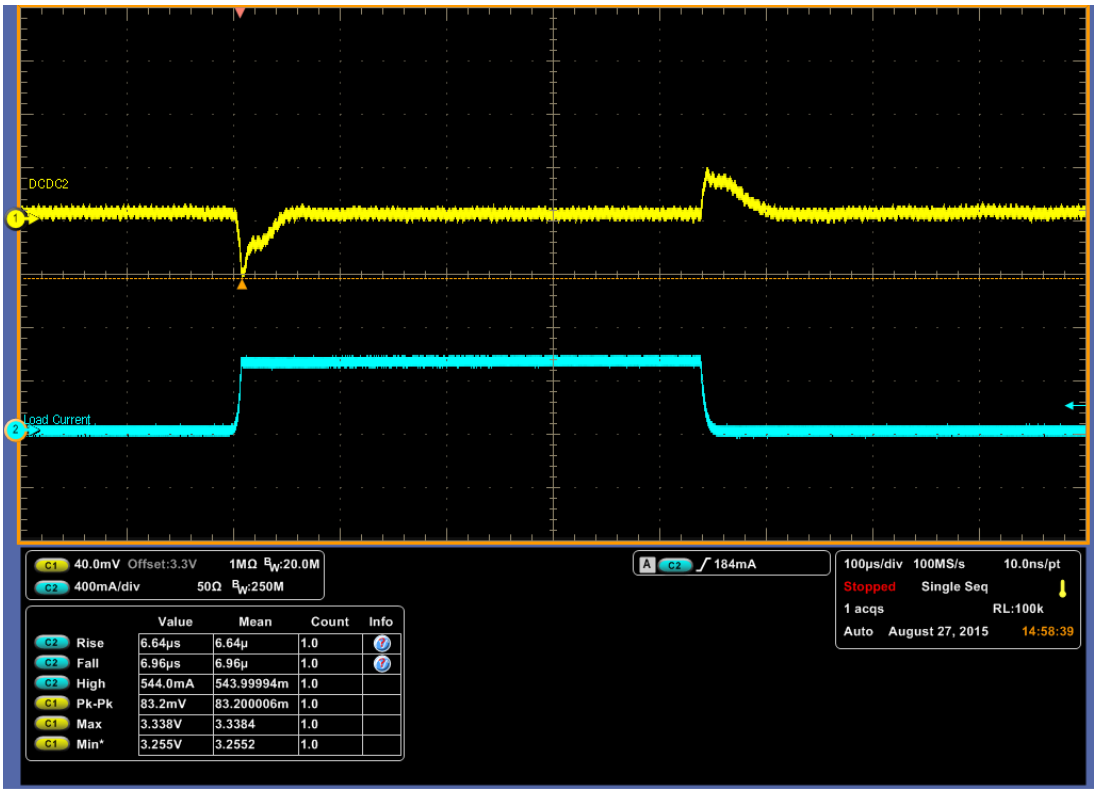

Figure 17 – DCDC2 Load Transient Response @ 25C

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DCDC3 (Vout = 1.2V) – MGTAVCC, MGTAVCCPLL, MGTAVTTX/RX, MGGTATTRCAL Load Step (0mA to 500mA, Rise Time: 7µS; Fall Time:7µS)

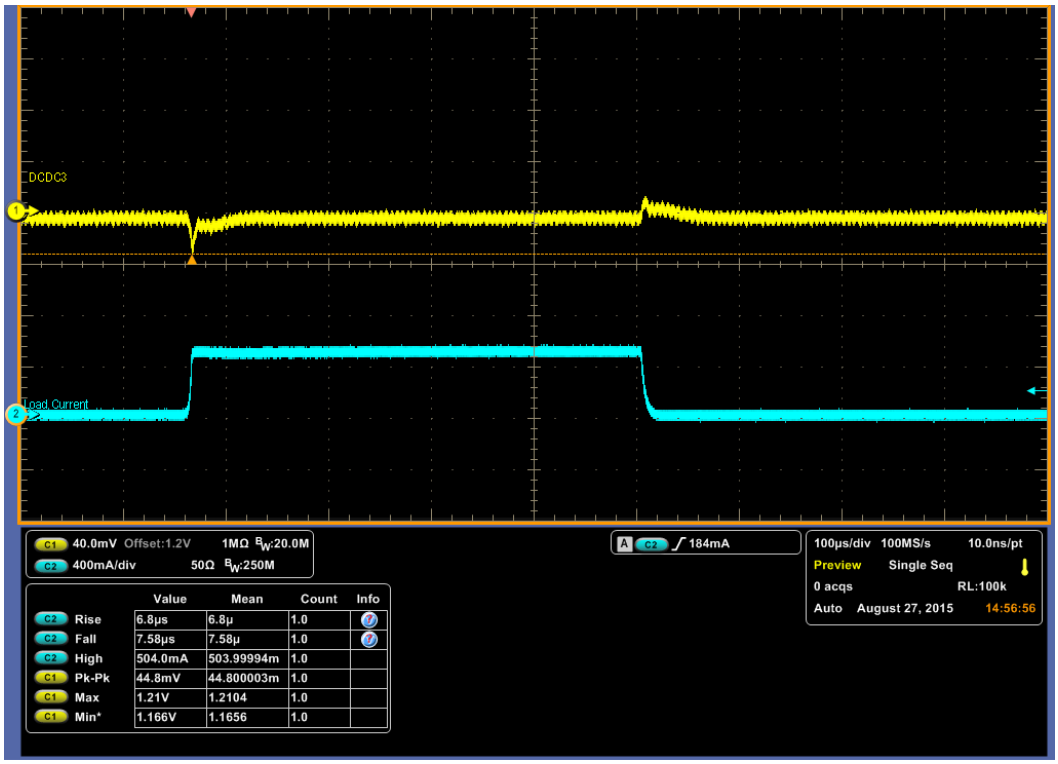

Figure 18 – DCDC3 Load Transient Response @ 25C

Design Considerations (Return to Top)

Xilinx® Spartan® 6 Recommended Power Considerations

For reference, the power requirements from the Xilinx Spartan 6 datasheet and DC Switching Characteristics are shown below:

Power Supply	Description
V_{CCINT}	Core voltage power supply
V_{CCAUX}	Auxiliary supply voltage
V_{CCO}	Output drivers supply voltage
MGTAVCC	Analog supply voltage for the GTP transmitter and receiver circuits
MGTAVCCPLL	Analog supply voltage for the GTP transmitter and receiver PLL circuits
MGTAVTTX	Analog supply voltage for the GTP transmitter termination circuit relative
MGTAVTRX	Analog supply voltage for the GTP receiver termination circuit relative
MGGTAVTTRCAL	Analog supply voltage for the resistor calibration circuit of the GTP transceiver bank

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Power Sequencing Requirements
The Spartan 6 can be powered up and powered down in any sequence. In order for the POR Circuit to be released, all the inputs need to be valid, thus there is no specific order the rails must come up.

Refer to the Spartan 6 Users Guide: (http://www.xilinx.com/support/documentation/user_guides/ug380.pdf) for Power-On Sequence Precautions when using other device in the system such as SPI Flash.

Power Supply Ramp Time:

Power Supply	Ramp Time
V_{CCINT}	0.20 to 50.0ms
V_{CCAUX}	0.20 to 50.0ms
V_{CCO}	0.20 to 50.0ms

TPS650250 Recommended Power Considerations

Input Voltage Filter
An RC filter connected at the Vcc input is used to keep noise from the internal supply for the bandgap and other analog circuitry. A typical value of 1 Ω and 1 µF is used to filter the switching spikes, generated by the DC-DC converters. A larger resistor than 10 Ω should not be used because the current into Vcc of up to 2.5 mA causes a voltage drop at the resistor causing the undervoltage lockout circuitry connected at Vcc internally to switch off too early.

Input Capacitor Selection
Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing interference with other circuits caused by high input voltage spikes. Each DC-DC converter requires a 10 µF ceramic input capacitor on its input pin VINDCDCx. The input capacitor can be increased without any limit for better input voltage filtering. The Vcc pin should be separated from the input for the DC-DC converters. A filter resistor of up to 10 Ω and a 1 µF capacitor should be used for decoupling the Vcc pin from switching noise. Note that the filter resistor may affect the UVLO threshold since up to 3 mA can flow via this resistor into the Vcc pin when all converters are running in PWM mode.

CAPACITOR VALUE	CASE SIZE	COMPONENT SUPPLIER	COMMENTS
22µF	1206	TDK C3216X5R0J226M	Ceramic
22µF	1206	Taiyo Yuden JMK316BJ226ML	Ceramic
22µF	0805	TDK C2012X5R0J226MT	Ceramic
22µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10µF	0805	TDK C2012X5R0J106M	Ceramic

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Power Supply Recommendations
The TPS650250 is designed to operate from an input voltage supply range between 3.5 V and 5.5 V. The input supply should be well regulated. If the input supply is located more than a few inches from the TPS650250, additional bulk capacitance may be required in addition to the ceramic bypass capacitors.

Output Voltage Selection:
The DCDC Converters can be set via an external resistor divider or by the logic level of the DEDCDCX pins.

PIN	LEVEL	DEFAULT OUTPUT VOLTAGE
DEFDCDC1	VCC	3.3 V
	GND	2.80 V
DEFDCDC2	VCC	2.5 V
	GND	1.8 V
DEFDCDC3	external voltage divider	0.6 V to VinDCDC3

If the desired voltages cannot be met, using an external resistor divider will allow the user to select a voltage between 0.6V up to the input.

$$V_{OUT} = V_{DEFDCDCx} \times \frac{R1 + R2}{R2}$$

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{DEFDCDCx}} \right) - R2$$

The output voltage of the LDO1 and LDO2 are set via an external resistor divider. VFBLDOX = 1.0V

$$V_{OUT} = V_{FBLDOx} \times \frac{R5 + R6}{R6}$$

$$R5 = R6 \times \left(\frac{V_{OUT}}{V_{FBLDOx}} \right) - R6$$

Inductor Selection for Buck Converters:
The three converters operate with 2.2 µH output inductors. Larger or smaller inductor values can be used to optimize performance of the device for specific conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductor influences directly the efficiency of the converter. Therefore, an inductor with the lowest DC resistance should be selected for the highest efficiency.

For a fast transient response, a 2.2 µH inductor in combination with a 22 µF output capacitor is recommended. For an output voltage above 2.8 V, an inductor value of 3.3 µH minimum is required. Lower values result in an increased output voltage ripple in PFM mode. The minimum inductor value is 1.5 µH, but an output capacitor of 22 µF minimum is needed in this case.

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The equation below calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 4. This is recommended because during heavy load transient the inductor current rises above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f}$$

$$I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2}$$

with:

f = Switching Frequency (2.25 MHz typical)
L = Inductor Value
ΔI_L = Peak-to-Peak inductor ripple current
I_{LMAX} = Maximum Inductor current

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor.

A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. Consideration must be given to the difference in the core material from inductor to inductor which has an impact on efficiency especially at high switching frequencies.

Layout Guidelines

- The VINDCDC1, VINDCDC2 and VINDCDC3 terminals should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 10 uF ceramic with a X5R or X7R dielectric.
- The VINLDO terminal should be bypassed to ground with a low ESR ceramic bypass capacitor. The typical recommended bypass capacitance is 1 uF ceramic with a X5R or X7R dielectric.
- The optimum placement is closest to the individual voltage terminals and the AGNDx terminals
- The AGNDx terminals should be tied to the PCB ground plane at the terminal of the IC.
- The cross sectional area loop from the input capacitor to the VINDCDCx input and corresponding PGNDx terminal should be minimized as much as possible.
- Route the feedback signal for each of the step-down converters next to the current path of the converter in order to decrease the cross sectional area of the feedback loop which minimizes noise injection into the loop.
- Do not route any noise sensitive signals under or next to any of the step-down inductors. Ensure a keepout region directly under the inductors or at least provide ground shielding.
- It is recommended to have the layer directly underneath the IC to be a solid copper ground plane.

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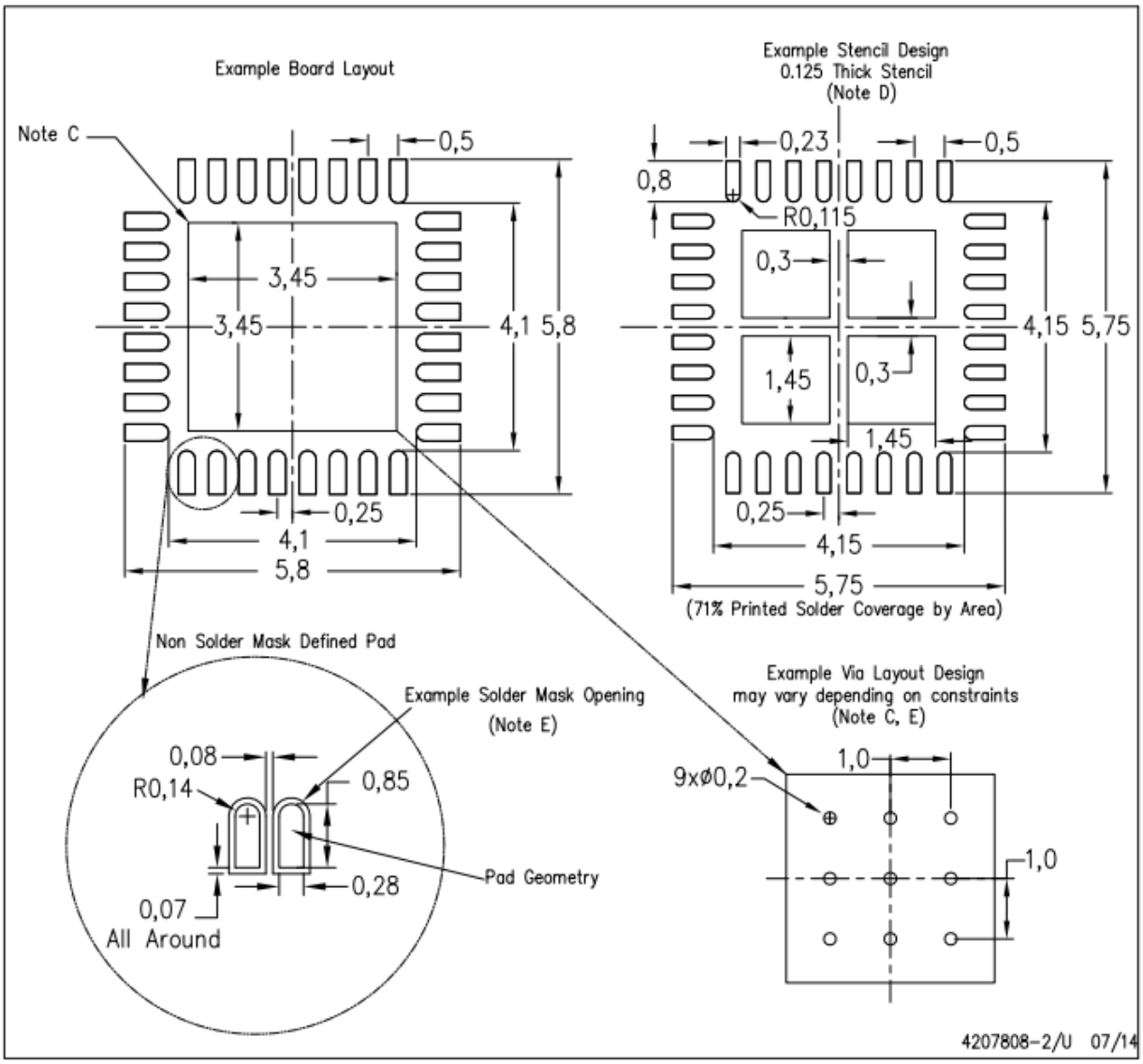
QFN Package Information

RHB (S–PVQFN–N32) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for any larger diameter vias placed in the thermal pad.

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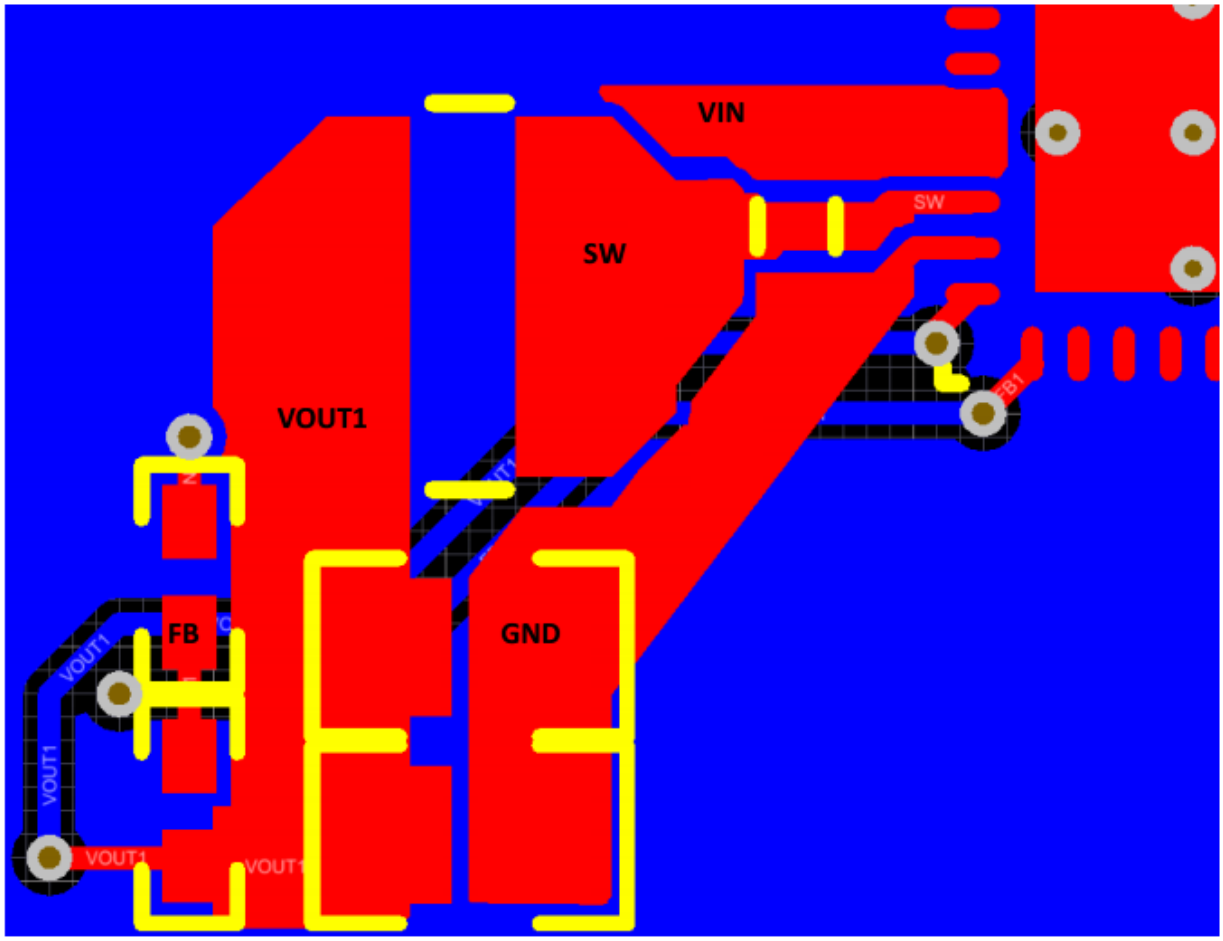
Layout Example



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