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Analog Linearized 3-Wire PT100 RTD to 2-Wire 4-20mA Current Loop Transmitter Reference Design

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Design Resources

TIPD161	All Design files
XTR105	Product Folder

Circuit Description

This 2-wire 4-20mA sensor transmitter uses analog linearization methods to provide a simple single-chip solution to interface 3-wire PT100 resistive temperature detectors (RTD) to 4-20mA current loops.

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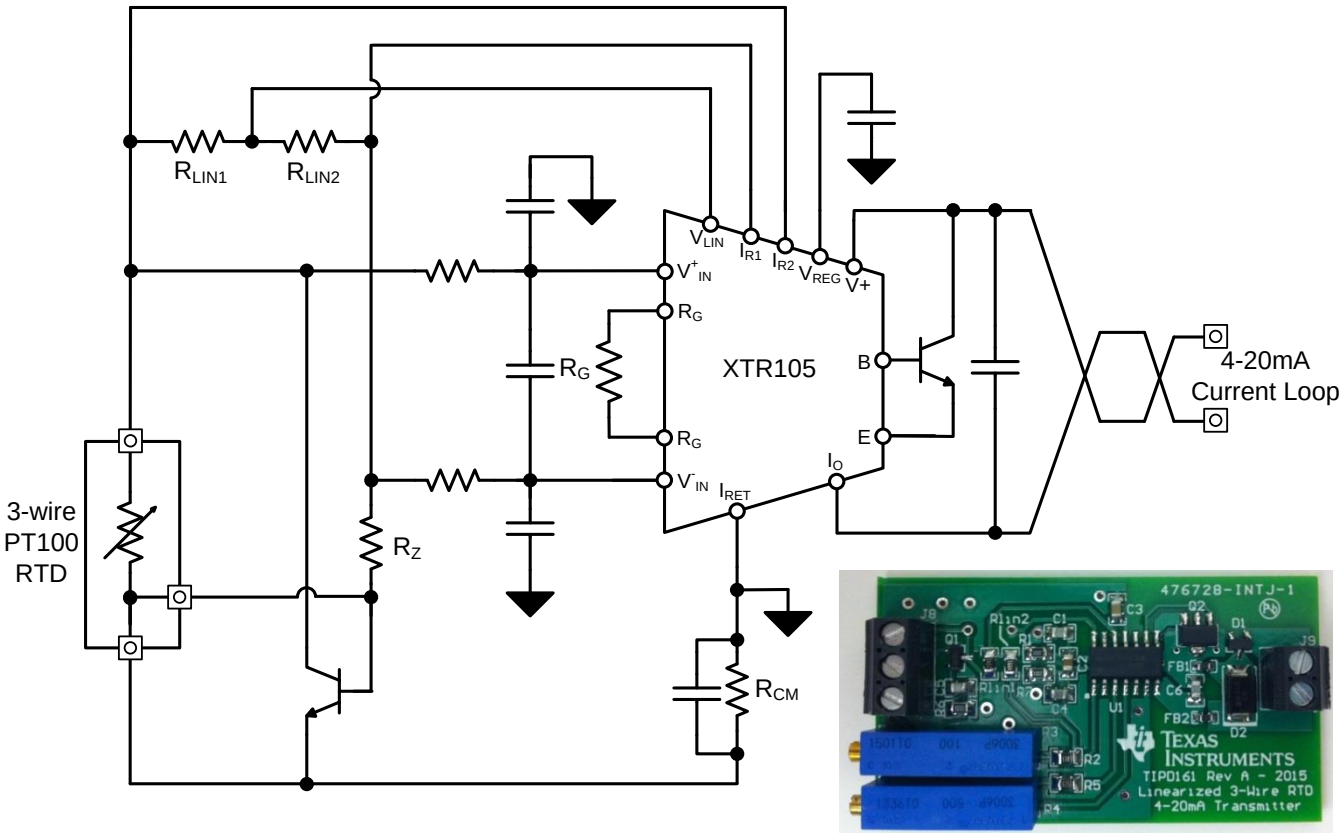

1 Design Summary

The design requirements are as follows:

- Loop Supply Voltage: +7.5 – 40V
- Input: 3-Wire PT100 RTD
- RTD Temperature Range: -200 - 800°C (1000°C span)
- Output: 4-20mA 2-Wire Current Loop
  - Ideal Output Slope of 16µA/°C
- Circuit Protection: Protected against IEC61000-4 Transients and EMI/EMC

The design goals and performance for the RTD sensor transmitter are summarized in Table 1. Figure 1 and Figure 2 depict the unadjusted and calibrated temperature accuracy results for the design.

Table 1: Comparison of Design Goals, Simulated, and Measured Performance

Specification	Goals	Calculated	Measured
Total Unadjusted Error (TUE)	±5°C, (±0.5 %FSR)	±3.83°C, (±0.383%FSR)	-5.87°C, (-0.587 %FSR)
Calibrated Output Error	±2°C, (±0.2%FSR)	±1.35°C, (±0.135%FSR)	±0.8°C, (±0.08 %FSR)
IEC61000-4 Immunity	Pass	n/a	Pass

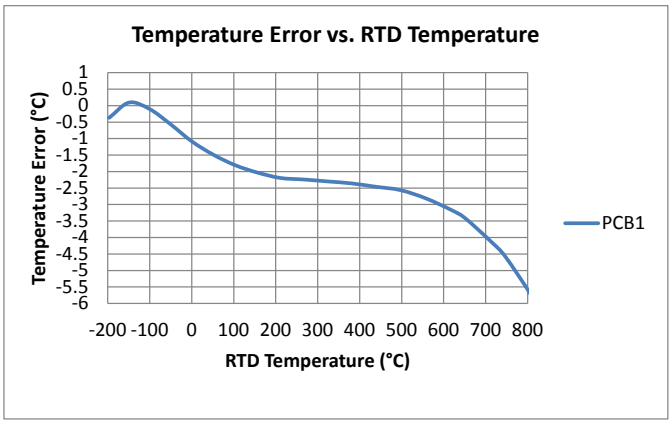

Figure 1: Measured Unadjusted Temperature Error

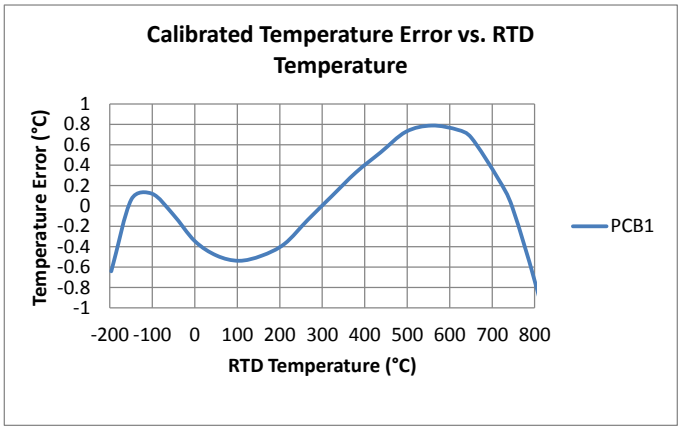

Figure 2: Calibrated Temperature Error

2 Theory of Operation

3-wire RTD sensors require excitation sources, amplification, and linearization circuits to convert the RTD resistance into a linear output representing temperature [1]. In this application, the linearized RTD output will be transmitted over a standard 2-wire 4-20mA current loop to a 2-wire analog input module for use in process/control applications. The complete RTD sensor conditioning and 2-wire transmitter circuitry for this design is featured in a single integrated component, the XTR105, as shown in Figure 3. The output current transfer function of the transmitter is shown in Equation 1.

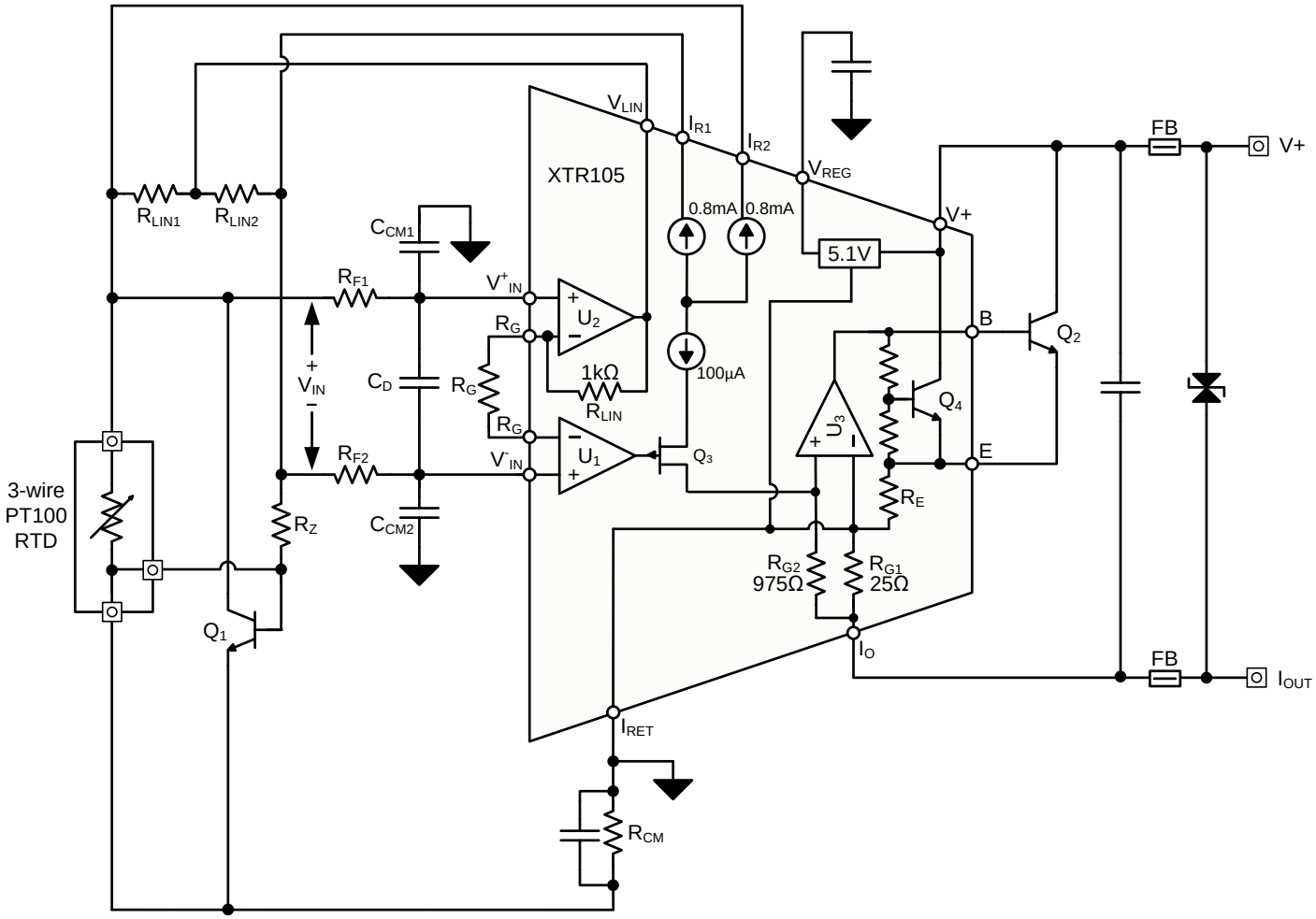

Figure 3: Detailed Schematic

$$I_{OUT}(mA) = \left(V^+_{IN} - V^-_{IN}\right) * \left(\frac{40000}{R_G}\right) + 4 \quad (1)$$

2.1 Input Amplification and Linearization Stage

The input amplification and linearization stage of the XTR105 is shown in Figure 4. It is comprised of two excitation current sources, I_{R1} and I_{R2}, several passive components, and two op amps, U1 and U2, that work together to amplify and linearize the RTD resistance. The two 800µA current sources, I_{R1} and I_{R2}, are used to create voltage drops across the RTD and zero-scale resistor, R_Z. Using two current sources allows for the lead resistances of the 3-wire RTD to be cancelled [1]. The difference in voltage drops across the RTD and R_Z resistors creates the differential input voltage, V_{IN}, to the XTR105 input stage. Differential and common-mode input filters are formed with R_{F1}, R_{F2}, C_D, C_{CM1}, and C_{CM2} which help reject noise that may couple into the RTD lead wires.

The gain of the input stage, formed by U1 and U2, is set by the ratio of the external resistor, R_G, and internal resistor, R_{LIN}. The U1 output controls the amount of current the Q_3 JFET sources to the output stage. The JFET current, I_{Q3}, is the sum of a 100uA offsetting current source and a current proportional to the differential input voltage, V_{IN}, and the ratio of the R_{LIN1} and R_G resistors. The 100uA offsetting current source is included so a zero-volt differential input signal results in a transmitter output of 4mA after the output stage gain. The transfer function for the output current of the input stage is shown in Equation 2.

The U2 amplifier also provides a controlled amount of positive feedback that increases the excitation current to the RTD over the span of the measurement. The increase in excitation current is designed to correct for the decrease in RTD sensitivity (α) over the span of the temperature measurement [1][2]. The amount of excitation current increase through the RTD is set by R_{LIN1}. R_{LIN2} balances the circuit, increasing the effectiveness of the lead resistance cancellation.

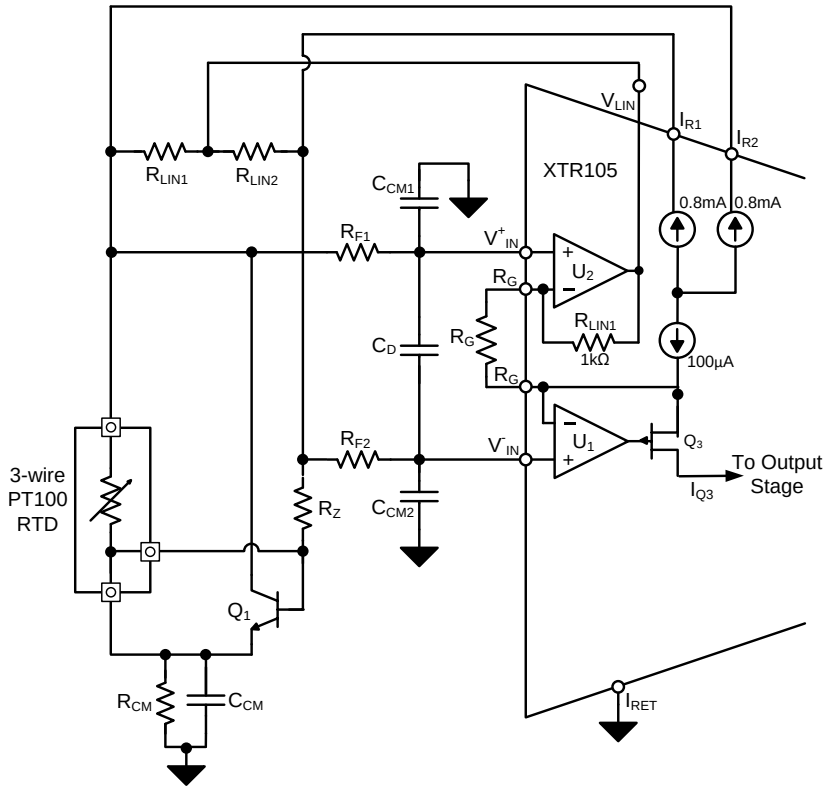

Figure 4: XTR105 Input Excitation, Linearization, and Amplification Stage

$$I_{Q3}(\mu A) = \left(V^{+}_{IN} - V^{-}_{IN}\right) * \left(\frac{R_{LIN1}}{R_G}\right) + 100\mu A = V_{IN} * \left(\frac{1000}{R_G}\right) + 100\mu A \quad (2)$$

2.2 Output Current Loop Driver Stage

The output current loop driver stage controls the output current in the 2-wire loop based on the output current from the input stage, I_{Q3}. The I_{Q3} current passes through the R_{G2} resistor creating a voltage at the non-inverting input of U3. U3 controls the current flowing through the external transistor, Q2, so the voltage drop across R_{G1} is equal to the drop across R_{G2}. The sensor excitation currents as well as the current for circuitry powered from the V_{REG} output (I_{RET}) also flow through R_{G1} and the op amp controls the Q2 output to provide the remaining required current [3]. The transfer function for the output stage is shown in Equation 3.

$$I_O(mA) = (I_{Q3}) * \left(1 + \frac{R_{G2}}{R_{G1}}\right) \quad (3)$$

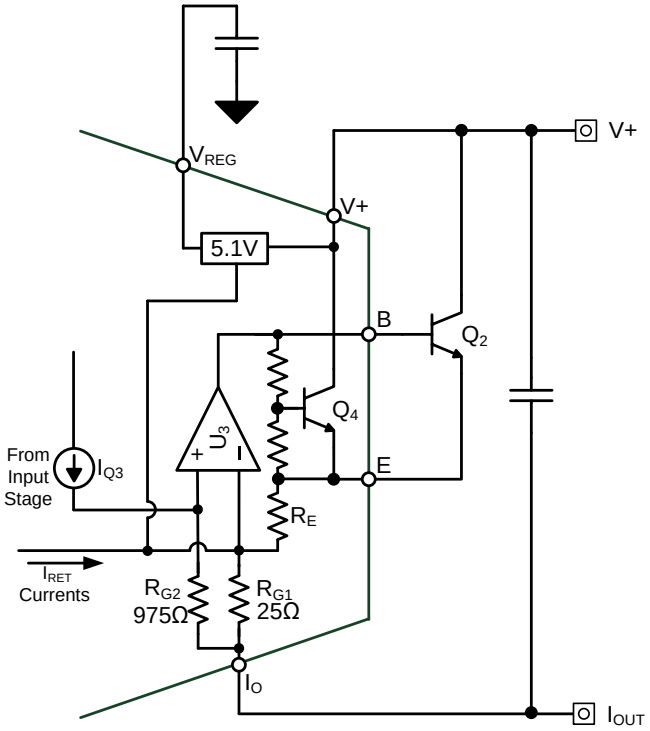

Figure 5: XTR105 Current Loop Transmitter Circuitry

3 Component Selection

3.1 XTR105

The XTR105 is a single-chip 2-wire current loop sensor transmitter designed specifically for 2 or 3-wire PT100 RTD sensors. The XTR105 integrates the excitation sources, amplification, linearization, and current loop drive circuitry described in Section 2. The linearization engine in the XTR105 results in roughly 40:1 improvement in the linearity of the final output current over the measured temperature span versus a non-linearized RTD sensor as shown in Section 4.2.

The XTR105 features strong dc specifications with a maximum 100µV initial offset and 1.5µV/°C drift. The maximum span error is 0.2% with 35ppm/°C of span drift. The internal 4mA zero-scale offsetting circuitry has a maximum error of 25µA. The internal 800 µA excitation sources have a maximum error of 0.2% with matching of 0.1%. The maximum non-linearity of 0.01% enables strong post-calibration accuracy.

3.2 Passive Component Selection

Four external resistors are required to configure the gain, offset, and linearization circuitry for the XTR105 based on the desired 3-wire RTD temperature measurement range. These resistors are R_Z, R_G, R_{LIN1}, and R_{LIN2}. The R_Z resistor is selected to produce a zero-volt differential input signal when the RTD is at the minimum resistance ($R_{RTD}(T_{MIN})$) as shown in Equation 4.

$$R_Z = R_{RTD@TMIN} \tag{4}$$

R_G sets the gain of the circuit and is based on the change of the RTD over the measurement temperature span. The complete equation to calculate the R_G value is shown in Equation 5 where $R_{RTD}(T_{MAX})$ is the maximum RTD resistance over the measurement temperature and $R_{RTD}(T_{MID})$ is equal to $R_{RTD}(T_{MAX}) – R_{RTD}(T_{MIN}) / 2$.

$$R_G = \frac{2(R_{MAX} - R_Z)(R_{MAX} - R_Z)}{R_{MAX} - R_{MID}}$$
Where
$$R_{MAX} = R_{RTD@TMAX} \tag{5}$$
$$R_{MID} = R_{RTD@TMID}$$
$$T_{MID} = \frac{T_{MAX} - T_{MIN}}{2}$$

R_{LIN1} and R_{LIN2} are calculated using the same variables found in the R_G equation as shown in Equation 6.

$$R_{LIN1} = \frac{R_{LIN}(R_{MAX} - R_{MID})}{2(2R_{MID} - R_{MAX} - R_Z)}$$
$$R_{LIN2} = \frac{(R_{LIN} + R_G)(R_{MAX} - R_{MID})}{2(2R_{MID} - R_{MAX} - R_Z)} \tag{6}$$
Where
$$R_{LIN} = 1000\Omega$$

The minimum, mid, and maximum values of a PT100 RTD operating from -200C to 800C are shown in Table 2.

Table 2: PT100 Resistance Values for -200°C to 800°C Span

	Temperature	Resistance
RTD(T_{MIN})	-200°C	18.52 Ω
RTD(T_{MID})	300°C	212.05 Ω
RTD(T_{MAX})	800°C	375.7 Ω

Plugging the RTD resistance values from Table 2 into Equations 4 –6 results in the external passive component values shown in Table 3. The closest 0.1% values are also shown along with the error resulting from the discrepancy from the ideal value.

Table 3: XTR105 Zero, Gain, and Linearity Resistor Selections with Error

	Calculated Value	Closest 0.1% Value	Error from Calculated Value
RZ	18.52 Ω	18.7 Ω	0.05%
RG	844.79 Ω	845 Ω	0.025%
RLIN1	2738.69 Ω	2740 Ω	0.05%
RLIN2	5052.31 Ω	4990 Ω	1.233%

The two 800µA excitation currents flow through the R_{CM} resistor to bias the differential input signal to within the XTR105 input common-mode voltage range of 1.25 V to 3.5 V. The minimum resistance is calculated in Equation 7.

$$R_{CM\_MIN} = \frac{1.25V}{2 \cdot 800\mu A} = 781.3\Omega \tag{7}$$

R_{CM} was selected to be a standard value of 1 kΩ, resulting in a minimum common-mode input voltage of 1.6 V.

Most temperature measurements do not require high bandwidths because the change in temperature is not very fast. In this design, the inputs to the XTR105 have been filtered to reduce interference from extrinsic noise sources. R_{F1} and R_{F2} combine with C_D, C_{CM1} and C_{CM2} to form common-mode and differential input filters. The common-mode filter cutoff frequency is set roughly forty times greater than the differential filter to prevent component tolerances from degrading the common-mode rejection of the amplifier. The cutoff frequencies for these filters are calculated in Equation 8.

$$f_{-3dB\_DIFF} = \frac{1}{2 \cdot \pi \cdot (2 * 10k\Omega) \cdot 0.22\mu F} = 36Hz$$
$$f_{-3dB\_CM} = \frac{1}{2 \cdot \pi \cdot 10k\Omega \cdot 0.01\mu F} = 1591Hz \quad (8)$$

3.3 Protection Component Selection

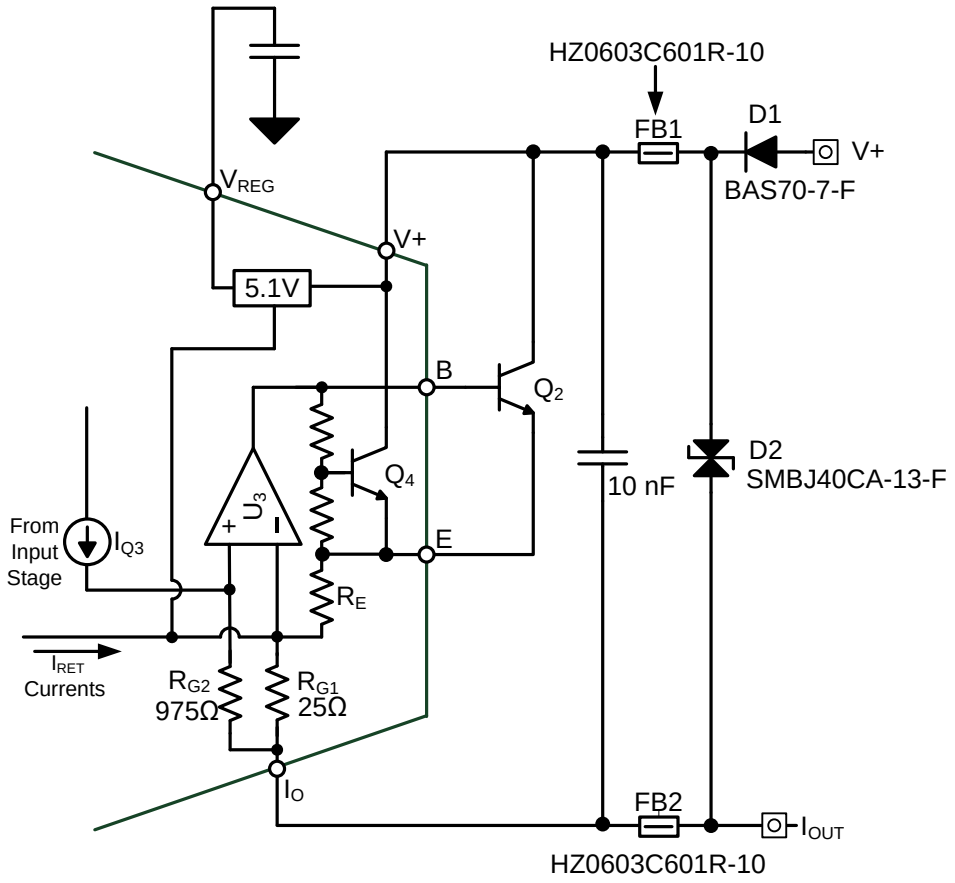

Figure 6: Simplified Schematic Showing Output Protection Components

The protection scheme in this design, shown in Figure 6, is intended to provide immunity to EMI/RFI interference and transient voltage disturbances as described in the IEC61000-4 tests[5][6][7][8][9][10]. The IEC61000-4 transients have two components: a high frequency component and a high energy component. Therefore the protection strategy focuses on attenuating the high frequency transients and diverting the energy from the high energy components away from the sensitive circuitry[4].

Attenuation is achieved through resistors and capacitors that attenuate high-frequency transients and also limit series current. Ferrite beads are used to maintain dc accuracy while still limiting current from high frequency transients. Capacitors placed between the output terminals help attenuate transient energy from high frequency tests such as electrostatic discharge (ESD) and electrically fast transients (EFT).

Diverting the large energy transients is accomplished using transient voltage suppressor (TVS) diodes. The protection scheme must limit the level of the voltage transients to a level less than the absolute maximum rating for the output of the XTR105. More information on the IEC61000-4 tests and the protection circuitry requirements can be obtained in TIPD153 [4].

3.3.1 Reverse Protection Diode

A Schottky diode rectifier is used in this design to prevent damage to the components in the design if the supply and output wires are connected improperly. Selection of this diode should be based on low reverse leakage current and low forward voltage. The BAS70 was chosen for this design because it features low forward voltages of 0.41V, a maximum reverse breakdown voltage of 70V and forward current rating of 70mA continuous. A diode bridge could have been used to maintain proper transmitter operation regardless of the wiring connections at the cost of an extra diode drop in the loop.

3.3.2 TVS Diode

A bidirectional TVS diode is used to divert energy from high voltage transients away from the XTR105 and sensor. Select the TVS diode based on the working voltage, breakdown voltage, leakage current and power rating. The working voltage specification defines the largest reverse voltage that the diode is meant to be operated at continuously without it conducting. This is the voltage at the “knee” of the reverse breakdown curve where the diode begins to break down and exhibits some small leakage current. As the voltage increases above the working voltage, more current will begin to flow through the diode. The breakdown voltage defines the reverse voltage at which the diode is fully allowing current to flow. It is important to keep in mind that if large currents flow through the diode, the breakdown voltage will rise.

The diode breakdown voltage should be low enough to protect all components connected to the output terminals and to provide headroom to continue providing this protection as the breakdown voltage rises with large currents. In this design the working voltage of the TVS diode should be at or above the upper limit of the allowed supply voltages since any higher voltage would cause leakage through the diode. In this case the SMBJ40CA diode was selected with a working voltage of 40V, breakdown voltage of 44 V, and power rating of 600 W.

An additional parameter to consider for TVS diode selection is leakage current. At the working voltage, when the diode is not operating in its breakdown region, some current will flow through the diode and can affect system accuracy. The diode selected for this design features 1 µA maximum leakage current at the working voltage.

3.3.3 Passive Comonents

Series ferrite beads and a parallel capacitor are used to attenuate transient signals that may remain after passing across the TVS diode. The ferrites are chosen based on their current rating, impedance at dc, and impedance at high frequency. In this design the chosen ferrites feature 42 mΩ max impedance at dc, 600 Ω impedance at 100MHz, and 3 A current rating. The capacitor chosen has a voltage rating of 100V.

4 Circuit Performance Calculations

The circuit performance is based on the specifications of the XTR105 and the external R_Z, R_G, R_{LIN1}, and R_{LIN2} resistors. The final temperature accuracy depends also on the effectiveness of the RTD non-linearity correction methods.

4.1 Circuit Accuracy

A simplified error calculation using only the dominant error terms is shown in this section. A full error calculation is shown in the datasheet for the XTR105 that includes all error sources in the XTR105. The specifications that dominate the XTR105 performance are listed in Table 4.

Table 4: XTR105 Performance Specifications

XTR105 Specification	Maximum Value
Offset (mV)	0.1
Zero Current Error (µA)	25
Excitation Current Error (%)	0.2
Gain Error (%)	0.2
Nonlinearity (%)	0.01

The total unadjusted error, TUE, of the XTR105 can be roughly calculated as shown in Equation 9.

$$TUE_{XTR105}(\%FSR) = \left(\sqrt{\left(\frac{V_{OS}}{V_{IN\_SPAN}}\right)^2 + \left(\frac{Zero}{I_{OUT\_SPAN}}\right)^2 + \left(\frac{GainError\%}{100}\right)^2 + \left(\frac{ExcitationError\%}{100}\right)^2 + \left(\frac{Nonlinearity}{100}\right)^2} \right) \times 100$$

$$TUE_{XTR105}(\%FSR) = \left(\sqrt{\left(\frac{0.1mV}{0.2856V}\right)^2 + \left(\frac{0.025mA}{16mA}\right)^2 + \left(\frac{0.2}{100}\right)^2 + \left(\frac{0.2}{100}\right)^2 + \left(\frac{0.01}{100}\right)^2} \right) \times 100 = 0.325\%FSR \quad (9)$$

The R_Z resistor tolerance and deviation from the ideal calculated value introduce offset errors into the design. The errors caused by tolerance (R_{Z_TOL}) actual value (R_{Z_ACTUAL}) of R_Z are calculated in Equation 10.

$$R_{Z\_TOL} = 0.1\%FSR$$

$$R_{Z\_ACTUAL}(\%FSR) = \left(\frac{(R_Z - R_{Z\_IDEAL}) * 800\mu A}{V_{IN\_SPAN}} \right) \times 100$$

$$R_{Z\_ACTUAL}(\%FSR) = \left(\frac{(18.7 - 18.52) * 800\mu A}{0.2856} \right) \times 100 = 0.05\%FSR \quad (10)$$

The R_G resistor tolerance and deviation from the ideal calculated value introduce gain errors into the design. The errors caused by tolerance (R_{G_TOL}) actual value (R_{G_ACTUAL}) of R_G are calculated in Equation 11.

$$R_{G\_TOL} = 0.1\%FSR$$

$$R_{G\_IDEAL}(\%FSR) = \left(\frac{(R_G - R_{G\_IDEAL})}{R_{G\_IDEAL}} \right) \times 100$$

$$R_{G\_IDEAL}(\%FSR) = \left(\frac{845 - 844.794}{844.794} \right) \times 100 = 0.025\%FSR \quad (11)$$

The XTR105 errors can be combined with the errors from the external components to calculate the total error of the circuit as shown in Equation 12.

$$I_{OUT}(\%FSR) = \left(\sqrt{(TUE_{XTR105})^2 + (R_{Z\_TOL})^2 + (R_{Z\_ACTUAL})^2 + (R_{G\_TOL})^2 + (R_{G\_ACTUAL})^2} \right) \times 100$$

$$I_{OUT}(\%FSR) = \left(\sqrt{(0.325\%)^2 + (0.1\%)^2 + (0.05\%)^2 + (0.1\%)^2 + (0.025\%)^2} \right) = 0.359\%FSR \quad (12)$$

A worst-case calculation can be performed by directly adding the error sources together which yields a maximum output error of 0.876%FSR.

4.2 RTD Sensor Linearization Circuitry Accuracy

As shown in Figure 7 a PT100 RTD measurement will have roughly 4.2% nonlinearity over a -200C – 800C span if a simple endpoint fit is used. The linearization circuit in the XTR105 can ideally correct a standard RTD nonlinearity by over forty times compared with an end-point fit. Figure 7 displays the nonlinearity of a PT100 compared with the ideal output using the XTR105. As shown, the XTR105 linearization circuitry can ideally reduce the output nonlinearity to roughly ±0.075%FSR.

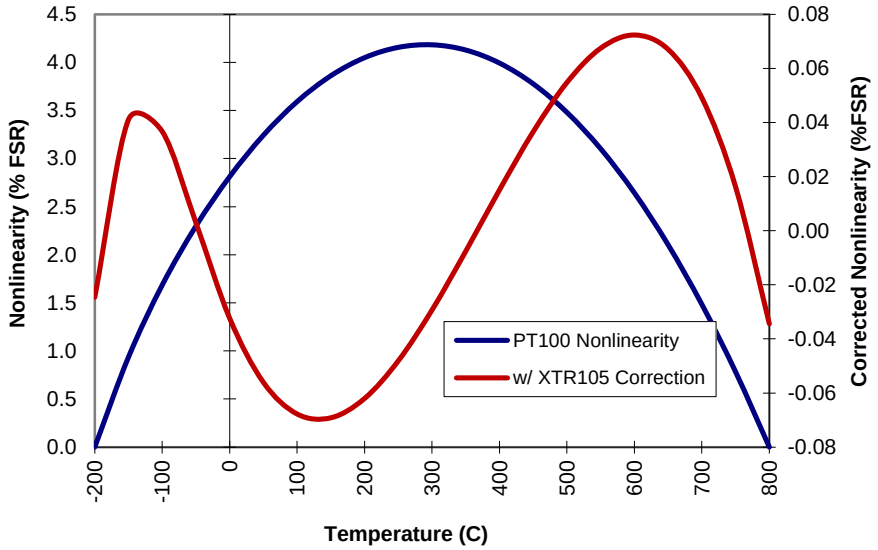

Figure 7: XTR105 Linearization Circuitry Ideal Improvements

Component tolerance and deviation from the ideal calculated value for RLIN1 will reduce the effectiveness of the linearization engine. The tolerance and deviation of RLIN2 will have minimal impact on the transfer function but will impact the effectiveness of the 3-wire RTD lead resistance cancellation. The accuracy of the linearization engine and the effects of RLIN1 are combined with the error calculations to predict the final transmitter accuracy as shown in Equation 13.

$$I_{OUT}(\%FSR) = \left(\sqrt{(TUE_{XTR105})^2 + (Linearization_{ERROR})^2 + (R_{LIN1\_TOL})^2 + (R_{LIN1\_ACTUAL})^2}\right) \times 100$$
$$I_{OUT}(\%FSR) = \left(\sqrt{(0.359\%)^2 + (0.075\%)^2 + (0.1\%)^2 + (0.05\%)^2}\right) = 0.383\%FSR \quad (13)$$

4.3 Calibrated Output Accuracy

The gain and offset calibration circuit shown and explained in Appendix A.3 can be used to remove the gain and offset errors of the circuit leaving only the linearity errors of the XTR105 gain stage and linearization circuitry. These terms are combined in Equation 14 which predicts the calibrated circuit accuracy.

$$I_{OUT\_CAL}(\%FSR) = \left(\sqrt{(XTR105_{NONLINEARITY})^2 + (Linearization_{ERROR})^2 + (R_{LIN1\_TOL})^2 + (R_{LIN1\_ACTUAL})^2}\right) \times 100$$
$$I_{OUT\_CAL}(\%FSR) = \left(\sqrt{0.01^2 + 0.075^2 + 0.1^2 + 0.05^2}\right) \times 100 = 0.135\%FSR \quad (14)$$

5 PCB Design

The PCB schematic and bill of materials can be found in Appendix A.1.

5.1 PCB Layout

For optimal performance of this design follow standard precision PCB layout guidelines, including proper decoupling close to all mixed signal integrated circuits and providing adequate power and GND connections with large copper pours.

Additional considerations must be made for providing robust EMC/EMI immunity. All protection elements should be placed as close to the output connectors as possible to provide a controlled return path for transient currents that does not cross sensitive components. Optimal dissipation of the transient energy occurs with wide, low-impedance, low-inductance traces along the output signal path and protection elements. When possible, copper pours are used in place of traces. Stitching the GND pours provides an effective return path around the PCB and helps reduce the impact of radiated emissions.

The layout for the design is shown in Figure 8.

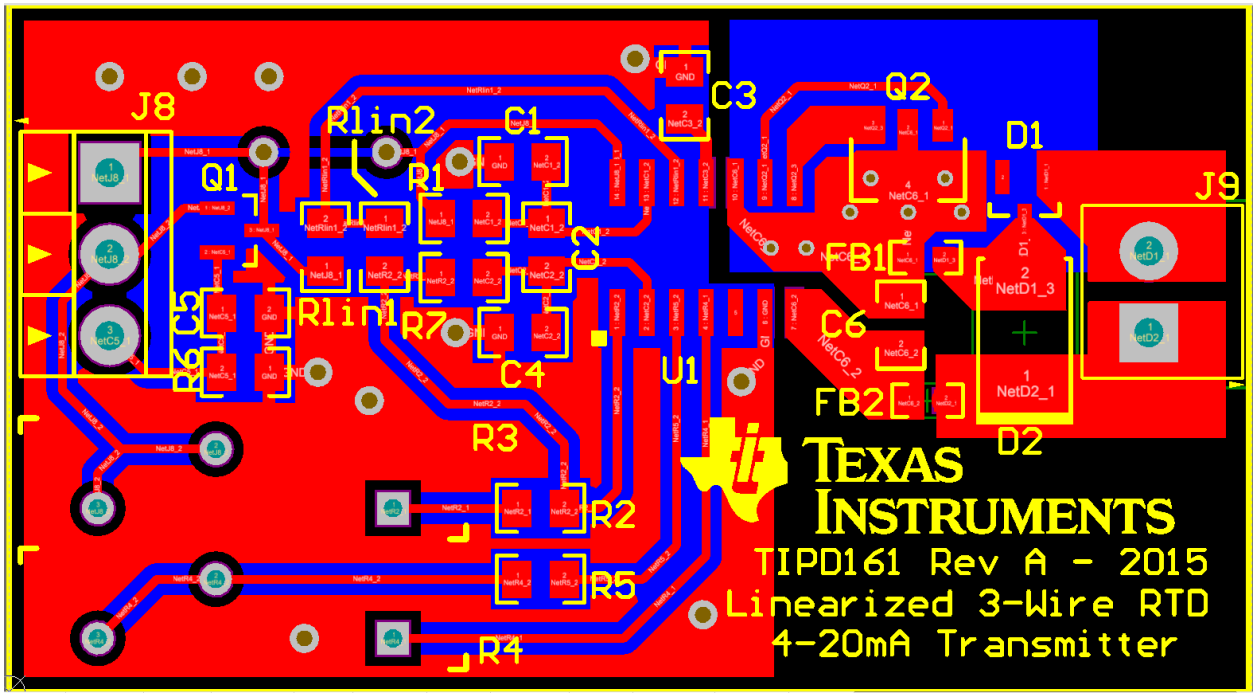

Figure 8: Altium PCB Layout

6 Verification and Measured Performance

6.1 Measured Transfer Function with Precision Resistor Input

To test the accuracy of only the acquisition circuit, a series of calibrated high-precision discrete resistors were used as the input to the system. Figure 9 displays the output current of the system over an input span of 20 Ω to 380 Ω, roughly representing a PT100 RTD resistance change from -200C to 800C. The design performs as expected and outputs a linear 4-20mA over the input RTD temperature range.

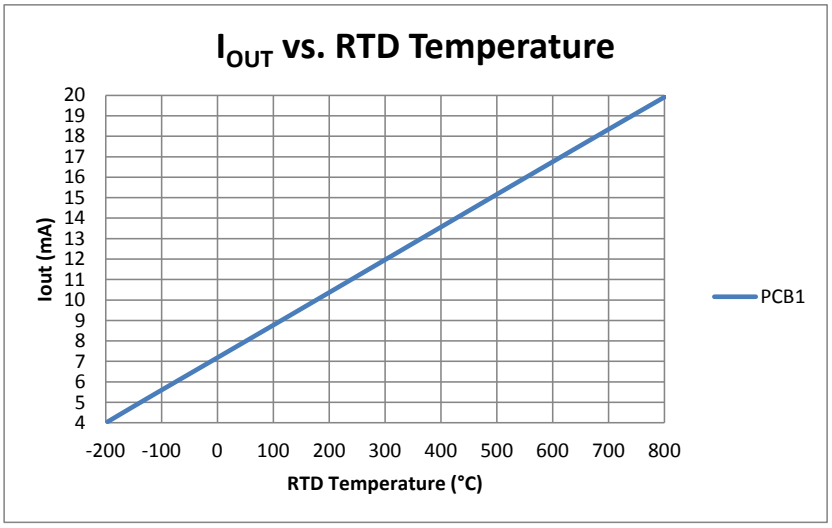

Figure 9: Output Current (I_{OUT}) vs. RTD Temperature

The output current error is displayed in Figure 10. Without including the nonlinearity due to the output correction, the design has a maximum gain error of roughly -0.08mA or -0.5%FSR.

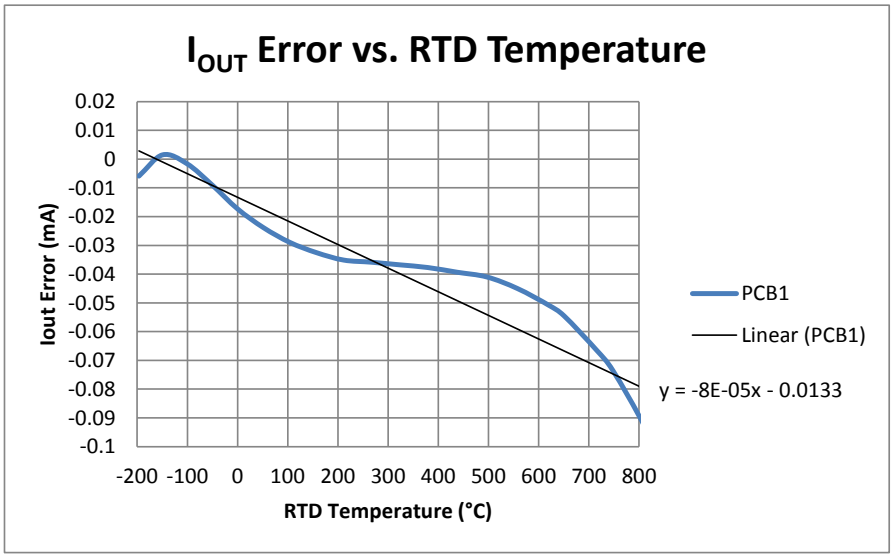

Figure 10: Output Current Error vs. RTD Temperature

The output current error can be converted to output temperature error based on the ideal output slope of 0.016mA/°C or 62.5°C/mA. The output temperature error over the measurement range is shown in Figure 11.

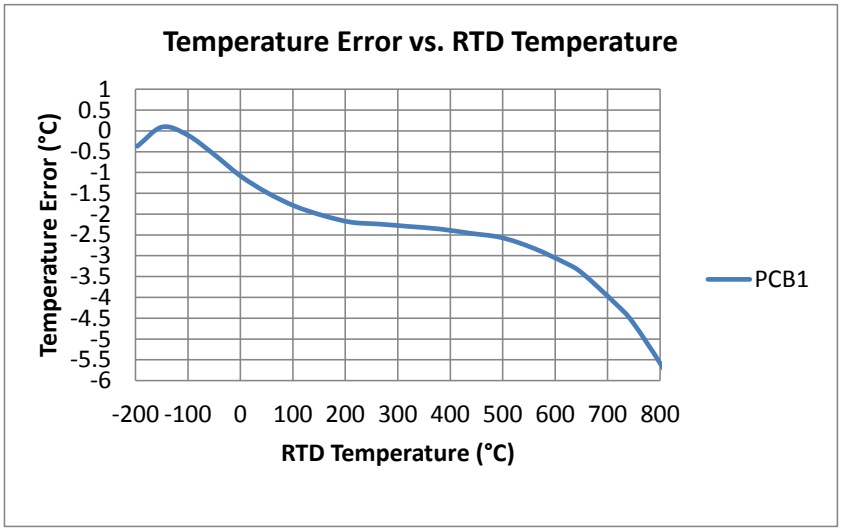

Figure 11: Output Temperature Error vs. RTD Temperature

By removing the offset and gain errors through manual calibration described in Appendix A.3 the results shown in Figure 12 were achieved. The final calibrated error is about ±0.8°C or 0.08% FSR which is within the range of the calculated value of 0.135% FSR.

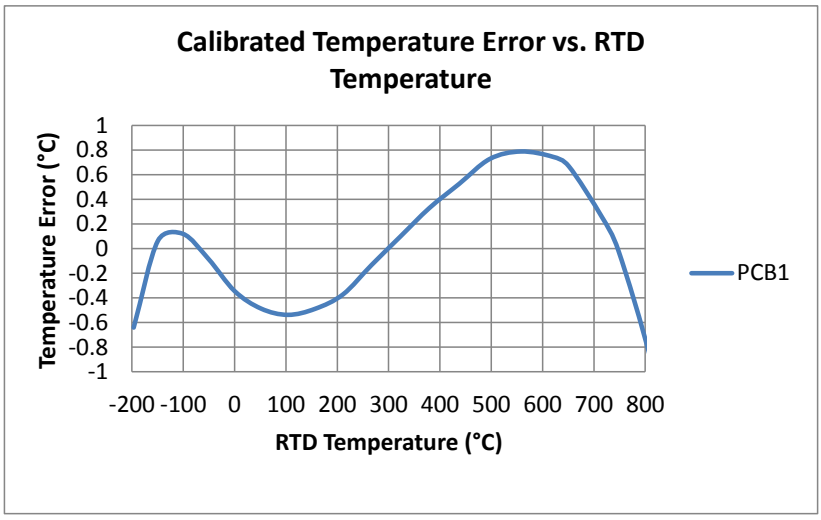

Figure 12: Calibrated Output Current Error vs. RTD Temperature

6.2 Measured Result Summary

The measured performance is summarized and compared with the goals and calculated values in Table 5.

Table 5: Comparison of Design Goals, Calculated, and Measured Performance

Specification	Goals	Calculated	Measured
Total Unadjusted Error (TUE)	±5°C, (±0.5 %FSR)	±3.83°C, (±0.383%FSR)	-5.87°C, (-0.587 %FSR)
Calibrated Output Error	±2 °C, (±0.2%FSR)	±1.35°C, (±0.135%FSR)	±0.8°C, (±0.08 %FSR)

7 Certification Testing Results

Class A performance for this EUT will be assigned for outputs that stay within 0.5% FSR (±80µA) of their intended value, during exposure to each IEC61000-4 disturbance. The output was configured to a 12mA static dc level before the tests and the input was not changed while the tests were active. The IEC61000-4 certifications do not specify what supporting equipment is used to monitor the output of the EUT. For this design, an Agilent 34401A 6.5 digit digital multi-meter with resolution set to fast 5.5 digit mode was selected to monitor the output current.

7.1 IEC61000-4-2: ESD (Electrostatic Discharge)

ESD tests were conducted at ±8 kV vertical and horizontal coupling plane and ±15 kV air discharge. ESD had minimal effect on the output current. During and after the tests the output stayed within 1% FSR of the output value. Table 6 summarizes the results of the ESD tests. Figure 13 and Figure 14 show the outputs during each test.

Table 6. IEC61000-4-2 Results

Test	Level	Result	Class
Horizontal Coupling Plane	8 kV	Pass	A
Vertical Coupling Plane	8 kV	Pass	A
Air Discharge	15 kV	Pass	A

7.1.1 I_{OUT} ESD Results

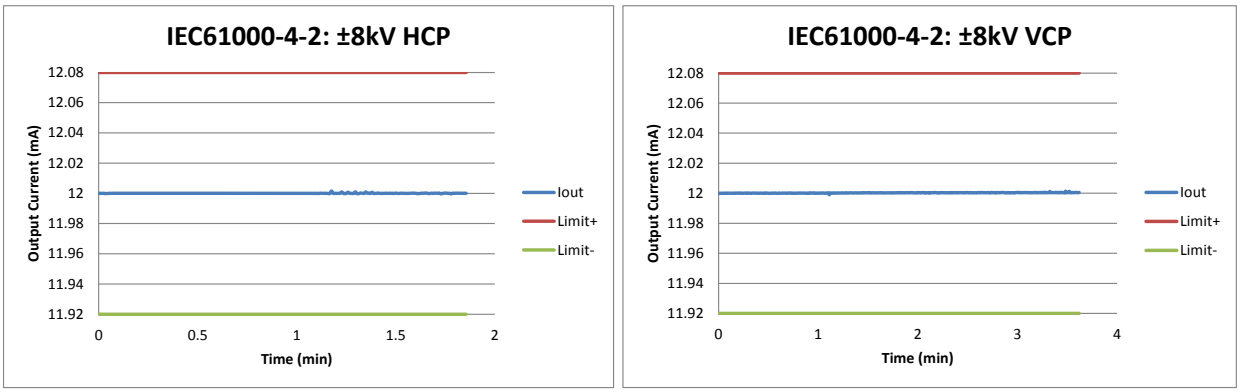

Figure 13: ±8 - kV ESD Horizontal (left) and Vertical (right) Coupling Planes (HCP and VCP)

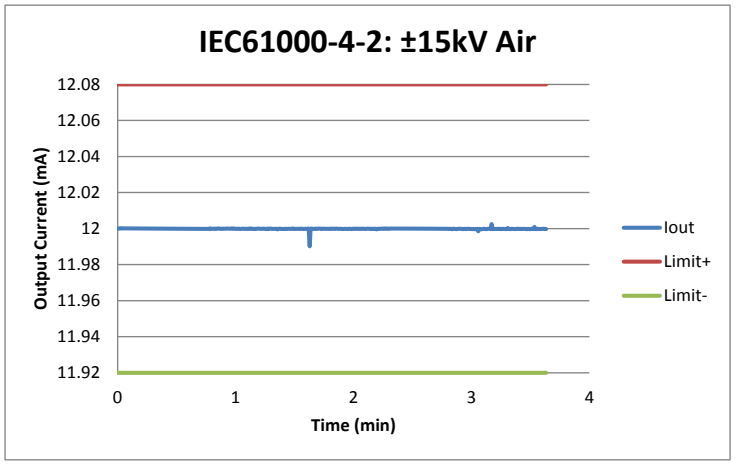

Figure 14: ±15 kV ESD Air Discharge

7.2 IEC61000-4-3: RI (Radiated Immunity)

Exposure to radiated emissions with field strengths at 10V/m and above caused the current output to deviate outside of the class A limit, resulting in a class B rating for these tests. After the test was completed the output current returned to normal operation without deviation. Table 7 summarizes the results of each test and Figure 15 through Figure 17 shows the output during each test.

Table 7. IEC61000-4-3 Results

Antennae Orientation	Level	Result	Class
Horizontal and Vertical	3 V/m	Pass	A
	10 V/m	Pass	B
	18 V/m	Pass	B

7.2.1 I_{OUT} RI Results

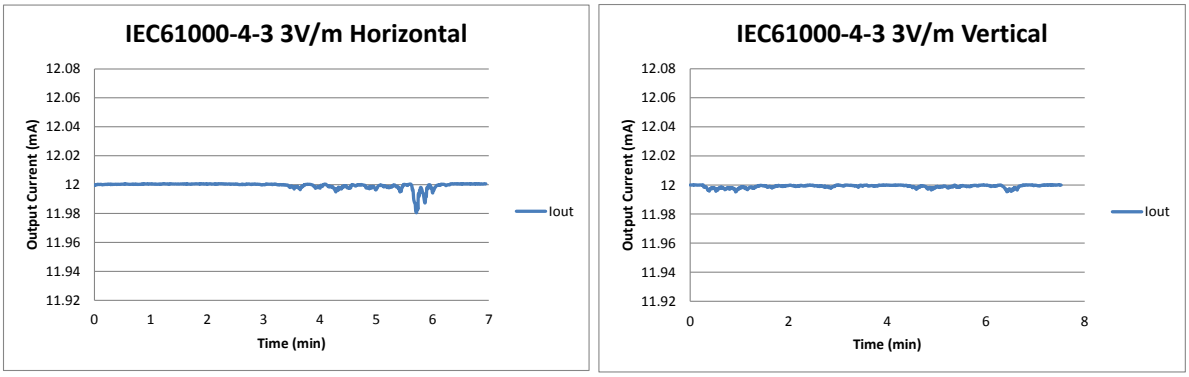

Figure 15: Horizontal (left) and Vertical (right) Polarity at 3V/m

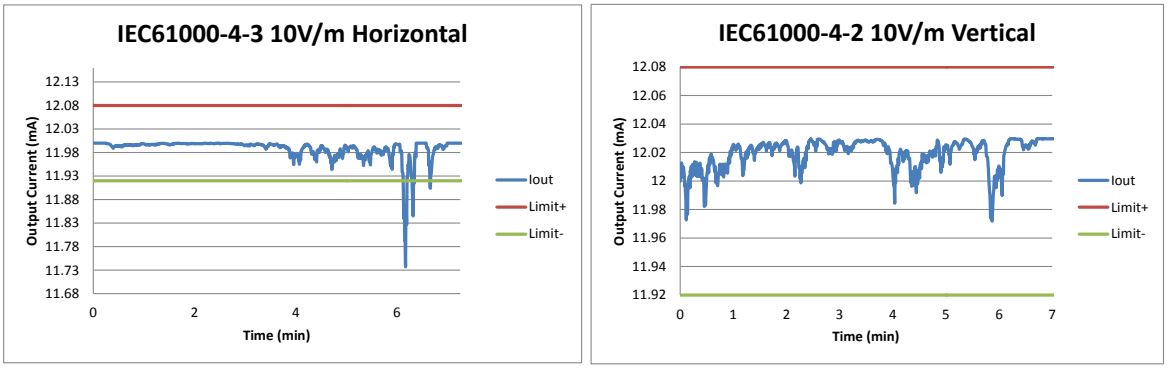

Figure 16: Horizontal (left) and Vertical (right) Polarity at 10V/m

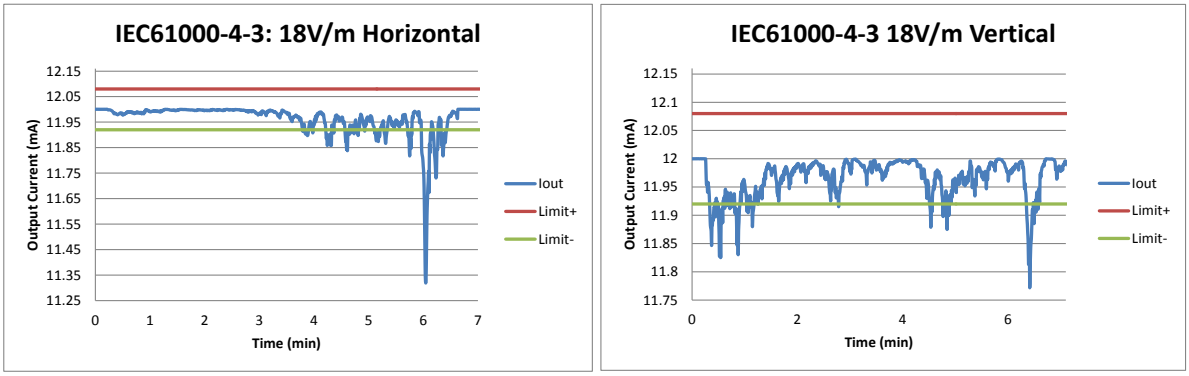

Figure 17: Horizontal (left) and Vertical (right) Polarity at 18V/m

7.3 IEC61000-4-4: EFT (Electrically Fast Transient)

The electrical fast transient bursts had an effect on the output current at ±4kV, but almost no effect at ±2kV. After testing was complete normal functionality was restored. Table 8 summarizes the results of each test. Figure 18 and Figure 19 show the current and voltage outputs during each test.

Table 8. IEC61000-4-4 Results

Level	Result	Class
± 2 kV	Pass	A
± 4 kV	Pass	A

7.3.1 I_{OUT} EFT Results

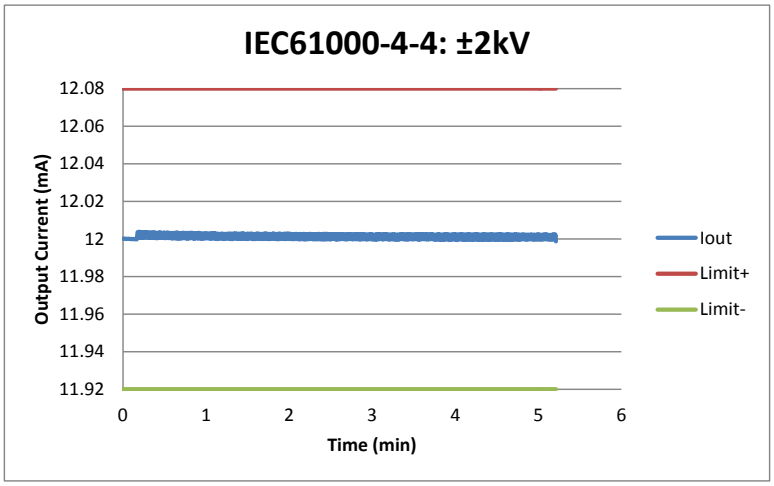

Figure 18: ±2 kV EFT

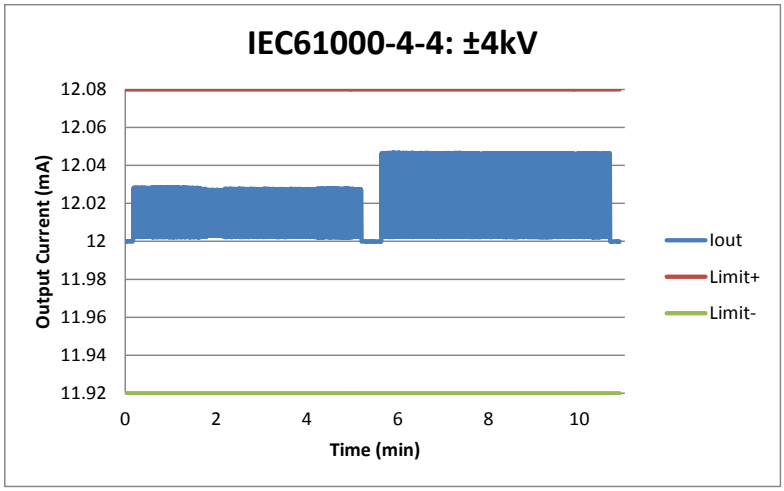

Figure 19: ±4 kV EFT

7.4 IEC61000-4-5: Surge

The electrical lightning surge bursts had little effect on the voltage and current outputs. After testing was complete normal functionality was restored. The Line-to-Line configuration connects the surge generator directly between the two terminals. Line-to-GND configurations connect the generator between the I_{OUT} terminal or RTN and the generator chassis GND.

Table 9 summarizes the results of each test Figure 20 and Figure 21 show the outputs during each test.

Table 9. IEC61000-4-5 Results

Configuration	Source Impedance	Level	Result	Class
Line-to-Line	47 Ω	±0.5 kV	Pass	A
Line-to-GND – Iout	47 Ω	±2 kV	Pass	A
Line-to-GND - RTN	47 Ω	±2 kV	Pass	A

7.4.1 I_{OUT} Surge Results

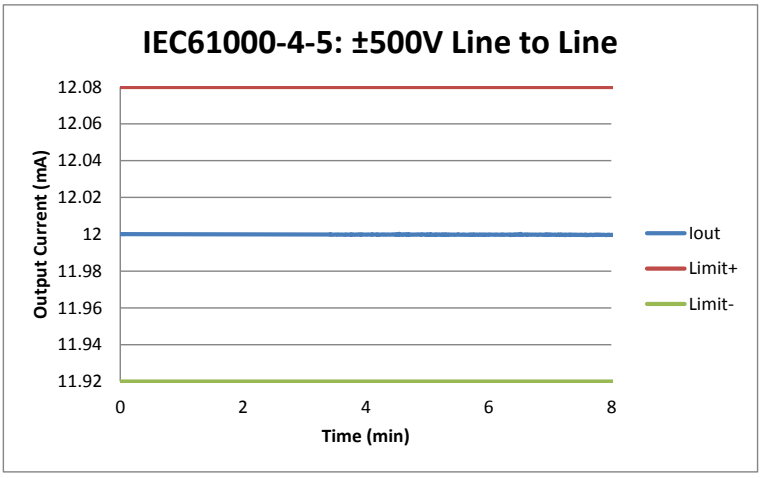

Figure 20: ±0.5 kV Surge - Line-to-Line

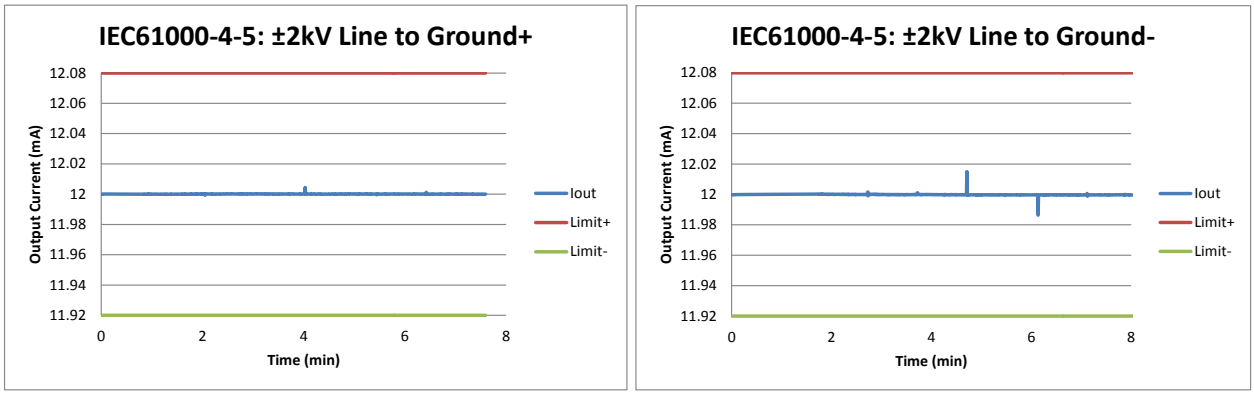

Figure 21: ±2 kV Surge - Line-to-Ground on I_{OUT} (left) and RTN (right)

7.5 IEC61000-4-6: CI (Conducted Immunity)

The conducted immunity tests caused deviations in the output current resulting in a Class B rating for these tests. The results are summarized in Table 10. Figure 22 and Figure 23 shows the behavior of the output during exposure to the CI test.

Table 10. IEC61000-4-6 Results

Result	Class
Pass	B

7.5.1 I_{OUT} CI Results

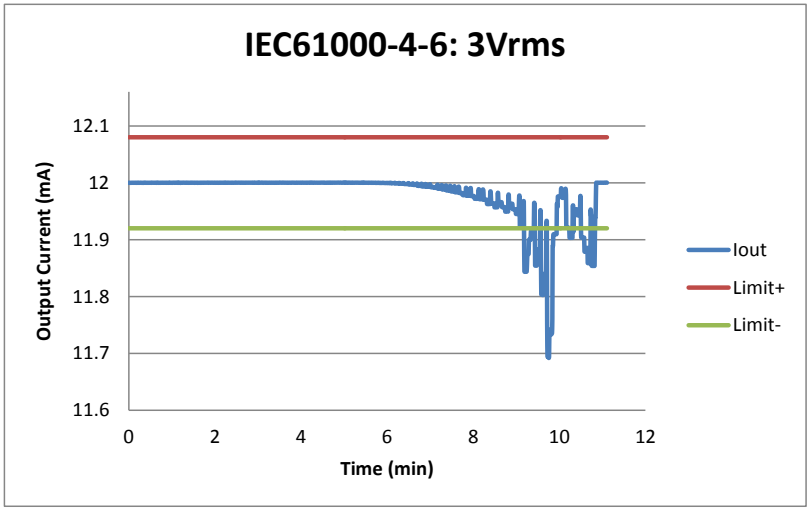

Figure 22: 3 Vrms Conducted Immunity Results

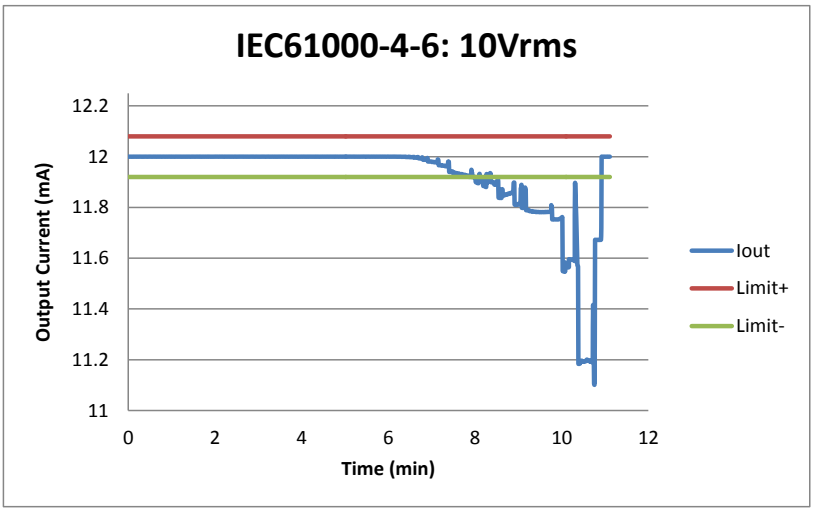

Figure 23: 10 Vrms Conducted Immunity Results

8 Modifications

The XTR105 is the only integrated solution available from Texas Instruments that convert a PT100 RTD to 4-20mA without any external active circuitry. A discrete solution could be used to create a similar system using an ADC, MCU, and DAC such as the design featured in http://www.ti.com/tool/TIDA-00095.

9 About the Authors

Collin Wells is an applications engineer in the Precision Linear group at Texas Instruments where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

10 Acknowledgements & References

The author wishes to acknowledge NTS (National Technical Systems) in Plano, TX for their assistance performing the electromagnetic compatibility tests.

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8. *IEC Publication 61000-4-5 "Electromagnetic compatibility (EMC) - Part 4-5: Testing and measurement techniques - Surge immunity test," International Electrotechnical Commission, 2012.*
9. *IEC Publication 61000-4-6 "Electromagnetic Compatibility (EMC) – Part 4-6: Testing and Measurement Techniques – Immunity to Conducted Disturbances, Induced by Radio-Frequency Fields," International Electrotechnical Commission, 2008.*
10. *H. Ott, Electromagnetic Compatibility. John Wiley & Sons Inc., 2009.*

Appendix A.

A.1 Electrical Schematic

The Altium electrical schematic for this design can be seen in Figure 24.

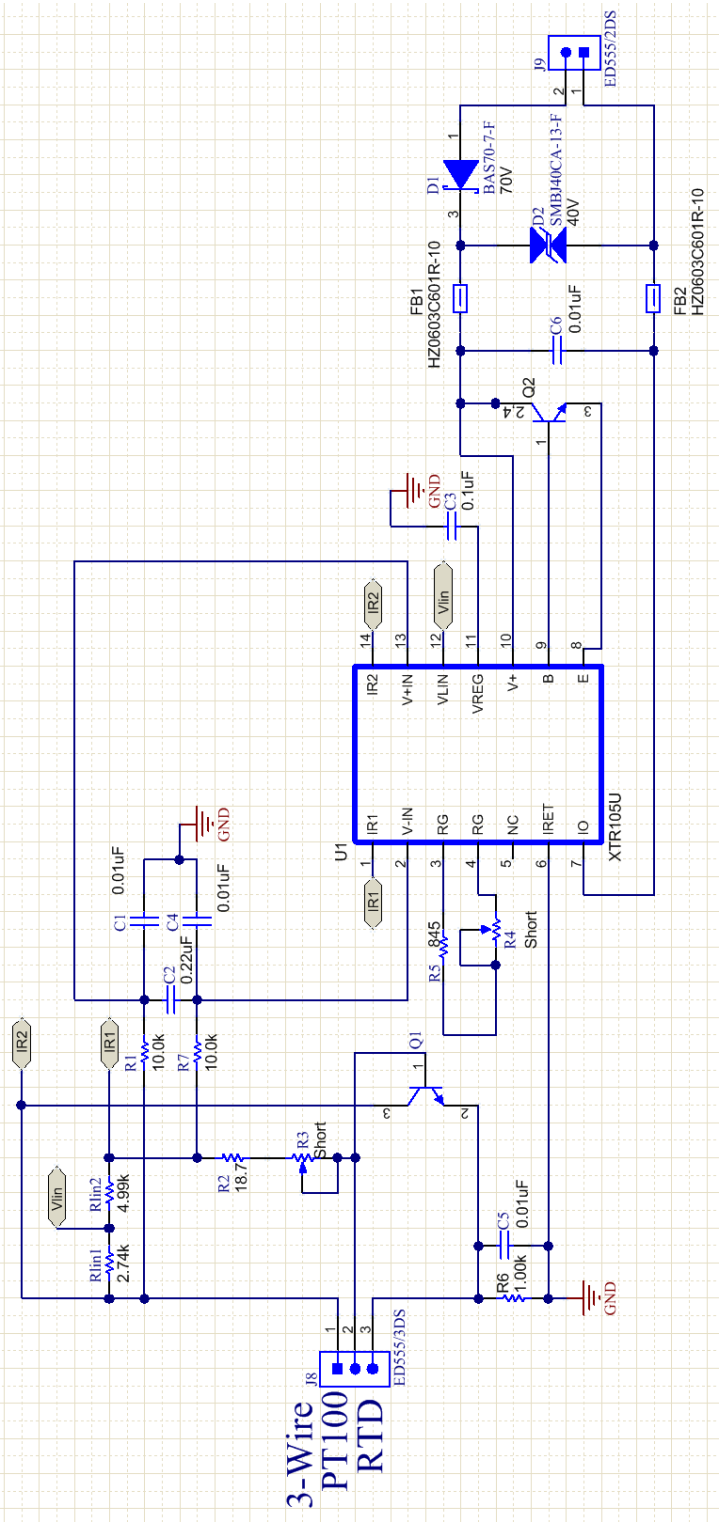

Figure 24: Altium Schematic

A.2 Bill of Materials

The bill of materials for this circuit can be seen in Figure 25.

Texas Instruments

Bill of Materials

TI DESIGNS

TIPD161: Single-Chip Analog Linearized 3-Wire RTD 2-Wire 4-20mA Transmitter Reference Design

Item #	Quantity	Designator	Value	Description	Manufacturer	Part Number
1	2	C1, C4	0.01uF	CAP, CERM, 0.01uF, 50V, +/-5%, C0G/NP0, 0805	TDK	C2012C0G1H103J
2	1	C2	0.22uF	CAP, CERM, 0.22uF, 50V, +/-10%, X7R, 0805	MuRata	GRM21BR71H224KA01L
3	1	C3	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0805	AVX	08055C104KAT2A
4	2	C5, C6	0.01uF	CAP, CERM, 0.01uF, 50V, +/-10%, X7R, 0805	MuRata	GRM216R71H103KA01D
5	1	D4		DIODE TVS ARRAY 15V SOD323	Bourns	CDSOD323-T15SC
6	2	FB1, FB2		300mA Ferrite Bead, 600 ohm @ 100MHz	Bourns	HZ0603C601R-10
7	1	J8		Terminal Block, 6A, 3.5mm Pitch, 3-Pos, TH	On-Shore Technology	ED555/3DS
8	1	J9		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS
9	1	Q1		Transistor, NPN, 45V, 0.1A, SOT-23	ON Semiconductor	BC847CLT1G
10	1	Q2		Transistor, NPN, 45V, 1A, SOT-89	Diodes Inc.	FCX690BTA
11	2	R1, R7	10.0k	RES, 10.0k ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW080510K0FKEA
12	1	R2	18.7	RES SMD 18.7 OHM 0.1% 1/4W 0805	TE Connectivity	5-1625868-3
13	1	R3	0	DNI - Short		
14	1	R4	0	DNI - Short		
15	1	R5	845	RES SMD 845 OHM 0.1% 1/10W 0805	TE Connectivity	1676446-2
16	1	R6	1.00k	RES, 1.00k ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW08051K00FKEA
17	1	Rlin1	2.74k	RES SMD 2.74K OHM 0.1% 1/10W	TE Connectivity	1676294-2
18	1	Rlin2	4.99k	RES SMD 4.99K OHM 0.1% 1/10W	TE Connectivity	RN73C2A4K99BTD
19	1	U1		IC, 4-20mA Current Transmitter with Sensor Excitation and Linearization	Texas Instruments	XTR105U

Figure 25: Bill of Materials

A.3 Manual Calibration Using Trim Potentiometers

The calibrated circuit results shown in Figure 12 were achieved using trim potentiometers to set the gain resistor, R_G, and zero resistor, R_Z, values as shown in Figure 26. The range of values for R_G and R_Z are shown in Table 11. The BOM featuring the hardware compensation components is shown in Figure 28.

Table 11: Comparison of Design Goals, Simulated, and Measured Performance

Calibration Element	Ideal Value	Calibration Range	Calibration % of Span
R_Z	18.52 Ω	13.7 Ω + 10 Ω	-26% to +28%
R_G	844.79 Ω	825 Ω +50 Ω	-2.34% to +3.58%

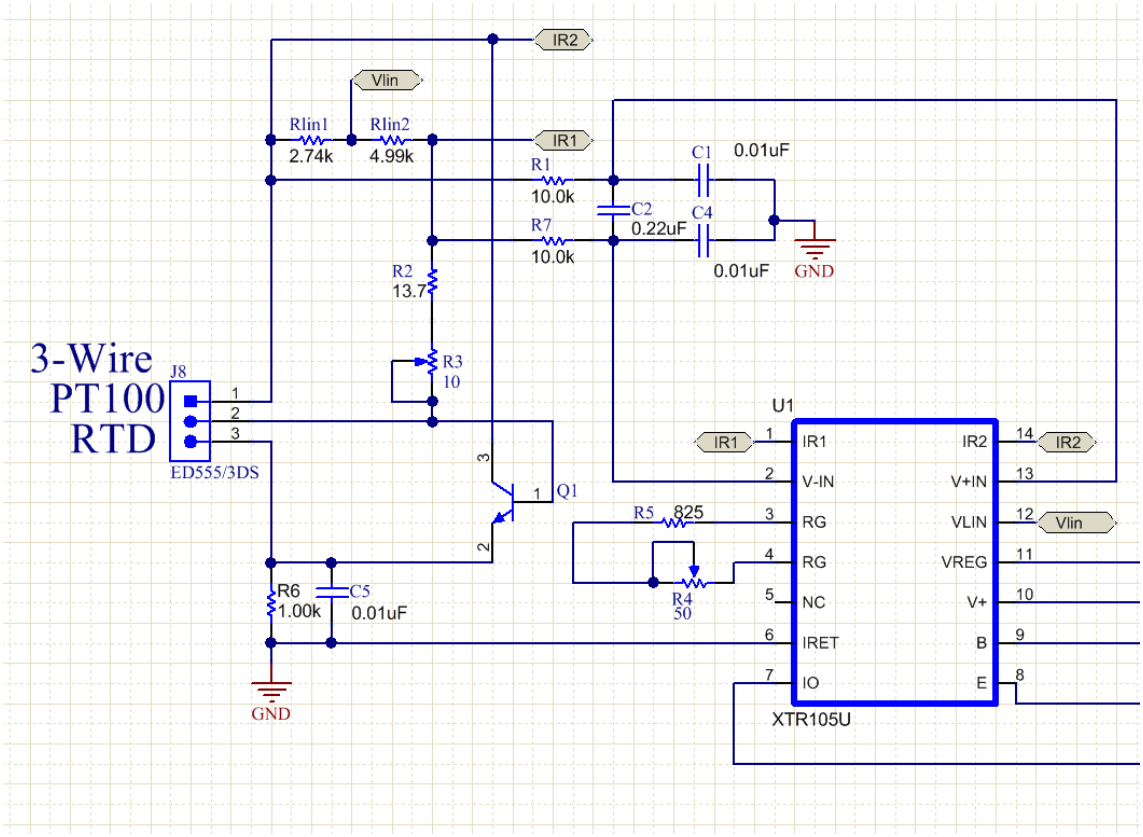

Figure 26: Schematic with Calibration Components Shown

The results from Figure 27 are shown in terms of output current (I_{OUT}) error to help explain the calibration process. The first step is to set the R_Z trim potentiometer with the RTD set to the minimum resistance (18.52 Ω). Adjust the output current to 3.99mA so at zero-scale the output will intersect the y-axis at 0.01mA below the ideal value of 4mA. Then adjust the R_G trim resistor so the output is 19.987mA with the RTD set to the maximum value (375.7 Ω). The output should then be verified with the RTD set to the mid-temperature value of 300ºC (212.05 Ω) and the output error should be very close to 12mA and can be adjusted up and down using the R_G trim resistor if any final adjustments are required.

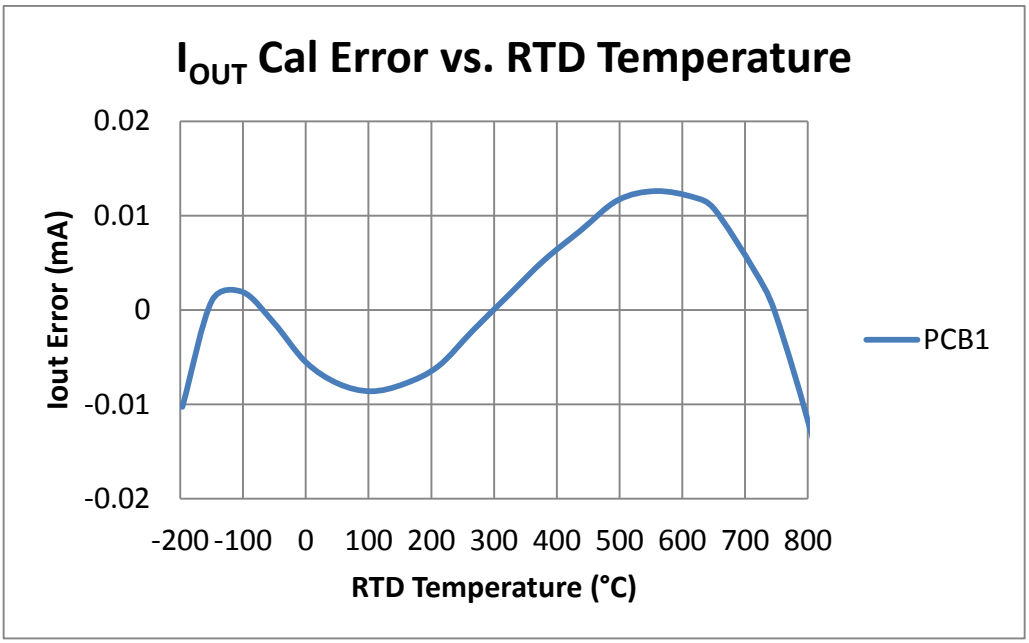

Figure 27: Calibrated Output Current Error vs. RTD Temperature

Texas Instruments

Bill of Materials

TI DESIGNS

TIPD161: Single-Chip Analog Linearized 3-Wire RTD 2-Wire 4-20mA Transmitter Reference Design

Item #	Quantity	Designator	Value	Description	Manufacturer	Part Number
1	2	C1, C4	0.01uF	CAP, CERM, 0.01uF, 50V, +/-5%, C0G/NP0, 0805	TDK	C2012C0G1H103J
2	1	C2	0.22uF	CAP, CERM, 0.22uF, 50V, +/-10%, X7R, 0805	MuRata	GRM21BR71H224KA01L
3	1	C3	0.1uF	CAP, CERM, 0.1uF, 50V, +/-10%, X7R, 0805	AVX	08055C104KAT2A
4	2	C5, C6	0.01uF	CAP, CERM, 0.01uF, 50V, +/-10%, X7R, 0805	MuRata	GRM216R71H103KA01D
5	1	D4		DIODE TVS ARRAY 15V SOD323	Bourns	CDSOD323-T15SC
6	2	FB1, FB2		300mA Ferrite Bead, 600 ohm @ 100MHz	Bourns	HZ0603C601R-10
7	1	J8		Terminal Block, 6A, 3.5mm Pitch, 3-Pos, TH	On-Shore Technology	ED555/3DS
8	1	J9		Terminal Block, 6A, 3.5mm Pitch, 2-Pos, TH	On-Shore Technology	ED555/2DS
9	1	Q1		Transistor, NPN, 45V, 0.1A, SOT-23	ON Semiconductor	BC847CLT1G
10	1	Q2		Transistor, NPN, 45V, 1A, SOT-89	Diodes Inc.	FCX690BTA
11	2	R1, R7	10.0k	RES, 10.0k ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW080510K0FKEA
12	1	R2	13.7	RES SMD 13.7 OHM 0.1% 1/4W 0805	TE Connectivity	4-1625868-0
13	1	R3	10	TRIMMER 10 OHM 0.75W PC PIN	Bourns	3006P-1-100LF
14	1	R4	50	TRIMMER, 10K, 0.75W, TH	Bourns	3006P-1-500LF
15	1	R5	825	RES SMD 825 OHM 0.1% 1/4W 0805	TE Connectivity	1-2176092-0
16	1	R6	1.00k	RES, 1.00k ohm, 1%, 0.125W, 0805	Vishay-Dale	CRCW08051K00FKEA
17	1	Rlin1	2.74k	RES SMD 2.74K OHM 0.1% 1/10W	TE Connectivity	1676294-2
18	1	Rlin2	4.99k	RES SMD 4.99K OHM 0.1% 1/10W	TE Connectivity	RN73C2A4K99BTD
19	1	U1		IC, 4-20mA Current Transmitter with Sensor Excitation and Linearization	Texas Instruments	XTR105U

Figure 28: Hardware Calibration Bill of Materials

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