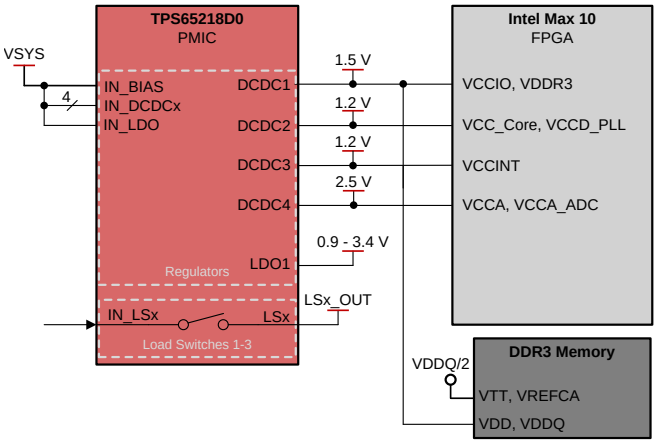
Test Report: TIDA-00607

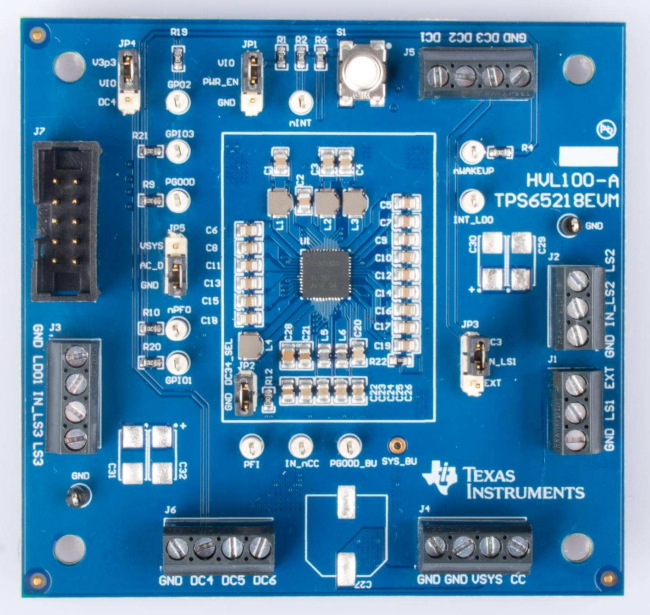
Powering the Intel® MAX® 10 FPGA With Power Management IC Reference Design

Description

This TPS65218D0-based reference design is a compact, integrated power solution for Intel® MAX® 10 FPGAs. This design showcases TPS65218D0 as an all-in-one PMIC used to supply the five rails needed for powering the MAX® 10 FPGAs. Intel offers a single supply and dual supply solution for the MAX 10. This TI Design is for the MAX 10 Dual Supply solution. The total board area needed for TPS65218D0, including passive components, to supply the five power rails to the MAX® 10 is just 1.594 in^2.

The TPS65218D0 has the flexibility to support either DDR3L or DDR3 memory and integrates three (3) load switches to enable or disable external peripherals in the system for managing power consumption. This power management IC can be run from a single 5-V supply or from a single cell Li-Ion battery. This design is ensured to operate across an industrial temperature range (-40°C to +105°C).





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1 Test Prerequisites

1.1 Voltage and Current Requirements

Table 1. Voltage and Current Requirements

PARAMETER	VOLTAGE (V)	CURRENT (A)	TPS65218D0 PIN OR RAIL NAME
V_{IN}	3.3 – 5	—	IN_BIAS, IN_DCDCx, IN_LDO1
VCCIO_1V5	1.5	Scalable	DCDC1
VDDR3	1.5	0.13	
VCC_Core	1.2	1.7	DCDC2
VCCD_PLL	1.2	0.01	
VCCINT	1.2	0.5	DCDC3
VCCA	2.5	0.1	DCDC4
VCCA_ADC	2.5	0.03	
VCCIO_3V3	3.3	Scalable	LDO1

1.2 Required Equipment

- TPS65218EVM-100 evaluation module
- IPG-UI software
- TPS65218D0 sample IC
- BOOSTXL-TPS65218 socketed EVM (optional)

1.3 Design Considerations

The TPS65218D0 operates over a range of input voltages from 2.7 V to 5.5 V, such that the system can be powered from a 5-V, line-powered supply. Another common voltage rail, such as 3.3 V, or any voltage in-between, can be used as the input to the TPS65218D0 device. Figure 1 shows the block diagram of this design. In applications that require LDO1 to provide 3.3 V for VCCIO_3V3, a supply voltage greater than 3.6 V is recommended.

Figure 1. Max 10 FPGA Power Supply Diagram

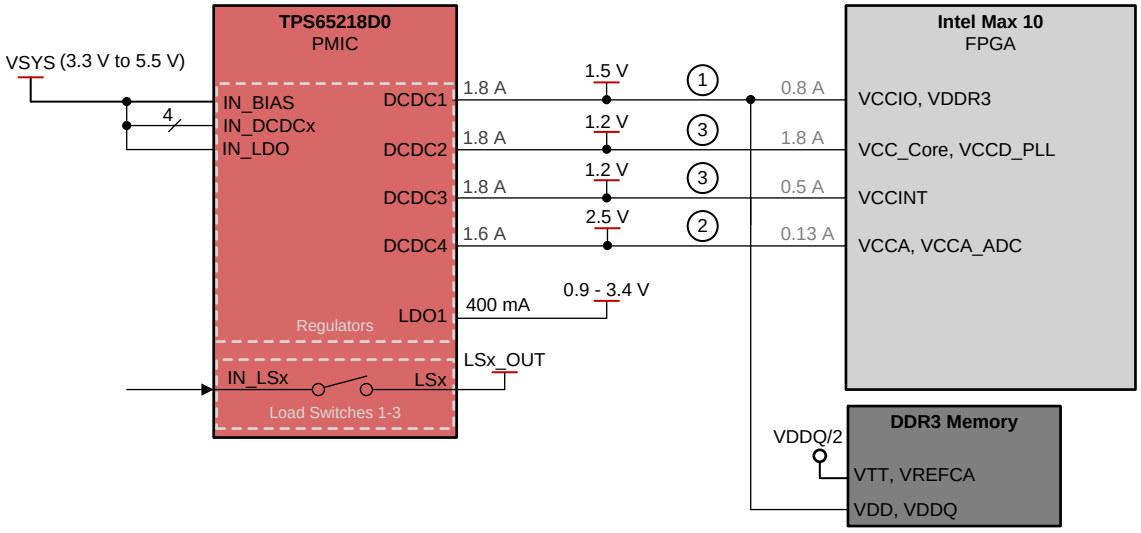


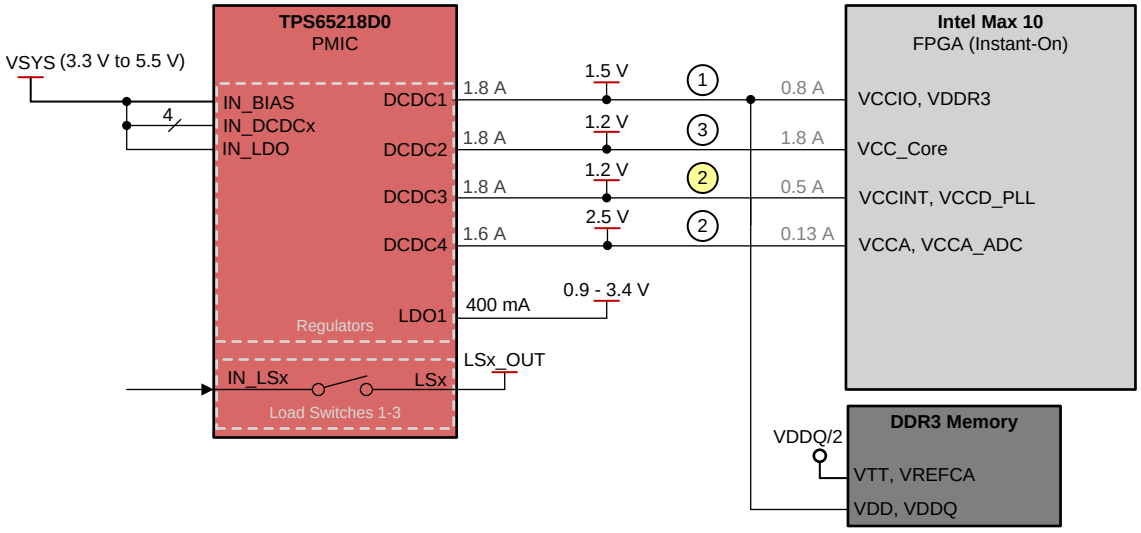
Table 2 lists the voltage settings required for the TPS65218D0 to power the Intel MAX 10 properly.

Table 2. Voltage Settings

Max 10 Rail	TPS65218D0 Regulator	Voltage (V)	Register Address (Name)	Register Value
VCCIO_1V5, VDDR3	DCDC1	1.5	0x16 (DCDC1)	0xB8
VCC_Core, VCCD_PLL	DCDC2	1.2	0x17 (DCDC2)	0xA3
VCCINT	DCDC3	1.2	0x18 (DCDC3)	0x8C
VCCA, VCCA_ADC	DCDC4	2.5	0x19 (DCDC4)	0xA2
VCCO_3.3V	LDO1	3.3	0x1B (LDO1)	0x3D

The Intel MAX 10 has an *Instant-On* feature, which allows the FPGA to wake up very quickly to begin operation. With Instant-On, the MAX 10 device can directly enter configuration mode without any POR delay after the POR trips for the monitored power supplies. This TI Design is for normal operation of the Intel MAX 10, but Figure 2 shows the connection diagram and sequencing number to support Instant-On for applications that require this feature. The new sequence order of each rail is circled in the diagram and the change in sequence order is highlighted.

Figure 2. Max 10 FPGA Power Supply Diagram for Instant-On



1.3.1 Intel® MAX® 10 Specific Design Requirements

For reference, the power connections of the Intel MAX 10 FPGA are described in Table 3, with the power pin name on the left and the MAX 10 dual-supply description on the right.

Table 3. Max 10 Power Pins

Pin Name	Description
VCC_Core	Power supply pin for core and peripherals
VCCIO (VCCIO_1V5 and VCCIO_3V3)	I/O supply voltage pins
VCCA	Power supply pins for analog PLL
VCCD_PLL	Power supply pins for digital PLL
VCCA_ADC	Power supply for ADC block
VCCINT	Power supply for ADC digital block

For MAX 10 single-supply devices, only one power supply is required—3.0 V or 3.3 V to power the core of the FPGA. The same power supply can be used to power the I/O if the same 3.0 V or 3.3 V voltage is required. If different I/O voltage is used, then additional voltage regulators will be needed.

For MAX 10 dual-supply devices, two power supplies are required to supply power to the device core, periphery, phase-locked loop (PLL), and analog-to-digital converters (ADC) blocks—1.2 V and 2.5 V. Depending on the I/O standard voltage requirement, you may use two or more voltage regulators. During power-up, the output buffers are tri-stated and the internal weak pull-up resistors are disabled by default.

Even though the MAX 10 does not require power sequencing, Intel recommends designing sequencing for the best device reliability. This can help prevent problems with long-term device reliability in multi-rail power systems. The TPS65218D0 and this TI Design support a power sequence to increase system reliability.

1.3.1.1 Instant-On Support

In some applications, it is necessary for a device to wake up very quickly to begin operation. The MAX 10 device offers the instant-on feature to support fast wake-up time applications. With the Instant-On feature, MAX 10 device can directly enter configuration mode without any POR (Power on Reset) delay after the POR trips for the monitored power supplies. Table 4 lists the Instant-On sequence recommendations for single and dual-supply systems.

Table 4. Instant-On Sequence Recommendations

Power Supply Option	Instant-On Power-Up Sequence
Single-supply	VCCIO rail must ramp up to full rail before VCCA and VCC_ONE start ramping
Dual-supply	All power supplies must ramp up to full rail before VCC_Core starts ramping

If your application does not require instant-on support, you can use the power sequence that is provided in the TI Design. Figure 2 in this document shows the connection diagram and sequencing order for Instant-On support.

1.3.1.2 Intel® MAX® 10 Pin Connection Guidelines

For reference, the sequencing requirements from the Intel MAX 10 datasheet are as follows:

- Connect VCCA to a 2.5V supply even if the PLL is not being used. All VCCA pins must be powered up and down at the same time.
- Connect VCCD_PLL to 1.2V supply even if the digital PLL is not being used.

1.3.2 TPS65218D0 Wake-up and Power Sequencing

The TPS65218D0 has a pre-defined power-up / power-down sequence which may need to be adjusted for each different SoCs, processors, or FPGAs. Re-programming the nonvolatile EEPROM memory of the TPS65218D0 device with I^2C control allows the user to change the sequence order and timing to match the target SoC, processor, or FPGA.

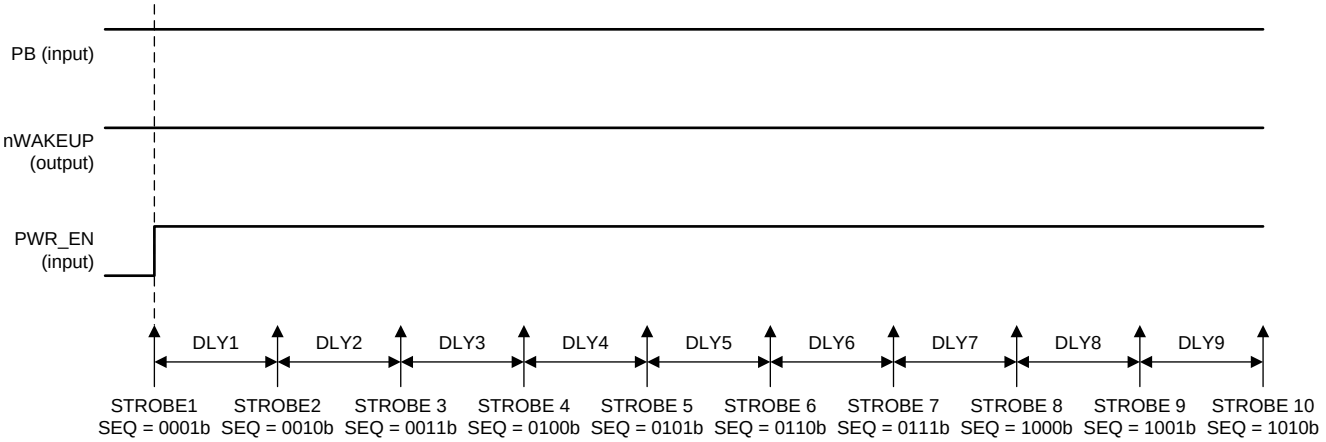
The power-up sequence is defined by a series of ten strobes and nine delay times. Each output rail is assigned to a strobe to determine the order in which the rails are enabled. A rail can be assigned to only one strobe, but multiple rails can be assigned to the same strobe. The delay times in-between strobes are selectable between 2 ms and 5 ms.

1.3.2.1 General Power-Up Sequencing

When the power-up sequence initiates, STROBE1 occurs, and any rail assigned to this strobe is enabled.

After a delay time of DLY1, STROBE2 occurs and the rail assigned to this strobe is powered up. The sequence continues until all strobes occur and all DLYx times execute. Strobe assignments and delay times are defined in the SEQx registers, and are changed under I^2C control. Figure 3 shows a timing diagram detailing the power sequence when PWN_EN is the power-up event leaving the SUSPEND state. For further information on power up/down sequence, please consult the TPS65218D0 data sheet. Power-down sequencing follows the reverse order of power-up sequencing.

Figure 3. TPS65218D0 Power-Up from SUSPEND State (PWR_EN Set High)



1.3.2.2 TPS65218D0 Adjusted Sequencing for Intel® MAX® 10

Table 5 lists the strobe assignments required for the TPS65218D0 to power the Intel MAX 10 properly. The delay (DLY1-9) between each strobe can also be adjusted in registers 0x20 (SEQ1) and 0x21 (SEQ2, bit 0) and multiplied by a factor of 1 or 10 (SEQ2, bit 7). Each bit in SEQ1 and bit 0 of SEQ2 can be set to 0b for a delay of 2 ms or set to 1b for a delay of 5 ms. Bit 7 of SEQ2 can be set to 0b for a factor of 1x or set to 1b for a factor of 10x. For this design, all delays will be kept at the defaults of 2 ms with a delay factor of 1x. As a result, the data in both registers, 0x20 and 0x21, will be 0x00.

Table 5. Strobe Assignments

Max 10 Rail	TPS65218D0 Regulator	Strobe #	Register Address (Name)	Register Value
VCCIO_1V5, VDDR3	DCDC1	3	0x22 (SEQ3)	0x73
VCC_Core, VCCD_PLL	DCDC2	7		
VCCINT	DCDC3	7	0x23 (SEQ4)	0x57
VCCA, VCCA_AUX	DCDC4	5		
VCCIO_3V3	LDO1	9	0x25 (SEQ6)	0xA9

2 Testing and Results

2.1 Efficiency Graphs

Figure 4 shows the efficiency curve for DCDC1, set to output a voltage of 1.5 V for the VCCIO_1V5 and VDDR3 rail.

Figure 5 shows the efficiency curve for DCDC2, set to output a voltage of 1.2 V for the VCC_Core and VCCD_PLL rails.

Figure 4. DCDC1 Efficiency vs Load Current, T_A = 25 °C

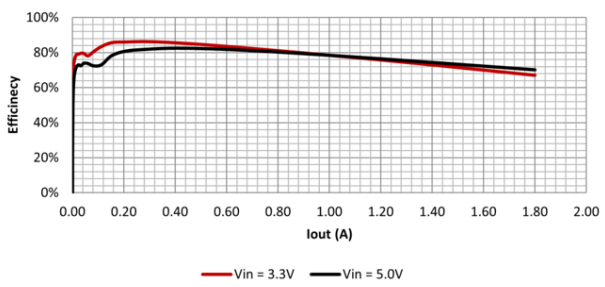


Figure 5. DCDC2 Efficiency vs Load Current, T_A = 25 °C

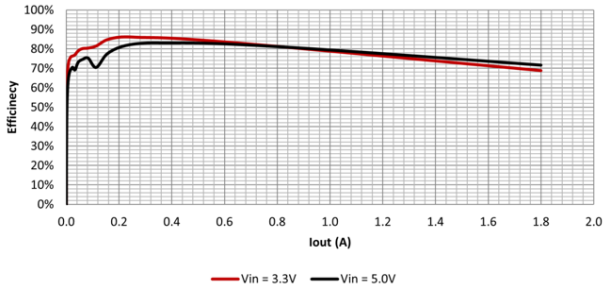


Figure 6 shows the efficiency curve for DCDC3, set to output a voltage of 1.2 V for the VCCINT rail.

Figure 7 shows the efficiency curve for DCDC4, set to output a voltage of 2.5 V for the VCCA and VCCA_ADC rails.

Figure 6. DCDC3 Efficiency vs Load Current, T_A = 25 °C

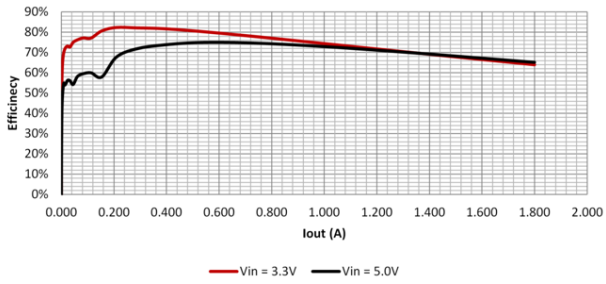
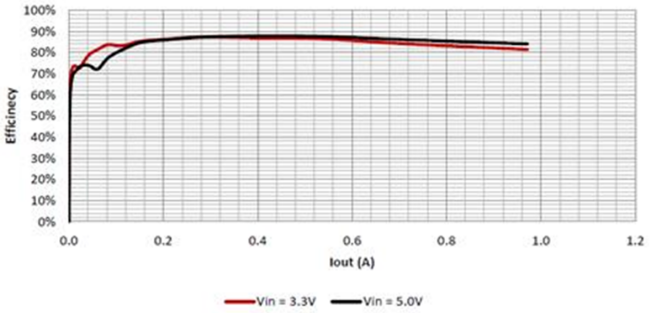


Figure 7. DCDC4 Efficiency vs Load Current, T_A = 25 °C



2.2 Load Regulation

Figure 8 shows the load regulation plot for DCDC1.

Figure 9 shows the load regulation plot for DCDC2.

Figure 8. DCDC1 Load Regulation, T_A = 25 °C

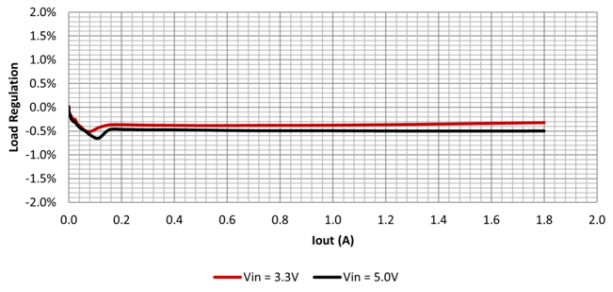


Figure 9. DCDC2 Load Regulation, T_A = 25 °C

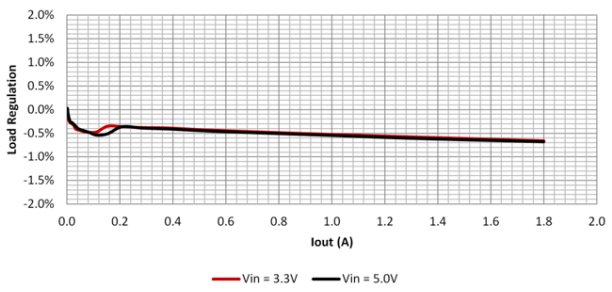


Figure 10 shows the load regulation plot for DCDC3.

Figure 11 shows the load regulation plot for DCDC4.

Figure 10. DCDC3 Load Regulation, T_A = 25 °C

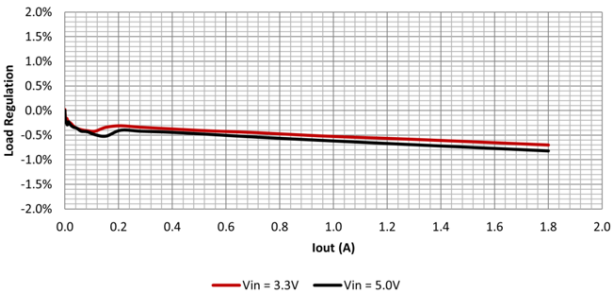
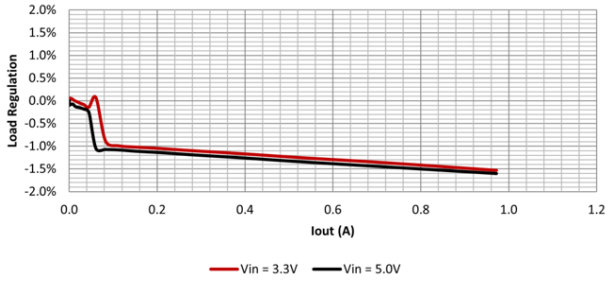


Figure 11. DCDC4 Load Regulation, T_A = 25 °C

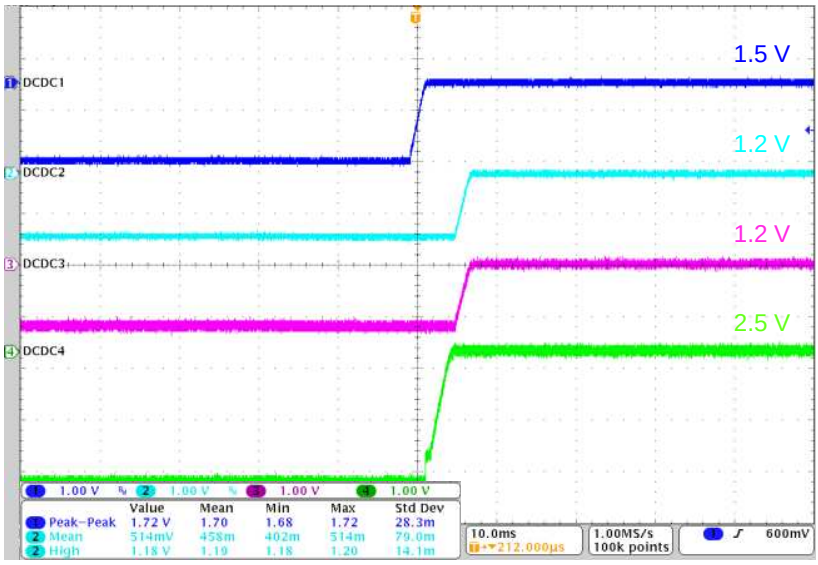


3 Waveforms

3.1 Start-up Sequence

Figure 12 shows the start-up (or power-up) sequence of the TPS65218D0 rails programmed for the MAX 10 with no load applied.

Figure 12. Power-Up Sequence (No Load) Voltage and Timing Waveforms



3.2 Output Voltage Ripple

Figure 13 shows the measured output voltage ripple for DCDC1 at the maximum typical load of the VCCIO_1V5 and VDDR3 rails.

Figure 14 shows the measured output voltage ripple for DCDC2 at the maximum typical load of the VCC_Core and VCCD_PLL rails.

Figure 13. DCDC1 Output Voltage Ripple

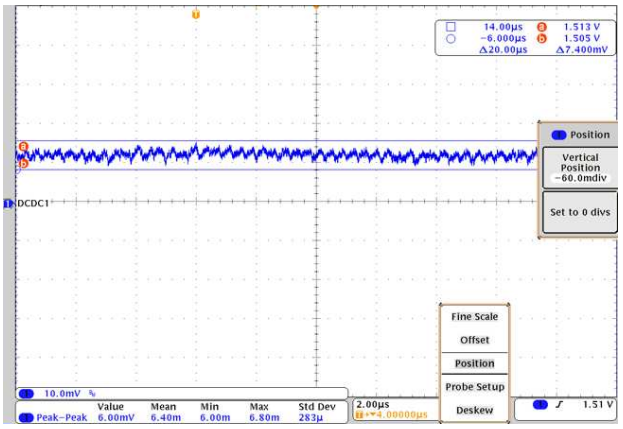


Figure 14. DCDC2 Output Voltage Ripple

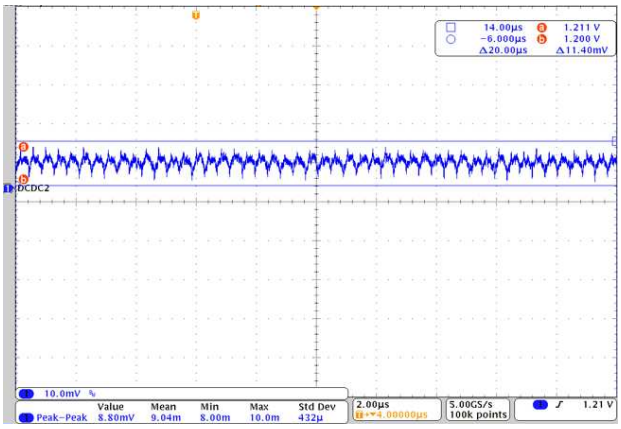


Figure 15 shows the measured output voltage ripple for DCDC3 at the maximum typical load of the VCCINT rail.

Figure 16 shows the measured output voltage ripple for DCDC4 at the maximum typical load of the VCCA and VCCA_ADC rails.

Figure 15. DCDC3 Output Voltage Ripple

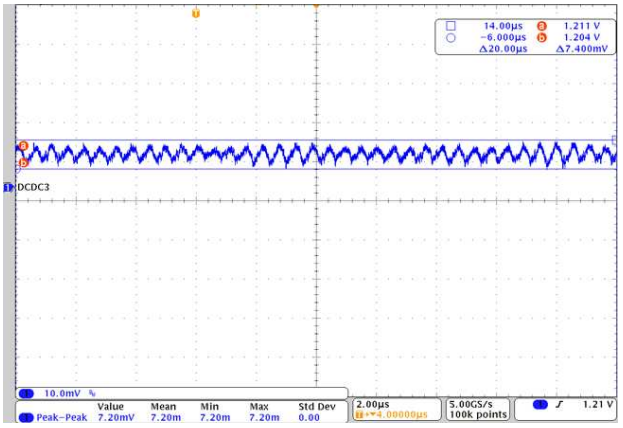
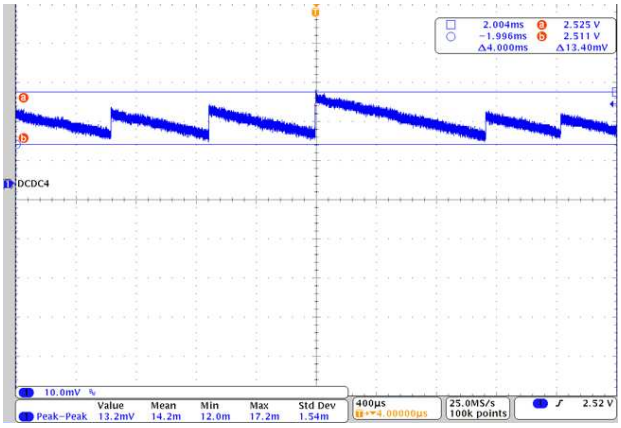


Figure 16. DCDC4 Output Voltage Ripple



3.3 Load Transients

Figure 17 shows the measured load transient response for DCDC1 for a step from 0 mA to 975 mA.

Figure 18 shows the measured load transient response for DCDC2 for a step from 0 mA to 975 mA.

Figure 17. DCDC1 Load Transient Response (0 mA to 975 mA)

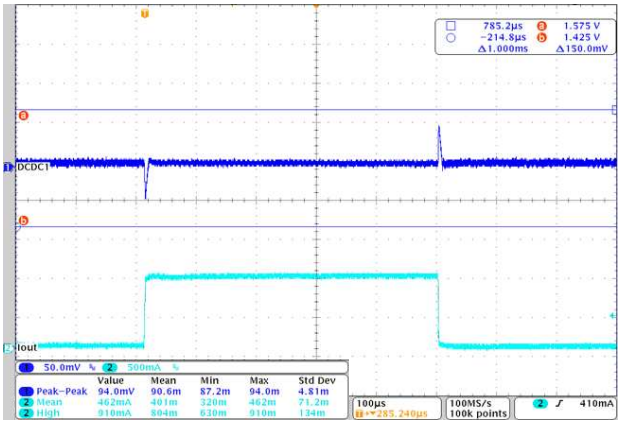


Figure 18. DCDC2 Load Transient Response (0 mA to 975 mA)

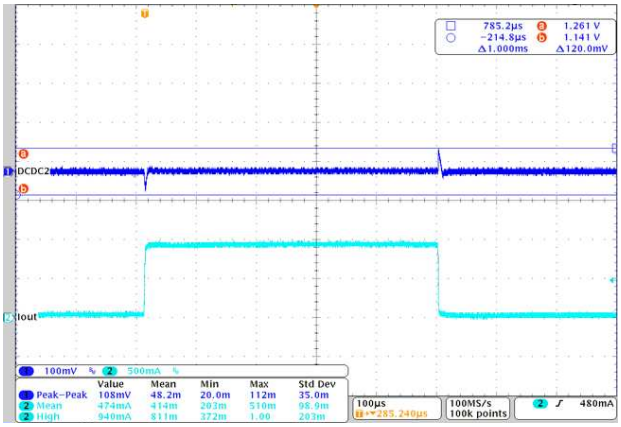


Figure 19 shows the measured load transient response for DCDC3 for a step from 0 mA to 975 mA.

Figure 20 shows the measured load transient response for DCDC4 for a step from 0 mA to 500 mA.

Figure 19. DCDC3 Load Transient Response (0 mA to 975 mA)

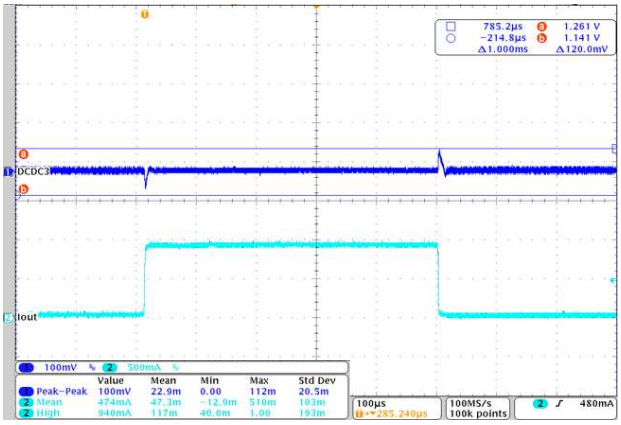
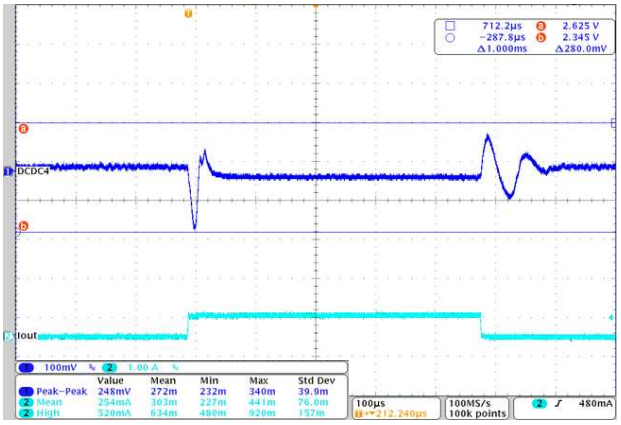


Figure 20. DCDC4 Load Transient Response (0 mA to 500 mA)



4 Next Steps

After reviewing this test report, the next steps towards building a design using the TPS65218D0 PMIC for an Intel MAX 10 FPGA are simple. The EEPROM of TPS65218D0 samples can be re-programmed using a socketed BOOSTXL-TPS65218 BoosterPack EVM and an MSP430F5529 LaunchPad. The output voltage settings and sequencing outlined in this document are modified and re-programmed into the TPS65218D0 nonvolatile memory using the IPG-UI software.

The re-programmed TPS65218D0 sample is then soldered down onto the TPS65218EVM-100 board to evaluate the performance and obtain the same results captured in this documentation. If this documentation is sufficient to prove the TPS65218D0 PMIC will work in the final application, the re-programmed TPS65218D0 sample can be soldered directly into a prototype board and evaluated for use in the final application.

Although the scope of this document is limited to powering the Intel MAX 10 FPGA, the TPS65218D0 device can be used to power a wide variety of SoCs, processors, and FPGAs using this same workflow.

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