TI Designs

High-Accuracy, Fast-Settling, ±10-V Analog Voltage Output Reference Design

TI Designs - Precision

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Resources

TIPD192	Design Folder
TINA-TI™	Software Folder
DAC8832	Product Folder
OPA4192	Product Folder
REF5050	Product Folder

Circuit Description

This circuit performs the function of producing a ±10-V voltage output where both a high level of accuracy and a fast update rate are desired. These features are achieved by combining the fast settling time and precision of a 16-bit unbuffered R-2R digital-to-analog converter (DAC) DAC8832 and the low-input offset voltage and fast slew rate of two output amplifier stages (OPA4192). The circuit provides an analog output voltage that is useful for precisely tuning feedback circuits as well as driving off-board components.

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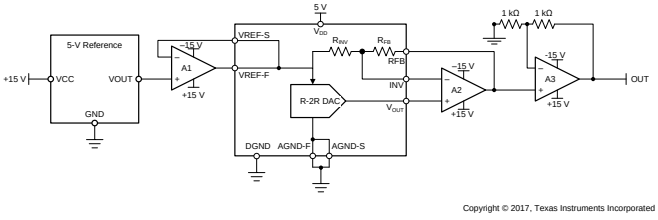

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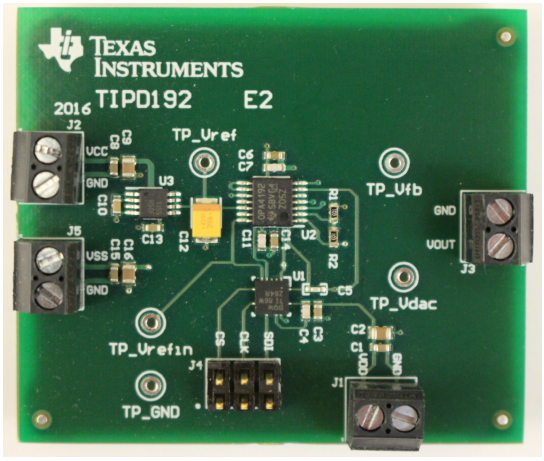

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1 Design Summary

The design requirements are as follows:

- Supply voltage: ±15 V (analog), 5 V (digital)
- Input: Three-wire, 16-bit serial peripheral interface (SPI)
- Output: –10 V to +10 V
- Settling time: ≤ 5 µs to 2 least significant bits (LSBs), ¼ scale to ¾ scale
- System total unadjusted error (TUE): ≤ 0.1% full-scale range
- Flicker noise: ≤ 0.5 LSB pk-pk

Table 1 summarizes the design goals and performance. Figure 1 shows the measured TUE of the design.

Table 1. Comparison of Design Goals, Simulation and Measured Performance

SPECIFICATION	GOAL	SIMULATED	MEASURED
System total unadjusted error (%FSR)	≤ 0.1%	0.088%	.00272%
Settling time	≤ 5 µs	4.2 µs	3.3 µs
Flicker noise	≤ 0.5 LSB pk-pk	0.2 LSB pk-pk	.134 LSB pk-pk

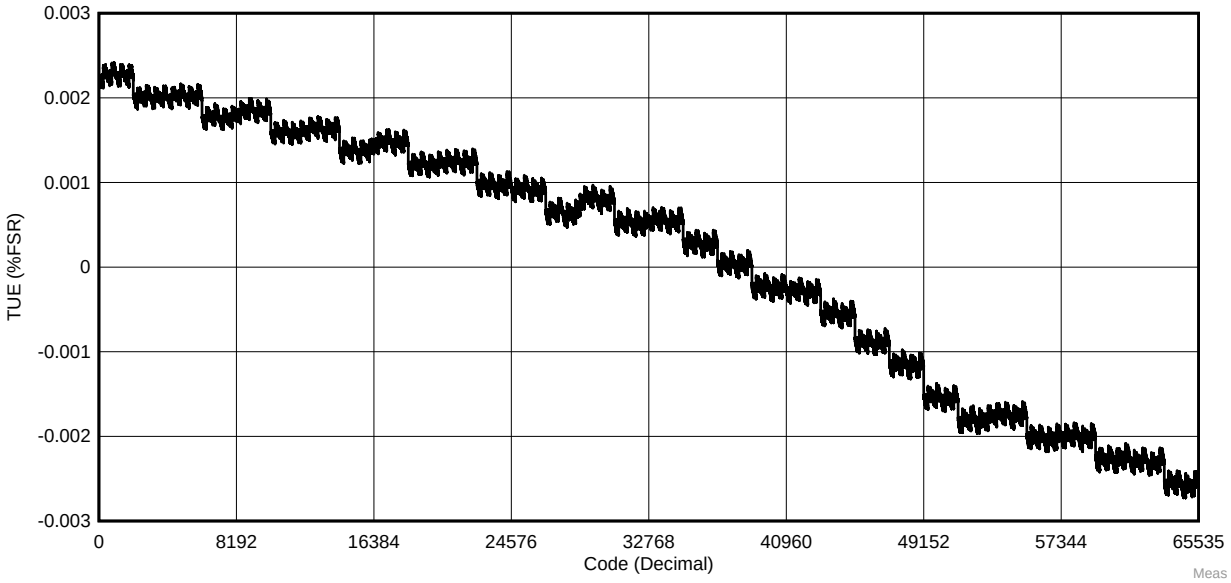

Figure 1. Measured Total Unadjusted Error

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2 System Description

Figure 2 shows a block diagram of the entire system, including some of the internal mechanics of the DAC.

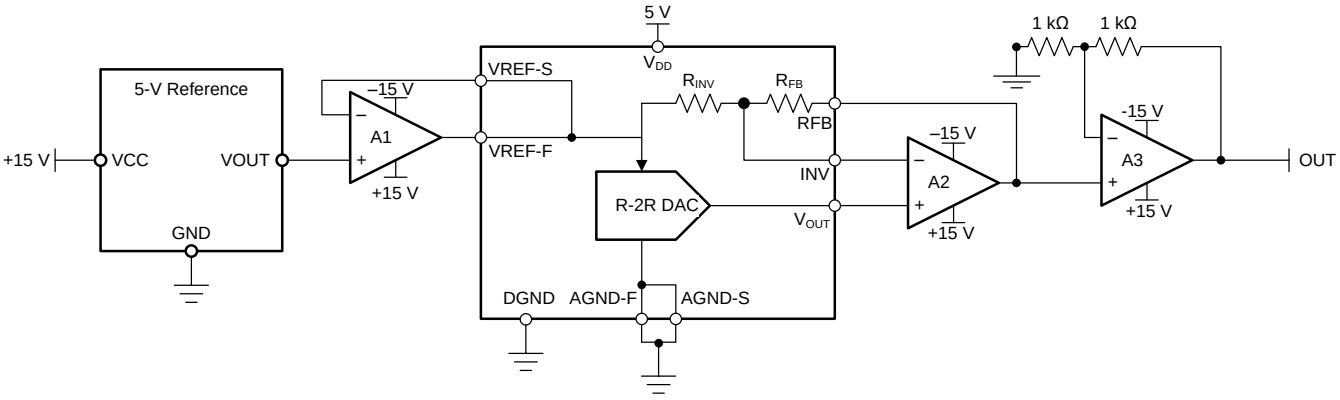

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Figure 2. Simplified Block Diagram

This design has three separate stages: the reference input, the bipolar DAC, and the final gain stage. Each of these stages are described in detail in the following sections.

2.1 Reference Input

The DAC chosen for this design does not have an internal reference, so an external one must be implemented.

A 5-V series voltage reference has been selected and an operational amplifier (op amp) is used as the reference driver as Figure 3 shows. The reference driver helps to minimize loading of the reference device, as most references are sensitive to small loads. The driver also allows use of the force and sense connections at the DAC reference input to ensure a precise 5-V reference voltage at the VREF-F pin. The reference voltage is driven by the amplifier on the force line by the output and sensed at the inverting input.

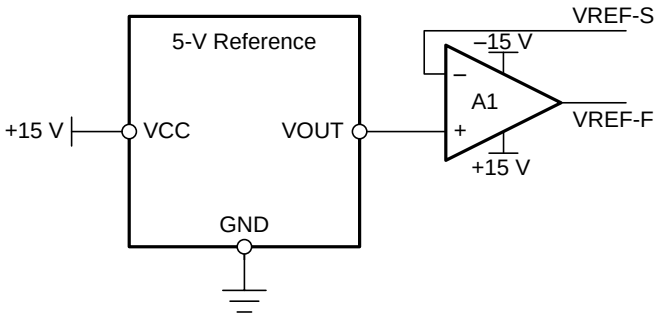

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Figure 3. Schematic Segment – Reference Input

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2.2 Bipolar DAC

The bipolar DAC stage consists of the DAC and one amplifier. Figure 4 shows a simplified block diagram of this stage with the internal structure of the DAC.

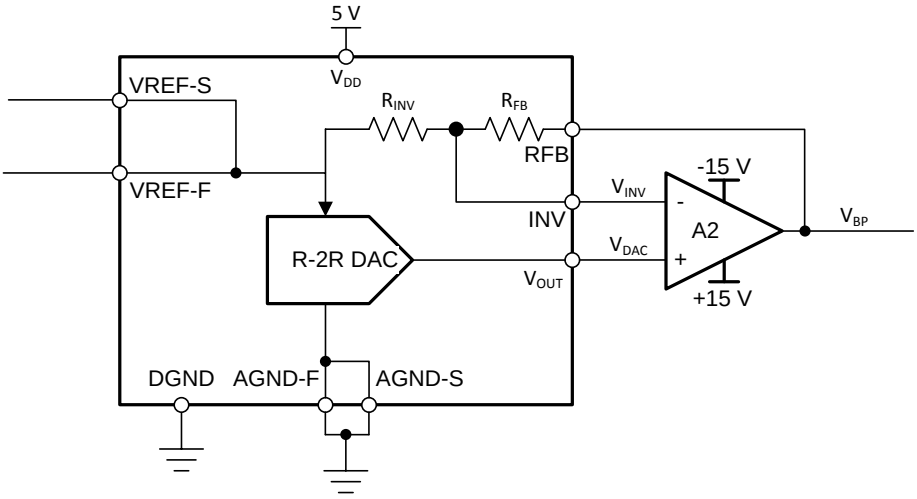

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Figure 4. Schematic Segment – Bipolar DAC

A standard voltage output DAC has an output based on the reference voltage; this relationship is defined in Equation 1.

$$V_{DAC} = V_{REF} \frac{CODE}{2^N} \tag{1}$$

Where V_{REF} is the reference voltage on the VREF-F pin, CODE represents the input code to the DAC in decimal form and N is the resolution of the DAC.

In the preceding Figure 4, V_{INV}, the voltage at the INV output of the DAC and the input to the inverting terminal of the amplifier is defined by Equation 2. V_{BP} is the output of the amplifier.

$$V_{INV} = (V_{BP} - V_{REF}) \frac{R_{INV}}{R_{FB} + R_{INV}} \tag{2}$$

Assuming an ideal amplifier ($V_{DAC} = V_{INV}$), the user can surmise the ideal transfer function for the voltage V_{BP} in Equation 3 using Equation 1 and Equation 2.

$$V_{BP} = V_{REF} \left(\frac{CODE}{2^N} \left(\frac{R_{FB} + R_{INV}}{R_{INV}} \right) - 1 \right) \tag{3}$$

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2.3 Final Gain Stage

The last stage is a gain stage that gains the potential at the V_{BP} node by 2. Figure 5 shows the gain configuration.

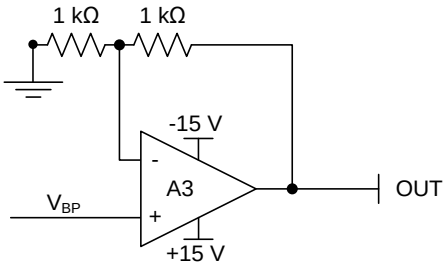

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Figure 5. Schematic Segment - Final Gain Stage

Adding a gain of 2 to Equation 3, Equation 4 shows the final system output equation.

$$V_{OUT} = 2 \times V_{REF} \left(\frac{CODE}{2^N} \left(\frac{R_{FB} + R_{INV}}{R_{INV}} \right) - 1 \right) \quad (4)$$

The internal resistors R_{FB} and R_{INV} are specified to be extremely close matched ®$_{FB}$ = R_{INV}), so the resistor ratio in Equation 4 reduces to 2.

Therefore, Equation 5 is the ideal description of the system.

$$V_{OUT} = 2 \times V_{REF} \left(2 \times \left(\frac{CODE}{2^N} \right) - 1 \right) \quad (5)$$

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3 Component Selection

3.1 DAC Selection

The DAC8832 has been chosen for this design because of low DNL, INL, offset, and gain errors and also for its fast settling time. Figure 6 shows the internal architecture of this DAC.

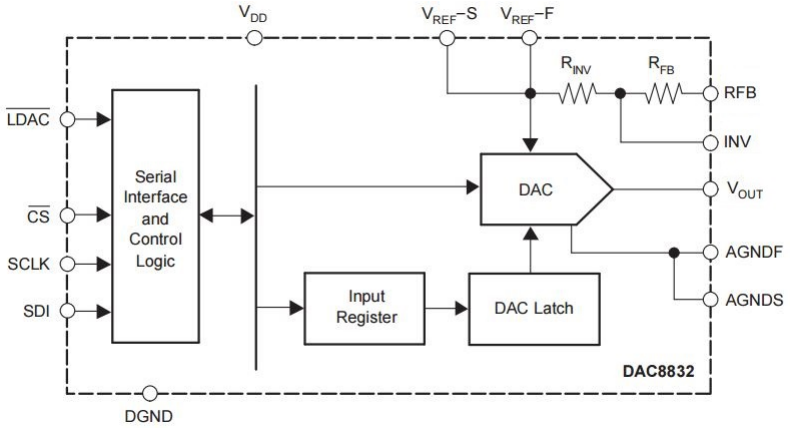

Figure 6. DAC8832 Block Diagram

The objective of this design is to quickly and accurately transition from one code to the next, which makes both settling time and DC specifications paramount in this application. The unbuffered architecture of DAC8832 exhibits fast settling time (1 µs) and very-low DC errors, which make this DAC an ideal choice for this design. In addition, the SPI digital interface for DAC8832 is also easy to use as the device has only one register to program.

3.2 Amplifier Selection

Three amplifiers are required in this design (see Figure 2): A1 is used as a reference buffer, A2 to generate a bipolar output from the unipolar DAC, and A3 to gain the signal by two. The reference buffer amplifier (A1) must be able to maintain a steady, accurate voltage level while the other two amplifiers, A2 and A3, must feature both DC accuracy and fast settling time.

In this application, slew rate and input offset voltage are critical specifications when choosing an amplifier. The design calls for a fast settling output, which requires that the slew rate of the output amplifier be high. For this design, a full-scale transition (20-V span) in 5 µs requires a 4-V/µs slew rate at the least. Additionally, for high DC accuracy, the amplifier must have a low-input offset voltage.

The OPA4192, a quad-channel amplifier, has been chosen for this design for both its AC and DC specifications. The slew rate of the amplifier is 20 V/µs and the input offset voltage is typically ±5 µV. In addition, this amplifier also exhibits low output noise (5.5 nV/$\sqrt{\text{Hz}}$ at 1 kHz).

3.3 Reference Selection

The onboard reference must have a low temperature drift and high initial accuracy to maintain a high DC accuracy across a wide temperature range. With a temperature coefficient of 2.5 ppm/°C and initial accuracy of 0.05%, the REF5050 has been chosen for this design.

3.4 Passive Component Selection

All of the capacitors in this design have been chosen based on the suggestions given in the datasheets of the active devices. The feedback resistors on the output require 0.1% tolerances to achieve the design goals. Resistors with tight tolerance must be used to minimize resistor contributions to gain and offset errors of the system. A resistance of 1 KΩ has been chosen as a balance between power consumption and contribution to thermal noise.

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4 Simulation

Simulation of this design was performed using theTINA-TI™ software available for free to all users. TI provides SPICE models for some of its devices and users can simulate with these models in the TINA software.

Simulation for TIPD192 was performed using the schematic that Figure 7 shows, which is available in the design files that accompany TIPD192. The simulation includes all of the active and passive components in the circuit except for the voltage reference, which is substituted for an idea voltage source. This simulation schematic uses the DAC8831 device in the circuit, which has same internal structure as the DAC8832 except for a power-on reset voltage. Because the power-on reset functionality is not built into the model and is not a part of these simulations, this difference can be disregarded.

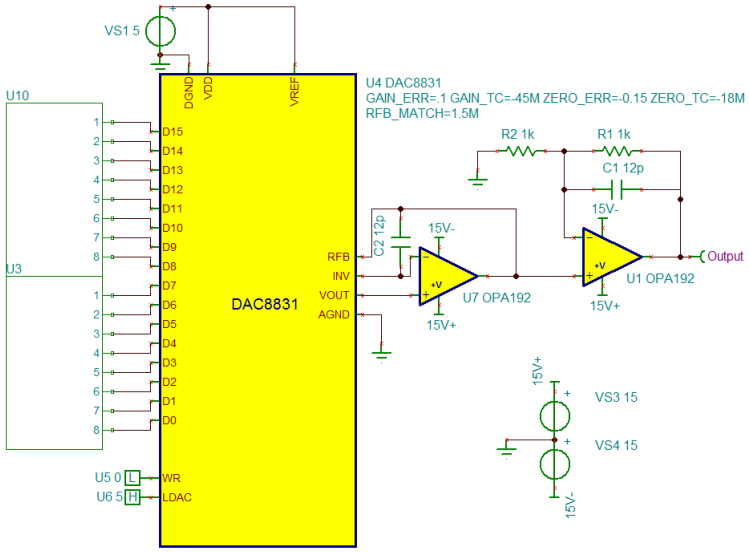

Figure 7. TINA-TI™ Simulation Schematic

4.1 Transfer Function

Figure 8 shows the simulated transfer curve for the input code versus the output. The simulation file used to generate this graph is included in the design file. The DAC spice model includes parameters to simulate gain error and zero error (and their respective temperature drift coefficients) to better match the true behavior of the device. For this simulation, the parameters are set to match the typical characteristics as listed in the datasheet.

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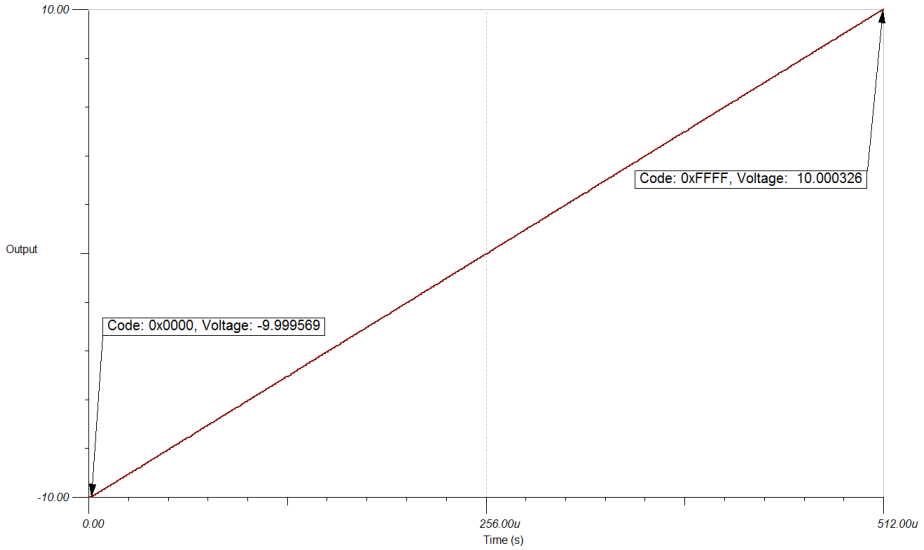

Figure 8. TINA-TI™ Simulated Transfer Function

4.2 Total Unadjusted Error

From the data collected, the endpoints plotted on the graph represent the full-scale and zero-scale outputs and can be used to calculate the simulated TUE of the system. The following results in Table 2 have been obtained using Equation 12 through Equation 15, substituting the data from the graph and the INL from the datasheet (1 LSB for DAC8832).

Table 2. TINA-TI™ Simulated TUE

OFFSET ERROR	GAIN ERROR	INL ERROR	TUE
.00216%	.0105%	.00153%	.0108%

4.3 Noise

The flicker noise is calculated cumulatively at three points: at the reference input to the DAC, the output of the first gain amplifier, and the output of the second gain amplifier.

The noise at the DAC reference input has contributions from the precision voltage reference and the amplifier to drive its output. From the component datasheets, the REF5050 contributes 15 μV_{PP} on its output and the amplifier A1 (OPA4192) contributes 1.3 μV_{PP} on its output. Because the gain configuration of the reference driver is unity, the noise at the reference pin of the DAC (E_{N1}) is calculated in Equation 6:

$$E_{N1} = \sqrt{15^2 + 1.3^2} = 15.06\ \mu V_{PP} \quad (6)$$

The noise at the output of the first gain amplifier has contributions from the reference noise (E_{N1}), the DAC (which includes the feedback resistors), and the amplifier A2. From the datasheet, the DAC contributes 18nV/$\sqrt{Hz}$, so the peak-to-peak contribution is calculated in Equation 7:

$$E_{NDAC} = 18 \times \sqrt{10} \times 6 = 0.341\ \mu V_{PP} \quad (7)$$

The typical value of the internal feedback resistors is 28 kΩ; therefore, the noise contribution from these resistors is calculated in Equation 8:

$$E_{NRFB} = 6 \times \sqrt{4 \times 1.38 \times 10^{-23} \times 300 \times 14000 \times 10} = 0.289\ \mu V_{PP} \quad (8)$$

As previously noted, the OPA4192 contributes 1.3 μV_{PP} of noise to the circuit. With a gain of 2 in this stage, the total noise at the output of the first gain amplifier A2 (E_{N2}) is calculated in Equation 9:

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$$E_{N2} = 2 \times \sqrt{15.06^2 + 0.341^2 + 0.289^2 + 1.3^2} = 30.25\ \mu V_{PP} \quad (9)$$

Lastly, the noise at the output of the second gain amplifier (A3) has contributions from the amplifier input (E_{N2}), the feedback resistors, and the amplifier (A3). The value of the feedback resistors used in this stage is 1 kΩ; therefore, the noise contribution from these resistors is calculated in Equation 10:

$$E_{NRFB} = 6 \times \sqrt{4 \times 1.38 \times 10^{-23} \times 300 \times 500 \times 10} = 0.054\ \mu V_{PP} \quad (10)$$

With a gain of two in this stage, the final output noise (E_{NOUT}) is calculated in Equation 11 to be:

$$E_{NOUT} = 2 \times \sqrt{30.25^2 + 0.054^2 + 1.3^2} = 60.55\ \mu V_{PP} \quad (11)$$

This calculated noise of 60.55 μV_{PP} equates to 0.2 LSB of noise, which meets the design requirement of 0.5 LSB of noise.

4.4 Settling Time

Figure 9 shows the simulation of the small-signal settling time for the output of the circuit. This capture was taken for the DAC transitioning from ¼ scale (code x4000) to ¾ scale (code xC000), or a transition from –5 V to 5 V at the output for this design. The marker shows the point at which the DAC has settled to within the ±2 LSB window defined as the goal for this design. The code transition takes place at 5 µs in this capture; therefore, the settling time is calculated to be ≈4.2 µs.

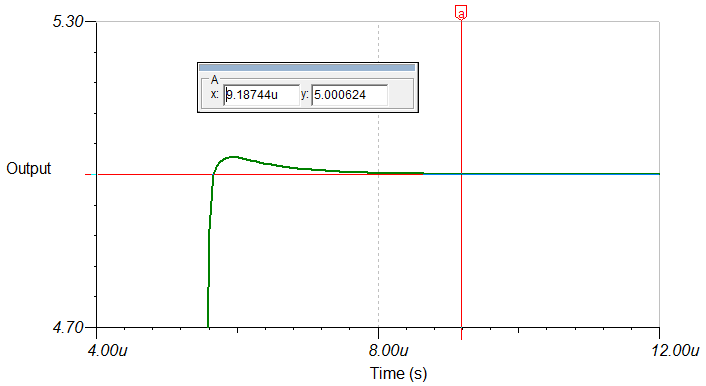

Figure 9. TINA-TI™ Simulated Small-Signal Settling

4.5 Error Equations

The TUE is a metric for the DC accuracy of a precision DAC design. Three main components comprise a TUE: offset error, gain error, and INL error. Gain and offset errors are calculated using Equation 12 and Equation 13.

$$\text{OffsetError}[\%FSR] = \frac{\left|V_{zero,meas} - V_{zero,ideal}\right|}{V_{FSR}} \times 100 \quad (12)$$

$$\text{GainError}[\%FSR] = \frac{\left|(V_{FS,meas} - V_{zero,meas}) - (V_{FS,ideal} - V_{zero,ideal})\right|}{V_{FSR}} \times 100 \quad (13)$$

INL error is usually specified in the datasheet in LSBs, so to include the INL in the TUE calculation the designer must convert it from LSBs to %FSR, which can be done by using Equation 14.

$$\text{INLError}[\%FSR] = \frac{\text{INL}[LSB]}{2^n} \times 100 \quad (14)$$

TUE is calculated by taking a root-sum-squared (RSS) approach of adding the DC errors in the system together, as these errors are uncorrelated. TUE is calculated using Equation 15.

$$\text{TUE} = \sqrt{\text{OffsetError}^2 + \text{GainError}^2 + \text{INLError}^2} \quad (15)$$

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5 Verification and Measured Performance

SPI communication was controlled using a National Instruments PXI-6289 card. Voltage measurements for TUE, linearity, gain, and offset were taken with an HP 3458A digital multimeter. Noise was measured with a 0.1-Hz to 10-Hz noise characterization circuit and the data was captured with a LeCroy WaveSurfer™ 3054 digital oscilloscope. Settling time was captured with the National Instruments PXI-5922 card. Power for the board came directly from the HP E3631A triple-rail power supply.

5.1 Transfer Function

The voltage at all codes (decimal 0 to 65535) was measured at the output of the design yielding the transfer function in Figure 10.

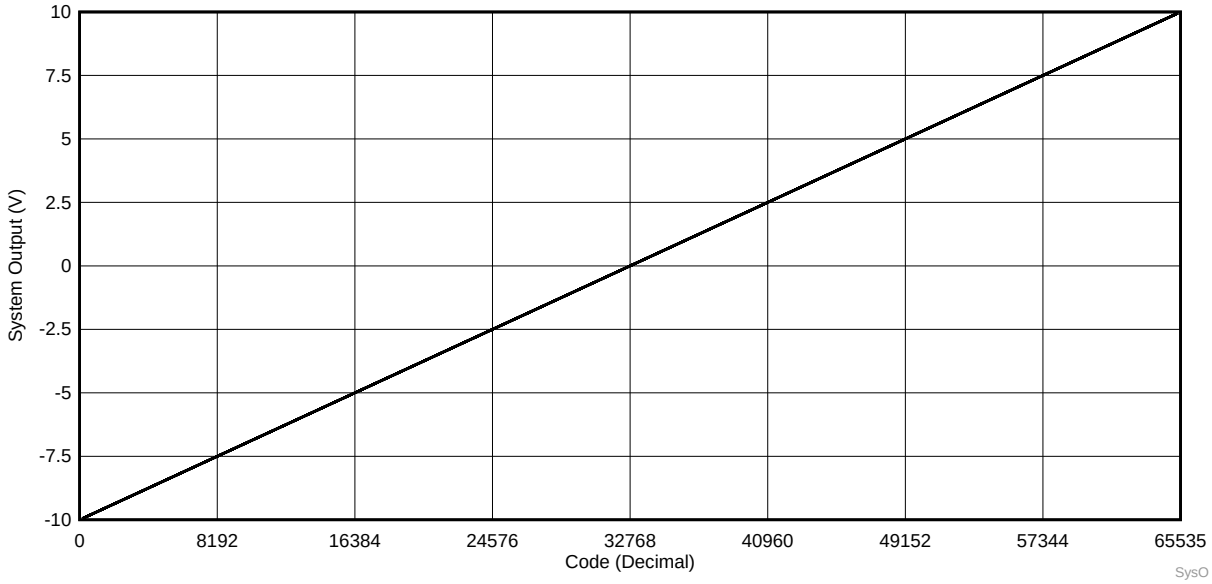

Figure 10. Measured System Transfer Function

Figure 11 shows the measured TUE for the entire code range.

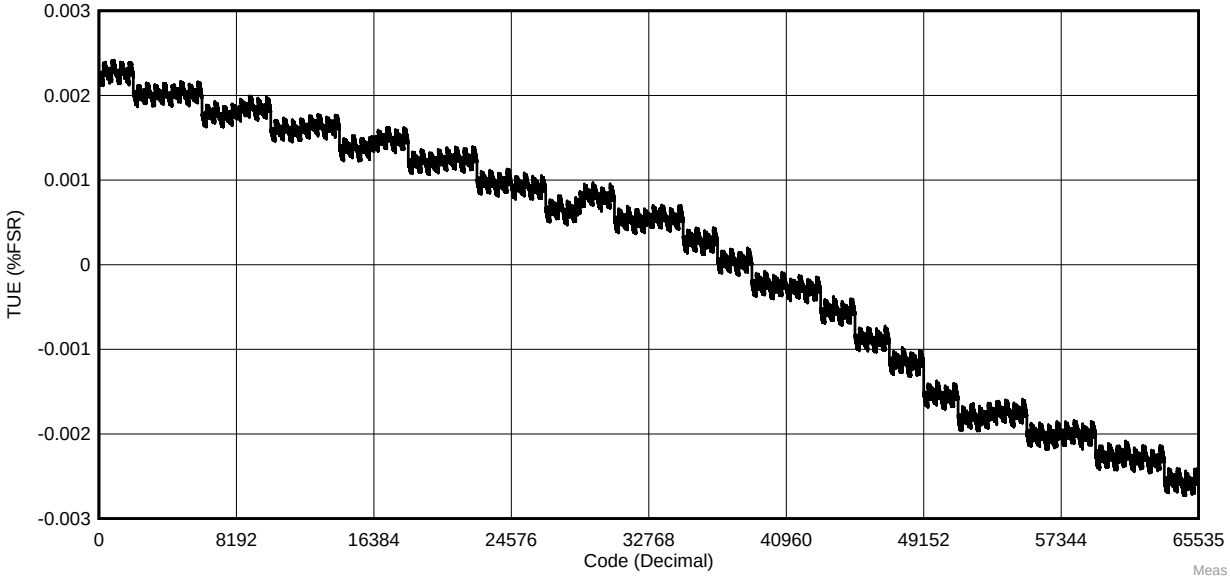

Figure 11. Measured Total Unadjusted Error

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INL and DNL data were also calculated from the output measurements and are shown in Figure 12.

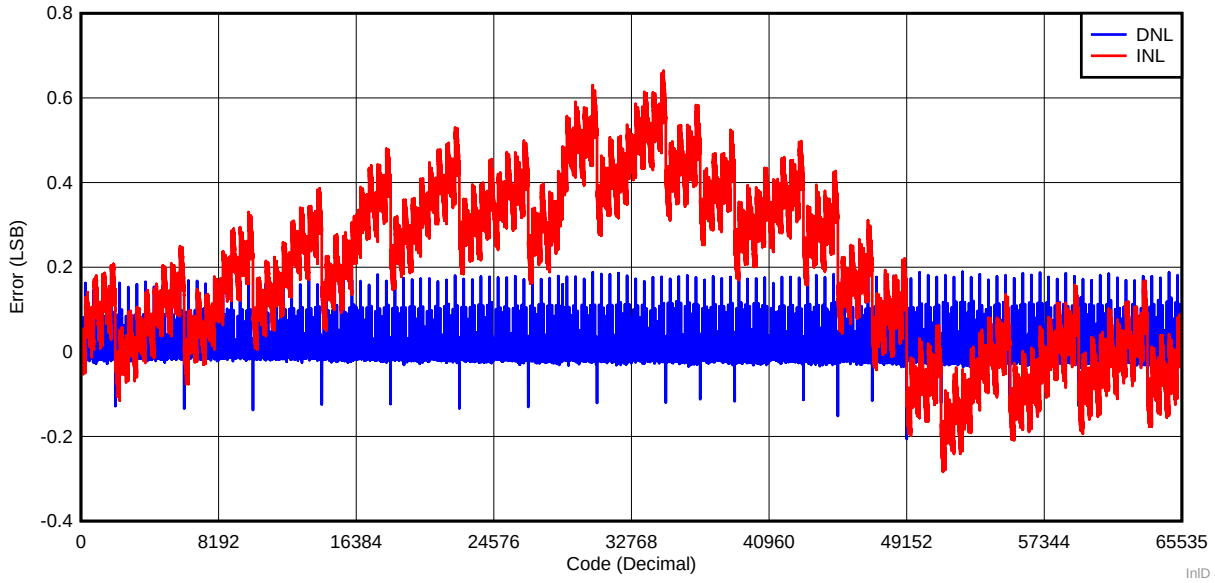

Figure 12. Measured INL and DNL Errors

Offset, gain, and INL parameters are calculated using the measured data from Equation 12 through Equation 14 and the TUE is calculated on a code-by-code basis, resulting in Table 3.

Table 3. Measured TUE

OFFSET ERROR	GAIN ERROR	INL ERROR	TUE
.00221%	.00628%	.00101%	.00272%

5.2 System Noise

The noise plot in Figure 13 was taken with the DAC set to full scale. The maximum peak-to-peak voltage visible in multiple iterations of noise capture was 41 μV_{PP}, 26.8% of the design goal of 0.5 LSB pk-pk (or 152 μV_{PP}).

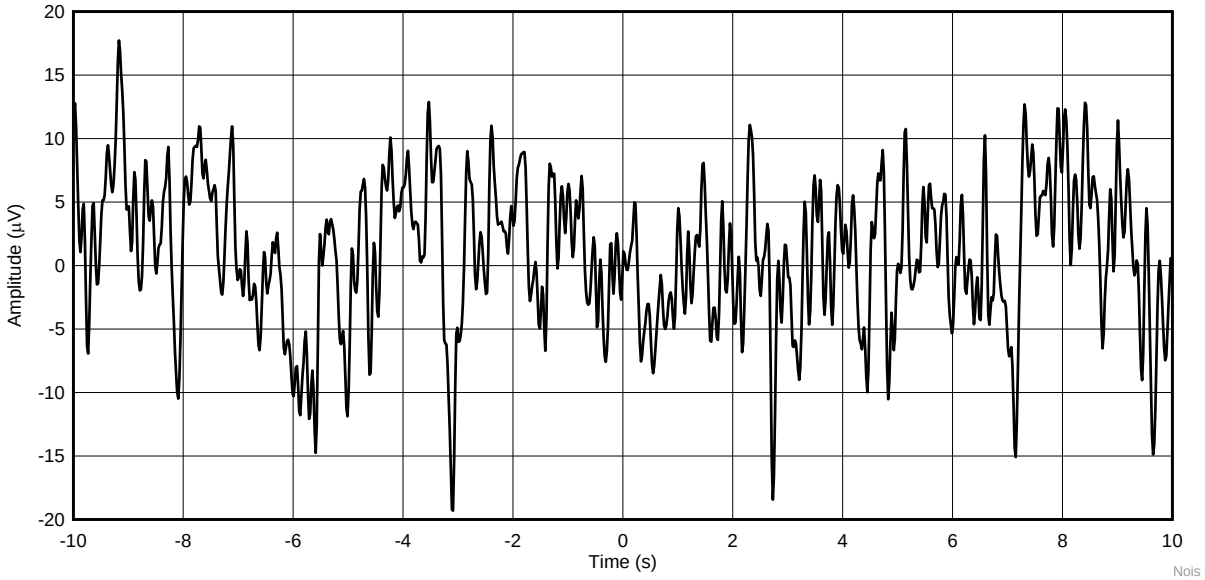

Figure 13. Measured Output Noise at Full-Scale Code

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5.3 Settling Time

The plot in Figure 14 is the measured settling time for both a rising transition and a falling transition. The high and low codes used in both measurements were xC000 and x4000, respectively, representing the settling time for ¼ to ¾ scale and ¾ to ¼ scale transitions. The two dotted-lines in Figure 14 represent an error of ±2 LSBs of the settled voltage. The typical measured settling time was 3.3 µs.

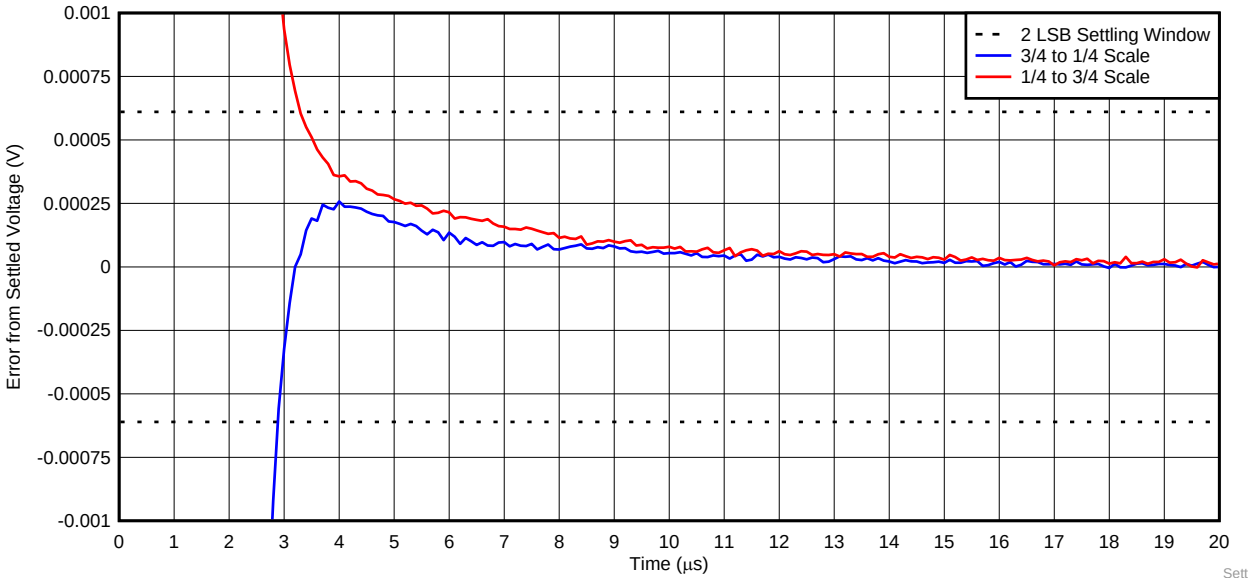

Figure 14. Measured Settling Time

6 Modifications

The following modifications can be made to the design based on performance goals.

The resistors on the final gain stage have a tolerance of 0.1% to meet the design goal of 0.1% FSR TUE. Relaxing the tolerance of the resistors to 1% offers a tradeoff between overall system accuracy and cost.

The DAC8832 device can be replaced by the DAC8831/0. The DAC8831/0 devices have the same analog architecture as the DAC8832 device with the exception of a power-on reset value, which Table 4 shows.

Table 4. Other Suggested Precision DACs

DEVICE	OUTPUT RANGE	GAIN ERROR	INL (TYP)	SETTLING TIME	OUTPUT NOISE	POWER-ON RESET
DAC8832	0 to 5 V	1 LSB	1 LSB	1 µs	18 nV/√Hz	Mid-scale
DAC8831/0	0 to 5 V	1 LSB	1 LSB	1 µs	18 nV/√Hz	Zero-scale

Table 5. Other Suggested Precision Amplifiers

DEVICE	GBW	SLEW RATE	INPUT OFFSET	INPUT OFFSET DRIFT	NOISE AT 1 kHz	I_Q PER CHANNEL
OPA4192	10 MHz	20 V/µs	5 µV	0.1 µV/°C	5.5 nV/√Hz	1 mA
OPA4197	10 MHz	20 V/µs	25 µV	0.5 µV/°C	5.5 nV/√Hz	1 mA
OPA4191	2.5 MHz	7.5 V/µs	5 µV	0.1 µV/°C	15 nV/√Hz	0.14 mA

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7 Design Files

7.1 Schematics

To download the schematics, see the design files at TIPD192.

7.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIPD192.

7.3 PCB Layout

The best practices for general printed-circuit board (PCB) layout were used in creating this design. These practices include separating the digital signal lines from analog lines, keeping bypass capacitors as close to the devices as possible, and using a ground plane. Note that the layout files used in creating the PCB are included in the design files that are available for download at TI.com. Figure 15 shows an image of the top side of the PCB.

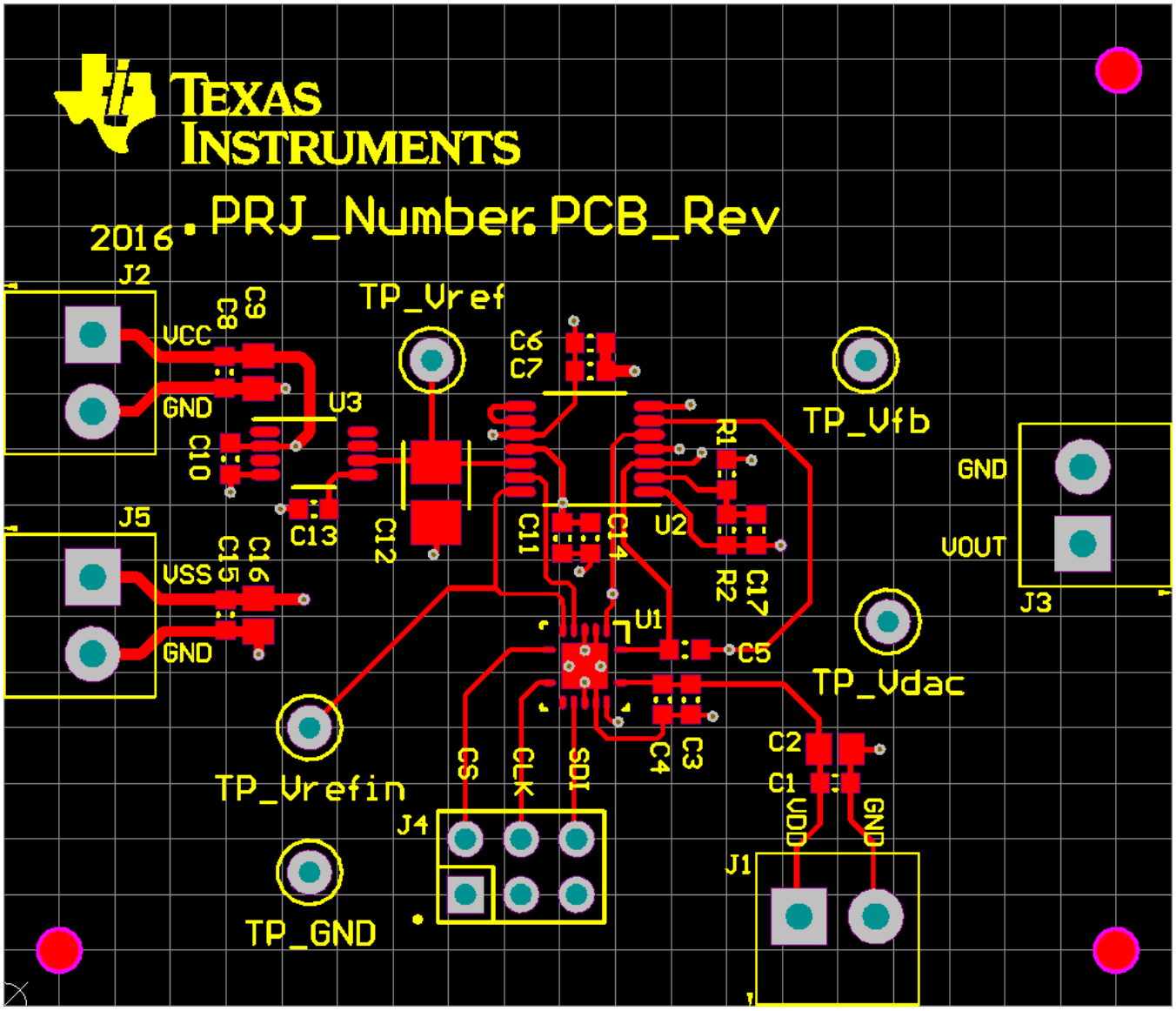

Figure 15. Top Side of PCB Layout

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7.4 Altium Project

To download the Altium project files, see the design files at TIPD192.

7.5 Gerber Files

To download the Gerber files, see the design files at TIPD192.

7.6 Assembly Drawings

To download the assembly drawings, see the design files at TIPD192.

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9 Acknowledgments and References

The authors wish to acknowledge Paul Frost and Adam Rozenberg, validation engineers for the TI Precision DAC product line. Their contributions to debugging the test setups for this design were crucial to making the project a success.

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