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A High-Power High-Fidelity Headphone Amplifier for Current Output Audio DACs Reference Design



TI Designs—Precision

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Design Resources

TIPD177	Design Folder
TINA-TI	SPICE Simulator
OPA1612	Product Folder
OPA1622	Product Folder



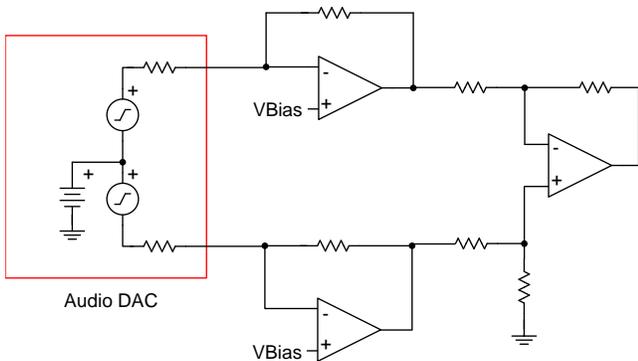
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Design Features

- THD+N of 0.000210% at 1 kHz While Driving a 16-Ω Load at 100 mW of Output Power
- THD+N of 0.000148% at 1 kHz While Driving a 32-Ω Load at 100 mW of Output Power
- Magnitude Variation of Only 0.0086 dB From 20 Hz to 20 kHz
- Phase Variation of Only 4.02° From 20 Hz to 20 kHz

Featured Applications

- Hi-Fi Smart Phones
- Headphone Amplifiers
- USB DAC
- Notebooks and Gaming Mother Boards
- Tablets



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1 Circuit Description

This circuit is designed to convert the differential output current of an audio digital-to-analog converter (DAC) into a single-ended voltage capable of driving low impedance headphones. Two op amps are used as transimpedance amplifiers which convert the DAC output current to a differential voltage. A difference amplifier then converts the differential voltage to single-ended. A high-power, high-fidelity two-channel audio op amp was used in the difference amplifier to directly drive stereo headphone loads at output powers > 100 mW.

2 Design Summary

The design requirements are:

- Supply voltage: ± 5 V
- Supply current: < 20 mA for a full stereo output (< 10 mA per channel).

Table 1 lists the design goals and performance.

Table 1. Comparison of Design Goals, Simulation, and Measured Performance

	GOAL	SIMULATED	MEASURED
Magnitude Variation (20 Hz to 20 kHz)	0.01 dB	0.0105 dB	0.0086 dB
Phase Variation (20 Hz to 20 kHz)	5.0°	4.02°	4.02°
THD+N (1 kHz, 10 mW, 16 Ω and 32 Ω)	< 0.001%	0.000240% (32 Ω) 0.000340% (16 Ω)	0.000350% (32 Ω) 0.000496% (16 Ω)
THD+N (1 kHz, 100 mW, 16 Ω and 32 Ω)	< 0.0005%	0.000076% (32 Ω) 0.000108% (16 Ω)	0.000148% (32 Ω) 0.000210% (16 Ω)
Maximum Output Power (Low Distortion Operation)	> 100 mW	N/A	156 mW (32 Ω) 124 mW (16 Ω)

Figure 1 shows the measured THD+N versus output power.

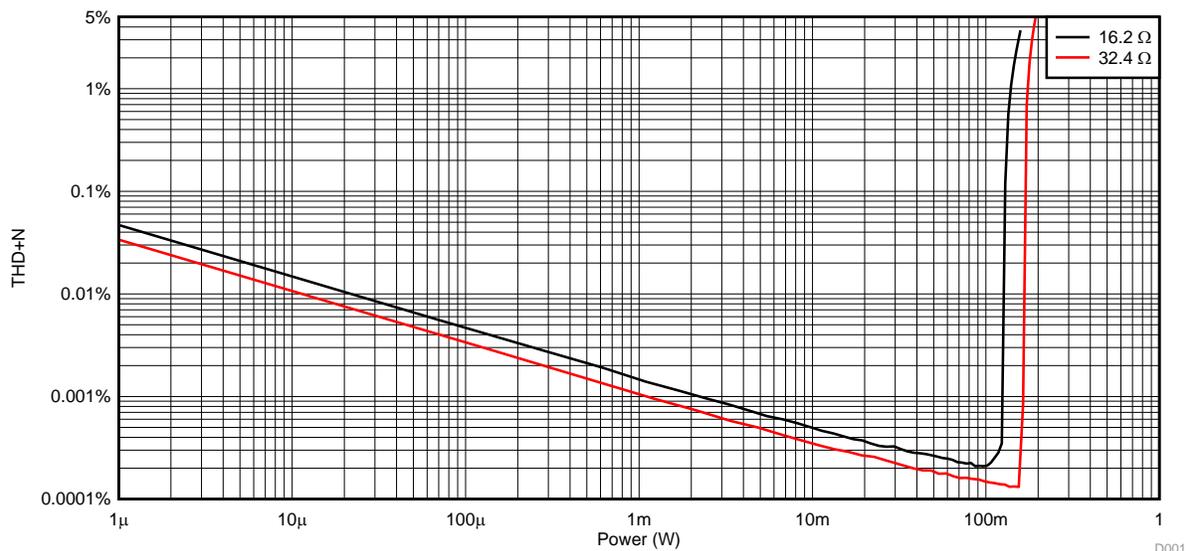


Figure 1. Measured THD+N versus Output Power

3 Theory of Operation

Many audio digital-to-analog converters (DACs) show improved linearity when used in the current output mode. These DACs provide a differential output current that varies with the input digital audio signal. A headphone output circuit must convert this differential current to a single-ended voltage signal capable of driving headphones at reasonable listening levels. A simplified schematic of the circuit used to accomplish this function is shown in [Figure 2](#).

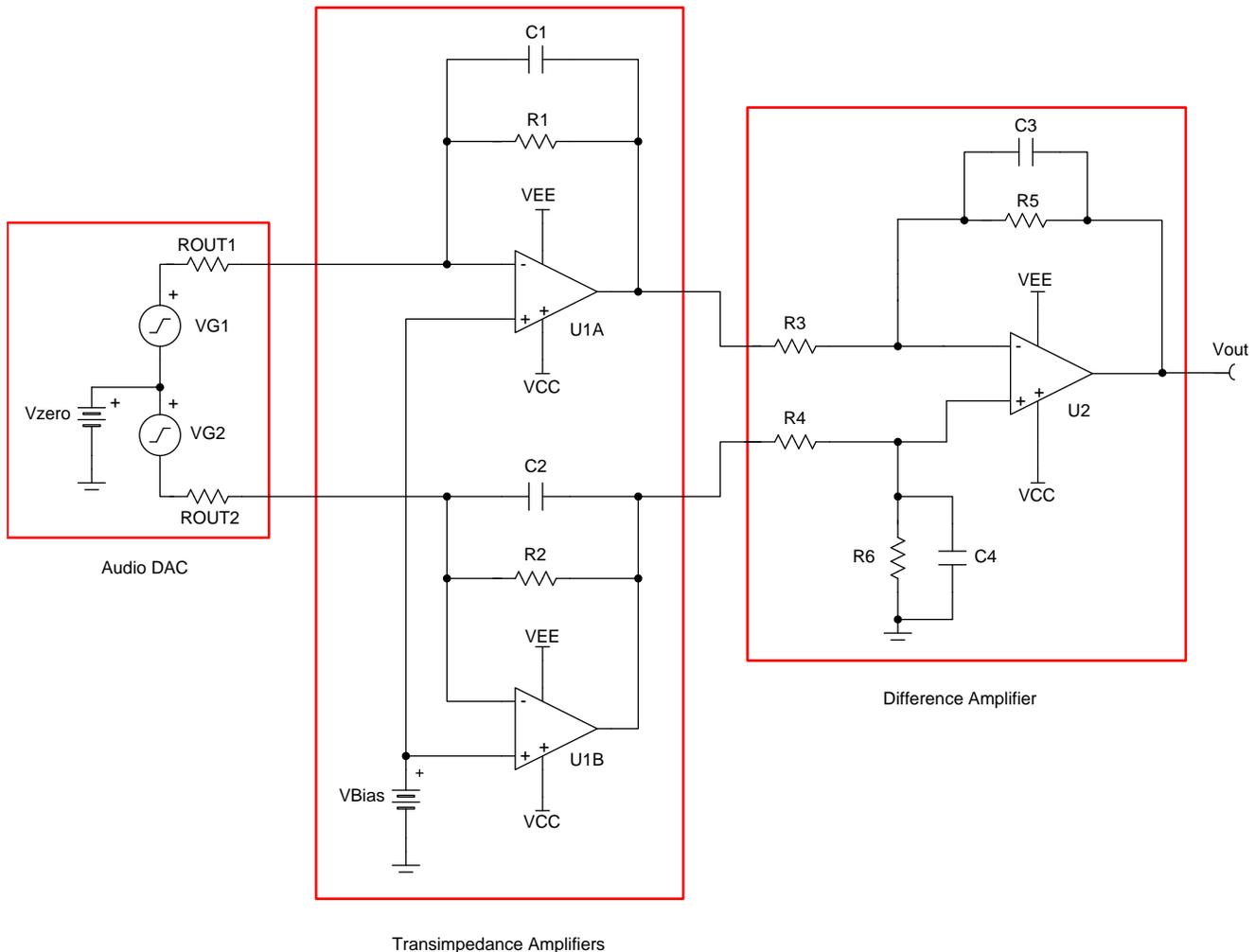


Figure 2. Simplified Schematic of DAC Output Circuit

Two transimpedance amplifiers are used to convert the differential output current from the audio DAC to a differential output voltage. Although the audio DAC has a current output, it is more accurately approximated by differential voltage sources with series resistances. There may also be an offset voltage when the DAC code is 0, represented by V_{zero} in [Figure 2](#).

Once the differential output current from the DAC has been converted to a differential voltage by the transimpedance amplifiers, the differential voltage is converted to a single-ended voltage by the difference amplifier. The amplifier must also be capable of driving the headphone impedance.

3.1 Transimpedance Amplifiers

From a noise standpoint, the total DAC output circuit consists of two amplifier stages in series in the signal path. [Figure 3](#) is a simplified block diagram of the signal path, with the two stages represented by amplifiers A_1 and A_2 . Each amplifier has two gains: the gain applied to the input signal, G_S , and a noise gain, G_N , which is the gain applied to the amplifier's intrinsic noise, en . The total signal gain of the circuit is the individual signal gains, G_{S1} and G_{S2} multiplied together.

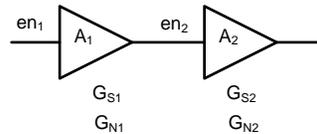


Figure 3. Symbolic Representation of Cascaded Amplifiers

Determining the total noise of the circuit is not quite as simple. The output noise of amplifier A_1 is multiplied by the noise gain of amplifier A_1 and the signal gain amplifier A_2 . Therefore, the total output noise is shown in [Equation 1](#).

$$en_r = \sqrt{(en_1 G_{N1} G_{S2})^2 + (en_2 G_{N2})^2} \quad (1)$$

Although the noise gain will always be equal to or greater than 1, the signal gain of an amplifier can be made less than 1. This offers an interesting opportunity to reduce the overall noise of the circuit. If the signal gain of the second stage can be made much less than 1, the amount of gain in the first stage can be maximized and the noise of the first stage amplifier dominates the total noise. For this reason, the gain of the transimpedance amplifiers should be as high as possible and the difference amplifier is configured for a signal gain less than one.

The appropriate gain of the transimpedance amplifiers is determined by the output current from the audio DAC and the output voltage swing capability of the op amp selected.

[Figure 4](#) shows a simplified model of a popular audio DAC.

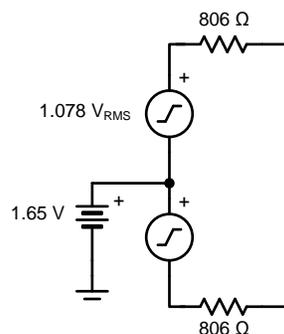


Figure 4. Simplified Model of a Popular Audio D/A Converter

In order to calculate the feedback resistors of the transimpedance amplifiers, the maximum ac output current from the DAC must be determined. For this analysis the contributions of the 1.65-V offset can be ignored. The peak single-ended output current is shown in [Equation 2](#).

$$i_{ec(MAX)} = \frac{1.078 V_{RMS} \times \sqrt{2}}{806} = 1.891467 \text{ mA}_P \quad (2)$$

The output voltage of a transimpedance amplifier is given in [Equation 3](#).

$$|V_{OUT}| = R_F |i_{IN}| \quad (3)$$

R_F is the value of the feedback resistor of the transimpedance amplifier. The maximum value of R_F is determined by the power supply voltages and the linear output swing of the op amp used. The linear output swing specification is normally given as a condition of the open loop gain measurement in the *OPA161x SoundPlus™ High-Performance, Bipolar-Input Audio Operational Amplifiers* datasheet (SBOS450), and listed in Table 2.

Table 2. Datasheet Conditions for Open Loop Gain Measurement Indicates the Linear Output Swing

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN					
A_{OL} Open-loop voltage gain	$(V-) + 0.2\text{ V} \leq V_O \leq (V+) - 0.2\text{ V}, R_L = 10\text{ k}\Omega$	114	130		dB
	$(V-) + 0.6\text{ V} \leq V_O \leq (V+) - 0.6\text{ V}, R_L = 2\text{ k}\Omega$	110	114		dB

For example, the op amp specified in Table 2 is able to maintain linear operation for output voltages within 600 mV of its power supplies for 2-k Ω loads. For ± 5 -V power supplies, the feedback resistor may be calculated as shown in Equation 4.

$$R_F = \frac{V_{OUT(MAX)}}{i_{IN}} = \frac{5\text{ V} - 0.6\text{ V}}{1.891467\text{ mA}} = 2326.24 \rightarrow 2.32\text{ k}\Omega \quad (4)$$

A capacitor is required across the feedback resistor in order to compensate for parasitic capacitance at the inverting input of the amplifier. The capacitor also limits the amount of high-frequency noise from the amplifier or DAC that may be aliased into the audio bandwidth by other circuits.

The capacitance at the inverting input is not known, therefore, the capacitor value must be as large as possible without contributing significant phase shift within the audio band. A design goal for this circuit is less than -5° . If it is assumed that the transimpedance amplifier and difference amplifier stages contribute equally to this phase shift, then the phase shift from the transimpedance amplifiers must be set to -2.5° at 20 kHz. Knowing the phase shift at 20 kHz, allows the pole frequency to appear as shown in Equation 5.

$$\theta = -\tan^{-1}\left(\frac{f}{f_P}\right) \rightarrow f_P = \frac{f}{\tan(-\theta)} = \frac{20000\text{ Hz}}{\tan(2.5^\circ)} = 458075\text{ Hz} \quad (5)$$

The maximum feedback capacitance may be calculated using the pole frequency and the feedback resistor value is as shown in Equation 6.

$$C_F \leq \frac{1}{2\pi R_F F_P} \leq \frac{1}{2\pi R_F F_P} \leq \frac{1}{2\pi(2320\ \Omega)(458075\text{ Hz})} \leq 149.75\text{ pF} \rightarrow 100\text{ pF} \quad (6)$$

3.2 Bias Voltage

When the DAC output code is zero, there is still an output current due to the offset of the DAC. In [Figure 2](#) a voltage, V_{Bias} , is applied to the non-inverting inputs of the transimpedance amplifiers to center their outputs at 0 V when the DAC code is zero. [Figure 5](#) shows the effective circuit when the DAC output code is zero.

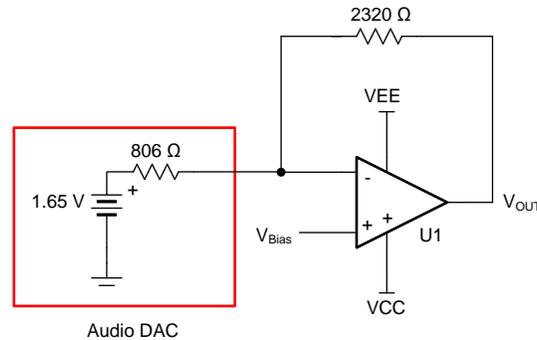


Figure 5. Simplified Schematic for Bias Voltage Calculation (Single Amplifier Shown)

The appropriate voltage for V_{Bias} may be calculated from [Equation 7](#).

$$V_{OUT} = 0 \text{ V} = V_{BIAS} \left(1 + \frac{2320 \text{ } \Omega}{806 \text{ } \Omega} \right) - 1.65 \left(\frac{2320 \text{ } \Omega}{806 \text{ } \Omega} \right)$$

$$\frac{1.65 \left(\frac{2320 \text{ } \Omega}{806 \text{ } \Omega} \right)}{\left(1 + \frac{232 \text{ } \Omega}{806 \text{ } \Omega} \right)} = V_{Bias}$$

$$1.225 = V_{Bias}$$

(7)

A resistor divider may be used to provide the bias voltage to the non-inverting inputs of the transimpedance amplifiers, as shown in [Figure 6](#).

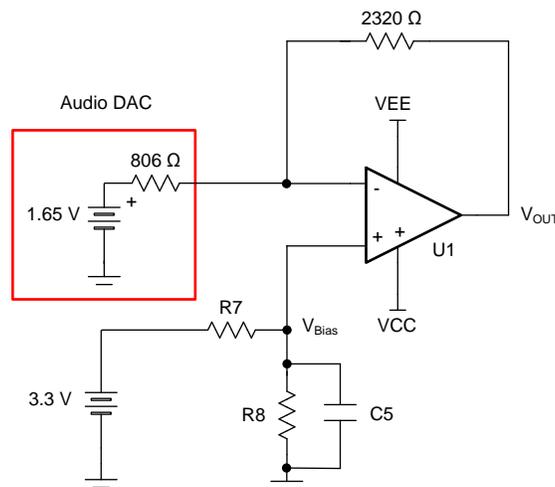


Figure 6. Bias Voltage Circuit for Transimpedance Amplifier

A 3.3-V supply is assumed for the resistor divider. R7 and R8 may be calculated to provide the desired bias voltage, as shown in Equation 8.

$$V_{\text{Bias}} = 1.225 \text{ V} = 3.3 \text{ V} \frac{R_8}{R_7 + R_8}$$

$$R_7 = 1.693878 R_8 \tag{8}$$

A capacitor must be placed in parallel with R8 to prevent noise from the 3.3-V supply from entering the signal path. The corner frequency produced by capacitor C5 is shown in Equation 9.

$$f_C = \frac{1}{2\pi(R_7 \parallel R_8)C_5} \tag{9}$$

The corner frequency should be less than 20Hz to attenuate supply noise within the audio bandwidth. C5 is then calculated, as shown in Equation 10.

$$C_5 \geq \frac{1}{2\pi(R_7 \parallel R_8)f_C} \geq \frac{1}{2\pi(9243.182 \text{ k}\Omega)(20 \text{ Hz})} \geq 0.861 \mu\text{F} \tag{10}$$

2.2 μF is selected as the value for C5. Larger capacitors may be used but they may require larger PCB footprints and will extend the start-up time of the circuit.

3.3 Difference Amplifier

The difference amplifier portion converts the differential output signal from the transimpedance amplifiers into a single-ended signal and attenuates it to proper amplitude for headphones, as shown in Figure 7.

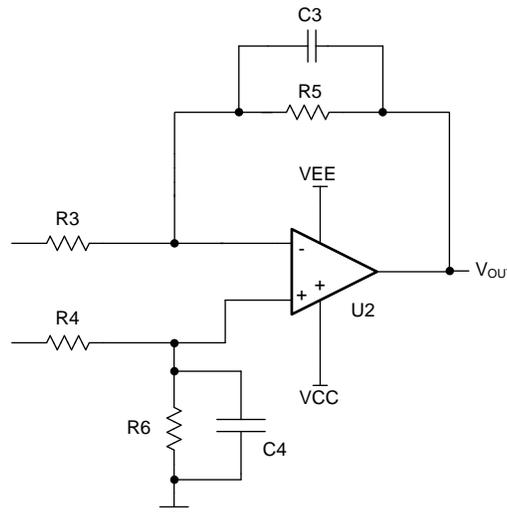


Figure 7. The Difference Amplifier Portion of the Output Circuit

The amount of attenuation implemented in the difference amplifier is determined by the desired maximum output voltage level. Headphones used for portable applications typically have low impedances (16 Ω or 32 Ω) and therefore do not require high voltages to produce loud sounds. For example, to deliver 10 mW to 32- Ω headphones only requires an output voltage of 0.566 V_{RMS} .

This output level suggests that the attenuation used in the difference amplifier must be large to achieve the best overall noise performance of the system. However, headphone outputs are often also used to interface portable electronics to larger audio systems through analog auxiliary inputs. Thus, the maximum output voltage is set to 2.2 V_{RMS} . The attenuation in the difference amplifier is then calculated by dividing the output amplitude by the differential input amplitude

The full-scale differential input to the difference amplifier is shown in [Equation 11](#).

$$V_{\text{DIFF}} = 2 \times 1.078 V_{\text{RMS}} \left(\frac{R_F}{R_{\text{OUT}}} \right) = 2 \times 1.078 V_{\text{RMS}} \left(\frac{2320 \Omega}{806 \Omega} \right) = 6.206 V_{\text{RMS}} \quad (11)$$

R_F is the feedback resistor value used in the transimpedance amplifiers and R_{OUT} is the output resistance of the audio DAC. The attenuation factor is shown in [Equation 12](#).

$$A = \frac{V_{\text{OUT}}}{V_{\text{DIFF}}} = \frac{2.2 V_{\text{RMS}}}{6.206 V_{\text{RMS}}} = 0.3545 \frac{\text{V}}{\text{V}} \quad (12)$$

The attenuation factor determines the ratio of resistor values used in the difference amplifier is shown in [Equation 13](#).

$$A = \frac{R_5}{R_3} = \frac{R_6}{R_4} \quad (13)$$

These resistor values must be low enough to avoid introducing significant thermal noise, but high enough to not excessively load the transimpedance amplifier outputs. In laboratory testing, a value near 1.6 k Ω for R3 and R4 yielded the best performance. R5 and R6 may thus be calculated, as shown in [Equation 14](#).

$$R_5, R_6 = 1.58 \text{ k}\Omega \times A = 560.11 \Omega \rightarrow 560 \Omega \quad (14)$$

Capacitors C3 and C4 are required to attenuate high frequency noise and may also assist in maintaining stability in the circuit under certain conditions. As mentioned in [Section 3.1](#), the values of these capacitors are limited by the phase shift they contribute at audible frequencies. The pole frequency produced by capacitors C3 and C4 is shown in [Equation 15](#).

$$F_P = \frac{1}{2\pi(R_5, R_6)(C_3, C_4)} \quad (15)$$

By setting the pole frequency equal to the value calculated in [Section 3.1](#), C3 and C4 may be calculated to meet the goals for phase shift at 20 kHz. See [Equation 16](#).

$$C_3, C_4 \leq \frac{1}{2\pi R_5 F_P} \leq \frac{1}{2\pi(560 \Omega)(458075 \text{ Hz})} \leq 620.4 \text{ pF} \rightarrow 560 \text{ pF} \quad (16)$$

560 pF was selected because as it is a readily-available denomination below the calculated value.

4 Component Selection

4.1 Resistors

The feedback resistors in the transimpedance amplifiers (R1, R2) as well as the resistors forming the difference amplifier (R3, R4, R5, R6) must be high tolerance 0.1% resistors for best performance. Choosing high tolerance resistors ensures that the output voltages of the transimpedance amplifiers are matched well. High tolerance resistors also maximize the common-mode rejection of the difference amplifier, which may reduce DC offset at the headphone output and cancel even harmonic distortion from the transimpedance amplifiers, or DAC.

4.2 Capacitors

All capacitors that may have a substantial signal voltage across them (C1, C2, C3, C4) must be C0G/NP0 type ceramics. Other types of ceramic capacitors (X7R, X5R, and more) produce large amounts of distortion and degrade the performance of the circuit. See reference one and two in [Section 11](#) for more information on this effect.

4.3 Amplifiers

Dual op amps in QFN packages are selected for this design for simplicity of implementation and to minimize the solution size. Dual op amps allow the two sets of transimpedance amplifiers and the stereo difference amplifier to be in the same packages. A quad op amp may further reduce the total solution cost and size, but there are fewer devices to choose from. The minimum requirements for all dual op amps in this circuit are a maximum supply voltage greater than 10 V, and power supply current of less than 5 mA per channel. The audio op amps that meet these requirements are listed in [Table 3](#).

Table 3. Dual Audio Op Amps That Meet Power Supply Voltage and Current Design Requirements

OP AMP	MAXIMUM SUPPLY VOLTAGE	SUPPLY CURRENT PER CHANNEL
OPA1612	36 V	3.6 mA
OPA1602	36 V	2.6 mA
OPA1622	36 V	2.6 mA
OPA1652	36 V	2.0 mA
OPA1662	36 V	1.4 mA
LME49725	36 V	3.0 mA
LME49723	36 V	3.4 mA

4.3.1 Transimpedance Amplifiers

The amount of gain in the transimpedance amplifiers is limited by the op amp's linear swing to its power supply rails. A value of 0.6 V was used in [Section 3.1](#) to calculate the feedback resistor value. As listed in [Table 4](#), four audio op amps meet the basic requirements for the circuit and are able to linearly swing to 0.6 V from the power supplies.

Table 4. Linear Output Swing of Dual Audio Op Amps

OP AMP	LINEAR SWING TO RAIL
OPA1612	0.6 V
OPA1602	0.6 V
OPA1622	0.6 V
OPA1662	0.6 V
OPA1652	0.8 V
LME49725	> 1 V
LME49723	> 1V

The second requirement for the transimpedance amplifiers is low noise in order to preserve extremely high audio fidelity. Unlike other transimpedance amplifier applications, the source impedance is rather low, being the parallel combination of the 830 ohm DAC output resistors and the 2.37-k Ω feedback resistors ($R_S = 830 \parallel 2.37k = 614.7 \Omega$). Furthermore, the feedback resistor is larger than the source resistance, resulting in a noise gain greater than 1, as shown in [Equation 17](#).

$$G_{\text{Noise}} = 1 + \frac{R_F}{R_1} = 1 + \frac{2.37 \text{ k}\Omega}{830 \Omega} = 3.855 \quad (17)$$

The source impedance and noise gain both indicate that the input voltage noise, rather than the input current noise, is the dominant factor in the total output noise. Comparing the input voltage noise of the four op amps from [Table 4](#), which met the linear output swing requirement shows that the OPA1612 has the lowest voltage noise and is selected for the transimpedance amplifier. [Table 5](#) lists the input voltage noise of audio amps which met the output swing requirement.

Table 5. Input Voltage Noise of Audio Amps Which Met The Output Swing Requirement

OP AMP	INPUT VOLTAGE NOISE
OPA1612	1.1 nV / $\sqrt{\text{Hz}}$
OPA1602	2.5 nV / $\sqrt{\text{Hz}}$
OPA1622	2.8 nV / $\sqrt{\text{Hz}}$
OPA1662	3.3 nV / $\sqrt{\text{Hz}}$

4.3.2 Output Difference Amplifier

The most difficult requirement for the output difference op amp is to maintain low distortion at output current levels above those usually found in small signal design. Table 1 contains the design requirement of THD+N < 0.001% (–100 dB) for an output power of 10 mW and < 0.0005% (–106 dB) for an output power of 100 mW into 16-Ω and 32-Ω loads. The design requirement is more difficult to meet into a 16-Ω load because the output current is larger. To deliver 100 mW to a 16-Ω load, the headphone circuit must output what is shown in Equation 18.

$$I_{OUT} = \sqrt{\frac{P_{OUT}}{R_L}} = \sqrt{\frac{100 \text{ mW}}{16}} = 79 \text{ mA}_{RMS} \tag{18}$$

From the amplifiers listed in Table 5, the OPA1622 is the only device that delivers the required output current to support 100 mW into a 16-Ω load. While many datasheets for audio op amps only characterize the THD+N performance for higher load impedances, the OPA161x SoundPlus™ High-Performance, Bipolar-Input Audio Operational Amplifiers datasheet (SBOS450) also includes performance information with 16-Ω and 32-Ω loads. The THD+N versus output voltage graph from the OPA161x SoundPlus™ High-Performance, Bipolar-Input Audio Operational Amplifiers datasheet (SBOS450) application circuit is shown in Figure 8. Output levels of 1.265 V_{RMS} and 1.789 V_{RMS} are required to produce 100 mW into 16-Ω and 32-Ω loads, respectively. Figure 8 shows a THD+N near –119 dB (.00002%) for 16 loads and near –120 dB (0.00001%) for 32-Ω loads at the required output levels.

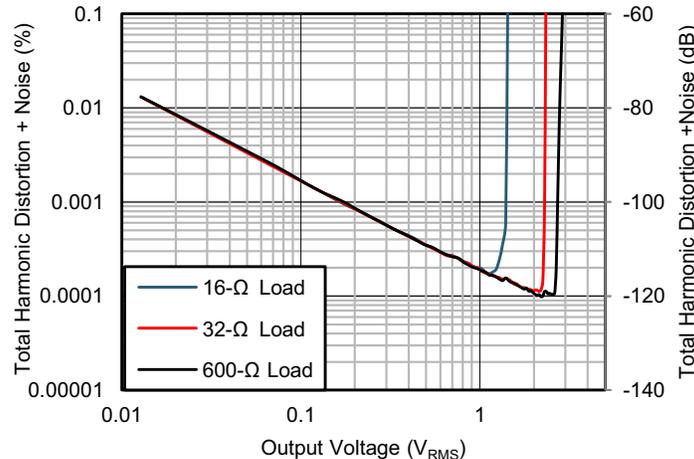


Figure 8. THD+N versus Output Voltage From The OPA1622 Datasheet Application Circuit

The results in Figure 8 do not include the additional noise from the rest of the circuit, and must be used only to verify that the OPA1622 is a good candidate to provide low distortion audio performance at the required output power levels.

5 Simulation

The simulation schematic shown in [Figure 9](#) is used for the noise and transfer function simulations. The audio DAC is represented on the left of the schematic in a blue rectangle. For many analyses in TINA-TI™ only a single input signal source can be accommodated, therefore a voltage controlled voltage source (VCVS) with a gain of 1 allows the DAC output voltage to be differential without requiring two voltage sources.

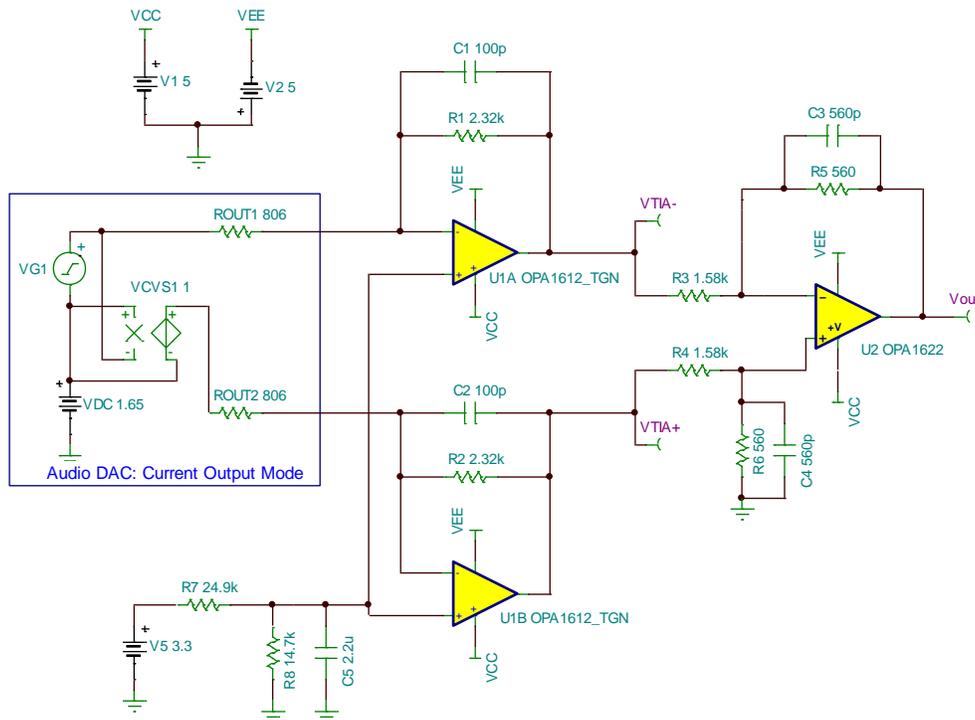


Figure 9. TINA-TI Simulation Schematic for Transfer Function, Transient, and Noise Analysis

5.1 Transfer Function

An AC transfer characteristic analysis was used to determine the magnitude and phase response of the circuit. At 20 kHz, the magnitude response was down -0.0105dB and the phase had deviated -4.02 degrees. These results satisfy the design goals listed in [Section 2](#).

Figure 10 shows the circuit magnitude and phase response plotted using an AC transfer characteristic simulation.

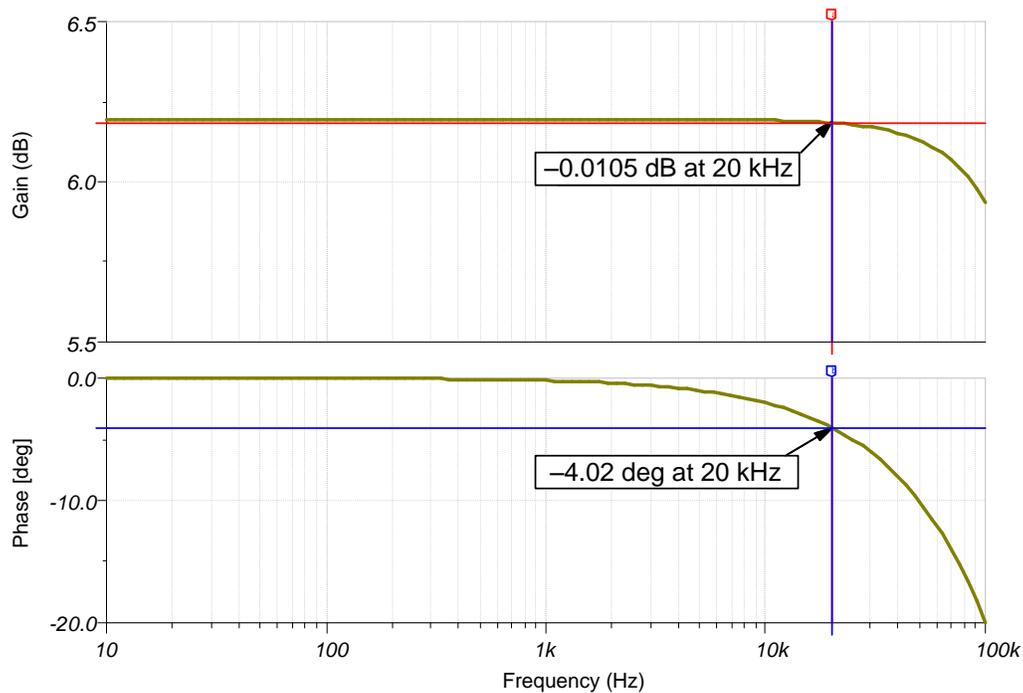


Figure 10. Circuit Magnitude and Phase Response Plotted Using an AC Transfer Characteristic Simulation

5.2 Transient Response

A transient simulation was run with a 1 kHz full-scale sine-wave input of $\pm 1.078 V_{RMS}$ ($1.525 V_{PP}$). As desired the transimpedance stages swing roughly 4.4 Vp and stay 0.6 V away from the supplies for best linearity performance. The output stage produces the desired $2.2 V_{RMS}$ ($3.111 V_{PP}$) output level.

Figure 11 shows the circuit magnitude and phase response plotted using an AC transfer characteristic simulation.

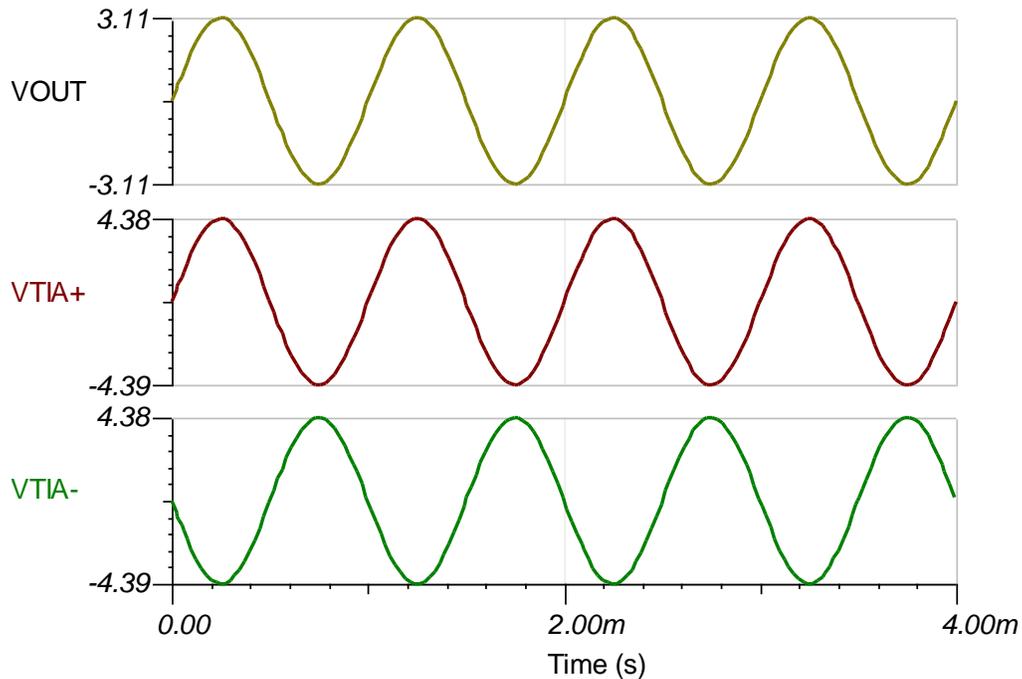


Figure 11. Circuit Magnitude and Phase Response Plotted Using an AC Transfer Characteristic Simulation

5.3 Noise

The total output noise was integrated over an 80-kHz bandwidth using the noise analysis function of TINA-TI. The predicted RMS noise voltage was $1.36 \mu\text{V}_{\text{RMS}}$ for a 22-kHz bandwidth and $2.58 \mu\text{V}_{\text{RMS}}$ for an 80-kHz bandwidth, as shown in Figure 12.

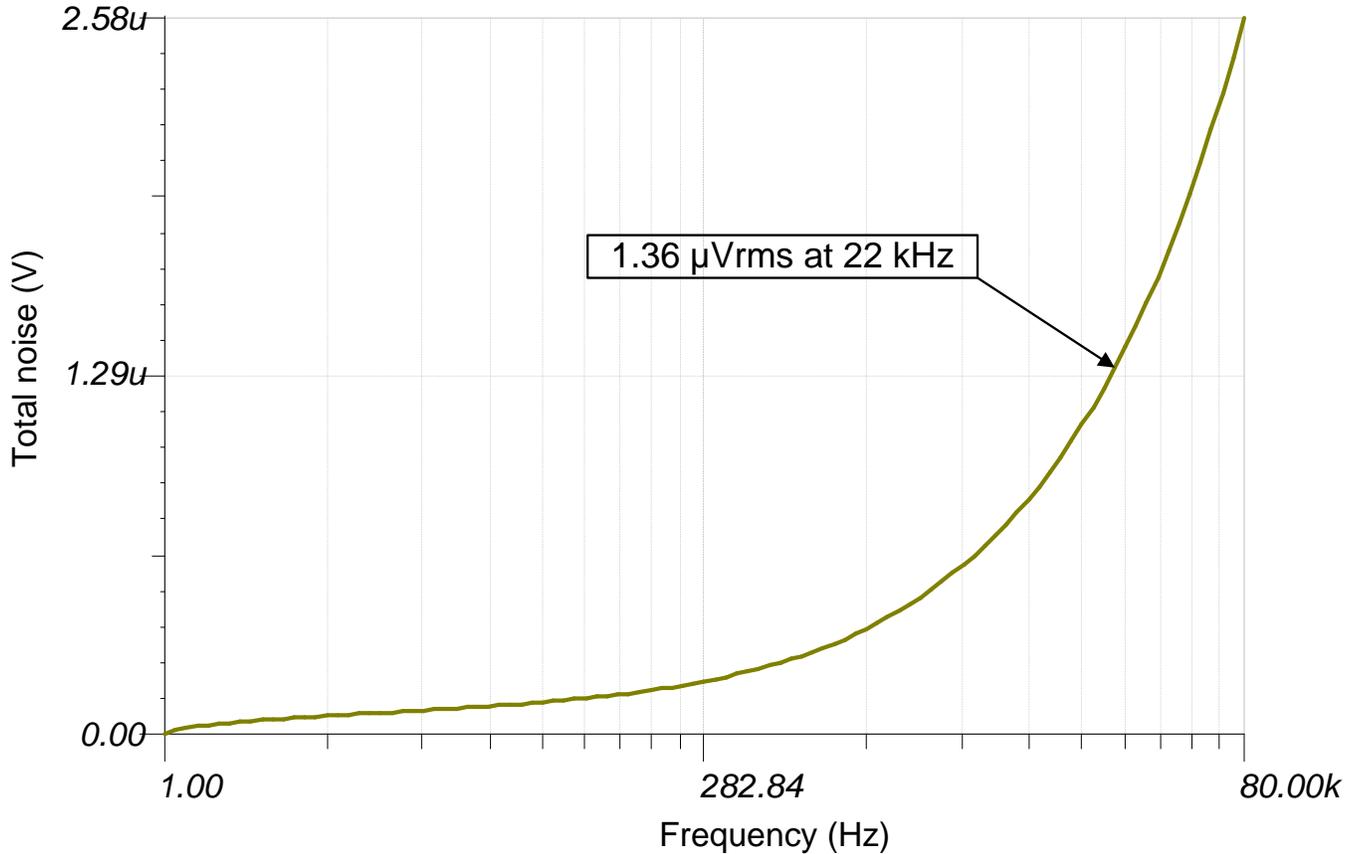


Figure 12. TINA-TI Total Noise Simulation Showing $1.36 \mu\text{V}_{\text{RMS}}$ Noise in a 22-kHz Bandwidth

Using the RMS noise voltage, the noise contribution to the THD+N figure may be calculated for different output levels using Equation 19.

$$\text{THD}_N (\%) = 100 \times \sqrt{\frac{V_n^2}{V_f^2}} \tag{19}$$

V_n is the RMS noise voltage and V_f is the RMS voltage of the fundamental. The calculated THD+N results in the noise-dominated region are listed in [Table 6](#) and [Table 7](#) using the 22-kHz noise level of $1.36 \mu V_{RMS}$.

Table 6. Predicted Noise-Dominated THD+N Values for 10 mW of Output Power into 16- Ω and 32- Ω Loads

LOAD IMPEDANCE	OUTPUT VOLTAGE AT 10 mW	PREDICTED THD+N (NOISE DOMINATED)
16 Ω	0.4 V_{RMS}	0.00034%
32 Ω	0.566 V_{RMS}	0.00024%

Table 7. Predicted Noise-Dominated THD+N Values for 100 mW of Output Power into 16- Ω and 32- Ω Loads

LOAD IMPEDANCE	OUTPUT VOLTAGE AT 100 mW	PREDICTED THD+N (NOISE DOMINATED)
16 Ω	1.265 V_{RMS}	0.000108%
32 Ω	1.789 V_{RMS}	0.000076%

5.4 Circuit Stability

The TINA-TI simulation schematic used to test the stability of the difference amplifier is shown in Figure 13. The feedback loop of the difference amplifier (U2) is broken by inductor LT and a signal is injected by voltage source VG1 through capacitor CT. The loop-gain (Aolβ) and loop-gain phase margin are measured at the AolB voltage probe. A network of passive components (labeled headphone impedance approximation) is used to simulate the impedance of many headphones at high frequencies. The inductance of the driver voice coils in the headphones combined with the inductance and capacitance of the cord forms a resonance typically at 1.0 to 1.5 MHz, which may cause stability problems. The effect of the headphones impedance must be accounted for in the design of the circuit.

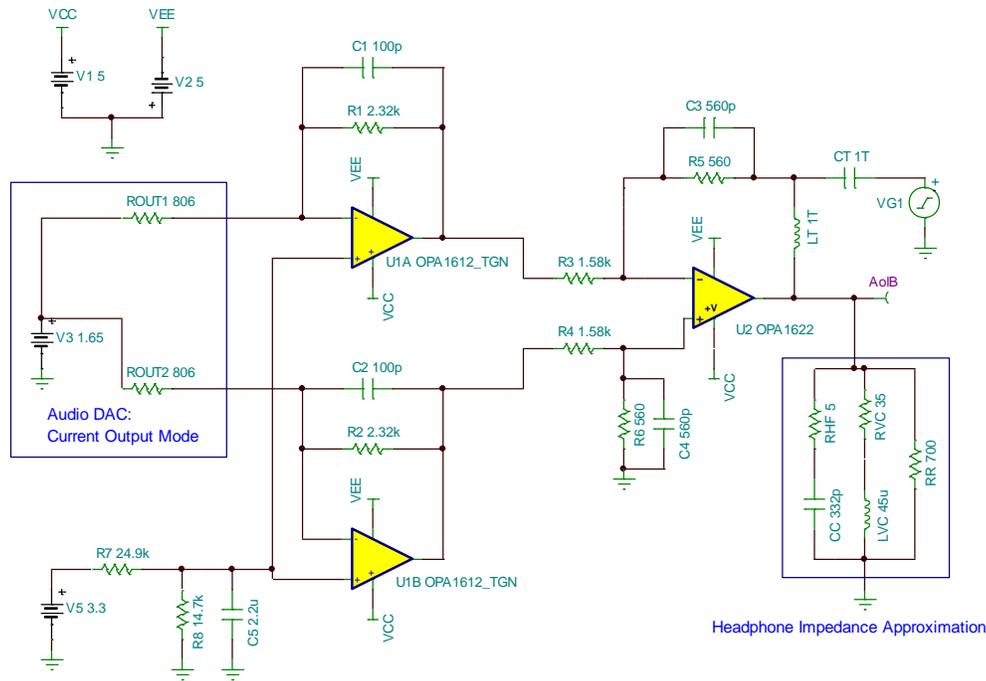


Figure 13. TINA-TI Simulation Schematic to Determine the Phase Margin of the Headphone Amplifier

The phase margin of the circuit is determined by performing an AC transfer characteristic simulation and measuring the phase at the loop closure point (0 dB). The phase margin of amplifier U2A is 52.06°, with the simulated headphone load, indicating stable operation, as shown in Figure 14.

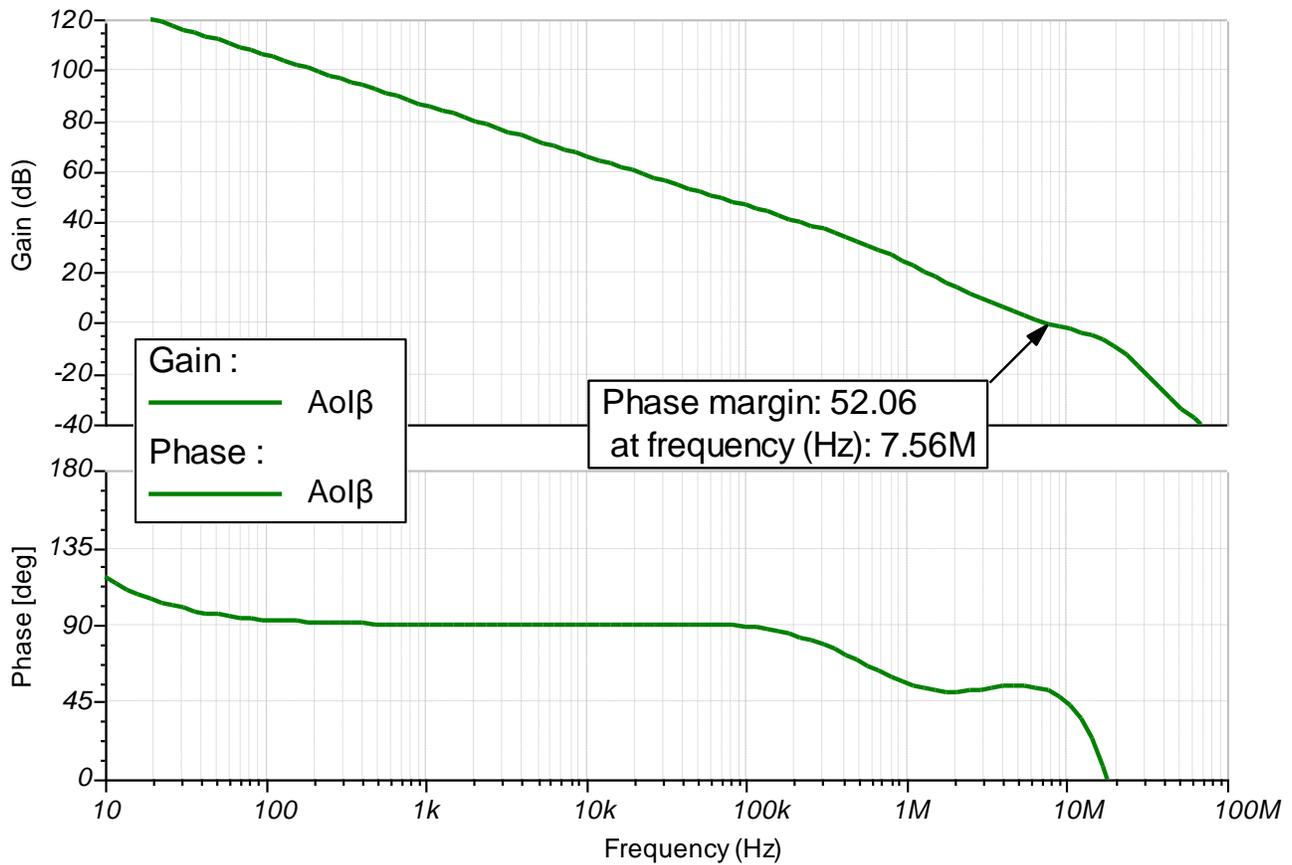


Figure 14. Magnitude and Phase Response of the Difference Amplifier Loop

6 Design Files

6.1 PCB Design

The PCB schematic can be found in [Appendix A](#).

6.1.1 PCB Layout

A four-layer PCB was used for this design to achieve the best thermal performance while handling the large currents associated with the > 100 mW stereo headphone output power requirement. Solid GND planes were used on mid-layer 2 and the bottom layer to provide a low impedance path for the GND return currents to exit the PCB. A solid plane connected to V– was included on mid-layer 1 to act as a heat-sink for the OPA1612 and OPA1622 op amps which feature PowerPADs connected to V–.

The trace lengths in the difference amplifier must be carefully considered in the circuit layout. Recall from [Section 4.1](#) that 0.1% resistors were selected in order to maximize the common-mode rejection of the difference amplifier and improve the overall performance of the circuit. The traces used to route signals between these resistors also add resistance, which can degrade the matching between resistors. To maximize circuit performance, the traces from the outputs of the transimpedance amplifier to the difference amplifier should be kept as short as possible and, ideally, of equal length.

[Figure 15](#) shows the top layer (left) and bottom layer (right) of the PCB.

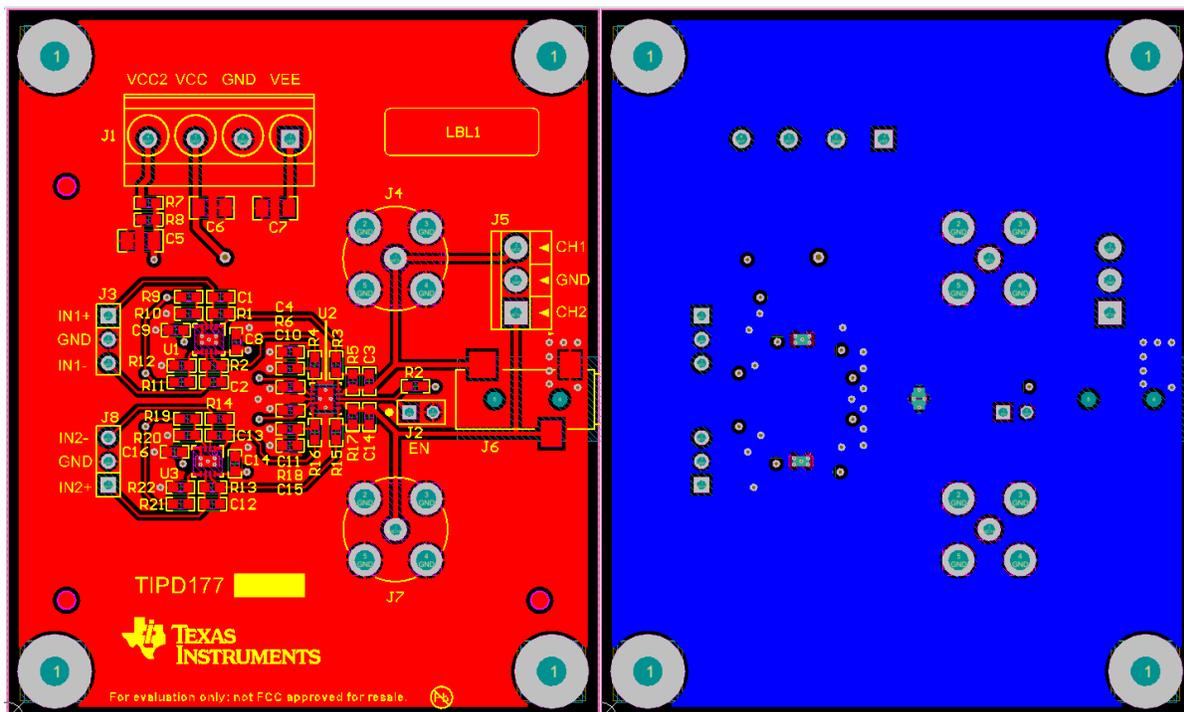


Figure 15. Top Layer (Left) and Bottom Layer (Right) of the PCB

Figure 16 shows the mid layer 1 (left) and mid layer 2 (right) of the PCB.

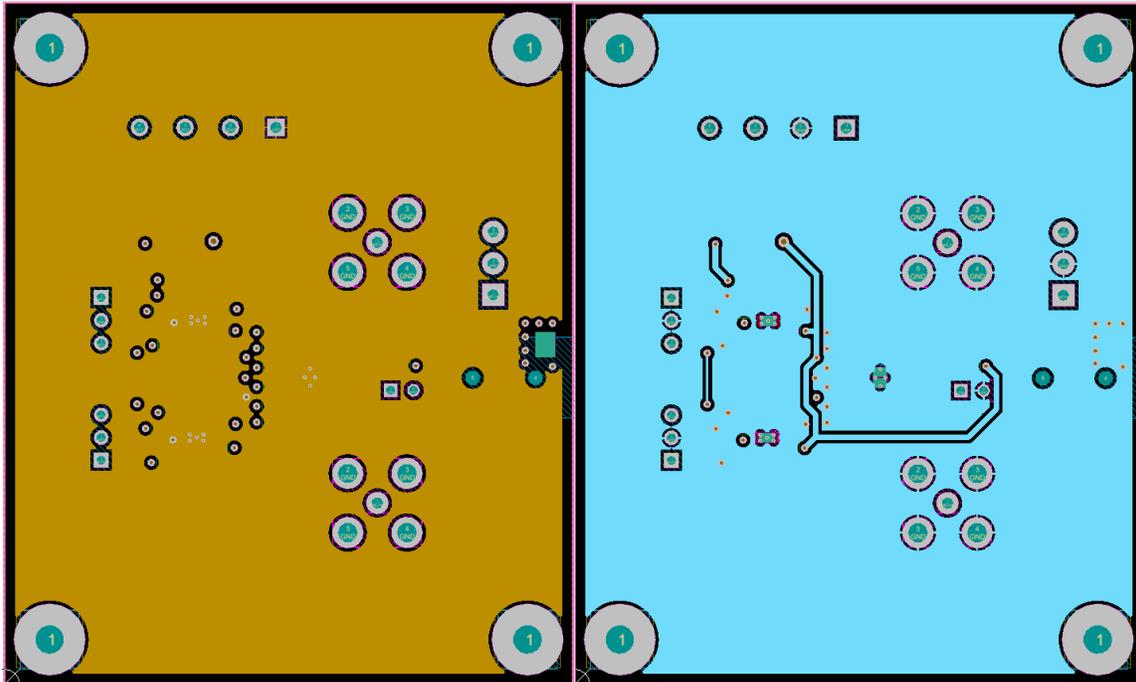


Figure 16. Mid Layer 1 (Left) and Mid Layer 2 (Right) of the PCB

7 Verification and Measured Performance

The output of a low-distortion audio analyzer is passed to an OPA1632 fully-differential amplifier in order to add a 1.65-V common-mode voltage to the signal. Using the OPA1632 simulates the audio DAC output used for the design calculations. 825-Ω resistors in series with the outputs of the OPA1632 also mimic the DAC output impedance. By operating the OPA1632 in a signal gain of less than 1, some of the noise from the audio analyzer is attenuated, improving the measurement noise floor.

Figure 17 shows a circuit to adjust the common-mode voltage and output impedance of an audio analyzer.

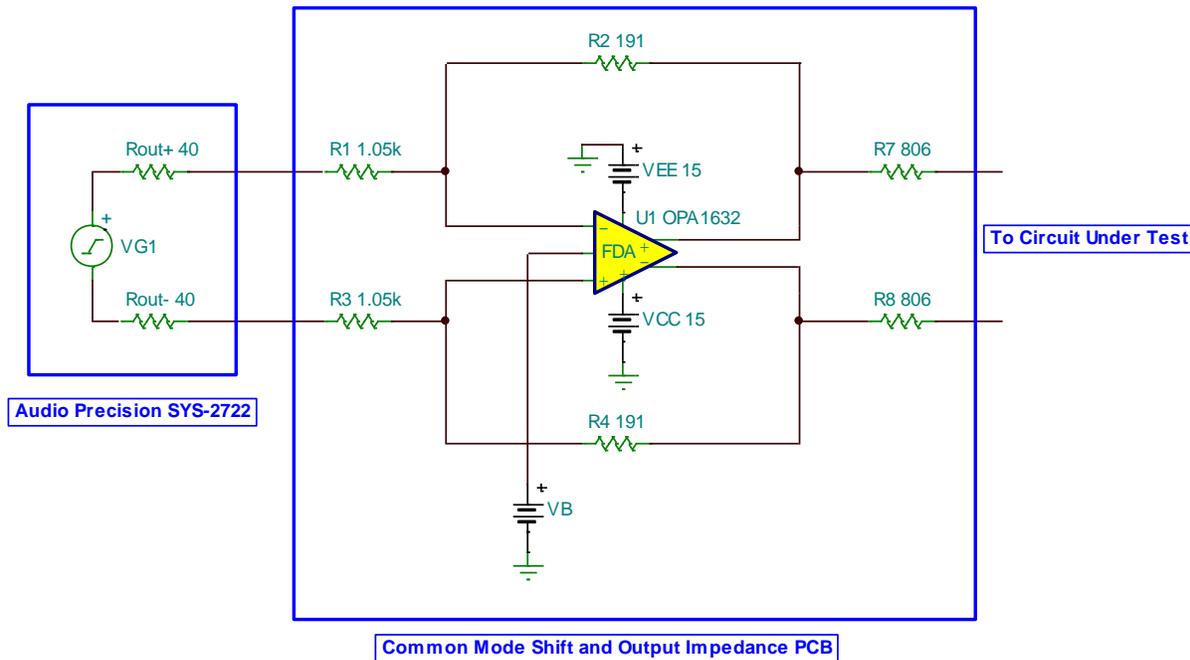


Figure 17. A Circuit to Adjust the Common-Mode Voltage and Output Impedance of an Audio Analyzer

7.1 Transfer Function

Magnitude Response and Output Impedance

The magnitude response of the headphone amplifier was measured over a bandwidth of 10 Hz to 100 kHz. At 20 kHz, the magnitude response was down 0.0088 dB, as shown in Figure 18.

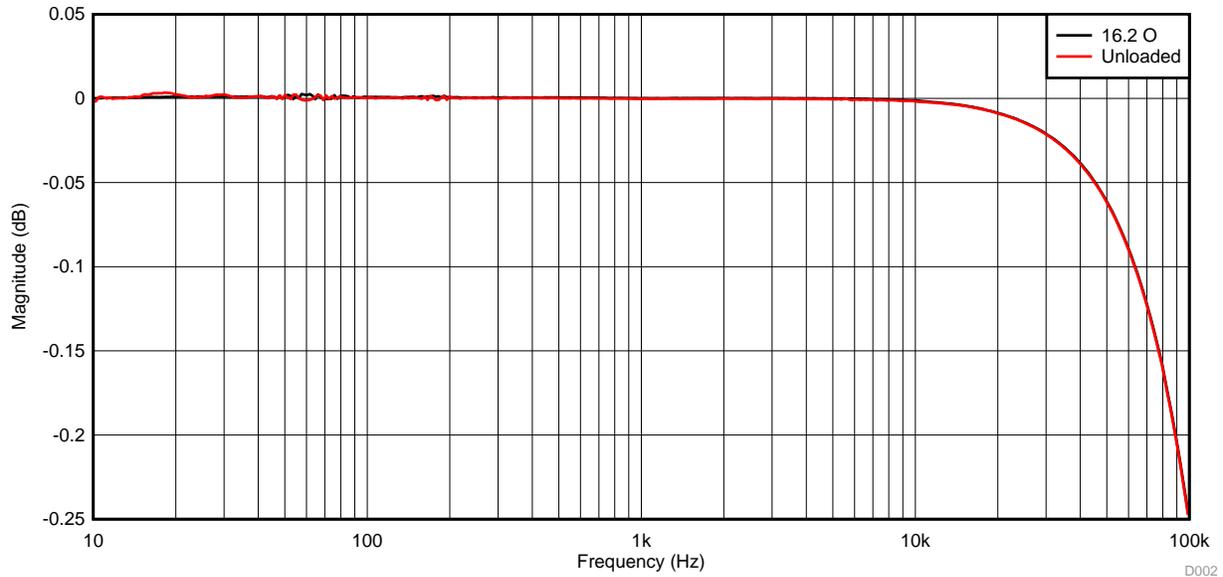


Figure 18. Magnitude Response of the Headphone Amplifier

Phase Response

The phase response was also measured over a bandwidth of 10 Hz to 100 kHz. At 20 kHz, the phase has deviated 4.02°, as shown in Figure 19.

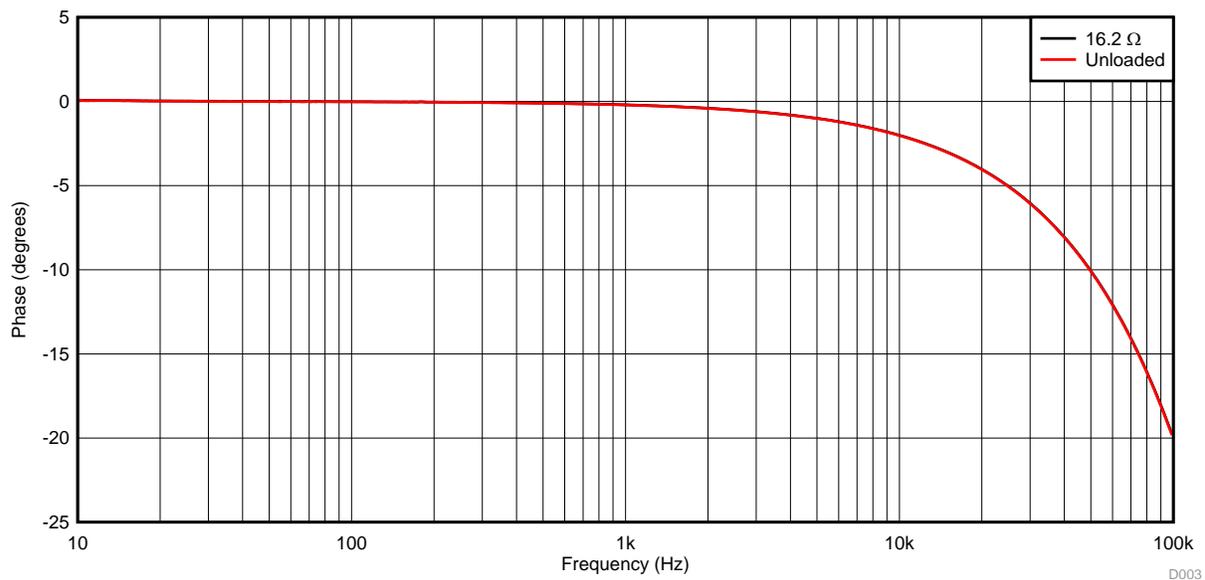


Figure 19. Phase Response of the Amplifier Circuit

7.2 THD+N versus Output Power

The THD+N versus output power level is shown in [Figure 20](#) for a 1-kHz signal. The receiver bandwidth was set to 22 kHz. For 100 mW of output power, the THD+N is 0.000148% into a 32.4- Ω load, and 0.000210% into a 16.2- Ω load. For 10 mW of output power, the THD+N is 0.000350% into a 32.4- Ω load, and 0.000496% into a 16.2- Ω load.

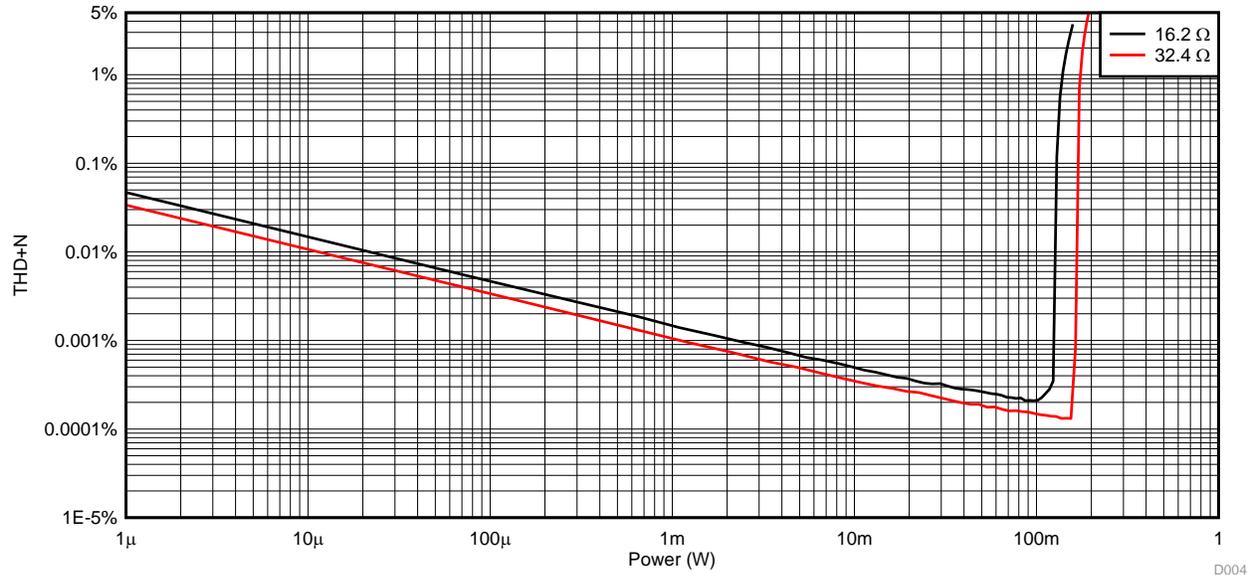


Figure 20. Measured THD+N versus Output Power (1-kHz Signal)

The maximum output power for both the 32- Ω and 16- Ω loads was limited by the maximum output current of the circuit. The maximum power into a 32- Ω load is limited to 156 mW with a THD+N of 0.000131% (–117.62 dB). The maximum power into a 16- Ω load is limited to 124 mW with a THD+N of 0.00035% (–109.14 dB).

The constant downward slope of the THD+N versus output power graph indicates that the noise of the circuit is the dominant factor in the THD+N calculation. Therefore, the degraded THD+N measurement for a 16.2- Ω load is not due to additional loading causing distortion. Rather, the smaller output signal voltage required to deliver 10 mW into a 16.2- Ω load degrades the signal-to-noise ratio. Also, at these extremely low THD+N levels, the noise of the audio analyzer used for the measurement effects the result.

7.3 THD + N versus Frequency

The THD+N was measured from 20 Hz to 20 kHz at several different output power levels into 32.4- Ω and 16.2- Ω loads with a measurement bandwidth of 80 kHz. At high frequencies, the measurement slightly degrades due to the declining open loop gain of the op amp. Figure 21 displays the results with 150 mW of output power into a 32.4- Ω load. At 20 kHz, the THD+N is 0.00055% (-105.19 dB).

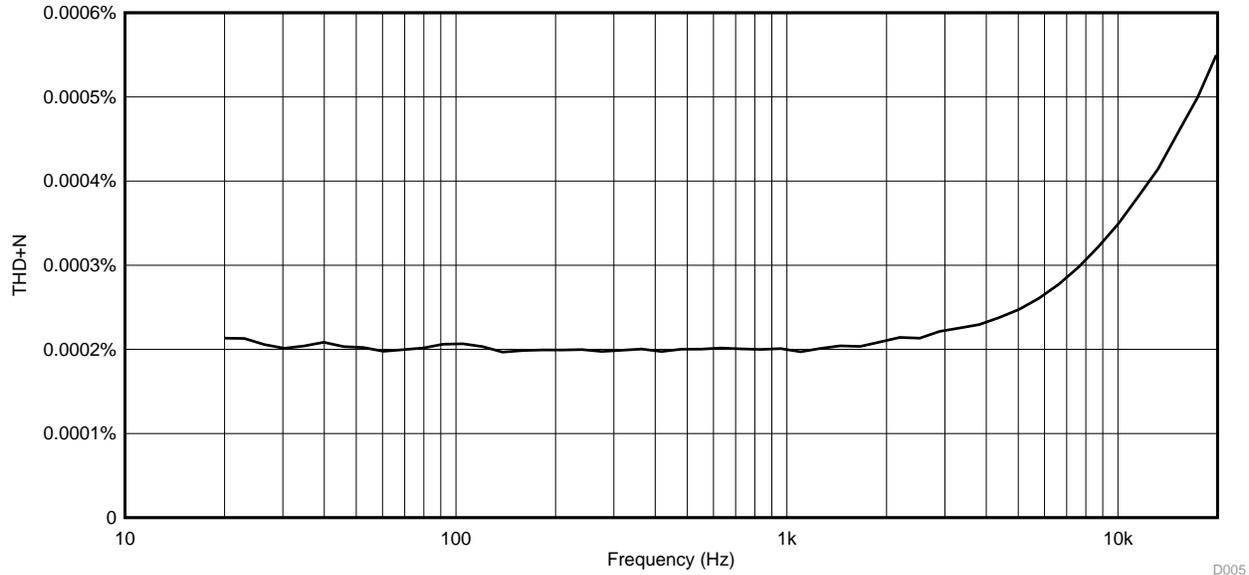


Figure 21. THD+N versus Frequency Graph for 150-mW of Output Power

Figure 22 shows the results for 100 mW of output power for 32.4- Ω and 16.2- Ω loads. At 20 kHz, the THD+N is 0.00037% (-108.64 dB) for a 32.4- Ω load and 0.00135% (-97.39 dB) for 16.2- Ω loads.

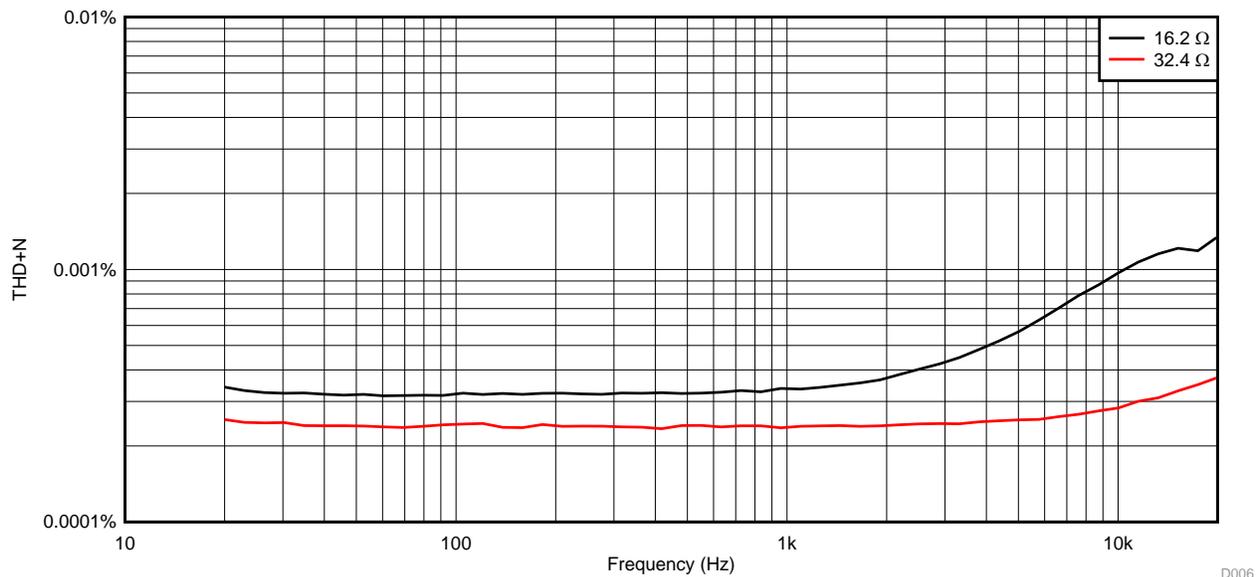


Figure 22. THD+N versus Frequency Graph for 100 mW of Output Power

Figure 23 shows the results for 10 mW of output power for 32.4-Ω and 16.2-Ω loads. At 20 kHz, the THD+N is 0.00072% (–102.85 dB) for a 32.4-Ω load and 0.00115% (–98.79 dB) for 16.2-Ω loads.

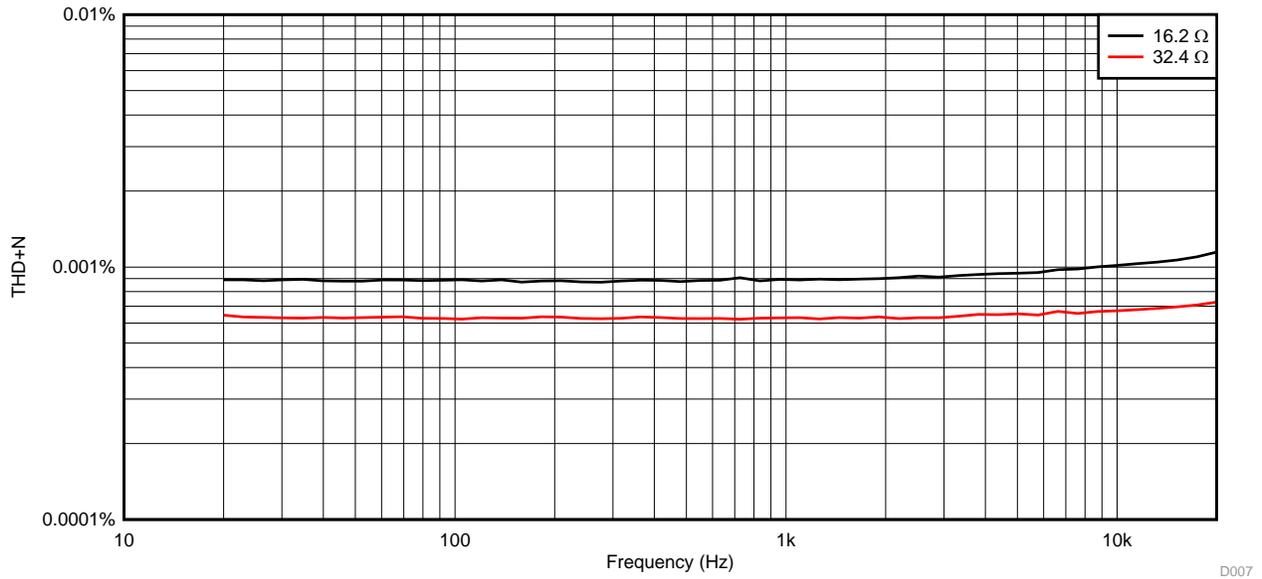


Figure 23. THD+N versus Frequency Graph for 10 mW of Output Power

7.4 Output Spectrum

Figure 24 and Figure 25 are Fast Fourier Transforms (FFTs) of the output signal when delivering 10 mW at 1 kHz to 32- Ω and 16- Ω loads. Plots such as these are useful for determining which harmonics are largest, which may impact the sound quality perceived by the listener. For the 32.4- Ω load, the 2nd and 3rd harmonics are of similar magnitude, -141.4 dBc (0.0000085%) and -141.9 dBc (0.000008%), respectively. Spurs visible in the spectrum at frequencies below 1 kHz are due to 60-Hz mains interference.

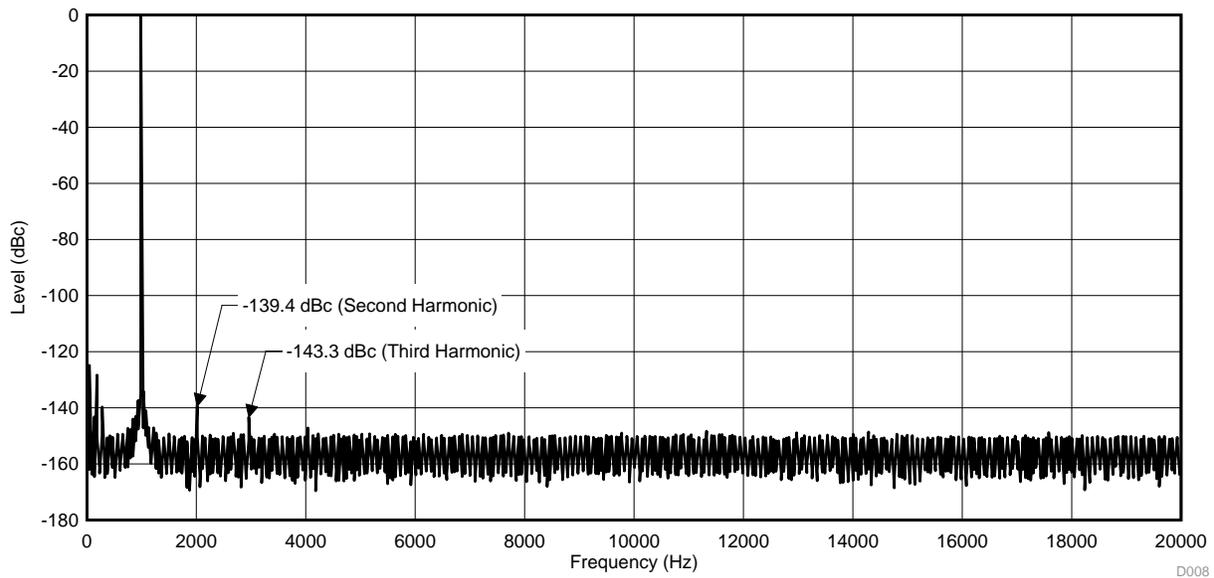


Figure 24. Output Spectrum of a 10-mW, 1-kHz, Sine Wave Into a 32.4- Ω Load

When the load impedance is decreased to 16.2 Ω , the 2nd harmonic becomes the dominant harmonic with a level of -139.3 dBc (0.0000108%).

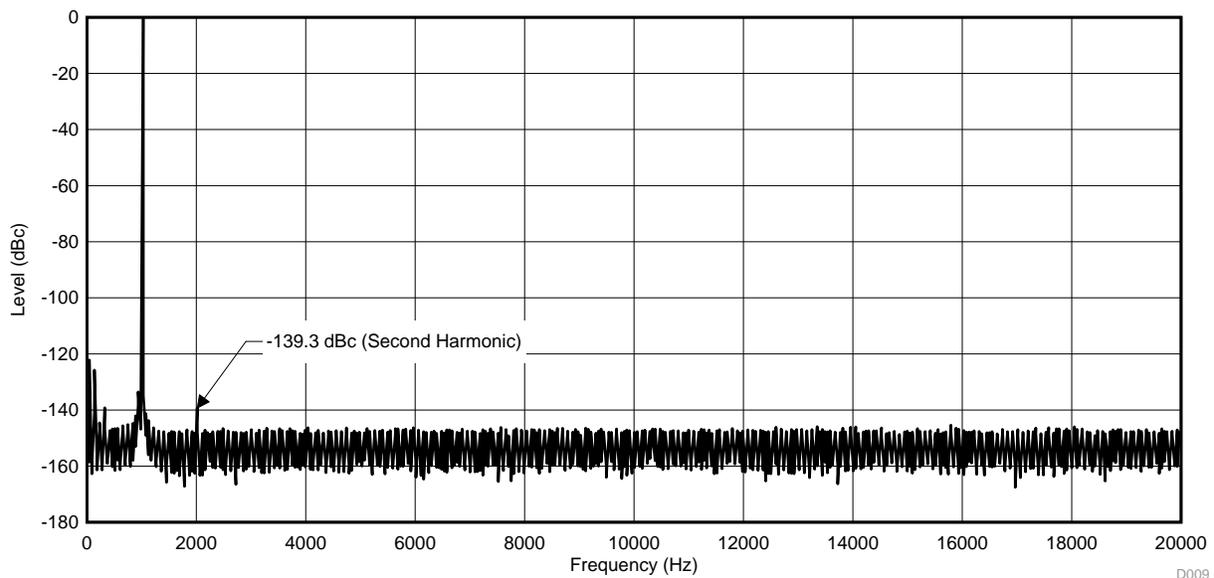


Figure 25. Output Spectrum of a 10-mW, 1-kHz, Sine Wave Into a 16.2- Ω Load

Figure 26 and Figure 27 show the output spectrum for a 1-kHz, 100-mW output signal into 32 Ω and 16- Ω loads. The 3rd harmonic is the dominant harmonic for the 32- Ω load at -132.2 dBc (0.000025%). The second harmonic is at -136.3 dBc (0.000015%). Additional higher-order harmonics become visible compared with the 10-mW output, but this is largely because the noise floor is lower with the higher output amplitude used to create the 100-mW output power.

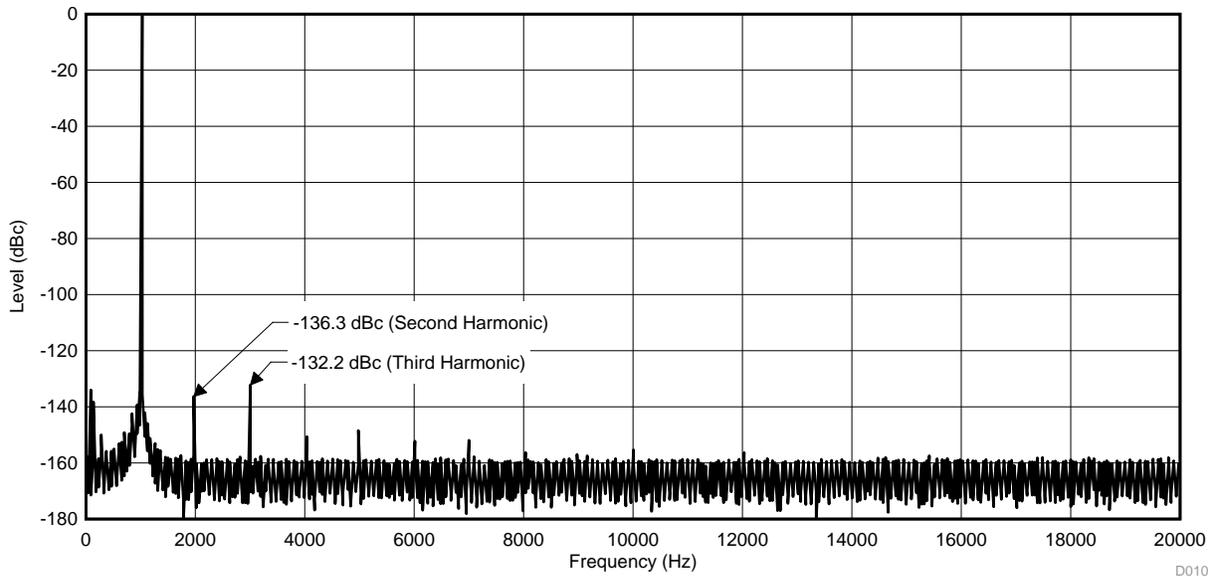


Figure 26. Output Spectrum of a 100-mW, 1-kHz, Sine Wave Into a 32.4- Ω Load

For the 16.2- Ω load, the 3rd harmonic is dominant with the 4th and 5th harmonics at similar levels. The 3rd is at -125.2 dBc (0.000055%). The 4th harmonic is at -128.8 dBc (0.000036%), and the 5th harmonic is at -128.5 dBc (0.000038%). The output current required to produce the 100-mW output into the 16.2- Ω loads begins to cause some output clipping, which results in the additional higher order harmonics observed compared with the 100 mW, 32- Ω output spectrum.

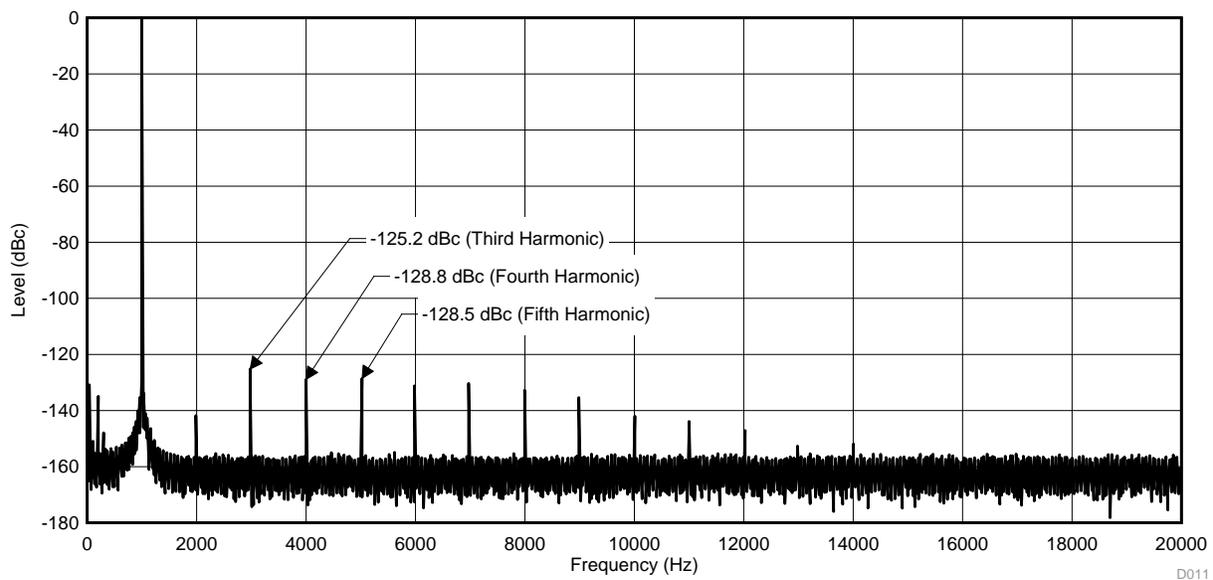


Figure 27. Output Spectrum of a 100-mW, 1-kHz, Sine Wave Into a 16.2- Ω Load

7.5 Verification With Real Headphones

Real headphones are not a resistive load. Over the operating frequency range their impedance may shift between inductive, capacitive, and resistive behavior. This impedance is also modulated by the cone movement and so at any instant in time the impedance of the driver depends on where the voice coil is in its range of motion. The end result is that the current drawn by headphones is not sinusoidal and will produce distortion for headphone amplifier circuits with non-zero output impedance[3]. Therefore, the performance of a headphone amplifier circuit must also be verified using real headphones as a load instead of resistors. A pair of over-the-ear headphones with a 32- Ω nominal impedance were used for testing in this section.

The THD+N was re-measured for increasing output power as shown in Figure 28. At 100 mW, the THD+N is 0.000144%, which is essentially unchanged from the results in Figure 20.

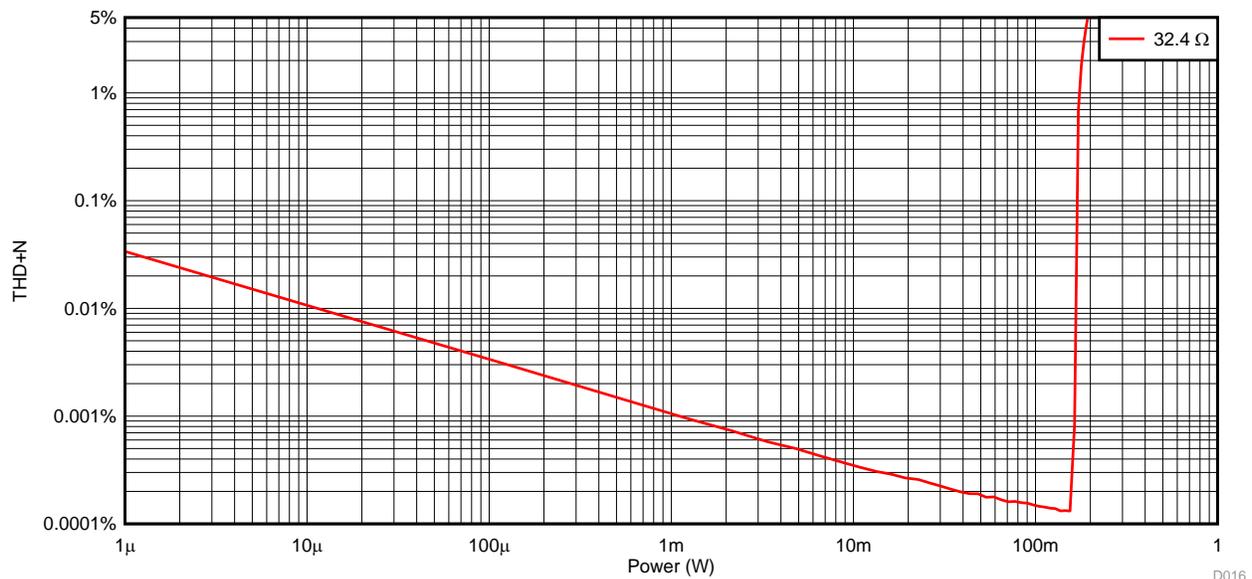


Figure 28. Measured THD+N versus Output Power in 32- Ω Headphones (1-kHz Signal)

In Figure 29, the THD+N over frequency was measured with 32-Ω headphones as a load. Above 200 Hz, the results are unchanged from Figure 23. However, at low frequencies the THD+N increases for the 100-mW and 150-mW output powers. The increase in THD+N is because at low frequencies the cone motion of the drivers in the headphones is much larger. Therefore, the current waveform in the headphones is much less sinusoidal. Because the output impedance of the headphone circuit is non-zero, the headphone current will produce some distortion. This effect is much larger in headphone amplifiers which have a resistor in series with the output.

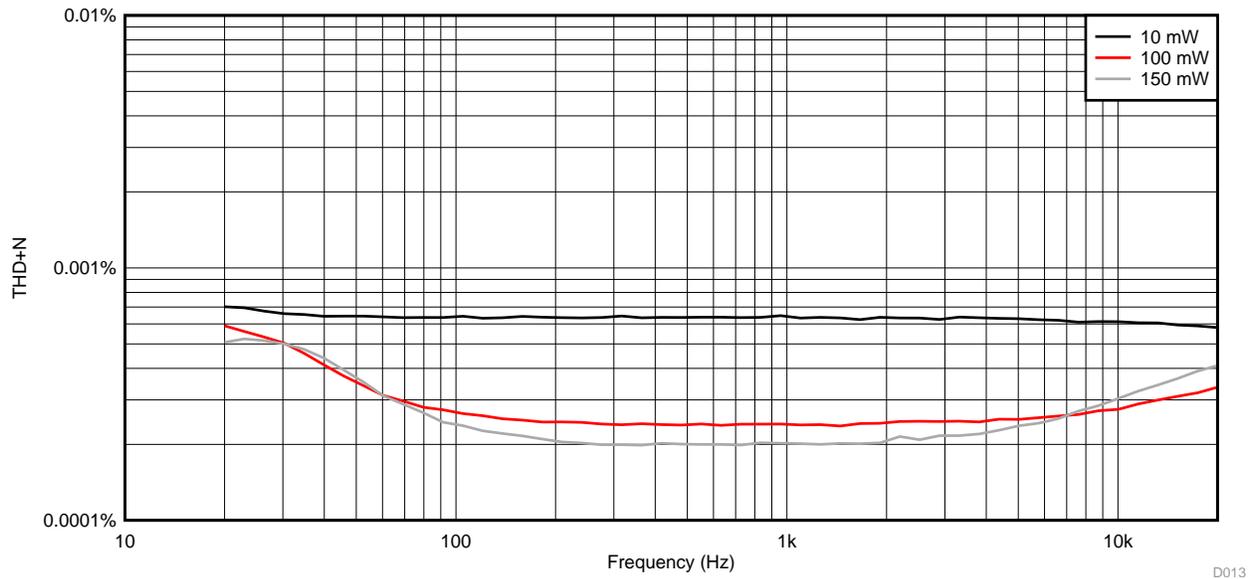


Figure 29. THD+N versus Frequency Graph for 10 mW, 100 mW, and 150 mW of Output Power

Figure 30 shows the output spectrum of a 10-mW, 1-kHz, sine wave into 32-Ω headphones. The 2nd harmonic remained the dominant harmonic at -141.4 dBc (0.0000085%), which is slightly lower than it was with the resistive load results shown in Figure 24. The 3rd harmonic is slightly higher in magnitude than the Figure 24 results at -141.9 dBc (0.000008%).

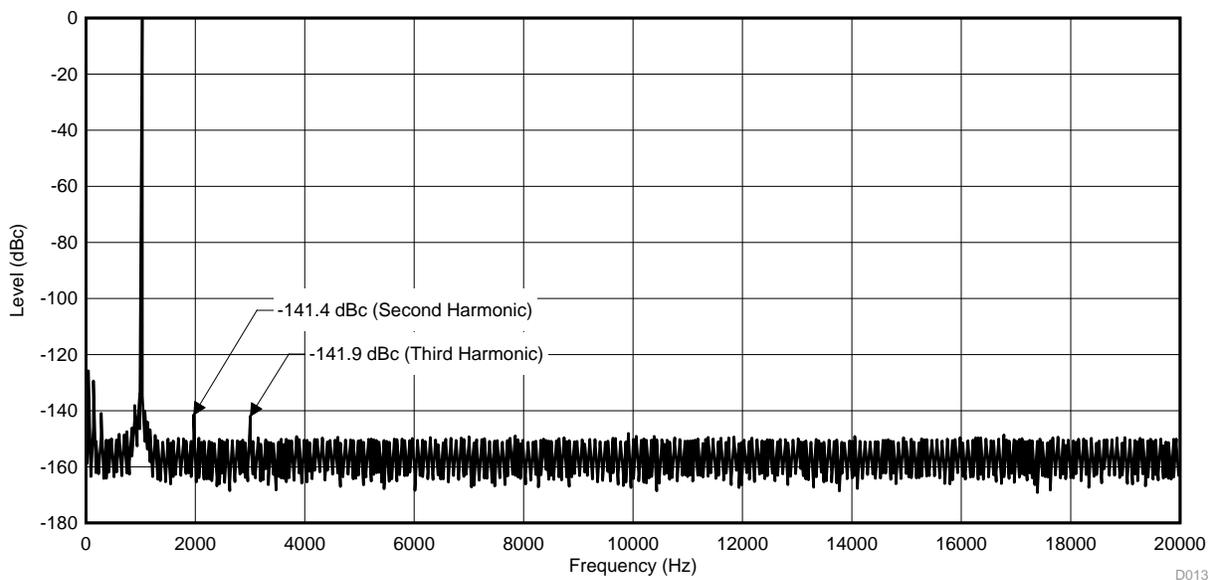


Figure 30. Output Spectrum of a 10-mW, 1-kHz, Sine Wave Into 32-Ω Headphones

Figure 31 shows the output spectrum of a 100-mW, 1-kHz, sine wave into the 32- Ω headphones. The 3rd harmonic matched the results in Figure 26 and was the dominant harmonic at -132.2 dBc (0.000025%). Similar to the results in Figure 30, the 2nd harmonic slightly improved to -137.2 dBc (0.000014%).

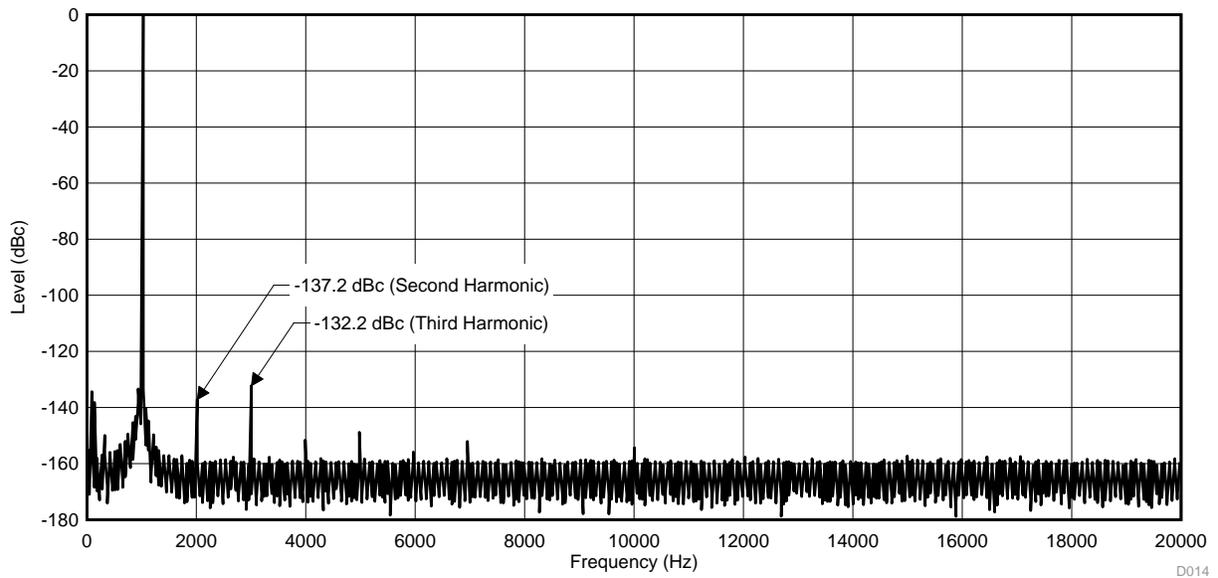


Figure 31. Output Spectrum of a 100-mW, 1-kHz, Sine Wave Into 32- Ω Headphones

8 Modifications

A number of modifications can be performed to this design to reduce cost, adjust audio performance, decrease power consumption, or change the output power. For example, the OPA1652 is available in the same 3-mm×3-mm SON-8 package as the OPA1612, and the OPA1652 may be used in the transimpedance amplifier stage for lower total power consumption and significantly reduced solution cost, but with slightly reduced audio performance.

8.1 THD+N versus Output Power

The performance of the OPA1652+OPA1622 solution was measured for comparison purposes to the original solution. Figure 32 shows the THD+N versus output power measured for a 1-kHz fundamental in a 22-kHz measurement bandwidth.

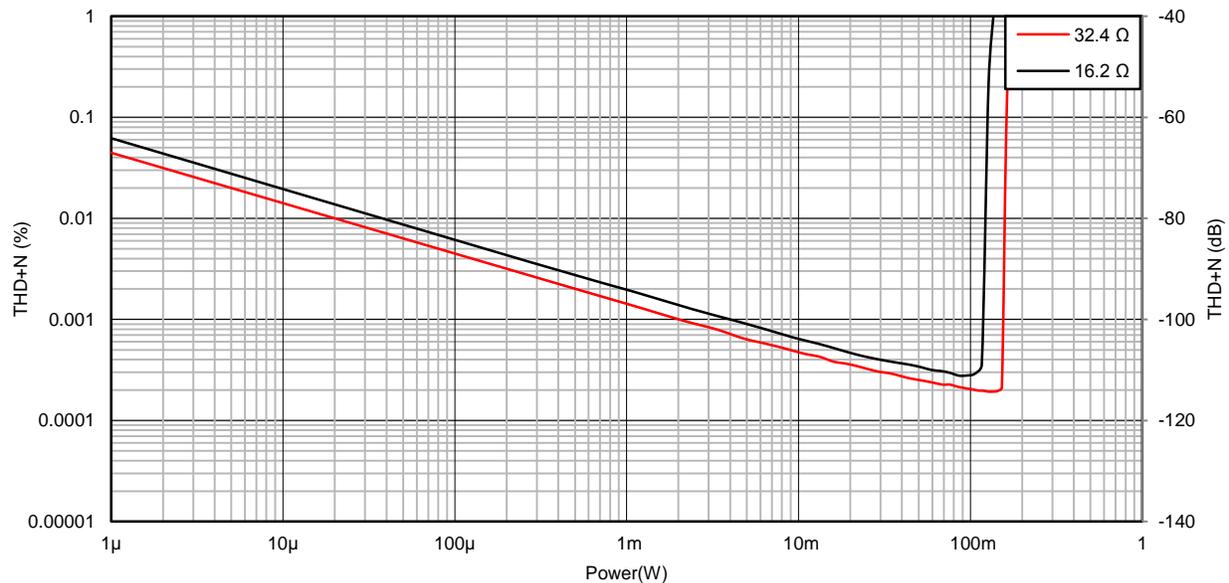


Figure 32. Measured THD+N versus Output Power (1-kHz Signal)

Table 8 compares the measured performance of the OPA1652 solution to the original version using the OPA1612. There is an approximately a 3-dB degradation in THD+N due to the higher voltage noise of the OPA1652 at the majority of the comparison points. Maximum output power is the same for both circuits because it is limited by the output amplifier (OPA1622), not the transimpedance amplifier.

Table 8. Comparison of Modified Solution Using OPA1652 in Transimpedance Stage to Original Solution Using OPA1612

TEST CONDITION	OPA1652 + OPA1622	OPA1612 + OPA1622
10 mW (16.2-Ω load)	0.00065% (–103.7 dB)	0.000496% (–106.1 dB)
10 mW (32.4-Ω load)	0.00046% (–106.7 dB)	0.00035% (–109.1 dB)
100 mW (16.2-Ω load)	0.00029% (–110.75 dB)	0.00021% (–113.6 dB)
100 mW (32.4-Ω load)	0.0002% (–113.98 dB)	0.000148% (–116.6 dB)
124 mW (16.2-Ω load)	0.00035 (–109.1 dB)	0.00035% (–109.1 dB)
156 mW (32.4-Ω load)	0.00021% (–113.6 dB)	0.000131% (–117.62 dB)

8.2 THD+N versus Frequency

The THD+N was measured from 20 Hz to 20 kHz at several different output power levels into 32.4- Ω and 16.2- Ω loads with a measurement bandwidth of 80 kHz. [Figure 33](#) displays the results for a 150-mW output power into a 32.4- Ω load. At 20 kHz, the THD+N is 0.00186% (–94.6 dB).

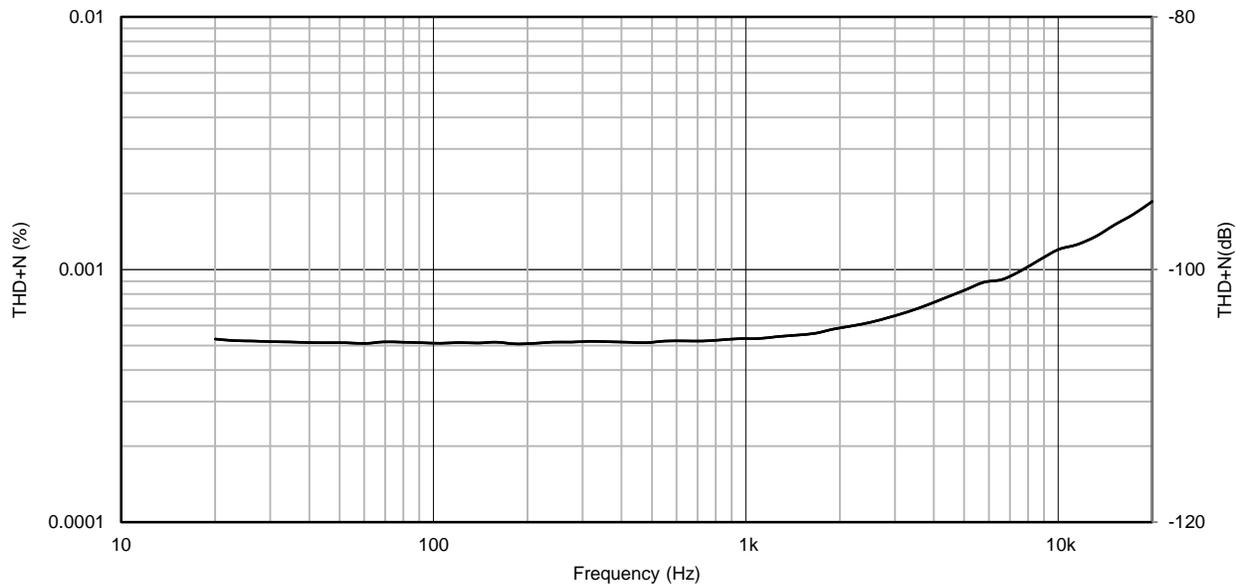


Figure 33. THD+N versus Frequency for 150-mW of Output Power Into a 32.4- Ω Load

[Figure 34](#) shows the results for 100 mW of output power for 32.4- Ω and 16.2- Ω loads. At 20 kHz, the THD+N is 0.0013% (–97.7 dB) for a 32.4- Ω load and 0.0022% (–93.15 dB) for 16.2- Ω loads.

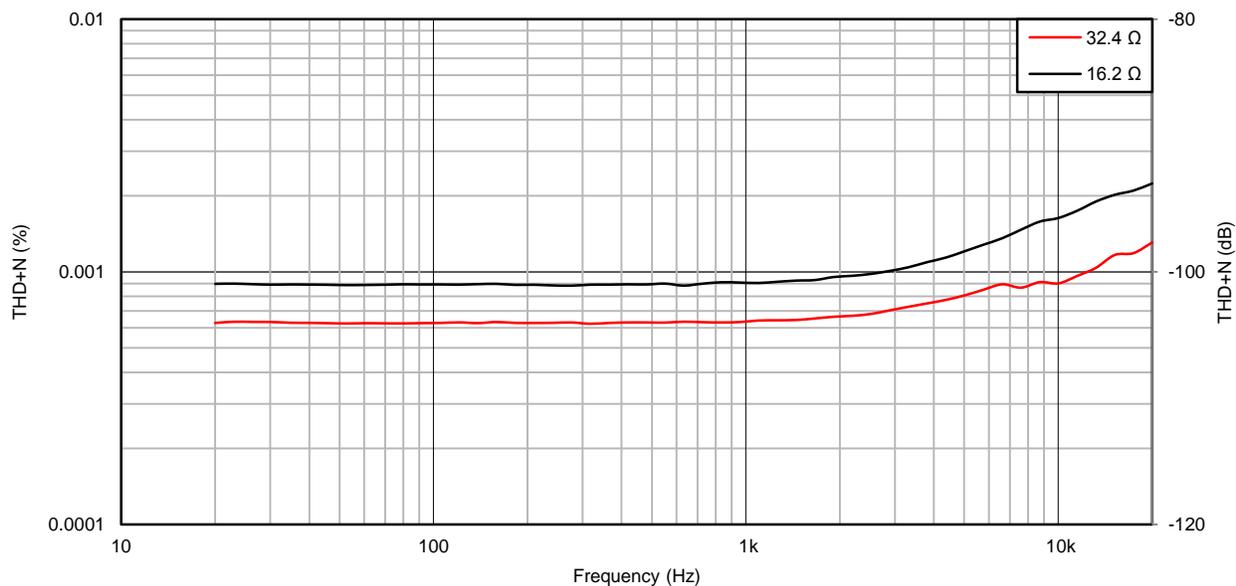


Figure 34. THD+N versus Frequency Graph for 100-mW Output Power

Figure 35 shows the results for 10 mW of output power for 32.4-Ω and 16.2-Ω loads. At 20 kHz, the THD+N is 0.0026% (–91.7 dB) for a 32.4-Ω load and 0.00297% (–90.53 dB) for 16.2-Ω loads.

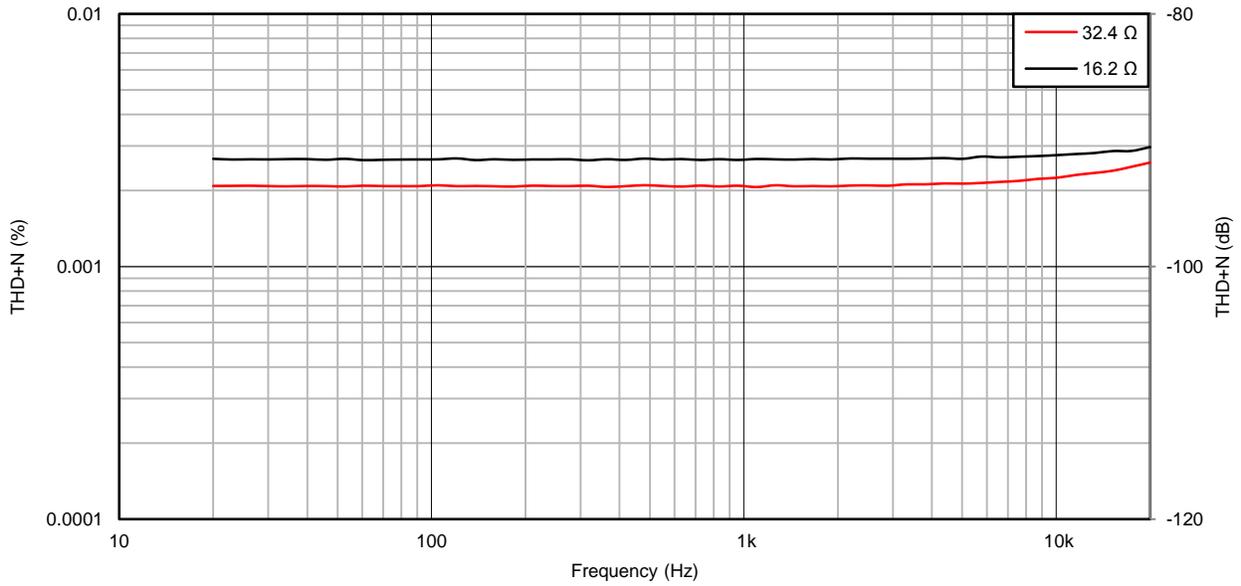


Figure 35. THD+N versus Frequency Graph for 10-mW Output Power

8.3 Output Spectrum

Figure 36 and Figure 37 are Fast Fourier Transforms (FFTs) of the output signal when delivering 10 mW at 1 kHz to 32- Ω and 16- Ω loads. For the 32.4- Ω load, the second and third harmonics are of similar magnitude, -122.8 dBc (0.000085%) and -122.3 dBc (0.000077%), respectively. Spurs visible in the spectrum at frequencies below 1 kHz are due to 60-Hz mains interference.

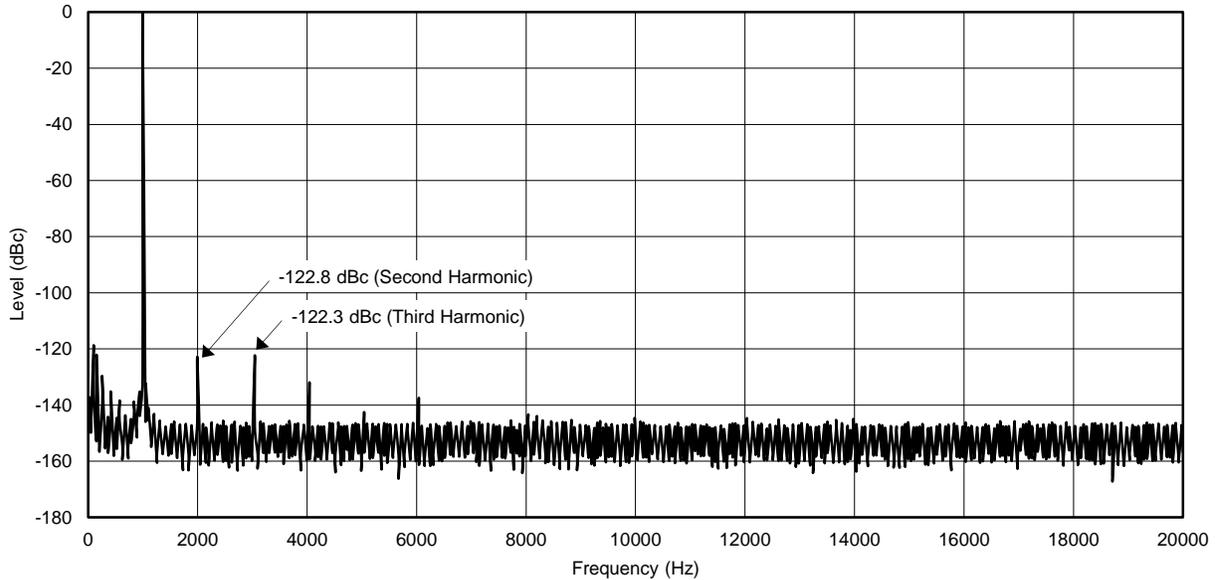


Figure 36. Output Spectrum of a 10-mW, 1-kHz, Sine Wave Into a 32.4- Ω Load

When the load impedance is decreased to 16.2 Ω , the second harmonic becomes the dominant harmonic with a level of -118.6 dBc (0.000117%).

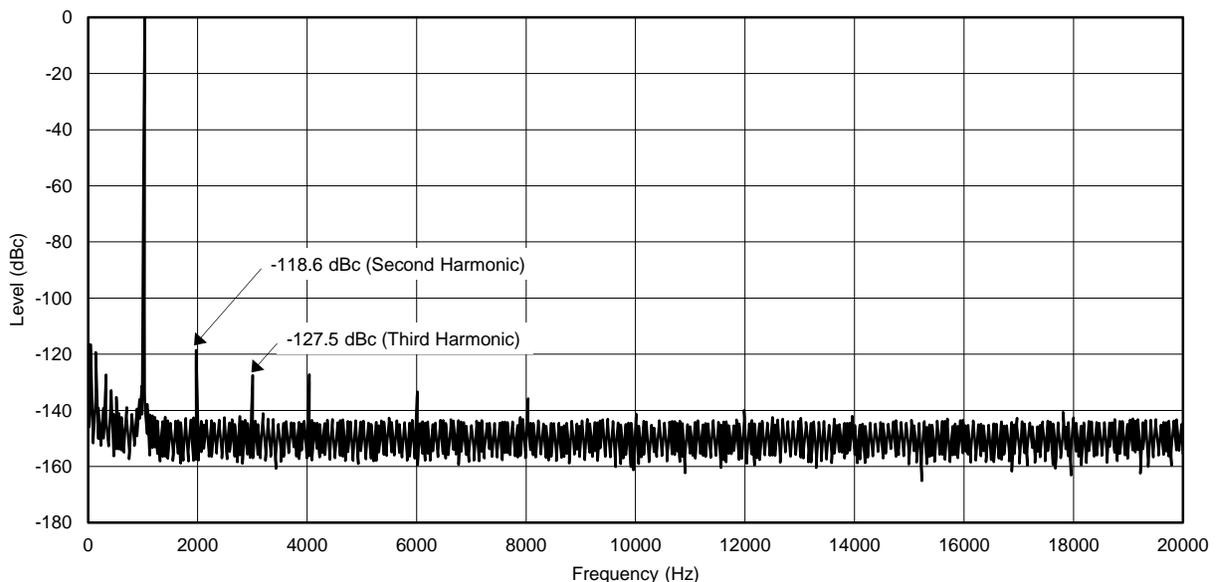


Figure 37. Output Spectrum of a 10-mW, 1-kHz, Sine Wave Into a 16.2- Ω Load

Figure 38 and Figure 39 show the output spectrum for a 1-kHz, 100-mW output signal into 32-Ω and 16-Ω loads. The second harmonic is the dominant harmonic for the 32-Ω load at -123.6 dBc (0.000066%). The third harmonic is at -125.4 dBc (0.000054%). Additional higher-order harmonics become visible compared with the 10-mW output.

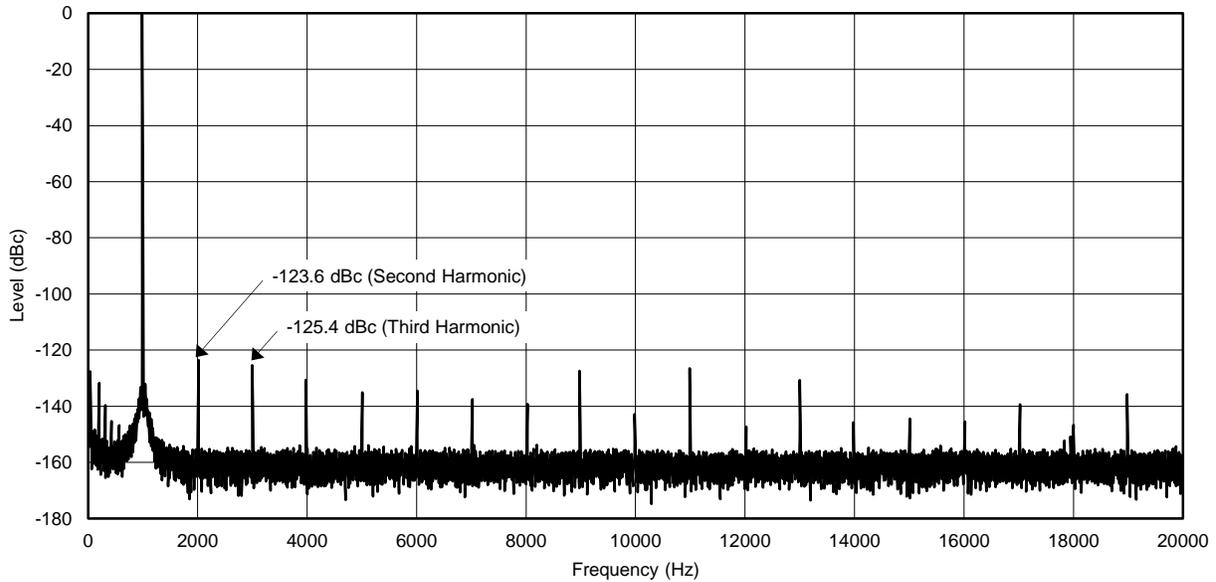


Figure 38. Output Spectrum of a 100-mW, 1-kHz, Sine Wave Into a 32.4-Ω Load

For the 16.2-Ω load, the second harmonic is dominant with the third, fourth, and fifth harmonics at similar levels. The second harmonic is at -120.3 dBc (0.000097%).

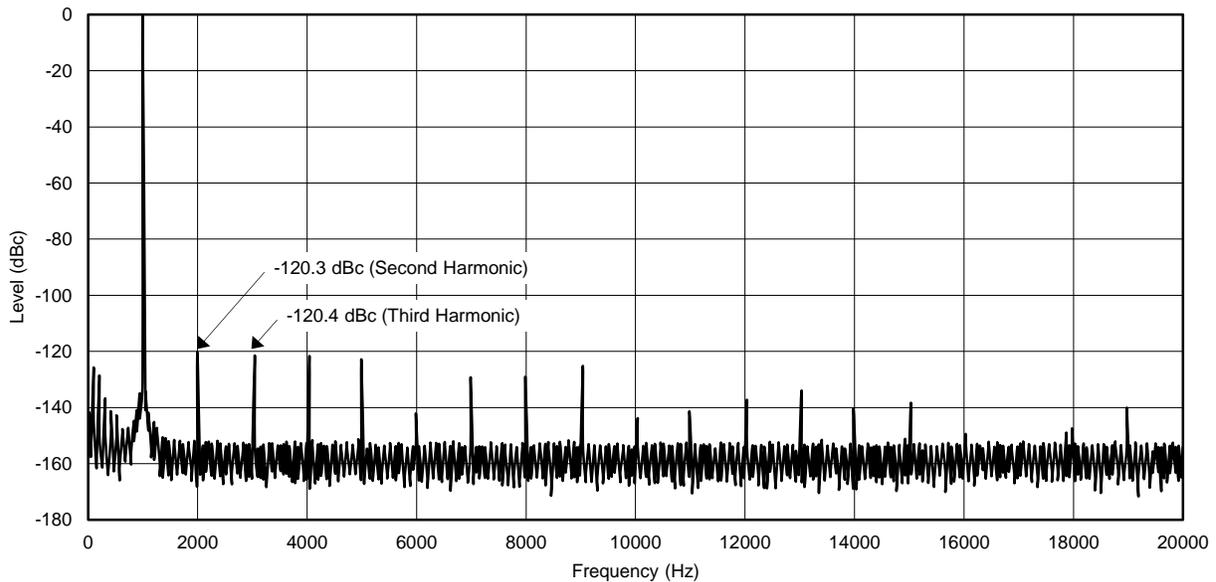


Figure 39. Output Spectrum of a 100-mW, 1-kHz, Sine Wave Into a 16.2-Ω Load

9 Bill of Materials

To download the bill of materials (BOM), see the design files at [TIPD177](#).

Table 9. BOM

ITEM	DESIGNATOR	QTY	VALUE	PART NUMBER	MANUFACTURER	DESCRIPTION
1	C1, C2, C12, C13	4	100 pF	GRM1885C1H101JA01D	MuRata™	CAP, CERM, 100 pF, 50 V, ± 5%, C0G/NP0, 0603
2	C3, C4, C14, C15	4	560 pF	GRM1885C1H561JA01D	MuRata	CAP, CERM, 560 pF, 50 V, ± 5%, C0G/NP0, 0603
3	C5	1	2.2 μF	GRM316R61E225KA12D	MuRata	CAP, CERM, 2.2 μF, 25 V, ± 0%, X5R, 1206
4	C6, C7	2	10 μF	C3216X5R1C106M	TDK™	CAP, CERM, 10 μF, 16 V, ± 20%, X5R, 1206
5	C8 – C11, C16, C17	6	0.1 μF	GRM188R71H104KA93D	MuRata	CAP, CERM, 0.1 μF, 50 V, ± 10%, X7R, 0603
6	H1 – H4	4		NY PMS 440 0025 PH	B&F Fastener Supply™	Machine Screw, Round, #4-40 × 1/4, Nylon, Philips panhead
7	H5 – H8	4		1902C	Keystone	Standoff, Hex, 0.5"L #4-40 Nylon
8	J1	1		39544-3004	Molex™	Terminal Block, 4 × 1, 5.08 mm, TH
9	J2	1		5-146261-1	TE Connectivity	Header, 100 mil, 2 × 1, Gold, TH
10	J3, J8	2		PBC03SAAN	Sullins Connector Solutions®	Header, 100 mil, 3 × 1, Gold, TH
11	J4, J7	2		112404	Amphenol Connex™	Connector, TH, BNC
12	J5	1		ED555/3DS	Onshore Technology™	Terminal Block, 3.5 mm Pitch, 3 × 1, TH
13	J6	1		SJ-3523-SMT	CUI Inc.™	Audio Jack, 3.5 mm, Stereo, R/A, SMT
14	LBL1	1		THT-14-423-10	Brady™	Thermal Transfer Printable Labels, 0.650" W × 0.200" H - 10,000 per roll
15	R1, R2, R13, R14	4	2.32 k	RT0603BRD072K32L	Yageo America™	RES, 2.32 k, 0.1%, 0.1 W, 0603
16	R3, R4, R15, R16	4	1.58 k	RT0603BRD071K58L	Yageo America	RES, 1.58 k, 0.1%, 0.1 W, 0603
17	R5, R6, R17, R18	4	560 k	RG1608P-561-B-T5	Susumu Co Ltd™	RES, 560, 0.1%, 0.1 W, 0603
18	R7	1	24.9 k	RT0603BRD0724K9L	Yageo America	RES, 24.9 k, 0.1%, 0.1 W, 0603
19	R8	1	14.7 k	RT0603BRD0714K7L	Yageo America	RES, 14.7 k, 0.1%, 0.1 W, 0603
20	R9 – R12, R19 – R22	8	0	CRCW06030000Z0EA	Vishay-Dale™	RES, 0, 5%, 0.1 W, 0603

10 Software Files

To download the software files, see the design files at [TIDP177](#).

11 References

1. *Signal Distortion From High-K Ceramic Capacitors*, <http://www.edn.com/design/analog/4416466/Signal-distortion-from-high-K-ceramic-capacitors>.
2. *More About Understanding the Distortion Mechanism of High-K MLCCs*, <http://edn.com/design/analog/4426318/More-about-understanding-the-distortion-mechanism-of-high-K-MLCCs>.
3. *The Sonic Advantages of Low-Impedance Headphone Amplifiers*, http://benchmarkmedia.com/blogs/application_notes/11653109-the-0-ohm-headphone-amplifier.

12 About the Authors

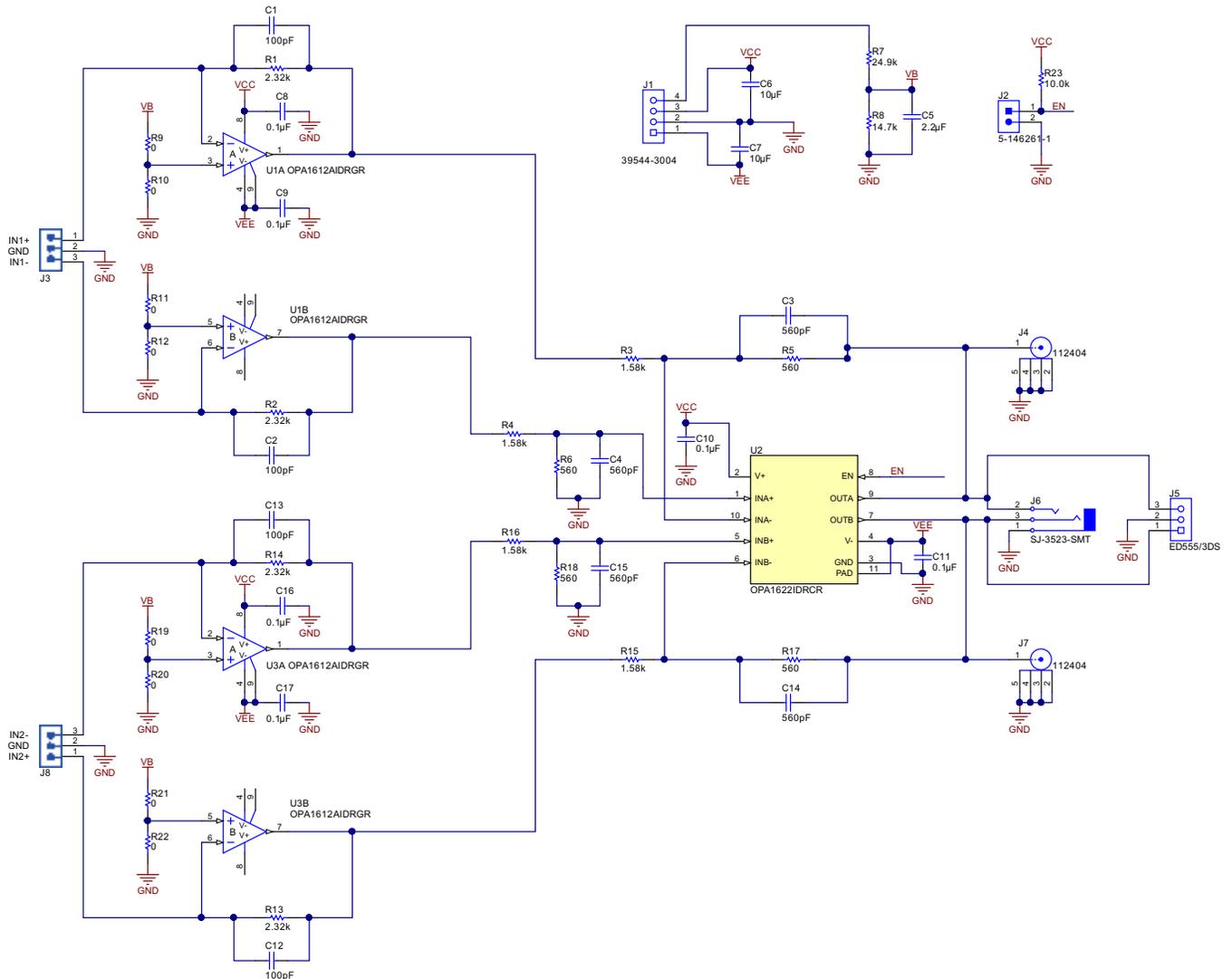
JOHN CALDWELL is a systems engineer with TI Precision Analog, where he develops operational amplifiers for audio applications. He specializes in precision circuit design for sensors, low-noise design and measurement, and electromagnetic interference issues. He received his MSEE and BSEE from Virginia Tech with a research focus on biomedical electronics and instrumentation. Prior to joining TI in 2010, John worked at Danaher Motion and Ball Aerospace.

COLLIN WELLS is an applications engineer in the Precision Analog group at TI where he supports industrial products and applications. Collin received his BSEE from the University of Texas, Dallas.

Appendix A

A.1 Electrical Schematic

Figure 40 shows the electrical schematic.



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Figure 40. Electrical Schematic

Revision C History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from B Revision (September 2016) to C Revision	Page
• Changed Section 8 introduction	31
• Added Section 8.1	31
• Added Section 8.2	32
• Added Section 8.3	34

Revision B History

Changes from A Revision (July 2016) to B Revision	Page
• Changed THD+N value from the incorrect 0.00148% to the correct 0.000148%	1
• Changed goal of THD+N (1 kHz, 100 mW, 16 Ω and 32 Ω) from < 0.005%	2
• Added reference footnote	28
• Changed link to <i>More About Understanding the Distortion Mechanism of High-K MLCCs</i>	37

Revision A History

Changes from Original (December 2014) to A Revision	Page
• Deleted Circuit Description from front page and added as Section 1	1
• Added OPA1622 to Design Resources	1
• Added Design Features	1
• Added Featured Applications	1
• Added the "THD + N (1 kHz, 100 mW, 16 Ω and 32 Ω)" row to Table 1	2
• Changed from > 50 mW	2
• Changed from "55 mW (32 Ω), 51.7 mW (16 Ω)"	2
• Changed resistor value from 830 Ω to 806 Ω	4
• Changed resistor value from 830 Ω to 806 Ω , changing the answer from 1.836 mA _p to 1.891467 mA _p	4
• Changed R _F from 2370 Ω to 2320 Ω	5
• Changed resistor values in Figure 5	6
• Changed V _{Bias} value from 1.222 to 1.225	6
• Changed resistor values in Figure 6	6
• Changed resistors from R14 and R16 to R7 and R8, respectively	7
• Changed capacitor from C13 to C5	7
• Changed resistors and capacitors featured in Figure 7	7
• Changed V _{DIFF} from 5.7108 V _{RMS} to 6.206 V _{RMS}	8
• Changed A from 0.21503 V/V to 0.3545 V/V	8
• Changed C ₃ , C ₄ value from 820 pF to 560 pF	8
• Deleted Section 2.4: Parallel Output Driver	8
• Changed feedback resistors in transimpedance amplifiers (from "R1, R9" to "R1, R2") and difference amplifier (from "R2, R5, R7, R11" to "R3, R4, R5, R6")	9
• Added OPA1622 to Table 3	9
• Added OPA1622 to Table 4	10
• Added OPA1622 to Table 5	10
• Deleted Table 5: A comparison of the predicted THD+N(%) of several audio op amps	11
• Changed magnitude response from -0.0095 dB to -0.0105 dB and phase deviation from -3.83 degrees to -4.02 degrees	13
• Added Section 5.2: Transient Response	14

• Added predicted RMS noise voltage for a 22-kHz bandwidth	15
• Changed predicted RMS noise voltage for a 80-kHz bandwidth from 1.65 μV_{RMS} to 2.58 μV_{RMS}	15
• Changed Figure 12 to focus on the 22-kHz bandwidth instead of the 80-kHz bandwidth	15
• Changed predicted THD+N values for both load impedances	16
• Added Table 7 : Predicted Noise-Dominated THD + N Values for 100 mW of Output Power Into 16 Ω and 32 Ω Loads .	16
• Changed Figure 14 : Magnitude and Phase Response of the Difference Amplifier Loop	18
• Deleted Section 4.4: Stability-Parallel Output Amplifier	18
• Added Mid Layer 1 (Left) and Mid Layer 2 (Right) of the PCB to Section 6.1.1	20
• Changed magnitude response from 0.007 dB to 0.0088 dB	22
• Changed phase deviation from 4.06° to 4.02°	22
• Changed THD+N value from 0.00052% to 0.000350% for a 32.4- Ω load, and 0.00078% to 0.000496% for a 16.2- Ω load	23
• Added "THD + N versus Frequency Graph for 150-mW of Output Power" and "THD + N versus Frequency Graph for 100 mW of Output Power"	24
• Changed the 32.4- Ω load 2nd and 3rd harmonics from -124.37 dB and -125.05 dB to -141.4 dBc and -141.9 dBc	26
• Changed the 16.2- Ω load 2nd harmonic from -117.1 dB to -139.3 dBc	26
• Added output spectrum for a 1-kHz, 100-mW output signal	27
• Added information of the output spectrum of a 100-mW, 1-kHz, sine wave and Figure 31	30
• Added Collin Wells to Section 12	37

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